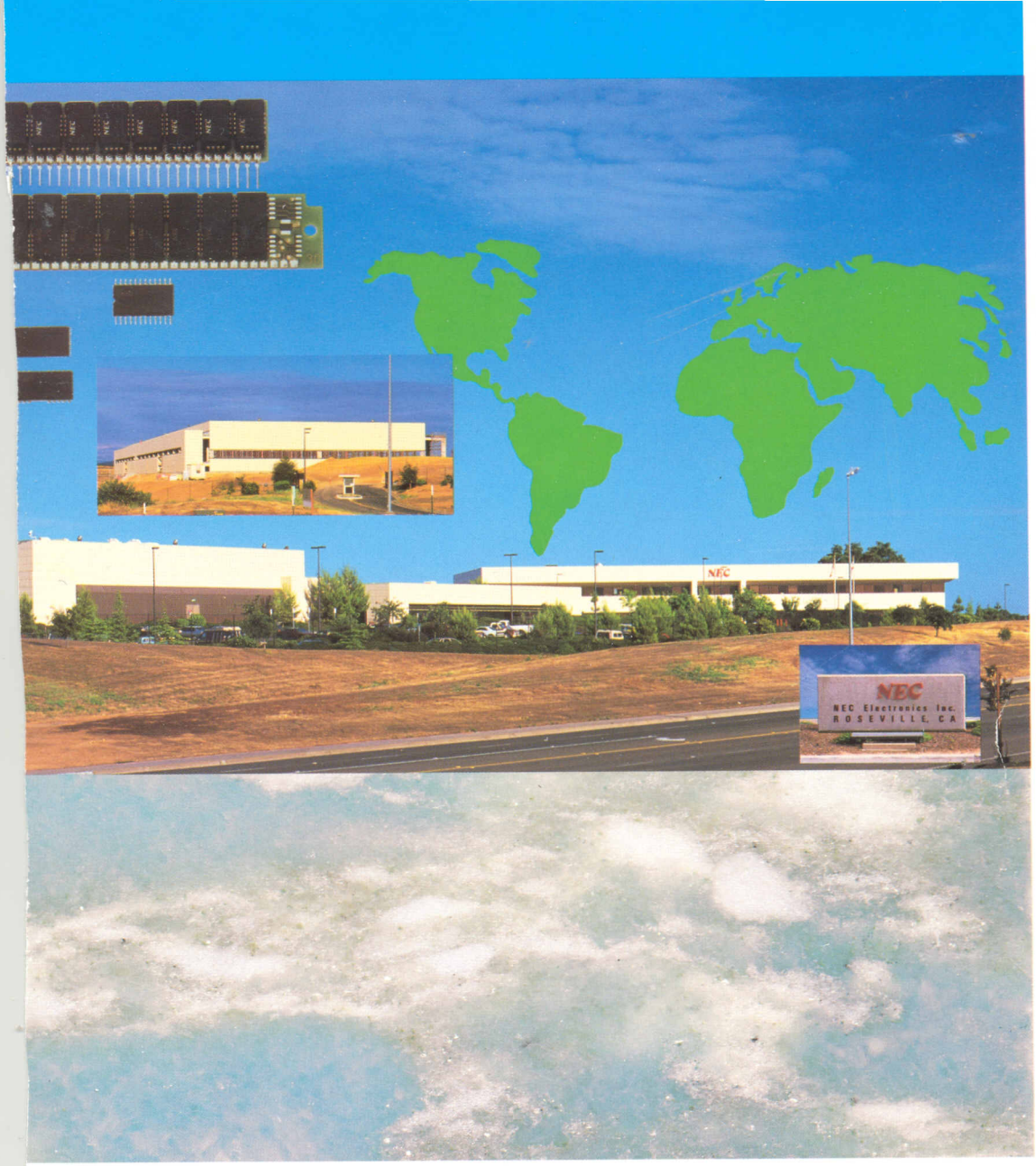


MEMORY PRODUCTS DATA BOOK

NEC

NEC Electronics Inc.

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1991
MEMORY PRODUCTS
DATA BOOK

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Front Cover Photo

NEC Electronics' fabrication, testing and assembly factory in Roseville, California, is expanding to become one of the most advanced facilities in the United States. The new buildings shown in the inset will quadruple the total plant area, allowing for approximately 30% of total revenue to be derived from products manufactured in the United States.

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Introduction

This 1991 edition of the *MEMORY PRODUCTS DATA BOOK* contains the most current information available at the time of printing. Please contact your local representative of NEC Electronics Inc. to stay informed of upcoming releases. Additional products in development but not yet announced are referred to below. The addition of these products to our memory line, already the broadest in the industry (and briefly described in this section), means that NEC is able to offer an even greater selection of device types, configurations, and packaging options in each of the major memory groups.

Among our new application-specific products are high performance devices for graphics, video/TV, image processing, data processing, and other specialized applications. The μPD42275, for example, expands our leadership line of 1-Mbit video buffers with an 8-bit organization that provides increased bandwidth for high-end applications as well as a low-cost, best-fit solution for low-end graphics systems. Our 256K video buffer capabilities have been extended with the CMOS-fabricated μPD42264. Densities beyond 1 Mbit will be announced in 1991. The μPD42272 picture-in-picture generator provides an easy design path for simultaneous viewing of multiple screens in television, imaging, and security systems. The μPD42271 provides the same functions, minus the colored border of the inset picture. In 1991, you can also expect new field buffer and silicon file products and modules based on video buffers.

In building on our position as an industry leader in the production of latest-generation DRAMs, we have focused our attention on developing products with higher density, lower power consumption, and faster access times. Our 1-Mbit CMOS DRAMs are now available in 60 ns versions. Write-per-bit options are also offered. NEC's recently released 4-Mbit CMOS DRAMs—the μPD424100, μPD424101, μPD424102, μPD424400, μPD424402, μPD424410, μPD424412, and μPD424800-series—reflect the trend toward higher integration and continue NEC's advances in high-volume manufacturing of fast DRAMs. These 4-Mbit DRAMs will be the key devices produced in our new factory addition in Roseville, California (see description elsewhere in this section). TSOP packages will also eventually be offered on DRAMs of 1 Mbit or greater, and 300-mil SOJ packaging will be available for 4-Mbit DRAMs by 1991.

A family of modules based on our 1- and 4-Mbit DRAMs is being offered with 8-, 9-, 36- or 40-bit organizations and either leaded or socket-mountable mounting options. Single Inline Memory Module (SIMM™) packaging enhances reliability and reduces the size, weight and cost of a system, providing the same high performance at the module level as at the device level. The DRAM product family will be extended in 1991 to include new SIMM modules, additional DRAMs of 8 data bits or more, and new 16-Mbit DRAMs with a variety of operating features and data bus widths.

An increasing demand for enlarged program and data memory in point-of-sale systems, numerically controlled machining systems, hand-held computers, portable terminals and word processors has led to our development of low-power static CMOS RAMs, all of which feature advanced circuitry, a short-channel silicon-gate fabrication process, fast access times, and fully static operation (with no clock or refreshing). Densities through 1Mbit are now available in this family, as is the popular new TSOP package. Density will increase to 4 Mbits and beyond in our byte-wide SRAMs.

NEC has continued to develop more efficient, super high-speed products for use as cache memory, main memory, and control storage memory in workstations, file servers, mainframe computers and IC testers, as evidenced by our announcement of 17 new fast CMOS and BiCMOS SRAMs and bipolar ECL RAMs. These devices are available in densities through 1 Mbit, with data bus widths of up to 20 bits for cache applications. Additional products, through 4 Mbits for CMOS and 1 Mbit for ECL-compatible BiCMOS, are in development.

SIMM is a trademark of Wang Laboratories.

Our family of EPROMs has also been expanded to include higher density products offering greater integrity, improved programming features, and a considerable savings in both operating and standby power. Our fast 1-, 2- and 4-Mbit EPROMs are in production now; samples of even high density versions will be available in 1991. The μPD27HC65 is our first product offered as a low-cost replacement of high-speed bipolar PROMs. Our EEPROMs now span the range of densities from 4 to 256 Kbits; additional devices will be announced later. Low-profile TSOP and WSOP packages are offered on NEC's EPROMs and EEPROMs.

Six new mask-programmable ROMs featuring very large capacity (as high as 16 Mbits) and either 8- or 16-bit organization have been developed in response to the growing demand for storing greater quantities of data on one chip, e.g., dictionary and thesaurus data, embedded application routines and data for portable computers and electronic games, and large-size character sets/fonts. Future efforts in this area will concentrate on producing denser and faster speed versions for these applications.

Two memory cards based on SRAM technology are also being offered. Future products will cover additional densities and additional memory types—ROM and EPROM.

This 1991 *MEMORY PRODUCTS DATA BOOK* is for your reference. The most complete information available at the time of printing is included, but several new devices or enhancements will be available very soon. Please refer to the table below for imminent products which will require follow-up action for your consideration of the latest from NEC. If you need further assistance, please contact one of the sales offices listed in the back of this book. Our field applications engineers or technology center personnel will be happy to assist you.

Additional New Product Information

Device Number	Description	Comments
Application-Specific Devices		
μPD42273	256K x 4-bit dual-port graphics buffer	New speed of 80 ns
μPD42274	256K x 4-bit dual-port graphics buffer with flash write option	New speed of 80 ns
MC-42256D32V	256K x 32-bit dual-port graphics buffer SIMM with flash write option	80 pins, leaded, zig-zag configuration
MC-42601EA9B-60L	1M x 9-bit silicon file SIMM	30 pins, socket-mountable
μPD42271	7568 x 18-bit picture-in-picture generator	Same as μPD42272, except no colored frame on inset picture
μPD42641	4M x 1-bit silicon file	New in first half of 1991, with speeds to 80 ns
μPD42644	1M x 4-bit silicon file	New in first half of 1991, with speeds to 80 ns
Dynamic RAM Modules		
MC-42256AE9	256K x 9-bit fast-page SIMM	Three-piece solution, with speeds to 70 ns
MC-424256AE36	256K x 36-bit fast-page SIMM	One-inch height, with speeds to 70 ns
MC-424512AE36	512K x 36-bit fast-page SIMM	One-inch height, with speeds to 70 ns
MC-421000A36xD	1M x 36-bit fast-page SIMM	One-inch height, with speeds to 70 ns
MC-424512AA40	512K x 40-bit fast-page SIMM	Speeds to 60 ns
MC-421000AA40	1M x 40-bit fast-page SIMM	Speeds to 70 ns
MC-422000AA40	2M x 40-bit fast-page SIMM	Speeds to 70 ns
Dynamic RAMs		
μPD421000/1/2	1M x 1-bit; TSOP packaging	New package (GX suffix)
μPD424256/258/266/268	256K x 4 bits; TSOP packaging	New package (GX suffix)
μPD424100/1/2	4M x 1-bit DRAM enhancements	New speeds of 60 and 70 ns; new 300-mil SOJ (LA suffix); new TSOP package (Gx suffix)
μPD424400/402/410/412	1M x 4-bit DRAM enhancements	New speeds of 60 and 70 ns; new 300-mil SOJ package (LA suffix); new TSOP package (Gx suffix)

Additional New Product Information (cont)

Device Number	Description	Comments
μPD424802	512K x 8-bit static-column DRAM	Speeds to 70 ns; SOJ and ZIP packaging
μPD424810	512K x 8-bit fast-page DRAM with write-per-bit option	Speeds to 70 ns; SOJ and ZIP packaging
μPD424812	512K x 8-bit static-column DRAM with write-per-bit option	Speeds to 70 ns; SOJ and ZIP packaging
μPD42xxxx	Various 256K x 16-bit DRAMs	40-pin SOJ, samples first half 1991
Static RAMs		
μPD4361	64K x 1-bit	New speeds to 12 ns
μPD4362	16K x 4 bits	New speeds to 12 ns
μPD4363	16K x 4 bits, with $\overline{OE}$	New speeds to 12 ns
μPD4368	8K x 8 bits	New device, with speeds to 15 ns
μPD4369	8K x 9 bits	New device, with speeds to 15 ns
μPD43251	256K x 1 bit	New speeds to 15 ns
μPD43253	64K x 4 bits, with $\overline{OE}$	New device, with speeds to 15 ns
μPD43254	64K x 4 bits	New speeds to 15 ns
μPD43258	32K x 8 bits	New speeds to 20 ns
μPD43259	32K x 9 bits	New device
EPROMs		
μPD27C1000A	128K x 8 bits, ROM-compatible, WSOP packaging	New package (B suffix)
μPD27C1001A	128K x 8 bits, JEDEC-compatible, WSOP packaging	New package (B suffix)
μPD27C2001	256K x 8 bits, WSOP packaging	New speed of 120 ns and new package (B suffix)
μPD27C4000	256K x 16 bits or 512K x 8 bits	New device, with speeds to 150 ns
μPD27C4096	256K x 16 bits	New device, with speeds to 120 ns
EEPROMs		
μPD28C64	8K x 8 bits, TSOP packaging	New package (GX suffix)
Mask-Programmable ROMs		
μPD23C2001E	256K x 8 bits	New device, with speed of 200 ns
μPD23C4001EA	512K x 8 bits	New speed of 200 ns
μPD23HC4001E	512K x 8 bits	New device, with speed of 100 ns

Manufacturing in Roseville, California

NEC Electronics Inc. has been successfully providing the American market with high quality semiconductors and electronic components since 1979. As a subsidiary of Tokyo-based NEC Corporation, NEC Electronics is the company's commitment to the growing requirements of the U.S. market for electronic devices.

A quarter of a century ago, NEC Corporation put into place a strategy for globalization. Through a carefully planned process, the company has moved from placing sales offices throughout the world to opening manufacturing plants, design centers, and research and development facilities in key markets.

NEC's global strategy in the semiconductor industry is based on providing customers worldwide with competitive products. In putting this philosophy in practice, the company has recognized the need to "localize" the development and manufacturing functions by getting closer to the customer. NEC Electronics' operations in the United States can be viewed as an example of how the company has implemented its globalization strategy.

NEC Electronics Inc., headquartered in Mountain View, California, opened its first manufacturing facility in 1984 in Roseville, California. As the first Japanese company to make a major investment in the United States in the production of semiconductor devices, beginning with 64K DRAMs, NEC Electronics quickly moved to the production of 256K DRAMS in 1985. Today the facility is still producing high quality 256K DRAMs in a number of different package types to meet the needs of its U.S. customers. Additionally, the Roseville plant also produces microprocessors and application-specific integrated circuits (ASICs).

The success of the Roseville facility can be attributed to its excellent process technology and to the outstanding performance of its employees, who place their primary emphasis on manufacturing high quality, reliable products on time. The plant operates with a "zero defects" policy and its employees take pride in reaching this goal.



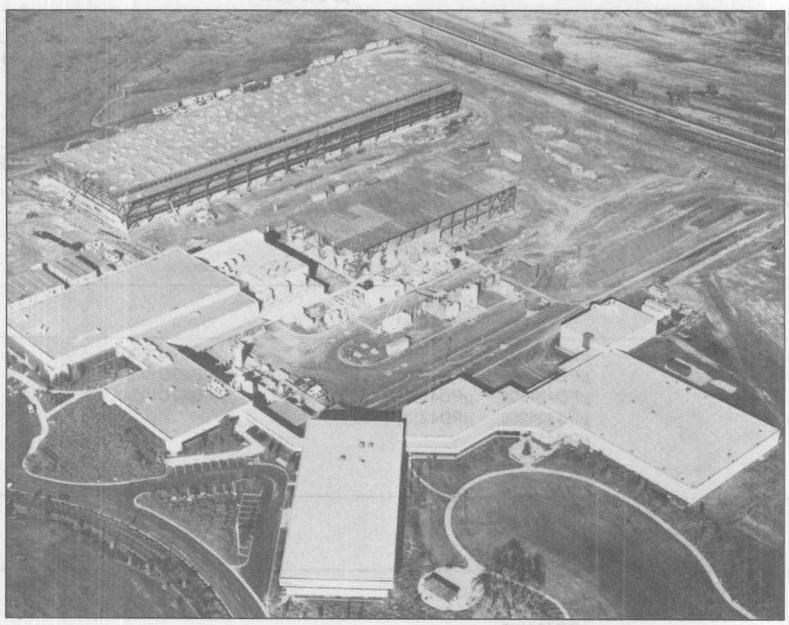
NEC Electronics' Roseville, California, manufacturing facility prior to expansion. This 200,000-square-foot facility currently fabricates 256K DRAMs, 256K dual-port graphics buffers, microprocessors and application-specific integrated circuits (ASICs).

The plant currently employs more than 700 employees in fabrication, test, assembly, engineering and administrative functions in its 200,000-square-foot facility. In addition to providing customers with a "local" source, our staff in Roseville, as well as in corporate headquarters in Mountain View, the Technology Center in Natick, Massachusetts, and the field offices throughout the United States are always available to answer customer questions.

It is NEC's commitment to provide leading edge technology on a local basis. As a result, the company announced its decision in 1989 to expand the Roseville manufacturing facility. In Spring 1991, NEC Electronics will open the doors to one of the most advanced fabrication facilities in the United States. This 465,000-square-foot addition will be capable of producing the most technologically advanced products available anywhere in the world. Although the plant initially will produce 4 Meg DRAMs, it is being designed to quickly move to 16 Meg and higher as customer requirements demand. The facility will also be capable of manufacturing other advanced products as well.

The new addition will increase square footage of the Roseville plant by more than four times, enabling NEC Electronics to offer a higher volume of product, manufactured locally for U.S. customers, as well as a broad range of devices—from memories to custom microprocessors and ASICs. The $500 million investment to expand manufacturing in Roseville represents NEC's ongoing commitment to the needs of the U.S. market.

Approximately 30% of NEC Electronics' sales revenue comes from chips produced in the United States (compared to the 5% produced here by other Japanese chipmakers). This percentage is expected to increase as NEC's expanded facilities will have the capacity to produce 3 to 5 million chips per month. The expansion will also directly result in the creation of 600 new jobs in the United States, with a total annual payroll in excess of $18 million.



Construction of the expansion at NEC Electronics' manufacturing facility in Roseville, California. Due to be completed in Spring 1991, this state-of-the-art plant will add the capability to produce the 4 Meg DRAM, as well as advanced SRAMs, microprocessors and ASIC devices. In addition, the plant has been designed to be easily upgraded to produce the 16 Meg DRAM.

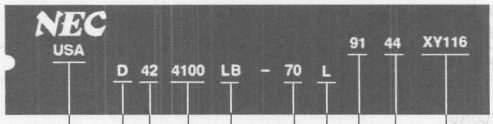
Product Line Overview

Bit Density	Application Specific	RAM				EPROM	EEPROM	ROM
		Module	Dynamic	MOS Static	ECL			
1K					μPB10422 μPB100422			
4K					μPB10470 μPB10474 μPB10474A μPB10474E μPB100470 μPB100474 μPB100474A μPB100474E		μPD28C04 μPD28C05	
8K	μPD42101 μPD42102							
16K	μPD43501				μPB10480 μPB10484 μPB10484A μPB10A484 μPB100480 μPB100484 μPB100484A μPB100A484			
40K	μPD42505							
64K	μPD43608			μPD4361 μPD4362 μPD4363		μPD27HC65	μPD28C64	
133K	μPD42272							
256K	μPD41264 μPD42264 μPD42532		μPD41256 μPD41464	μPD43251 μPD43254 μPD43256A μPD43256B μPD43258 μPD46251	μPD10500 μPD10504 μPD100500 μPD100504		μPD28C256	
320K				μPD46710 μPD46741				
1M	μPD42270 μPD42273 μPD42274 μPD42275 μPD42601	MC-174	μPD421000 μPD421001 μPD421002 μPD424256 μPD424258 μPD424266 μPD424268	μPD431000 μPD431000A μPD431001 μPD431004		μPD27C1000A μPD27C1001A μPD27C1024A		μPD23C1000A μPD23C1000EA μPD23C1001E μPD23C1010A μPD23C1024E
2M		MC-41256A8 MC-41256A9 MC-157				μPD27C2001		μPD23C2000 μPD23C2000A μPD23C2001
4M		MC-176	μPD424100 μPD424101 μPD424102 μPD424400 μPD424402 μPD424410 μPD424412 μPD424800			μPD27C4001		μPD23C4000 μPD23C4000A μPD23C4001E

Product Line Overview (cont)

Bit Density	Application Specific	RAM				EPROM	EEPROM	ROM
		Module	Dynamic	MOS Static	ECL			
8M		MC-421000A8 MC-421000A9 MC-424256A36						μPD23C8000 μPD23C8001E
16M		MC-424512A36						μPD23C16000
32M		MC-424100A8 MC-424100A9 MC-421000A36						
64M		MC-422000A36						

Device Numbering Guide



Country of Origin

Device Type

B = Digital bipolar
D = Digital MOS

Product Class

10 = 10K ECL RAM
100 = 100K ECL RAM
23(H)C = CMOS ROM
27(H)C = CMOS EPROM
28C = CMOS EEPROM
41 = NMOS dynamic RAM
42 = CMOS dynamic RAM
43 = CMOS static RAM
44 = CMOS static RAM (6-T cell)
46 = BiCMOS static RAM

Device Identifier

Package

B or BH = Ceramic flatpack, with a quartz window if appropriate
C, CR or CZ = Plastic DIP
D, DH, DX or DZ = Cerdip or ceramic DIP, with a quartz window if appropriate
G (≤ 40 pins), GU or GW = Plastic miniflat
G (> 40 pins) or GF = Plastic QFP
GX or GZ = Plastic TSOP
K = Ceramic LCC
L = PLCC
LA, LB or LE = Plastic SOJ
R = Ceramic PGA
V = Plastic ZIP

Speed Selection

-10 = 100 ns or 10 ns
-12 = 120 ns or 12 ns
-15 = 150 ns or 15 ns
-70 = 70 ns
-80 = 80 ns
-85 = 85 ns
-XX = Etc.

Low Power Indicator [Optional]

L = Low power
LL = Very low power

Year

Date Code
Week

NEC Lot Code

Notes:
(1) The marking format may vary among package types.
(2) Regardless of the format, the device number does not change.
(3) The "μP" in NEC part numbers does not appear on the package.
(4) DIP = dual-inline package
(5) LCC = leadless chip carrier
(6) PLCC = plastic leaded chip carrier
(7) PGA = pin grid array
(8) SOJ = small-outline J-lead package
(9) ZIP = zig-zag inline package
(10) TSOP = thin small-outline package
(11) QFP = quad flatpack

83SL-7321B

Application-Specific Devices

Device	Organization	Access Time (ns)	Package (Note 1)	Pins
μPD41264-12	64K x 4 with two ports	120 Port A 40 Port B	C/V	24
μPD41264-15		150 Port A 60 Port B		
μPD42264-10	64K x 4 with two ports	100 Port A 25 Port B	C/LA/V	24
μPD42273-10	256K x 4 with two ports	100 Port A 30 Port B	LE/V	28
μPD42273-12		120 Port A 40 Port B		
μPD42274-10	256K x 4 with two ports	100 Port A 30 Port B	LE/V	28
μPD42274-12		120 Port A 40 Port B		
μPD42275-80	128K x 8 with two ports	80 Port A 25 Port B	LE	40
μPD42275-10		100 Port A 30 Port B		
μPD42275-12		120 Port A 40 Port B		
μPD42101-3	910 x 8	27	C/G	24
μPD42101-2		27		
μPD42101-1		49		
μPD42102-5	1135 x 8	18	C/G	24
μPD42102-3		21		
μPD42102-2		21		
μPD42102-1		40		
μPD42505-50	5048 x 8	40	C	24
μPD42505-50H		40		
μPD42505-75		55		
μPD42505-75H		55		
μPD42270	910 x 263 x 4	40	C	28
μPD42272	7568 x 18	6 MHz (input sampling)	GF	64
μPD42532-10	32K x 8	50	C	40
μPD42601-60	1M x 1	600 (Single) 100 (Page)	C/LA/V	C = 18 LA = 26/20
μPD42601-60L				V = 20
μPD43501	2 x 1K x 8	60	R	132
μPD43608-3	512 x 32 x 4 or 1K x 16 x 4	64	R	132
μPD43608-2		85		

Notes:

(1) C = plastic DIP; G = plastic miniflat; GF = plastic QFP; LA or LE = plastic SOJ; R = ceramic PGA; V = plastic ZIP.

Memory Cards

Device	Organization	Access Time (ns)	Package	Pins
MC-174	128K x 8 (static RAM)	250	Memory card	60
MC-176	512K x 8 (static RAM)	250	Memory card	60

Dynamic RAM Modules

Device	Organization	Access Time (ns)	Package (Note 1)	Pins
MC-157-10	256K x 8 (fast-page)	100	B	30
MC-41256A8-80	256K x 8 (page)	80	A/B	30
MC-41256A8-10		100		
MC-421000A8-60	1M x 8 (fast-page)	60	A/B	30
MC-421000A8-70		70		
MC-421000A8-80		80		
MC-421000A8-10		100		
MC-424100A8-70	4M x 8 (fast-page)	70	A/B	30
MC-424100A8-80		80		
MC-424100A8-10		100		
MC-41256A9-80	256K x 9 (page)	80	A/B	30
MC-41256A9-10		100		
MC-421000A9-60	1M x 9 (fast-page)	60	A/B	30
MC-421000A9-70		70		
MC-421000A9-80		80		
MC-421000A9-10		100		
MC-424100A9-70	4M x 9 (fast-page)	70	A/B	30
MC-424100A9-80		80		
MC-424100A9-10		100		
MC-424256A36-80	256K x 36 (page)	80	B/F	72
MC-424256A36-85		85		
MC-424256A36-10		100		
MC-424256A36BH/FH-70	256K x 36 (fast-page)	70	BH/FH	72
MC-424256A36BH/FH-80		80		
MC-424256A36BH/FH-10		100		
MC-424512A36-80	512K x 36 (page)	80	B/F	72
MC-424512A36-85		85		
MC-424512A36-10		100		
MC-424512A36BH/FH-70	512K x 36 (fast-page)	70	BH/FH	72
MC-424512A36BH/FH-80		80		
MC-424512A36BH/FH-10		100		
MC-421000A36BH/FH-70	1M x 36 (fast-page)	70	BH/FH	72
MC-421000A36BH/FH-80		80		
MC-421000A36BH/FH-10		100		
MC-422000A36BH/FH-70	2M x 36 (fast-page)	70	BH/FH	72
MC-422000A36BH/FH-80		80		
MC-422000A36BH/FH-10		100		

Notes:

(1) A = leaded SIMM; B = socket-mountable SIMM; BH = special-height, socket-mountable SIMM; F = socket-mountable SIMM with gold-plated contacts; FH = special-height, socket-mountable SIMM with gold-plated contacts.

Dynamic RAMs

Device	Organization	Access Time (ns)	Package (Note 1)	Pins
μPD41256-80	256K x 1 (page)	80	C/L	C = 16
μPD41256-10		100		L = 18
μPD41464-80	64K x 4	80	C/L/V	C = 18
μPD41464-10		100		L = 18
μPD41464-12		120		V = 20
μPD421000-60	1M x 1 (fast-page)	60	C/LA/V	C = 18
μPD421000-70		70		LA = 26/20
μPD421000-80		80		V = 20
μPD421000-10		100		
μPD421001-60	1M x 1 (nibble)	60	C/LA/V	C = 18
μPD421001-70		70		LA = 26/20
μPD421001-80		80		V = 20
μPD421001-10		100		
μPD421002-60	1M x 1 (static-column)	60	C/LA/V	C = 18
μPD421002-70		70		LA = 26/20
μPD421002-80		80		V = 20
μPD421002-10		100		
μPD424256-60	256K x 4 (fast-page)	60	C/LA/V	C = 20
μPD424256-70		70		LA = 26/20
μPD424256-80		80		V = 20
μPD424256-10		100		
μPD424258-60	256K x 4 (static-column)	60	C/LA/V	C = 20
μPD424258-70		70		LA = 26/20
μPD424258-80		80		V = 20
μPD424258-10		100		
μPD424266-60	256K x 4 (fast-page, write-per-bit)	60	C/LA/V	C = 20
μPD424266-70		70		LA = 26/20
μPD424266-80		80		V = 20
μPD424266-10		100		
μPD424268-60	256K x 4 (static-column, write-per-bit)	60	C/LA/V	C = 20
μPD424268-70		70		LA = 26/20
μPD424268-80		80		V = 20
μPD424268-10		100		
μPD424100-70	4M x 1 (fast-page)	70	LB/V (Note 2)	V = 20
μPD424100-80		80		LB = 26/20
μPD424100-10		100		
μPD424101-70	4M x 1 (nibble)	70	LB/V (Note 2)	V = 20
μPD424101-80		80		LB = 26/20
μPD424101-10		100		
μPD424102-70	4M x 1 (static-column)	70	LB/V (Note 2)	V = 20
μPD424102-80		80		LB = 26/20
μPD424102-10		100		
μPD424400-70	1M x 4 (fast-page)	70	LB/V (Note 2)	V = 20
μPD424400-80		80		LB = 26/20
μPD424400-10		100		
μPD424402-70	1M x 4 (static-column)	70	LB/V (Note 2)	V = 20
μPD424402-80		80		LB = 26/20
μPD424402-10		100		
μPD424410-70	1M x 4 (fast-page, write-per-bit)	70	LB/V (Note 2)	V = 20
μPD424410-80		80		LB = 26/20
μPD424410-10		100		
μPD424412-70	1M x 4 (static-column, write-per-bit)	70	LB/V (Note 2)	V = 20
μPD424412-80		80		LB = 26/20
μPD424412-10		100		

Dynamic RAMs (cont)

Device	Organization	Access Time (ns)	Package (Note 1)	Pins
μPD424800-70	512K x 8 (fast-page)	70	LE/V	28
μPD424800-80		80		
μPD424800-10		100		

Notes:

(1) C = plastic DIP; L = PLCC; LA, LB or LE = plastic SOJ; V = plastic ZIP.

(2) A 300-mil SOJ package will be available in 1990. Ordering information was not defined at the time this 1991 edition was released for printing.

Static RAMs

Device	Organization	Access Time (ns)	Package (Note 1)	Pins
μPD46710-15	16K x 10 x 2	15	LN	52
μPD46710-20		20		
μPD46741-15	8K x 20 x 2	15	LP	68
μPD46741-20		20		
μPD4361-40	64K x 1	40	K	22
μPD4361-45		45	C/K/LA	
μPD4361-55		55	C/K/LA	
μPD4361-70		70	C	
μPD4362-45	16K x 4 ($\overline{CS}$ only)	45	C	22
μPD4362-55		55		
μPD4362-70		70		
μPD4363-45	16K x 4 ($\overline{CS}$, $\overline{OE}$)	45	C	24
μPD4363-55		55		
μPD4363-70		70		
μPD43251-35	256K x 1	35	C/LA	24
μPD43251-45		45		
μPD43251-55		55		
μPD46251-20	256K x 1	20	CR/LA	24
μPD46251-25		25		
μPD43254-35	64K x 4	35	C	24
μPD43254-45		45		
μPD43254-55		55		
μPD43256A-85	32K x 8	85	C/GU/GX	C = 28
μPD43256A-10		100		GU = 28
μPD43256A-12		120		GX = 32
μPD43256A-15		150		
μPD43256B-55	32K x 8	55	C/GU/GX	C = 28
μPD43256B-70		70		GU = 28
μPD43256B-85		85		GX = 32
μPD43258-35	32K x 8	35	CR/LA	28
μPD43258-45		45		
μPD431000-85	128K x 8	85	CZ/GW	32
μPD431000-10		100		
μPD431000-12		120		
μPD431000A-70	128K x 8	70	CZ/GW/GZ	32
μPD431000A-85		85		
μPD431001-25	1M x 1	25	LE	28
μPD431001-35		35		ECL RAMs

Static RAMs (cont)

Device	Organization	Access Time (ns)	Package (Note 1)	Pins
μPD431004-25	256K x 4	25	LE	28
μPD431004-35		35		

Notes:

(1) C, CR or CZ = plastic DIP; GU or GW = plastic miniflat; GX or GZ = plastic TSOP; K = ceramic LCC; LA or LE = plastic SOJ; LN or LP = PLCC.

ECL RAMs

Device	Organization	Access Time (ns)	Package (Note 1)	Pins
μPB10422-7	256 x 4	7	D	24
μPB10422-10		10		
μPB10470-10	4K x 1	10	D	18
μPB10470-15		15		
μPB10474-8	1K x 4	8	D	24
μPB10474-10		10		
μPB10474-15		15		
μPB10474A-5	1K x 4	5	D	24
μPB10474A-6		6		
μPB10474E-3	1K x 4	3	D	24
μPB10474E-4		4		
μPB10480-10	16K x 1	10	B/D	20
μPB10480-15		15		
μPB10484-10	4K x 4	10	B/D	28
μPB10484-15		15		
μPB10484A-5	4K x 4	5	B/D	28
μPB10484A-7		7		
μPB10A484-5	4K x 4	5	BH/D	28
μPB10A484-7		7		
μPD10500-15	256K x 1	15	D	24
μPD10500-20		20		
μPD10504-15	64K x 4	15	D	32
μPB100422-7	256 x 4	7	B/DH	24
μPB100422-10		10		
μPB100470-10	4K x 1	10	D	18
μPB100470-15		15		
μPB100474-4.5	1K x 4	4.5	K	24
μPB100474-6		6	B/K	
μPB100474-8		8	B/D	
μPB100474-10		10	B/D	
μPB100474-15		15	B/D	
μPB100474A-5	1K x 4	5	BH/D	24
μPB100474A-6		6		
μPB100474E-3	1K x 4	3	B/D	24
μPB100474E-4		4		
μPB100480-10	16K x 1	10	B/D	20
μPB100480-15		15		
μPB100484-10	4K x 4	10	B/D	28
μPB100484-15		15		

ECL RAMs (cont)

Device	Organization	Access Time (ns)	Package (Note 1)	Pins
μPB100484A-5	4K x 4	5	B/D	28
μPB100484A-7		7		
μPB100A484-5	4K x 4	5	B/D	28
μPB100A484-7		7		
μPD100500-15	256K x 1	15	D	24
μPD100500-20		20		
μPD100504-15	64K x 4	15	D	32

Notes:

(1) B or BH = ceramic flatpack; D or DH = ceramic DIP and cerdip; K = ceramic LCC.

EPROMs

Device	Organization	Access Time (ns)	Package (Note 1)	Pins
μPD27HC65-25	8K x 8	25	DX	24
μPD27HC65-35		35		
μPD27HC65-45		45		
μPD27C1000A-12	128K x 8 (ROM Comp.)	120	D	32
μPD27C1000A-15		150		
μPD27C1000A-20		200		
μPD27C1001A-12	128K x 8 (JEDEC)	120	D	32
μPD27C1001A-15		150		
μPD27C1001A-20		200		
μPD27C1024A-12	64K x 16	120	D	40
μPD27C1024A-15		150		
μPD27C1024A-20		200		
μPD27C2001-15	256K x 8	150	D	32
μPD27C2001-17		170		
μPD27C2001-20		200		
μPD27C4001-15	512K x 8	150	DZ	32
μPD27C4001-17		170		
μPD27C4001-20		200		

Notes:

(1) D, DX or DZ = ceramic DIP with quartz window.

EEPROMs

Device	Organization	Access Time (ns)	Package (Note 1)	Pins
μPD28C04-20	512 x 8	200	C/G	24
μPD28C04-25		250		
μPD28C05-20	512 x 8	200	C/G	24
μPD28C05-25		250		
μPD28C64-20	8K x 8	200	C	28
μPD28C64-25		250		
μPD28C256-20	32K x 8	200	CZ	28
μPD28C256-25		250		

Notes:

(1) C or CZ = plastic DIP; G = plastic miniflat.

Mask-Programmable ROMs

Device	Organization	Access Time (ns)	Package (Note 1)	Pins
μPD23C1000A	128K x 8 ($\overline{CE}$)	200	C/G	28
μPD23C1000EA	128K x 8 ($\overline{CE}$/$\overline{OE}$)	200	C	32
μPD23C1001E	128K x 8	200	C	32
μPD23C1010A	128K x 8 ($\overline{OE}$)	200	C	28
μPD23C1024E	64K x 16	200	C	40
μPD23C2000	128K x 16 or 256K x 8	250	C/GC	40/52
μPD23C2000A	128K x 16 or 256K x 8	200	C	40
μPD23C2001	256K x 8	250	C	32
μPD23C4000	256K x 16 or 512K x 8	250	C/GF	40/64
μPD23C4000A	256K x 16 or 512K x 8	200	C	40
μPD23C4001E	512K x 8	250	C/GW	32
μPD23C8000	512K x 16 or 1M x 8	250	CZ	42
μPD23C8001E	1M x 8	250	CZ	32
μPD23C16000	1M x 16 or 2M x 8	250	CZ	42

Notes:

(1) C or CZ = plastic DIP; G or GW = plastic miniflat;
GC or GF = plastic QFP.

Alternate Source Index

AMD	NEC
AM27C010	μPD27C1001A
AM27C020	μPD27C2001
AM27C1024	μPD27C1024
μPD27C49	μPD27HC65
μPD27549	μPD27HC65
AM2864A	μPD28C64
AM9864	μPD28C64
AM99C164	μPD4362
AM99C328	μPD43256A
AM99C641	μPD4361

ATMEL	NEC
AT27C010	μPD27C1001A
AT27C1024	μPD27C1024A
AT27HC641/2	μPD27HC65
AT28C04	μPD28C04
AT28C256	μPD28C256
AT28C64	μPD28C64

CATALYST	NEC
CAT27HC010	μPD27C1001A
CAT27C210	μPD27C1024A
CAT28C64A	μPD28C64
CAT28C256	μPD28C256

CYPRESS	NEC
CY100E474L	μPB100474
CY10E474L	μPB10474
CY7C164	μPD4362
CY7C187	μPD4361
CY7C194	μPD43254
CY7C198	μPD43256A
CYC261	μPD27HC65
CYC263	μPD27HC65
CYC264	μPD27HC65

DENSE-PAC	NEC
DPV27C1024A	μPD27C1024A

EXEL	NEC
XLS2864A	μPD28C64
XL28C64	μPD28C64

FUJITSU	NEC
MB61461	μPD41264
MB81256	μPD41256
MB814100	μPD424100
MB81C4256	μPD424256
MB814400	μPD424400
MB81464	μPD41464
MB81C1000	μPD421000
MB81C1001	μPD421001
MB81C1002	μPD421002
MB81C4251	μPD42273
MB81C4253	μPD42274
MB81C71	μPD4361
MB81C74	μPD4362
MB8184	μPD43254
MB82B001	μPD431001
MB82B005	μPD431004
MB82B81	μPD46251
MB84256	μPD43256A
MB831000	μPD23C1000A
MB831124	μPD23C1000A
MB85225	MC-41256A8
MB85225	MC-41256A8
MB85227	MC-41256A9
MB85227	MC-41256A9
MB85230	MC-421000A8
MB85231	MC-421000B8
MB85235	MC-421000A9
MB85327	MC-421000C9
MBM100422	μPB100422
MBM100470	μPB100470
MBM100474	μPB100474
MBM100480	μPB100480
MBM100484	μPB100484
MBM100484	μPB100484A
MBM100C500	μPD100500
MBM10422	μPB10422
MBM10470	μPB10470
MBM10474	μPB10474
MBM10484	μPB10484A
MBM10C500	μPD10500
MBM27C1000	μPD27C1000A
MBM27C1001	μPD27C1001A
MBM27C1024	μPD27C1024A
MBM28C64	μPD28C64
MB7143	μPD27HC65
MB7144E	μPD27HC65
MB7144H	μPD27HC65

GI	NEC
27HC641	μPD27HC65

HARRIS	NEC
HM-76641	μPD27HC65
HM-76641A	μPD27HC65

HITACHI	NEC
HB561003	MC-41256A9
HB56A18	MC-421000A8
HB56A19	MC-421000A9
HB56A42	MC-424100A8
HB56A49	MC-424100A9
HB56C18	MC-421000C8
HB56D136	MC-421000A36BH
HB56D236	MC-422000A36BH
HB56D25636	MC-424256A36BH
HB56D51236	MC-424512A36BH
HB58A19-	MC-421000A9
HM100422	μPB100422
HM100470	μPB100470
HM100474	μPB100474
HM100500	μPD100500
HM100504	μPD100504
HM10422	μPB10422
HM10470	μPB10470
HM10474	μPB10474
HM10500	μPD10500
HM10504	μPD10504
HM50256	μPD41256
HM50464	μPD41464
HM511000	μPD421000
HM511001	μPD421001
HM511002	μPD421002
HM514100	μPD424100
HM514101	μPD424101
HM514256	μPD424256
HM514400	μPD424400
HM514410	μPD424410
HM534251	μPD42273
HM534253	μPD42274
HM53461	μPD41264
HM6208	μPD43254
HM62256	μPD43256A
HM624256	μPD431004
HM628128	μPD431000
HM6287	μPD4361
HM658128	μPD431000

Alternate Source Index (cont)

HITACHI	NEC
HN27301	μPD27C1000A
HN27C101	μPD27C1001A
HN27C1024	μPD27C1024A
HN27C256	μPD27C256A
HN58C256	μPD28C256
HN58C65	μPD28C64
HN58064	μPD28C64
HN58C66	μPD28C64
HN62301	μPD23C1000A

HYUNDAI	NEC
HY62C64	μPD28C64

ICT	NEC
27CX641	μPD27HC65
27CX642	μPD27HC65

IDT	NEC
IDT6167	μPD4311
IDT71256	μPD43256A
IDT71258	μPD43254
IDT7187	μPD4361
IDT7188	μPD4362
IDT7M7864	μPD28C64
IDT78C64A	μPD28C64

INMOS	NEC
IMS1600	μPD4361
IMS1620	μPD4362
IMS1630	μPD4364
IMS1820	μPD43254
IMS1830	μPD43256A

INTEL	NEC
27C010	μPD27C1001A
27C020	μPD27C2001
27C210	μPD27C1024A
27C256	μPD27C256A
2864A	μPD28C64
MT5C1001	μPD431001
MT5C1005	μPD431004

LATTICE	NEC
SR256K4	μPD43254
SR256K8	μPD43256A
SR64K1	μPD4361
SR64K4	μPD4362

MICROCHIP	NEC
28C04A	μPD28C04
28C64A	μPD28C64
28CP256A	μPD28C256
28C256B	μPD28C256

MICRON	NEC
MT4C1004	μPD424100
MT4C4001	μPD424400
MT8C8024	MC-421000A8
MT8C9024	MC-421000A9

MITSUBISHI	NEC
M5M27C101K	μPD27C1001A
M5M27C201K	μPD27C2001
M5M28C64	μPD28C64
M5M4256	μPD41256
M5M44100	μPD424100
M5M44101	μPD424101
M5M44102	μPD424102
M5M4C264	μPD41264
M5M442256	μPD42274
M5M442256	μPD42273
M5M44400	μPD424400
M5M44402	μPD424402
M5M4464	μPD41464
M5M482128	μPD42275
M5M4C1000	μPD421000
M5M4C1001	μPD421001
M5M4C1002	μPD421002
M5M4C256	μPD424256
M5M51001	μPD431001
M5M51004	μPD431004
M5M51008	μPD431000A
M5M5256	μPD43256A
M5M5258	μPD43254
MH1M08A	MC-421000A8
MH1M09	MC-421000A9
MH25608J	MC-41256A8
MH25609J	MC-41256A9
MH25636A	MC-424256A36BH
MH51236H	MC-424512A36BH

MOSAIC	NEC
MDM14000	μPD424100
MDM41000	μPD424400

MOTOROLA	NEC
MCM100422	μPB100422
MCM100470	μPB100470
MCM100474	μPB100474

MOTOROLA	NEC
MCM10422	μPB10422
MCM10470	μPB10470
MCM10474	μPB10474
MCM514100	μPD424100
MCM514400	μPD424400
MCM6187	μPD4361
MCM6188	μPD4362

NATIONAL	NEC
DM100422	μPB100422
DM100470	μPB100470
DM100474	μPB100474
DM10422	μPB10422
DM10470	μPB10470
DM10474	μPB10474
NMC27C010	μPD27C1001A
NMC27C1024	μPD27C1024A
NMC98C64	μPD28C64
93Z665C	μPD27HC65
93Z667C	μPD27HC65

OKI	NEC
MSC2304-KS9	MC-41256A9
MSC2304KS8	MC-41256A8
MSC2310Y59/KS9	MC-421000A9
MSC231148/K58	MC-421000A8
MSM27C1000	μPD27C1000
MSM27C1024	μPD27C1024
MSM27C256	μPD27C256A
MSM28C64	μPD28C64
MSM41257	μPD41257
MSM514100	μPD424100
MSM514252	μPD42274
MSM514400	μPD424400

PANASONIC	NEC
MN41C4000	μPD424100
MN41C4001	μPD424101
MN41C4002	μPD424102
MN41C41000	μPD424400
MN41C41002	μPD424402

PERFORMANCE	NEC
P4C187	μPD4361
P4C188	μPD4362

PHILIPS-SIGNETICS	NEC
27C210	μPD27C1024A

Alternate Source Index (cont)

RAYTHEON	NEC
39VP864	μPD27HC65

SHARP	NEC
LH5749	μPD27HC65

SIGNETICS	NEC
27HC641	μPD27HC65
27HC642	μPD27HC65
N82HS641	μPD27HC65
N82S641	μPD27HC65

SSI	NEC
SSI203	μPD27HC65

SAMSUNG	NEC
KM28C64	μPD28C64
KM28C256	μPD28C256
KM41C4000	μPD424100
KM41C4001	μPD424101
KM41C4002	μPD424102
KM44C1000	μPD424400
KM611001	μPD431001
KM641001	μPD431004

SEEQ	NEC
27C256	μPD27C256A
2804A	μPD28C04
28C256	μPD28C256
28C64	μPD28C64

SGS-THOMPSON	NEC
MK48Z30	μPD43256A
M27C1001	μPD27C1001A
M27C1024	μPD27C1024A

SIEMENS	NEC
HYB514100	μPD424100
HYB514400	μPD424400
HYM910005	MC-421000A9
HYM940005	MC-424100A9

TI	NEC
TMO24GAD9	MC-421000A9
TMO24GADB	MC-421000A8
TMS27C256	μPD27C256A
TMS27C010	μPD27C1001A
TMS27C210	μPD27C1024A
TMS278C49	μPD27HC65
TMS4256	μPD41256
TMS44100	μPD424100
TMS44400	μPD424400
TMS4461	μPD41264
TMS4464	μPD41464
TMS44C251	μPD42273
TMS44C251	μPD42274
TMS48C121	μPD42275
TMS44C256	μPD424256
TMS4C1024	μPD421000
TMS4C1025	μPD421001
TMS4C1027	μPD421002
TMS62456	μPD431004
TMS62828	μPD431000

TOSHIBA	NEC
TC511000	μPD421000
TC511001	μPD421001
TC511002	μPD421002
TC514100	μPD424100
TC514101	μPD424101
TC514102	μPD424102
TC514256	μPD424256
TC514400	μPD424400
TC514402	μPD424402
TC514410	μPD424410
TC518128	μPD431000A
TC524128A	μPD42275
TC524256	μPD42274

TOSHIBA	NEC
TC524256A	μPD42273
TC524258A	μPD42274
TC531000	μPD23C1000A
TC55256	μPD43256
TC55257	μPD43256
TC55257	μPD43256A
TC55257	μPD43256B
TC55416	μPD4362
TC55417	μPD4363
TC55464	μPD43254
TC5561/62	μPD4361
TC5561	μPD4361
TC571000	μPD27C1000A
TC571001D	μPD27C1001A
TC571024	μPD27C1024A
TC58257	μPD28C256
THM362500	MC-424256A36BH
THM365120	MC-424512A36BH
THM81000	MC-421000A8
THM81000A	MC-421000A8
THM91000	MC-421000A9
THM91000	MC-424256A36BH/FH
THM91000A	MC-421000A9
TMM41256	μPD41256
TMM41464	μPD41464

WAFERSCALE	NEC
WS27C010L	μPD27C1001A
WS27C210L	μPD27C1024A
WS57C49	μPD27HC65
WS57C49B	μPD27HC65

XICOR	NEC
X24C04	μPD28C04
X28C256	μPD28C256
X28C64	μPD28C64

Notes:

(1) Electrical differences may exist. Check the manufacturers' data sheets for complete information.

(2) The competitive data contained herein was obtained from industry and public sources. NEC Electronics is not responsible for changes or deletions to this information.

NEC

Quality and Reliability

2

Section 2
Reliability and Quality Control

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Introduction

As large-scale integration reaches a higher level of density, the reliability of individual devices imposes a more profound impact on system reliability. Great emphasis has thus been placed on assuring device reliability.

Conventionally, performing reliability tests and attaining feedback from the field were the only methods by which reliability had been monitored and measured. At these higher levels of LSI density, however, it has become increasingly difficult to activate all of the internal circuit elements in a device, and moreover, to detect the degradation of those elements by measuring characteristics across external terminals. As a result, testing alone may not provide enough information to ensure today's demanding reliability requirements. A different philosophy and methodology is needed for reliability assurance.

In order to guarantee and improve a high level of reliability for large-scale integrated circuits, it is essential to build quality and reliability into the product. Conventional testing can then be performed to confirm that the product demonstrates acceptable reliability.

Built-In Quality and Reliability

NEC has introduced the concept of total quality control (TQC) across its entire semiconductor product line for implementing this philosophy. Rather than performing only a few simple quality inspections, quality control is distributed into each process step and then summed to form a consolidated system. TQC involves workers, engineers, quality control staffs, and all levels of management in company-wide activities (figure 1). Through TQC, NEC builds quality into the product and thus can assure high reliability. Additionally, NEC has introduced a prescreening method into the production line for eliminating potentially defective units. This combination of building quality in and screening projected early failures out has resulted in superior quality and excellent reliability.

Technology Description

Most large-scale integrated circuits utilize high density MOS technology. State-of-the-art high performance has been achieved by improving fine-line generation techniques. By reducing physical parameters, circuit density and performance increase while active circuit power dissipation decreases. The data presented here shows that this advanced technology, combined with the practice of TQC, yields products as reliable as those from previous technologies.

Approaches to Total Quality Control

TQC activities are geared toward total satisfaction of the customer. The success of these activities is dependent upon the total commitment of management to enhancing employee development, maintaining a customer-first attitude, and fulfilling community responsibilities.

First, the quality control function is embedded into each process. This method enables early detection of possible causes of failure and immediate feedback.

Second, the reliability and quality assurance policy reflects the beliefs and practices of the entire organization. This enables companywide quality control activities: at NEC, everyone is involved with the concept and methodology of total quality control.

Third, there is an ongoing research and development effort to set even higher standards of device quality and reliability.

Fourth, extensive failure analysis is performed periodically and appropriate corrective actions are taken as preventative measures. Process control is based on statistical data gathered from this analysis.

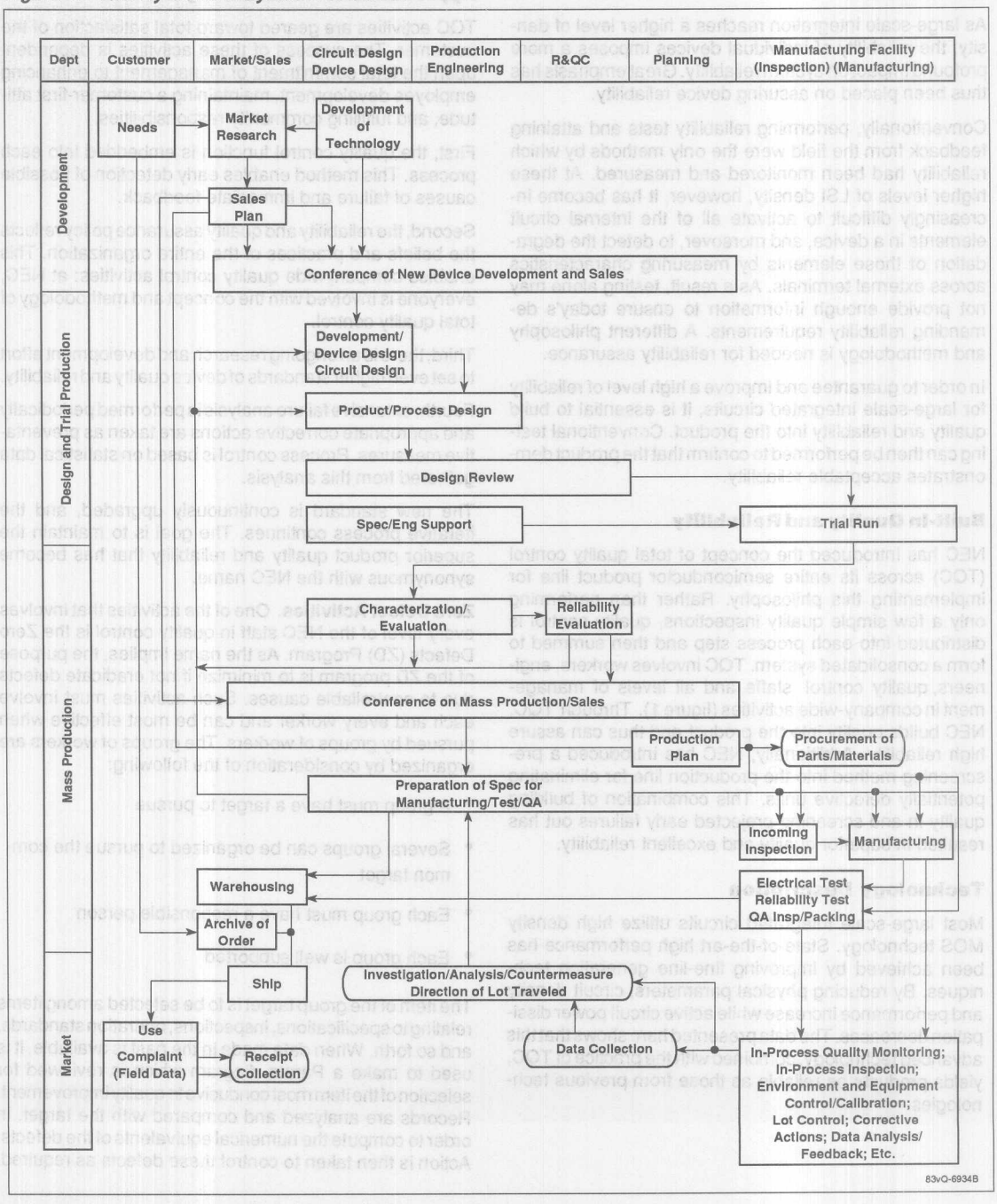
The new standard is continuously upgraded, and the iterative process continues. The goal is to maintain the superior product quality and reliability that has become synonymous with the NEC name.

Zero Defect Activities. One of the activities that involves every level of the NEC staff in quality control is the Zero Defects (ZD) Program. As the name implies, the purpose of the ZD program is to minimize if not eradicate defects due to controllable causes. Such activities must involve each and every worker and can be most effective when pursued by groups of workers. The groups of workers are organized by consideration of the following:

- A group must have a target to pursue
- Several groups can be organized to pursue the common target
- Each group must have a responsible person
- Each group is well supported

The item of the group target is to be selected among items relating to specifications, inspections, operation standards, and so forth. When data made in the past is available, it is used to make a Pareto diagram which is reviewed for selection of the item most conducive to quality improvement. Records are analyzed and compared with the target, in order to compute the numerical equivalents of the defects. Action is then taken to control these defects as required.

Figure 1. Quality Control System Flowchart



Statistical Approach. Another approach to quality control is the use of statistical analysis. NEC has been utilizing statistical analysis at each stage of LSI production development, trial runs, and mass production in order to build and maintain product quality. Some of the methods for implementing this statistical approach are:

- Design of experiments
- Control charts
- Data analysis: Variance, correlation, regression, multivariance, etc.
- Cp, Cpk study: Variables and attributes data (Normally, study is done on a monthly basis)

Process control sheets and other QC tools are used to monitor various important parameters such as Cp, Cpk, X, X, X-R, electrical parameters, pattern dimensions, bond strength, test percentage defects, etc.

The results of these studies are watched by the production staff, QC Engineers, and other responsible engineers. If any out-of-control or out-of-specification limit is observed, quick action is taken in accordance with corrective action procedures.

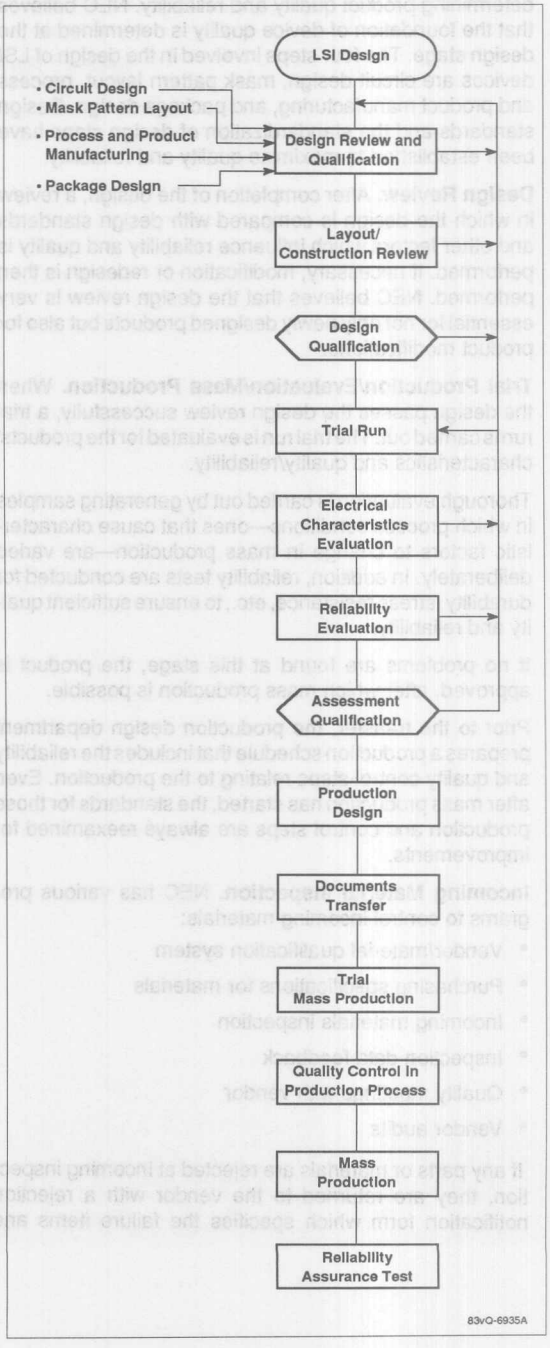
Implementation of Quality Control

Building quality into a product requires early detection of possible causes of failure at each process step, then immediate feedback to remove these causes. A fixed station quality inspection is often lacking in immediate feedback; it is therefore necessary to distribute quality control functions to each process step—including the conceptual stage. Following is a breakdown of the significant steps at which NEC has implemented these functions:

- Product development
- Incoming material inspection
- Wafer processing
- Chip mounting and packaging
- Electrical testing and thermal aging
- Outgoing material inspection
- Reliability testing
- Process/product changes

New Product Development Phase. The product development phase includes conception of a product, review of the device proposal, physical element design and organization, engineering evaluation, and finally, transfer of the product to manufacturing. Quality and reliability are considered at every step (figure 2).

Figure 2. New Product Development Flow



Design. Design plays an extremely important role in determining product quality and reliability. NEC believes that the foundation of device quality is determined at the design stage. The four steps involved in the design of LSI devices are circuit design, mask pattern layout, process and product manufacturing, and package design. Design standards and the standardization of design steps have been established to maximize quality and reliability.

Design Review. After completion of the design, a review in which the design is compared with design standards and other factors which influence reliability and quality is performed. If necessary, modification or redesign is then performed. NEC believes that the design review is very essential for not only newly designed products but also for product modifications.

Trial Production/Evaluation/Mass Production. When the design passes the design review successfully, a trial run is carried out. The trial run is evaluated for the products' characteristics and quality/reliability.

Thorough evaluation is carried out by generating samples in which process conditions—ones that cause characteristic factors to change in mass production—are varied deliberately. In addition, reliability tests are conducted for durability, stress resistance, etc., to ensure sufficient quality and reliability.

If no problems are found at this stage, the product is approved, after which mass production is possible.

Prior to the transfer, the production design department prepares a production schedule that includes the reliability and quality control steps relating to the production. Even after mass production has started, the standards for those production and control steps are always reexamined for improvements.

Incoming Material Inspection. NEC has various programs to control incoming materials:

- Vendor/material qualification system
- Purchasing specifications for materials
- Incoming materials inspection
- Inspection data feedback
- Quality meetings with vendor
- Vendor audits

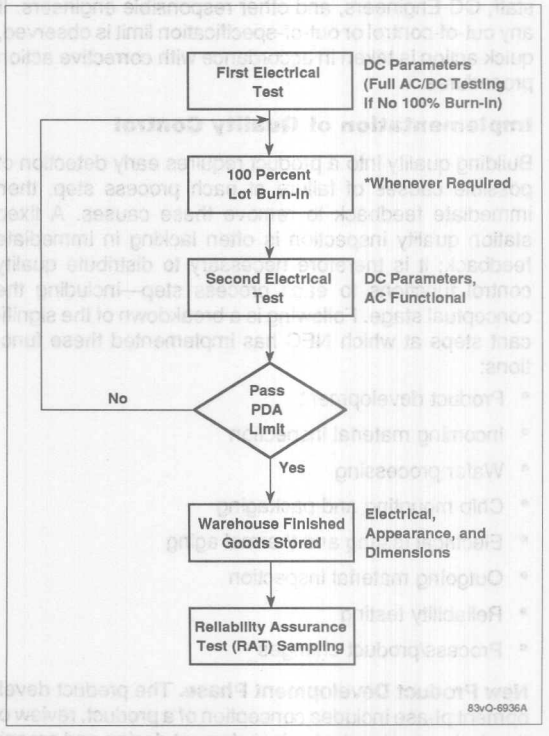
If any parts or materials are rejected at incoming inspection, they are returned to the vendor with a rejection notification form which specifies the failure items and modes. The results of these inspections are used to rate the vendors for future purchasing.

In-process Quality Inspections. Typical in-process quality inspections done at the wafer fabrication, chip mounting and packaging, and device testing stages are listed in Appendix 1.

Electrical Testing and Screening. A flowchart of the typical infant mortality screening (when required) and electrical testing is depicted in figure 3.

At the first electrical test, DC parameters are tested according to the electrical specifications on 100% of each lot. This is a prescreening prior to any infant mortality test. At the second electrical test, AC functional tests as well as DC parameter tests are performed on 100% of each lot. If the percentage of defective units exceeds the limit, the lot is subjected to rescreen. During this time, the defective units undergo failure analysis, the results of which are fed back into the process through corrective actions.

Figure 3. Electrical Testing and Screening



Outgoing Inspection. Prior to warehouse storage, lots are subjected to an outgoing inspection according to the following sampling plan.

• Electrical test:	DC parameters LTPD	3%
	Functional test LTPD	3%
• Appearance:	Major LTPD	3%
	Minor LTPD	7%

Reliability Assurance Tests. Samples are continually taken prior to shipment and subjected to monitoring reliability tests. They are taken from similar process groups, so it may be assumed that the samples' reliability is representative of the reliability of the group.

Reliability Testing

Reliability is defined as the characteristics of an item expressed by the probability that it will perform a required function under stated conditions for a stated period of time. This involves the concepts of probability, the definition of required function(s), and the critical time used in defining the reliability.

Definition of a required function, by implication, treats the definition of a failure. Failure is defined as the termination of the ability of a device to perform its required function. A device is said to have failed if it shows the inability to perform within guaranteed parameters as given in an electrical specification.

Discussion of reliability and failure can be approached in two ways: with respect to systems or to individual devices. Important considerations are the constant failure period, the early failure (infant mortality) period, and overall reliability level.

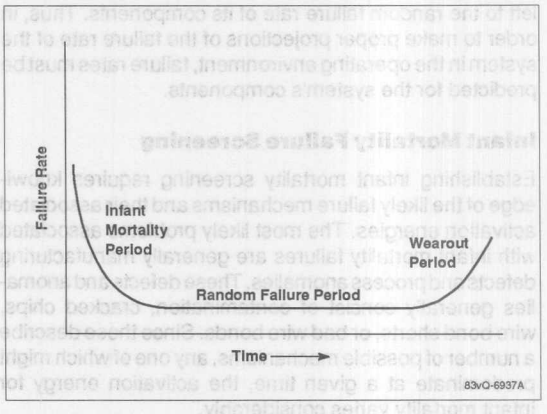
With regard to individual devices, areas of prime interest include specific failure mechanisms, failures in accelerated tests, and failures in screening tests.

The accumulation of normal device failure rates constitutes the expected failure rate of the system hardware: the probability that no device failures will occur in a system is the product of each device's probability that it will not fail. The failure rate of system hardware is then the sum of the failure rates of the components used to construct the system.

Life Distribution

The fundamental principles of reliability engineering predict that the failure rate of a group of devices will follow the well-known bathtub curve in Figure 4. The curve is divided into three regions: infant mortality, random failures, and wearout failures.

Figure 4. Reliability Life (Bathtub) Curve



Infant mortality, as the name implies, represents the early-life failures of devices. These failures are usually associated with one or more manufacturing defects.

After some period of time, the failure rate reaches a low value. This is the random failure portion of the curve, representing the useful portion of the life of a device. During this random failure period, there is a decline in the failure rate due to the depletion of potential random failures from the general population.

The wearout failures occur at the end of the device's useful life. They are characterized by a rapidly rising failure rate over time as devices wear out both physically and electrically.

Thus, for a device that has a very long life expectancy compared to the system which contains it, the areas of concern will be the infant mortality and the random failure portions of the bathtub curve.

Failure Distribution at NEC

In an effort to eliminate infant mortality failures, NEC subjects its products to production burn-in whenever necessary. This burn-in is performed at an elevated temperature for 100 percent of the lots involved and is designed to remove the potentially defective units.

To study the random failure population, integrated circuits returned to NEC from the field undergo extensive failure analysis at respective NEC Manufacturing Divisions. Failure mechanisms are identified and data fed back to cognizant Production and Engineering groups.

This data coupled with in-line data is then used to introduce corrective actions and quality improvement measures.

After elimination of early device failures, a system will be left to the random failure rate of its components. Thus, in order to make proper projections of the failure rate of the system in the operating environment, failure rates must be predicted for the system's components.

Infant Mortality Failure Screening

Establishing infant mortality screening requires knowledge of the likely failure mechanisms and their associated activation energies. The most likely problems associated with infant mortality failures are generally manufacturing defects and process anomalies. These defects and anomalies generally consist of contamination, cracked chips, wire bond shorts, or bad wire bonds. Since these describe a number of possible mechanisms, any one of which might predominate at a given time, the activation energy for infant mortality varies considerably.

Correspondingly, the effectiveness of a screening condition—preferably at some stress level in order to shorten the screening time—varies greatly with the failure mechanism. For example, failures due to ionic contamination have an activation energy of approximately 1.0 eV. Therefore, a 15-hour stress at 125°C junction temperature would be the equivalent of approximately 314 days of operation at a junction temperature of 55°C. On the other hand, failures due to oxide defects have an activation energy of approximately 0.3 eV, and a 15-hour stress at 125°C junction temperature would be the equivalent of approximately four days' operation at 55°C junction temperature. As indicated by this situation, the conditions and duration of infant mortality screening must be strongly dependent on the allowable component, hence system, failures in the field, as well as the economic factors involved.

Empirical data gathered at NEC indicates that early failures (if any) occur after less than 4 hours of stress at 125°C ambient temperature. This fact is supported by the bathtub curve created from the life test results of the same lots, where the failure rate shows a random distribution as opposed to a decreasing failure rate that runs into the random failure region.

Whenever necessary, NEC has adopted this initial infant mortality burn-in at 125°C as a standard production screening procedure. As a result, the field reliability of NEC devices is an order of magnitude higher than the goal set for NEC's integrated circuit products.

NEC believes it is imperative that failure modes associated with infant mortality screens be understood and fixed at the manufacturing level. If such failures can be minimized or eliminated, and countermeasures appropriately monitored, then such screens can be eliminated.

Long-Term Failure Rate

NEC's long-term failure rate goal, based on the mask and process design, is confirmed by life testing using the following conditions:

- A minimum of 1.2 million device hours (= sample size x test period) at 125°C should be accumulated to obtain the accuracy necessary for predicting a failure rate of 0.02% per 1000 hours at 55°C with a 60% confidence level.
- A minimum of 3 million device hours at 125°C should be accumulated to obtain the accuracy necessary for predicting a failure rate of 0.01% per 1000 hours at 55°C with a 60% confidence level.

Accelerated Reliability Testing

NEC performs extensive reliability testing both at preproduction and post-production levels to insure that its products meet the minimum expectations set by NEC. Accelerated reliability testing results are then used to quantitatively monitor the reliability.

As an example, assume that an electronic system contains 1000 integrated circuits and can tolerate 1 percent system failures per month. The failure rate per component is:

$$\frac{1\% \text{ Failures}}{720 \text{ Hours} \times 1000 \text{ Pcs.}} = .0014 \frac{\% \text{ Failures}}{1000 \text{ Hrs}}$$

or 14 FITs

To demonstrate this failure rate, note that 14 FITs correspond to one failure in about 85 devices during an operating test of 10,000 hours. It is quickly apparent that a test condition is required to accelerate the time-to-failure in a predictable and understandable way. The implicit requirement for the accelerated stress test is that the relationship between the accelerated stress testing condition and the condition of actual use be known.

A most common time-to-failure relationship involves the effect of temperature, which accelerates many physiochemical reactions which may lead to device failure. Other environmental conditions are voltage, current, humidity, vibration, or some combination of these. Appendix 2 lists typical reliability assurance tests performed at NEC for molded integrated circuits. Figure 5 shows the results of some of these tests for various process types.

High-Temperature Operating/Bias Life Test (HTOL/HTB). This test is used to accelerate failure mechanisms by operating devices at an elevated temperature of 125°C. The data obtained is translated to a lower temperature by using the Arrhenius relationship.

Figure 5. Typical Reliability Test Results

	HTB	T/H	PCT	T/C
Micro:[1]				
NMOS	7/19113 (15 FIT)	15/9315	0/11752	—
CMOS	3/11892 (5.4 FIT)	2/7293	8/9476	—
Memory:	[HTOL]			
DRAM[2]	10/10052 (19 FIT)	0/9958	0/5880	1/2995
SRAM[3]	1/10421	2/8142	0/8768	—
1 MEG DRAM[4]	38/14300 (115 FIT)	0/3634	1/3060	1/1780
ASIC:[5]				
CMOS	2/3506 (33 FIT)	1/1111	1/4764	4/2680
ECL	0/1080 (8.4 FIT)	—	—	0/141
BiCMOS	1/895 (18 FIT)	0/1073	0/935	0/1781

Information has been extracted from NEC Report Numbers:
[1] TRQ-89-05-0030 [2] TRQ-89-01-0021
[3] TRQ-88-09-0008 [4] TRQ-89-01-0020
[5] TRQ-89-04-0025

High-Temperature and High-Humidity Test. Semiconductor integrated circuits are highly sensitive to the effect of humidity causing electrolytic corrosion between biased lines. The high-temperature and high-humidity test is performed to detect failure mechanisms that are accelerated by these conditions, such as leakage-related problems and drifts in device parameters due to process instability.

High-Temperature Storage Test. Another common test is the high-temperature storage test, in which devices are subjected to elevated temperatures with no applied bias. This test is used to detect process instability and stress migration problems.

Environmental Tests. Other environmental tests are performed to detect problems related to the package, material, susceptibility to extremes in environment, and problems related to usage of the devices.

Failure Rate Calculation/Prediction

When predicting the failure rate at a certain temperature from accelerated life test data, the activation energies of the failure mechanisms involved should be considered. This is done whenever the exact cause of failures is known through failure analyses results.

In some cases, an average activation energy is assumed in order to accomplish a quick first order approximation. NEC assumes an average activation energy of 0.7 eV for such approximations. This average value has been assessed from extensive reliability test results and yields a conservative failure rate.

Since most semiconductor failures are temperature dependent, the Arrhenius relationship is used to normalize failure rate predictions at a system operation temperature of 55°C. It assumes that temperature dependence is an exponential function that defines the probability of occurrence, and that the degradation of a performance parameter is linear with time. The Arrhenius model includes the effects of temperature and activation energies of the failure mechanisms in the following Arrhenius equation:

$$A = \exp \frac{-E_A (T_{J1} - T_{J2})}{k(T_{J1})(T_{J2})}$$

Where:

A = Acceleration factor
E_A = Activation energy
T_{J1} = Junction temperature (in K) at $T_{A1} = 55°C$
T_{J2} = Junction temperature (in K) at $T_{A2} = 125°C$
k = Boltzmann's constant $= 8.62 \times 10^{-5}$ eV/K.

Because the thermal resistance and power dissipation of a particular device type cannot be ignored, junction temperatures (T_{J1} and T_{J2}) are used instead of ambient temperatures (T_{A1} and T_{A2}). We calculate junction temperatures using the following formula:

$$T_J = T_A + (\text{Thermal Resistance})(\text{Power Diss. at } T_A)$$

In order to estimate long term failure rate, the acceleration factor must be used to determine the simulated test time. From the high temperature operating life test results, failure rates can then be predicted at a 60% confidence level using the following equation:

$$L = \frac{\chi^2 \, 10^5}{2T}$$

Where:

L = Failure rate in %/1000 hours
$*\chi^2$ = The tabular value of chi-squared distribution at a given confidence level and calculated degrees of freedom (2f + 2, where f = number of failures)
T = # of equivalent device hours
= (# of devices) x (# of test hours) x (acceleration factor)

*Since the failures of concern here are the random, not the infant mortality failures [that is, the end of the downward slope and the middle (constant) section of the bathtub curve in Figure 4], χ^2 is determined assuming a one-sided, fixed time test.

Another method of expressing failures is in FITs (failures in time). One FIT is equal to one failure in 10^9 hours. Since L is already expressed as %/1000 hours (10^{-5} failure/hr), an easy conversion from %/1000 hours to FIT would be to multiply the value of L by 10^4.

EXAMPLE: A sample of 960 pieces was subjected to 1000 hours 125°C burn-in. One reject was observed. Given that the acceleration factor was calculated to be 34.6 using the Arrhenius equation, what is the failure rate normalized to 55°C using a confidence level of 60%? Express the failure rate in FIT:

Solution:

For $n = 2f + 2 = 2(1) + 2 = 4$, $\chi^2 = 4.046$.

$$\text{Then } L = \frac{\chi^2\, 10^5}{2T} \quad (\%/1000 \text{ hour})$$

$$= \frac{\chi^2\, 10^5 \quad (\%/1000 \text{ hr})}{2\ (\#\text{ of dev.})\ (\#\text{ of test hrs.})\ (\text{accl. factor})}$$

$$= \frac{(4.046) \quad 10^5}{2(960)\ (1000)\ (34.6)} = 0.0061\ (\%/1000 \text{ hr})$$

Therefore, $\text{FIT} = 0.0061 \bullet (10^4) = 61$

Product/Process Changes

As mentioned previously, a design review is performed for product modifications or changes. Once the design is approved and processes altered (if necessary) for maximum quality, the device goes through qualification testing to check the reliability. If the test results are acceptable, the product is released for mass production.

Testing is also performed when only a process modification or change is made.

The typical qualification/process change tests are listed in Appendix 3.

Failure Analysis

At NEC, failure analysis is performed not only on field failures, but also routinely on products which exhibit defects during the production process. This data is closely checked for correlation with the production process quality information, inspection results, and reliability test data. Information derived from these failure analyses is used to improve product quality.

As there are a lot of failure mechanisms of LSI devices, highly advanced analytical technologies are required to investigate such failures in detail. The standard failure analysis flowchart relating to the returned products from customers is shown in Appendix 4.

NEC's Goals on Failure Rates

The reject rate at customer's incoming inspection, the infant mortality rate, and the long term reliability, are all monitored and checked against NEC's quality and reliability targets (listed in Figure 6).

Figure 6. NEC Quality and Reliability Targets

	Reject Rate at Customer's Incoming Electrical Inspection (PPM)						Long Term Reliability (FIT)						Infant Mortality (FIT)					
	Memory		µCOM	Gate Arrays			Memory		µCOM	Gate Arrays			Memory		µCOM	Gate Arrays		
Year	ECL RAM	MOS		BiCMOS	ECL	CMOS	ECL RAM	MOS		BiCMOS	ECL	CMOS	ECL RAM	MOS		BiCMOS	ECL	CMOS
1988	150	50	100	1000	300	300	100	50	100	1000	300	150	100	100	150	1000	300	400
1990	100	50	100	500	200	150	80	50	80	500	250	100	80	100	150	500	250	300

Summary and Conclusion

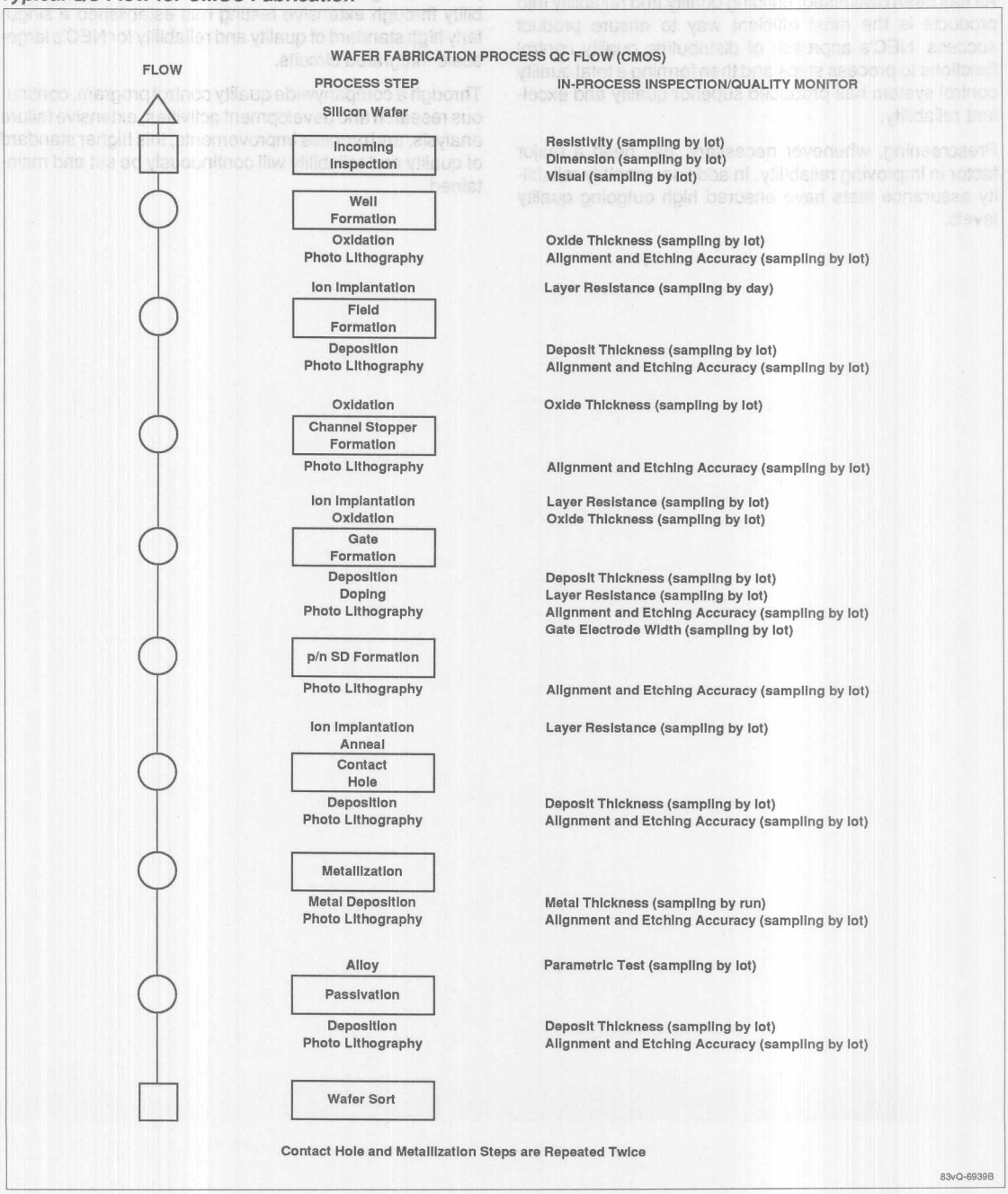
As has been discussed, building quality and reliability into products is the most efficient way to ensure product success. NEC's approach of distributing quality control functions to process steps and then forming a total quality control system has produced superior quality and excellent reliability.

Prescreening, whenever necessary, has been a major factor in improving reliability. In addition, monthly reliability assurance tests have ensured high outgoing quality levels.

The combination of building quality into products, effective prescreening of potential failures, and monitoring of reliability through extensive testing has established a singularly high standard of quality and reliability for NEC's large-scale integrated circuits.

Through a companywide quality control program, continuous research and development activities, extensive failure analysis, and process improvements, this higher standard of quality and reliability will continuously be set and maintained.

Appendix 1
Typical QC Flow for CMOS Fabrication



Appendix 1
Typical QC Flow for PLCC Assembly/Test

Process/Materials	The Check of Manufacturing Conditions				The Check of Manufacturing Qualities			
	Check Items	Frequency	Instrument	Checked By	Check Item	Frequency	Instrument	Checked By
1 Sorted Wafers								
2 Wafer Visual					Wafer Visual	100%	(Naked Eye)	Operator
3 Dicing	Table Speed DI Water Blade Height	Every Shift	Indicators Gauges	P.C.	Sawing Dimensions	Before Running	Microscope with Filter Eyepiece	Operator
4 Break and Expand	Wafer Break Conditions Wafer Expand Conditions	Every Shift	Indicators Gauges	P.C.	Wafer Visual	100%	(Naked Eye)	Operator
5 Die Visual Inspection					Die Visual	Every Lot Sampling (0r 100%)	Microscope	Operator
6 Lead Frames	Die Attached Conditions	Every Shift	Indicators Thermocouple, Potentiometer	P.C.	Die Visual Epoxy Coverage	Every Magazine	(Naked Eye)	Operator
7 Die Attached	Temperature					Every Shift	Microscope	
8 Epoxy Cure (Not Done for Gold Die Attached product)	Heat Temperature N_2 Flow	Every Shift	Indicators Gauges	P.C.	Shear Strength	Every Shift	Dynamometer	Operator
9 Fine Wire	Bonding Conditions	Every Shift	Indicators	P.C.	Visual	Every Magazine	Microscope	Operator
10 Wire Bonding	Temperature	Every Week	Thermocouple and Potentiometer	P.C.	Wire Pull Test	Every Shift	Tension Gauge	Operator
11 Pre-Seal Visual Inspection					Die Visual	Every Lot Sampling (or 100%)	Microscope	Inspector
12 Molding Compound	Temperature of Pellet, Expiration Date	Every Shift	Thermocouple	P.C.				
13 Molding	Temperature Profile of Die Set Preheat Temperature Pressure Cure Time	Every Shift	Thermocouple, Potentiometer	P.C.	Visual	100%	(Naked Eye)	Operator
14 Mold Aging	Temperature	Every Shift	Indicator	P.C.				
15 Deflashing	Deflashing Conditions	Every Shift	Indicators	P.C.	Visual	Every Lot	(Naked Eye)	Operator
	Concentration	Every Week	Titration	Tech.				
	Density	Every Week	Density Meter	Tech.				
	Water Jet Pressure	Every Day	Gauge	Tech.				
16 Plating	Plating Conditions	Every Day	Indicators	P.C.				
	Concentration	Every Week	Titration	Tech.				

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Appendix 1
Typical QC Flow for PLCC Assembly/Test (Cont.)

Process/Materials	The Check of Manufacturing Conditions				The Check of Manufacturing Qualities			
	Check Items	Frequency	Instrument	Checked By	Check Item	Frequency	Instrument	Checked By
17 Plating Inspection					Visual	Every Lot	(Naked Eye)	Technician
					Plating Thickness	Every Lot	X-ray	Technician
					Composition	Every Lot	X-ray	Technician
					Solderability	Once/Day	(Naked Eye)	Technician
18 Marking Ink	Marking Conditions	Every Shift	Indicators	P.C.	Visual	Every Lot	(Naked Eye)	Operator
19 Marking								
20 Mark Cure	Temperature	Every Shift	Thermocouple	P.C.	Marking Permanency	Twice/Shift	Automatic Tester	Operator
21 Lead Forming	Dimensions	Every Shift (Before Running)	Test Jig. Caliper	Operator	Visual	Every Lot	(Naked Eye)	Operator
22 Final Assembly Inspection					Visual	Every Lot	Magnifying Lamp	Operator
23 1st Electrical Sorting	P.M. Check	Every Day	P.M. Jig.	Operator				
	Sample Check	Before Testing	Test Samples	Operator	Electrical Characteristics	100%	IC Tester	Operator
24 Burn-In (Whenever Necessary)	Burn-In Conditions	Every Batch	Indicator	P.C.				
25 2nd Electrical Sorting		Every Day Before Testing	P.M. Jig. Test Samples	Operator Operator	Electrical Characteristics	100%	IC Tester	Operator
26 Reliability Assurance Test		Every Month						
27 In-Warehouse Inspection		Every Day Before Testing	P.M. Jig. Test Samples		Electrical Characteristics	Every Lot	IC Tester	Inspector
					Visual (Major)	Every Lot	(Naked Eye) and Microscope	Inspector
					Visual (Minor)	Every Lot	(Naked Eye)	Inspector
28 Warehousing								

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Appendix 2
Typical Reliability Assurance Tests

The life tests performed by NEC consist of high temperature operating/bias life (HTOL/HTB), high temperature storage life (HTSL), high temperature/high humidity (T/H), and high humidity storage life (HHSL) tests. Additionally, various environmental and mechanical tests are performed. The table below shows the conditions of the various life tests, environmental tests, and mechanical tests.

Test Item	Symbol	MIL-STD-883C Method	Condition	Remarks
High Temperature Operating/Bias Life	HTOL/HTB	1005	T_A = 125°C, V_{DD} specified per device type	(Note 1)
High Temperature Storage Life	HTSL	1008	T_A = 150°C	(Note 1)
High Temperature/ High Humidity	T/H		T_A = 85°C, RH = 85%, V_{DD} = 5.5 V	(Note 1)
High Humidity Storage Life	HHSL		T_A = 85°C, RH = 85%	(Note 1)
Pressure Cooker	PCT		T_A = 125°C, P = 2.3 atm	(Note 1)
Temperature Cycling	T/C	1010	– 65°C to 150°C, 1 hr/cycle	(Note 1)
Lead Fatigue	C3	2004	90° bends. 3 bends without breaking	(Note 2)
Solderability	C4	2003	230°C, 5 sec, Rosin Base Flux	(Note 3)
Soldering Heat/ Temperature Cycle/ Thermal Shock	C6	(Note 4) 1010 1011	260°C, 10 sec, Rosin Base Flux/ 10-1 hr cycles, –65°C to 150°C/ 15-10 min cycles, 0°C to 100°C	(Note 1)

Notes:

(1) Electrical test per data sheet is performed. Devices that exceed the data sheet limits are considered to be rejects.

(2) Broken lead is considered to be a reject.

(3) Less than 95% coverage is considered to be a reject.

(4) MIL-STD-750A, method 2031.

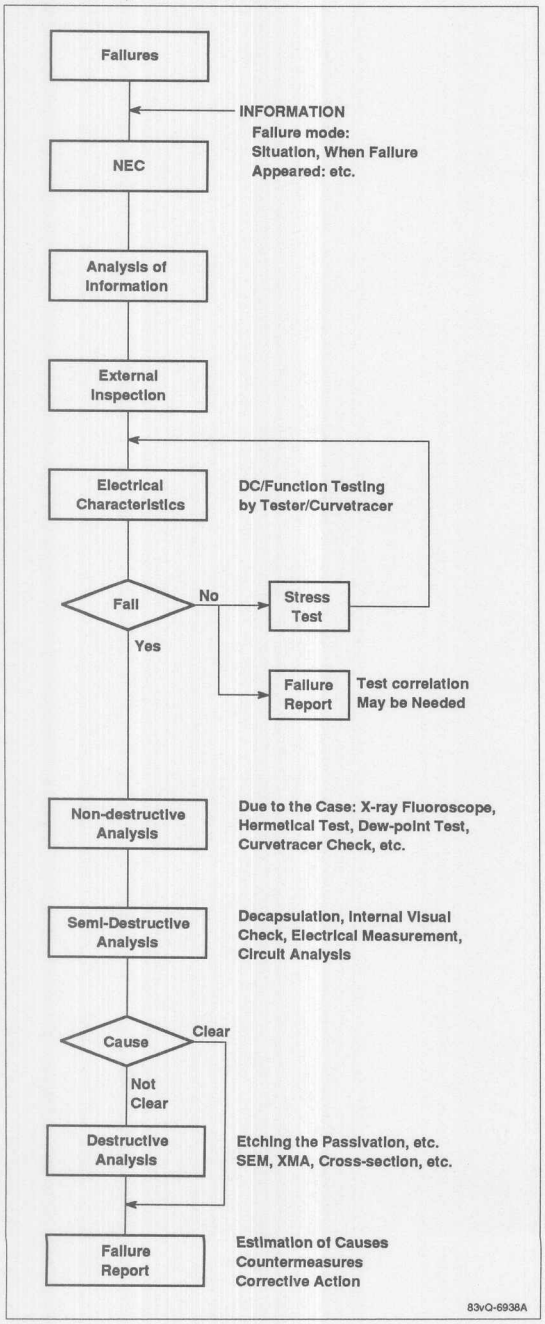
NEC

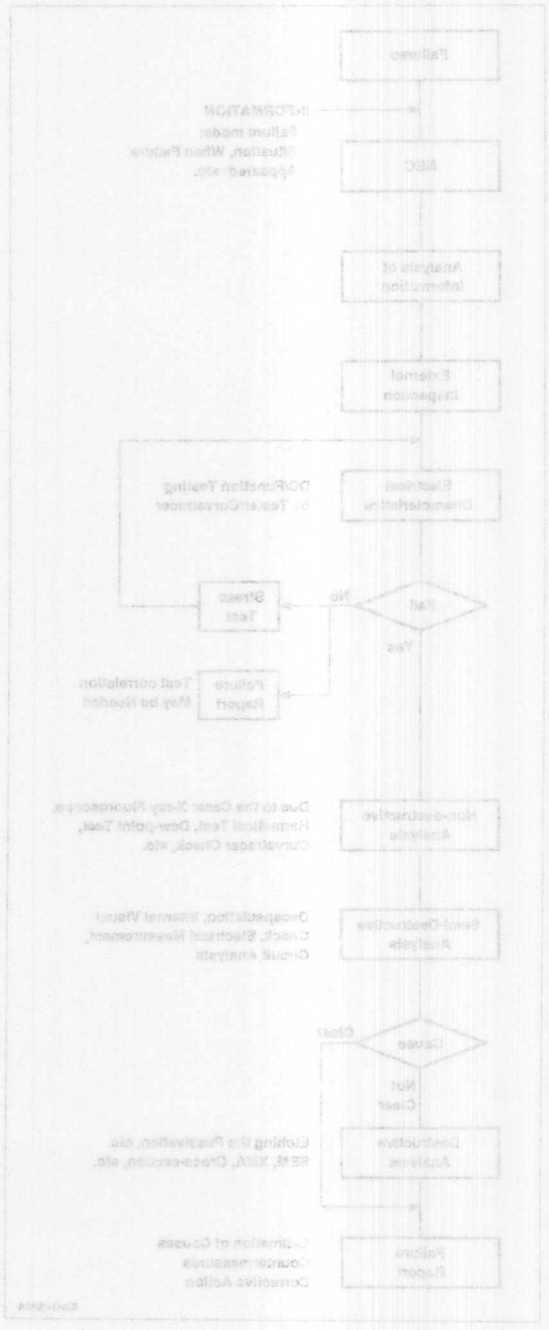
Appendix 3
New Product / Process Change Tests

Test Item	Test Conditions	Sample Size	Newly Developed Product	Shrink Die	New Package	Wafer	Assembly
High Temp. Operating Life	See Appendix 2, 1000H	20 to 50 pcs X 1 to 3 lots	0	0	0	0	0
High Temp. Storage Life	T = 150°C (Plastic), 175°C (Ceramic), 1000H	10 to 20 pcs X 1 to 3 lots	0	0	0	0	0
High Temp. and Humidity Bias Life (Plastic Device)	See Appendix 2, 1000H	20 to 50 pcs X 1 to 3 lots	0	0	0	0	0
Pressure cooker (Plastic Device)	See Appendix 2, 288H	10 to 20 pcs X 1 to 3 lots	0	0	0	0	0
Thermal Environmental	See Appendix 2	10 to 20 pcs X 1 to 3 lots	0	X	0	X	0
Mechanical Environmental (Ceramic Device)	20G, 10 to 2000 Hz 1500G, 0.5 ms 20000G, 1 min	10 to 20 pcs X 1 to 3 lots	0	X	0	X	0
Lead Fatigue	See Appendix 2	5 pcs X 1 to 3 lots	X	—	X	—	X
Solderability	See Appendix 2	5 pcs X 1 to 3 lots	X	—	X	—	X
ESD	(1) C = 200 pF, R = 0Ω (2) C = 100 pF, R = 1.5 KΩ	20 pcs X 1 to 3 lots	0	0	X	0	X
Long Term T/C	See Appendix 2, 1000 cy	10 to 50 pcs X 1 to 3 lots	0	0	0	0	0

0 – Performed X – Perform if Necessary — – Not Performed

Appendix 4
Failure Analysis Flowchart





Application-Specific Devices

Section 3
Application-Specific Devices

μPD41264 3-1
65,536 x 4-Bit Dual-Port Graphics Buffer

μPD42264 3-25
65,536 x 4-Bit Dual-Port Graphics Buffer

μPD42273 3-47
262,144 x 4-Bit Dual-Port Graphics Buffer

μPD42274 3-71
262,144 x 4-Bit Dual-Port Graphics Buffer

μPD42275 3-99
131,072 x 8-Bit Dual-Port Graphics Buffer

μPD42101 3-133
910 x 8-Bit Line Buffer for NTSC TV

μPD42102 3-151
1,135 x 8-Bit Line Buffer for PAL TV

μPD42505 3-161
5,048 x 8-Bit Line Buffer for Communications Systems

μPD42270 3-177
910 x 263 x 4-Bit NTSC Field Buffer

μPD42272 3-201
Picture-In-Picture Generator

μPD42532 3-207
32,768 x 8-Bit Bidirectional Data Buffer

μPD42601 3-227
1,048,576-Bit Silicon File

μPD43501 3-239
1,024-Channel Time Division Switch

μPD43608 3-245
Single-Chip Cache Subsystem

μPD71641 3-251
Cache Memory Controller

μPD72120 3-253
Advanced Graphics Display Controller

μPD72123 3-255
Advanced Graphics Display Controller II

μPD72185 3-257
Advanced Compression/Expansion Engine

μPD7220A 3-259
High-Performance Graphics Display Controller

Application Note 54 3-263
μPD42505 Line Buffer for Communications System

Application Note 55 3-273
μPD411011/μPD41102 High-Speed Line Buffers

Application Note 56 3-289
μPD42601 Silicon File

Application Note 57 3-297
μPD41101/μPD41102/μPD42505 High-Speed Line Buffers

Application Note 58 3-307
Interlaced to Noninterlaced Scan Conversion Using the μPD41101 High-Speed Line Buffer

Application Note 89-15 3-325
Computer Graphics Overview

Application Note 89-16 3-337
Frame Buffer Architecture

Application Note 90-01 3-359
Realism in Computer Graphics

Application Note 90-02 3-367
High Performance Systems

Application Note 90-03 3-377
Memory Systems Overview

Application Note 90-06 3-399
Silicon File System Architecture

Additional New Product Information

Device Number	Description	Comments
Application-Specific Devices		
μPD42273	256K x 4-bit dual-port graphics buffer	New speed of 80 ns
μPD42274	256K x 4-bit dual-port graphics buffer with flash write option	New speed of 80 ns
MC-42256D32V	256K x 32-bit dual-port graphics buffer SIMM with flash write option	80 pins, leaded, zig-zag configuration
MC-42601EA9B-60L	1M x 9-bit silicon file SIMM	30 pins, socket-mountable
μPD42271	7568 x 18-bit picture-in-picture generator	Same as μPD42272, except no colored frame on inset picture
μPD42641	4M x 1-bit silicon file	New in first half of 1991, with speeds to 80 ns
μPD42644	1M x 4-bit silicon file	New in first half of 1991, with speeds to 80 ns

μPD41264
Dual-Port Graphics Buffer

Description

The μPD41264 is a dual-port graphics buffer equipped with a 64K x 4-bit random access port and a 256 x 4-bit serial read port. The serial read port is connected to an internal 1024-bit data register through a 256 x 4-bit serial read output circuit. The random access port is used by the host CPU to read or write data addressed in any desired order and has a write-per-bit option that allows each of the four data bits to be individually selected or masked for a write cycle.

The μPD41264 features fully asynchronous dual access, except when transferring stored graphics data from a selected row of the storage array to the data register. During a data transfer, the random access port requires a special timing cycle using a transfer clock, while the serial read port continues to operate normally. Following the clock transition of a data transfer, serial read output data changes from an old line to a new line and the starting location on the new line is addressable in the data transfer cycle.

The μPD41264 is fabricated with a double polylayer, N-channel, silicon gate process that provides high storage cell density, high performance, and high reliability. Refreshing is accomplished by means of $\overline{RAS}$-only refresh cycles or by normal read or write cycles on the 256 address combinations of A_0 through A_7 during a 4-ms period. Automatic internal refreshing, by means of either hidden refreshing or the $\overline{CAS}$ before $\overline{RAS}$ timing and on-chip refresh circuitry, is also available. The transfer of a row of data from the storage array to the data register also refreshes that row automatically.

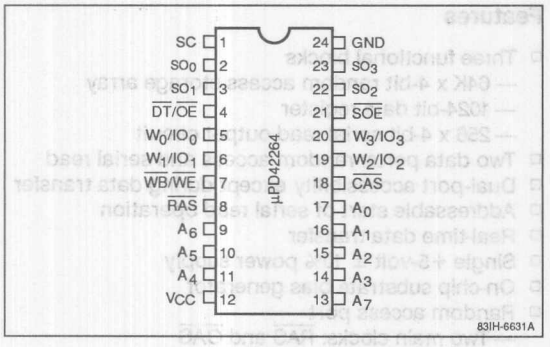
All inputs and outputs, including clocks, are TTL-compatible. All address and data-in signals are latched on-chip to simplify system design. Data-out is unlatched to allow greater system flexibility. The μPD41264 is available in a 24-pin plastic DIP, or 24-pin plastic ZIP, and is guaranteed for operation at 0 to +70°C.

Features

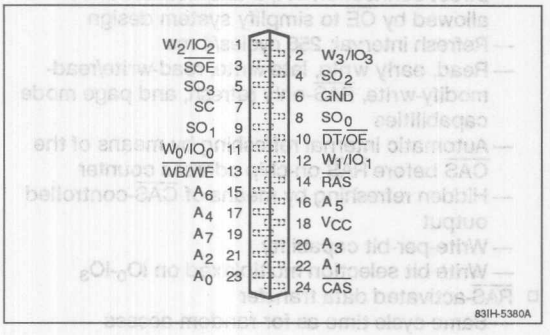
- Three functional blocks
  - 64K x 4-bit random access storage array
  - 1024-bit data register
  - 256 x 4-bit serial read output circuit
- Two data ports: random access and serial read
- Dual-port accessibility except during data transfer
- Addressable start of serial read operation
- Real-time data transfer
- Single +5-volt ± 10% power supply
- On-chip substrate bias generator
- Random access port
  - Two main clocks: $\overline{RAS}$ and $\overline{CAS}$
  - Multiplexed address inputs
  - Direct connection of I/O and address lines allowed by $\overline{OE}$ to simplify system design
  - Refresh interval: 256 cycles/4 ms
  - Read, early write, late write, read-write/read-modify-write, $\overline{RAS}$-only refresh, and page mode capabilities
  - Automatic internal refreshing by means of the $\overline{CAS}$ before $\overline{RAS}$ on-chip address counter
  - Hidden refreshing by means of $\overline{CAS}$-controlled output
  - Write-per-bit capability
  - Write bit selection multiplexed on IO_0-IO_3
- $\overline{RAS}$-activated data transfer
  - Same cycle time as for random access
  - Row data transferred to data register as specified by row address inputs
  - Starting location of following serial read operation specified by column address inputs
  - Transfer of 1024 bits of data on one row to the data register, and the starting location of the serial read circuit, activated by a low-to-high transition of $\overline{DT}$
  - Data transfer during real-time operation or standby of serial port
- Fast serial read operation by means of SC pins
  - Serial data presented on SO_0-SO_3
  - Direct connection of multiple serial outputs for extension of data length
- Fully TTL-compatible inputs, outputs, and clocks
- Three-state outputs for random and serial access
- 24-pin plastic DIP and 24-pin plastic ZIP packaging

Pin Configurations

24-Pin Plastic DIP and SOJ



24-Pin Plastic ZIP



Ordering Information

Part Number	Row Access Time (max)	Serial Access Time (max)	Package
μPD41264C-12	120 ns	40 ns	24-pin plastic DIP
C-15	150 ns	60 ns	
μPD41264V-12	120 ns	40 ns	24-pin plastic ZIP
V-15	150 ns	60 ns	

Pin Identification

Symbol	Function
A_0 - A_7	Address inputs
$\overline{CAS}$	Column address strobe
$\overline{DT/OE}$	Data transfer/output enable
$\overline{RAS}$	Row address strobe
SC	Serial control
SO_0 - SO_3	Serial read outputs
$\overline{SOE}$	Serial output enable
W_0/IO_0 - W_3/IO_3	Write-per-bit inputs/data inputs and outputs
GND	Ground
$\overline{WB/WE}$	Write-per-bit/write enable
V_{CC}	+5-volt power supply

Recommended Operating Conditions

Parameter	Symbol	Min	Typ	Max	Unit
Supply voltage	V_{CC}	4.5	5.0	5.5	V
Input voltage, high	V_{IH}	2.4		5.5	V
Input voltage, low	V_{IL}	−1.0		0.8	V
Operating temperature	T_A	0		70	°C

Absolute Maximum Ratings

Voltage on any pin except V_{CC} relative to GND, V_{R1}	−1.0 to +7.0 V
Voltage on V_{CC} relative to GND, V_{R2}	−1.0 V to +7.0 V
Operating temperature, T_{OPR}	0 to +70°C
Storage temperature, T_{STG}	−55 to +125°C
Short-circuit output current, I_{OS}	50 mA
Power dissipation, P_D	1.5 W

Exposure to Absolute Maximum Ratings for extended periods may affect device reliability; exceeding the ratings could cause permanent damage. The device should be operated within the limits specified under DC and AC Characteristics.

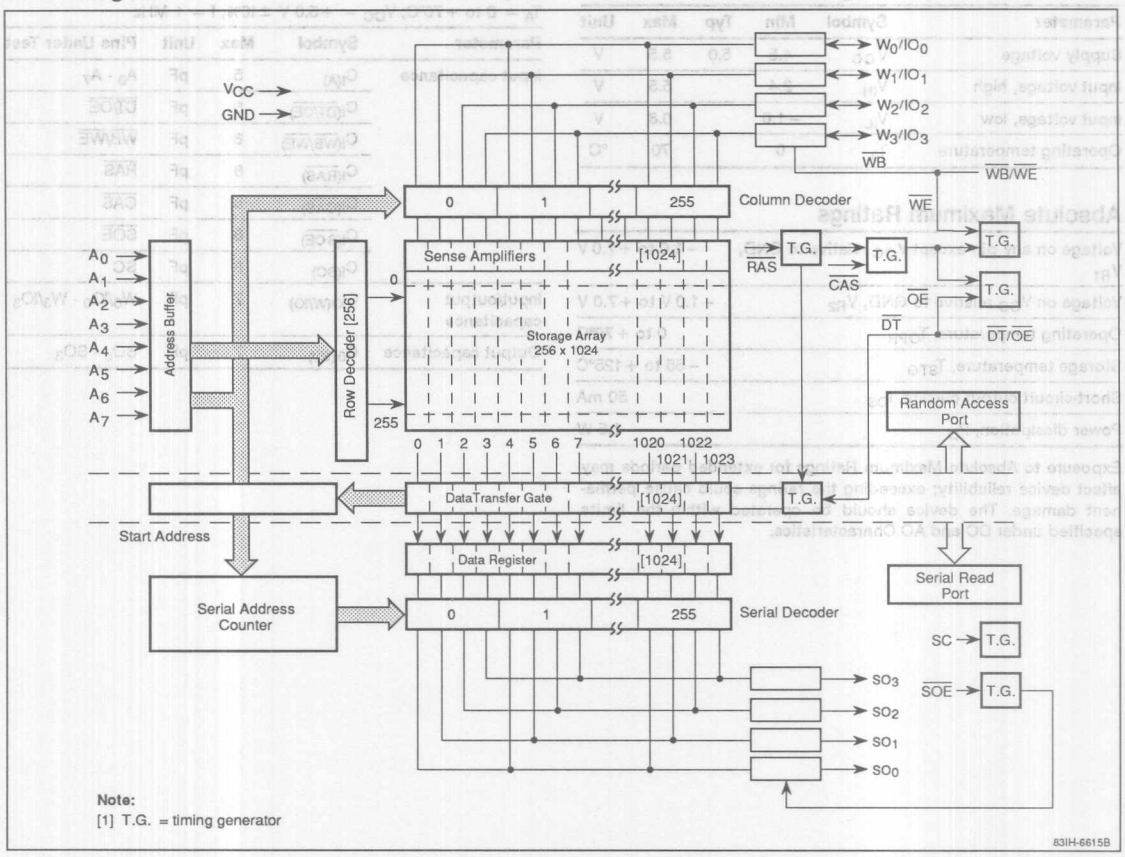
Capacitance

T_A = 0 to +70°C; V_{CC} = +5.0 V ±10%; f = 1 MHz

Parameter	Symbol	Max	Unit	Pins Under Test
Input capacitance	$C_{I(A)}$	5	pF	A_0 - A_7
	$C_{I(\overline{DT}/\overline{OE})}$	6	pF	$\overline{DT}/\overline{OE}$
	$C_{I(\overline{WB}/\overline{WE})}$	8	pF	$\overline{WB}/\overline{WE}$
	$C_{I(\overline{RAS})}$	8	pF	$\overline{RAS}$
	$C_{I(\overline{CAS})}$	8	pF	$\overline{CAS}$
	$C_{I(\overline{SOE})}$	8	pF	$\overline{SOE}$
	$C_{I(SC)}$	8	pF	SC
Input/output capacitance	$C_{IO(W/IO)}$	7	pF	W_0/IO_0 - W_3/IO_3
Output capacitance	$C_{O(SO)}$	7	pF	SO_0 - SO_3

3

Block Diagram



Device Operation

The μPD41264 has a random access port and a serial read port. The random access port executes standard read/write cycles as well as data transfer cycles, all of which are based on conventional $\overline{RAS}$/$\overline{CAS}$ timing. In a data transfer, data in each storage cell on the selected row is transferred simultaneously through a transfer gate to the corresponding register location. The serial read port shows the contents of the data register in serial order. The random access and serial read ports can operate asynchronously, except when the transfer gate is turned on during the data transfer period.

Addressing

The storage array is a 256-row by 1024-column matrix. Each of 4 data bits in the random access port corresponds to 65,536 storage cells, and 16 address bits are required to decode one cell location. Eight row address bits are set up on pins A_0 through A_7 and latched onto the chip by $\overline{RAS}$. Eight column address bits then are set up on pins A_0 through A_7 and latched onto the chip by $\overline{CAS}$. All addresses must be stable, on or before the falling edges of $\overline{RAS}$ and $\overline{CAS}$.

$\overline{RAS}$ is similar to a chip enable signal; whenever it is activated, 1024 cells on the selected row are sensed simultaneously and the sense amplifiers automatically restore the data. $\overline{CAS}$ is a chip selection signal that activates the column decoder and input/output buffers.

Through 1 of 256 column decoders, 4 storage cells on a row are connected to 4 data buses, respectively. In a data transfer cycle, 8 row address bits are used to select 1 of the 256 possible rows involved in the transfer of data to the data register. Eight column address bits are then used to select the 1 of 256 possible serial decoders that corresponds to the starting location of the next serial read cycle. In the serial read port, when SC is activated, 4 data bits in the 1024-bit data register are transferred to 4 serial data buses and read out. Activating SC repeatedly causes a serial read cycle (starting from the location specified in the data transfer) to be executed within the 1024 bits in the data register.

Random Access Port

An operation in the random access port begins with a negative transition of $\overline{RAS}$. Both $\overline{RAS}$ and $\overline{CAS}$ have minimum pulse widths, as specified in the timing table, which must be maintained for proper device operation and data integrity. Once begun, a cycle must meet all specifications, including minimum cycle time. To reduce the number of pins, the following functions are multi-plexed in the random access port:

- $\overline{DT}/\overline{OE}$
- $\overline{WB}/\overline{WE}$
- W_i/IO_i (i = 0, 1, 2, 3)

The $\overline{OE}$, $\overline{WE}$ and IO_i functions represent standard operations while $\overline{DT}$, $\overline{WB}$, and W_i are special inputs to be applied in the same way as row address inputs, with setup and hold times referenced to the negative transition of $\overline{RAS}$. The $\overline{DT}$ level determines whether a cycle is a random access operation or a data transfer operation. $\overline{WB}$ affects only write cycles and determines whether or not the write-per-bit option is used. W_i defines data bits to be written with the write-per-bit capability. In the following discussions, these multiplexed pins are designated as $\overline{DT}(/\overline{OE})$, for example, depending on the function being described.

To use the μPD41264 for random access, $\overline{DT}(/\overline{OE})$ must be high as $\overline{RAS}$ falls. Holding $\overline{DT}(/\overline{OE})$ high disconnects the 1024-bit data register from the corresponding 1024-digit lines of the storage array. Conversely, to execute a data transfer, $\overline{DT}(/\overline{OE})$ must be low as $\overline{RAS}$ falls to open the 1024 data transfer gates and transfer data from one of the rows to the data register.

Read Cycle. A read cycle is executed by activating $\overline{RAS}$, $\overline{CAS}$, and $\overline{OE}$ and maintaining $(\overline{WB}/)\overline{WE}$ high while $\overline{CAS}$ is active. The $(W_i/)IO_i$ data pin (i = 0, 1, 2, 3) remains in high impedance until valid data appears at the output at access time. Device access time, t_{ACC}, is the longest of the following three calculated intervals:

- t_{RAC}
- $\overline{RAS}$ to $\overline{CAS}$ delay (t_{RCD}) + t_{CAC}
- $\overline{RAS}$ to $\overline{OE}$ delay + t_{OEA}

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Access times from $\overline{RAS}$ (t_{RAC}), from $\overline{CAS}$ (t_{CAC}), and from $\overline{OE}$ (t_{OEA}) are device parameters. The $\overline{RAS}$ to $\overline{CAS}$ and $\overline{RAS}$ to $\overline{OE}$ delays are system-dependent timing parameters.

Output becomes valid after the access time has elapsed and it remains valid while both $\overline{CAS}$ and $\overline{OE}$ are low. $\overline{CAS}$ or $\overline{OE}$ high returns the output to high impedance.

Write Cycle. A write cycle is executed by bringing ($\overline{WB}$/)$\overline{WE}$ low during the $\overline{RAS}$/$\overline{CAS}$ cycle. The falling edge of $\overline{CAS}$ or ($\overline{WB}$/)$\overline{WE}$ strobes the data on (W_i/)IO_i into the on-chip data latch. To make use of the write-per-bit capability, $\overline{WB}$(/$\overline{WE}$) must be low as $\overline{RAS}$ falls. In this case, data bits targeted for write operation can be specified by keeping W_i(/IO_i) high, with setup and hold times referenced to the negative transition of $\overline{RAS}$.

For those data bits of W_i(/IO_i) that are kept low as $\overline{RAS}$ falls, write operation is inhibited on the chip. If $\overline{WB}$(/$\overline{WE}$) is high as $\overline{RAS}$ falls, the write-per-bit option is not used and a write cycle is executed for all four data bits.

Early Write Cycle. An early write cycle is executed by bringing ($\overline{WB}$/)$\overline{WE}$ low before $\overline{CAS}$. Data is strobed by $\overline{CAS}$, with setup and hold times referenced to this signal, and the output remains in high impedance for the entire cycle. As $\overline{RAS}$ falls, ($\overline{DT}$/)$\overline{OE}$ must meet the setup and hold times of a high $\overline{DT}$, but otherwise ($\overline{DT}$/)$\overline{OE}$ does not affect any circuit operation while $\overline{CAS}$ is active.

Read-Write/Read-Modify-Write Cycle. Bringing the ($\overline{WB}$/)$\overline{WE}$ signal low with $\overline{RAS}$ and $\overline{CAS}$ low executes this cycle. (W_i/)IO_i shows read data at access time. Afterward, in preparation for the upcoming write cycle, (W_i/)IO_i is returned to high impedance by a high ($\overline{DT}$/)$\overline{OE}$. The data to be written is strobed by ($\overline{WB}$/)$\overline{WE}$, with setup and hold times referenced to this signal.

Late Write Cycle. This cycle shows the timing flexibility of ($\overline{DT}$/)$\overline{OE}$, which can be activated just after ($\overline{WB}$/)$\overline{WE}$ falls, even when ($\overline{WB}$/)$\overline{WE}$ is brought low after $\overline{CAS}$.

Refresh Cycle. A cycle at each of the 256 row addresses (A_0 through A_7) will refresh all storage cells. Any cycle in the random access port (i.e., read, write, refresh, or data transfer) refreshes the 1024 bits selected by the $\overline{RAS}$ addresses or by the on-chip refresh address counter.

$\overline{RAS}$-only Refresh Cycle. A cycle having only $\overline{RAS}$ active refreshes one row of the storage array. A high $\overline{CAS}$ is maintained while $\overline{RAS}$ is active to keep (W_i/)IO_i in a state of high impedance. This cycle is preferred for refreshing, especially when the host system consists of multiple rows of random access devices. The data outputs may be OR-tied with no bus contention when $\overline{RAS}$-only refresh cycles are executed.

$\overline{CAS}$ Before $\overline{RAS}$ Refresh Cycle. This cycle executes internal refreshing using the on-chip control circuitry. Whenever $\overline{CAS}$ is low as $\overline{RAS}$ falls, this circuitry automatically refreshes the row addresses specified by the internal address counter. In this cycle, the circuit operation based on $\overline{CAS}$ is maintained in a reset state. When internal refreshing is complete, the address counter automatically increments in preparation for the next $\overline{CAS}$ before $\overline{RAS}$ cycle.

Hidden Refresh Cycle. This function performs hidden refreshing after a read cycle, without disturbing the read data output. Once valid, the data output is controlled by $\overline{CAS}$ and $\overline{OE}$. After the read cycle, $\overline{CAS}$ is held low while $\overline{RAS}$ goes high for precharging. A $\overline{RAS}$-only cycle is then executed (except that $\overline{CAS}$ is held low instead of high) and the data output remains valid. Since hidden refreshing is the same as $\overline{CAS}$ before $\overline{RAS}$ refreshing, the data output remains valid during either operation.

Fast-Page Cycle. This feature allows faster data access by keeping the same row address while successive column addresses are strobed onto the chip. By maintaining $\overline{RAS}$ low while successive $\overline{CAS}$ cycles are executed, data is transferred at a faster rate because $\overline{RAS}$ addresses are maintained internally and do not have to be reapplied. During this operation, it is also possible to execute read, write and read-write/read-modify-write cycles. Additionally, the write-per-bit control specified in the entry write cycle is maintained through the following fast-page write cycle.

Data Transfer Cycle. A data transfer cycle is executed by bringing $\overline{DT}(/\overline{OE})$ low as $\overline{RAS}$ falls. The specified 1 of the possible 256 rows involved in the data transfer, aswell as the starting location of the following serial read cycle in the serial read port, are defined by address inputs. $\overline{DT}(/\overline{OE})$ must be low for a specified time, measured from $\overline{RAS}$ and $\overline{CAS}$, so that the data transfer condition may be satisfied . The low-to-high transition of $\overline{DT}$ causes two transfer operations through the data transfer gates: column address buffer outputs are transferred to the serial address counters, and storage cell data amplified on digit lines is transferred to the data register. At least one SC cycle is required to hold the data in the register. Otherwise, the beginning of the next transfer cycle destroys the newly transferred data. $\overline{RAS}$ and $\overline{CAS}$ must be low during these operations to keep the transferred data in the random access port.

Serial Read Port

The serial read port is used only to read serially the contents of the data register starting from a specified location. The entire operation, therefore, follows a data transfer cycle. Data stored in the serial register remains valid for a minimum of 4 ms after the transfer cycle. The only condition under which the serial read port must synchronize with the random access port is when the positive transition of $\overline{DT}(/\overline{OE})$ must occur within a specified period in an SC cycle. Except for this SC cycle, the serial read port can operate asynchronously with the random access port. The output data appears at SO_i after an access time of t_{SCA}, measured from SC high, only when $\overline{SOE}$ is maintained low. The SC cycle that includes the positive transition of $\overline{DT}(/\overline{OE})$ shows old data in the data register; subsequent SC cycles show new data transferred to the data register serially and in a looped manner. The serial output is maintained until the next SC signal is activated. $\overline{SOE}$ controls the impedance of the serial output to allow multiplexing of more than one bank of μPD41264 graphics buffers into the same external circuitry. When $\overline{SOE}$ is low, SO_i is enabled and the proper data is read. When $\overline{SOE}$ is at a high logic level, SO_i is disabled and in a state of high impedance.

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DC Characteristics

T_A = 0 to +70°C; V_{CC} = 5.0 V ±10%

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions
Input leakage current	I_{IL}	−10		10	μA	V_{IN} = 0 to 5.5 V; all other pins not under test = 0 V
Output leakage current	I_{OL}	−10		10	μA	D_{OUT} (IO_i, SO_i) disabled; V_{OUT} = 0 to 5.5 V
Random access port output voltage, high	$V_{OH(R)}$	2.4			V	$I_{OH(R)}$ = −2 mA
Random access port output voltage, low	$V_{OL(R)}$			0.4	V	$I_{OL(R)}$ = 4.2 mA
Serial read port output voltage, high	$V_{OH(S)}$	2.4			V	$I_{OH(S)}$ = −2 mA
Serial read port output voltage, low	$V_{OL(S)}$			0.4	V	$I_{OL(S)}$ = 4.2 mA

Power Supply Current

T_A = 0 to +70°C; V_{CC} = +5.0 V ±10%

Random Access Port	Serial Read Port	Symbol	−12 Max	−15 Max	Unit	Test Conditions
Read/write cycle	Standby	I_{CC1}	95	85	mA	$\overline{RAS}$ and $\overline{CAS}$ cycling; $t_{RC} = t_{RC}$ min; IO = 0 mA; SC = $\overline{SOE}$ = V_{IH} (Note 1)
Standby	Standby	I_{CC2}	12	12	mA	$\overline{RAS}$ = V_{IH}; D_{OUT} = high impedance; SC = $\overline{SOE}$ = V_{IH}
$\overline{RAS}$-only refresh cycle	Standby	I_{CC3}	75	65	mA	$\overline{RAS}$ cycling; $\overline{CAS}$ = V_{IH}; $t_{RC} = t_{RC}$ min; SC = $\overline{SOE}$ = V_{IH}
Page cycle	Standby	I_{CC4}	65	55	mA	$\overline{RAS}$ = V_{IL}; $\overline{CAS}$ cycling; $t_{PC} = t_{PC}$ min; SC = $\overline{SOE}$ = V_{IH} (Note 1)
$\overline{CAS}$ before $\overline{RAS}$ refresh cycle	Standby	I_{CC5}	75	65	mA	$\overline{CAS}$ low as $\overline{RAS}$ falls; $t_{RC} = t_{RC}$ min; SC = $\overline{SOE}$ = V_{IH} (Note 1)
Data transfer	Standby	I_{CC6}	120	100	mA	$\overline{DT}$ low as $\overline{RAS}$ falls; $t_{RC} = t_{RC}$ min; SC = $\overline{SOE}$ = V_{IH}
Read/write cycle	Active	I_{CC7}	155	130	mA	$\overline{RAS}$ and $\overline{CAS}$ cycling; $t_{RC} = t_{RC}$ min; $\overline{SOE}$ = V_{IL}; SC cycling; $t_{SCC} = t_{SCC}$ min (Note 1)
Standby	Active	I_{CC8}	60	45	mA	$\overline{RAS}$ = V_{IH}; D_{OUT} = high impedance; $\overline{SOE}$ = V_{IL}; SC cycling; $t_{SCC} = t_{SCC}$ min (Note 1)
$\overline{RAS}$-only refresh cycle	Active	I_{CC9}	135	110	mA	$\overline{RAS}$ cycling; $\overline{CAS}$ = V_{IH}; $t_{RC} = t_{RC}$ min; $\overline{SOE}$ = V_{IL}; SC cycling; $t_{SCC} = t_{SCC}$ min (Note 1)
Page cycle	Active	I_{CC10}	125	100	mA	$\overline{RAS}$ = V_{IL}; $\overline{CAS}$ cycling; $t_{PC} = t_{PC}$ min; $\overline{SOE}$ = V_{IL}; SC cycling; $t_{SCC} = t_{SCC}$ min (Note 1)
$\overline{CAS}$ before $\overline{RAS}$ refresh cycle	Active	I_{CC11}	135	110	mA	$\overline{CAS}$ low as $\overline{RAS}$ falls; $t_{RC} = t_{RC}$ min; $\overline{SOE}$ = V_{IL}; SC cycling; $t_{SCC} = t_{SCC}$ min (Note 1)
Data transfer	Active	I_{CC12}	180	145	mA	$\overline{DT}$ low as $\overline{RAS}$ falls; $t_{RC} = t_{RC}$ min; $\overline{SOE}$ = V_{IL}; SC cycling; $t_{SCC} = t_{SCC}$ min (Note 1)

Notes:

(1) No load on IO_i or SO_i. Except for I_{CC2}, I_{CC3}, and I_{CC6}, real values depend on output loading and cycle rates.

AC Characteristics

T_A = 0 to +70°C; V_{CC} = +5.0 V±10%

Parameter	Symbol	μPD41264-12 Min	μPD41264-12 Max	μPD41264-15 Min	μPD41264-15 Max	Unit	Test Conditions
Column address hold time after $\overline{RAS}$ low	t_{AR}	80		100		ns	
Column address setup time	t_{ASC}	0		0		ns	
Row address setup time	t_{ASR}	0		0		ns	
Access time from $\overline{CAS}$	t_{CAC}		60		75	ns	(Notes 2, 5)
Column address hold time	t_{CAH}	20		25		ns	
$\overline{CAS}$ pulse width	t_{CAS}	60	10,000	75	10,000	ns	

AC Characteristics (cont)

Parameter	Symbol	μPD41264-12 Min	μPD41264-12 Max	μPD41264-15 Min	μPD41264-15 Max	Unit	Test Conditions
$\overline{DT}$ low hold time after $\overline{RAS}$ low	t_{CDH}	40		55		ns	(Note 12)
$\overline{CAS}$ before $\overline{RAS}$ refresh hold time	t_{CHR}	25		30		ns	
$\overline{CAS}$ precharge time (page cycle only)	t_{CP}	50		60		ns	
$\overline{CAS}$ precharge time (nonpage cycle)	t_{CPN}	25		30		ns	
$\overline{CAS}$ high to $\overline{RAS}$ low precharge time	t_{CRP}	10		10		ns	
$\overline{CAS}$ hold time	t_{CSH}	120		150		ns	
$\overline{CAS}$ before $\overline{RAS}$ refresh setup time	t_{CSR}	10		10		ns	
$\overline{CAS}$ to $\overline{WE}$ delay	t_{CWD}	100		120		ns	(Note 10)
Write command to $\overline{CAS}$ lead time	t_{CWL}	40		45		ns	
Data-in hold time	t_{DH}	35		45		ns	(Note 11)
$\overline{DT}$ high hold time	t_{DHH}	20		25		ns	
Data-in hold time after $\overline{RAS}$ low	t_{DHR}	95		120		ns	
$\overline{DT}$ high setup time	t_{DHS}	0		0		ns	
$\overline{DT}$ low setup time	t_{DLS}	0		0		ns	
Data-in setup time	t_{DS}	0		0		ns	(Note 11)
$\overline{DT}$ high to $\overline{CAS}$ high delay	t_{DTC}	10		10		ns	
$\overline{DT}$ high hold time after $\overline{RAS}$ high	t_{DTH}	20		25		ns	
$\overline{DT}$ high to $\overline{RAS}$ high delay	t_{DTR}	10		10		ns	
$\overline{OE}$ pulse width	t_{OE}	35		40		ns	
Access time from $\overline{OE}$	t_{OEA}		30		40	ns	(Note 2)
$\overline{OE}$ to data-in setup delay	t_{OED}	35		40		ns	
$\overline{OE}$ hold time after $\overline{WE}$ low	t_{OEH}	30		40		ns	
$\overline{OE}$ to $\overline{RAS}$ inactive setup time	t_{OES}	10		10		ns	
Output disable time from $\overline{OE}$ high	t_{OEZ}	0	30	0	40	ns	(Note 6)
Output disable time from $\overline{CAS}$ high	t_{OFF}	0	30	0	40	ns	(Note 6)
Page cycle time	t_{PC}	120		145		ns	
Access time from $\overline{RAS}$	t_{RAC}		120		150	nc	(Notes 2, 4)
Row address hold time	t_{RAH}	15		20		ns	
$\overline{RAS}$ pulse width	t_{RAS}	120	10,000	150	10,000	ns	
Random read or write cycle time	t_{RC}	220		270		ns	
$\overline{RAS}$ to $\overline{CAS}$ delay time	t_{RCD}	25	60	30	75	ns	(Note 4)
Read command hold time after $\overline{CAS}$ high	t_{RCH}	0		0		ns	(Note 9)
Read command setup time	t_{RCS}	0		0		ns	
$\overline{DT}$ low hold time after $\overline{RAS}$ low (serial port active)	t_{RDH}	100		130		ns	
Refresh interval	t_{REF}		4		4	ms	
$\overline{RAS}$ precharge time	t_{RP}	90		100		ns	
$\overline{RAS}$ high to $\overline{CAS}$ low precharge time	t_{RPC}	0		0		ns	
Read command hold after $\overline{RAS}$ high	t_{RRH}	20		20		ns	(Note 9)
$\overline{RAS}$ hold time	t_{RSH}	60		75		ns	

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AC Characteristics (cont)

Parameter	Symbol	μPD41264-12 Min	μPD41264-12 Max	μPD41264-15 Min	μPD41264-15 Max	Unit	Test Conditions
Read-write/read-modify-write cycle time	t_{RWC}	300		355		ns	
$\overline{RAS}$ to $\overline{WE}$ delay	t_{RWD}	160		195		ns	(Note 10)
Write command to $\overline{RAS}$ lead time	t_{RWL}	40		45		ns	
SC pulse width	t_{SCH}	10		20		ns	
Serial output access time from SC	t_{SCA}		40		60	ns	(Notes 2, 7)
Serial clock cycle time	t_{SCC}	40	50,000	60	50,000	ns	
SC precharge time	t_{SCL}	10		20		ns	
SC high to $\overline{DT}$ high delay	t_{SDD}	10		20		ns	
SC low hold time after $\overline{DT}$ high	t_{SDH}	10		20		ns	
Serial output access time from $\overline{SOE}$	t_{SOA}		35		50	ns	
$\overline{SOE}$ pulse width	t_{SOE}	15		20		ns	
Serial output hold time after SC high	t_{SOH}	10		10		ns	
$\overline{SOE}$ low to serial output setup delay	t_{SOO}	5		5		ns	
$\overline{SOE}$ precharge time	t_{SOP}	15		20		ns	
Serial output disable time from $\overline{SOE}$ high	t_{SOZ}	0	30	0	40	ns	(Note 6)
Rise and fall transition time	t_T	3	50	3	50	ns	
Write-per-bit hold time	t_{WBH}	20		25		ns	
Write-per-bit setup time	t_{WBS}	0		0		ns	
Write command hold time	t_{WCH}	35		45		ns	
Write command hold time after $\overline{RAS}$ low	t_{WCR}	95		120		ns	
Write command setup time	t_{WCS}	0		0		ns	(Note 10)
Write bit selection hold time	t_{WH}	20		25		ns	
Write command pulse width	t_{WP}	35		45		ns	
Write bit selection setup time	t_{WS}	0		0		ns	

Notes:

(1) See input/output timing waveforms for timing reference voltages.

(2) See figures 1 and 2 for output loads.

(3) An initial pause of 100 μs is required after power-up, followed by any eight $\overline{RAS}$ cycles (except CAS-before-$\overline{RAS}$ cycles), before proper device operation is achieved.

(4) Operation within the t_{RCD} (max) limit ensures that t_{RAC} (max) can be met. The t_{RCD} (max) limit is specified as a reference point only. If t_{RCD} is greater than the specified t_{RCD} (max) limit, access time is controlled exclusively by t_{CAC}.

(5) Assumes that $t_{RCD} \geq t_{RCD}$ (max).

(6) An output disable time defines the time at which the output achieves the open-circuit condition and is not referenced to output voltage levels.

(7) Data in the serial output register remains valid for 4 ms (min) after a data transfer cycle.

(8) V_{IH} (min) and V_{IL} (min) are reference levels for measuring the timing of input signals. Additionally, transition times are measured between V_{IH} and V_{IL}.

(9) Either t_{RRH} or t_{RCH} must be satisfied for a read cycle.

(10) t_{WCS}, t_{CWD}, and t_{RWD} are restrictive operating parameters in read-write and read-modify-write cycles only. If $t_{WCS} \geq t_{WCS}$ (min), the cycle is an early write cycle and the data output will remain open-circuit throughout the entire cycle. If $t_{CWD} \geq t_{CWD}$ (min) and $t_{RWD} \geq t_{RWD}$ (min), the cycle is a read-write cycle and the data output will contain data read from the selected cell. If neither of the above conditions is met, the condition of the data output (at access time and until CAS returns to V_{IH}) is indeterminate.

(11) These parameters are referenced to the falling edge of $\overline{CAS}$ in early write cycles and to the falling edge of (WB/)WE in delayed write or read-modify-write cycles.

(12) Use t_{RDH} and t_{CDH} when the serial port is active and t_{RDH1}, t_{RSD}, t_{CSD} and t_{SSC} if it is in standby.

(13) $\overline{SOE}$ may be tied to GND if the output enable function of the serial port is not needed.

Figure 1. Input Timing

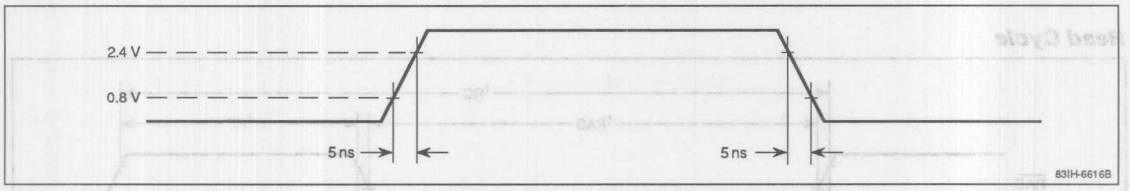


Figure 2. Output Timing

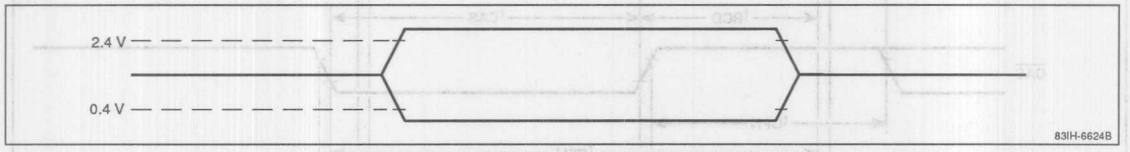


Figure 3. Output Loading in Random Access Port

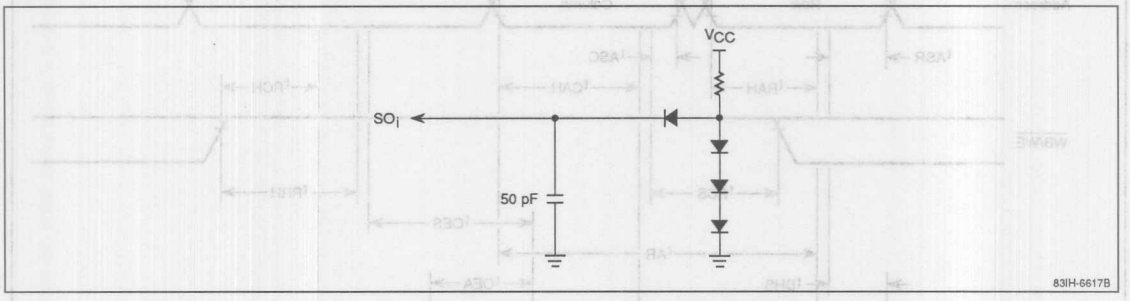
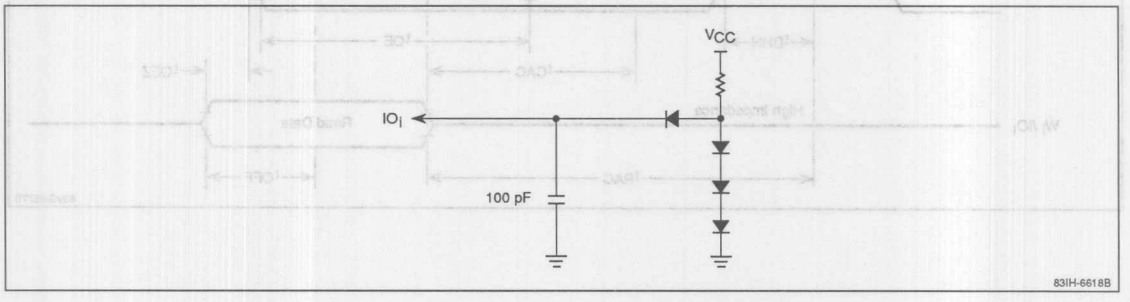


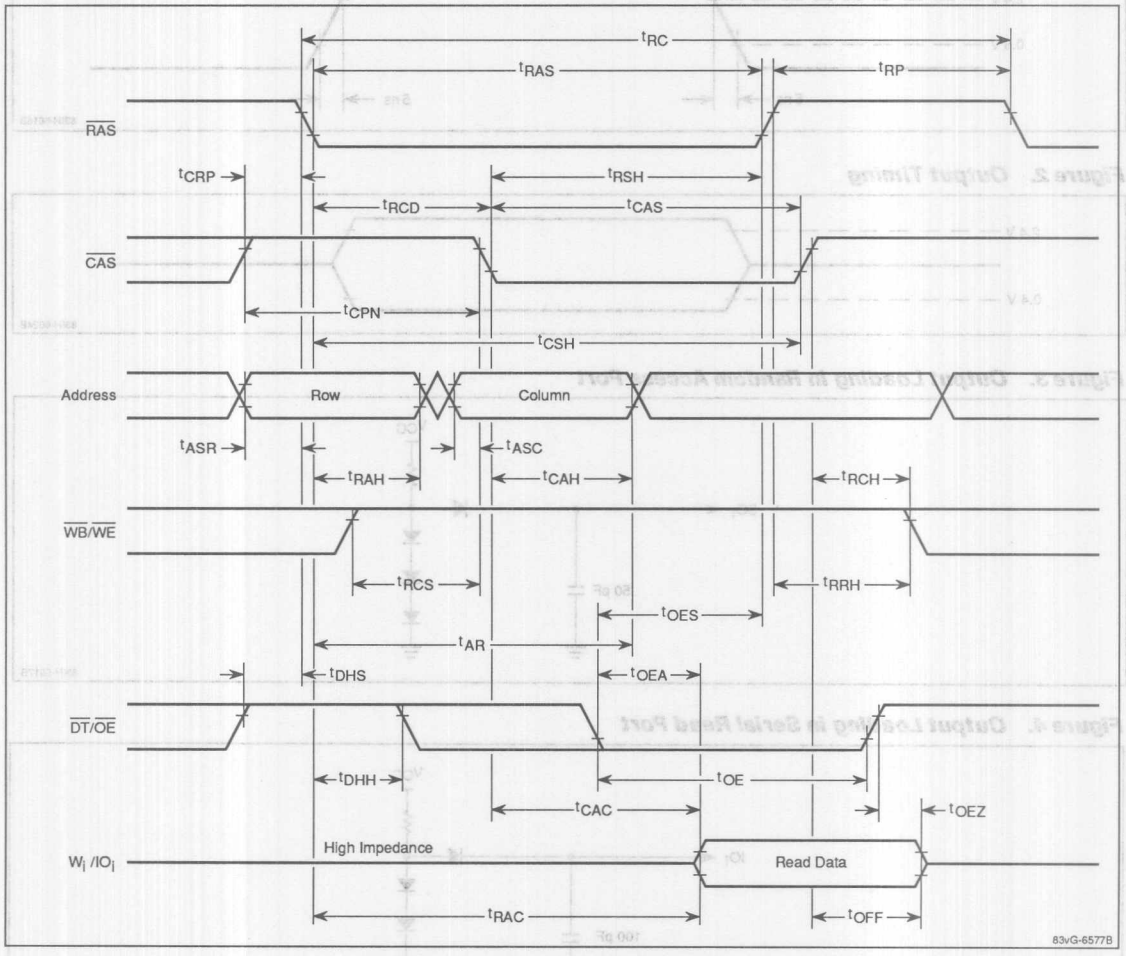
Figure 4. Output Loading in Serial Read Port



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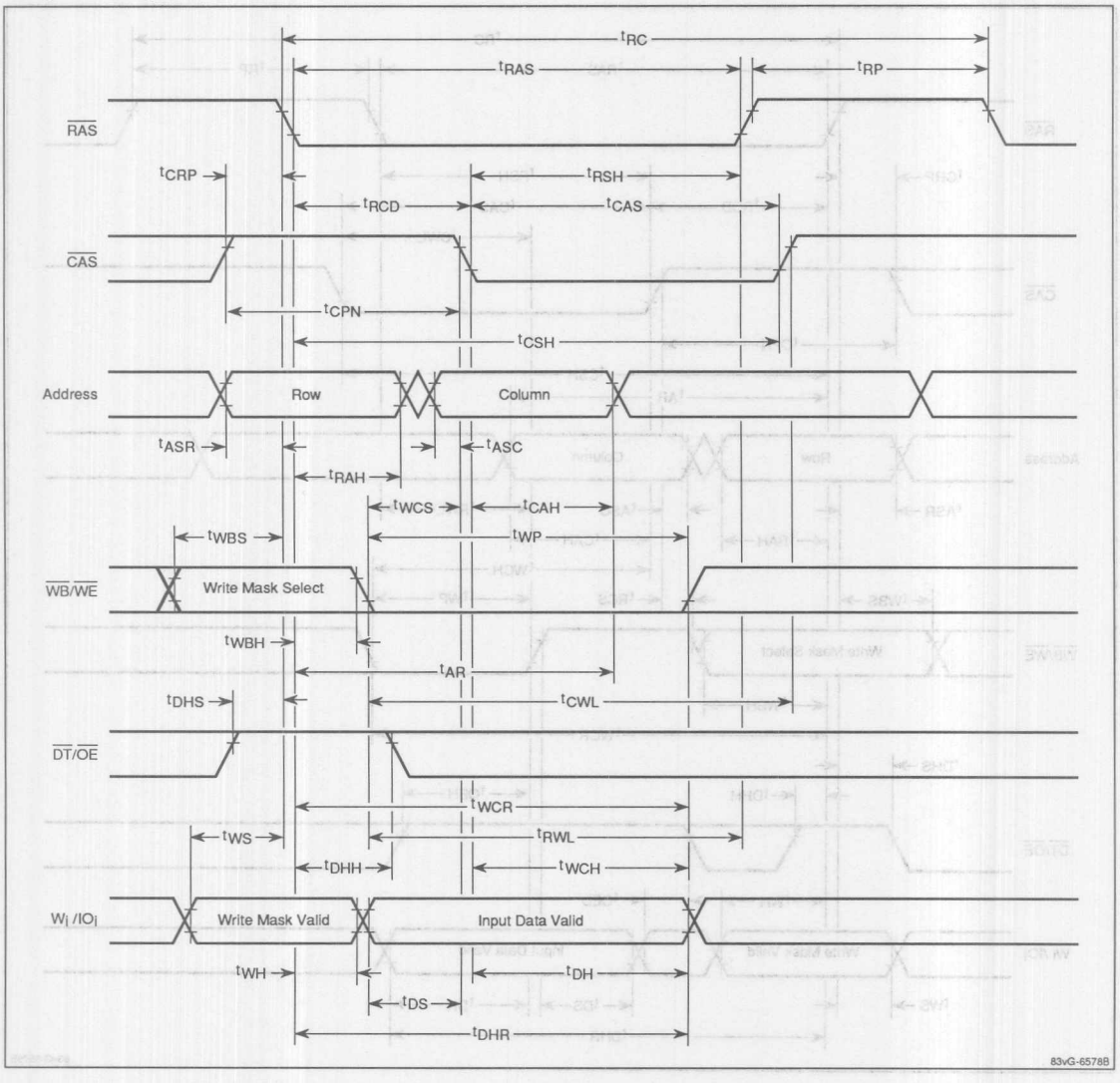
Timing Waveforms

Read Cycle



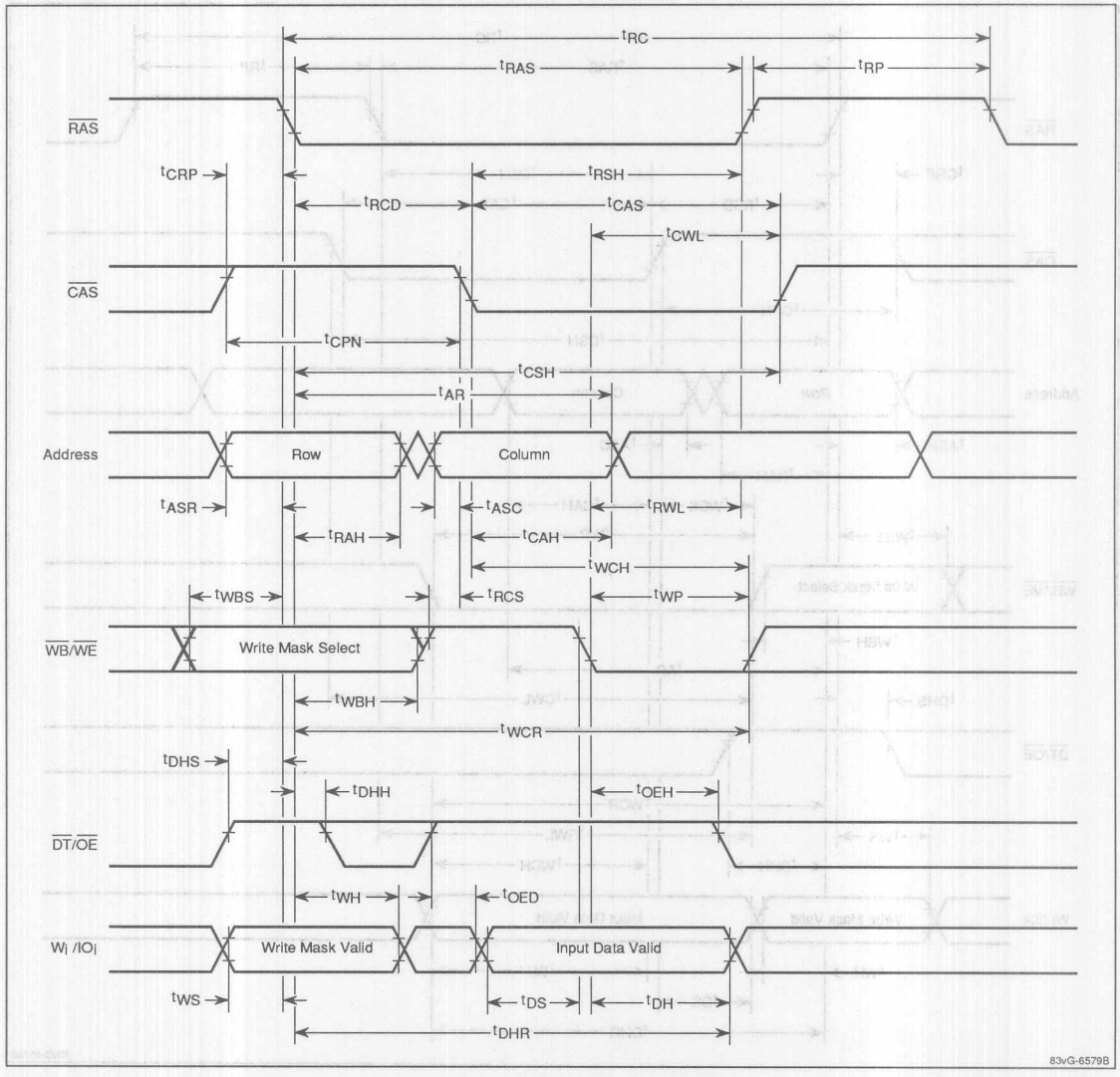
Timing Waveforms (cont)

Early Write Cycle



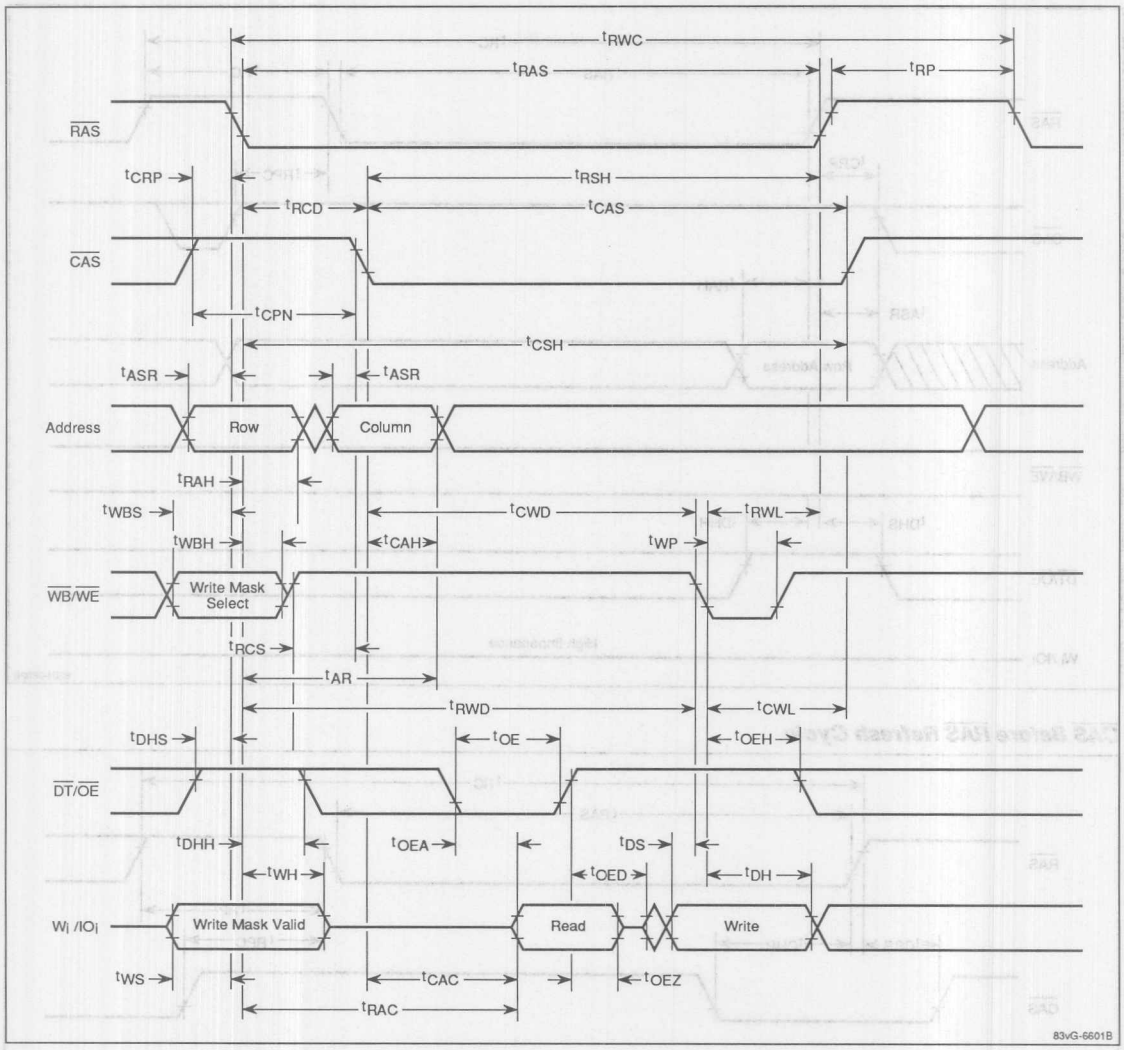
Timing Waveforms (cont)

Late Write Cycle



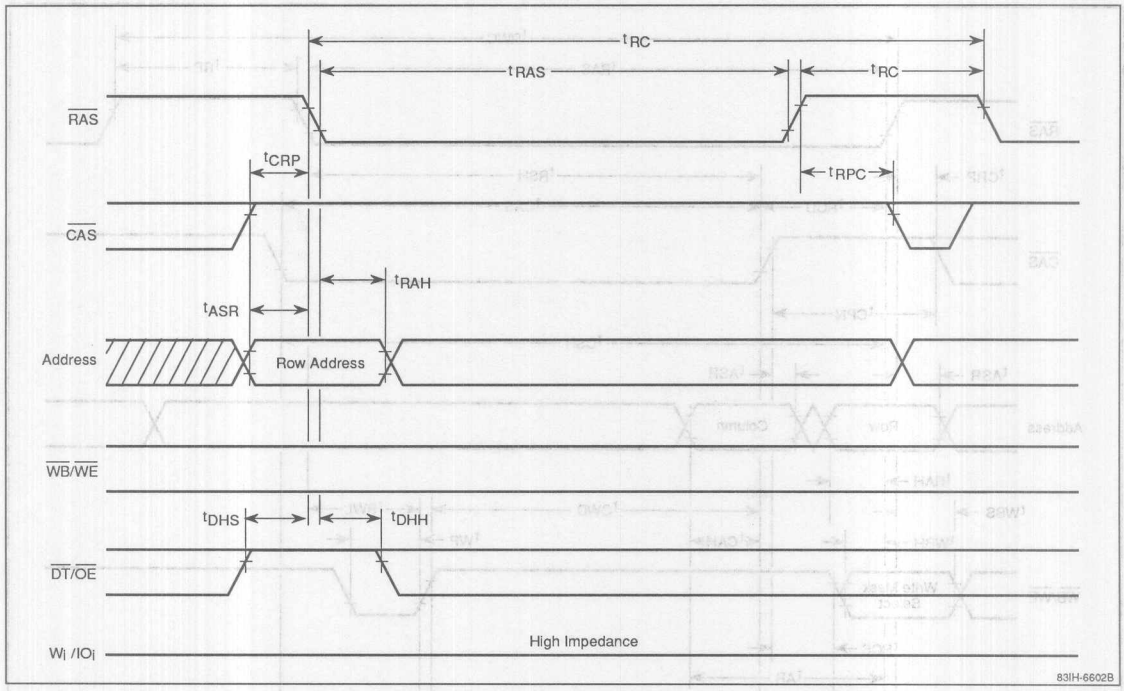
Timing Waveforms (cont)

Read-Write/Read-Modify-Write Cycle

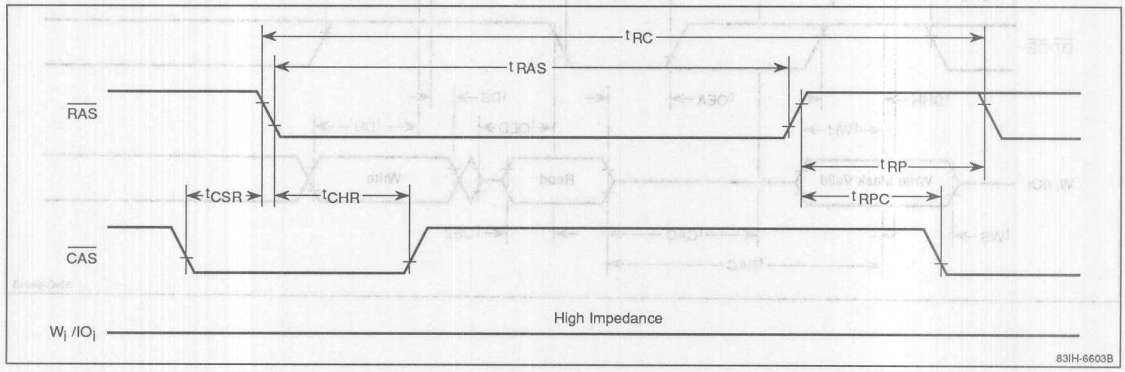


Timing Waveforms (cont)

$\overline{RAS}$-Only Refresh Cycle

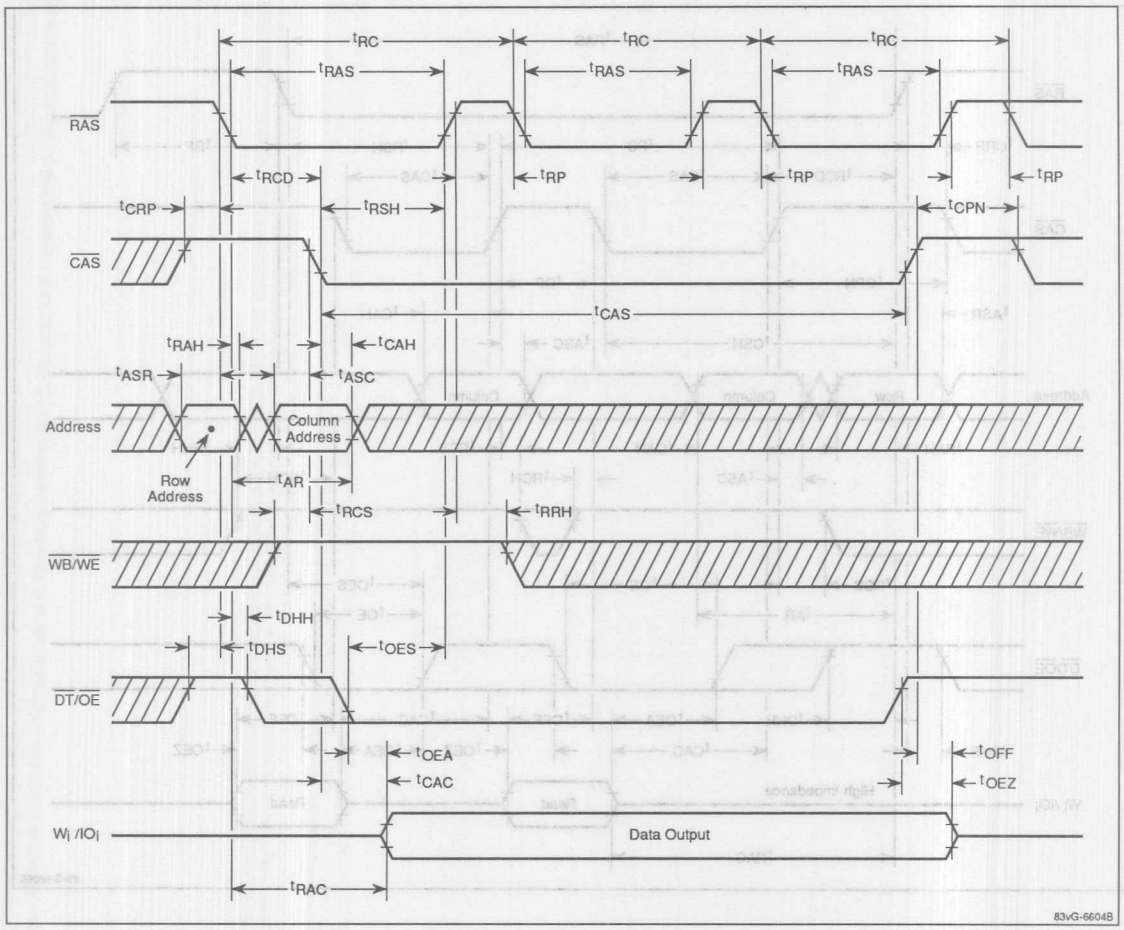


$\overline{CAS}$ Before $\overline{RAS}$ Refresh Cycle



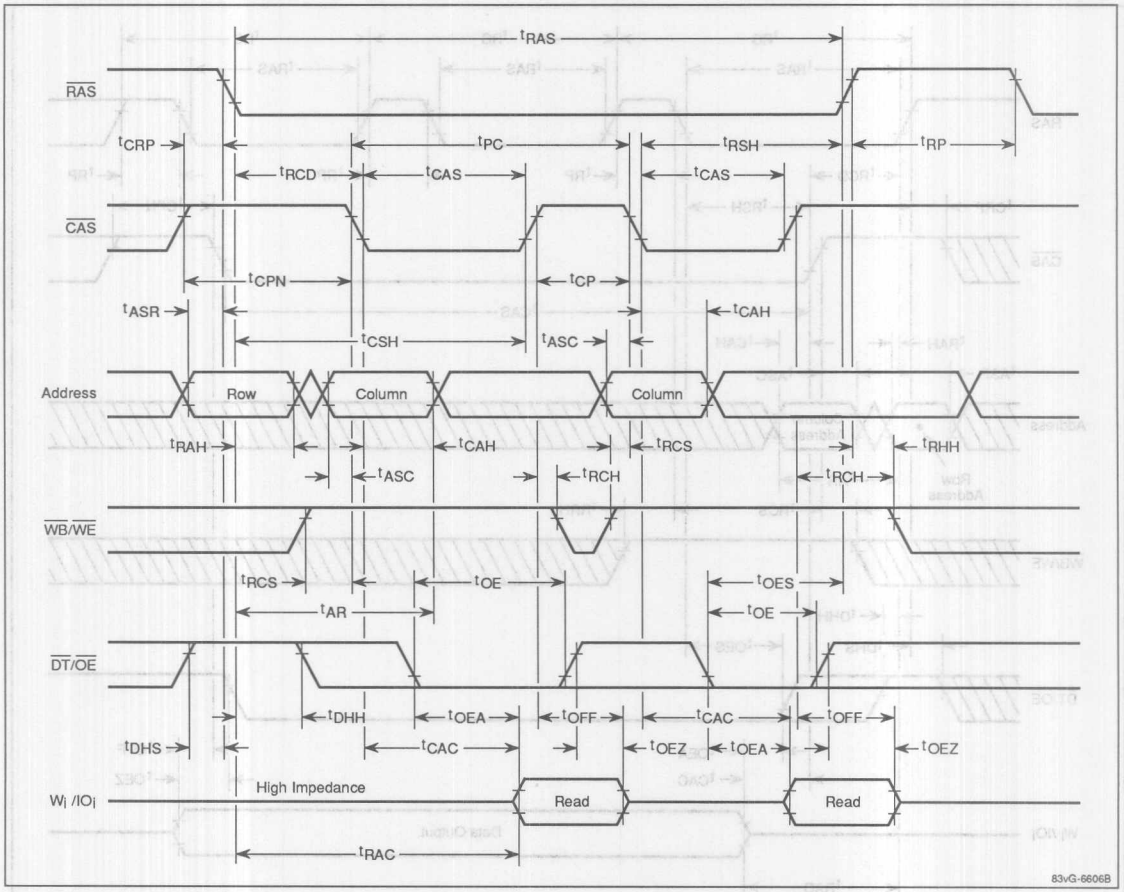
Timing Waveforms (cont)

Hidden Refresh Cycle



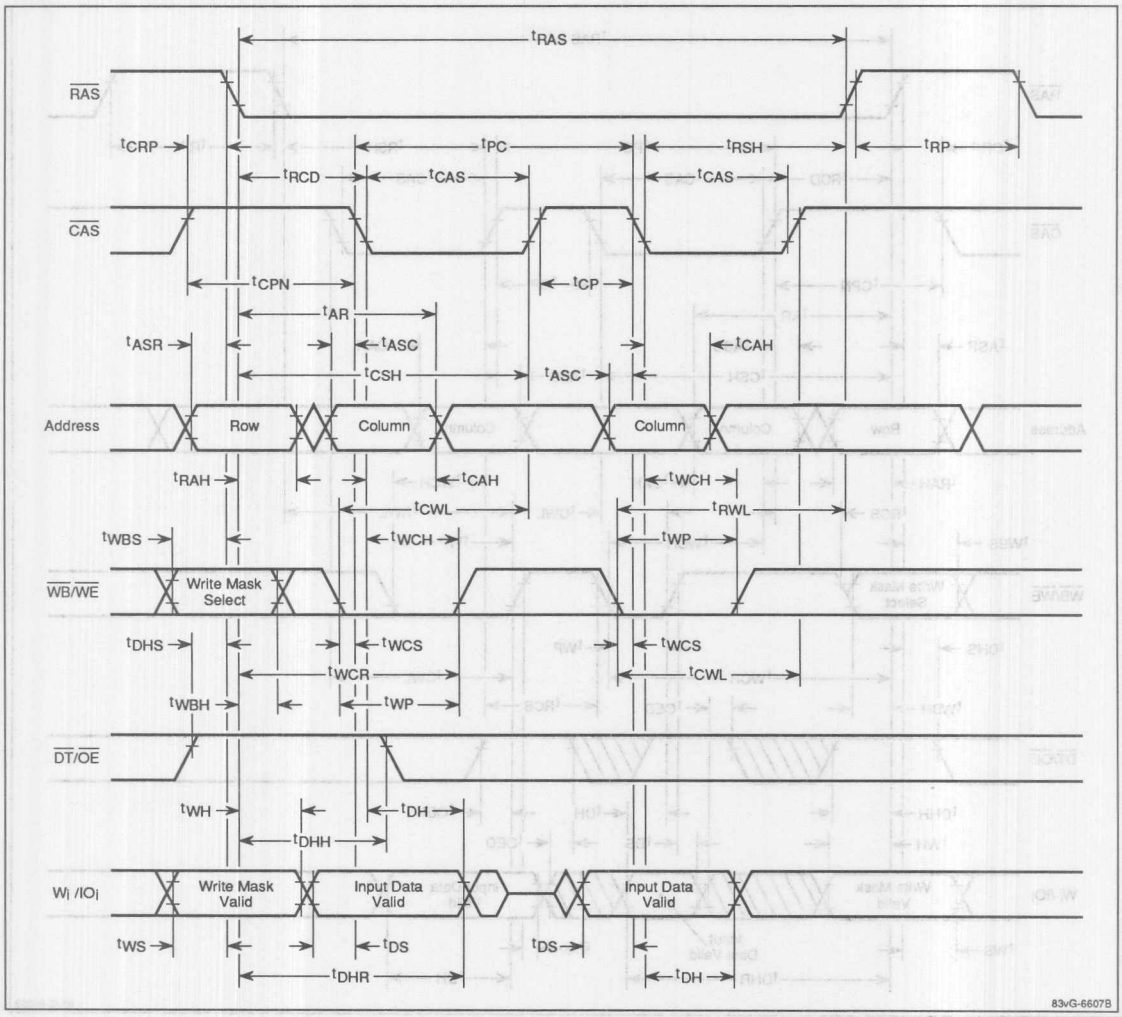
Timing Waveforms (cont)

Page Read Cycle



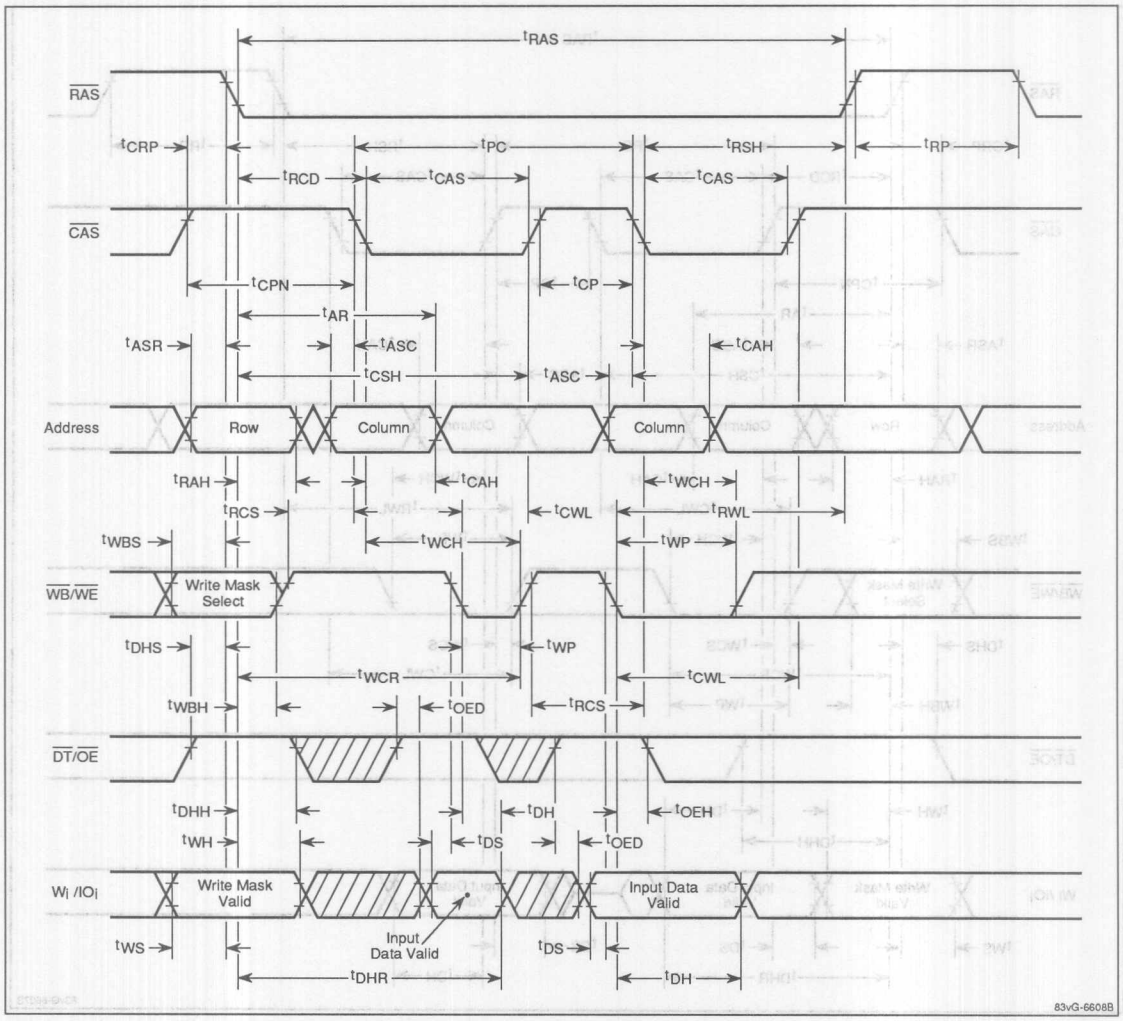
Timing Waveforms (cont)

Page Early Write Cycle



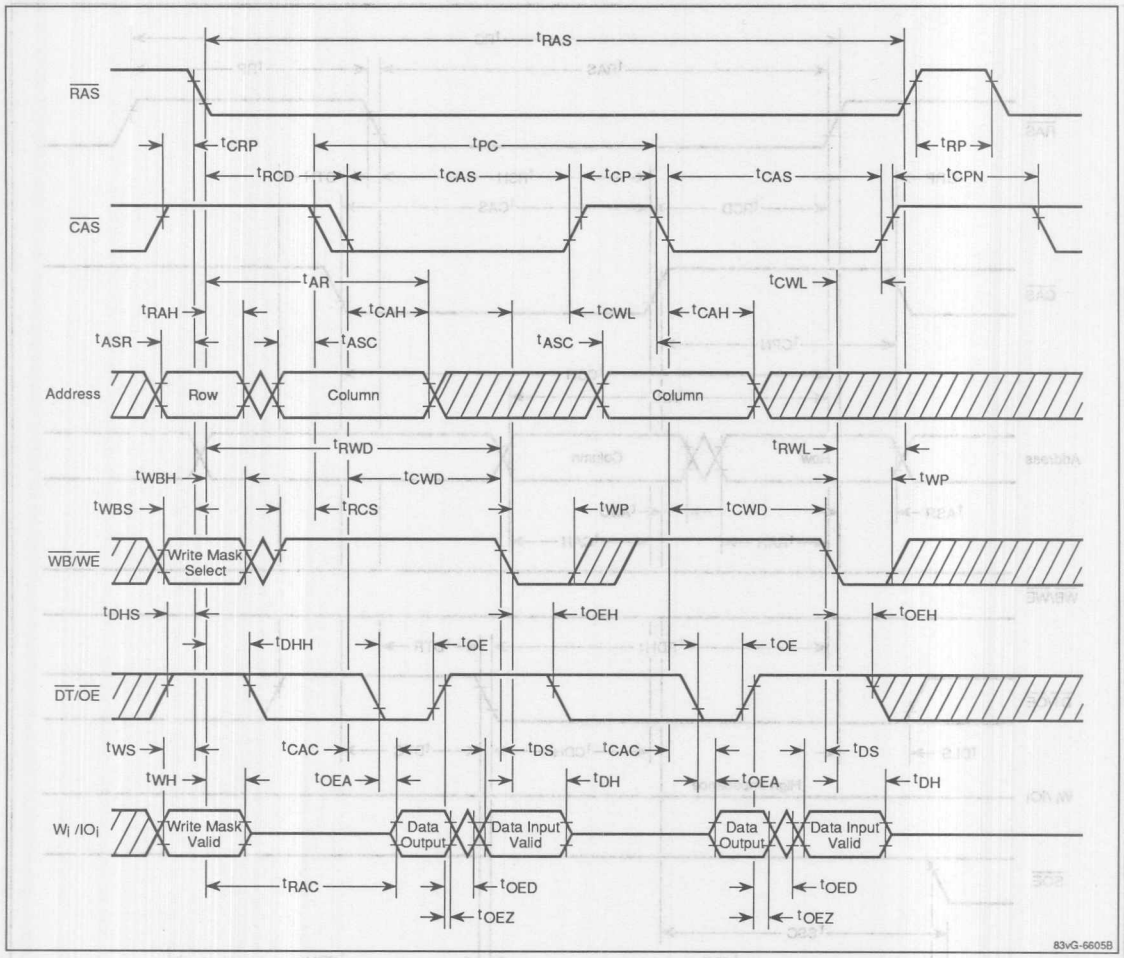
Timing Waveforms (cont)

Page Late Write Cycle



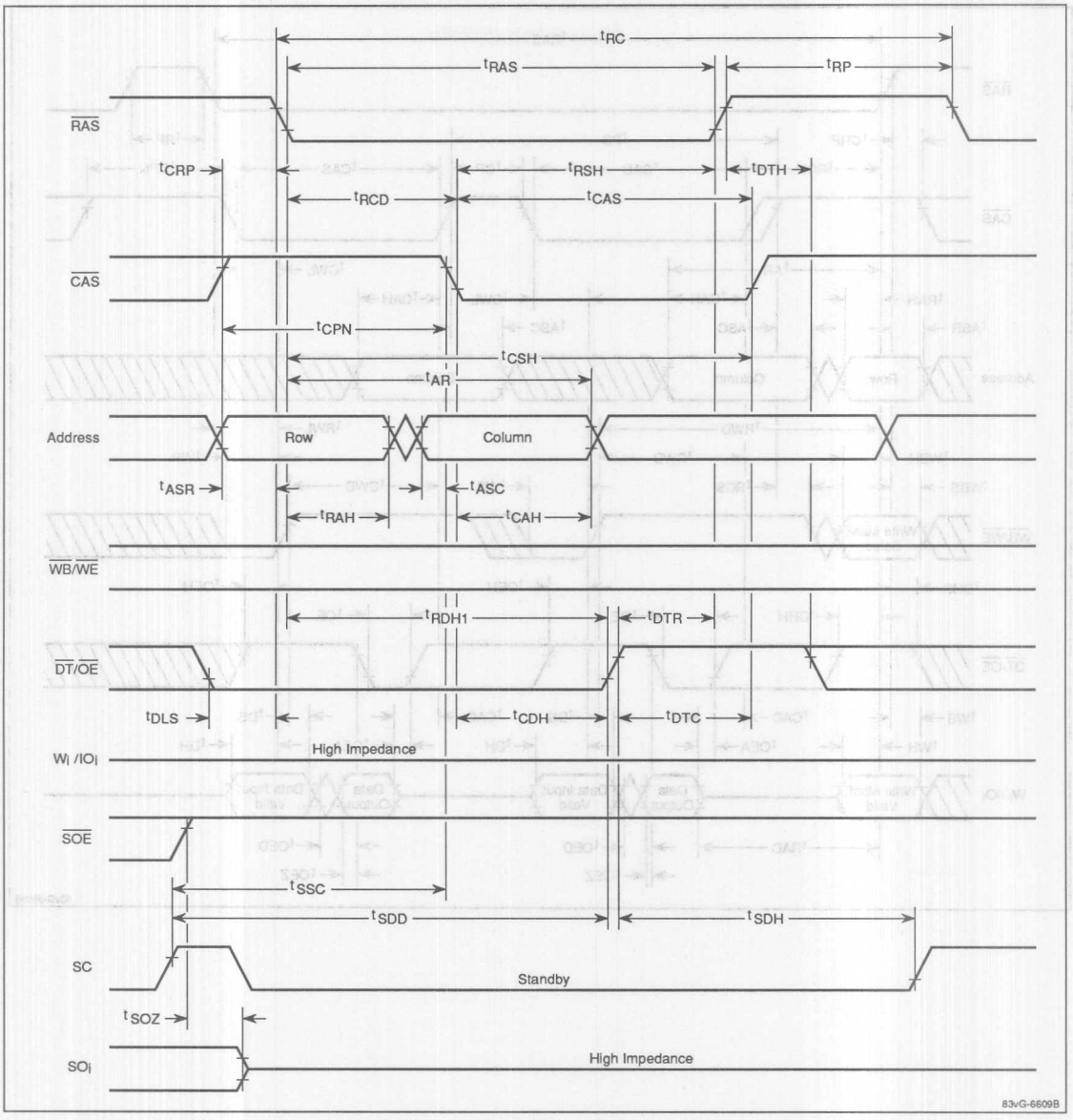
Timing Waveforms (cont)

Page Read-Modify-Write Cycle



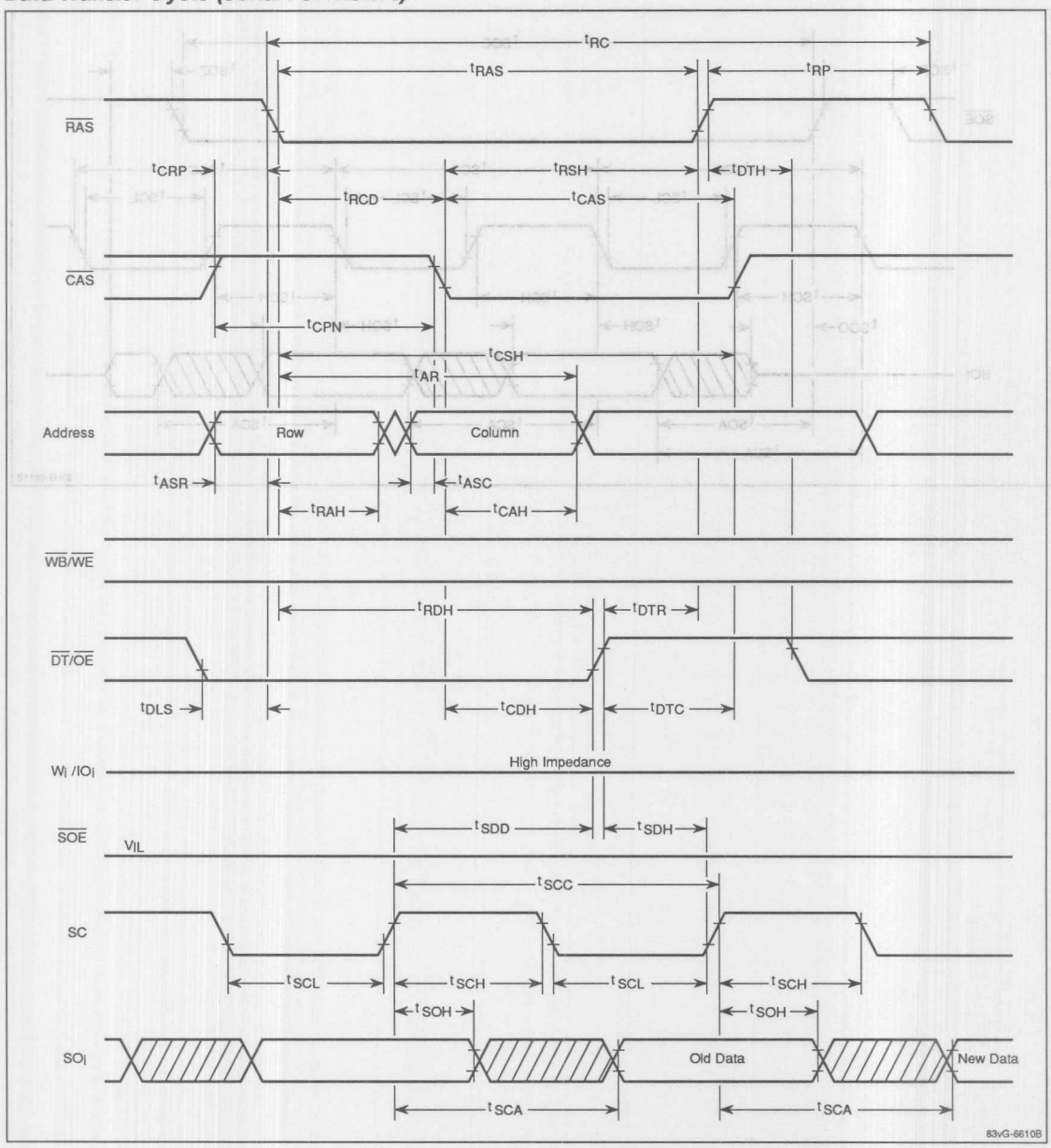
Timing Waveforms (cont)

Data Transfer Cycle (Serial Port in Standby)



Timing Waveforms (cont)

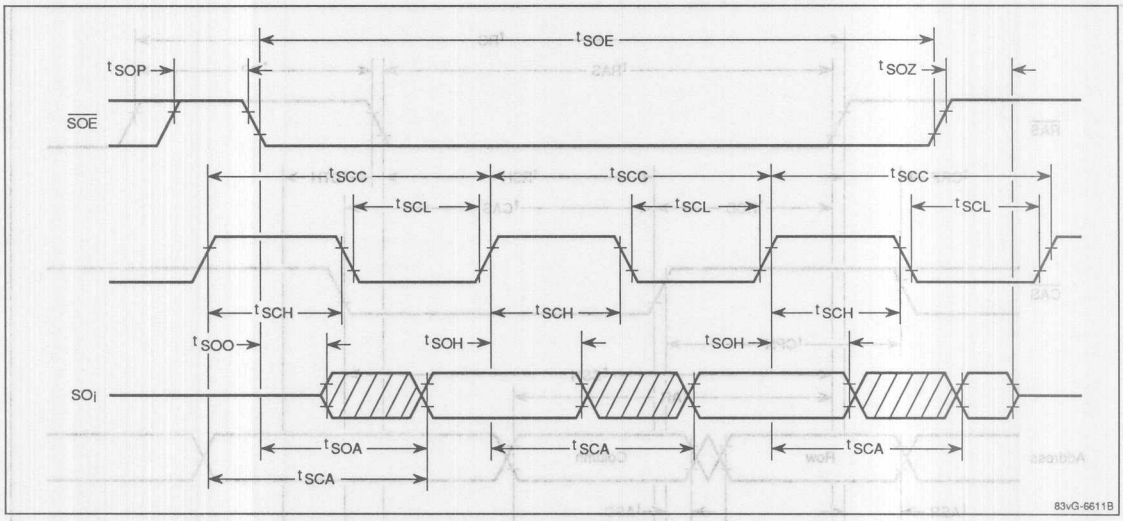
Data Transfer Cycle (Serial Port Active)



3

Timing Waveforms (cont)

Serial Read Cycle



μPD42264
Dual-Port Graphics Buffer

Description

The μPD42264 is a dual-port graphics buffer equipped with a 64K x 4-bit random access port and a 256 x 4-bit serial read port. The serial read port is connected to an internal 1024-bit data register through a 256 x 4-bit serial read output circuit. The random access port is used by the host CPU to read or write data addressed in any desired order and has a write-per-bit option that allows each of the four data bits to be individually selected or masked for a write cycle.

The μPD42264 features fully asynchronous dual access, except when transferring stored graphics data from a selected row of the storage array to the data register. During a data transfer, the random access port requires a special timing cycle using a transfer clock, while the serial read port continues to operate normally. Following the clock transition of a data transfer, serial read output data changes from an old line to a new line and the starting location on the new line is addressable in the data transfer cycle.

The μPD42264 is fabricated with CMOS technology that provides high storage cell density, high performance, and high reliability. Refreshing is accomplished by means of $\overline{RAS}$-only refresh cycles or by normal read or write cycles on the 256 address combinations of A_0 through A_7 during a 4-ms period. Automatic internal refreshing, by means of either hidden refreshing or the $\overline{CAS}$ before $\overline{RAS}$ timing and on-chip internal refresh circuitry, is also available. The transfer of a row of data from the storage array to the data register also refreshes that row automatically.

All inputs and outputs, including clocks, are TTL-compatible. All address and data-in signals are latched on-chip to simplify system design. Data-out is unlatched to allow greater system flexibility. The μPD42264 is available in a 24-pin plastic DIP, 24-pin plastic SOJ, and 24-pin plastic ZIP, and is guaranteed for operation at 0 to +70°C.

Ordering Information

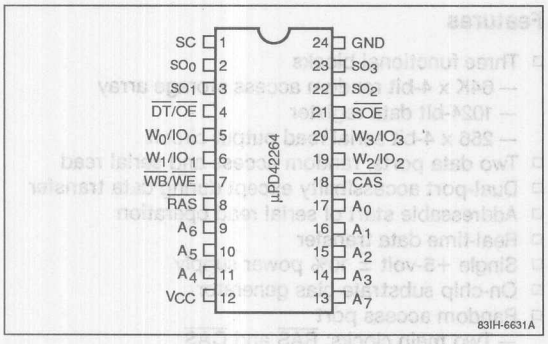
Part Number	Row Access Time (max)	Serial Access Time (max)	Package
μPD42264C-10	100 ns	25 ns	24-pin plastic DIP
μPD42264LA-10	100 ns	25 ns	24-pin plastic SOJ
μPD42264V-10	100 ns	25 ns	24-pin plastic ZIP

Features

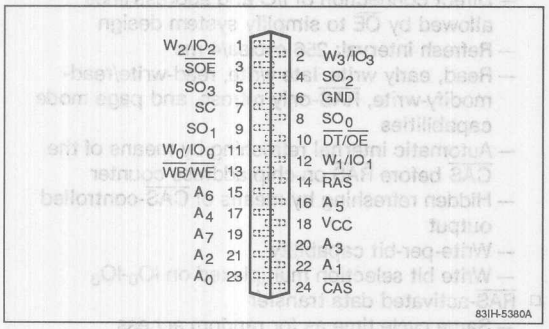
- Three functional blocks
  - 64K x 4-bit random access storage array
  - 1024-bit data register
  - 256 x 4-bit serial read output circuit
- Two data ports: random access and serial read
- Dual-port accessibility except during data transfer
- Addressable start of serial read operation
- Real-time data transfer
- Single +5-volt ± 10% power supply
- On-chip substrate bias generator
- Random access port
  - Two main clocks: $\overline{RAS}$ and $\overline{CAS}$
  - Multiplexed address inputs
  - Direct connection of I/O and address lines allowed by $\overline{OE}$ to simplify system design
  - Refresh interval: 256 cycles/4 ms
  - Read, early write, late write, read-write/read-modify-write, $\overline{RAS}$-only refresh, and page mode capabilities
  - Automatic internal refreshing by means of the $\overline{CAS}$ before $\overline{RAS}$ on-chip address counter
  - Hidden refreshing by means of $\overline{CAS}$-controlled output
  - Write-per-bit capability
  - Write bit selection multiplexed on IO_0-IO_3
- $\overline{RAS}$-activated data transfer
  - Same cycle time as for random access
  - Row data transferred to data register as specified by row address inputs
  - Starting location of following serial read operation specified by column address inputs
  - Transfer of 1024 bits of data on one row to the data register, and the starting location of the serial read circuit, activated by a low-to-high transition of $\overline{DT}$
  - Data transfer during real-time operation or standby of serial port
- Fast serial read operation by means of SC pins
  - Serial data presented on SO_0-SO_3
  - Direct connection of multiple serial outputs for extension of data length
- Fully TTL-compatible inputs, outputs, and clocks
- Three-state outputs for random and serial access
- 24-pin plastic DIP, 24-pin plastic SOJ, and 24-pin plastic ZIP packaging

Pin Configurations

24-Pin Plastic DIP and SOJ



24-Pin Plastic ZIP



Pin Identification

Symbol	Function
A_0 - A_7	Address inputs
$\overline{CAS}$	Column address strobe
$\overline{DT/OE}$	Data transfer/output enable
$\overline{RAS}$	Row address strobe
SC	Serial control
SO_0 - SO_3	Serial read outputs
$\overline{SOE}$	Serial output enable
W_0/IO_0 - W_3/IO_3	Write-per-bit inputs/data inputs and outputs
GND	Ground
$\overline{WB/WE}$	Write-per-bit/write enable
V_{CC}	+5-volt 10% power supply

Absolute Maximum Ratings

Voltage on any pin except V_{CC} relative to GND, V_{R1}	− 1.0 to +7.0 V
Voltage on V_{CC} relative to GND, V_{R2}	− 1.0 V to +7.0 V
Operating temperature, T_{OPR}	0 to +70°C
Storage temperature, T_{STG}	− 55 to +125°C
Short-circuit output current, I_{OS}	50 mA

Exposure to Absolute Maximum Ratings for extended periods may affect device reliability; exceeding the ratings could cause permanent damage. The device should be operated within the limits specified under DC and AC Characteristics.

Capacitance

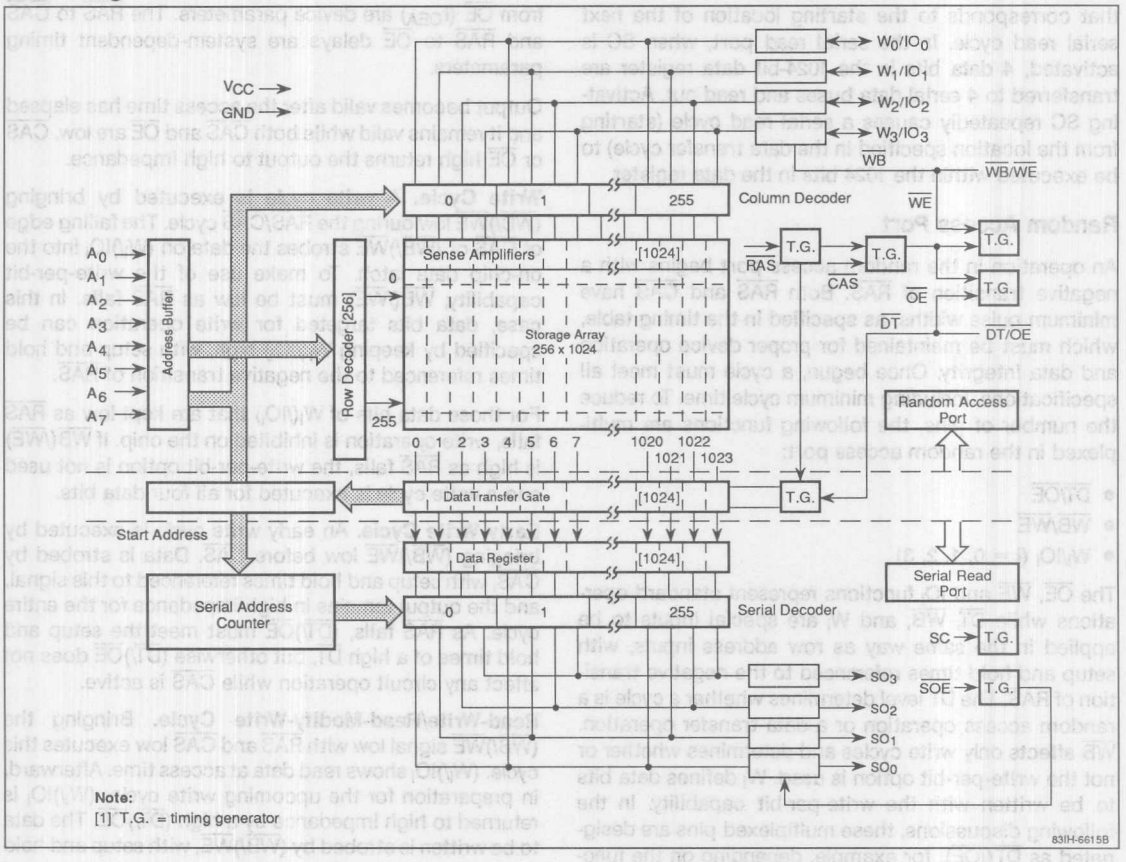
T_A = 0 to +70°C; V_{CC} = +5.0 V ±10%; f = 1 MHz

Parameter	Symbol	Max	Unit	Pins Under Test
Input capacitance	$C_{I(A)}$	5	pF	A_0 - A_7
	$C_{I(\overline{DT/OE})}$	8	pF	$\overline{DT/OE}$
	$C_{I(\overline{WB/WE})}$	8	pF	$\overline{WB/WE}$
	$C_{I(\overline{RAS})}$	8	pF	$\overline{RAS}$
	$C_{I(\overline{CAS})}$	8	pF	$\overline{CAS}$
	$C_{I(\overline{SOE})}$	8	pF	$\overline{SOE}$
	$C_{I(SC)}$	8	pF	SC
Input/output capacitance	$C_{IO(W/IO)}$	7	pF	W_0/IO_0 - W_3/IO_3
Output capacitance	$C_{O(SO)}$	7	pF	SO_0 - SO_3

Recommended Operating Conditions

Parameter	Symbol	Min	Typ	Max	Unit
Supply voltage	V_{CC}	4.5	5.0	5.5	V
Input voltage, high	V_{IH}	2.4		5.5	V
Input voltage, low	V_{IL}	− 1.0		0.8	V
Operating temperature	T_A	0		70	°C

Block Diagram



DEVICE OPERATION

The μPD42264 consists of a random access port and a serial read port. The random access port executes standard read and write cycles as well as data transfer cycles, all of which are based on conventional $\overline{RAS}$/$\overline{CAS}$ timing. In a data transfer, data in each storage cell on the selected row is transferred simultaneously through a transfer gate to the corresponding register location. The serial read port shows the contents of the data register in serial order. The random access port and the serial read port can operate asynchronously, except when the transfer gate is turned on during the data transfer period.

Addressing

The storage array is arranged in a 256-row by 1024-column matrix. Each of 4 data bits in the random access port corresponds to 65,536 storage cells. Therefore, 16 address bits are required to decode one cell location. Eight row address bits are set up on pins A_0 through A_7 and latched onto the chip by $\overline{RAS}$. Eight column address bits then are set up on pins A_0 through A_7 and latched onto the chip by $\overline{CAS}$. All addresses must be stable, on or before the falling edges of $\overline{RAS}$ and $\overline{CAS}$.

$\overline{RAS}$ is similar to a chip enable signal; whenever it is activated, 1024 cells on the selected row are sensed simultaneously and the sense amplifiers automatically restore the data. $\overline{CAS}$ serves as a chip selection signal to activate the column decoder and the input and output buffers.

Through 1 of 256 column decoders, 4 storage cells on the row are connected to 4 data buses, respectively. In the data transfer cycle, 8 row address bits are used to select 1 of the 256 possible rows involved in the transfer of data to the data register. Eight column address bits are

then used to select the 1 of 256 possible serial decoders that corresponds to the starting location of the next serial read cycle. In the serial read port, when SC is activated, 4 data bits in the 1024-bit data register are transferred to 4 serial data buses and read out. Activating SC repeatedly causes a serial read cycle (starting from the location specified in the data transfer cycle) to be executed within the 1024 bits in the data register.

Random Access Port

An operation in the random access port begins with a negative transition of $\overline{RAS}$. Both $\overline{RAS}$ and $\overline{CAS}$ have minimum pulse widths, as specified in the timing table, which must be maintained for proper device operation and data integrity. Once begun, a cycle must meet all specifications, including minimum cycle time. To reduce the number of pins, the following functions are multiplexed in the random access port:

- $\overline{DT}/\overline{OE}$
- $\overline{WB}/\overline{WE}$
- W_i/IO_i (i = 0, 1, 2, 3)

The $\overline{OE}$, $\overline{WE}$ and IO_i functions represent standard operations while $\overline{DT}$, $\overline{WB}$, and W_i are special inputs to be applied in the same way as row address inputs, with setup and hold times referenced to the negative transition of $\overline{RAS}$. The $\overline{DT}$ level determines whether a cycle is a random access operation or a data transfer operation. $\overline{WB}$ affects only write cycles and determines whether or not the write-per-bit option is used. W_i defines data bits to be written with the write-per-bit capability. In the following discussions, these multiplexed pins are designated as $\overline{DT}(/\overline{OE})$, for example, depending on the function being described.

To use the μPD42264 for random access, $\overline{DT}(/\overline{OE})$ must be high as $\overline{RAS}$ falls. Holding $\overline{DT}(/\overline{OE})$ high disconnects the 1024-bit data register from the corresponding 1024-digit lines of the storage array. Conversely, to execute a data transfer, $\overline{DT}(/\overline{OE})$ must be low as $\overline{RAS}$ falls to open the 1024 data transfer gates and transfer data from one of the rows to the data register.

Read Cycle. A read cycle is executed by activating $\overline{RAS}$, $\overline{CAS}$, and $\overline{OE}$ and maintaining $(\overline{WB}/)\overline{WE}$ high while $\overline{CAS}$ is active. The $(W_i/)IO_i$ data pin (i = 0, 1, 2, 3) remains in high impedance until valid data appears at the output at access time. Device access time, t_{ACC}, will be the longest of the following three calculated intervals:

- t_{RAC}
- $\overline{RAS}$ to $\overline{CAS}$ delay (t_{RCD}) + t_{CAC}
- $\overline{RAS}$ to $\overline{OE}$ delay + t_{OEA}

Access times from $\overline{RAS}$ (t_{RAC}), from $\overline{CAS}$ (t_{CAC}), and from $\overline{OE}$ (t_{OEA}) are device parameters. The $\overline{RAS}$ to $\overline{CAS}$ and $\overline{RAS}$ to $\overline{OE}$ delays are system-dependent timing parameters.

Output becomes valid after the access time has elapsed and it remains valid while both $\overline{CAS}$ and $\overline{OE}$ are low. $\overline{CAS}$ or $\overline{OE}$ high returns the output to high impedance.

Write Cycle. A write cycle is executed by bringing $(\overline{WB}/)\overline{WE}$ low during the $\overline{RAS}/\overline{CAS}$ cycle. The falling edge of $\overline{CAS}$ or $(\overline{WB}/)\overline{WE}$ strobes the data on $(W_i/)IO_i$ into the on-chip data latch. To make use of the write-per-bit capability, $\overline{WB}(/\overline{WE})$ must be low as $\overline{RAS}$ falls. In this case, data bits targeted for write operation can be specified by keeping $W_i(/IO_i)$ high, with setup and hold times referenced to the negative transition of $\overline{RAS}$.

For those data bits of $W_i(/IO_i)$ that are kept low as $\overline{RAS}$ falls, write operation is inhibited on the chip. If $\overline{WB}(/\overline{WE})$ is high as $\overline{RAS}$ falls, the write-per-bit option is not used and a write cycle is executed for all four data bits.

Early Write Cycle. An early write cycle is executed by bringing $(\overline{WB}/)\overline{WE}$ low before $\overline{CAS}$. Data is strobed by $\overline{CAS}$, with setup and hold times referenced to this signal, and the output remains in high impedance for the entire cycle. As $\overline{RAS}$ falls, $(\overline{DT}/)\overline{OE}$ must meet the setup and hold times of a high $\overline{DT}$, but otherwise $(\overline{DT}/)\overline{OE}$ does not affect any circuit operation while $\overline{CAS}$ is active.

Read-Write/Read-Modify-Write Cycle. Bringing the $(\overline{WB}/)\overline{WE}$ signal low with $\overline{RAS}$ and $\overline{CAS}$ low executes this cycle. $(W_i/)IO_i$ shows read data at access time. Afterward, in preparation for the upcoming write cycle, $(W_i/)IO_i$ is returned to high impedance by a high $(\overline{DT}/)\overline{OE}$. The data to be written is strobed by $(\overline{WB}/)\overline{WE}$, with setup and hold times referenced to this signal.

Late Write Cycle. This cycle shows the timing flexibility of $(\overline{DT}/)\overline{OE}$, which can be activated just after $(\overline{WB}/)\overline{WE}$ falls, even when $(\overline{WB}/)\overline{WE}$ is brought low after $\overline{CAS}$.

Refresh Cycle. A cycle at each of the 256 row addresses (A_0 through A_7) will refresh all storage cells. Any cycle in the random access port (i.e., read, write, refresh, or data transfer) refreshes the 1024 bits selected by the $\overline{RAS}$ addresses or by the on-chip refresh address counter.

$\overline{RAS}$-only Refresh Cycle. A cycle having only $\overline{RAS}$ active refreshes one row of the storage array. A high $\overline{CAS}$ is maintained while $\overline{RAS}$ is active to keep $(W_i/)IO_i$ in a state of high impedance. This cycle is preferred for refreshing, especially when the host system consists of multiple rows of random access devices. The data outputs may be OR-tied with no bus contention when $\overline{RAS}$-only refresh cycles are executed.

$\overline{CAS}$ Before $\overline{RAS}$ Refresh Cycle. This cycle executes internal refreshing using the on-chip control circuitry. Whenever $\overline{CAS}$ is low as $\overline{RAS}$ falls, this circuitry automatically refreshes the row addresses specified by the internal address counter. In this cycle, the circuit operation based on $\overline{CAS}$ is maintained in a reset state. When internal refreshing is complete, the address counter automatically increments in preparation for the next $\overline{CAS}$ before $\overline{RAS}$ cycle.

Hidden Refresh Cycle. This function performs hidden refreshing after a read cycle, without disturbing the read data output. Once valid, the data output is controlled by $\overline{CAS}$ and $\overline{OE}$. After the read cycle, $\overline{CAS}$ is held low while $\overline{RAS}$ goes high for precharging. A $\overline{RAS}$-only cycle is then executed (except that $\overline{CAS}$ is held low instead of high) and the data output remains valid. Since hidden refreshing is the same as $\overline{CAS}$ before $\overline{RAS}$ refreshing, the data output remains valid during either operation.

Fast-Page Cycle. This feature allows faster data access by keeping the same row address while successive column addresses are strobed onto the chip. By maintaining $\overline{RAS}$ low while successive $\overline{CAS}$ cycles are executed, data is transferred at a faster rate because $\overline{RAS}$ addresses are maintained internally and do not have to be reapplied. During this operation, it is also possible to execute read, write and read-write/read-modify-write cycles. Additionally, the write-per-bit control specified in the entry write cycle is maintained through the following fast-page write cycle.

Data Transfer Cycle. A data transfer cycle is executed by bringing $\overline{DT}(/\overline{OE})$ low as $\overline{RAS}$ falls. The specified 1 of the possible 256 rows involved in the data transfer, as well as the starting location of the following serial read cycle in the serial read port, are defined by address inputs. $\overline{DT}(/\overline{OE})$ must be low for a specified time, measured from $\overline{RAS}$ and $\overline{CAS}$, so that the data transfer condition may be satisfied. The low-to-high transition of $\overline{DT}$ causes two transfer operations through the data transfer gates: column address buffer outputs are transferred to the serial address counters, and storage cell data amplified on digit lines is transferred to the data register. At least one SC cycle is required to hold the data in the register. Otherwise, the beginning of the next transfer cycle destroys the newly transferred data. $\overline{RAS}$ and $\overline{CAS}$ must be low during these operations to keep the transferred data in the random access port.

Serial Read Port

The serial read port is used only to read serially the contents of the data register starting from a specified location. The entire operation, therefore, follows a data transfer cycle. Data stored in the serial register remains valid for a minimum of 4 ms after the transfer cycle. The only condition under which the serial read port must synchronize with the random access port is when the positive transition of $\overline{DT}(/\overline{OE})$ must occur within a specified period in an SC cycle. Except for this SC cycle, the serial read port can operate asynchronously with the random access port. The output data appears at SO_i after an access time of t_{SCA}, measured from SC high, only when $\overline{SOE}$ is maintained low. The SC cycle that includes the positive transition of $\overline{DT}(/\overline{OE})$ shows old data in the data register; subsequent SC cycles show new data transferred to the data register serially and in a looped manner. The serial output is maintained until the next SC signal is activated. $\overline{SOE}$ controls the impedance of the serial output to allow multiplexing of more than one bank of μPD42264 graphics buffers into the same external circuitry. When $\overline{SOE}$ is low, SO_i is enabled and the proper data is read. When $\overline{SOE}$ is at a high logic level, SO_i is disabled and in a state of high impedance.

3

DC Characteristics

T_A = 0 to +70°C; V_{CC} = 5.0 V ±10%

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions
Input leakage current	I_{IL}	−10		10	μA	V_{IN} = 0 to 5.5 V; all other pins not under test = 0 V
Output leakage current	I_{OL}	−10		10	μA	D_{OUT} (IO_i, SO_i) disabled; V_{OUT} = 0 to 5.5 V
Random access port output voltage, high	$V_{OH(R)}$	2.4			V	$I_{OH(R)}$ = −2 mA
Random access port output voltage, low	$V_{OL(R)}$			0.4	V	$I_{OL(R)}$ = 4.2 mA
Serial read port output voltage, high	$V_{OH(S)}$	2.4			V	$I_{OH(S)}$ = −2 mA
Serial read port output voltage, low	$V_{OL(S)}$			0.4	V	$I_{OL(S)}$ = 4.2 mA

Power Supply Current

T_A = 0 to +70°C; V_{CC} = +5.0 V ±10%

Random Access Port	Serial Read Port	Symbol	Max	Unit	Test Conditions
Read/write cycle	Standby	I_{CC1}	70	mA	$\overline{RAS}$ and $\overline{CAS}$ cycling; t_{RC} = t_{RC} min; IO = 0 mA; SC = $\overline{SOE}$ = V_{IH} (Note 1)
Standby	Standby	I_{CC2}	5	mA	$\overline{RAS}$ = V_{IH}; D_{OUT} = high impedance; SC = $\overline{SOE}$ = V_{IH}
$\overline{RAS}$-only refresh cycle	Standby	I_{CC3}	60	mA	$\overline{RAS}$ cycling; $\overline{CAS}$ = V_{IH}; t_{RC} = t_{RC} min; SC = $\overline{SOE}$ = V_{IH}
Page cycle	Standby	I_{CC4}	50	mA	$\overline{RAS}$ = V_{IL}; $\overline{CAS}$ cycling; t_{PC} = t_{PC} min; SC = $\overline{SOE}$ = V_{IH} (Note 1)
$\overline{CAS}$ before $\overline{RAS}$ refresh cycle	Standby	I_{CC5}	60	mA	$\overline{CAS}$ low as $\overline{RAS}$ falls; t_{RC} = t_{RC} min; SC = $\overline{SOE}$ = V_{IH} (Note 1)
Data transfer	Standby	I_{CC6}	75	mA	$\overline{DT}$ low as $\overline{RAS}$ falls; t_{RC} = t_{RC} min; SC = $\overline{SOE}$ = V_{IH}
Read/write cycle	Active	I_{CC7}	120	mA	$\overline{RAS}$ and $\overline{CAS}$ cycling; t_{RC} = t_{RC} min; IO = 0 mA; $\overline{SOE}$ = V_{IL}; SC cycling; t_{SCC} = t_{SCC} min (Note 1)
Standby	Active	I_{CC8}	50	mA	$\overline{RAS}$ = V_{IH}; D_{OUT} = high impedance; $\overline{SOE}$ = V_{IL}; SC cycling; t_{SCC} = t_{SCC} min (Note 1)
$\overline{RAS}$-only refresh cycle	Active	I_{CC9}	110	mA	$\overline{RAS}$ cycling; $\overline{CAS}$ = V_{IH}; t_{RC} = t_{RC} min; $\overline{SOE}$ = V_{IL}; SC cycling; t_{SCC} = t_{SCC} min (Note 1)
Page cycle	Active	I_{CC10}	100	mA	$\overline{RAS}$ = V_{IL}; $\overline{CAS}$ cycling; t_{PC} = t_{PC} min; $\overline{SOE}$ = V_{IL}; SC cycling; t_{SCC} = t_{SCC} min (Note 1)
$\overline{CAS}$ before $\overline{RAS}$ refresh cycle	Active	I_{CC11}	110	mA	$\overline{CAS}$ low as $\overline{RAS}$ falls; t_{RC} = t_{RC} min; $\overline{SOE}$ = V_{IL}; SC cycling; t_{SCC} = t_{SCC} min (Note 1)
Data transfer	Active	I_{CC12}	125	mA	$\overline{DT}$ low as $\overline{RAS}$ falls; t_{RC} = t_{RC} min; $\overline{SOE}$ = V_{IL}; SC cycling; t_{SCC} = t_{SCC} min (Note 1)

Notes:

(1) No load on IO_i or SO_i. Except for I_{CC2}, I_{CC3}, and I_{CC6}, real values depend on output loading and cycle rates.

AC Characteristics

T_A = 0 to +70°C; V_{CC} = +5.0 V±10%

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions
Column address hold time after $\overline{RAS}$ low	t_{AR}	70			ns	
Column address setup time	t_{ASC}	0			ns	
Row address setup time	t_{ASR}	0			ns	
Access time from $\overline{CAS}$	t_{CAC}			50	ns	(Notes 2, 5)
Column address hold time	t_{CAH}	20			ns	
$\overline{CAS}$ pulse width	t_{CAS}	50		10,000	ns	
$\overline{DT}$ low hold time after $\overline{RAS}$ low	t_{CDH}	30			ns	(Note 12)
$\overline{CAS}$ before $\overline{RAS}$ refresh hold time	t_{CHR}	20			ns	
$\overline{CAS}$ precharge time (page cycle only)	t_{CP}	40			ns	
$\overline{CAS}$ precharge time (nonpage cycle)	t_{CPN}	20			ns	
$\overline{CAS}$ high to $\overline{RAS}$ low precharge time	t_{CRP}	10			ns	
SC delay time from $\overline{CAS}$	t_{CSD}	45			ns	(Note 12)
$\overline{CAS}$ hold time	t_{CSH}	100			ns	
$\overline{CAS}$ before $\overline{RAS}$ refresh setup time	t_{CSR}	10			ns	

AC Characteristics (cont)

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions
$\overline{CAS}$ to $\overline{WE}$ delay	t_{CWD}	85			ns	(Note 10)
Write command to $\overline{CAS}$ lead time	t_{CWL}	35			ns	
Data-in hold time	t_{DH}	30			ns	(Note 11)
$\overline{DT}$ high hold time	t_{DHH}	15			ns	
Data-in hold time after $\overline{RAS}$ low	t_{DHR}	80			ns	
$\overline{DT}$ high setup time	t_{DHS}	0			ns	
$\overline{DT}$ low setup time	t_{DLS}	0			ns	
Data-in setup time	t_{DS}	0			ns	(Note 11)
$\overline{DT}$ high to $\overline{CAS}$ high delay	t_{DTC}	10			ns	
$\overline{DT}$ high hold time after $\overline{RAS}$ high	t_{DTH}	15			ns	
$\overline{DT}$ high to $\overline{RAS}$ high delay	t_{DTR}	10			ns	
$\overline{OE}$ pulse width	t_{OE}	25			ns	
Access time from $\overline{OE}$	t_{OEA}			25	ns	(Note 2)
$\overline{OE}$ to data-in setup delay	t_{OED}	25			ns	
$\overline{OE}$ hold time after $\overline{WE}$ low	t_{OEH}	10			ns	
$\overline{OE}$ to $\overline{RAS}$ inactive setup time	t_{OES}	10			ns	
Output disable time from $\overline{OE}$ high	t_{OEZ}	0		25	ns	(Note 6)
Output disable time from $\overline{CAS}$ high	t_{OFF}	0		25	ns	(Note 6)
Page cycle time	t_{PC}	100			ns	
Access time from $\overline{RAS}$	t_{RAC}			100	nc	(Notes 2, 4)
Row address hold time	t_{RAH}	15			ns	
$\overline{RAS}$ pulse width	t_{RAS}	100		10,000	ns	
Random read or write cycle time	t_{RC}	190			ns	
$\overline{RAS}$ to $\overline{CAS}$ delay time	t_{RCD}	25		50	ns	(Note 4)
Read command hold time after $\overline{CAS}$ high	t_{RCH}	0			ns	(Note 9)
Read command setup time	t_{RCS}	0			ns	
$\overline{DT}$ low hold time after $\overline{RAS}$ low (serial port active)	t_{RDH}	80			ns	(Note 12)
$\overline{DT}$ low hold time after $\overline{RAS}$ low (serial port in standby)	t_{RDH1}	15			ns	(Note 12)
Refresh interval	t_{REF}			4	ms	
$\overline{RAS}$ precharge time	t_{RP}	80			ns	
$\overline{RAS}$ high to $\overline{CAS}$ low precharge time	t_{RPC}	0			ns	
Read command hold after $\overline{RAS}$ high	t_{RRH}	10			ns	(Note 9)
SC delay from $\overline{RAS}$	t_{RSD}	95			ns	(Note 12)
$\overline{RAS}$ hold time	t_{RSH}	50			ns	
Read-write/read-modify-write cycle time	t_{RWC}	260			ns	
$\overline{RAS}$ to $\overline{WE}$ delay	t_{RWD}	135			ns	(Note 10)
Write command to $\overline{RAS}$ lead time	t_{RWL}	35			ns	
SC pulse width	t_{SCH}	10			ns	
Serial output access time from SC	t_{SCA}			30	ns	(Notes 2, 7)
Serial clock cycle time	t_{SCC}	30		50,000	ns	

3

AC Characteristics (cont)

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions
SC precharge time	t_{SCL}	10			ns	
SC high to $\overline{DT}$ high delay	t_{SDD}	10			ns	
SC low hold time after $\overline{DT}$ high	t_{SDH}	10			ns	
Serial output access time from $\overline{SOE}$	t_{SOA}			25	ns	
$\overline{SOE}$ pulse width	t_{SOE}	10			ns	(Note 13)
Serial output hold time after SC high	t_{SOH}	5			ns	
$\overline{SOE}$ low to serial output setup delay	t_{SOO}	5			ns	
$\overline{SOE}$ precharge time	t_{SOP}	10			ns	(Note 13)
Serial output disable time from $\overline{SOE}$ high	t_{SOZ}	0		25	ns	(Note 6)
SC setup time to $\overline{CAS}$	t_{SSC}	10			ns	(Note 12)
Rise and fall transition time	t_T	3		50	ns	
Write-per-bit hold time	t_{WBH}	15			ns	
Write-per-bit setup time	t_{WBS}	0			ns	
Write command hold time	t_{WCH}	25			ns	
Write command hold time after $\overline{RAS}$ low	t_{WCR}	75			ns	
Write command setup time	t_{WCS}	0			ns	(Note 10)
Write bit selection hold time	t_{WH}	15			ns	
Write command pulse width	t_{WP}	15			ns	
Write bit selection setup time	t_{WS}	0			ns	

Notes:

(1) See input/output timing waveforms for timing reference voltages.

(2) See figures 1 and 2 for output loads.

(3) An initial pause of 100 μs is required after power-up, followed by any eight $\overline{RAS}$ cycles (except $\overline{CAS}$-before-$\overline{RAS}$ cycles), before proper device operation is achieved.

(4) Operation within the t_{RCD} (max) limit ensures that t_{RAC} (max) can be met. The t_{RCD} (max) limit is specified as a reference point only. If t_{RCD} is greater than the specified t_{RCD} (max) limit, access time is controlled exclusively by t_{CAC}.

(5) Assumes that $t_{RCD} \geq t_{RCD}$ (max).

(6) An output disable time defines the time at which the output achieves the open-circuit condition and is not referenced to output voltage levels.

(7) Data in the serial output register remains valid for 4 ms (min) after a data transfer cycle.

(8) V_{IH} (min) and V_{IL} (min) are reference levels for measuring the timing of input signals. Additionally, transition times are measured between V_{IH} and V_{IL}.

(9) Either t_{RRH} or t_{RCH} must be satisfied for a read cycle.

(10) t_{WCS}, t_{CWD}, and t_{RWD} are restrictive operating parameters in read-write and read-modify-write cycles only. If $t_{WCS} \geq t_{WCS}$ (min), the cycle is an early write cycle and the data output will remain open-circuit throughout the entire cycle. If $t_{CWD} \geq t_{CWD}$ (min) and $t_{RWD} \geq t_{RWD}$ (min), the cycle is a read-write cycle and the data output will contain data read from the selected cell. If neither of the above conditions is met, the condition of the data output (at access time and until $\overline{CAS}$ returns to V_{IH}) is indeterminate.

(11) These parameters are referenced to the falling edge of $\overline{CAS}$ in early write cycles and to the falling edge of (WB/)$\overline{WE}$ in delayed write or read-modify-write cycles.

(12) Use t_{RDH} and t_{CDH} when the serial port is active and t_{RDH1}, t_{RSD}, t_{CSD} and t_{SSC} if it is in standby.

(13) $\overline{SOE}$ may be tied to GND if the output enable function of the serial port is not needed.

Figure 1. Input Timing

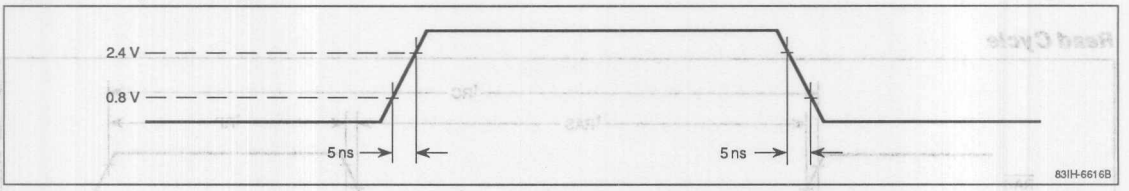


Figure 2. Output Timing

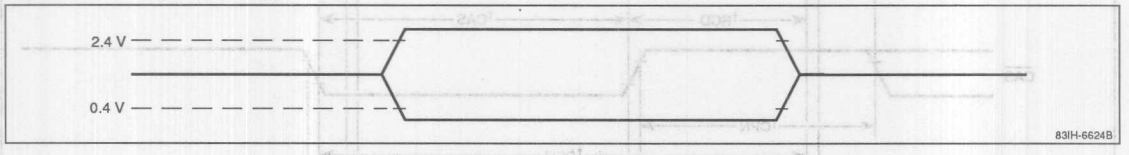


Figure 3. Output Loading in Random Access Port

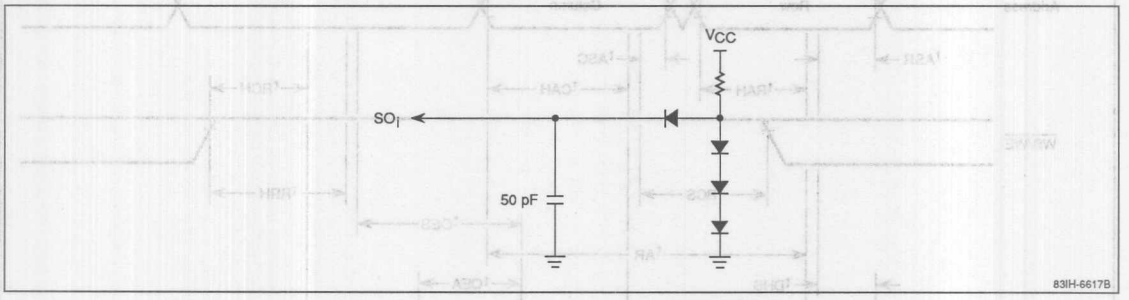
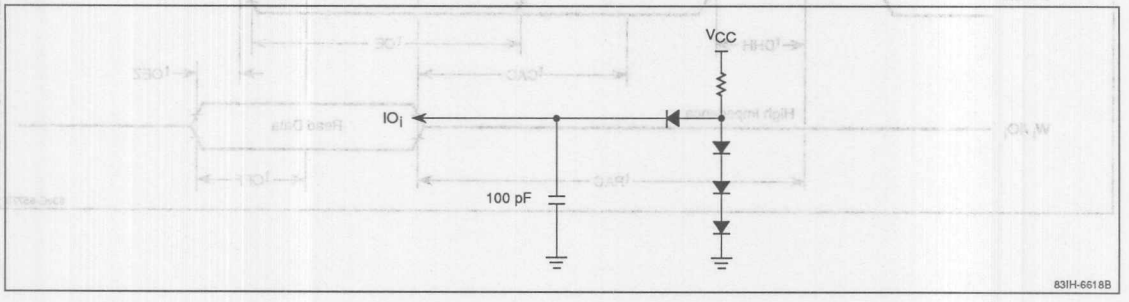
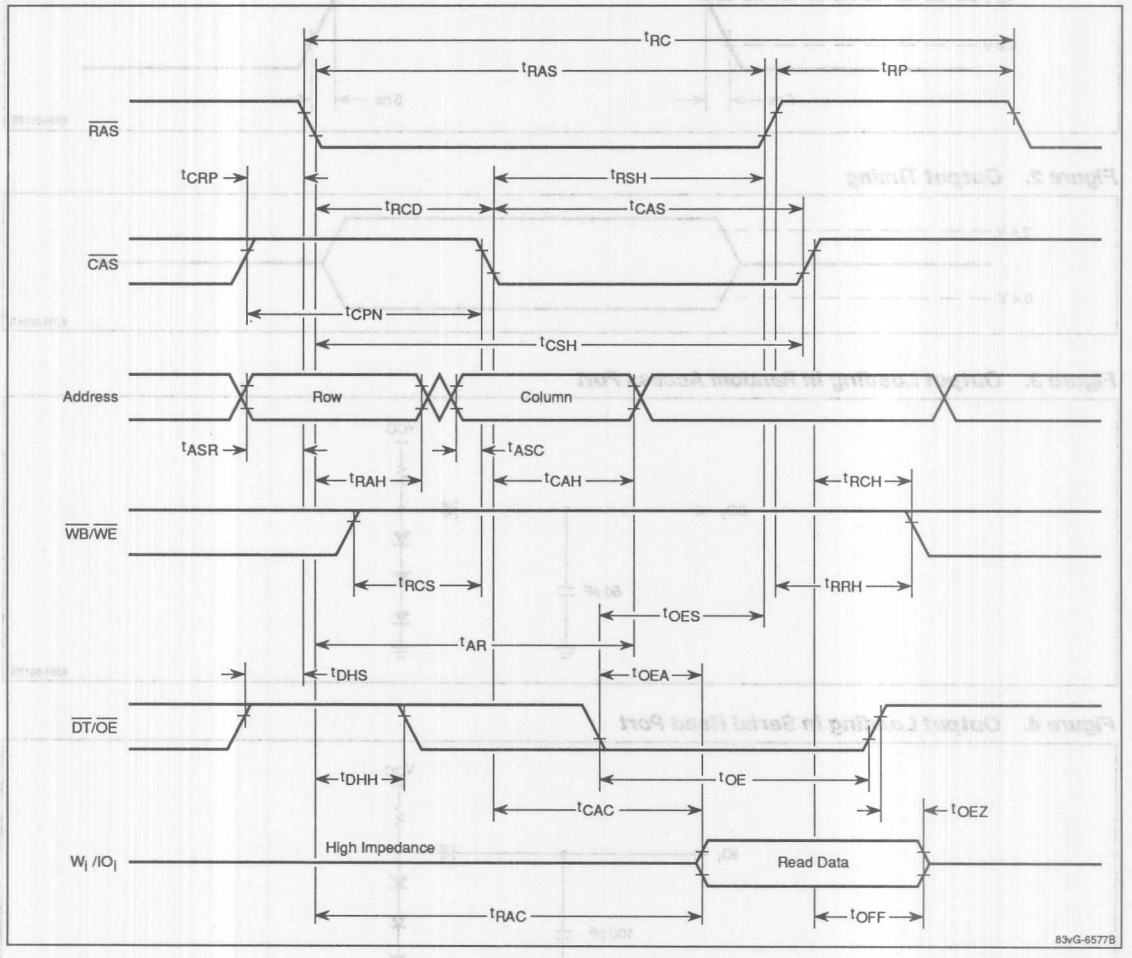


Figure 4. Output Loading in Serial Read Port



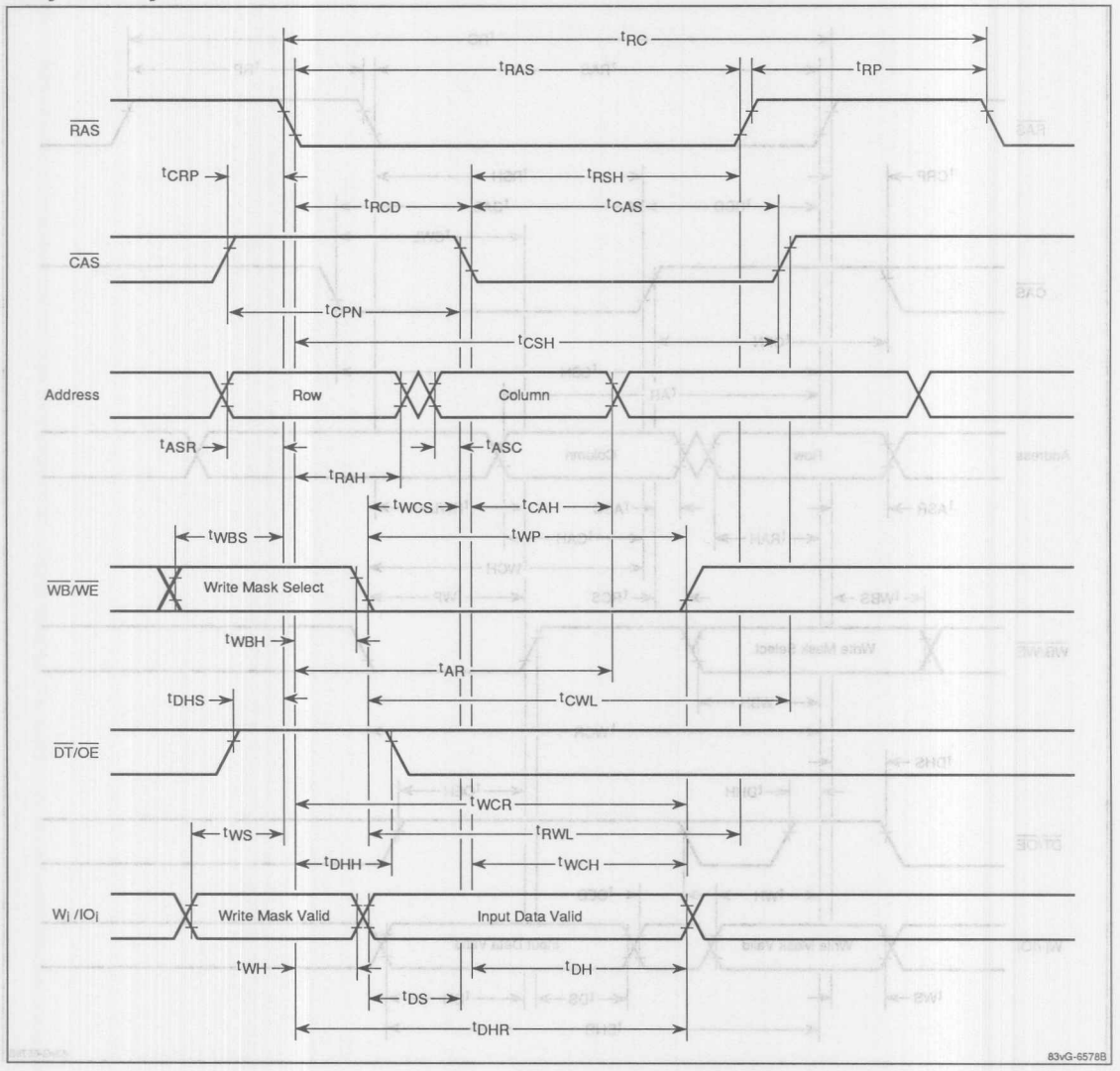
Timing Waveforms

Read Cycle



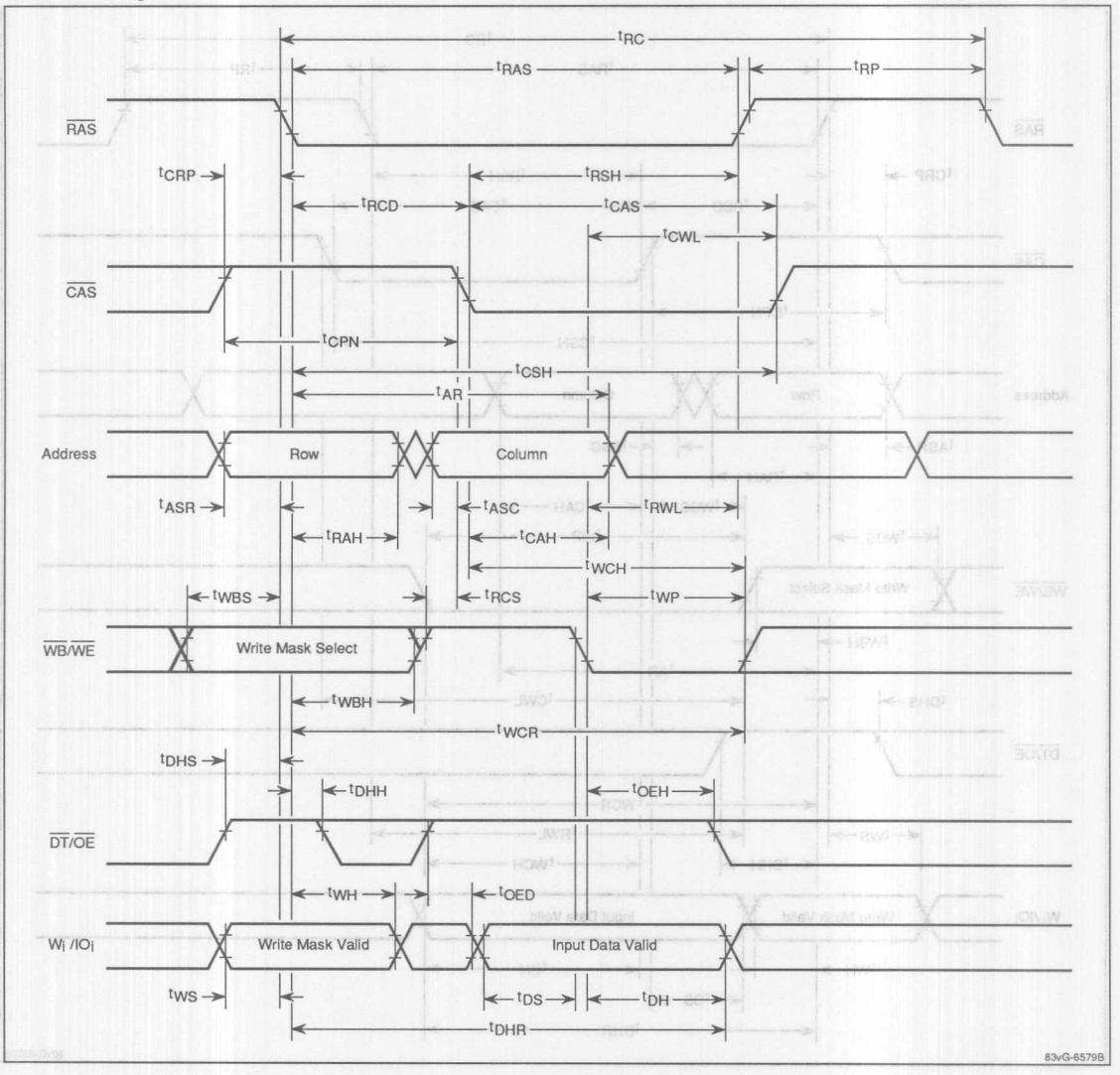
Timing Waveforms (cont)

Early Write Cycle



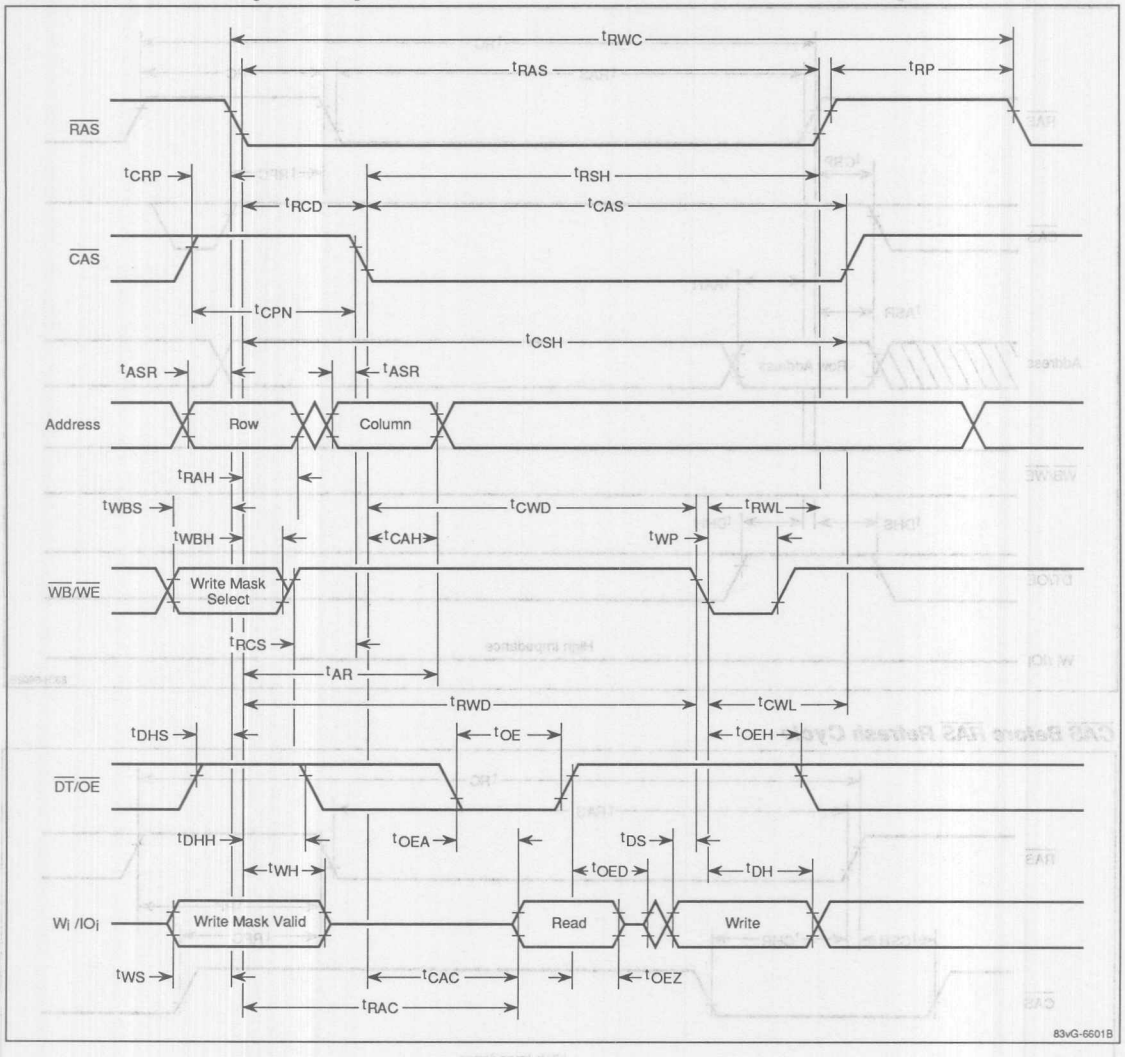
Timing Waveforms (cont)

Late Write Cycle



Timing Waveforms (cont)

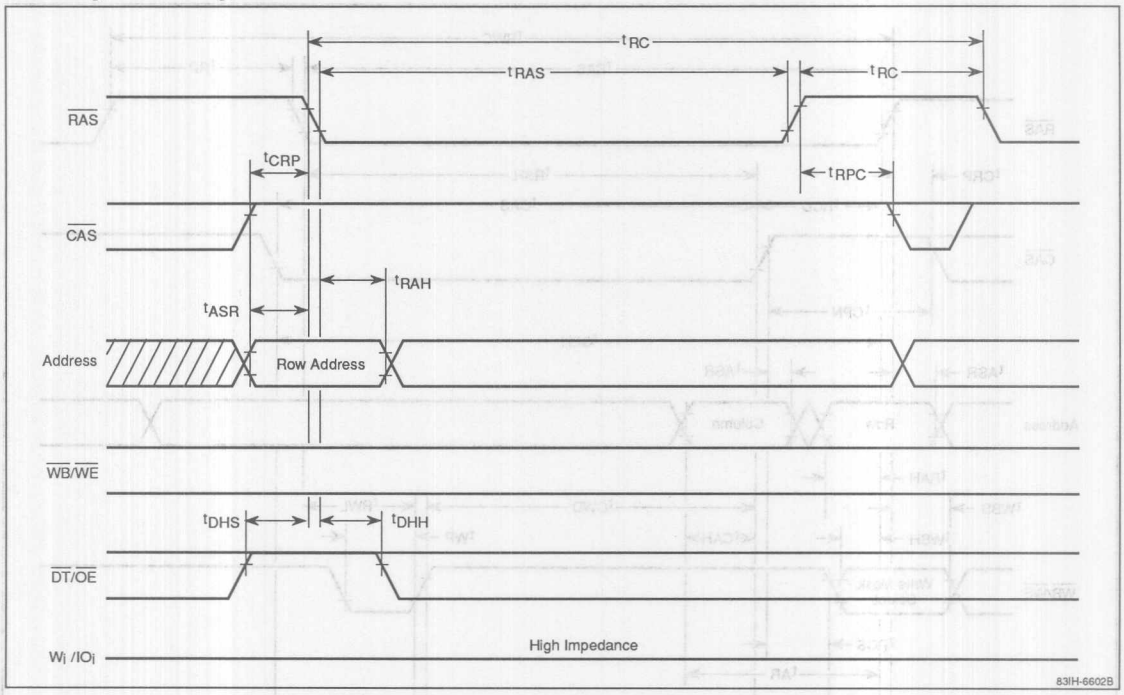
Read-Write/Read-Modify-Write Cycle



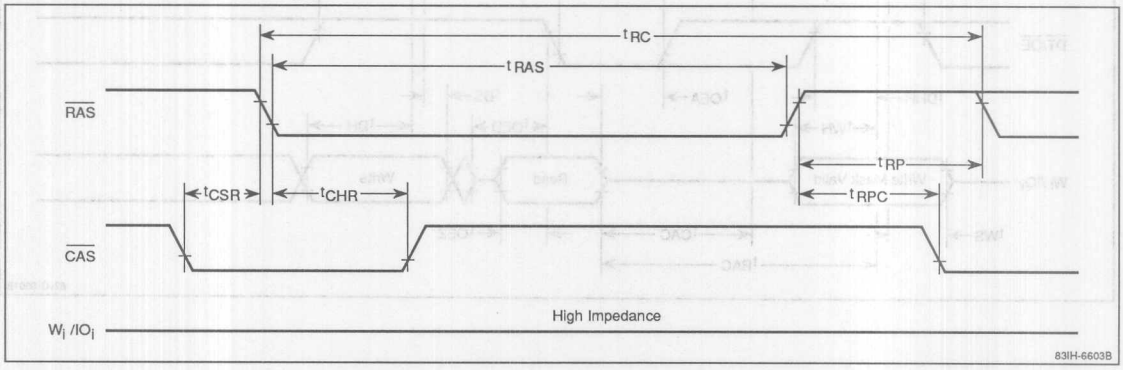
3

Timing Waveforms (cont)

$\overline{RAS}$-Only Refresh Cycle

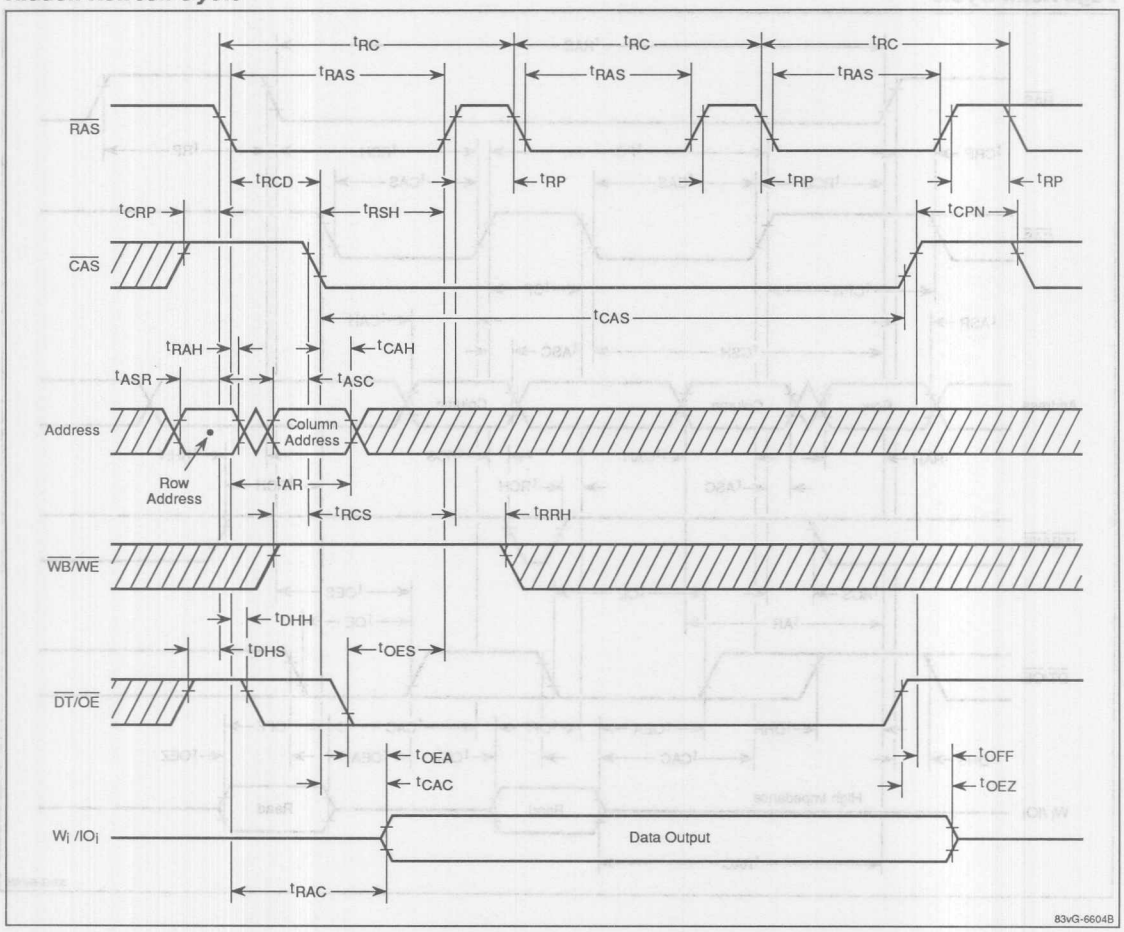


$\overline{CAS}$ Before $\overline{RAS}$ Refresh Cycle



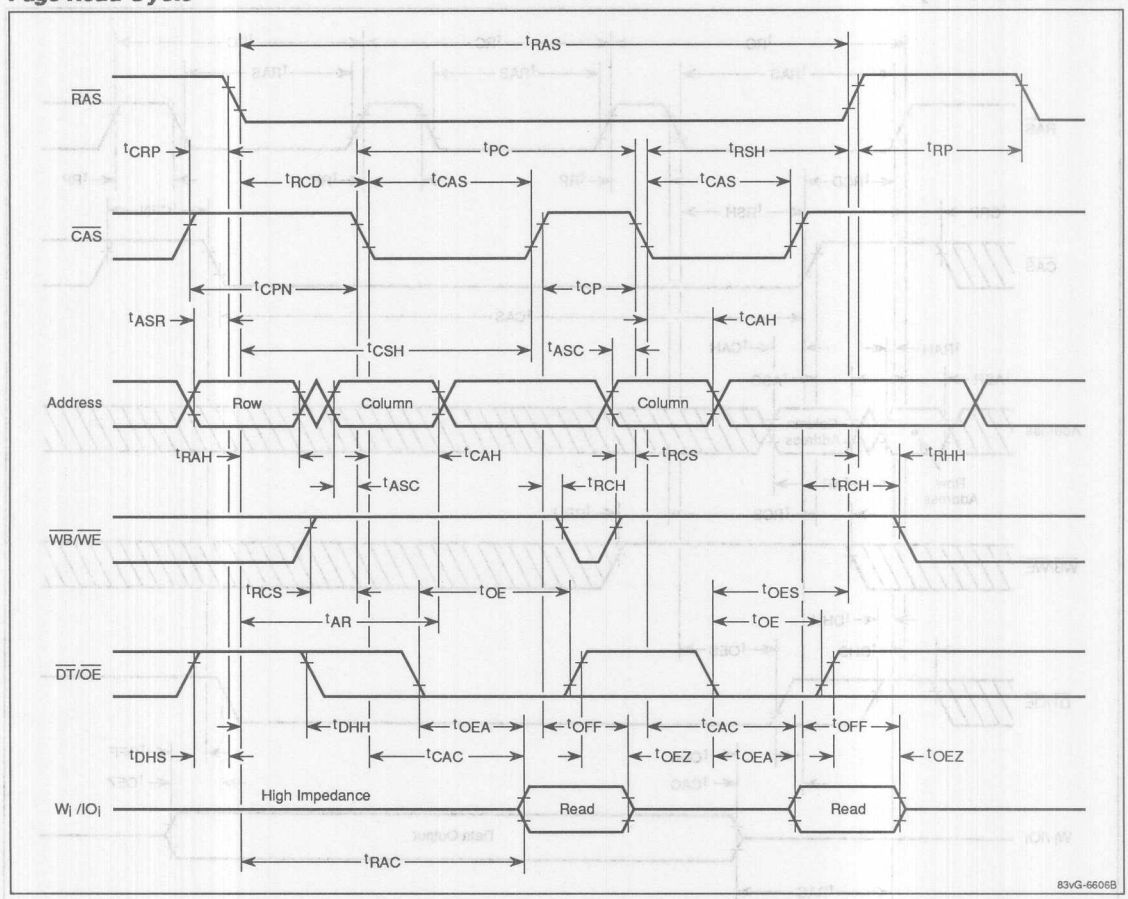
Timing Waveforms (cont)

Hidden Refresh Cycle



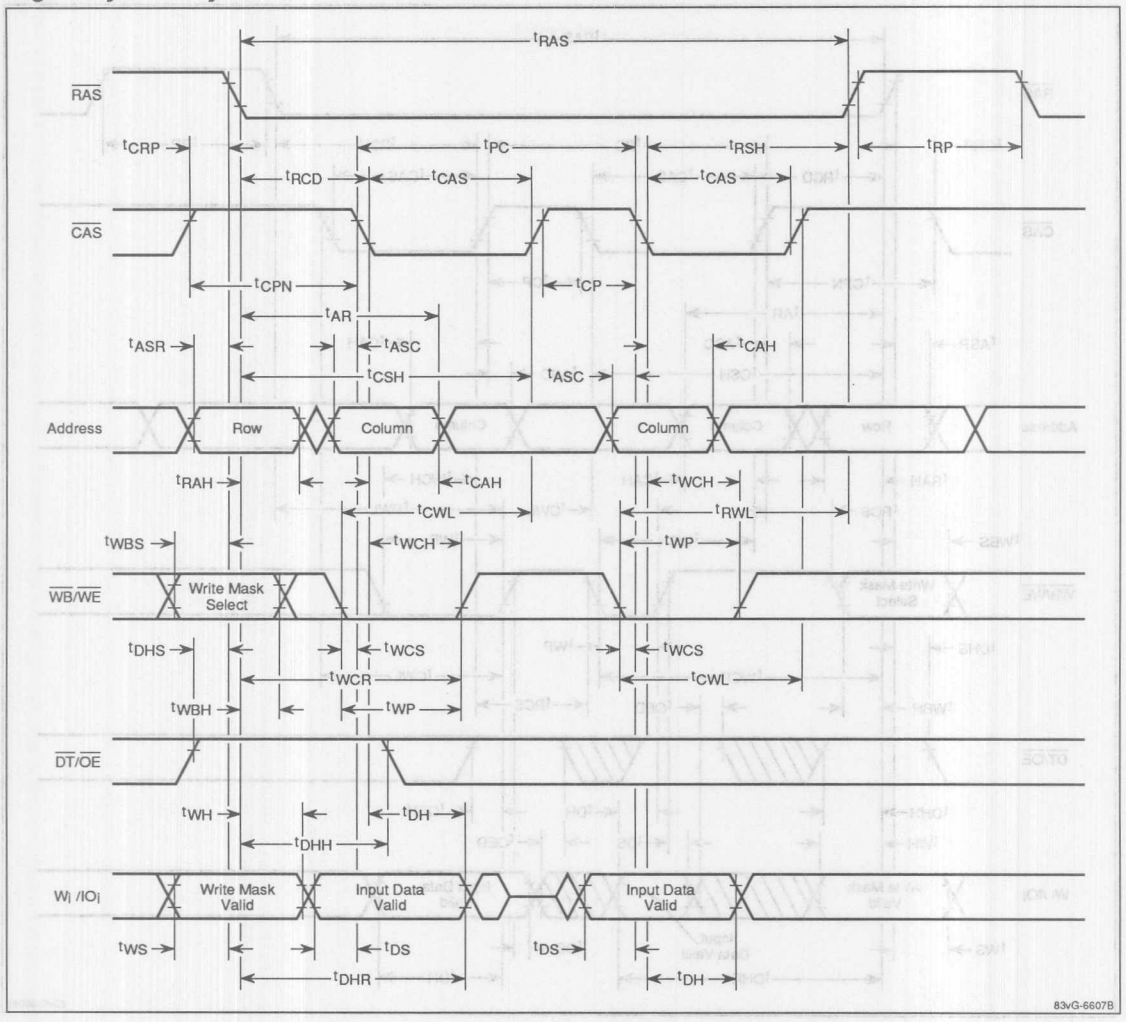
Timing Waveforms (cont)

Page Read Cycle



Timing Waveforms (cont)

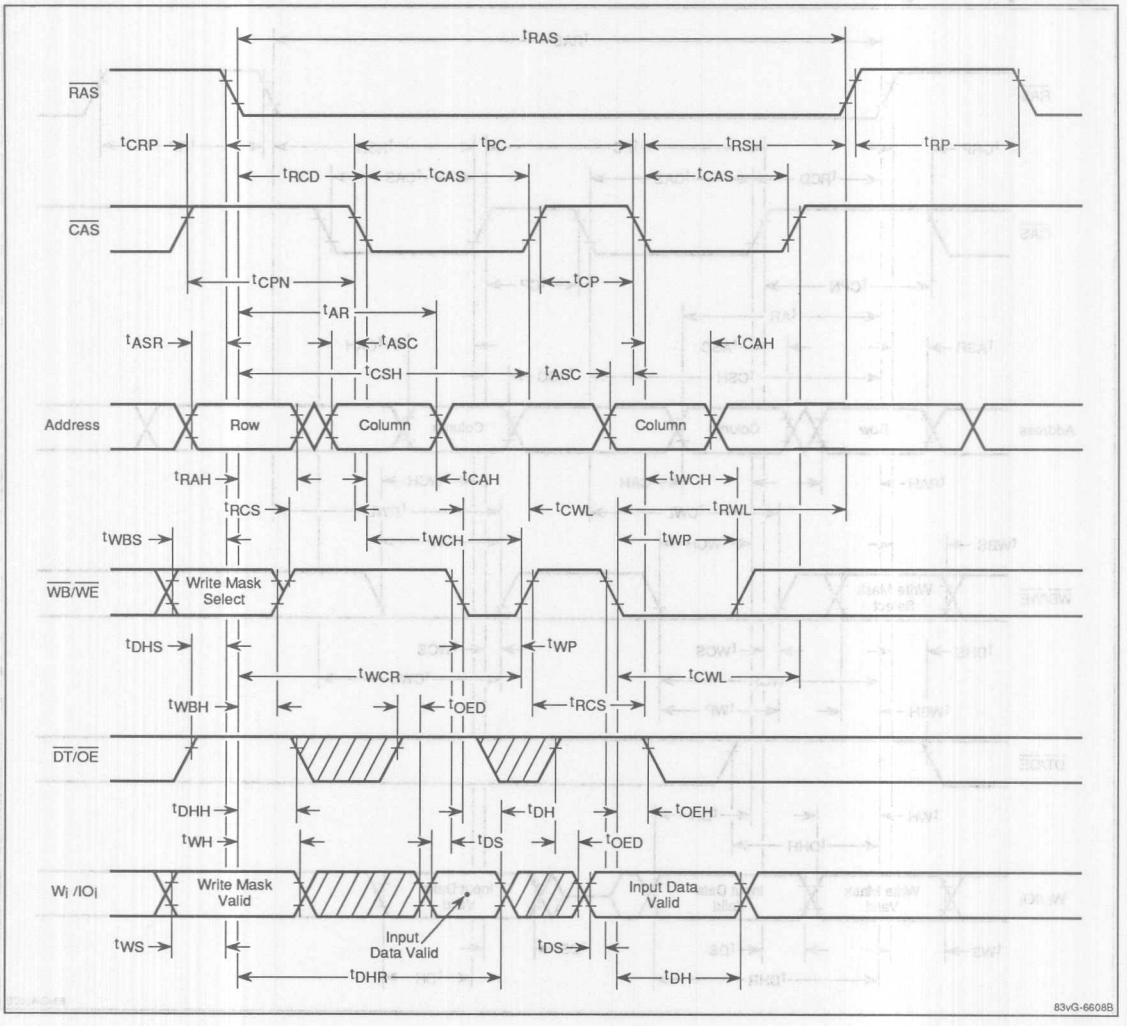
Page Early Write Cycle



3

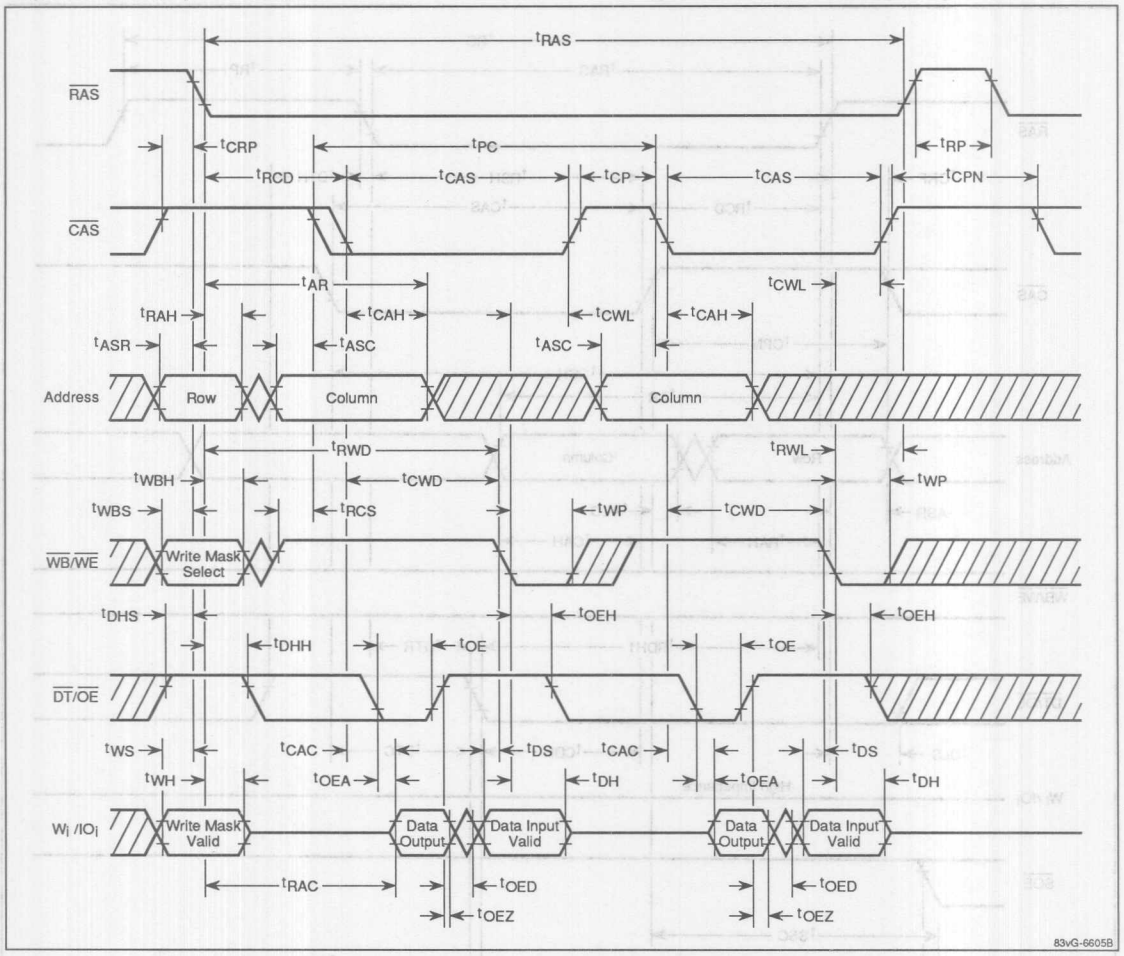
Timing Waveforms (cont)

Page Late Write Cycle



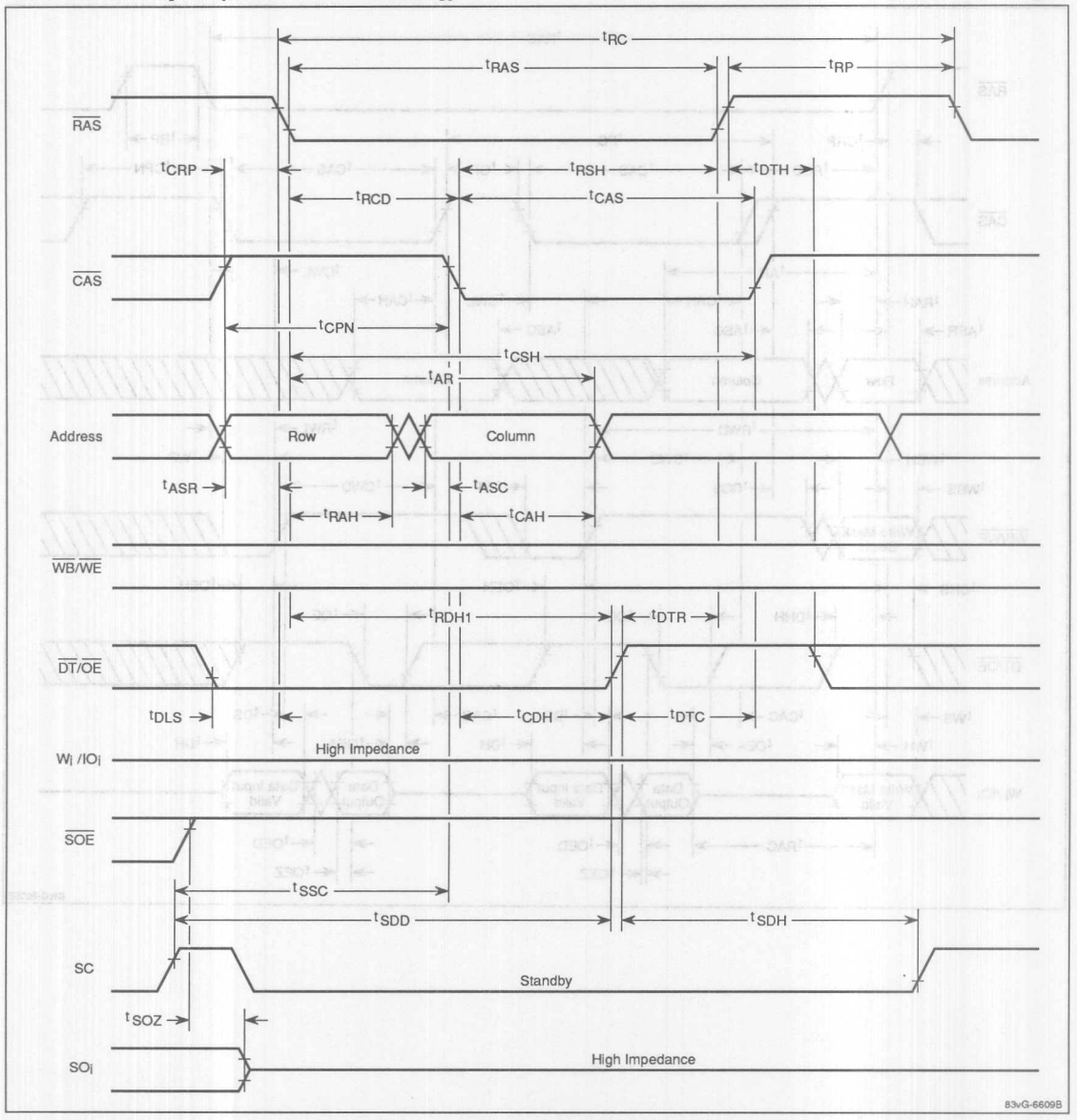
Timing Waveforms (cont)

Page Read-Modify-Write Cycle



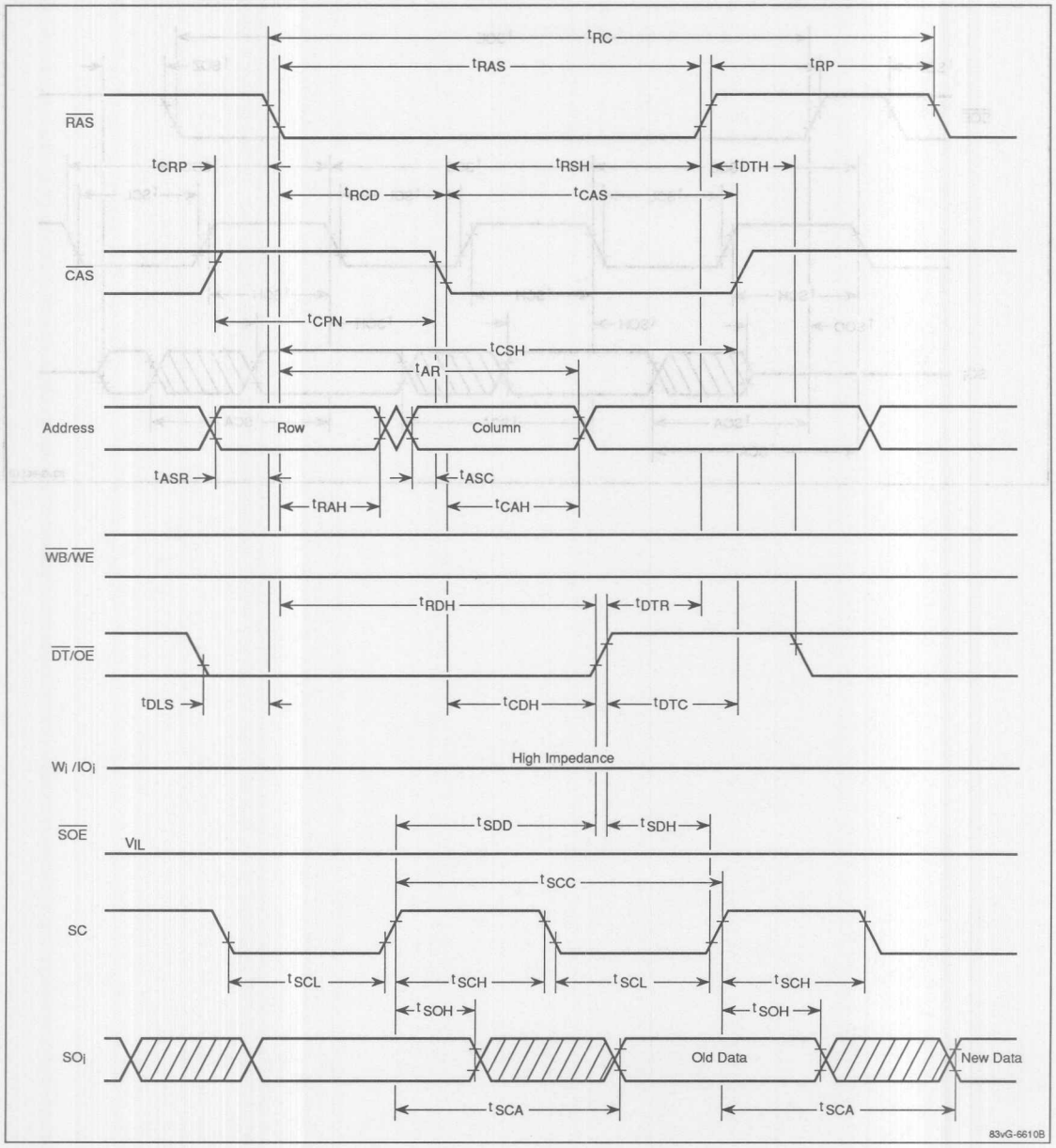
Timing Waveforms (cont)

Data Transfer Cycle (Serial Port in Standby)



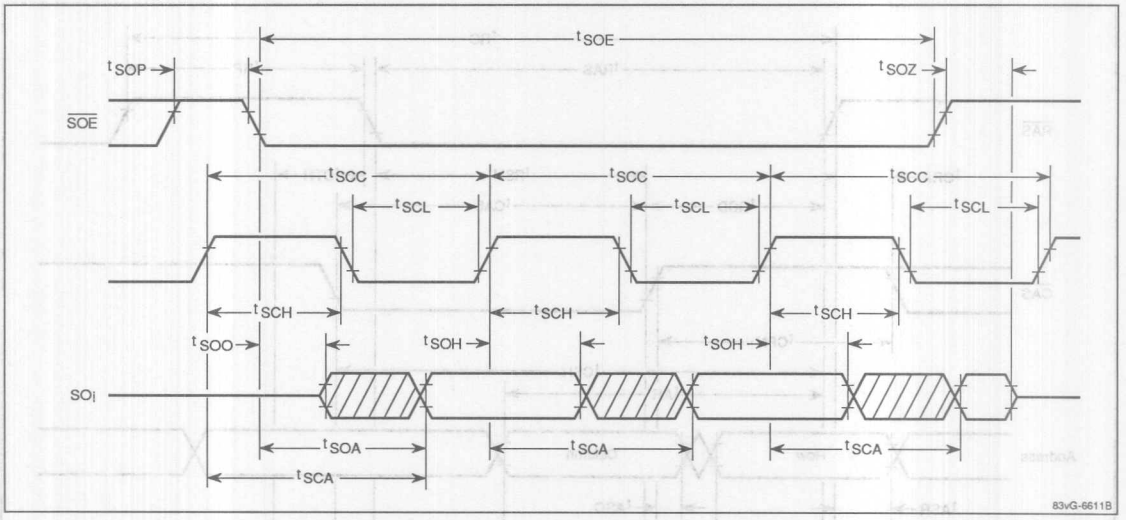
Timing Waveforms (cont)

Data Transfer Cycle (Serial Port Active)



Timing Waveforms (cont)

Serial Read Cycle



μPD42273
Dual-Port Graphics Buffer

Description

The μPD42273 is a dual-port graphics buffer equipped with a 256K x 4-bit random access port and a 512 x 4-bit serial read port. The serial read port is connected to an internal 2048-bit data register through a 512 x 4-bit serial read output circuit. The random access port is used by the host CPU to read or write data addressed in any desired order. A write-per-bit capability allows each of the four data bits to be individually selected or masked for a write cycle.

The μPD42273 features fully asynchronous dual access, except when transferring stored graphics data from a selected row of the storage array to the data register. During a data transfer, the random access port requires a special timing cycle using a transfer clock; the serial read port continues to operate normally. Following the clock transition of a data transfer, serial output data changes from an old line to a new line and the starting location on the new line is addressable in the data transfer cycle.

An advanced CMOS silicon-gate process using polycide technology and trench capacitors provides high storage cell density, high performance, and high reliability.

Refreshing is accomplished by means of $\overline{RAS}$-only refresh cycles or by normal read or write cycles on the 512 address combinations of A_0 through A_8 during an 8-ms period. Automatic internal refreshing, by means of either hidden refreshing or the $\overline{CAS}$ before $\overline{RAS}$ timing and on-chip internal refresh circuitry, is also available. The transfer of a row of data from the storage array to the data register also refreshes that row automatically.

The μPD42273 is an alternative to the μPD42274 for applications that do not require the flash write function.

All inputs and outputs, including clocks, are TTL-compatible. All address and data-in signals are latched on-chip to simplify system design. Data-out is unlatched to allow greater system flexibility.

The μPD42273 is available in a 28-pin plastic ZIP or 28-pin plastic SOJ and is guaranteed for operation at 0 to + 70°C.

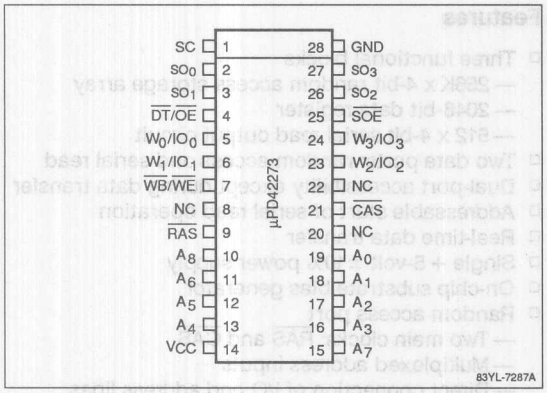
Features

- Three functional blocks
  - — 256K x 4-bit random access storage array
  - — 2048-bit data register
  - — 512 x 4-bit serial read output circuit
- Two data ports: random access and serial read
- Dual-port accessibility except during data transfer
- Addressable start of serial read operation
- Real-time data transfer
- Single + 5-volt ±10% power supply
- On-chip substrate bias generator
- Random access port
  - — Two main clocks: $\overline{RAS}$ and $\overline{CAS}$
  - — Multiplexed address inputs
  - — Direct connection of I/O and address lines allowed by $\overline{OE}$ to simplify system design
  - — 512 refresh cycles every 8 ms
  - — Read, early write, late write, read-write/read-modify-write, $\overline{RAS}$-only refresh, and fast-page cycles
  - — Automatic internal refreshing by means of the $\overline{CAS}$ before $\overline{RAS}$ on-chip address counter
  - — $\overline{CAS}$-controlled hidden refreshing
  - — Write-per-bit option regarding four I/O bits
  - — Write bit selection multiplexed on IO_0-IO_3
- $\overline{RAS}$-activated data transfer
  - — Same cycle time as for random access
  - — Row data transferred to data register as specified by row address inputs
  - — Starting location of following serial read cycle specified by column address inputs
  - — Transfer of 2048 bits of data on one row to the data register, and the starting location of the serial read circuit, activated by a low-to-high transition of $\overline{DT}$
  - — Data transfer during real-time operation or standby of serial port
- Fast serial read operation by means of SC pins
- Serial data output on SO_0-SO_3
- Direct connection of multiple serial outputs for extension of data length
- Fully TTL-compatible inputs, outputs, and clocks
- Three-state outputs for random and serial access
- CMOS silicon-gate process with trench capacitors

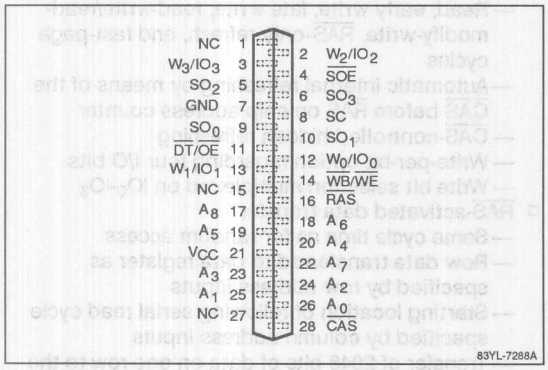
New speed of 80 ns will be available in 1991.

Pin Configurations

28-Pin Plastic SOJ



28-Pin Plastic ZIP



Pin Identification

Symbol	Function
A_0 - A_8	Address inputs
W_0/IO_0 - W_3/IO_3	Write-per-bit selects/data inputs and outputs
$\overline{RAS}$	Row address strobe
$\overline{CAS}$	Column address strobe
$\overline{WB/WE}$	Write-per-bit/write enable
$\overline{DT/OE}$	Data transfer/output enable
SO_0 - SO_3	Serial read outputs
SC	Serial control
$\overline{SOE}$	Serial output enable
GND	Ground
V_{CC}	+5-volt ±10% power supply
NC	No connection

Ordering Information

Part Number	Row Access Time (max)	Serial Access Time (max)	Package
μPD42273LE-10	100 ns	30 ns	28-pin plastic SOJ
LE-12	120 ns	40 ns	
μPD42273V-10	100 ns	30 ns	28-pin plastic ZIP
V-12	120 ns	40 ns	

Absolute Maximum Ratings

Voltage on any pin except V_{CC} relative to GND, V_{R1}	−1.0 to +7.0 V
Voltage on V_{CC} relative to GND, V_{R2}	−1.0 to +7.0 V
Operating temperature, T_{OPR}	0 to +70°C
Storage temperature, T_{STG}	−55 to +125°C
Short-circuit output current, I_{OS}	50 mA
Power dissipation, P_D	1.5 W

Exposure to Absolute Maximum Ratings for extended periods may affect device reliability; exceeding the ratings could cause permanent damage. The device should be operated within the limits specified under DC and AC Characteristics.

Recommended Operating Conditions

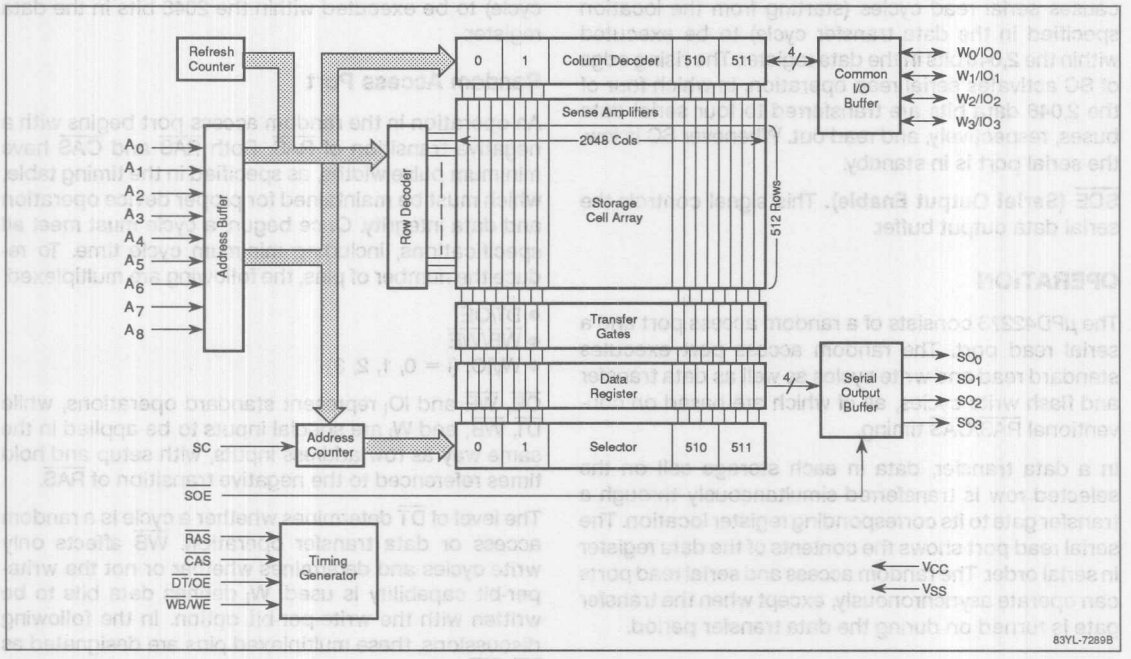
Parameter	Symbol	Min	Typ	Max	Unit
Supply voltage	V_{CC}	4.5	5.0	5.5	V
Input voltage, high	V_{IH}	2.4		5.5	V
Input voltage, low	V_{IL}	−1.0		0.8	V
Ambient temperature	T_A	0		70	°C

Capacitance

T_A = 0 to +70°C; V_{CC} = +5.0 V ±10%; f = 1 MHz; GND = 0 V

Parameter	Symbol	Limit (max)	Unit	Pins Under Test
Input capacitance	$C_{I(A)}$	5	pF	A_0 through A_8
	$C_{I(\overline{DT/OE})}$	8	pF	$\overline{DT/OE}$
	$C_{I(\overline{WB/WE})}$	8	pF	$\overline{WB/WE}$
	$C_{I(\overline{RAS})}$	8	pF	$\overline{RAS}$
	$C_{I(\overline{CAS})}$	8	pF	$\overline{CAS}$
	$C_{I(\overline{SOE})}$	8	pF	$\overline{SOE}$
	$C_{I(SC)}$	8	pF	SC
Input/output capacitance	$C_{IO(W/IO)}$	7	pF	W_0/IO_0 through W_3/IO_3
Output capacitance	$C_{O(SO)}$	7	pF	SO_0 through SO_3

Block Diagram



Pin Functions

A_0-A_8 (Address Inputs). These pins are multiplexed as row and column address inputs. Each of four data bits in the random access port corresponds to 262,144 storage cells, which means that nine row addresses and nine column addresses are required to decode one cell location. Nine row addresses are first used to select one of the 512 possible rows for a read, write, data transfer, or refresh cycle. Nine column addresses are then used to select the one of 512 possible column decoders for a read or write cycle or the one of 512 possible starting locations for the next serial read cycle. (Column addresses are not required in $\overline{RAS}$-only refresh or flash write cycles.)

W_0/IO_0-W_3/IO_3 (Write-Per-Bit Inputs/Common Data Inputs and Outputs). Each of the four data bits can be individually latched by these inputs at the falling edge of $\overline{RAS}$ in a write cycle, and then updated at the next falling edge of $\overline{RAS}$. In a read cycle, these pins serve as outputs for the selected storage cells. In a write cycle, data input on these pins is latched by the falling edge of $\overline{CAS}$ or $\overline{WE}$.

$\overline{RAS}$ (Row Address Strobe). This pin is functionally equivalent to a chip enable signal in that whenever it is activated, the 2,048 storage cells of a selected row are sensed simultaneously and the sense amplifiers restore all data. The nine row address bits are latched by this signal and must be stable on or before its falling edge. $\overline{CAS}$, $\overline{DT/OE}$ and $\overline{WB/WE}$ are simultaneously latched to determine device operation.

$\overline{CAS}$ (Column Address Strobe). This pin serves as a chip selection signal to activate the column decoder and the input/output buffers. The nine column address bits are latched at the falling edge of $\overline{CAS}$.

$\overline{WB/WE}$ (Write-Per-Bit Control/Write Enable). At the falling edge of $\overline{RAS}$ the $\overline{WB/WE}$ input must be low and $\overline{CAS}$ and $\overline{DT/OE}$ high to enable the write- per-bit option. A high $\overline{WB/WE}$ can be used at the beginning of a standard write or read cycle.

$\overline{DT/OE}$ (Data Transfer/Output Enable). At the falling edge of $\overline{RAS}$, $\overline{CAS}$ high and FWE and $\overline{DT/OE}$ low initiate a data transfer, regardless of the level of $\overline{WB/WE}$. $\overline{DT/OE}$ high initiates conventional read or write cycles and controls the output buffer in the random access port.

SO_0-SO_3 (Serial Data Output). Four-bit data is read from these pins. Data remains valid until the next SC signal is activated.

SC (Serial Control). Repeatedly activating this signal causes serial read cycles (starting from the location specified in the data transfer cycle) to be executed within the 2,048 bits in the data register. The rising edge of SC activates serial read operation, in which four of the 2,048 data bits are transferred to four serial data buses, respectively, and read out. Whenever SC is low, the serial port is in standby.

$\overline{SOE}$ (Serial Output Enable). This signal controls the serial data output buffer.

OPERATION

The μPD42273 consists of a random access port and a serial read port. The random access port executes standard read and write cycles as well as data transfer and flash write cycles, all of which are based on conventional $\overline{RAS}/\overline{CAS}$ timing.

In a data transfer, data in each storage cell on the selected row is transferred simultaneously through a transfer gate to its corresponding register location. The serial read port shows the contents of the data register in serial order. The random access and serial read ports can operate asynchronously, except when the transfer gate is turned on during the data transfer period.

Addressing

The storage array is arranged in a 512-row by 2048-column matrix, whereby each of 4 data bits in the random access port corresponds to 262,144 storage cells and 18 address bits are required to decode one cell location. Nine row address bits are set up on pins A_0 through A_8 and latched onto the chip by $\overline{RAS}$. Nine column address bits then are set up on pins A_0 through A_8 and latched onto the chip by $\overline{CAS}$. All addresses must be stable, on or before the falling edges of $\overline{RAS}$ and $\overline{CAS}$. Whenever $\overline{RAS}$ is activated, 2048 cells on the selected row are sensed simultaneously and the sense amplifiers automatically restore the data. $\overline{CAS}$ serves as a chip selection signal to activate the column decoder and the input and output buffers.

Through 1 of 512 column decoders, 4 storage cells on the row are connected to 4 data buses, respectively. In a data transfer cycle, 9 row address bits are used to select 1 of the 512 possible rows involved in the transfer of data to the data register. Nine column address bits are then used to select the 1 of 512 possible serial decoders that corresponds to the starting location of the next serial read cycle. In the serial read port, when SC is activated, 4 data bits in the 2048-bit data register are transferred to 4 serial data buses and read out. Activating SC repeatedly causes serial read cycles (starting from the location specified in the data transfer cycle) to be executed within the 2048 bits in the data register.

Random Access Port

An operation in the random access port begins with a negative transition of $\overline{RAS}$. Both $\overline{RAS}$ and $\overline{CAS}$ have minimum pulse widths, as specified in the timing table, which must be maintained for proper device operation and data integrity. Once begun, a cycle must meet all specifications, including minimum cycle time. To reduce the number of pins, the following are multiplexed.

- $\overline{DT}/\overline{OE}$
- $\overline{WB}/\overline{WE}$
- W_i/IO_i (i = 0, 1, 2, 3)

$\overline{OE}$, $\overline{WE}$ and IO_i represent standard operations, while $\overline{DT}$, $\overline{WB}$, and W_i are special inputs to be applied in the same way as row address inputs, with setup and hold times referenced to the negative transition of $\overline{RAS}$.

The level of $\overline{DT}$ determines whether a cycle is a random access or data transfer operation. $\overline{WB}$ affects only write cycles and determines whether or not the write-per-bit capability is used. W_i defines data bits to be written with the write-per-bit option. In the following discussions, these multiplexed pins are designated as $\overline{DT}(/\overline{OE})$, for example, depending on the function being described.

To use the μPD42273 for random access, $\overline{DT}(/\overline{OE})$ must be high as $\overline{RAS}$ falls to disconnect the 2048-bit register from the corresponding 2048-digit lines of the storage array. Conversely, to execute a data transfer, $\overline{DT}(/\overline{OE})$ must be low as $\overline{RAS}$ falls to open the 2048 transfer gates and transfer data from one of the rows to the register.

Truth Table for the Random Access Port

$\overline{CAS}$	$\overline{DT}/\overline{OE}$	$\overline{WB}/\overline{WE}$	Cycle
H	H	H	Read or write (Note 1)
H	H	L	Mask write (Note 2)
H	L	X	Read data transfer (Note 3)
L	X	X	$\overline{CAS}$ before $\overline{RAS}$ refresh (Note 4)

Notes:

(1) Initiates a normal read or write cycle and disables the write-per-bit capability.

(2) Enables individual bits to be selected or masked for a write cycle. Four-bit masked data is latched at the falling edge of $\overline{RAS}$ and reset at the rising edge of $\overline{RAS}$.

(3) Initiates a read data transfer cycle.

(4) Initiates a $\overline{CAS}$ before $\overline{RAS}$ refresh cycle. As $\overline{RAS}$ falls, $\overline{WB}/\overline{WE}$ and $\overline{DT}/\overline{OE}$ = don't care.

(5) X = don't care.

Read Cycle. A read cycle is executed by activating $\overline{RAS}$, $\overline{CAS}$, and $\overline{OE}$ and by maintaining ($\overline{WB}$/)$\overline{WE}$ while $\overline{CAS}$ is active. The (W_i/)IO_i pin (i = 0, 1, 2, 3) remains in high impedance until valid data appears at the output at access time. Device access time, t_{ACC}, will be the longest of the following four calculated intervals:

- t_{RAC}
- $\overline{RAS}$ to ±CAS delay (t_{RCD}) + t_{CAC}
- $\overline{RAS}$ to column address delay (t_{RAD}) + t_{AA}
- $\overline{RAS}$ to $\overline{OE}$ delay + t_{OEA}

Access times from $\overline{RAS}$ (t_{RAC}), from $\overline{CAS}$ (t_{CAC}), from the column addresses (t_{AA}), and from $\overline{OE}$ (t_{OEA}) are device parameters. The $\overline{RAS}$-to-$\overline{CAS}$, $\overline{RAS}$-to-column address, and $\overline{RAS}$-to-$\overline{OE}$ delays are system-dependent timing parameters. Output becomes valid after the access time has elapsed and it remains valid while both $\overline{CAS}$ and $\overline{OE}$ are low. Either $\overline{CAS}$ or $\overline{OE}$ high returns the output pins to high impedance.

Write Cycle. A write cycle is executed by bringing ($\overline{WB}$/)$\overline{WE}$ low during the $\overline{RAS}$/$\overline{CAS}$ cycle. The falling edge of $\overline{CAS}$ or ($\overline{WB}$/)$\overline{WE}$ strobes the data on (W_i/)IO_i into the on-chip data latch. To make use of the write-per-bit option, $\overline{WB}$(/$\overline{WE}$) must be low as $\overline{RAS}$ falls. In this case, write data bits can be specified by keeping W_i($/IO_i$) high, with setup and hold times referenced to the negative transition of $\overline{RAS}$.

For those data bits of W_i($/IO_i$) that are kept low as $\overline{RAS}$ falls, write operation is inhibited on the chip. If $\overline{WB}$(/$\overline{WE}$) is high as $\overline{RAS}$ falls, the write-per-bit option is not used and a write cycle is executed for all four data bits.

Early Write Cycle. An early write cycle is executed by bringing ($\overline{WB}$/)$\overline{WE}$ low before $\overline{CAS}$ falls. Data is strobed by $\overline{CAS}$, with setup and hold times referenced to this signal, and the output remains in high impedance for the entire cycle. As $\overline{RAS}$ falls, ($\overline{DT}$/)$\overline{OE}$ must meet the setup and hold times of a high $\overline{DT}$, but otherwise ($\overline{DT}$/)$\overline{OE}$ does not affect anything while $\overline{CAS}$ is active.

Read-Write/Read-Modify-Write Cycle. This cycle is executed by bringing ($\overline{WB}$/)$\overline{WE}$ low with the $\overline{RAS}$ and $\overline{CAS}$ signals low. (W_i/)IO_i shows read data at access time. Afterward, in preparation for the upcoming write cycle, (W_i/)IO_i returns to high impedance when ($\overline{DT}$/)$\overline{OE}$ goes high. The data to be written is strobed by ($\overline{WB}$/)$\overline{WE}$, with setup and hold times referenced to this signal.

Late Write Cycle. This cycle shows the timing flexibility of ($\overline{DT}$/)$\overline{OE}$, which can be activated just after ($\overline{WB}$/)$\overline{WE}$ falls, even when ($\overline{WB}$/)$\overline{WE}$ is brought low after $\overline{CAS}$.

Refresh Cycle. A cycle at each of the 512 row addresses (A_0 through A_8) will refresh all storage cells. Any read, write, refresh, or data transfer cycle executed in the random access port refreshes the 2048 bits selected by the $\overline{RAS}$ addresses or by the on-chip address counter.

$\overline{RAS}$-Only Refresh Cycle. A cycle having only $\overline{RAS}$ active refreshes all cells in one row of the storage array. A high $\overline{CAS}$ is maintained while $\overline{RAS}$ is active to keep (W_i/)IO_i in high impedance. This method is preferred for refreshing, especially when the host system consists of multiple rows of random access devices. The data outputs may be OR-tied with no bus contention when $\overline{RAS}$-only refresh cycles are executed.

$\overline{CAS}$ Before $\overline{RAS}$ Refresh Cycle. This cycle executes internal refreshing using the on-chip circuitry. Whenever $\overline{CAS}$ is low as $\overline{RAS}$ falls, the row addresses specified by the internal counter are automatically refreshed and the circuit operation based on $\overline{CAS}$ is maintained in a reset state. When internal refreshing is complete, the address counter automatically increments in preparation for the next $\overline{CAS}$ before $\overline{RAS}$ cycle.

Hidden Refresh Cycle. This cycle is executed after a read cycle, without disturbing the read data output. Once valid, the data output is controlled by $\overline{CAS}$ and $\overline{OE}$. After the read cycle, $\overline{CAS}$ is held low while $\overline{RAS}$ goes high for precharge. A $\overline{RAS}$-only cycle is then executed (except that $\overline{CAS}$ is held at a low level instead of a high level) and the data output remains valid. Since hidden refreshing is the same as $\overline{CAS}$ before $\overline{RAS}$ refreshing, the data output remains valid during either operation.

Fast-Page Cycle. This feature allows faster data access by keeping the same row address while successive column addresses are strobed onto the chip. Maintaining $\overline{RAS}$ low while successive $\overline{CAS}$ cycles are executed causes data to be transferred at a faster rate because row addresses are maintained internally and do not have to be reapplied. In fast-page operation, read, write and read-write/read-modify-write cycles may be executed. Additionally, the write-per-bit control specified in the entry write cycle is maintained throughout the next fast-page write cycle.

During a fast-page read cycle, (W_i/)IO_i remains in high impedance until valid data appears at the output pin at access time. Device access time in this cycle will be one of the following calculated intervals:

Fast-Page Access Time

Calculated Interval	Conditions
t_{ACP}	$t_{ASC} \geq t_{CP}$ and $t_{CP} \leq t_{CP}$ (max)
t_{AA}	$t_{ASC} \leq t_{ASC}$ (max) and $t_{CP} \geq t_{CP}$ (max)
	$t_{ASC} \leq t_{CP}$ and $t_{CP} \leq t_{CP}$ (max)
t_{CAC}	$t_{ASC} \geq t_{ASC}$ (max) and $t_{CP} \leq t_{CP}$ (max)

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Data Transfer Cycle. A data transfer is executed by bringing $\overline{DT}(/\overline{OE})$ low as $\overline{RAS}$ falls. $\overline{DT}(/\overline{OE})$ must be low for a specified time, measured from $\overline{RAS}$ and $\overline{CAS}$. The specified 1 of the possible 512 rows involved in the data transfer, as well as the starting location of the following serial read cycle, are defined by address inputs. The low-to-high transition of $\overline{DT}$ causes column address buffer outputs to be transferred to the serial address counters, and storage cell data amplified on digit lines to be transferred to the data register. $\overline{RAS}$ and $\overline{CAS}$ must be low during these operations to keep the data in the random access port.

Serial Read Port

After the data transfer cycle, the serial read port is only used to serially read the contents of the data register starting from a specified location. The only condition under which the serial read port must synchronize with the random access port is when the positive transition of $\overline{DT}(/\overline{OE})$ must occur within a specified period in an SC cycle. Otherwise, the serial read port can operate asynchronously. Output data appears at SO_i after an access time of t_{SCA}, measured from SC high, only when $\overline{SOE}$ is maintained low. The SC cycle which includes the positive transition of $\overline{DT}(/\overline{OE})$ shows old data in the data register; subsequent SC cycles show new data transferred to the data register serially and in a looped manner. The serial output is maintained until the next SC signal is activated. $\overline{SOE}$ controls the impedance of the serial output to allow multiplexing of more than one bank of μPD42273 graphics buffers into the same external circuitry. When $\overline{SOE}$ is at a low logic level, SO_i is enabled and the proper data is read. When $\overline{SOE}$ is high, SO_i is disabled and in a state of high impedance.

Power Supply Current

T_A = 0 to +70°C; V_{CC} = +5.0 V ±10%; GND = 0 V

Port Operation			μPD42273-10	μPD42273-12		
Random Access	Serial Read	Parameter	(max)	(max)	Unit	Test Conditions
Read/write cycle	Standby	I_{CC1}	95	85	mA	$\overline{RAS}$, $\overline{CAS}$ cycling; $t_{RC} = t_{RC}$ min; $\overline{SOE} = V_{IH}$; SC = V_{IH} or V_{IL}
Standby	Standby	I_{CC2}	4	4	mA	$\overline{CAS} = \overline{RAS} = V_{IH}$; $\overline{SOE} = V_{IH}$; SC = V_{IH} or V_{IL}
$\overline{RAS}$-only refresh cycle	Standby	I_{CC3}	95	85	mA	$\overline{RAS}$ cycling; $\overline{CAS} = V_{IH}$; $t_{RC} = t_{RC}$ min; $\overline{SOE} = V_{IH}$; SC = V_{IH} or V_{IL} (Note 2)
Fast-page cycle	Standby	I_{CC4}	90	80	mA	$\overline{RAS} = V_{IL}$; $\overline{CAS}$ cycling; $t_{PC} = t_{PC}$ min; $\overline{SOE} = V_{IH}$; SC = V_{IH} or V_{IL} (Note 3)
$\overline{CAS}$ before $\overline{RAS}$ refresh cycle	Standby	I_{CC5}	95	85	mA	$\overline{CAS}$ low as $\overline{RAS}$ falls; $t_{RC} = t_{RC}$ min; $\overline{SOE} = V_{IH}$; SC = V_{IH} or V_{IL}
Data transfer cycle	Standby	I_{CC6}	135	120	mA	$\overline{DT}$ low as $\overline{RAS}$ falls; $t_{RC} = t_{RC}$ min; $\overline{SOE} = V_{IH}$; SC = V_{IH} or V_{IL}
Read/write cycle	Active	I_{CC7}	120	105	mA	$\overline{RAS}$ and $\overline{CAS}$ cycling; $t_{RC} = t_{RC}$ min $\overline{SOE} = V_{IL}$; SC cycling; $t_{SCC} = t_{SCC}$ min
Standby	Active	I_{CC8}	30	25	mA	$\overline{CAS} = \overline{RAS} = V_{IH}$; $\overline{SOE} = V_{IL}$; SC cycling; $t_{SCC} = t_{SCC}$ min
$\overline{RAS}$-only refresh cycle	Active	I_{CC9}	120	105	mA	$\overline{RAS}$ cycling; $\overline{CAS} = V_{IH}$; $t_{RC} = t_{RC}$ min; $\overline{SOE} = V_{IL}$; SC cycling; $t_{SCC} = t_{SCC}$ min
Fast-page cycle	Active	I_{CC10}	115	100	mA	$\overline{RAS} = V_{IL}$; $\overline{CAS}$ cycling; $t_{PC} = t_{PC}$ min; $\overline{SOE} = V_{IL}$; SC cycling; $t_{SCC} = t_{SCC}$ min (Note 3)
$\overline{CAS}$ before $\overline{RAS}$ refresh cycle	Active	I_{CC11}	120	105	mA	$\overline{CAS}$ low as $\overline{RAS}$ falls; $t_{RC} = t_{RC}$ min; $\overline{SOE} = V_{IL}$; SC cycling; $t_{SCC} = t_{SCC}$ min
Data transfer cycle	Active	I_{CC12}	160	140	mA	$\overline{DT}$ low as $\overline{RAS}$ falls; $t_{RC} = t_{RC}$ min; $\overline{SOE} = V_{IL}$; SC cycling; $t_{SCC} = t_{SCC}$ min

Notes:

(1) No load on IO_i or SO_i. Except for I_{CC2}, I_{CC3}, I_{CC6}, and I_{CC14}, real values depend on output loading in addition to cycle rates.

(2) $\overline{CAS}$ is not clocked, but is kept at a stable high level. Column addresses are also assumed to be at a stable high or low level.

(3) A change in column addresses must not occur more than once in a fast-page cycle.

DC Characteristics

T_A = 0 to +70°C; V_{CC} = +5.0 V ±10%; GND = 0 V

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions
Input leakage current	I_{IL}	−10		10	μA	V_{IN} = 0 to 5.5 V; all other pins not under test = 0 V
Output leakage current	I_{OL}	−10		10	μA	D_{OUT} (IO_i, SO_i) disabled; V_{OUT} = 0 to 5.5 V
Random access port output voltage, high	$V_{OH(R)}$	2.4			V	$I_{OH(R)}$ = −2 mA
Random access port output voltage, low	$V_{OL(R)}$			0.4	V	$I_{OL(R)}$ = 4.2 mA
Serial read port output voltage, high	$V_{OH(S)}$	2.4			V	$I_{OH(S)}$ = −1 mA
Serial read port output voltage, low	$V_{OL(S)}$			0.4	V	$I_{OL(S)}$ = 2.1 mA

AC Characteristics

T_A = 0 to +70°C; V_{CC} = +5.0 V ±10%; GND = 0 V

		μPD42273-10		μPD42273-12			
Parameter	Symbol	Min	Max	Min	Max	Unit	Test Conditions
Switching Characteristics							
Access time from $\overline{RAS}$	t_{RAC}		100		120	ns	(Notes 3, 4 and 12)
Access time from falling edge of $\overline{CAS}$	t_{CAC}		25		30	ns	(Notes 3, 4, 13, 14 and 15)
Access time from column address	t_{AA}		55		65	ns	(Notes 3, 4, 14 and 15)
Access time from rising edge of $\overline{CAS}$	t_{ACP}		55		65	ns	(Notes 3 and 4)
Access time from $\overline{OE}$	t_{OEA}		25		30	ns	(Notes 3 and 4)
Serial output access time from SC	t_{SCA}		30		40	ns	(Notes 3 and 18)
Serial output access time from $\overline{SOE}$	t_{SOA}		25		30	ns	(Note 3)
Output disable time from $\overline{CAS}$ high	t_{OFF}	0	25	0	30	ns	(Note 5)
Output disable time from $\overline{OE}$ high	t_{OEZ}	0	25	0	30	ns	(Note 5)
Serial output disable time from $\overline{SOE}$ high	t_{SOZ}	0	15	0	20	ns	(Note 5)
$\overline{SOE}$ low to serial output setup delay	t_{SOO}	5		5		ns	
Serial output hold time after SC high	t_{SOH}	5		5		ns	
Timing Requirements							
Random read or write cycle time	t_{RC}	190		220		ns	(Note 11)
Read-write/read-modify-write cycle time	t_{RWC}	255		295		ns	(Note 11)
Fast-page cycle time	t_{PC}	60		70		ns	(Note 11)
Fast-page read-write/read-modify-write cycle time	t_{PRWC}	125		145		ns	(Note 11)
Rise and fall transition time	t_T	3	50	3	50	ns	(Notes 3, 10 and 18)
$\overline{RAS}$ precharge time	t_{RP}	80		90		ns	(Note 18)
$\overline{RAS}$ pulse width	t_{RAS}	100	10,000	120	10,000	ns	
Fast-page $\overline{RAS}$ pulse width	t_{RASP}	100	100,000	120	100,000	ns	
$\overline{RAS}$ hold time	t_{RSH}	25		30		ns	
$\overline{CAS}$ precharge time (nonpage cycle)	t_{CPN}	10		15		ns	
Fast-page $\overline{CAS}$ precharge time	t_{CP}	10	25	15	30	ns	
$\overline{CAS}$ pulse width	t_{CAS}	25	10,000	30	10,000	ns	
$\overline{CAS}$ hold time	t_{CSH}	100		120		ns	
$\overline{RAS}$ to $\overline{CAS}$ delay	t_{RCD}	25	75	25	90	ns	(Note 4)
$\overline{CAS}$ high to $\overline{RAS}$ low precharge time	t_{CRP}	10		10		ns	(Note 16)

AC Characteristics (cont)

Parameter	Symbol	μPD42273-10 Min	μPD42273-10 Max	μPD42273-12 Min	μPD42273-12 Max	Unit	Test Conditions
Timing Requirements (cont)							
Row address setup time	t_{ASR}	0		0		ns	
Row address hold time	t_{RAH}	12		15		ns	
Column address setup time	t_{ASC}	0	25	0	30	ns	(Note 15)
Column address hold time	t_{CAH}	15		20		ns	
$\overline{RAS}$ to column address delay time	t_{RAD}	17	45	20	55	ns	(Notes 9 and 14)
Column address to $\overline{RAS}$ lead time	t_{RAL}	55		65		ns	
Read command setup time	t_{RCS}	0		0		ns	
Read command hold time after $\overline{RAS}$ high	t_{RRH}	10		10		ns	(Note 6)
Read command hold time after $\overline{CAS}$ high	t_{RCH}	0		0		ns	(Note 6)
Write command setup time	t_{WCS}	0		0		ns	(Note 7)
Write command hold time	t_{WCH}	20		30		ns	
Write command pulse width	t_{WP}	20		25		ns	(Note 17)
Write command to $\overline{RAS}$ lead time	t_{RWL}	30		35		ns	
Write command to $\overline{CAS}$ lead time	t_{CWL}	30		35		ns	
Data-in setup time	t_{DS}	0		0		ns	(Note 8)
Data-in hold time	t_{DH}	20		25		ns	(Note 8)
Column address to $\overline{WE}$ delay	t_{AWD}	85		100		ns	(Note 7)
$\overline{CAS}$ to $\overline{WE}$ delay	t_{CWD}	55		65		ns	(Note 7)
$\overline{RAS}$ to $\overline{WE}$ delay	t_{RWD}	130		155		ns	(Note 7)
$\overline{OE}$ high to data-in setup delay	t_{OED}	30		35		ns	
$\overline{OE}$ high hold time after $\overline{WE}$ low	t_{OEH}	25		30		ns	
$\overline{CAS}$ before $\overline{RAS}$ refresh setup time	t_{CSR}	0		0		ns	
$\overline{CAS}$ before $\overline{RAS}$ refresh hold time	t_{CHR}	15		20		ns	
$\overline{RAS}$ high to $\overline{CAS}$ low precharge time	t_{RPC}	0		0		ns	
Refresh interval	t_{REF}		8		8	ms	Addresses A_0 through A_8
$\overline{DT}$ low setup time	t_{DLS}	0		0		ns	
$\overline{DT}$ low hold time after $\overline{RAS}$ low	t_{RDH}	80		90		ns	(Note 18)
$\overline{DT}$ low hold time after $\overline{CAS}$ low	t_{CDH}	30		35		ns	
SC high to $\overline{DT}$ high delay	t_{SDD}	10		15		ns	
SC low hold time after $\overline{DT}$ high	t_{SDH}	10		15		ns	
Serial clock cycle time	t_{SCC}	30		40		ns	(Note 11)
SC pulse width	t_{SCH}	10		15		ns	
SC precharge time	t_{SCL}	10		15		ns	
$\overline{DT}$ high setup time	t_{DHS}	0		0		ns	
$\overline{DT}$ high hold time	t_{DHH}	15		20		ns	
$\overline{DT}$ high to $\overline{RAS}$ high delay	t_{DTR}	10		10		ns	
$\overline{DT}$ high to $\overline{CAS}$ high delay	t_{DTC}	5		5		ns	

AC Characteristics (cont)

Parameter	Symbol	μPD42273-10 Min	μPD42273-10 Max	μPD42273-12 Min	μPD42273-12 Max	Unit	Test Conditions
Timing Requirements (cont)							
$\overline{OE}$ to $\overline{RAS}$ inactive setup time	t_{OES}	10		10		ns	
Write-per-bit setup time	t_{WBS}	0		0		ns	
Write-per-bit hold time	t_{WBH}	15		20		ns	
Write bit selection setup time	t_{WS}	0		0		ns	
Write bit selection hold time	t_{WH}	15		20		ns	
$\overline{SOE}$ pulse width	t_{SOE}	10		15		ns	
$\overline{SOE}$ precharge time	t_{SOP}	10		15		ns	
$\overline{DT}$ high hold time after $\overline{RAS}$ high	t_{DTH}	15		20		ns	

Notes:

(1) All voltages are referenced to GND.

(2) An initial pause of 100 μs is required after power-up, followed by any eight $\overline{RAS}$ cycles and four data transfer (DT) cycles, before proper device operation is achieved.

(3) See input/output timing waveforms for timing reference voltages. See figures 3 and 4 for output loads.

(4) Operation within the t_{RCD} (max) limit ensures that t_{RAC} (max) can be met. The t_{RCD} (max) limit is specified as a reference point only. If t_{RCD} is greater than the specified t_{RCD} (max) limit, access time is controlled exclusively by t_{CAC}, t_{OEA}, or t_{AA}.

(5) An output disable time defines the time at which the output achieves the open-circuit condition and is not referenced to output voltage levels.

(6) Either t_{RRH} or t_{RCH} must be satisfied for a read cycle.

(7) t_{WCS}, t_{AWD}, t_{CWD}, and t_{RWD} are restrictive operating parameters in read-write and read-modify-write cycles only. If $t_{WCS} \geq t_{WCS}$ (min), the cycle is an early write cycle and the data output will remain open-circuit throughout the entire cycle. If $t_{AWD} \geq t_{AWD}$ (min), $t_{CWD} \geq t_{CWD}$ (min), and $t_{RWD} \geq t_{RWD}$ (min), the cycle is a read-write cycle and the data output will contain data read from the selected cell. If neither of the above conditions is met, the condition of the data out (at access time and until $\overline{CAS}$ returns to V_{IH}) is indeterminate.

(8) These parameters are referenced to the falling edge of $\overline{CAS}$ in early write cycles and to the falling edge of (WB/)WE in delayed write or read-modify-write cycles.

(9) Assumes that t_{RAD} (min) = t_{RAH} (min) + typical t_T of 5 ns.

(10) V_{IH} (min) and V_{IL} (max) are reference levels for measuring the timing of input signals. Additionally, transition times are measured between V_{IH} and V_{IL}.

(11) The minimum specifications are used only to indicate the cycle time at which proper operation over the full temperature range (T_A = 0 to +70°C) is assured.

(12) Assumes that $t_{RCD} \leq t_{RCD}$ (max) and $t_{RAD} \leq t_{RAD}$ (max). If t_{RCD} or t_{RAD} is greater than the maximum recommended value in this table, t_{RAC} increases by the amount that t_{RCD} or t_{RAD} exceeds the value shown.

(13) Assumes that $t_{RCD} \geq t_{RCD}$ (max) and $t_{RAD} \leq t_{RAD}$ (max).

(14) If $t_{RAD} \geq t_{RAD}$ (max), then the access time is defined by t_{AA}.

(15) For fast-page read operation, the definition of access time is as follows.

$\overline{CAS}$ and Column Address Input Conditions	Access Time Definition
$t_{CP} \leq t_{CP}$ (max), $t_{ASC} \geq t_{CP}$	t_{ACP}
$t_{CP} \leq t_{CP}$ (max), $t_{ASC} \leq t_{CP}$	t_{AA}
$t_{CP} \geq t_{CP}$ (max), $t_{ASC} \leq t_{ASC}$ (max)	t_{AA}
$t_{CP} \geq t_{CP}$ (max), $t_{ASC} \geq t_{ASC}$ (max)	t_{CAC}

(16) The t_{CRP} requirement is applicable for $\overline{RAS}$/$\overline{CAS}$ cycles preceded by any cycle.

(17) Parameter t_{WP} is applicable for a delayed write cycle such as a read-write/read-modify-write cycle. For early write operation, both t_{WCS} and t_{WCH} must be met.

(18) Improvement in parameters t_{RDH}, t_{RP} and t_{SCA} are planned for process versions "x" and "m". Please contact your NEC sales office for details.

(19) Ac measurements assume t_T = 5 ns.

Figure 1. Input Timing

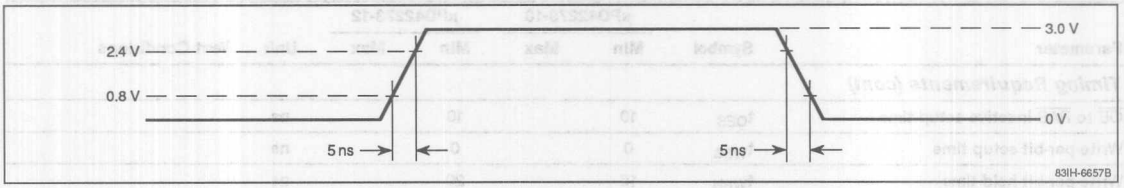


Figure 2. Output Timing

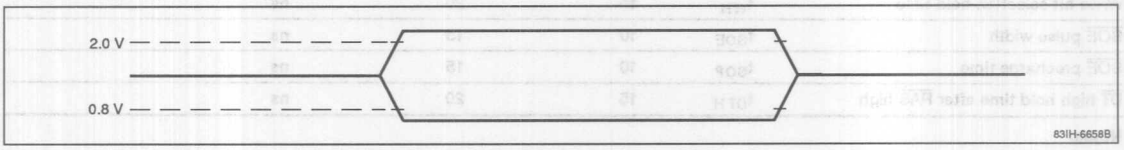


Figure 3. Output Load in Random Access Port

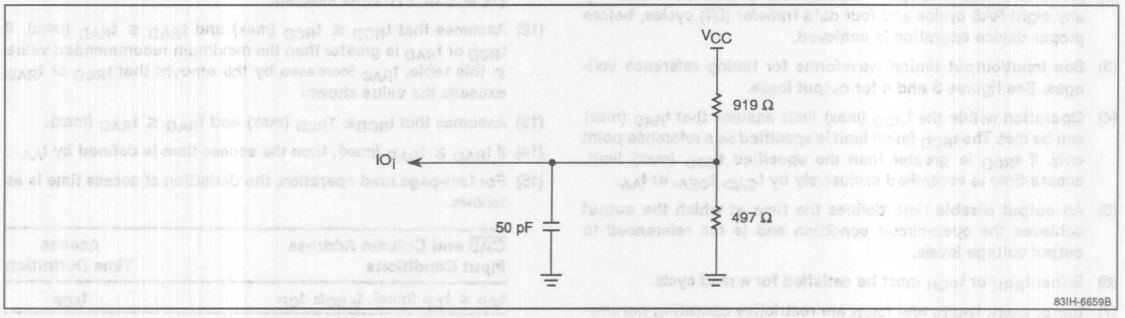
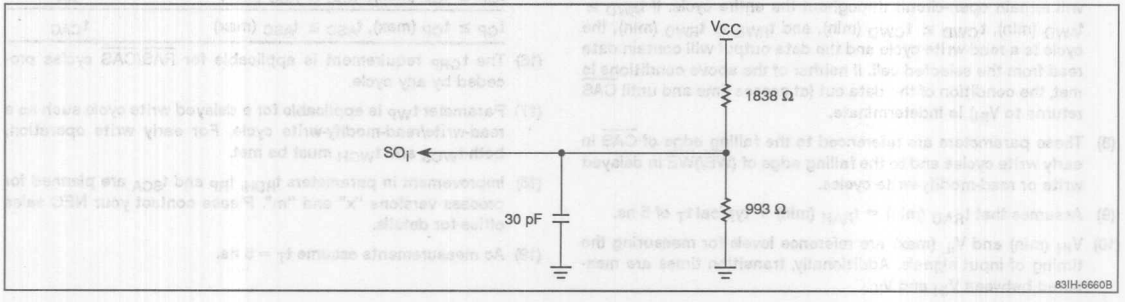
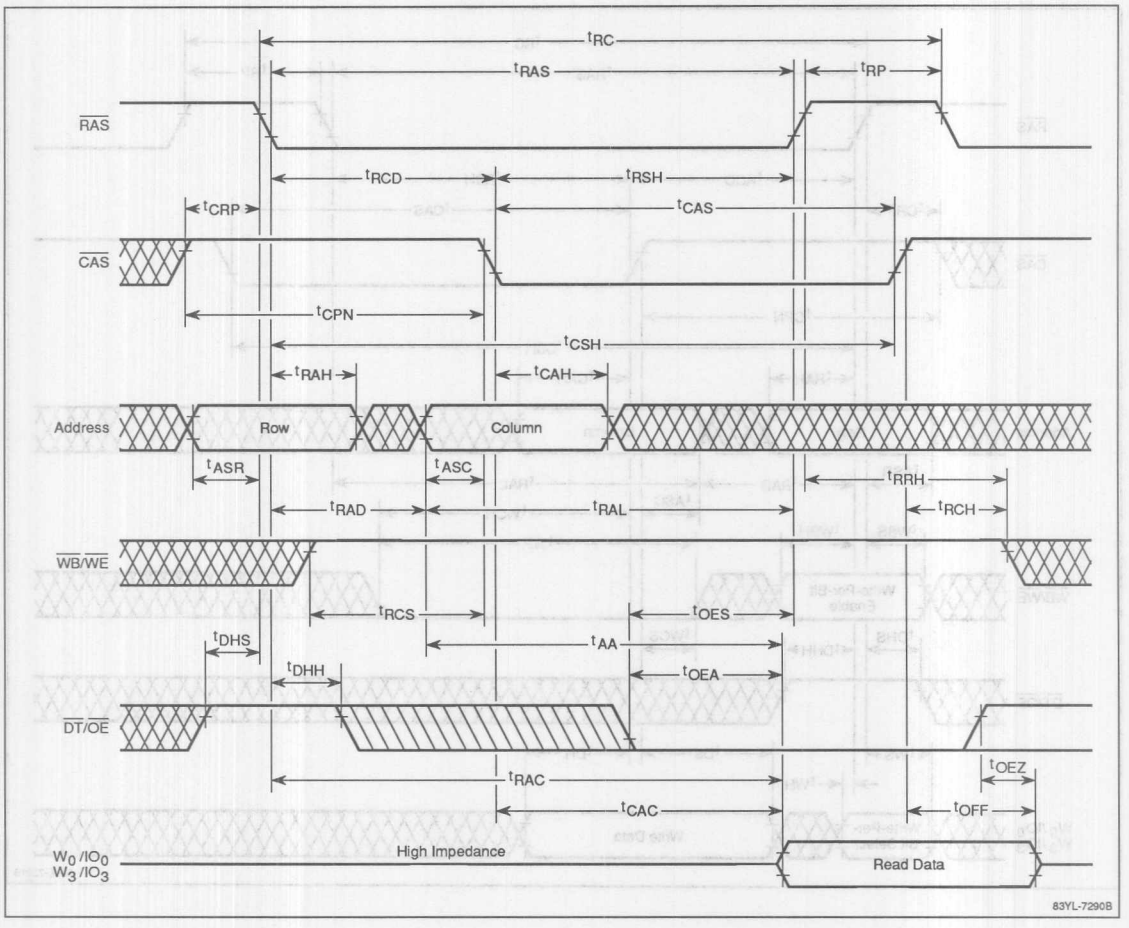


Figure 4. Output Load in Serial Read Port



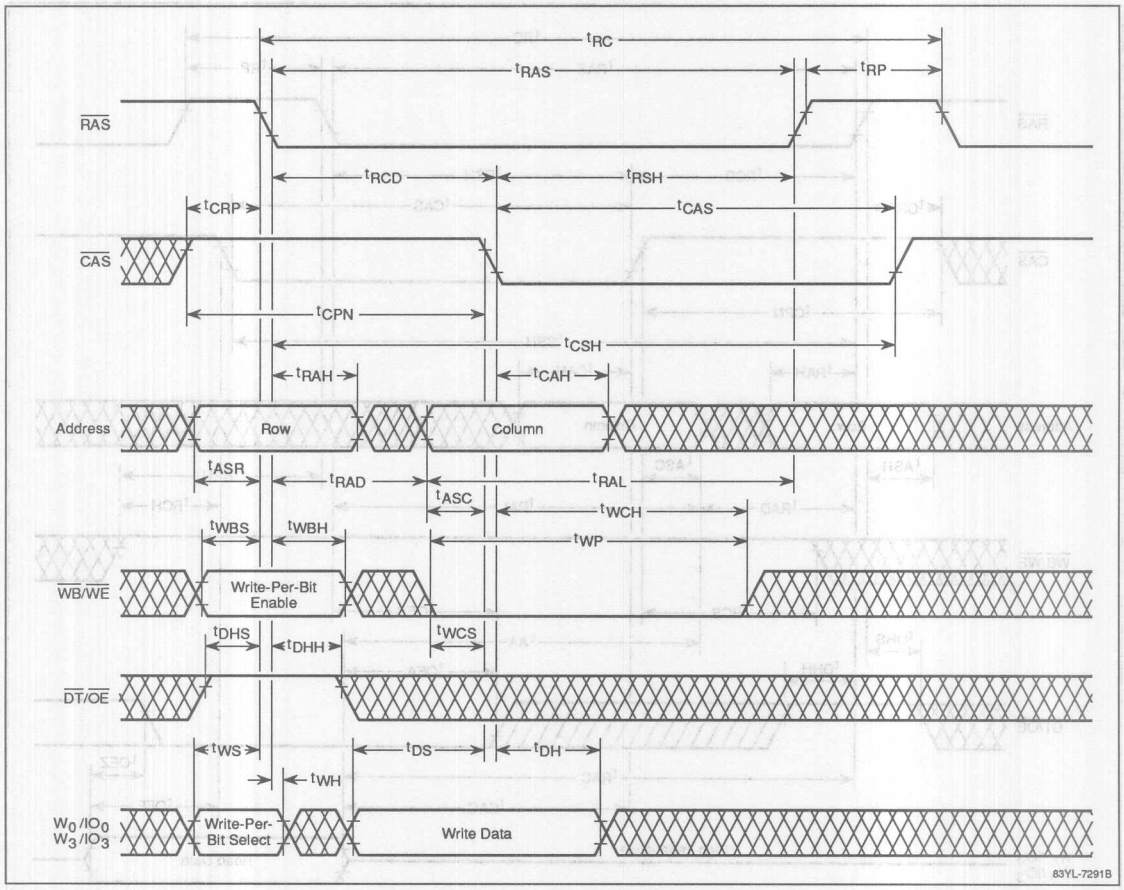
Timing Waveforms

Read Cycle



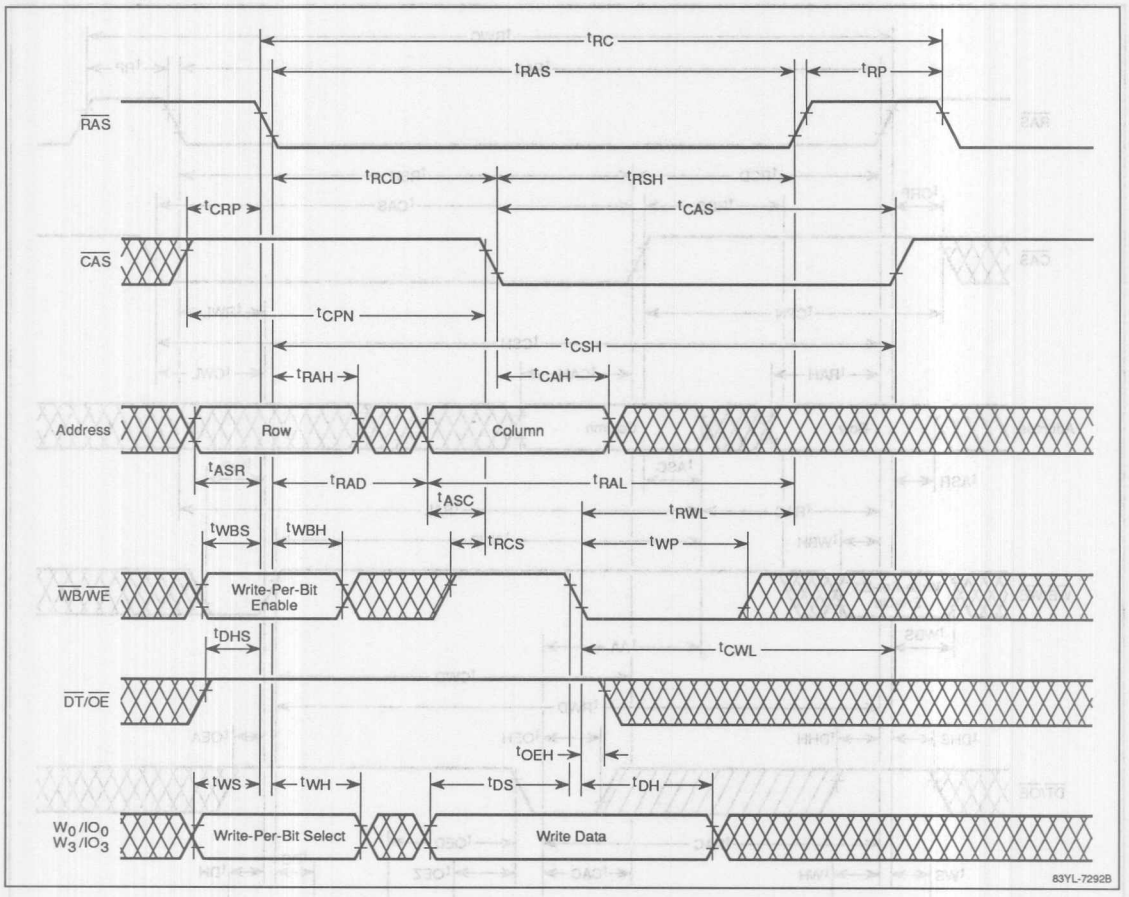
Timing Waveforms (cont)

Early Write Cycle



Timing Waveforms (cont)

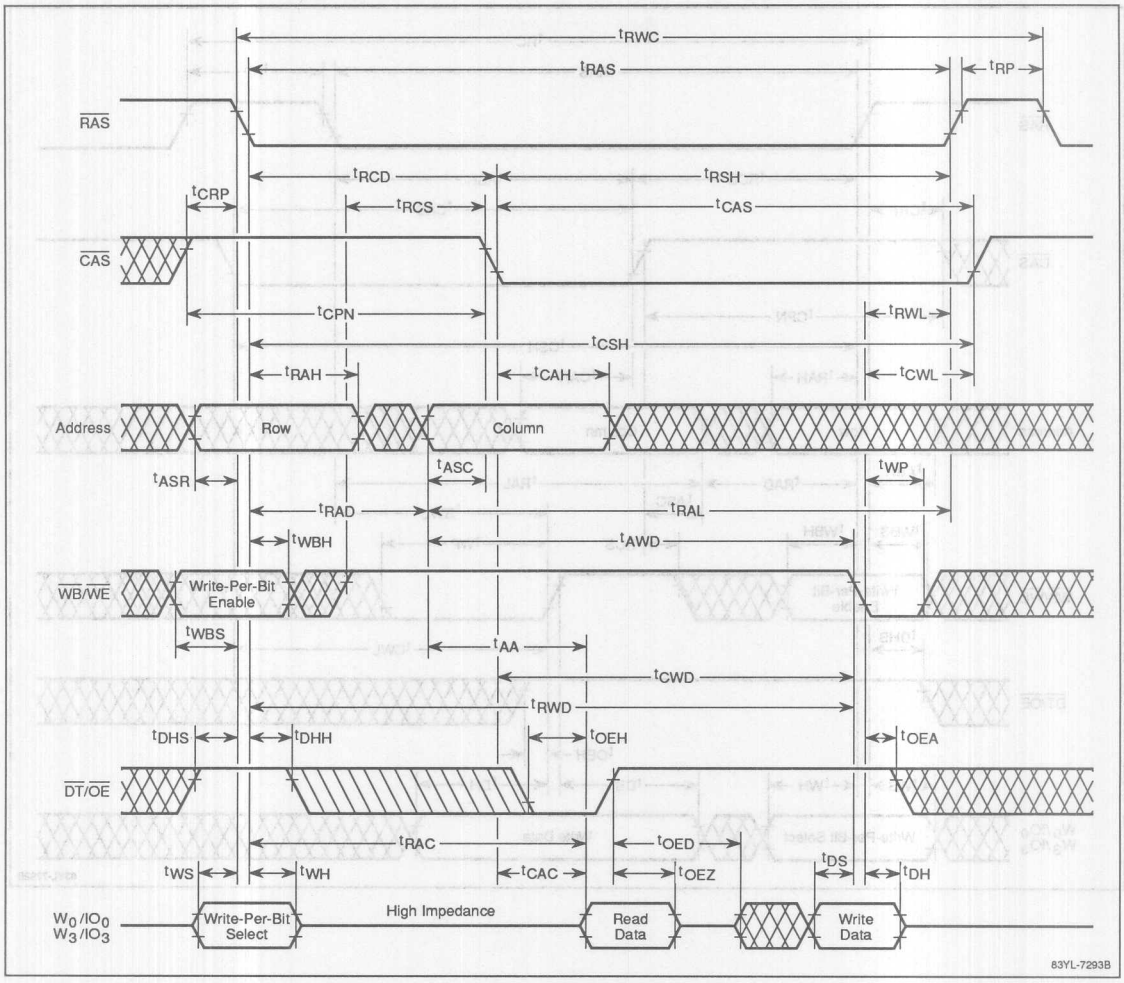
Late Write Cycle



3

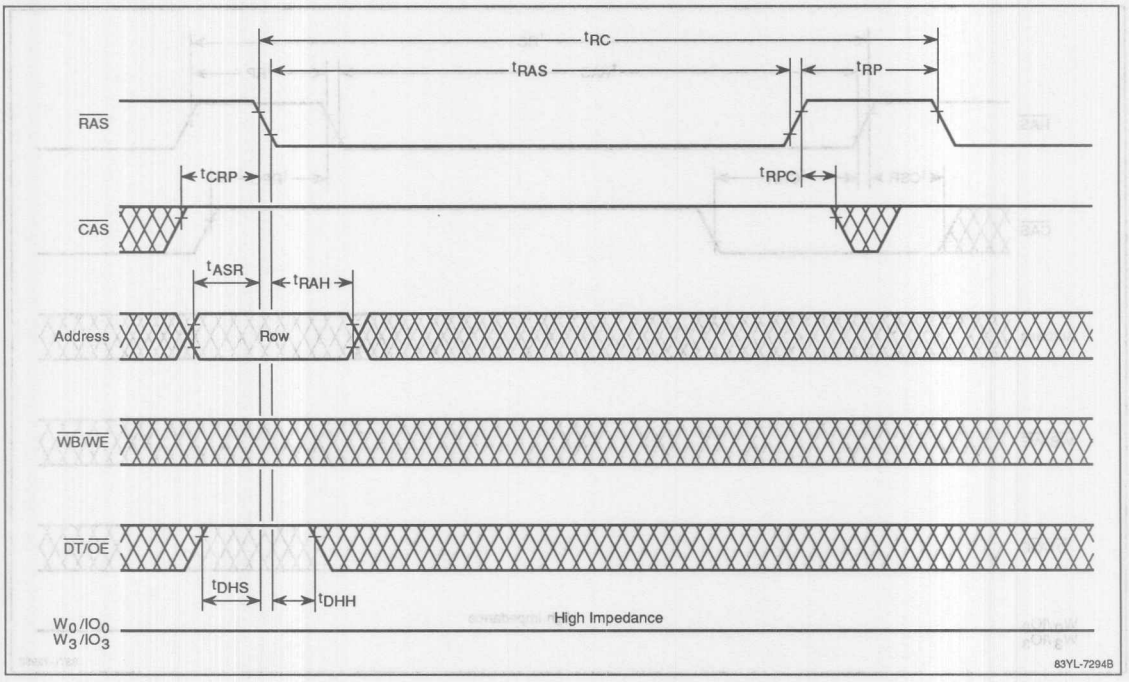
Timing Waveforms (cont)

Read-Write/Read-Modify-Write Cycle



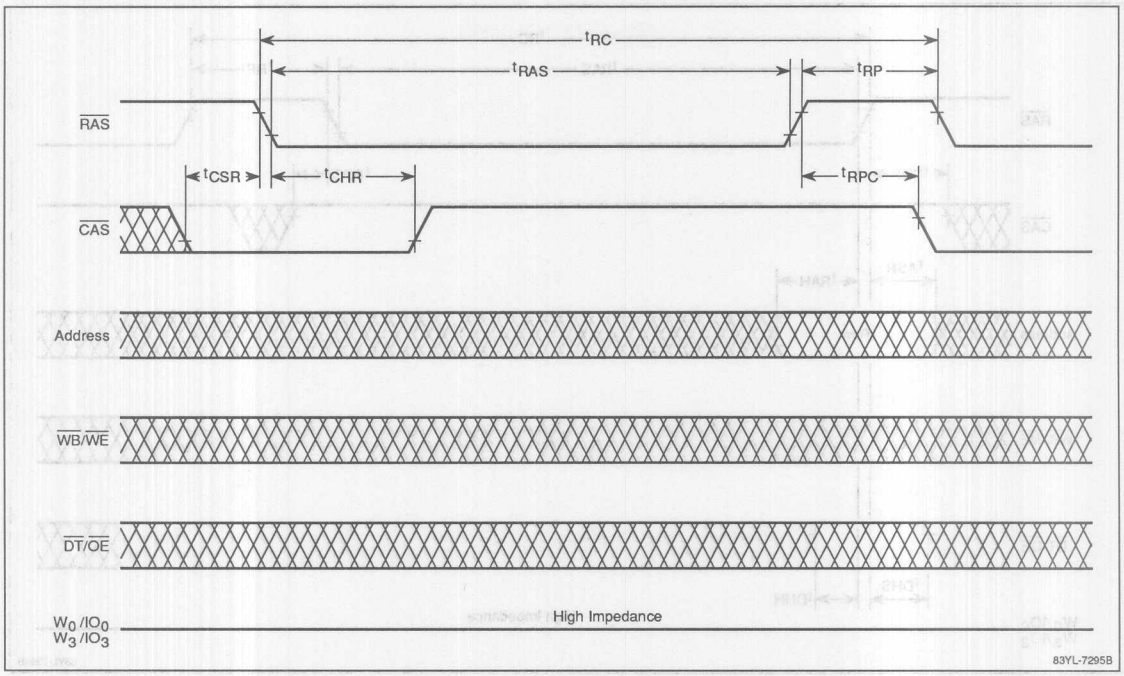
Timing Waveforms (cont)

$\overline{RAS}$-Only Refresh Cycle



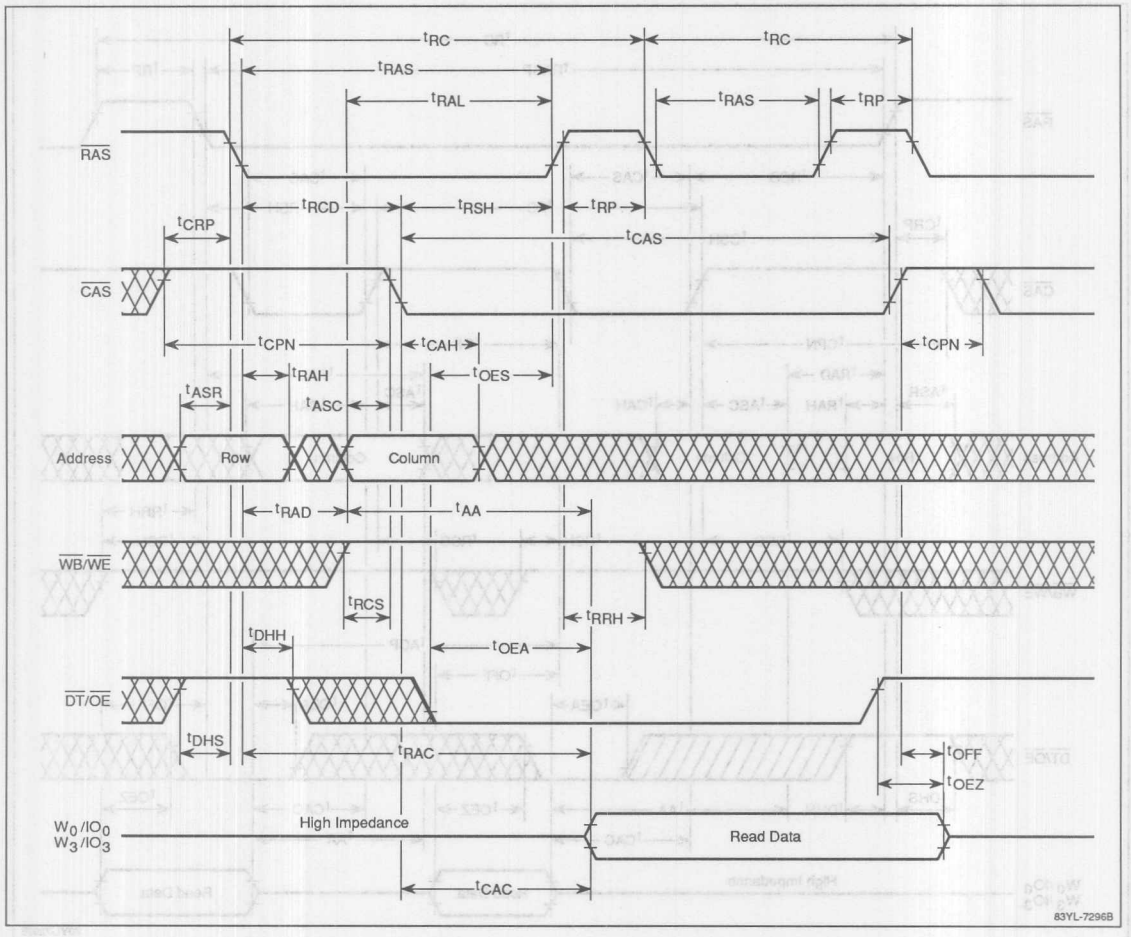
Timing Waveforms (cont)

$\overline{CAS}$ Before $\overline{RAS}$ Refresh Cycle



Timing Waveforms (cont)

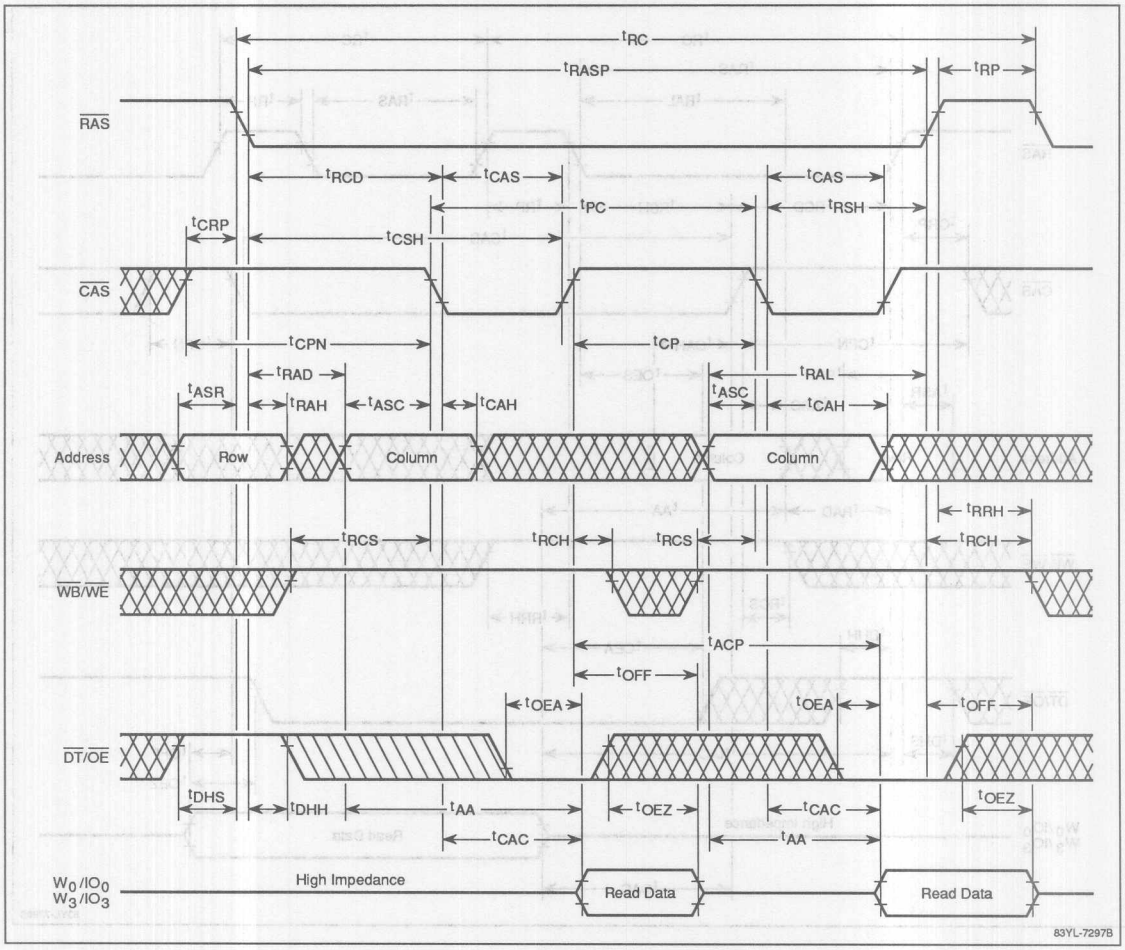
Hidden Refresh Cycle



3

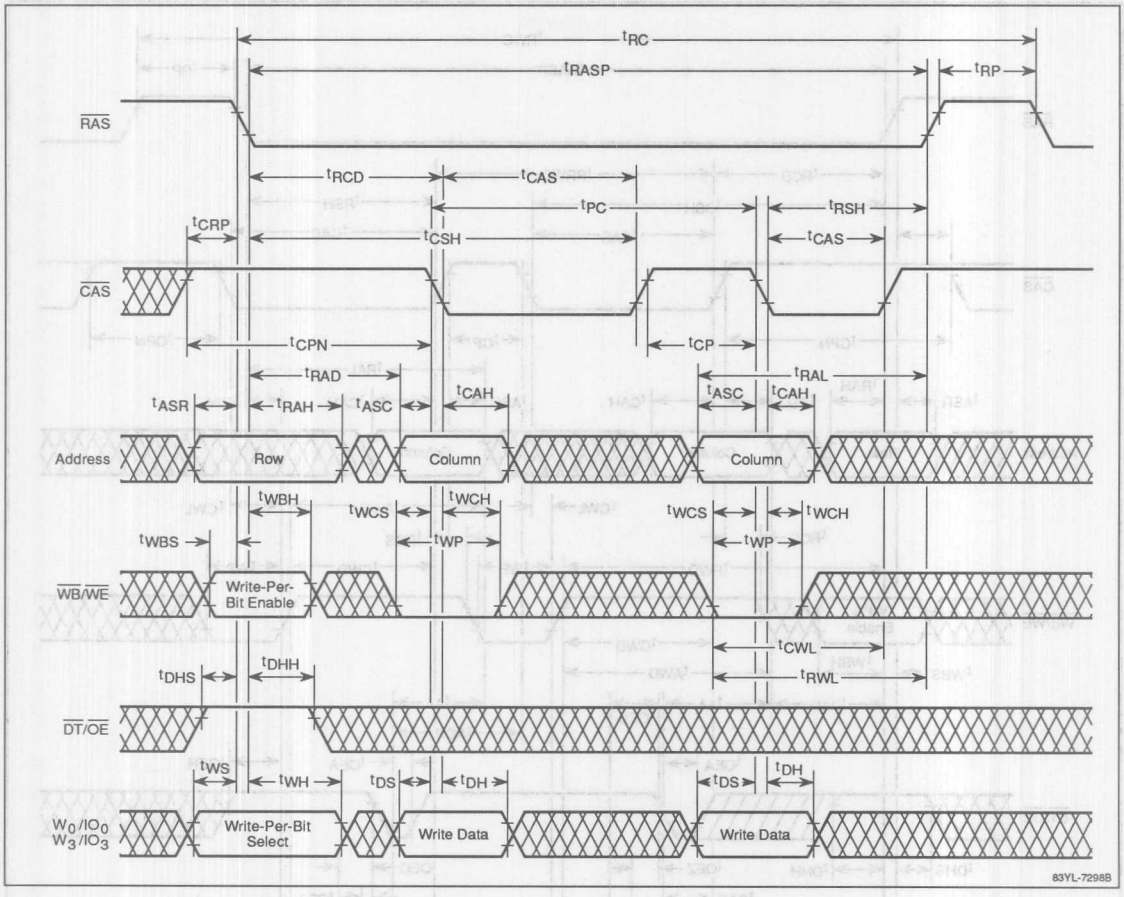
Timing Waveforms (cont)

Fast-Page Read Cycle



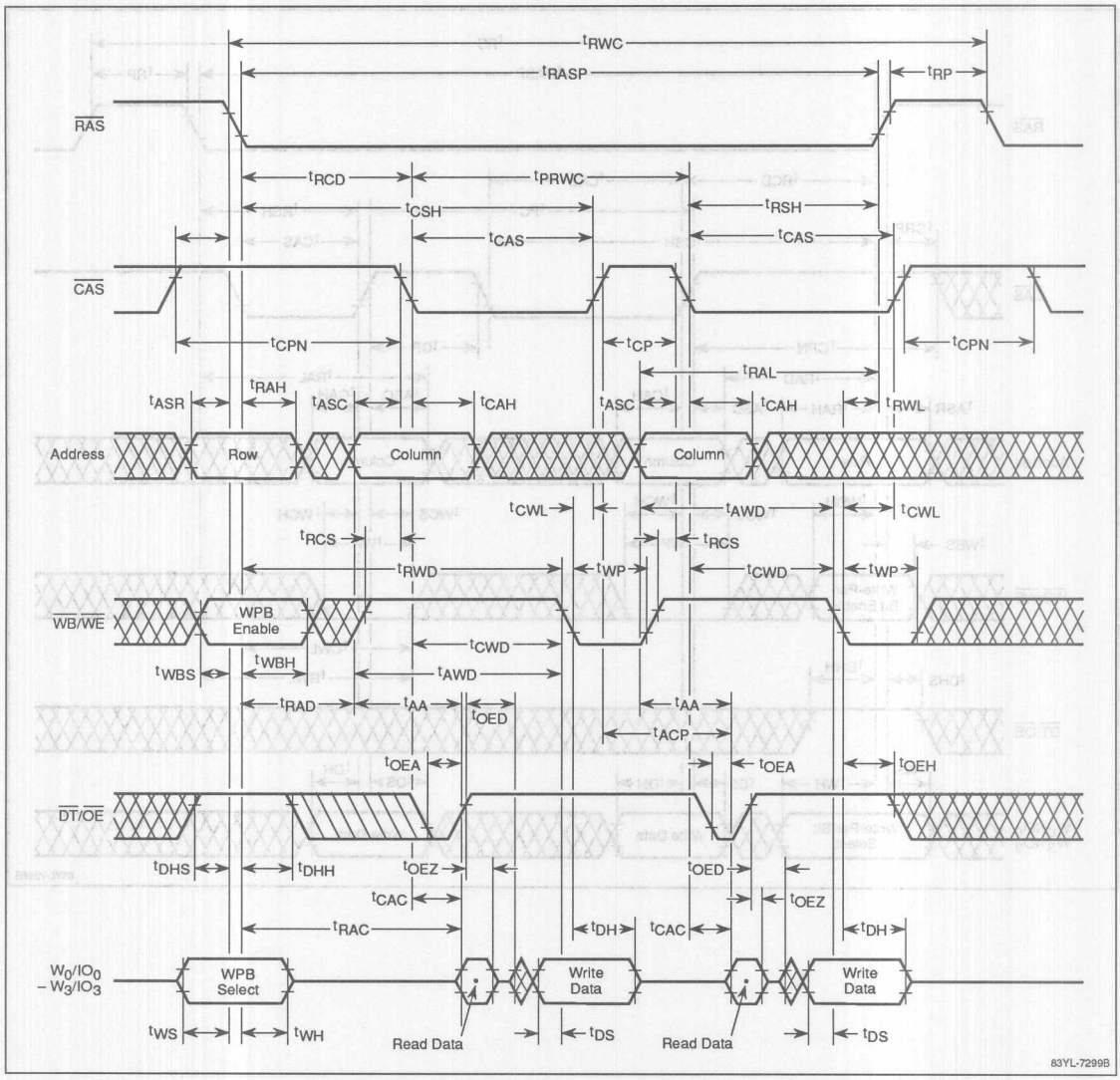
Timing Waveforms (cont)

Fast-Page Write Cycle



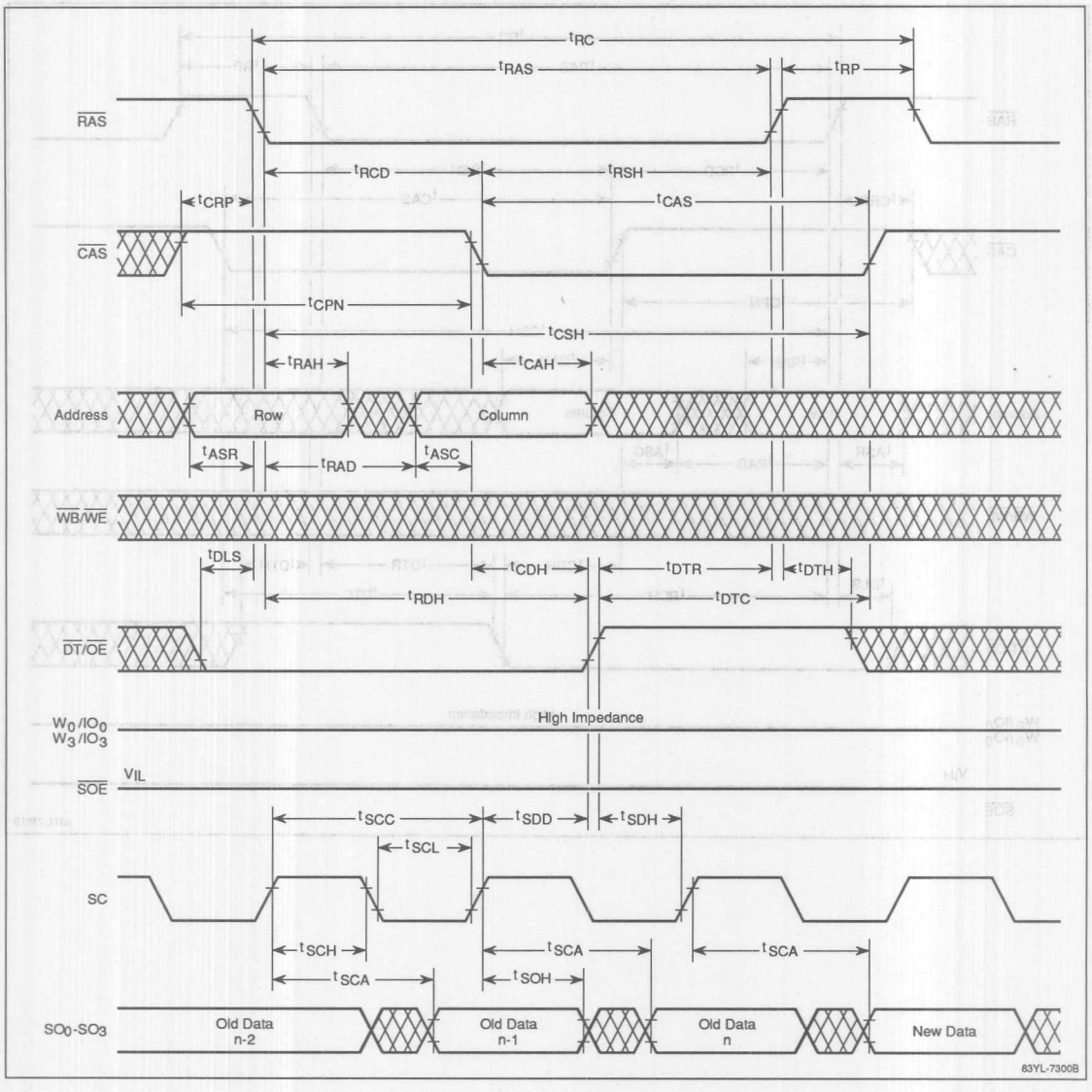
Timing Waveforms (cont)

Fast-Page Read-Modify-Write Cycle



Timing Waveforms (cont)

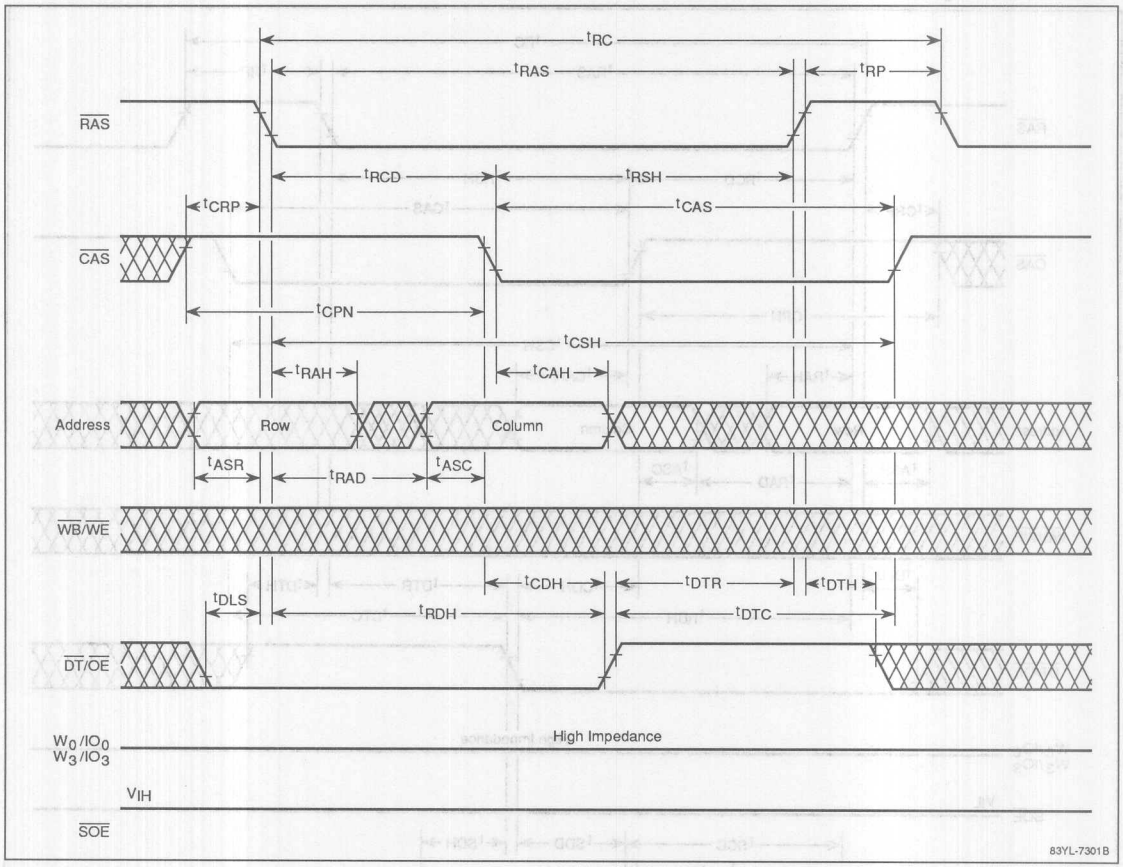
Data Transfer Cycle with Serial Port Active



3

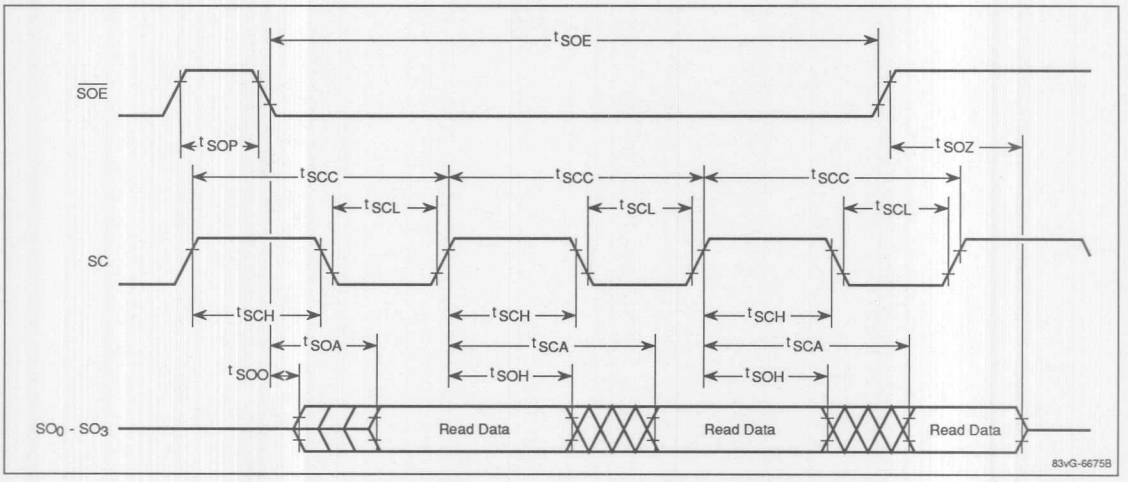
Timing Waveforms (cont)

Data Transfer Cycle with Serial Port in Standby

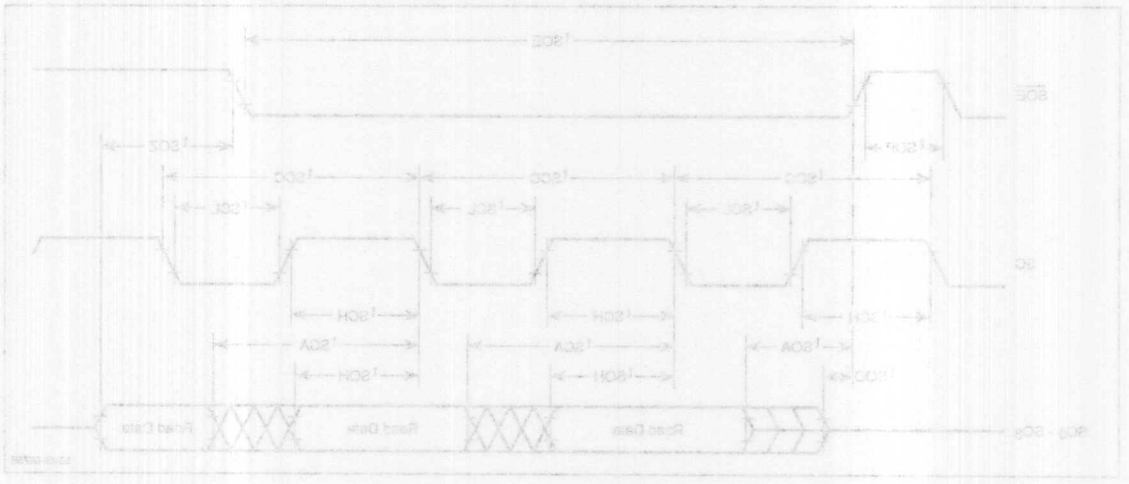


Timing Waveforms (cont)

Serial Read Cycle



3



μPD42274
Dual-Port Graphics Buffer

Description

The μPD42274 is a dual-port graphics buffer equipped with a 256K x 4-bit random access port and a 512 x 4-bit serial read port. The serial read port is connected to an internal 2048-bit data register through a 512 x 4-bit serial read output circuit. The random access port is used by the host CPU to read or write data addressed in any desired order. A write-per-bit capability allows each of the four data bits to be individually selected or masked for a write cycle. Furthermore, a flash write option with write-per-bit control enables data in the color register to be written to a selected row in the random access port.

The μPD42274 features fully asynchronous dual access, except when transferring stored graphics data from a selected row of the storage array to the data register. During a data transfer, the random access port requires a special timing cycle using a transfer clock; the serial read port continues to operate normally. Following the clock transition of a data transfer, serial output data changes from an old line to a new line and the starting location on the new line is addressable in the data transfer cycle.

An advanced CMOS silicon-gate process using polycide technology and trench capacitors provides high storage cell density, high performance, and high reliability.

Refreshing is accomplished by means of $\overline{RAS}$-only refresh cycles or by normal read or write cycles on the 512 address combinations of A_0 through A_8 during an 8-ms period. Automatic internal refreshing, by means of either hidden refreshing or the $\overline{CAS}$ before $\overline{RAS}$ timing and on-chip internal refresh circuitry, is also available. The transfer of a row of data from the storage array to the data register also refreshes that row automatically.

All inputs and outputs, including clocks, are TTL-compatible. All address and data-in signals are latched on-chip to simplify system design. Data-out is unlatched to allow greater system flexibility.

The μPD42274 is available in a 28-pin plastic ZIP or 28-pin plastic SOJ and is guaranteed for operation at 0 to + 70°C.

Features

- Three functional blocks
  - 256K x 4-bit random access storage array
  - 2048-bit data register
  - 512 x 4-bit serial read output circuit
- Two data ports: random access and serial read
- Dual-port accessibility except during data transfer
- Addressable start of serial read operation
- Real-time data transfer
- Single + 5-volt ±10% power supply
- On-chip substrate bias generator
- Random access port
  - Two main clocks: $\overline{RAS}$ and $\overline{CAS}$
  - Multiplexed address inputs
  - Direct connection of I/O and address lines allowed by $\overline{OE}$ to simplify system design
  - 512 refresh cycles every 8 ms
  - Read, early write, late write, read-write/read-modify-write, $\overline{RAS}$-only refresh, and fast-page cycles
  - Automatic internal refreshing by means of the $\overline{CAS}$ before $\overline{RAS}$ on-chip address counter
  - $\overline{CAS}$-controlled hidden refreshing
  - Write-per-bit option regarding four I/O bits
  - Write bit selection multiplexed on IO_0-IO_3
- Flash write option with write-per-bit control
- $\overline{RAS}$-activated data transfer
  - Same cycle time as for random access
  - Row data transferred to data register as specified by row address inputs
  - Starting location of following serial read cycle specified by column address inputs
  - Transfer of 2048 bits of data on one row to the data register, and the starting location of the serial read circuit, activated by a low-to-high transition of $\overline{DT}$
  - Data transfer during real-time operation or standby of serial port
- Fast serial read operation by means of SC pins
- Serial data output on SO_0-SO_3
- Direct connection of multiple serial outputs for extension of data length
- Fully TTL-compatible inputs, outputs, and clocks
- Three-state outputs for random and serial access
- CMOS silicon-gate process with trench capacitors

New speed of 80 ns will be available in 1991.

Ordering Information

Part Number	Row Access Time (max)	Serial Access Time (max)	Package
μPD42274LE-10	100 ns	30 ns	28-pin plastic SOJ
LE-12	120 ns	40 ns	
μPD42274V-10	100 ns	30 ns	28-pin plastic ZIP
V-12	120 ns	40 ns	

Pin Identification

Symbol	Function
A_0 - A_8	Address inputs
W_0/IO_0 - W_3/IO_3	Write-per-bit selects/data inputs and outputs
$\overline{RAS}$	Row address strobe
$\overline{CAS}$	Column address strobe
$\overline{WB/WE}$	Write-per-bit/write enable
$\overline{DT/OE}$	Data transfer/output enable
FWE	Flash write enable
SO_0 - SO_3	Serial read outputs
SC	Serial control
$\overline{SOE}$	Serial output enable
GND	Ground
V_{CC}	+5-volt ±10% power supply
NC	No connection

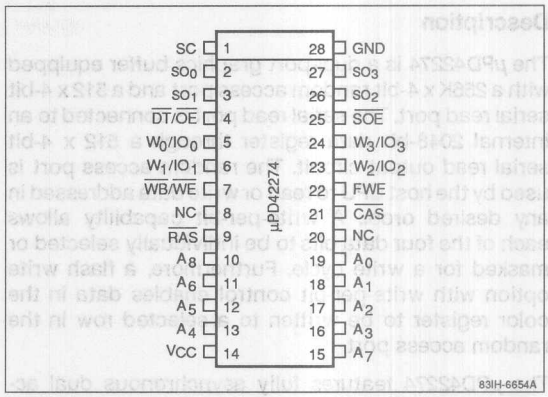
Absolute Maximum Ratings

Voltage on any pin except V_{CC} relative to GND, V_{R1}	−1.0 to +7.0 V
Voltage on V_{CC} relative to GND, V_{R2}	−1.0 to +7.0 V
Operating temperature, T_{OPR}	0 to +70°C
Storage temperature, T_{STG}	−55 to +125°C
Short-circuit output current, I_{OS}	50 mA
Power dissipation, P_D	1.5 W

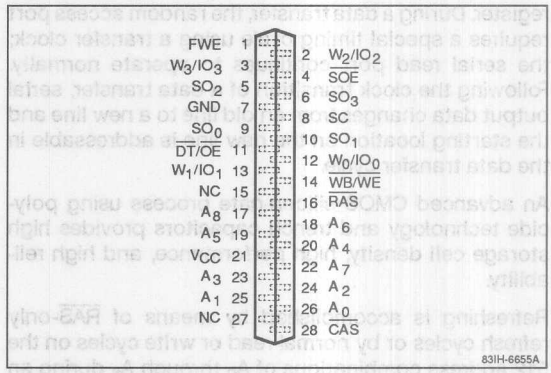
Exposure to Absolute Maximum Ratings for extended periods may affect device reliability; exceeding the ratings could cause permanent damage. The device should be operated within the limits specified under DC and AC Characteristics.

Pin Configurations

28-Pin Plastic SOJ



28-Pin Plastic ZIP



Pin Functions

A_0-A_8 (Address Inputs). These pins are multiplexed as row and column address inputs. Each of four data bits in the random access port corresponds to 262,144 storage cells, which means that nine row addresses and nine column addresses are required to decode one cell location. Nine row addresses are first used to select one of the 512 possible rows for a read, write, data transfer, or refresh cycle. Nine column addresses are then used to select the one of 512 possible column decoders for a read or write cycle or the one of 512 possible starting locations for the next serial read cycle. (Column addresses are not required in $\overline{RAS}$-only refresh or flash write cycles.)

W_0/IO_0-W_3/IO_3 (Write-Per-Bit Inputs/Common Data Inputs and Outputs). Each of the four data bits can be individually latched by these inputs at the falling edge of $\overline{RAS}$ in a write or flash write cycle, and then updated at the next falling edge of $\overline{RAS}$.

In a read cycle, these pins serve as outputs for the selected storage cells. In a write cycle, data input on these pins is latched by the falling edge of $\overline{CAS}$ or $\overline{WE}$.

$\overline{RAS}$ (Row Address Strobe). This pin is functionally equivalent to a chip enable signal in that whenever it is activated, the 2,048 storage cells of a selected row are sensed simultaneously and the sense amplifiers restore all data. The nine row address bits are latched by this signal and must be stable on or before its falling edge. $\overline{CAS}$, $\overline{DT/OE}$, $\overline{WB/WE}$, and FWE are simultaneously latched to determine device operation.

$\overline{CAS}$ (Column Address Strobe). This pin serves as a chip selection signal to activate the column decoder and the input/output buffers. The nine column address bits are latched at the falling edge of $\overline{CAS}$.

$\overline{WB/WE}$ (Write-Per-Bit Control/Write Enable). At the falling edge of $\overline{RAS}$, the $\overline{WB/WE}$ and FWE inputs must be low and $\overline{CAS}$ and $\overline{DT/OE}$ high to enable the write- per-bit option. When $\overline{CAS}$, $\overline{DT/OE}$ and FWE are high at the falling edge of $\overline{RAS}$, the level of this signal indicates either a color register set cycle or flash write cycle. A high $\overline{WB/WE}$ can be used at the beginning of a standard write or read cycle.

$\overline{DT/OE}$ (Data Transfer/Output Enable). At the falling edge of $\overline{RAS}$, $\overline{CAS}$ high and FWE and $\overline{DT/OE}$ low initiate a data transfer, regardless of the level of $\overline{WB/WE}$. $\overline{DT/OE}$ high initiates conventional read or write cycles and controls the output buffer in the random access port.

FWE (Flash Write Enable). If this signal is low and $\overline{CAS}$ and $\overline{DT/OE}$ are high at the falling edge of $\overline{RAS}$, a read or write cycle is initiated. If FWE, $\overline{CAS}$ and $\overline{DT/OE}$ are high at the falling edge of $\overline{RAS}$, either a color register set cycle or flash write cycle is initiated, depending on the level of $\overline{WB/WE}$.

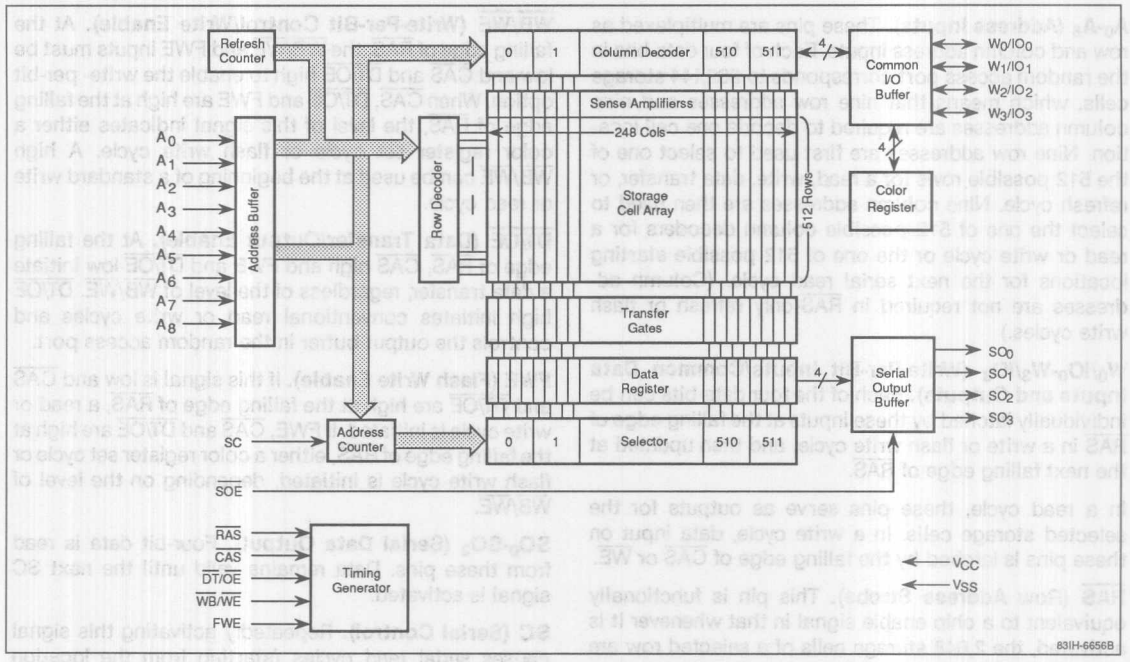
SO_0-SO_3 (Serial Data Output). Four-bit data is read from these pins. Data remains valid until the next SC signal is activated.

SC (Serial Control). Repeatedly activating this signal causes serial read cycles (starting from the location specified in the data transfer cycle) to be executed within the 2,048 bits in the data register. The rising edge of SC activates serial read operation, in which four of the 2,048 data bits are transferred to four serial data buses, respectively, and read out. Whenever SC is low, the serial port is in standby.

$\overline{SOE}$ (Serial Output Enable). This signal controls the serial data output buffer.

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Block Diagram



OPERATION

The μPD42274 consists of a random access port and a serial read port. The random access port executes standard read and write cycles as well as data transfer and flash write cycles, all of which are based on conventional $\overline{RAS}$/$\overline{CAS}$ timing.

In a data transfer, data in each storage cell on the selected row is transferred simultaneously through a transfer gate to its corresponding register location (unless the flash write option is used to write an entire row of data to predetermined values). The serial read port shows the contents of the data register in serial order. The random access and serial read ports can operate asynchronously, except when the transfer gate is turned on during the data transfer period.

Addressing

The storage array is arranged in a 512-row by 2048-column matrix, whereby each of 4 data bits in the random access port corresponds to 262,144 storage cells and 18 address bits are required to decode one cell location. Nine row address bits are set up on pins A_0 through A_8 and latched onto the chip by $\overline{RAS}$. Nine column address bits then are set up on pins A_0 through A_8 and latched onto the chip by $\overline{CAS}$. All addresses must be stable, on or before the falling edges of $\overline{RAS}$ and $\overline{CAS}$. Whenever $\overline{RAS}$ is activated, 2048 cells on the selected row are sensed simultaneously and the sense amplifiers automatically restore the data. $\overline{CAS}$ serves as a chip selection signal to activate the column decoder and the input and output buffers.

Through 1 of 512 column decoders, 4 storage cells on the row are connected to 4 data buses, respectively. In a data transfer cycle, 9 row address bits are used to select 1 of the 512 possible rows involved in the transfer of data to the data register. Nine column address bits are then used to select the 1 of 512 possible serial decoders that corresponds to the starting location of the next serial read cycle. In the serial read port, when SC is activated, 4 data bits in the 2048-bit data register are transferred to 4 serial data buses and read out. Activating SC repeatedly causes serial read cycles (starting from the location specified in the data transfer cycle) to be executed within the 2048 bits in the data register.

Random Access Port

An operation in the random access port begins with a negative transition of $\overline{RAS}$. Both $\overline{RAS}$ and $\overline{CAS}$ have minimum pulse widths, as specified in the timing table, which must be maintained for proper device operation and data integrity. Once begun, a cycle must meet all specifications, including minimum cycle time. To reduce the number of pins, the following are multiplexed.

- $\overline{DT/OE}$
- $\overline{WB/WE}$
- W_i/IO_i (i = 0, 1, 2, 3)

The $\overline{OE}$, $\overline{WE}$ and IO_i functions represent standard operations, while $\overline{DT}$, $\overline{WB}$, and W_i are special inputs to be applied in the same way as row address inputs, with setup and hold times referenced to the negative transition of $\overline{RAS}$.

The level of $\overline{DT}$ determines whether a cycle is a random access operation or a data transfer operation. $\overline{WB}$ affects only write cycles and determines whether or not the write-per-bit capability is used. W_i defines data bits to be written with the write-per-bit option. In the following discussions, these multiplexed pins are designated as $\overline{DT}(/\overline{OE})$, for example, depending on the function being described.

To use the μPD42274 for random access, $\overline{DT}(/\overline{OE})$ must be high as $\overline{RAS}$ falls. Holding $\overline{DT}(/\overline{OE})$ high disconnects the 2048-bit register from the corresponding 2048-digit lines of the storage array. Conversely, to execute a data transfer, $\overline{DT}(/\overline{OE})$ must be low as $\overline{RAS}$ falls to open the 2048 transfer gates and transfer data from one of the rows to the register.

Truth Table for the Random Access Port

$\overline{CAS}$	$\overline{DT/OE}$	$\overline{WB/WE}$	FWE	Cycle
H	H	H	L	Read or write (Note 1)
H	H	L	L	Mask write (Note 2)
H	L	X	L	Read data transfer (Note 3)
H	L	H	H	
L	X	X	X	$\overline{CAS}$ before $\overline{RAS}$ refresh (Note 4)
H	H	H	H	Color register set (Note 5)
H	H	L	H	Flash write/write-per-bit (Note 6)

Notes:

(1) Initiates a normal read or write cycle and disables the write-per- bit capability.

(2) Enables the write-per-bit capability, where individual bits can be selected or masked for a write cycle. Four-bit masked data is latched at the falling edge of $\overline{RAS}$ and reset at the rising edge of $\overline{RAS}$.

(3) Initiates a read data transfer cycle.

(4) Initiates a $\overline{CAS}$ before $\overline{RAS}$ refresh cycle. As $\overline{RAS}$ falls, $\overline{WB/WE}$, $\overline{DT/OE}$ and FWE = don't care.

(5) Defines a color register set cycle, where data in the register can be accessed in a read or write cycle.

(6) Initiates a flash write cycle, where the storage cells on an entire selected row can be set with write-per-bit control to the same data stored in the color register. As $\overline{RAS}$ falls, $\overline{DT/OE}$ = don't care. To avoid un-intended flash write operation, the FWE pin should be grounded. If grounding the FWE pin is not possible, use the non-flash write version μPD42273.

(7) X = don't care.

Read Cycle. A read cycle is executed by activating $\overline{RAS}$, $\overline{CAS}$, and $\overline{OE}$ and by maintaining $(\overline{WB}/)\overline{WE}$ while $\overline{CAS}$ is active. The $(W_i/)IO_i$ pin (i = 0, 1, 2, 3) remains in high impedance until valid data appears at the output at access time. Device access time, t_{ACC}, will be the longest of the following four calculated intervals:

- t_{RAC}
- $\overline{RAS}$ to ±CAS delay (t_{RCD}) + t_{CAC}
- $\overline{RAS}$ to column address delay (t_{RAD}) + t_{AA}
- $\overline{RAS}$ to $\overline{OE}$ delay + t_{OEA}

Access times from $\overline{RAS}$ (t_{RAC}), from $\overline{CAS}$ (t_{CAC}), from the column addresses (t_{AA}), and from $\overline{OE}$ (t_{OEA}) are device parameters. The $\overline{RAS}$-to-$\overline{CAS}$, $\overline{RAS}$-to-column address, and $\overline{RAS}$-to-$\overline{OE}$ delays are system-dependent timing parameters. Output becomes valid after the access time has elapsed and it remains valid while both $\overline{CAS}$ and $\overline{OE}$ are low. Either $\overline{CAS}$ or $\overline{OE}$ high returns the output pins to high impedance.

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Write Cycle. A write cycle is executed by bringing (WB/)WE low during the RAS/CAS cycle. The falling edge of CAS or (WB/)WE strobes the data on (W_i/)IO_i into the on-chip data latch. To make use of the write-per-bit option, WB(/WE) must be low as RAS falls. In this case, write data bits can be specified by keeping W_i(/IO_i) high, with setup and hold times referenced to the negative transition of RAS.

For those data bits of W_i(/IO_i) that are kept low as RAS falls, write operation is inhibited on the chip. If WB(/WE) is high as RAS falls, the write-per-bit option is not used and a write cycle is executed for all four data bits.

Early Write Cycle. An early write cycle is executed by bringing (WB/)WE low before CAS falls. Data is strobed by CAS, with setup and hold times referenced to this signal, and the output remains in high impedance for the entire cycle. As RAS falls, (DT/)OE must meet the setup and hold times of a high DT, but otherwise (DT/)OE does not affect any circuit operation while CAS is active.

Read-Write/Read-Modify-Write Cycle. This cycle is executed by bringing (WB/)WE low with the RAS and CAS signals low. (W_i/)IO_i shows read data at access time. Afterward, in preparation for the upcoming write cycle, (W_i/)IO_i returns to high impedance when (DT/)OE goes high. The data to be written is strobed by (WB/)WE, with setup and hold times referenced to this signal.

Late Write Cycle. This cycle shows the timing flexibility of (DT/)OE, which can be activated just after (WB/)WE falls, even when (WB/)WE is brought low after CAS.

Refresh Cycle. A cycle at each of the 512 row addresses (A_0 through A_8) will refresh all storage cells. Any cycle executed in the random access port (i.e., read, write, refresh, data transfer, color register set, or flash write) refreshes the 2048 bits selected by the RAS addresses or by the on-chip refresh address counter.

RAS-Only Refresh Cycle. A cycle having only RAS active refreshes all cells in one row of the storage array. A high CAS is maintained while RAS is active to keep (W_i/)IO_i in high impedance. This method is preferred for refreshing, especially when the host system consists of multiple rows of random access devices. The data outputs may be OR-tied with no bus contention when RAS-only refresh cycles are executed.

CAS Before RAS Refresh Cycle. This cycle executes internal refreshing using the on-chip control circuitry. Whenever CAS is low as RAS falls, this circuitry automatically refreshes the row addresses specified by the internal counter. In this cycle, the circuit operation based on CAS is maintained in a reset state. When internal refreshing is complete, the address counter automatically increments in preparation for the next CAS before RAS cycle.

Hidden Refresh Cycle. This cycle is executed after a read cycle, without disturbing the read data output. Once valid, the data output is controlled by CAS and OE. After the read cycle, CAS is held low while RAS goes high for precharge. A RAS-only cycle is then executed (except that CAS is held at a low level instead of a high level) and the data output remains valid. Since hidden refreshing is the same as CAS before RAS refreshing, the data output remains valid during either operation.

Fast-Page Cycle. This feature allows faster data access by keeping the same row address while successive column addresses are strobed onto the chip. Maintaining RAS low while successive CAS cycles are executed causes data to be transferred at a faster rate because row addresses are maintained internally and do not have to be reapplied. In fast-page operation, read, write and read-write/read-modify-write cycles may be executed. Additionally, the write-per-bit control specified in the entry write cycle is maintained throughout the next fast-page write cycle.

During a fast-page read cycle, the (W_i/)IO_i data pin (i = 0, 1, 2, or 3) remains in a state of high impedance until valid data appears at the output pin at access time. Device access time in this cycle will be one of the following calculated intervals:

Fast-Page Access Time

Calculated Interval	Conditions
t_{ACP}	$t_{ASC} \geq t_{CP}$ and $t_{CP} \leq t_{CP}$ (max)
t_{AA}	$t_{ASC} \leq t_{ASC}$ (max) and $t_{CP} \geq t_{CP}$ (max)
	$t_{ASC} \leq t_{CP}$ and $t_{CP} \leq t_{CP}$ (max)
t_{CAC}	$t_{ASC} \geq t_{ASC}$ (max) and $t_{CP} \leq t_{CP}$ (max)

Data Transfer Cycle. A data transfer is executed by bringing $\overline{DT}(/\overline{OE})$ and FWE low as $\overline{RAS}$ falls. The specified 1 of the possible 512 rows involved in the data transfer, as well as the starting location of the following serial read cycle in the serial read port, are defined by address inputs. $\overline{DT}(/\overline{OE})$ must be low for a specified time, measured from $\overline{RAS}$ and $\overline{CAS}$, so that the data transfer condition may be satisfied. The low-to-high transition of $\overline{DT}$ causes two operations through the data transfer gates: column address buffer outputs are transferred to the serial address counters, and storage cell data amplified on digit lines is transferred to the data register. $\overline{RAS}$ and $\overline{CAS}$ must be low during these operations to keep the data in the random access port.

Color Register Set Cycle. A color register set cycle is executed in the same fashion as a conventional read or write cycle, with the level of $\overline{WE}$ high as $\overline{RAS}$ falls. In this cycle, read or write operation is available to the color register under the control of $\overline{WE}$. In read operation, color register data is read out on the common IO_i pins. In write operation, common IO_i data can be written into the color register. $\overline{RAS}$-only refreshing is internally performed on the row selected by A_0 through A_8 in this cycle.

Flash Write Cycle. A flash write cycle can clear or set each of the four 512-bit data sets on the one row selected from among the 512 possible rows according to data stored in the color register. Bit mask inputs are latched as $\overline{RAS}$ falls. This cycle is useful in graphics processing applications when the screen should be cleared or set to some uniform value as quickly as possible.

Serial Read Port

The serial read port is only used to serially read the contents of the data register starting from a specified location. The entire operation, therefore, follows the data transfer cycle. The only condition under which the serial read port must synchronize with the random access port is when the positive transition of $\overline{DT}(/\overline{OE})$ must occur within a specified period in an SC cycle. Except for this cycle, the serial read port can operate asynchronously. The output data appears at SO_i after an access time of t_{SCA}, measured from SC high, only when $\overline{SOE}$ is maintained low. The SC cycle which includes the positive transition of $\overline{DT}(/\overline{OE})$ shows old data in the data register; subsequent SC cycles show new data transferred to the data register serially and in a looped manner. The serial output is maintained until the next SC signal is activated. $\overline{SOE}$ controls the impedance of the serial output to allow multiplexing of more than one bank of μPD42274 graphics buffers into the same external circuitry. When $\overline{SOE}$ is at a low logic level, SO_i is enabled and the proper data is read. When $\overline{SOE}$ is at a high logic level, SO_i is disabled and in a state of high impedance.

3

Recommended Operating Conditions

Parameter	Symbol	Min	Typ	Max	Unit
Supply voltage	V_{CC}	4.5	5.0	5.5	V
Input voltage, high	V_{IH}	2.4		5.5	V
Input voltage, low	V_{IL}	−1.0		0.8	V
Ambient temperature	T_A	0		70	°C

Capacitance

T_A = 0 to +70 °C; V_{CC} = +5.0 V ±10%; f = 1 MHz; GND = 0 V

Parameter	Symbol	Limit (max)	Unit	Pins Under Test
Input capacitance	$C_{I(A)}$	5	pF	A_0 through A_8
	$C_{I(\overline{DT}/\overline{OE})}$	8	pF	$\overline{DT}/\overline{OE}$
	$C_{I(\overline{WB}/\overline{WE})}$	8	pF	$\overline{WB}/\overline{WE}$
	$C_{I(FWE)}$	8	pF	FWE
	$C_{I(\overline{RAS})}$	8	pF	$\overline{RAS}$
	$C_{I(\overline{CAS})}$	8	pF	$\overline{CAS}$
	$C_{I(\overline{SOE})}$	8	pF	$\overline{SOE}$
	$C_{I(SC)}$	8	pF	SC
Input/output capacitance	$C_{IO(W/IO)}$	7	pF	W_0/IO_0 through W_3/IO_3
Output capacitance	$C_{O(SO)}$	7	pF	SO_0 through SO_3

Power Supply Current

T_A = 0 to +70°C; V_{CC} = +5.0 V ±10%; GND = 0 V

Port Operation						
Random Access	Serial Read	Parameter	μPD42274-10 (max)	μPD42274-12 (max)	Unit	Test Conditions
Read/write cycle	Standby	I_{CC1}	95	85	mA	$\overline{RAS}$, $\overline{CAS}$ cycling; FWE low as $\overline{RAS}$ falls; $t_{RC} = t_{RC}$ min; $\overline{SOE} = V_{IH}$; SC = V_{IH} or V_{IL}
Standby	Standby	I_{CC2}	4	4	mA	$\overline{CAS} = \overline{RAS} = V_{IH}$; $\overline{SOE} = V_{IH}$; SC = V_{IH} or V_{IL}
$\overline{RAS}$-only refresh cycle	Standby	I_{CC3}	95	85	mA	$\overline{RAS}$ cycling; $\overline{CAS} = V_{IH}$; FWE low as $\overline{RAS}$ falls; $t_{RC} = t_{RC}$ min; $\overline{SOE} = V_{IH}$; SC = V_{IH} or V_{IL} (Note 2)
Fast-page cycle	Standby	I_{CC4}	90	80	mA	$\overline{RAS} = V_{IL}$; $\overline{CAS}$ cycling; $t_{PC} = t_{PC}$ min ; $\overline{SOE} = V_{IH}$; SC = V_{IH} or V_{IL} (Note 3)
$\overline{CAS}$ before $\overline{RAS}$ refresh cycle	Standby	I_{CC5}	95	85	mA	$\overline{CAS}$ low as $\overline{RAS}$ falls; $t_{RC} = t_{RC}$ min; $\overline{SOE} = V_{IH}$; SC = V_{IH} or V_{IL}
Data transfer cycle	Standby	I_{CC6}	135	120	mA	$\overline{DT}$ low as $\overline{RAS}$ falls; $t_{RC} = t_{RC}$ min; $\overline{SOE} = V_{IH}$; SC = V_{IH} or V_{IL}
Read/write cycle	Active	I_{CC7}	120	105	mA	$\overline{RAS}$ and $\overline{CAS}$ cycling; FWE low as $\overline{RAS}$ falls; $t_{RC} = t_{RC}$ min $\overline{SOE} = V_{IL}$; SC cycling; $t_{SCC} = t_{SCC}$ min
Standby	Active	I_{CC8}	30	25	mA	$\overline{CAS} = \overline{RAS} = V_{IH}$; $\overline{SOE} = V_{IL}$; SC cycling; $t_{SCC} = t_{SCC}$ min
$\overline{RAS}$-only refresh cycle	Active	I_{CC9}	120	105	mA	$\overline{RAS}$ cycling; $\overline{CAS} = V_{IH}$; FWE low as $\overline{RAS}$ falls; $t_{RC} = t_{RC}$ min; $\overline{SOE} = V_{IL}$; SC cycling; $t_{SCC} = t_{SCC}$ min
Fast-page cycle	Active	I_{CC10}	115	100	mA	$\overline{RAS} = V_{IL}$; $\overline{CAS}$ cycling; $t_{PC} = t_{PC}$ min ; $\overline{SOE} = V_{IL}$; SC cycling; $t_{SCC} = t_{SCC}$ min (Note 3)
$\overline{CAS}$ before $\overline{RAS}$ refresh cycle	Active	I_{CC11}	120	105	mA	$\overline{CAS}$ low as $\overline{RAS}$ falls; $t_{RC} = t_{RC}$ min; $\overline{SOE} = V_{IL}$; SC cycling; $t_{SCC} = t_{SCC}$ min
Data transfer cycle	Active	I_{CC12}	160	140	mA	$\overline{DT}$ low as $\overline{RAS}$ falls; $t_{RC} = t_{RC}$ min; $\overline{SOE} = V_{IL}$; SC cycling; $t_{SCC} = t_{SCC}$ min
Color register set cycle	Standby	I_{CC13}	95	85	mA	FWE and $\overline{WB/WE}$ high as $\overline{RAS}$ falls; $t_{RC} = t_{RC}$ min; $\overline{SOE} = V_{IH}$; SC = V_{IH} or V_{IL}
Flash write cycle	Standby	I_{CC14}	95	85	mA	FWE high and $\overline{WB/WE}$ low as $\overline{RAS}$ falls; $t_{RC} = t_{RC}$ min; $\overline{SOE} = V_{IH}$; SC = V_{IH} or V_{IL}
Color register set cycle	Active	I_{CC15}	120	105	mA	FWE and $\overline{WB/WE}$ high as $\overline{RAS}$ falls; $t_{RC} = t_{RC}$ min; $\overline{SOE} = V_{IL}$; SC cycling; $t_{SCC} = t_{SCC}$ min
Flash write cycle	Active	I_{CC16}	120	105	mA	FWE high and $\overline{WB/WE}$ low as $\overline{RAS}$ falls; $t_{RC} = t_{RC}$ min; $\overline{SOE} = V_{IL}$; SC cycling; $t_{SCC} = t_{SCC}$ min

Notes:

(1) No load on IO_i or SO_i. Except for I_{CC2}, I_{CC3}, I_{CC6}, and I_{CC14}, real values depend on output loading in addition to cycle rates.

(2) $\overline{CAS}$ is not clocked, but is kept at a stable high level. The column addresses are also assumed to be kept stable, at either a high or low level.

(3) A change in column addresses must not occur more than once in a fast-page cycle.

DC Characteristics

T_A = 0 to +70°C; V_{CC} = +5.0 V ±10%; GND = 0 V

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions
Input leakage current	I_{IL}	−10		10	μA	V_{IN} = 0 to 5.5 V; all other pins not under test = 0 V
Output leakage current	I_{OL}	−10		10	μA	D_{OUT} (IO_i, SO_i) disabled; V_{OUT} = 0 to 5.5 V
Random access port output voltage, high	$V_{OH(R)}$	2.4			V	$I_{OH(R)}$ = −2 mA
Random access port output voltage, low	$V_{OL(R)}$			0.4	V	$I_{OL(R)}$ = 4.2 mA
Serial read port output voltage, high	$V_{OH(S)}$	2.4			V	$I_{OH(S)}$ = −1 mA
Serial read port output voltage, low	$V_{OL(S)}$			0.4	V	$I_{OL(S)}$ = 2.1 mA

AC Characteristics

T_A = 0 to +70°C; V_{CC} = +5.0 V ±10%; GND = 0 V

		μPD42274-10		μPD42274-12			
Parameter	Symbol	Min	Max	Min	Max	Unit	Test Conditions
Switching Characteristics							
Access time from $\overline{RAS}$	t_{RAC}		100		120	ns	(Notes 3, 4 and 12)
Access time from falling edge of $\overline{CAS}$	t_{CAC}		25		30	ns	(Notes 3, 4, 13, 14 and 15)
Access time from column address	t_{AA}		55		65	ns	(Notes 3, 4, 14 and 15)
Access time from rising edge of $\overline{CAS}$	t_{ACP}		55		65	ns	(Notes 3 and 4)
Access time from $\overline{OE}$	t_{OEA}		25		30	ns	(Notes 3 and 4)
Serial output access time from SC	t_{SCA}		30		40	ns	(Notes 3 and 18)
Serial output access time from $\overline{SOE}$	t_{SOA}		25		30	ns	(Note 3)
Output disable time from $\overline{CAS}$ high	t_{OFF}	0	25	0	30	ns	(Note 5)
Output disable time from $\overline{OE}$ high	t_{OEZ}	0	25	0	30	ns	(Note 5)
Serial output disable time from $\overline{SOE}$ high	t_{SOZ}	0	15	0	20	ns	(Note 5)
$\overline{SOE}$ low to serial output setup delay	t_{SOO}	5		5		ns	
Serial output hold time after SC high	t_{SOH}	5		5		ns	
Timing Requirements							
Random read or write cycle time	t_{RC}	190		220		ns	(Note 11)
Read-write/read-modify-write cycle time	t_{RWC}	255		295		ns	(Note 11)
Fast-page cycle time	t_{PC}	60		70		ns	(Note 11)
Fast-page read-write/read-modify-write cycle time	t_{PRWC}	125		145		ns	(Note 11)
Rise and fall transition time	t_T	3	50	3	50	ns	(Notes 3, 10 and 18)
$\overline{RAS}$ precharge time	t_{RP}	80		90		ns	(Note 18)
$\overline{RAS}$ pulse width	t_{RAS}	100	10,000	120	10,000	ns	
Fast-page $\overline{RAS}$ pulse width	t_{RASP}	100	100,000	120	100,000	ns	
$\overline{RAS}$ hold time	t_{RSH}	25		30		ns	
$\overline{CAS}$ precharge time (nonpage cycle)	t_{CPN}	10		15		ns	
Fast-page $\overline{CAS}$ precharge time	t_{CP}	10	25	15	30	ns	
$\overline{CAS}$ pulse width	t_{CAS}	25	10,000	30	10,000	ns	
$\overline{CAS}$ hold time	t_{CSH}	100		120		ns	
$\overline{RAS}$ to $\overline{CAS}$ delay	t_{RCD}	25	75	25	90	ns	(Note 4)
$\overline{CAS}$ high to $\overline{RAS}$ low precharge time	t_{CRP}	10		10		ns	(Note 16)

AC Characteristics (cont)

Parameter	Symbol	μPD42274-10 Min	μPD42274-10 Max	μPD42274-12 Min	μPD42274-12 Max	Unit	Test Conditions
Timing Requirements (cont)							
Row address setup time	t_{ASR}	0		0		ns	
Row address hold time	t_{RAH}	12		15		ns	
Column address setup time	t_{ASC}	0	25	0	30	ns	(Note 15)
Column address hold time	t_{CAH}	15		20		ns	
$\overline{RAS}$ to column address delay time	t_{RAD}	17	45	20	55	ns	(Notes 9 and 14)
Column address to $\overline{RAS}$ lead time	t_{RAL}	55		65		ns	
Read command setup time	t_{RCS}	0		0		ns	
Read command hold time after $\overline{RAS}$ high	t_{RRH}	10		10		ns	(Note 6)
Read command hold time after $\overline{CAS}$ high	t_{RCH}	0		0		ns	(Note 6)
Write command setup time	t_{WCS}	0		0		ns	(Note 7)
Write command hold time	t_{WCH}	20		30		ns	
Write command pulse width	t_{WP}	20		25		ns	(Note 17)
Write command to $\overline{RAS}$ lead time	t_{RWL}	30		35		ns	
Write command to $\overline{CAS}$ lead time	t_{CWL}	30		35		ns	
Data-in setup time	t_{DS}	0		0		ns	(Note 8)
Data-in hold time	t_{DH}	20		25		ns	(Note 8)
Column address to $\overline{WE}$ delay	t_{AWD}	85		100		ns	(Note 7)
$\overline{CAS}$ to $\overline{WE}$ delay	t_{CWD}	55		65		ns	(Note 7)
$\overline{RAS}$ to $\overline{WE}$ delay	t_{RWD}	130		155		ns	(Note 7)
$\overline{OE}$ high to data-in setup delay	t_{OED}	30		35		ns	
$\overline{OE}$ high hold time after $\overline{WE}$ low	t_{OEH}	25		30		ns	
$\overline{CAS}$ before $\overline{RAS}$ refresh setup time	t_{CSR}	0		0		ns	
$\overline{CAS}$ before $\overline{RAS}$ refresh hold time	t_{CHR}	15		20		ns	
$\overline{RAS}$ high to $\overline{CAS}$ low precharge time	t_{RPC}	0		0		ns	
Refresh interval	t_{REF}		8		8	ms	Addresses A_0 through A_8
$\overline{DT}$ low setup time	t_{DLS}	0		0		ns	
$\overline{DT}$ low hold time after $\overline{RAS}$ low	t_{RDH}	80		90		ns	(Note 18)
$\overline{DT}$ low hold time after $\overline{CAS}$ low	t_{CDH}	30		35		ns	
SC high to $\overline{DT}$ high delay	t_{SDD}	10		15		ns	
SC low hold time after $\overline{DT}$ high	t_{SDH}	10		15		ns	
Serial clock cycle time	t_{SCC}	30		40		ns	(Note 11)
SC pulse width	t_{SCH}	10		15		ns	
SC precharge time	t_{SCL}	10		15		ns	
$\overline{DT}$ high setup time	t_{DHS}	0		0		ns	
$\overline{DT}$ high hold time	t_{DHH}	15		20		ns	
$\overline{DT}$ high to $\overline{RAS}$ high delay	t_{DTR}	10		10		ns	
$\overline{DT}$ high to $\overline{CAS}$ high delay	t_{DTC}	5		5		ns	
$\overline{OE}$ to $\overline{RAS}$ inactive setup time	t_{OES}	10		10		ns	
Write-per-bit setup time	t_{WBS}	0		0		ns	

AC Characteristics (cont)

Parameter	Symbol	μPD42274-10 Min	μPD42274-10 Max	μPD42274-12 Min	μPD42274-12 Max	Unit	Test Conditions
Timing Requirements (cont)							
Write-per-bit hold time	t_{WBH}	15		20		ns	
Flash write enable setup time	t_{FWS}	0		0		ns	
Flash write enable hold time	t_{FWH}	15		20		ns	
Write bit selection setup time	t_{WS}	0		0		ns	
Write bit selection hold time	t_{WH}	15		20		ns	
$\overline{SOE}$ pulse width	t_{SOE}	10		15		ns	
$\overline{SOE}$ precharge time	t_{SOP}	10		15		ns	
$\overline{DT}$ high hold time after $\overline{RAS}$ high	t_{DTH}	15		20		ns	

Notes:

(1) All voltages are referenced to GND.

(2) An initial pause of 100 μs is required after power-up, followed by any eight $\overline{RAS}$ cycles and four data transfer (DT) cycles, before proper device operation is achieved.

(3) See input/output timing waveforms for timing reference voltages. See figures 3 and 4 for output loads.

(4) Operation within the t_{RCD} (max) limit ensures that t_{RAC} (max) can be met. The t_{RCD} (max) limit is specified as a reference point only. If t_{RCD} is greater than the specified t_{RCD} (max) limit, access time is controlled exclusively by t_{CAC}, t_{OEA}, or t_{AA}.

(5) An output disable time defines the time at which the output achieves the open-circuit condition and is not referenced to output voltage levels.

(6) Either t_{RRH} or t_{RCH} must be satisfied for a read cycle.

(7) t_{WCS}, t_{AWD}, t_{CWD}, and t_{RWD} are restrictive operating parameter in read-write and read-modify-write cycles only. If $t_{WCS} \geq t_{WCS}$ (min), the cycle is an early write cycle and the data output will remain open-circuit throughout the entire cycle. If $t_{AWD} \geq t_{AWD}$ (min), $t_{CWD} \geq t_{CWD}$ (min), and $t_{RWD} \geq t_{RWD}$ (min), the cycle is a read-write cycle and the data output will contain data read from the selected cell. If neither of the above conditions is met, the condition of the data out (at access time and until $\overline{CAS}$ returns to V_{IH}) is indeterminate.

(8) These parameters are referenced to the falling edge of $\overline{CAS}$ in early write cycles and to the falling edge of (WB/)WE in delayed write or read-modify-write cycles.

(9) Assumes that t_{RAD} (min) = t_{RAH} (min) + typical t_T of 5 ns.

(10) V_{IH} (min) and V_{IL} (max) are reference levels for measuring the timing of input signals. Additionally, transition times are measured between V_{IH} and V_{IL}.

(11) The minimum specifications are used only to indicate the cycle time at which proper operation over the full temperature range (T_A = 0 to +70°C) is assured.

(12) Assumes that $t_{RCD} \leq t_{RCD}$ (max) and $t_{RAD} \leq t_{RAD}$ (max). If t_{RCD} or t_{RAD} is greater than the maximum recommended value in this table, t_{RAC} increases by the amount that t_{RCD} or t_{RAD} exceeds the value shown.

(13) Assumes that $t_{RCD} \geq t_{RCD}$ (max) and $t_{RAD} \leq t_{RAD}$ (max).

(14) If $t_{RAD} \geq t_{RAD}$ (max), then the access time is defined by t_{AA}.

(15) For fast-page read operation, the definition of access time is as follows.

$\overline{CAS}$ and Column Address Input Conditions	Access Time Definition
$t_{CP} \leq t_{CP}$ (max), $t_{ASC} \geq t_{CP}$	t_{ACP}
$t_{CP} \leq t_{CP}$ (max), $t_{ASC} \leq t_{CP}$	t_{AA}
$t_{CP} \geq t_{CP}$ (max), $t_{ASC} \leq t_{ASC}$ (max)	t_{AA}
$t_{CP} \geq t_{CP}$ (max), $t_{ASC} \geq t_{ASC}$ (max)	t_{CAC}

(16) The t_{CRP} requirement is applicable for $\overline{RAS}$/$\overline{CAS}$ cycles preceded by any cycle.

(17) Parameter t_{WP} is applicable for a delayed write cycle such as a read-write/read-modify-write cycle. For early write operation, both t_{WCS} and t_{WCH} must be met.

(18) Improvement in parameters t_{RDH}, t_{RP} and t_{SCA} are planned for process versions "x" and "m". Please contact your NEC sales office for details.

(19) Ac measurements assume t_T = 5 ns.

Figure 1. Input Timing

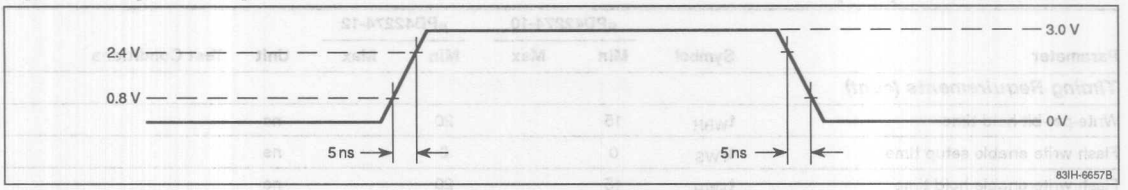


Figure 2. Output Timing

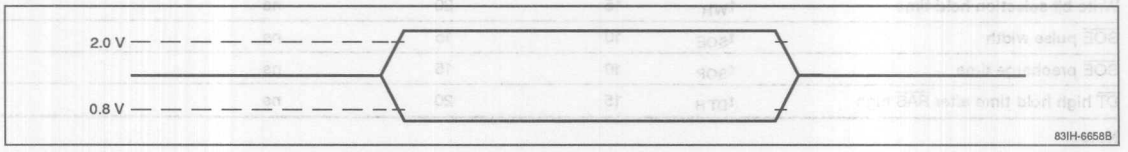


Figure 3. Output Load in Random Access Port

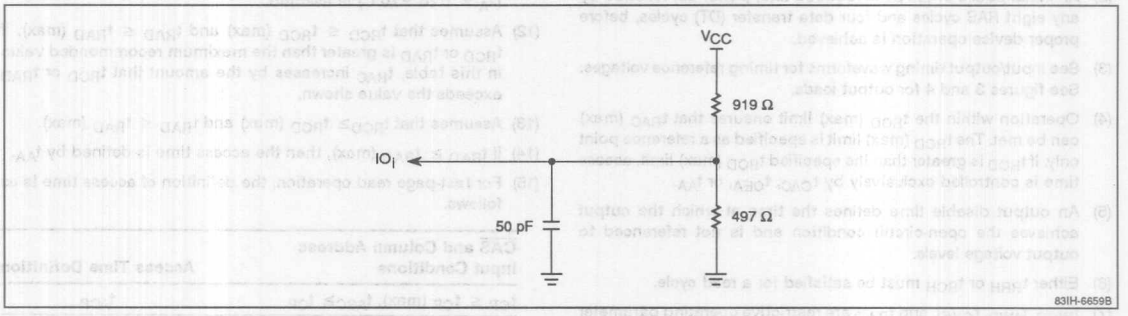
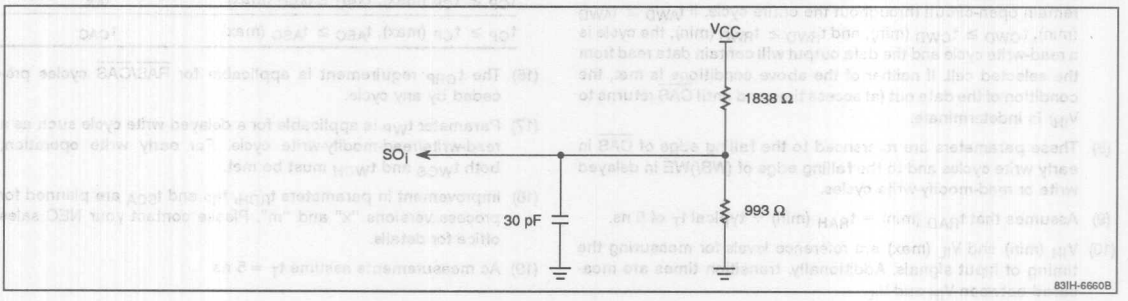
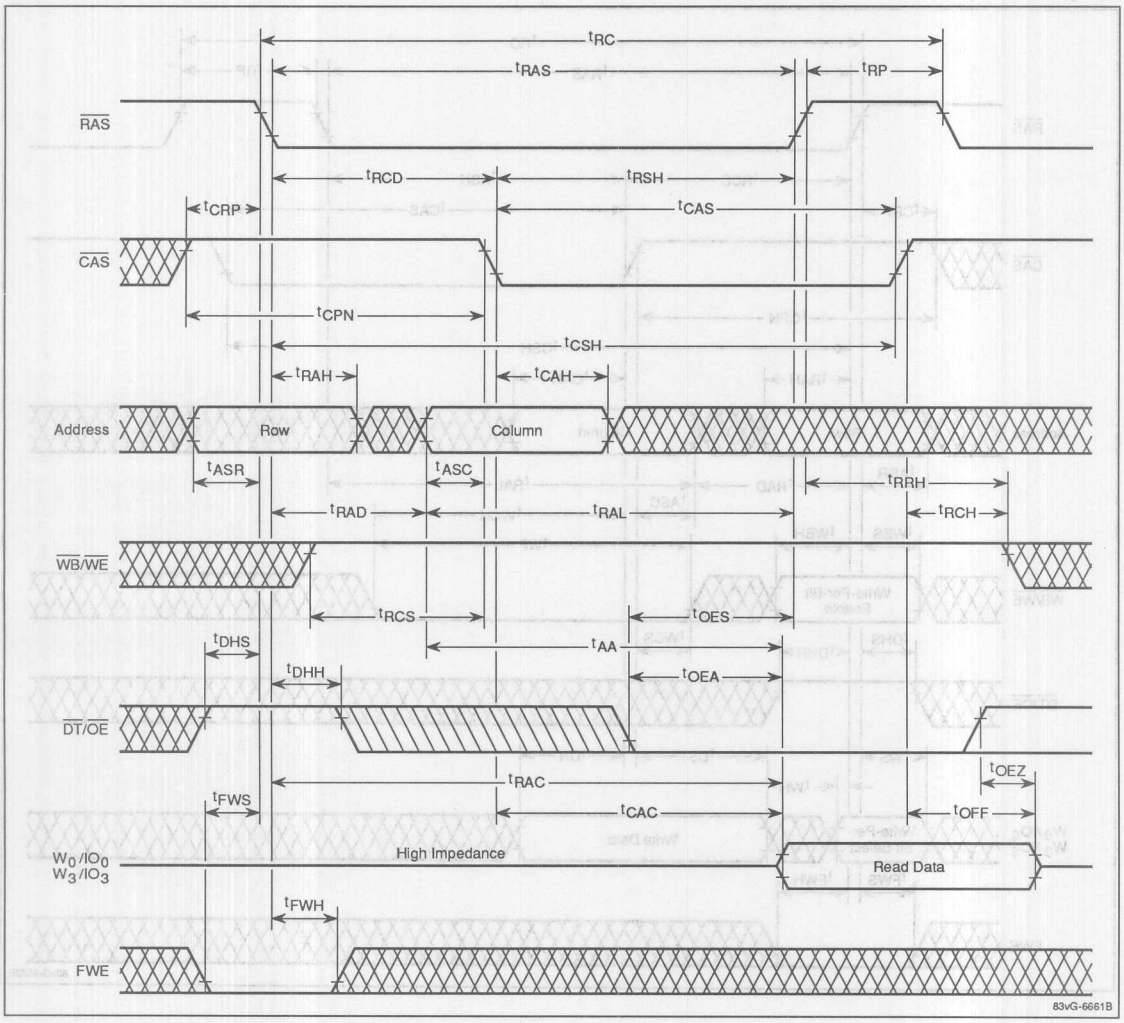


Figure 4. Output Load in Serial Read Port



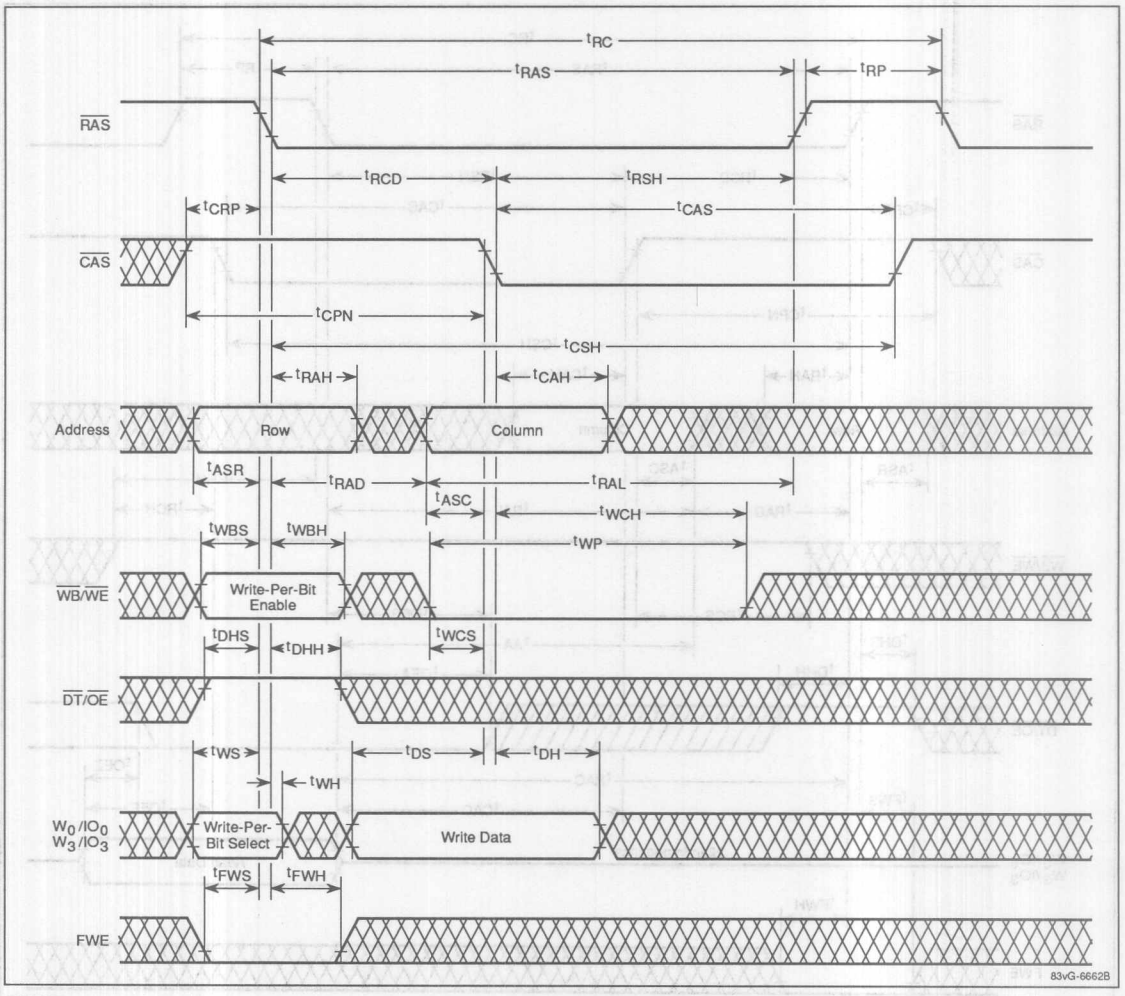
Timing Waveforms

Read Cycle



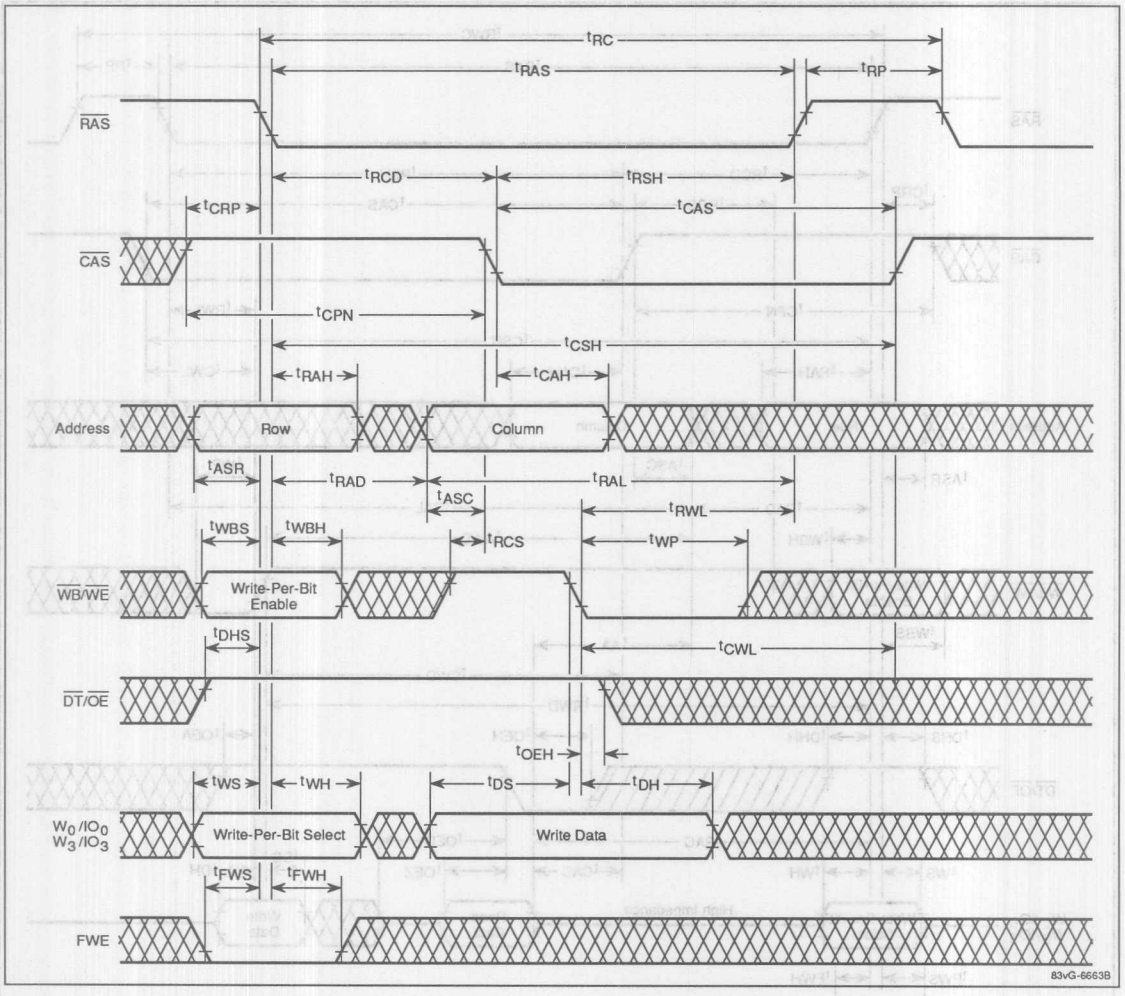
Timing Waveforms (cont)

Early Write Cycle



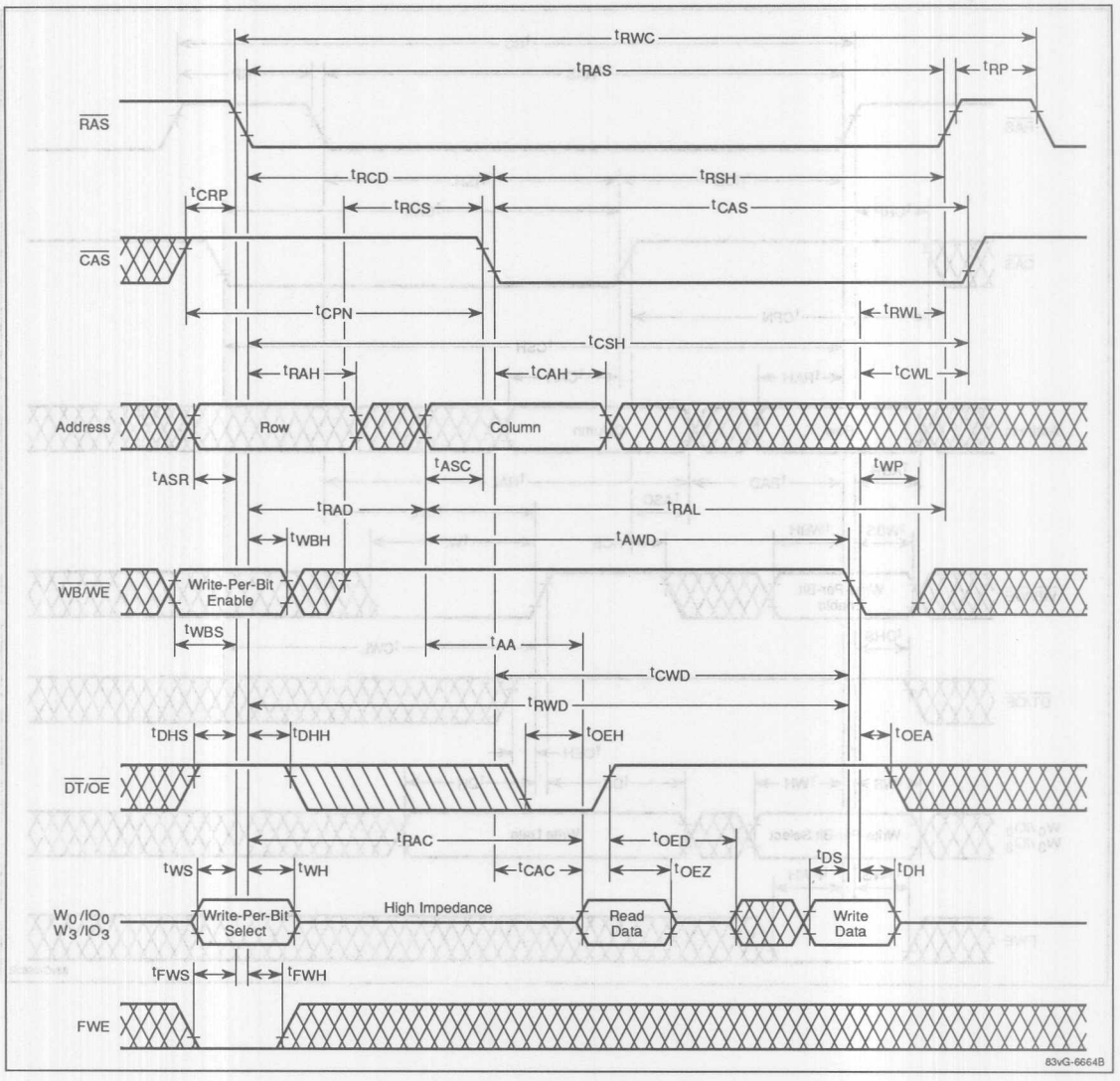
Timing Waveforms (cont)

Late Write Cycle



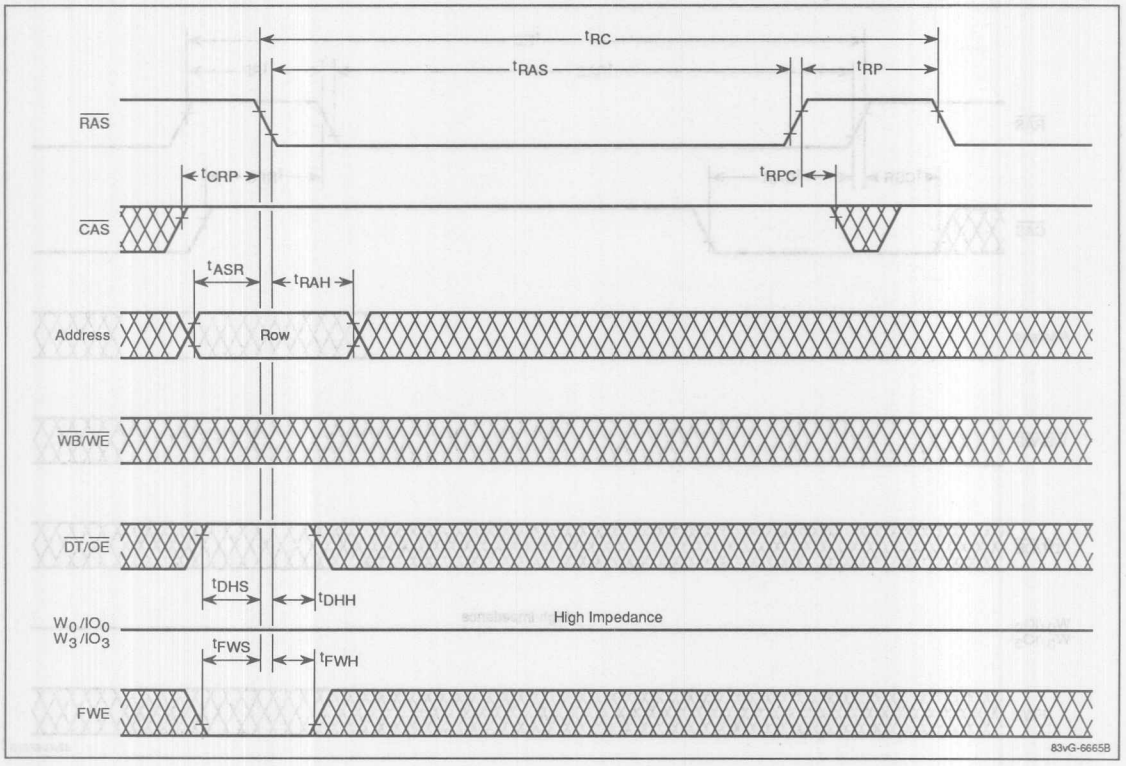
Timing Waveforms (cont)

Read-Write/Read-Modify-Write Cycle



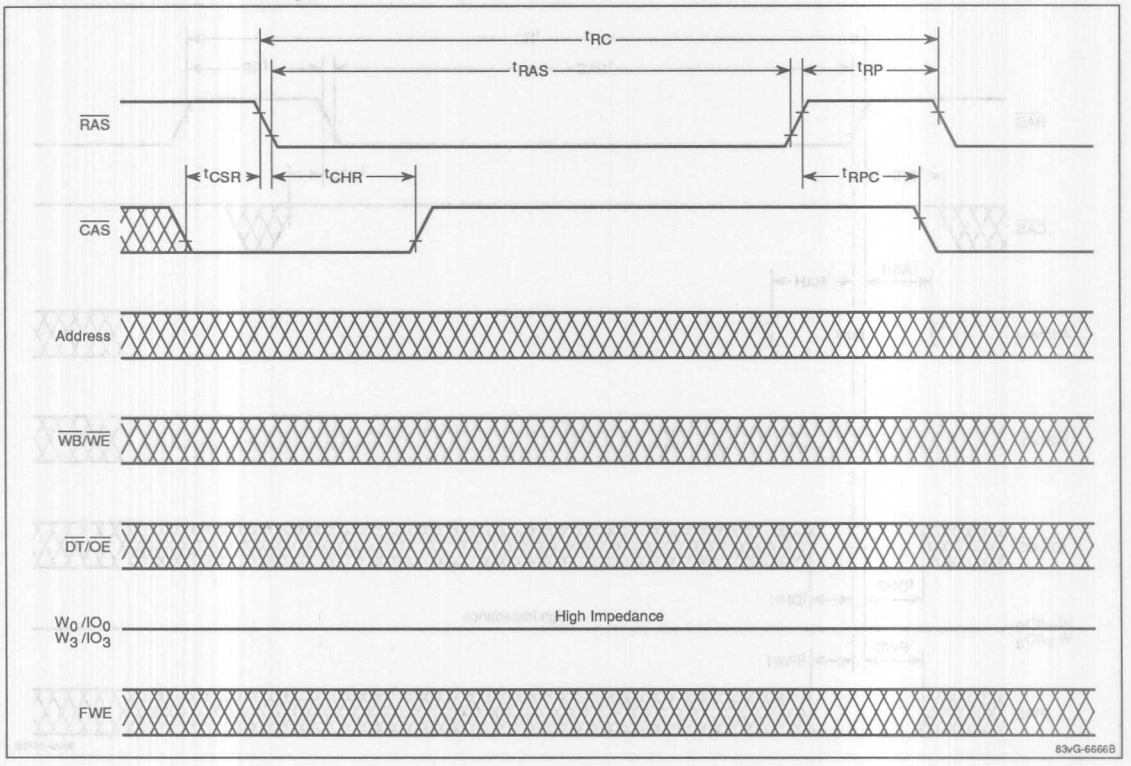
Timing Waveforms (cont)

$\overline{RAS}$-Only Refresh Cycle



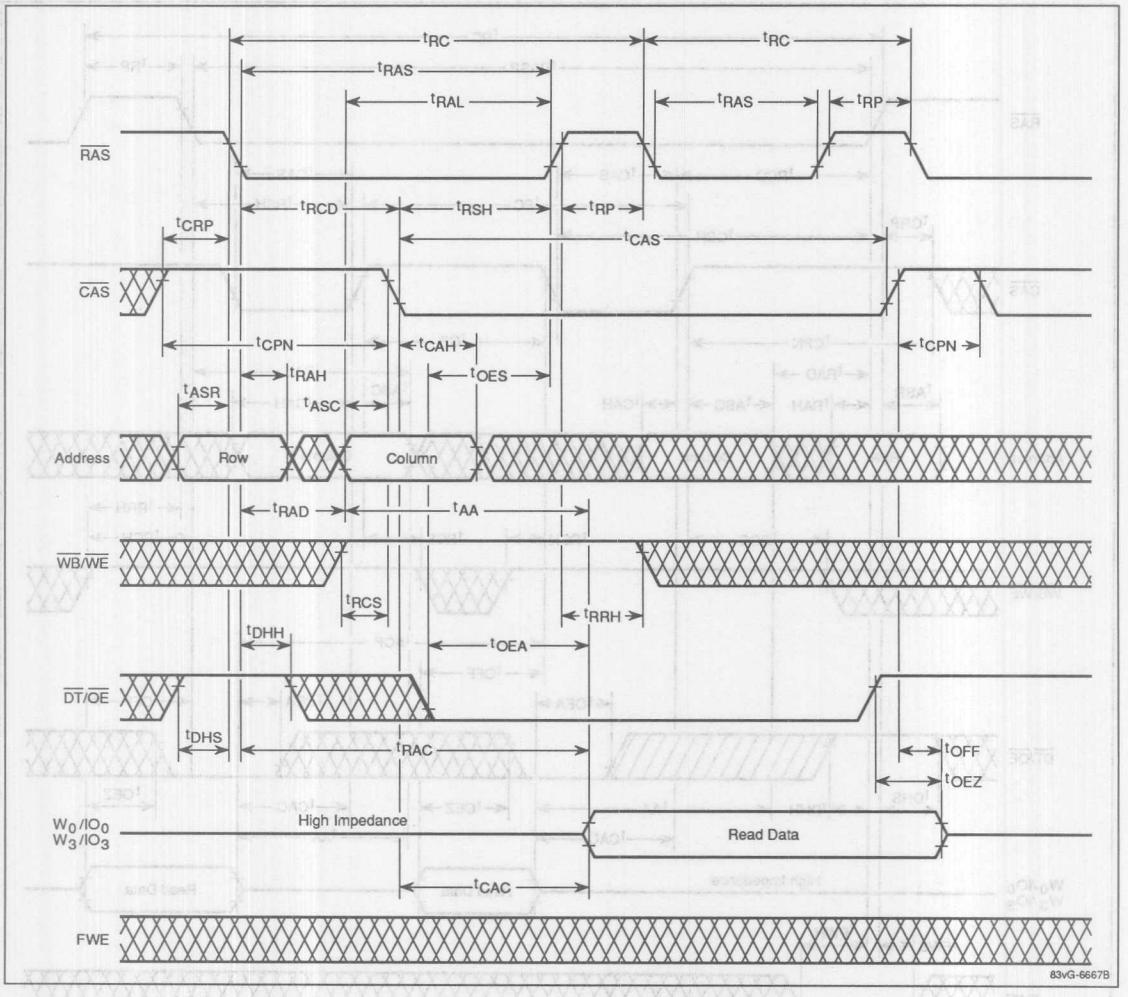
Timing Waveforms (cont)

$\overline{CAS}$ Before $\overline{RAS}$ Refresh Cycle



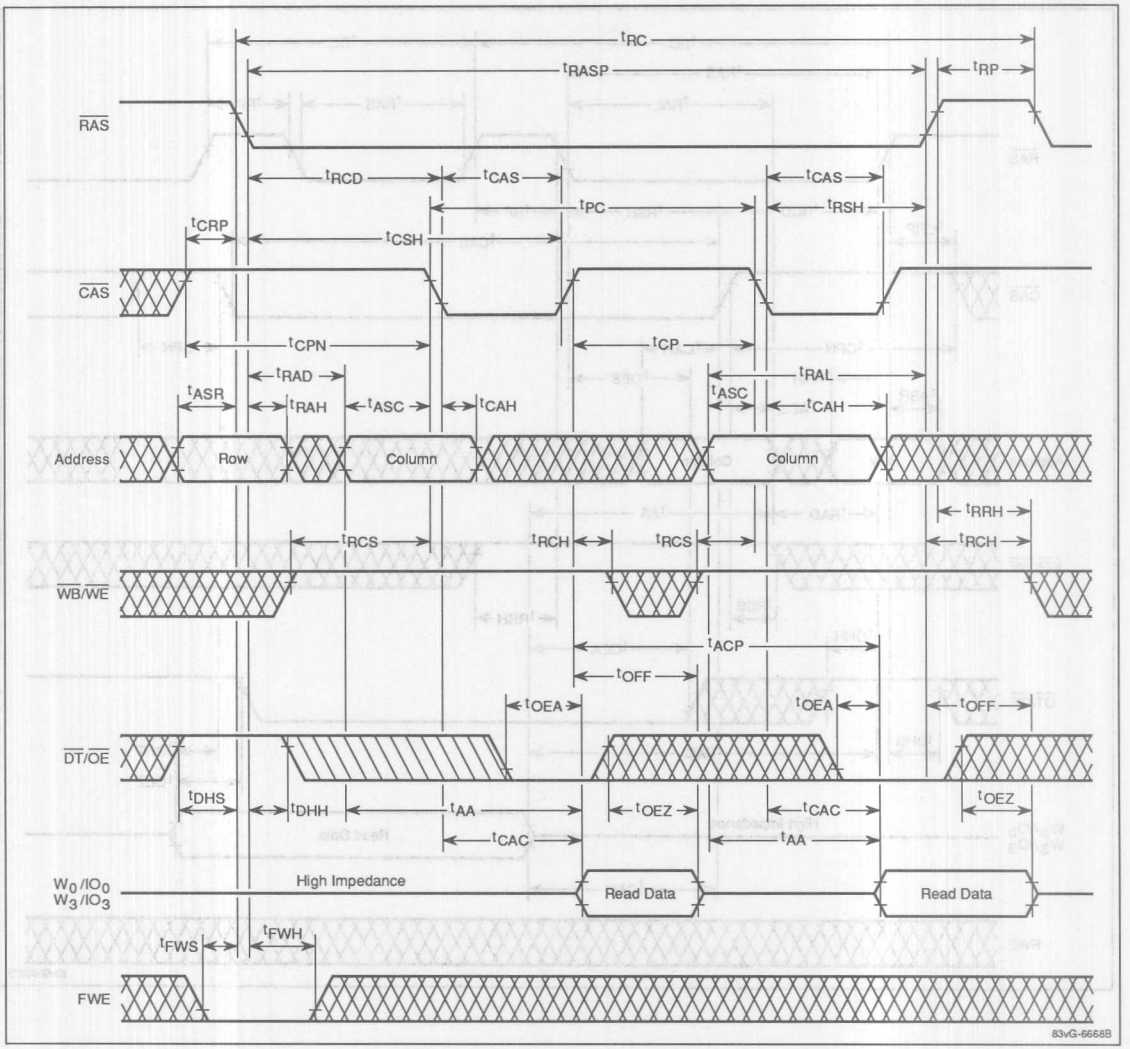
Timing Waveforms (cont)

Hidden Refresh Cycle



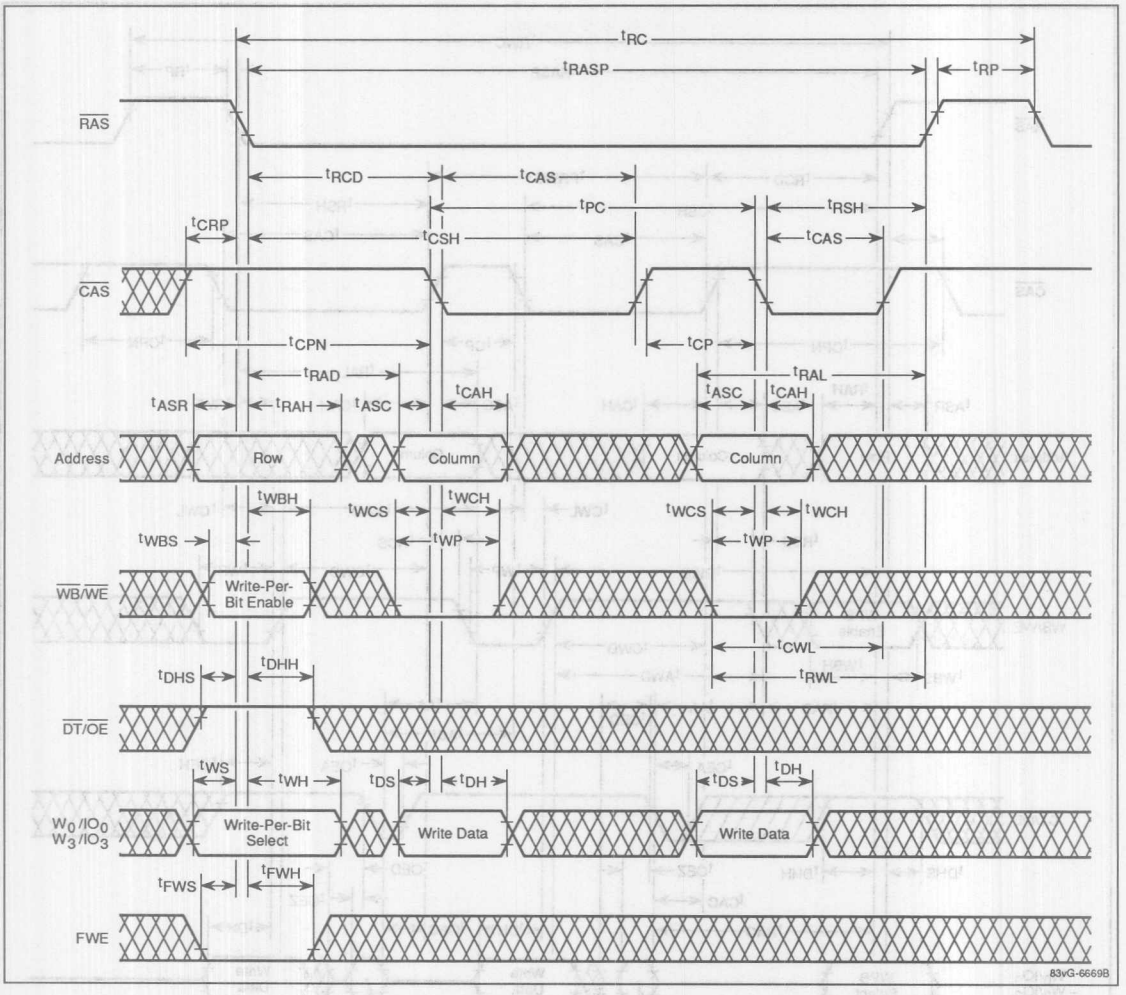
Timing Waveforms (cont)

Fast-Page Read Cycle



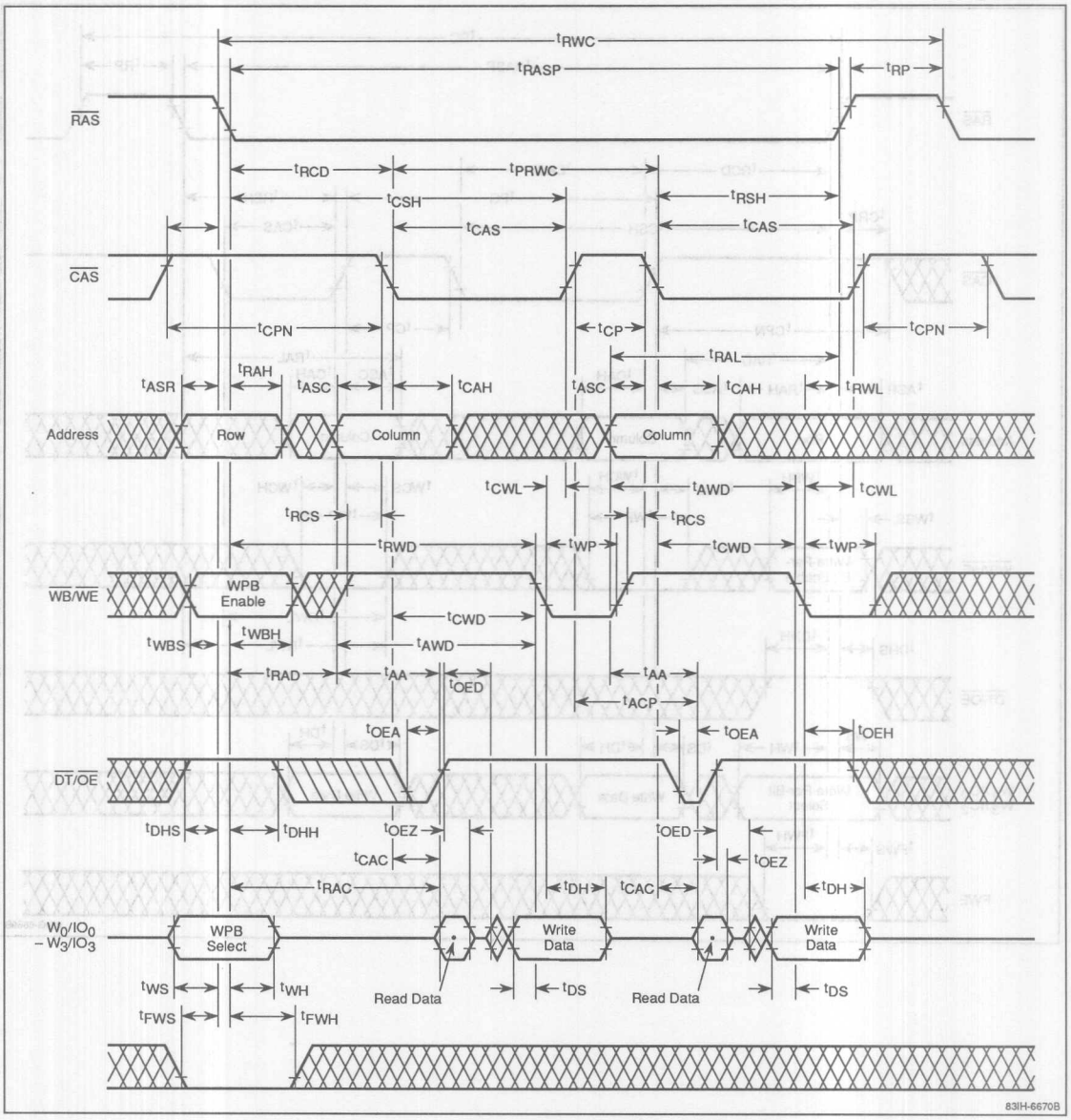
Timing Waveforms (cont)

Fast-Page Write Cycle



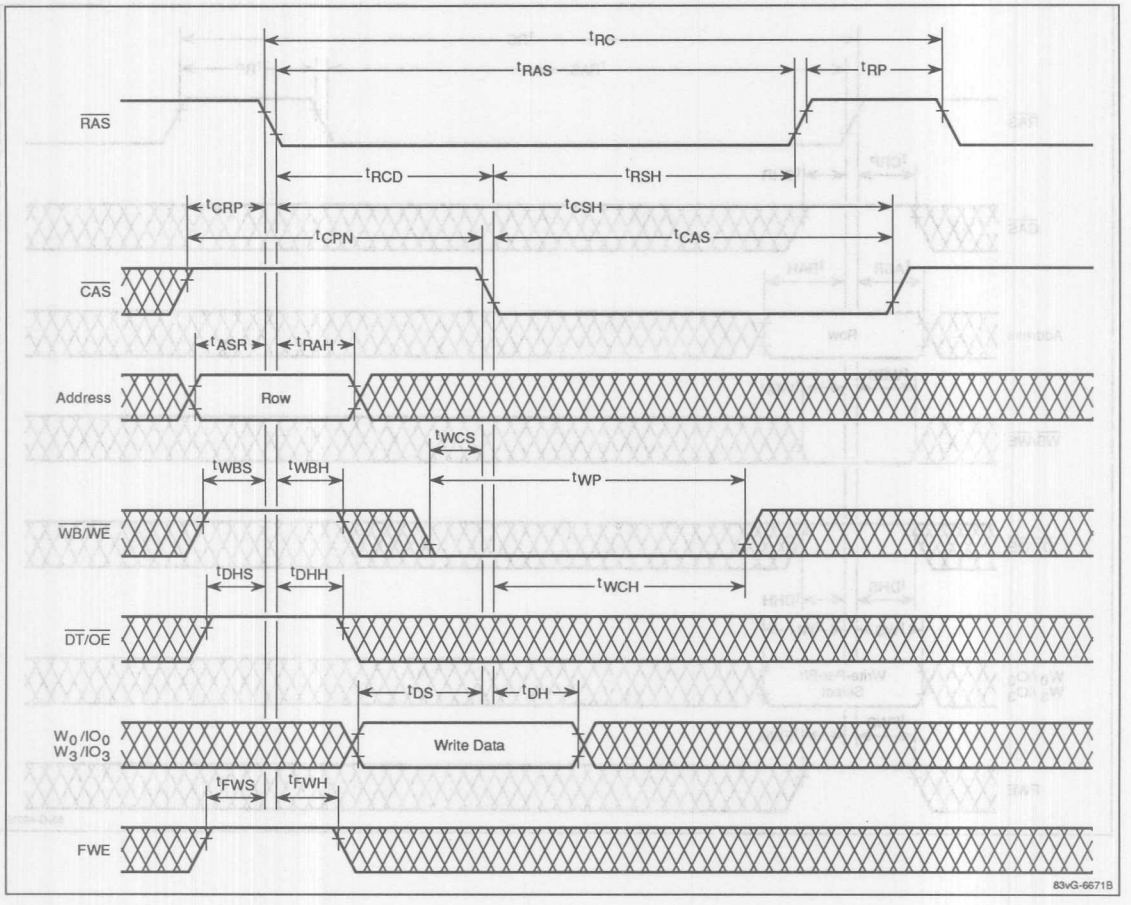
Timing Waveforms (cont)

Fast-Page Read-Modify-Write Cycle



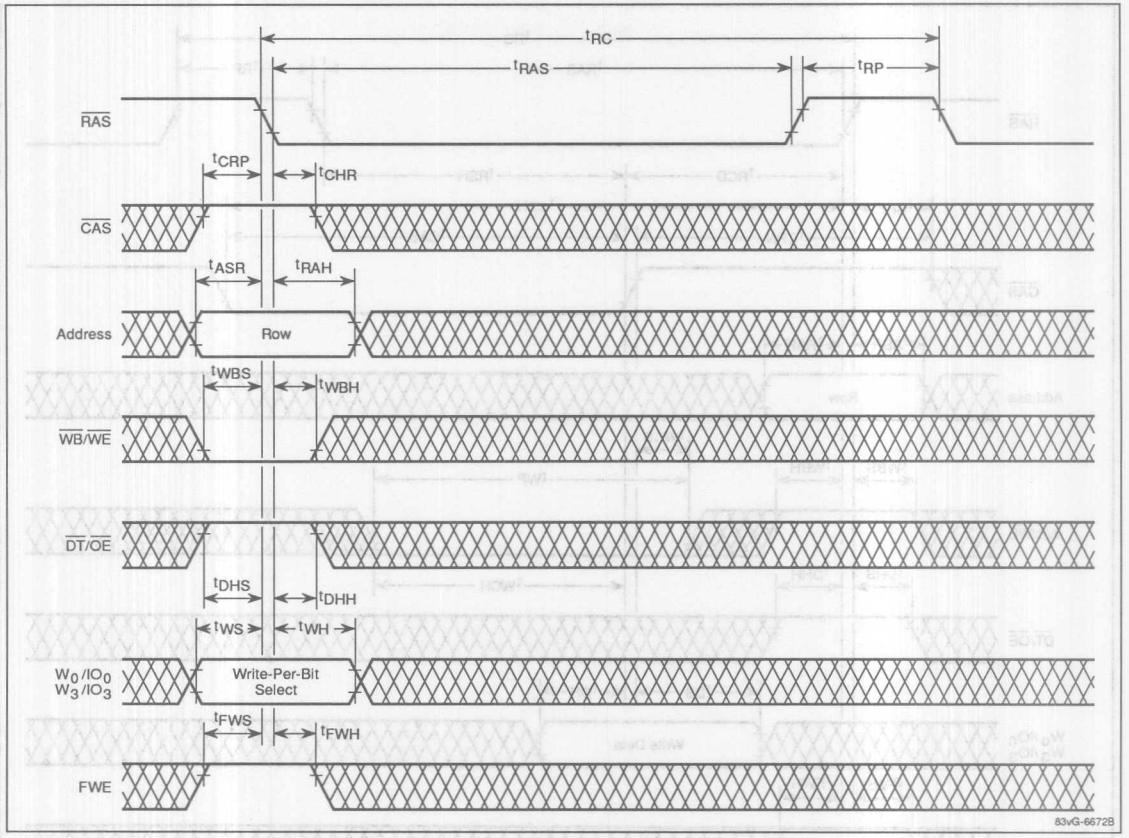
Timing Waveforms (cont)

Color Register Set Cycle



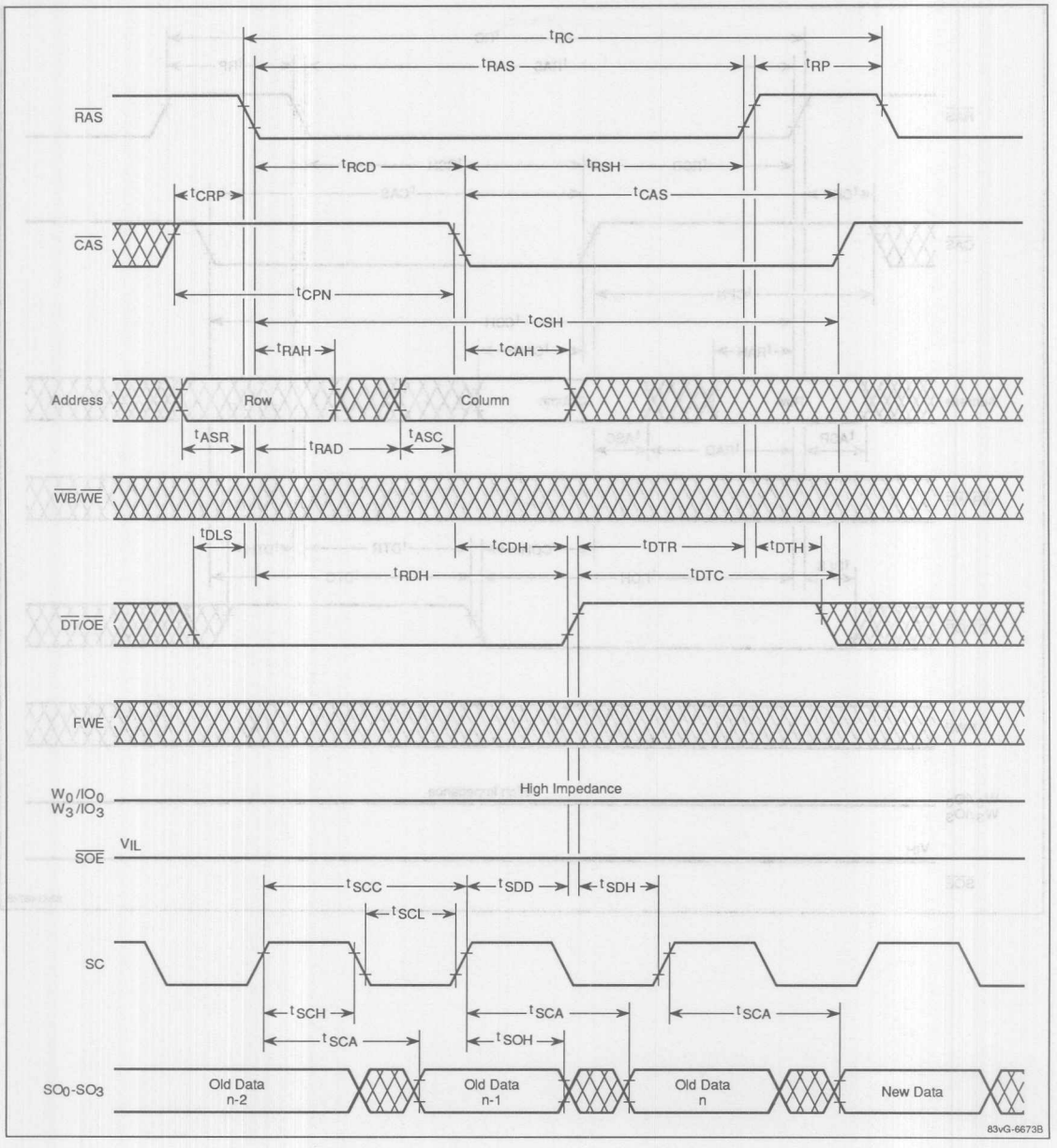
Timing Waveforms (cont)

Flash Write Cycle



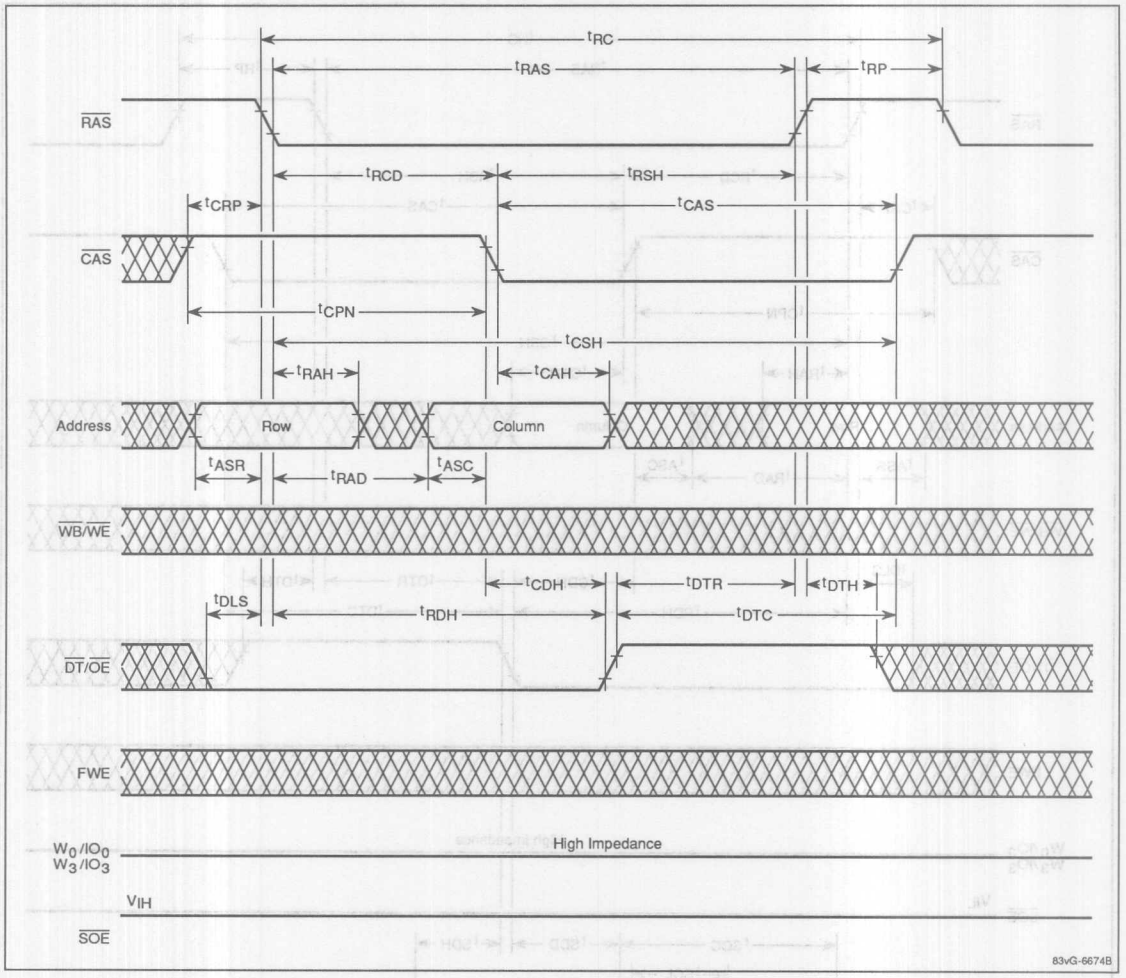
Timing Waveforms (cont)

Data Transfer Cycle with Serial Port Active



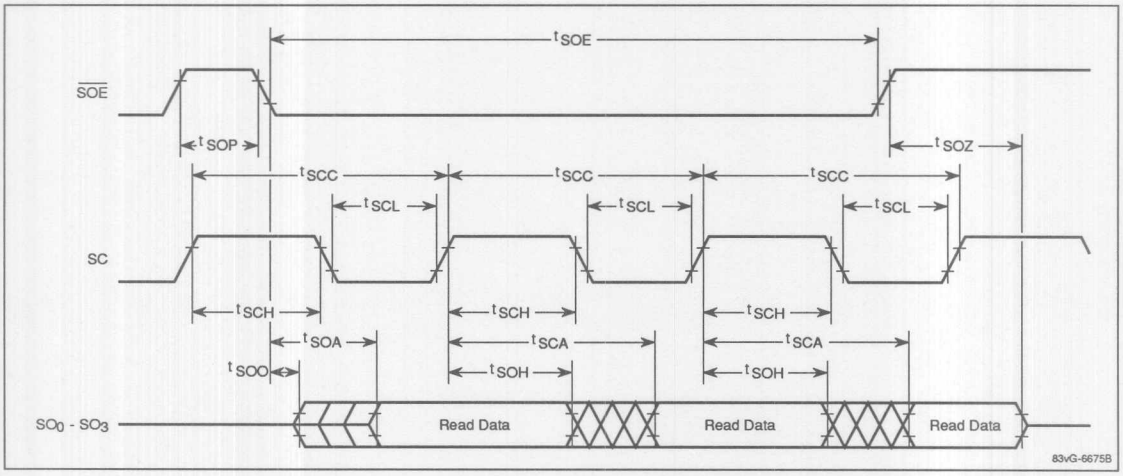
Timing Waveforms (cont)

Data Transfer Cycle with Serial Port in Standby



Timing Waveforms (cont)

Serial Read Cycle



μPD42275
Dual-Port Graphics Buffer

Description

The μPD42275 is a dual-port graphics buffer equipped with a random access port and a serial read port. The serial read port is connected to an internal 2048-bit data register through a 256 x 8-bit serial read output circuit. The 128K x 8-bit random access port is used by the host CPU to read or write data addressed in any desired order. A write-per-bit capability allows each of the eight data bits to be individually selected or masked for a write cycle. Block write cycles can also be used to write the eight data bits to four consecutive column addresses. Selection and masking of the eight data bits and four column addresses is provided. A flash write option with write-per-bit control enables data in the color register to be written to a selected row in the random access port.

The μPD42275 features fully asynchronous dual access, except when transferring graphics data from a selected row of the storage array to the data register. During a data transfer, the random access port requires a special cycle using a transfer clock; the serial port continues to operate normally. Following the clock transition of a data transfer, serial output data changes from an old line to a new line and the starting location on the new line is addressable in the data transfer cycle.

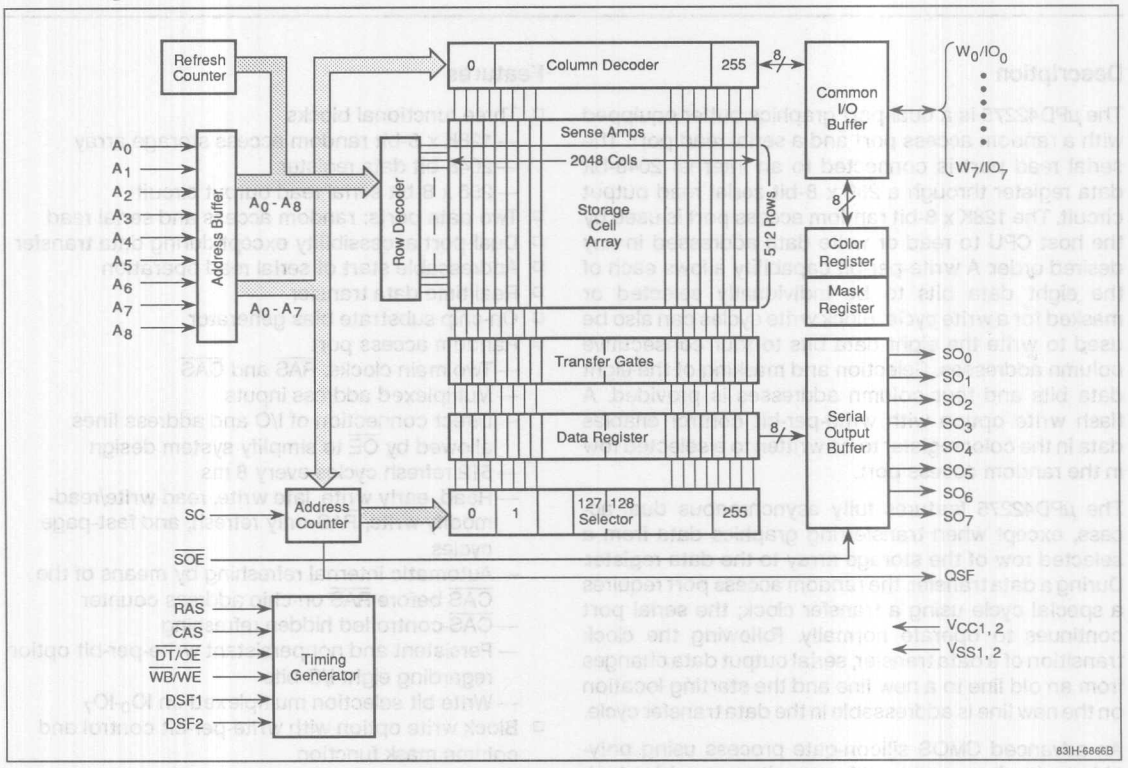
An advanced CMOS silicon-gate process using polycide technology and trench capacitors provides high storage cell density, high performance, and high reliability. Refreshing is accomplished by means of $\overline{RAS}$-only refresh cycles or by normal read or write cycles on the 512 address combinations of A_0 through A_8 during an 8-ms period. Automatic internal refreshing, by means of either hidden refreshing or the $\overline{CAS}$ before $\overline{RAS}$ timing and on-chip internal refresh circuitry, is also available. The transfer of a row of data from the storage array to the data register also refreshes that row automatically.

All inputs and outputs, including clocks, are TTL-compatible. All address and data-in signals are latched on-chip to simplify system design. Data-out is unlatched to allow greater system flexibility. The μPD42275 is available in a 400-mil, 40-pin plastic SOJ and is guaranteed for operation at 0 to + 70°C.

Features

- Three functional blocks
  - — 128K x 8-bit random access storage array
  - — 2048-bit data register
  - — 256 x 8-bit serial read output circuit
- Two data ports: random access and serial read
- Dual-port accessibility except during data transfer
- Addressable start of serial read operation
- Real-time data transfer
- On-chip substrate bias generator
- Random access port
  - — Two main clocks: $\overline{RAS}$ and $\overline{CAS}$
  - — Multiplexed address inputs
  - — Direct connection of I/O and address lines allowed by $\overline{OE}$ to simplify system design
  - — 512 refresh cycles every 8 ms
  - — Read, early write, late write, read-write/read-modify-write, $\overline{RAS}$-only refresh, and fast-page cycles
  - — Automatic internal refreshing by means of the $\overline{CAS}$ before $\overline{RAS}$ on-chip address counter
  - — $\overline{CAS}$-controlled hidden refreshing
  - — Persistent and nonpersistant write-per-bit option regarding eight I/O bits
  - — Write bit selection multiplexed on IO_0-IO_7
- Block write option with write-per-bit control and column mask function
- Flash write option with write-per-bit control
- Split serial data register to allow shifting from lower half while simultaneously loading upper half
- $\overline{RAS}$-activated data transfer
  - — Same cycle time as for random access
  - — Row data transferred to data register as specified by row address inputs
  - — Starting location of following serial read cycle specified by column address inputs
  - — Transfer of 2048 bits of data on one row to the data register, and the starting location of the serial read circuit, activated by a low-to-high transition of $\overline{DT}$
  - — Data transfer during real-time operation or standby of serial port
- Fast serial read operation by means of SC pins
- Serial data output on SO_0 - SO_7
- Direct connection of multiple serial outputs for extension of data length
- Fully TTL-compatible inputs, outputs, and clocks
- Three-state outputs for random and serial access
- CMOS silicon-gate process with trench capacitors

Block Diagram



Pin Identification

Symbol	Function
A_0 - A_8	Address inputs
W_0/IO_0 - W_7/IO_7	Write-per-bit selects/data inputs and outputs
$\overline{RAS}$	Row address strobe
$\overline{CAS}$	Column address strobe
$\overline{WB/WE}$	Write-per-bit/write enable
$\overline{DT/OE}$	Data transfer/output enable
DSF_1 and DSF_2	Special function enable
SO_0 - SO_7	Serial read outputs
SC	Serial control
$\overline{SOE}$	Serial output enable
QSF	Special function output
V_{SS1} and V_{SS2}	Ground
V_{CC1} and V_{CC2}	+5-volt ±10% power supply
NC	No connection

Ordering Information

Part Number	Row Access Time (max)	Serial Access Time (max)	Package
μPD42275LE-80	80 ns	25 ns	40-pin plastic SOJ
LE-10	100 ns	30 ns	
LE-12	120 ns	40 ns	

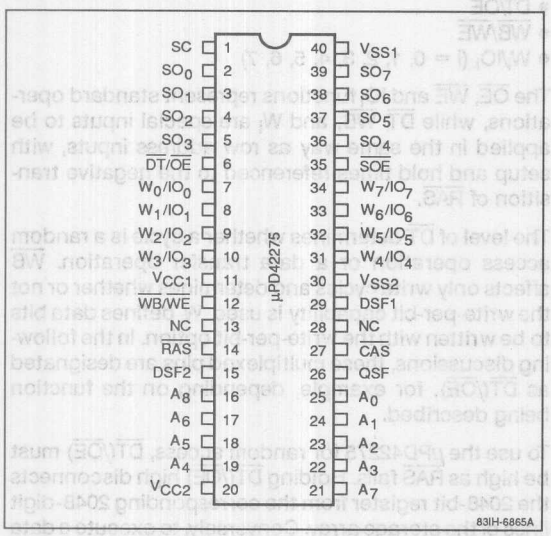
Absolute Maximum Ratings

Voltage on any pin except V_{CC} relative to GND, V_{R1}	−1.0 to +7.0 V
Voltage on V_{CC} relative to GND, V_{R2}	−1.0 to +7.0 V
Operating temperature, T_{OPR}	0 to +70°C
Storage temperature, T_{STG}	−55 to +125°C
Short-circuit output current, I_{OS}	50 mA
Power dissipation, P_D	1.5 W

Exposure to Absolute Maximum Ratings for extended periods may affect device reliability; exceeding the ratings could cause permanent damage. The device should be operated within the limits specified under DC and AC Characteristics.

Pin Configuration

40-Pin Plastic SOJ



Pin Functions

A_0-A_8 (Address Inputs). These pins are multiplexed as row and column address inputs. Each of eight data bits in the random access port corresponds to 131,072 storage cells, which means that nine row addresses and eight column addresses are required to decode one cell location. Nine row addresses are first used to select one of the 512 possible rows for a read, write, data transfer, or refresh cycle. Eight column addresses are then used to select the one of 256 possible column decoders for a read or write cycle or the one of 256 possible starting locations for the next serial read cycle. (Column addresses are not required in $\overline{RAS}$-only refresh cycles.)

W_0/IO_0-W_7/IO_7 (Write-Per-Bit Inputs/Common Data Inputs and Outputs). Each of the eight data bits can be individually latched by these inputs at the falling edge of $\overline{RAS}$ in any write cycle, and then updated at the next falling edge of $\overline{RAS}$. In a read cycle, these pins serve as outputs for the selected storage cells. In a write cycle, data input on these pins is latched by the falling edge of $\overline{CAS}$ or $\overline{WE}$.

$\overline{RAS}$ (Row Address Strobe). This pin is functionally equivalent to a chip enable signal in that whenever it is activated, the 2,048 storage cells of a selected row are sensed simultaneously and the sense amplifiers restore all data. The nine row address bits are latched by this signal and must be stable on or before its falling edge. $\overline{CAS}$, $\overline{DT/OE}$, $\overline{WB/WE}$, DSF_1 and DSF_2 are simultaneously latched to determine device operation.

$\overline{CAS}$ (Column Address Strobe). This pin serves as a chip selection signal to activate the column decoder and the input/output buffers. The eight column address bits are latched at the falling edge of $\overline{CAS}$.

QSF (Special Function Output). This pin indicates while side of the split register is active. QSF high shows that the upper half (addresses 128 through 255) is active, while QSF low indicates the lower half (addresses 0 through 127).

$DSF_1$and DSF_2 (Special Function Control). At the leading edge of $\overline{RAS}$ and $\overline{CAS}$, the high or low level of these pins is latched to initiate one of the operations shown in the Truth Table. Holding both pins low causes the device to operate without any special functions.

$\overline{WB/WE}$ (Write-Per-Bit Control/Write Enable). At the falling edge of $\overline{RAS}$, the $\overline{WB/WE}$ and DSF_1 inputs must be low and $\overline{CAS}$ and $\overline{DT/OE}$ high to enable the write-per-bit option. When $\overline{CAS}$, $\overline{DT/OE}$ and DSF_1 are high at the falling edge of $\overline{RAS}$, the level of this signal indicates either a color register set cycle or flash write cycle. A high $\overline{WB/WE}$ can be used at the beginning of a standard write or read cycle.

$\overline{DT/OE}$ (Data Transfer/Output Enable). At the falling edge of $\overline{RAS}$, $\overline{CAS}$ and $\overline{WB/WE}$ high and $\overline{DT/OE}$ low initiate a data transfer. $\overline{DT/OE}$ high initiates conventional read or write cycles and controls the output buffer in the random access port. The level of DSF_1 determines whether this is a read or split read data transfer.

SO_0-SO_7 (Serial Data Outputs). Eight-bit data is read from these pins and remains valid until the next SC signal is activated.

SC (Serial Control). Repeatedly activating this signal causes serial read cycles (starting from the location specified in the data transfer cycle) to be executed within the 2,048 bits in the data register. The rising edge of SC activates serial read operation, in which eight of the 2,048 data bits are transferred to eight serial data buses, respectively, and read out. Whenever SC is low, the serial port is in standby.

$\overline{SOE}$ (Serial Output Enable). This signal controls the serial data output buffer.

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OPERATION

The μPD42275 consists of a random access port and a serial read port. The random access port executes standard read and write cycles, as well as data transfer, block write and flash write cycles, all of which are based on conventional $\overline{RAS}/\overline{CAS}$ timing.

In a data transfer, data in each storage cell on the selected row is transferred simultaneously through a transfer gate to its corresponding register location. The serial read port shows the contents of the data register in serial order. The random access and serial read ports can operate asynchronously, except when the transfer gate is turned on during the data transfer period.

Addressing

The storage array is arranged in a 512-row by 2048-column matrix, whereby each of 8 data bits in the random access port corresponds to 131,072 storage cells and 17 address bits are required to decode one cell location. Nine row address bits are set up on pins A_0 through A_8 and latched onto the chip by $\overline{RAS}$. Eight column address bits then are set up on pins A_0 through A_7 and latched onto the chip by $\overline{CAS}$. All addresses must be stable, on or before the falling edges of $\overline{RAS}$ and $\overline{CAS}$. Whenever $\overline{RAS}$ is activated, 2048 cells on the selected row are sensed simultaneously and the sense amplifiers automatically restore the data. $\overline{CAS}$ serves as a chip selection signal to activate the column decoder and the input and output buffers.

Through 1 of 256 column decoders, 8 storage cells on the row are connected to 8 data buses, respectively. In a data transfer cycle, 9 row address bits are used to select 1 of the 512 possible rows involved in the transfer of data to the data register. Eight column address bits are then used to select the 1 of 256 possible serial decoders that corresponds to the starting location of the next serial read cycle. In the serial read port, when SC is activated, 8 data bits in the 2048-bit data register are transferred to 8 serial data buses and read out. Activating SC repeatedly causes serial read cycles (starting from the location specified in the data transfer cycle) to be executed within the 2048 bits in the data register.

Random Access Port

An operation in the random access port begins with a negative transition of $\overline{RAS}$. Both $\overline{RAS}$ and $\overline{CAS}$ have minimum pulse widths, as specified in the timing table, which must be maintained for proper device operation and data integrity. Once begun, a cycle must meet all specifications, including minimum cycle time. To reduce the number of pins, the following are multiplexed.

- $\overline{DT}/\overline{OE}$
- $\overline{WB}/\overline{WE}$
- W_i/IO_i (i = 0, 1, 2, 3, 4, 5, 6, 7)

The $\overline{OE}$, $\overline{WE}$ and IO_i functions represent standard operations, while $\overline{DT}$, $\overline{WB}$, and W_i are special inputs to be applied in the same way as row address inputs, with setup and hold times referenced to the negative transition of $\overline{RAS}$.

The level of $\overline{DT}$ determines whether a cycle is a random access operation or a data transfer operation. $\overline{WB}$ affects only write cycles and determines whether or not the write-per-bit capability is used. W_i defines data bits to be written with the write-per-bit option. In the following discussions, these multiplexed pins are designated as $\overline{DT}(/\overline{OE})$, for example, depending on the function being described.

To use the μPD42275 for random access, $\overline{DT}(/\overline{OE})$ must be high as $\overline{RAS}$ falls. Holding $\overline{DT}(/\overline{OE})$ high disconnects the 2048-bit register from the corresponding 2048-digit lines of the storage array. Conversely, to execute a data transfer, $\overline{DT}(/\overline{OE})$ must be low as $\overline{RAS}$ falls to open the 2048 transfer gates and transfer data from one of the rows to the register.

Glossary of Special Functions

Masked Write Cycle with New Mask. When the write-per-bit function is enabled as shown in the following table, mask data on the W/IO_i pins is latched by $\overline{RAS}$ and loaded directly into the write mask register. A masked write cycle is then executed using $\overline{CAS}$ or $\overline{WB}/\overline{WE}$ to strobe the W/IO_i data into the on-chip data latch.

Write-Per-Bit Function

Mask Register Data	Action
1	Write
0	Do not write

Write Mask Register Set Cycle. In this cycle, data on W_i/IO_i is written to an 8-bit write mask register, where it is retained and used by subsequent masked write and masked block write cycles.

Masked Write Cycle with Old Mask. This write-per-bit cycle, commonly referred to as a persistent mask write cycle, uses the mask data previously set by the last write mask register set cycle.

Truth Table for Random Access Port

Cycle	Must Be Valid at Falling Edge of $\overline{RAS}$					Must be valid at Falling Edge of $\overline{CAS}$	
	$\overline{CAS}$	$\overline{DT/OE}$	$\overline{WB/WE}$	DSF1	DSF2	DSF1	Mnemonic Code
Read/write cycle	H	H	H	L	X	L	RW
Block write cycle	H	H	H	L	X	H	BW
Write mask register set cycle	H	H	H	H	X	L	LWR
Color register set cycle	H	H	H	H	X	H	LCR
Write cycle with new mask	H	H	L	L	X	L	RWNM
Block write cycle with new mask	H	H	L	L	X	H	BWNM
Write cycle with old mask	H	H	L	H	L	L	RWOM
Block write cycle with old mask	H	H	L	H	L	H	BWOM
Read data transfer cycle	H	L	H	L	X	X	RT
Split read data transfer cycle	H	L	H	H	X	X	SRT
$\overline{CAS}$ before $\overline{RAS}$ refresh cycle	L	X	H	X	X	X	CBR
Flash write cycle with new mask	H	H	L	H	H	X	FWT

Notes:

(1) X = don't care.

(2) Combinations not shown are used for refresh operation.

Block Write Addresses

Column Select By I/O Data	Result	Corresponding Column Address
$I/O_3 = 1$	Write	$A_1 = 1, A_0 = 1$
$I/O_3 = 0$	No write	
$I/O_2 = 1$	Write	$A_1 = 1, A_0 = 0$
$I/O_2 = 0$	No Write	
$I/O_1 = 1$	Write	$A_1 = 0, A_0 = 1$
$I/O_1 = 0$	No write	
$I/O_0 = 1$	Write	$A_1 = 0, A_0 = 0$
$I/O_0 = 0$	No write	

Notes:

(1) Data on I/O_7, I/O_6, I/O_5 and I/O_4 are don't care at the falling edge of $\overline{CAS}$.

Color Register Set Cycle. This cycle is executed in the same fashion as a conventional read or write cycle, with a read or write cycle available to the color register under the control of $\overline{WE}$. In read operation, color register data is read on the common W_i/IO_i pins. In write operation, common W_i/IO_i data can be written into the color register. $\overline{RAS}$-only refreshing is internally performed on the row selected by A_0 through A_8. This setup cycle precedes the first flash write or block write cycle supplying the eight write data bits.

Block Write Cycle. In a block write cycle, A_1 and A_0 are ignored. I/O_0 - I/O_3 are used to select one or a combination of four column address(es) for writing in an early write, late write, page early write, or page late write cycle. Block write data is previously stored in the color register using a set color register cycle. Column select data is latched by the W/IO_i pins at the falling edge of $\overline{CAS}$ or $\overline{WE}$. Block write cycles are useful for clearing windows and for accelerating polygon fill operations.

Masked Block Write Cycle with New Mask. This cycle allows for $W/I/O_0$ - $W/I/O_7$ masking during a block write cycle. The masking function is identical to a standard masked write cycle with new mask, except that four consecutive columns are written.

Masked Block Write Cycle with Old Mask. This cycle uses the masked data previously set by the last write mask register set cycle to write four consecutive columns.

Flash Write Cycle. A flash write cycle can clear or set each of the eight 256-bit data sets on the selected one of 512 possible rows according to data stored in the previously set color register. Bit mask inputs are latched as $\overline{RAS}$. This cycle is useful in graphics processing applications when the screen should be cleared or set to some uniform value as quickly as possible.

Read Data Transfer Cycle. In a full row read data transfer cycle, one of the possible 512 rows, as well as the starting location of the following serial read cycle, is defined by address inputs. The low-to-high transition of DT/($\overline{OE}$) causes the 2048 bits of cell data to be transferred to the serial data register.

3

Split Read Transfer Cycle. This cycle is a half row data transfer in which one of the 512 rows, the starting location of the following serial read cycle, and either of the split registers are specified by the address inputs. On-chip control circuitry causes the previously specified half row to be transferred to the selected upper or lower split register.

Read Cycle. A read cycle is executed by activating $\overline{RAS}$, $\overline{CAS}$, and $\overline{OE}$ and by maintaining ($\overline{WB}$/)$\overline{WE}$ while $\overline{CAS}$ is active. The (W_i/)IO_i pin (i = 0 through 7) remains in high impedance until valid data appears at the output at access time. Device access time, t_{ACC}, will be the longest of the following four calculated intervals:

- t_{RAC}
- $\overline{RAS}$ to $\overline{CAS}$ delay (t_{RCD}) + t_{CAC}
- $\overline{RAS}$ to column address delay (t_{RAD}) + t_{AA}
- $\overline{RAS}$ to $\overline{OE}$ delay + t_{OEA}

Access times from $\overline{RAS}$ (t_{RAC}), from $\overline{CAS}$ (t_{CAC}), from the column addresses (t_{AA}), and from $\overline{OE}$ (t_{OEA}) are device parameters. The $\overline{RAS}$-to-$\overline{CAS}$, $\overline{RAS}$-to-column address, and $\overline{RAS}$-to-$\overline{OE}$ delays are system-dependent timing parameters. Output becomes valid after the access time has elapsed and it remains valid while both $\overline{CAS}$ and $\overline{OE}$ are low. Either $\overline{CAS}$ or $\overline{OE}$ high returns the output pins to high impedance.

Write Cycle. A write cycle is executed by bringing ($\overline{WB}$/)$\overline{WE}$ low during the $\overline{RAS}$/$\overline{CAS}$ cycle. The falling edge of $\overline{CAS}$ or ($\overline{WB}$/)$\overline{WE}$ strobes the data on (W_i/)IO_i into the on-chip data latch. To make use of the write-per-bit option, $\overline{WB}$(/$\overline{WE}$) must be low as $\overline{RAS}$ falls. In this case, write data bits can be specified by keeping W_i(/IO_i) high, with setup and hold times referenced to the negative transition of $\overline{RAS}$.

Write-Per-Bit Cycle. The falling edge of $\overline{RAS}$ latches the write-per-bit mask data input on W_0 through W_7. If DSF_1 is low at the falling edge of $\overline{RAS}$, mask data must be reloaded every write-per-bit mask cycle. If DSF_1 is high and DSF2 is low at the falling edge of $\overline{RAS}$, mask data is not reloaded from W_0 through W_7 but is retained from the previous write mask set cycle. The latter is called a persistent write-per-bit cycle.

Early Write Cycle. An early write cycle is executed by bringing ($\overline{WB}$/)$\overline{WE}$ low before $\overline{CAS}$ falls. Data is strobed by $\overline{CAS}$, with setup and hold times referenced to this signal, and the output remains in high impedance for the entire cycle. As $\overline{RAS}$ falls, ($\overline{DT}$/)$\overline{OE}$ must meet the setup and hold times of a high $\overline{DT}$, but otherwise ($\overline{DT}$/)$\overline{OE}$ does not affect any circuit operation while $\overline{CAS}$ is active.

Read-Write/Read-Modify-Write Cycle. This cycle is executed by bringing ($\overline{WB}$/)$\overline{WE}$ low with the $\overline{RAS}$ and $\overline{CAS}$ signals low. (W_i/)IO_i shows read data at access time. Afterward, in preparation for the upcoming write cycle, (W_i/)IO_i returns to high impedance when ($\overline{DT}$/)$\overline{OE}$ goes high. The data to be written is strobed by ($\overline{WB}$/)$\overline{WE}$, with setup and hold times referenced to this signal.

Late Write Cycle. This cycle shows the timing flexibility of ($\overline{DT}$/)$\overline{OE}$, which can be activated just after ($\overline{WB}$/)$\overline{WE}$ falls, even when ($\overline{WB}$/)$\overline{WE}$ is brought low after $\overline{CAS}$.

Refresh Cycle. A cycle at each of the 512 row addresses (A_0 through A_8) will refresh all storage cells. Any cycle executed in the random access port (i.e., read, write, refresh, data transfer, color register set, flash write or block write) refreshes the 2048 bits selected by the $\overline{RAS}$ addresses or by the on-chip address counter.

$\overline{RAS}$-Only Refresh Cycle. A cycle having only $\overline{RAS}$ active refreshes all cells in one row of the storage array. A high $\overline{CAS}$ is maintained while $\overline{RAS}$ is active to keep (W_i/)IO_i in high impedance. This method is preferred for refreshing, especially when the host system consists of multiple rows of random access devices. The data outputs may be OR-tied with no bus contention when $\overline{RAS}$-only refresh cycles are executed.

$\overline{CAS}$ Before $\overline{RAS}$ Refresh Cycle. This cycle executes internal refreshing using the on-chip control circuitry. Whenever $\overline{CAS}$ is low as $\overline{RAS}$ falls, this circuitry automatically refreshes the row addresses specified by the internal counter. In this cycle, the circuit operation based on $\overline{CAS}$ is maintained in a reset state. When internal refreshing is complete, the address counter automatically increments in preparation for the next $\overline{CAS}$ before $\overline{RAS}$ cycle.

Hidden Refresh Cycle. This cycle is executed after a read cycle, without disturbing the read data output. Once valid, the data output is controlled by $\overline{CAS}$ and $\overline{OE}$. After the read cycle, $\overline{CAS}$ is held low while $\overline{RAS}$ goes high for precharge. A $\overline{RAS}$-only cycle is then executed (except that $\overline{CAS}$ is held at a low level instead of a high level) and the data output remains valid. Since hidden refreshing is the same as $\overline{CAS}$ before $\overline{RAS}$ refreshing, the data output remains valid during either operation.

Fast-Page Cycle. This feature allows faster data access by keeping the same row address while successive column addresses are strobed onto the chip. Maintaining $\overline{RAS}$ low while successive $\overline{CAS}$ cycles are executed causes data to be transferred at a faster rate because

row addresses are maintained internally and do not have to be reapplied. In fast-page operation, read, write and read-write/read-modify-write cycles may be executed. Additionally, the write-per-bit control specified in the entry write cycle is maintained throughout the next fast-page write cycle.

During a fast-page read cycle, the $(W_i/)IO_i$ data pin (i = 0 through 7) remains in a state of high impedance until valid data appears at the output pin at access time. Device access time in this cycle will be the longest of the following intervals:

- t_{ACP}
- $t_{CP} + t_T + t_{CAC}$
- $\overline{CAS}$ high to column address delay $+ t_{AA}$

Serial Read Port

The serial read port is used to serially read the previously loaded contents of the data register starting from a specified location. Other graphics buffers require very tight timing to synchronize this port with the random access port, but the μPD42275 has been designed with a split register to eliminate the need for synchronized timing between the two ports.

Split Register Data Transfer. A review of the split register architecture shows that the lower register (addresses 0 - 127) and upper register (addresses 128 - 255) are selected by the most significant bit of the column addresses (A_7). With the serial port split in half, data transfers can be executed to the inactive side (no SC clocks) while SC clocks are input to access data from the active side. This sequence allows for a longer time window to perform the transfer, i.e., 128 x t_{SCC}, or 3.84 μs. Column address bits A_0 through A_6 are latched on-chip to provide the tap address pointer for each split register.

QSF Special Function Output. This pin outputs a signal indicating which half of the data register is active and is synchronized with the SC clock.

Split Data Transfer Cycle

Most Significant Bit (A_7)	Portion of Split Register	QSF
0	0 through 127	Low
1	128 through 255	High

Notes:

(1) A full data transfer cycle must precede all split register operations.

(2) Column address A_7 must be specified for a split data transfer cycle.

Data in the data register is clocked serially by SC, starting from the first specified address of either register. After the last specified address has been transferred, QSF changes its level at the next rising edge of SC and serial data transfer switches to the other (formerly inactive) register. Serial data output is maintained until the next SC clock.

SC clocks at the transition point, i.e., the end of one half and the beginning of the new half of the split registers, are restricted. Rising edges of the SC clock are not allowed for the last serial address (either 127 or 255) of the active register and for the first address (any address depending on current address pointer) of the next active register (figure 2).

$\overline{SOE}$ controls impedance of the serial output to allow multiplexing of more than one bank of μPD42275s on the same bus and has no effect on SC. When $\overline{SOE}$ is low, SO_i is disabled and in a state of high impedance.

Recommended Operating Conditions

Parameter	Symbol	Min	Typ	Max	Unit
Supply voltage	V_{CC}	4.5	5.0	5.5	V
Input voltage, high	V_{IH}	2.4		5.5	V
Input voltage, low	V_{IL}	−1.0		0.8	V
Ambient temperature	T_A	0		70	°C

Figure 1. Example of Split Register Transfer

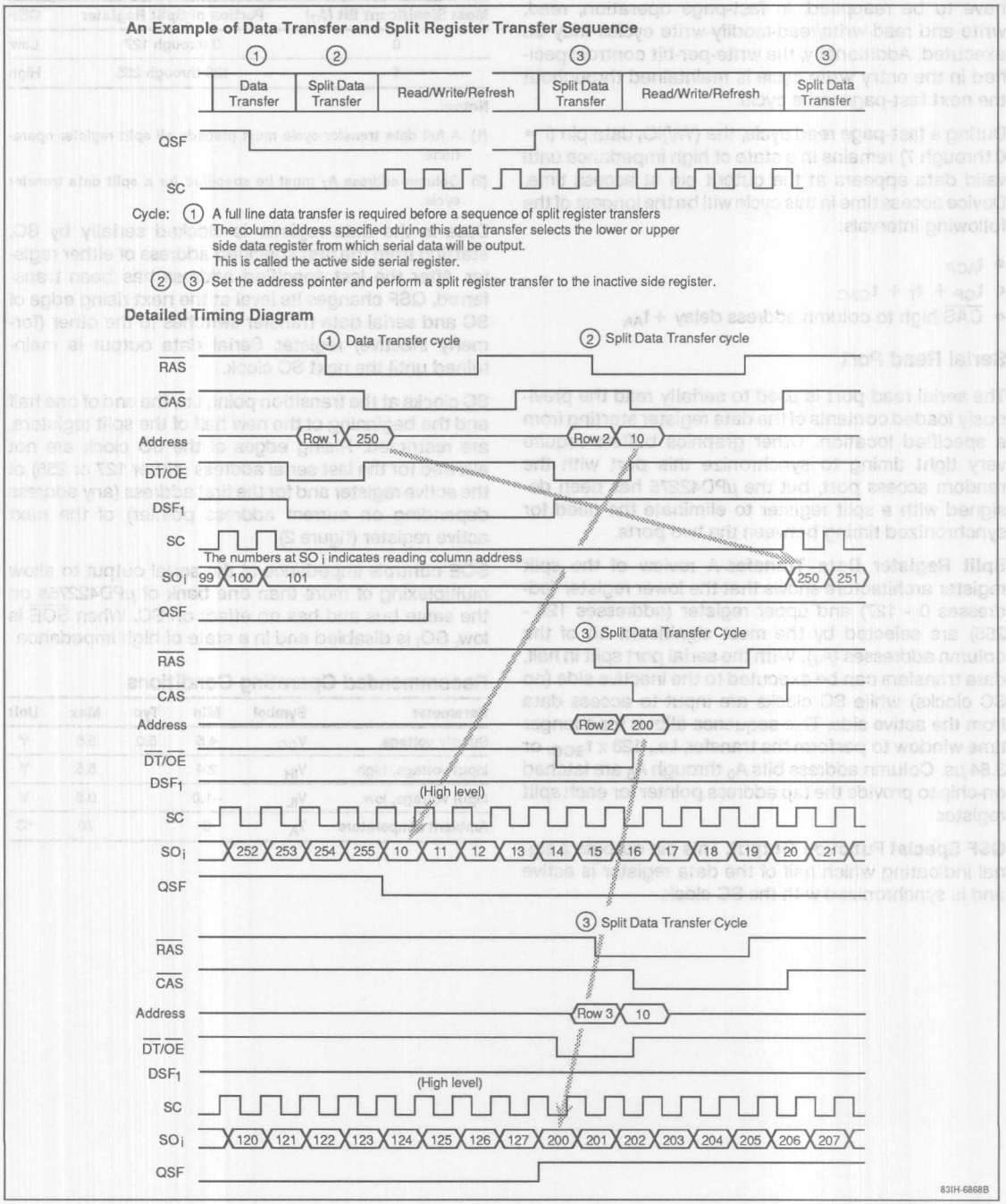
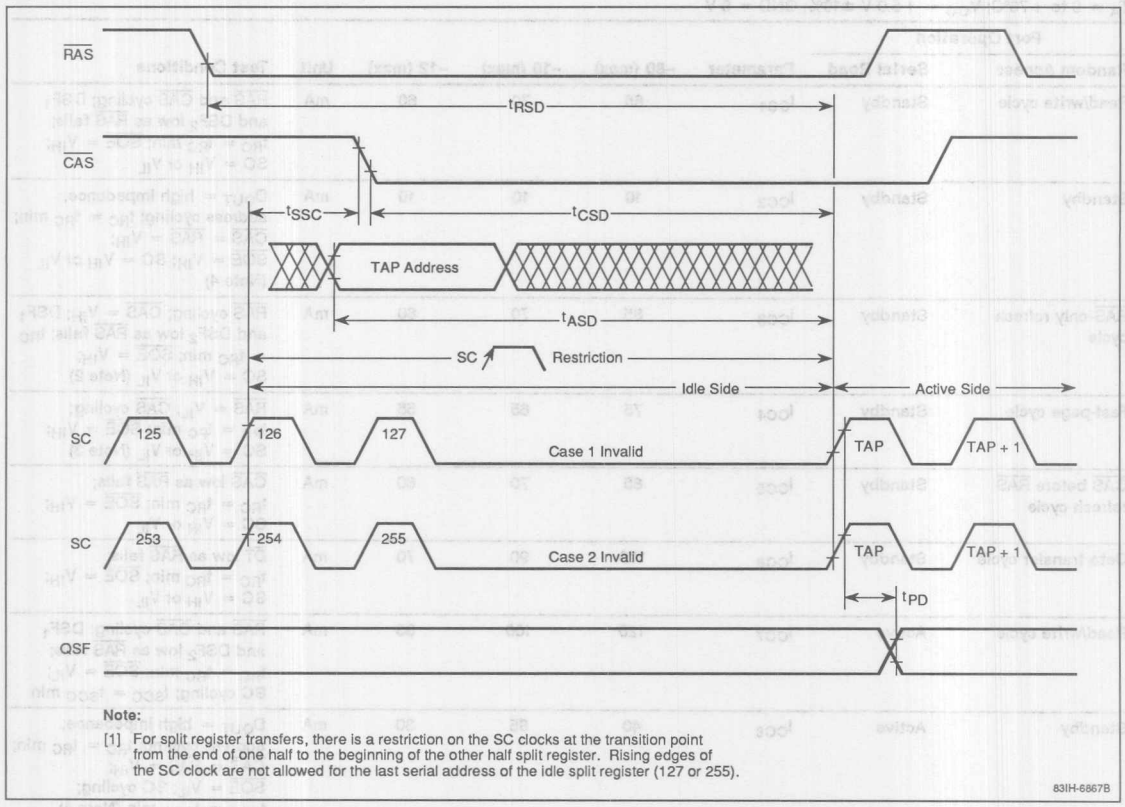


Figure 2. Restrictions on Rising Edges of SC



Note:

[1] For split register transfers, there is a restriction on the SC clocks at the transition point from the end of one half to the beginning of the other half split register. Rising edges of the SC clock are not allowed for the last serial address of the idle split register (127 or 255).

83IH-6867B

Capacitance

T_A = 0 to +70°C; V_{CC} = +5.0 V ±10%; f = 1 MHz; GND = 0 V

Parameter	Symbol	Limit (max)	Unit	Pins Under Test
Input capacitance	$C_{I(A)}$	5	pF	A_0 through A_8
	$C_{I(\overline{DT/OE})}$	8	pF	$\overline{DT/OE}$
	$C_{I(\overline{WB/WE})}$	8	pF	$\overline{WB/WE}$
	$C_{I(DSF)}$	8	pF	DSF_1 and DSF_2
	$C_{I(\overline{RAS})}$	8	pF	$\overline{RAS}$
	$C_{I(\overline{CAS})}$	8	pF	$\overline{CAS}$
	$C_{I(\overline{SOE})}$	8	pF	$\overline{SOE}$
	$C_{I(SC)}$	8	pF	SC
Input/output capacitance	$C_{IO(W/IO)}$	7	pF	W_0/IO_0 through W_7/IO_7
Output capacitance	$C_{O(SO)}$	7	pF	SO_0 through SO_7
	$C_{O(QSF)}$	7	pF	QSF

Power Supply Current

T_A = 0 to +70°C; V_{CC} = +5.0 V ±10%; GND = 0 V

Port Operation							
Random Access	Serial Read	Parameter	–80 (max)	–10 (max)	–12 (max)	Unit	Test Conditions
Read/write cycle	Standby	I_{CC1}	85	70	60	mA	$\overline{RAS}$ and $\overline{CAS}$ cycling; DSF_1 and DSF_2 low as $\overline{RAS}$ falls; $t_{RC} = t_{RC}$ min; $\overline{SOE} = V_{IH}$; SC = V_{IH} or V_{IL}
Standby	Standby	I_{CC2}	10	10	10	mA	D_{OUT} = high impedance; address cycling; $t_{RC} = t_{RC}$ min; $\overline{CAS} = \overline{RAS} = V_{IH}$; $\overline{SOE} = V_{IH}$; SC = V_{IH} or V_{IL} (Note 4)
$\overline{RAS}$-only refresh cycle	Standby	I_{CC3}	85	70	60	mA	$\overline{RAS}$ cycling; $\overline{CAS} = V_{IH}$; DSF_1 and DSF_2 low as $\overline{RAS}$ falls; $t_{RC} = t_{RC}$ min; $\overline{SOE} = V_{IH}$; SC = V_{IH} or V_{IL} (Note 2)
Fast-page cycle	Standby	I_{CC4}	75	65	55	mA	$\overline{RAS} = V_{IL}$; $\overline{CAS}$ cycling; $t_{PC} = t_{PC}$ min; $\overline{SOE} = V_{IH}$; SC = V_{IH} or V_{IL} (Note 3)
$\overline{CAS}$ before $\overline{RAS}$ refresh cycle	Standby	I_{CC5}	85	70	60	mA	$\overline{CAS}$ low as $\overline{RAS}$ falls; $t_{RC} = t_{RC}$ min; $\overline{SOE} = V_{IH}$; SC = V_{IH} or V_{IL}
Data transfer cycle	Standby	I_{CC6}	105	90	70	mA	$\overline{DT}$ low as $\overline{RAS}$ falls; $t_{RC} = t_{RC}$ min; $\overline{SOE} = V_{IH}$; SC = V_{IH} or V_{IL}
Read/write cycle	Active	I_{CC7}	120	100	85	mA	$\overline{RAS}$ and $\overline{CAS}$ cycling; DSF_1 and DSF_2 low as $\overline{RAS}$ falls; $t_{RC} = t_{RC}$ min; $\overline{SOE} = V_{IL}$; SC cycling; $t_{SCC} = t_{SCC}$ min
Standby	Active	I_{CC8}	40	35	30	mA	D_{OUT} = high impedance; address cycling; $t_{RC} = t_{RC}$ min; $\overline{CAS} = \overline{RAS} = V_{IH}$; $\overline{SOE} = V_{IL}$; SC cycling; $t_{SCC} = t_{SCC}$ min (Note 4)
$\overline{RAS}$-only refresh cycle	Active	I_{CC9}	120	100	85	mA	$\overline{RAS}$ cycling; $\overline{CAS} = V_{IH}$; DSF_1 and DSF_2 low as $\overline{RAS}$ falls; $t_{RC} = t_{RC}$ min; $\overline{SOE} = V_{IL}$; SC cycling; $t_{SCC} = t_{SCC}$ min
Fast-page cycle	Active	I_{CC10}	110	95	75	mA	$\overline{RAS} = V_{IL}$; $\overline{CAS}$ cycling; $t_{PC} = t_{PC}$ min; $\overline{SOE} = V_{IL}$; SC cycling; $t_{SCC} = t_{SCC}$ min (Note 3)
$\overline{CAS}$ before $\overline{RAS}$ refresh cycle	Active	I_{CC11}	120	100	85	mA	$\overline{CAS}$ low as $\overline{RAS}$ falls; $t_{RC} = t_{RC}$ min; $\overline{SOE} = V_{IL}$; SC cycling; $t_{SCC} = t_{SCC}$ min
Data transfer cycle	Active	I_{CC12}	140	120	95	mA	$\overline{DT}$ low as $\overline{RAS}$ falls; $t_{RC} = t_{RC}$ min; $\overline{SOE} = V_{IL}$; SC cycling; $t_{SCC} = t_{SCC}$ min
Color register set cycle	Standby	I_{CC13}	80	65	55	mA	$t_{RC} = t_{RC}$ min; $\overline{SOE} = V_{IH}$; SC = V_{IH} or V_{IL}
Flash write cycle	Standby	I_{CC14}	80	65	55	mA	$t_{RC} = t_{RC}$ min; $\overline{SOE} = V_{IH}$; SC = V_{IH} or V_{IL}
Color register set cycle	Active	I_{CC15}	115	95	80	mA	$t_{RC} = t_{RC}$ min; $\overline{SOE} = V_{IL}$; SC cycling; $t_{SCC} = t_{SCC}$ min

Power Supply Current (cont)

Port Operation							
Random Access	Serial Read	Parameter	−80 (max)	−10 (max)	−12 (max)	Unit	Test Conditions
Flash write cycle	Active	I_{CC16}	115	95	80	mA	$t_{RC} = t_{RC}$ min; $\overline{SOE} = V_{IL}$; SC cycling; $t_{SCC} = t_{SCC}$ min
Block write cycle	Standby	I_{CC17}	95	80	70	mA	$t_{RC} = t_{RC}$ min; $\overline{SOE} = V_{IH}$; SC = V_{IH} or V_{IL}
Block write cycle	Active	I_{CC18}	130	110	95	mA	$t_{RC} = t_{RC}$ min; $\overline{SOE} = V_{IL}$; SC cycling; $t_{SCC} = t_{SCC}$ min

Notes:

(1) No load on IO_i or SO_i. Except for I_{CC2}, I_{CC3}, I_{CC6}, and I_{CC14}, real values depend on output loading in addition to cycle rates.

(2) $\overline{CAS}$ is not clocked, but is kept at a stable high level. The column addresses are also assumed to be kept stable, at either a high or low level.

(3) A change in column addresses must not occur more than once in a fast-page cycle.

(4) A change in row addresses must not occur more than once in a read or write cycle.

3

DC Characteristics

T_A = 0 to +70 °C; V_{CC} = +5.0 V ±10%; GND = 0 V

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions
Input leakage current	I_{IL}	−10		10	μA	V_{IN} = 0 to 5.5 V; all other pins not under test = 0 V
Output leakage current	I_{OL}	−10		10	μA	D_{OUT} (IO_i, SO_i) disabled; V_{OUT} = 0 to 5.5 V
Random access port output voltage, high	$V_{OH(R)}$	2.4			V	$I_{OH(R)}$ = −1 mA
Random access port output voltage, low	$V_{OL(R)}$			0.4	V	$I_{OL(R)}$ = 2.1 mA
Serial read port output voltage, high	$V_{OH(S)}$	2.4			V	$I_{OH(S)}$ = −1 mA
Serial read port output voltage, low	$V_{OL(S)}$			0.4	V	$I_{OL(S)}$ = 2.1 mA

AC Characteristics

T_A = 0 to +70°C; V_{CC} = +5.0 V ±10%; GND = 0 V

		μPD42275-80		μPD42275-10		μPD42275-12			
Parameter	Symbol	Min	Max	Min	Max	Min	Max	Unit	Test Conditions
Switching Characteristics									
Access time from column address	t_{AA}		45		55		65	ns	(Notes 3 and 4)
Access time from rising edge of $\overline{CAS}$	t_{ACP}		45		55		65	ns	(Notes 3 and 4)
Access time from $\overline{RAS}$	t_{RAC}		80		100		120	ns	(Notes 3 and 4)
Access time from falling edge of $\overline{CAS}$	t_{CAC}		20		25		30	ns	(Notes 3 and 4
Access time from $\overline{CAS}$, mask register read cycle	t_{CAC}		25		30		35	ns	(Note 14)
Access time from $\overline{OE}$	t_{OEA}		20		25		30	ns	(Notes 3 and 4)
Output disable time from $\overline{CAS}$ high	t_{OFF}	0	20	0	25	0	30	ns	(Note 5)
Output disable time from $\overline{OE}$ high	t_{OEZ}	0	20	0	25	0	30	ns	(Note 5)
Serial output access time from SC	t_{SCA}		25		30		40	ns	(Note 3)
Serial output access time from $\overline{SOE}$	t_{SOA}		20		25		30	ns	(Note 3)
Serial output disable time from $\overline{SOE}$ high	t_{SOZ}	0	10	0	15	0	20	ns	(Note 5)

AC Characteristics (cont)

Parameter	Symbol	μPD42275-80 Min	μPD42275-80 Max	μPD42275-10 Min	μPD42275-10 Max	μPD42275-12 Min	μPD42275-12 Max	Unit	Test Conditions
Switching Characteristics (cont)									
Serial output hold time after SC high	t_{SOH}	5		7		7		ns	
$\overline{SOE}$ low to serial output setup delay	t_{SOO}	5		5		5		ns	
Timing Requirements									
Random read or write cycle time	t_{RC}	160		190		220		ns	(Note 11)
Read-write/read-modify-write cycle time	t_{RWC}	220		255		295		ns	(Note 11)
Fast-page cycle time	t_{PC}	50		60		70		ns	(Note 11)
Fast-page read-write/read-modify-write cycle time	t_{PRWC}	105		125		145		ns	(Note 11)
Rise and fall transition time	t_T	3	50	3	50	3	50	ns	(Notes 3 and 10)
$\overline{RAS}$ precharge time	t_{RP}	70		80		90		ns	
$\overline{RAS}$ pulse width	t_{RAS}	80	10,000	100	10,000	120	10,000	ns	
Fast-page $\overline{RAS}$ pulse width	t_{RASP}	80	100,000	100	100,000	120	100,000	ns	
$\overline{RAS}$ hold time	t_{RSH}	20		25		30		ns	
$\overline{CAS}$ precharge time (nonpage cycle)	t_{CPN}	10		10		15		ns	
Fast-page $\overline{CAS}$ precharge time	t_{CP}	10		10		15		ns	
$\overline{CAS}$ pulse width	t_{CAS}	25	10,000	30	10,000	35	10,000	ns	
$\overline{CAS}$ hold time	t_{CSH}	80		100		120		ns	
$\overline{RAS}$ to $\overline{CAS}$ delay time	t_{RCD}	22	60	25	75	25	90	ns	(Note 4)
$\overline{RAS}$ to $\overline{CAS}$ delay time, mask register read cycle	t_{RCD}	22	55	25	70	25	85	ns	(Note 14)
$\overline{CAS}$ high to $\overline{RAS}$ low precharge time	t_{CRP}	10		10		10		ns	(Note 12)
$\overline{RAS}$ high to $\overline{CAS}$ low precharge time	t_{RPC}	0		0		0		ns	
$\overline{RAS}$ low to SC high delay	t_{RSD}	85		105		125		ns	(Note 18)
$\overline{CAS}$ low to SC high delay	t_{CSD}	45		55		65		ns	(Notes 16 and 18)
Address to SC high delay	t_{ASD}	55		65		75		ns	(Notes 16 and 18)
Row address setup time	t_{ASR}	0		0		0		ns	
Row address hold time	t_{RAH}	12		12		15		ns	
Column address setup time	t_{ASC}	0		0		0		ns	
Column address hold time	t_{CAH}	15		20		25		ns	
$\overline{RAS}$ to column address delay time	t_{RAD}	17		17		20		ns	(Note 9)
Column address to $\overline{RAS}$ lead time	t_{RAL}	45		55		65		ns	
Read command setup time	t_{RCS}	0		0		0		ns	
Read command hold time after $\overline{RAS}$ high	t_{RRH}	0		0		0		ns	(Note 6)
Read command hold time after $\overline{CAS}$ high	t_{RCH}	0		0		0		ns	(Note 6)

AC Characteristics (cont)

Parameter	Symbol	μPD42275-80 Min	μPD42275-80 Max	μPD42275-10 Min	μPD42275-10 Max	μPD42275-12 Min	μPD42275-12 Max	Unit	Test Conditions
Timing Requirements (cont)									
Write command setup time	t_{WCS}	0		0		0		ns	(Note 7)
Write command hold time	t_{WCH}	15		20		25		ns	
Write command pulse width	t_{WP}	15		20		25		ns	(Note 13)
Write command to $\overline{RAS}$ lead time	t_{RWL}	30		30		35		ns	
Write command to $\overline{CAS}$ lead time	t_{CWL}	30		30		35		ns	
Data-in setup time	t_{DS}	0		0		0		ns	(Note 8)
Data-in hold time	t_{DH}	15		20		25		ns	(Note 8)
Column address to $\overline{WE}$ delay	t_{AWD}	70		85		100		ns	(Note 7)
$\overline{CAS}$ to $\overline{WE}$ delay	t_{CWD}	45		55		65		ns	(Note 7)
$\overline{RAS}$ to $\overline{WE}$ delay	t_{RWD}	105		130		155		ns	(Note 7)
$\overline{OE}$ high to data-in setup delay	t_{OED}	20		25		30		ns	
$\overline{OE}$ high hold time after $\overline{WE}$ low	t_{OEH}	20		25		30		ns	
$\overline{CAS}$ before $\overline{RAS}$ refresh setup time	t_{CSR}	0		0		0		ns	
$\overline{CAS}$ before $\overline{RAS}$ refresh hold time	t_{CHR}	12		12		15		ns	
Refresh interval	t_{REF}		8		8		8	ms	Addresses A_0 through A_8
$\overline{DT}$ low setup time	t_{DLS}	0		0		0		ns	
$\overline{DT}$ low hold time after $\overline{RAS}$ low, serial port active	t_{RDH}	65		80		95		ns	(Note 15)
$\overline{DT}$ low hold time after $\overline{RAS}$ low, serial port in standby, split data transfer	t_{RDHS}	12		12		15		ns	(Notes 16 and 18)
$\overline{DT}$ low hold time after $\overline{CAS}$ low	t_{CDH}	25		30		35		ns	(Note 15)
$\overline{DT}$ low hold time after address	t_{ADD}	35		40		45		ns	(Note 15)
SC high to $\overline{CAS}$ low delay	t_{SSC}	10		10		10		ns	(Notes 16 and 18)
SC high to $\overline{DT}$ high delay	t_{SDD}	0		0		0		ns	(Note 15)
SC low hold time after $\overline{DT}$ high	t_{SDH}	15		20		25		ns	(Note 15)
SC low hold time after $\overline{RAS}$ high	t_{SDHR}	25		30		40		ns	(Note 16)
Serial clock cycle time	t_{SCC}	25		30		40		ns	(Note 11)
SC pulse width	t_{SCH}	7		10		15		ns	
SC precharge time	t_{SCL}	7		10		15		ns	
$\overline{DT}$ high setup time	t_{DHS}	0		0		0		ns	
$\overline{DT}$ high hold time	t_{DHH}	12		12		15		ns	
$\overline{DT}$ high to $\overline{RAS}$ high delay	t_{DTR}	0		0		0		ns	(Note 15)
$\overline{DT}$ high pulse width	t_{DTP}	25		30		35		ns	
$\overline{OE}$ to $\overline{RAS}$ inactive setup time	t_{OES}	10		10		10		ns	
Write-per-bit setup time	t_{WBS}	0		0		0		ns	
Write-per-bit hold time	t_{WBH}	12		12		15		ns	
Write bit selection setup time	t_{WS}	0		0		0		ns	
Write bit selection hold time	t_{WH}	12		12		15		ns	

AC Characteristics (cont)

Parameter	Symbol	μPD42275-80 Min	μPD42275-80 Max	μPD42275-10 Min	μPD42275-10 Max	μPD42275-12 Min	μPD42275-12 Max	Unit	Test Conditions
Timing Requirements (cont)									
$\overline{SOE}$ pulse width	t_{SOE}	7		10		15		ns	
$\overline{SOE}$ precharge time	t_{SOP}	7		10		15		ns	
DSF_1 setup time from $\overline{RAS}$	t_{FRS1}	0		0		0		ns	
DSF_2 setup time from $\overline{RAS}$	t_{FRS2}	0		0		0		ns	
DSF_1 hold time from $\overline{RAS}$	t_{FRH1}	12		12		15		ns	
DSF_2 hold time from $\overline{RAS}$	t_{FRH2}	12		12		15		ns	
DSF_1 setup time from $\overline{CAS}$	t_{FCS1}	0		0		0		ns	
DSF_1 hold time from $\overline{CAS}$	t_{FCH1}	15		20		25		ns	
Propagation delay time from SC to QSF	t_{PD}		25		30		40	ns	
Propagation delay time from $\overline{DT/OE}$ to QSF	t_{DQD}		35		45		55	ns	(Note 20)
Propagation delay time from $\overline{RAS}$ to QSF	t_{DQR}		45		55		70	ns	(Note 20)
$\overline{RAS}$ to QSF delay time	t_{RQD}		105		135		155	ns	(Notes 16 and 19)
$\overline{CAS}$ to QSF delay time	t_{CQD}		70		85		100	ns	(Notes 16 and 19)

Notes:

(1) All voltages are referenced to GND.

(2) An initial pause of 100 μs is required after power-up, followed by any eight $\overline{RAS}$ cycles, before proper device operation is achieved.

(3) See figures 3 and 4 for reference voltages and figures 5 and 6 for output loads.

(4) Operation within the t_{RCD} (max) limit ensures that t_{RAC} (max) can be met. The t_{RCD} (max) limit is specified as a reference point only. If t_{RCD} is greater than the specified t_{RCD} (max) limit, access time is controlled exclusively by t_{CAC} or t_{AA}.

(5) An output disable time defines the time at which the output achieves the open-circuit condition and is not referenced to output voltage levels.

(6) Either t_{RRH} or t_{RCH} must be satisfied for a read cycle.

(7) t_{WCS}, t_{CWD}, and t_{RWD} are restrictive operating parameters in read-write and read-modify-write cycles only. If $t_{WCS} \geq t_{WCS}$ (min), the cycle is an early write cycle and the data output will remain open-circuit throughout the entire cycle. If $t_{CWD} \geq t_{CWD}$ (min) and $t_{RWD} \geq t_{RWD}$ (min), the cycle is a read-write cycle and the data output will contain data read from the selected cell. If neither of the above conditions is met, the condition of the data output (at access time and until $\overline{CAS}$ returns to V_{IH}) is indeterminate.

(8) These parameters are referenced to the falling edge of $\overline{CAS}$ in early write cycles and to the falling edge of (WB/)WE in delayed write or read-modify-write cycles.

(9) Assumes that t_{RAD} (min) = t_{RAH} (min) + typical t_T of 5 ns.

(10) V_{IH} (min) and V_{IL} (max) are reference levels for measuring the timing of input signals. Additionally, transition times are measured between V_{IH} and V_{IL}.

(11) The minimum specifications are used only to indicate the cycle time at which proper operation over the full temperature range (T_A = 0 to +70°C) is assured.

(12) The t_{CRP} requirement is applicable for $\overline{RAS}/\overline{CAS}$ cycles preceded by any cycle.

(13) Parameter t_{WP} is applicable for a delayed write cycle such as a read-write/read-modify-write cycle. For early write operation, both t_{WCS} and t_{WCH} must be met.

(14) Only for mask register read operation during register read cycles.

(15) For real-time data transfer operation (data transfer with $\overline{SC}$ active).

(16) For read data transfers with serial port in standby.

(17) Ac measurements assume t_T = 5 ns.

(18) For split data transfer cycles.

(19) If $t_{CDH} \leq t_{CDH}$ (min) or $t_{RDHS} \leq t_{RDH}$ (min), then the delay time for the switching of QSF is determined by t_{RQD} or t_{CQD}, whichever occurs later.

(20) If $t_{CDH} \geq t_{CDH}$ (min) and $t_{RDHS} \geq t_{RDH}$ (min), then the switching delay time of QSF is determined by t_{DQD} or t_{DQR}, whichever occurs first.

Figure 3. Input Timing

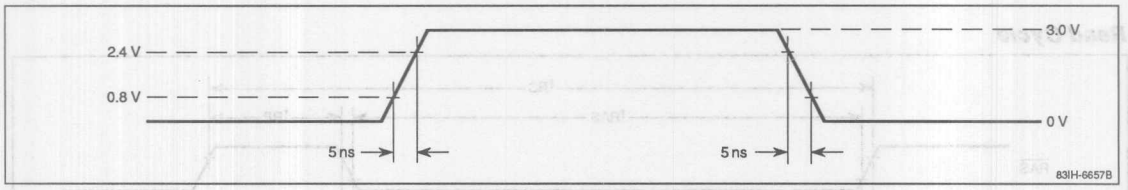


Figure 4. Output Timing

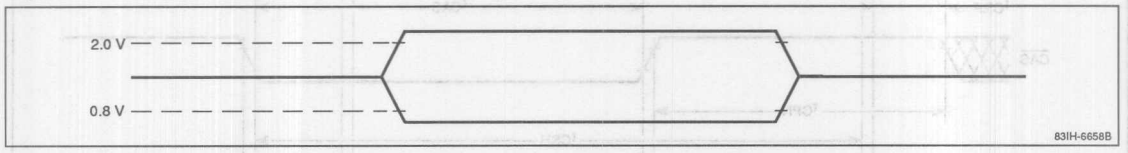


Figure 5. Output Load in Random Access Port

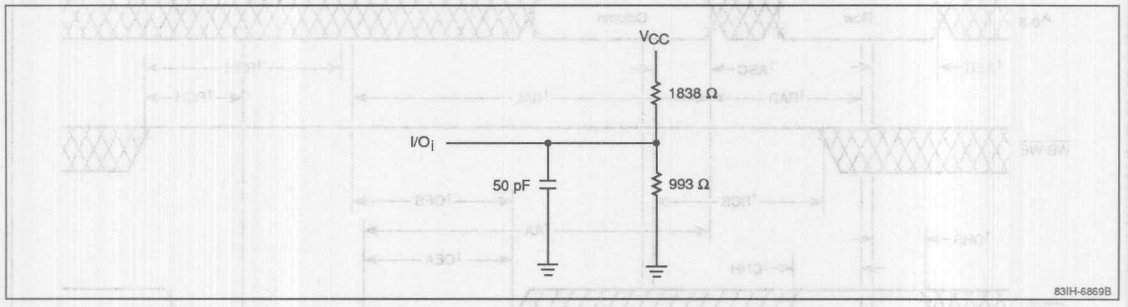
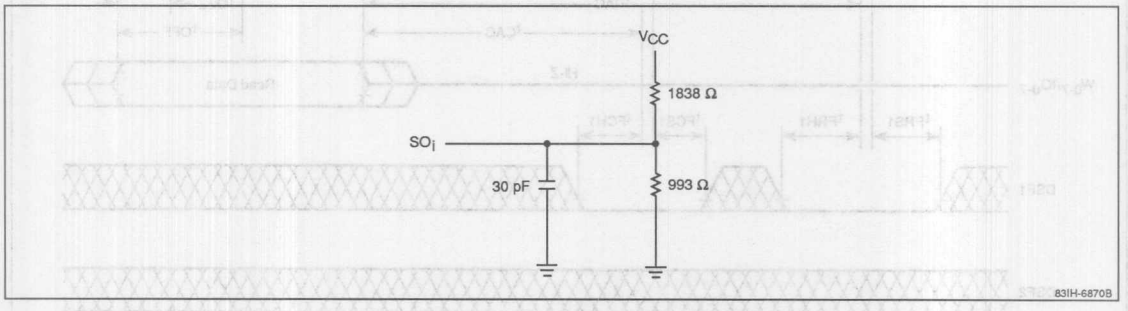
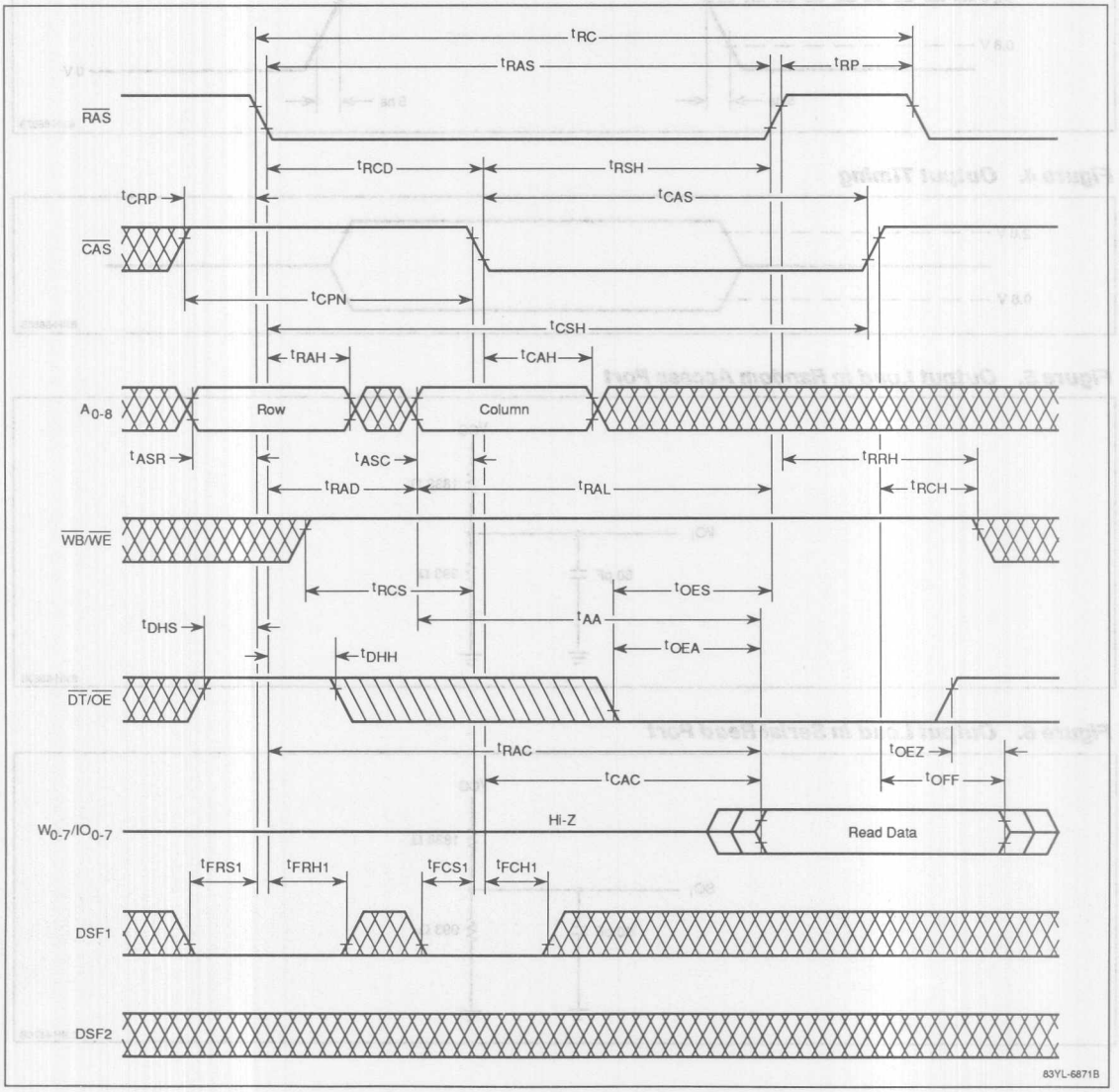


Figure 6. Output Load in Serial Read Port



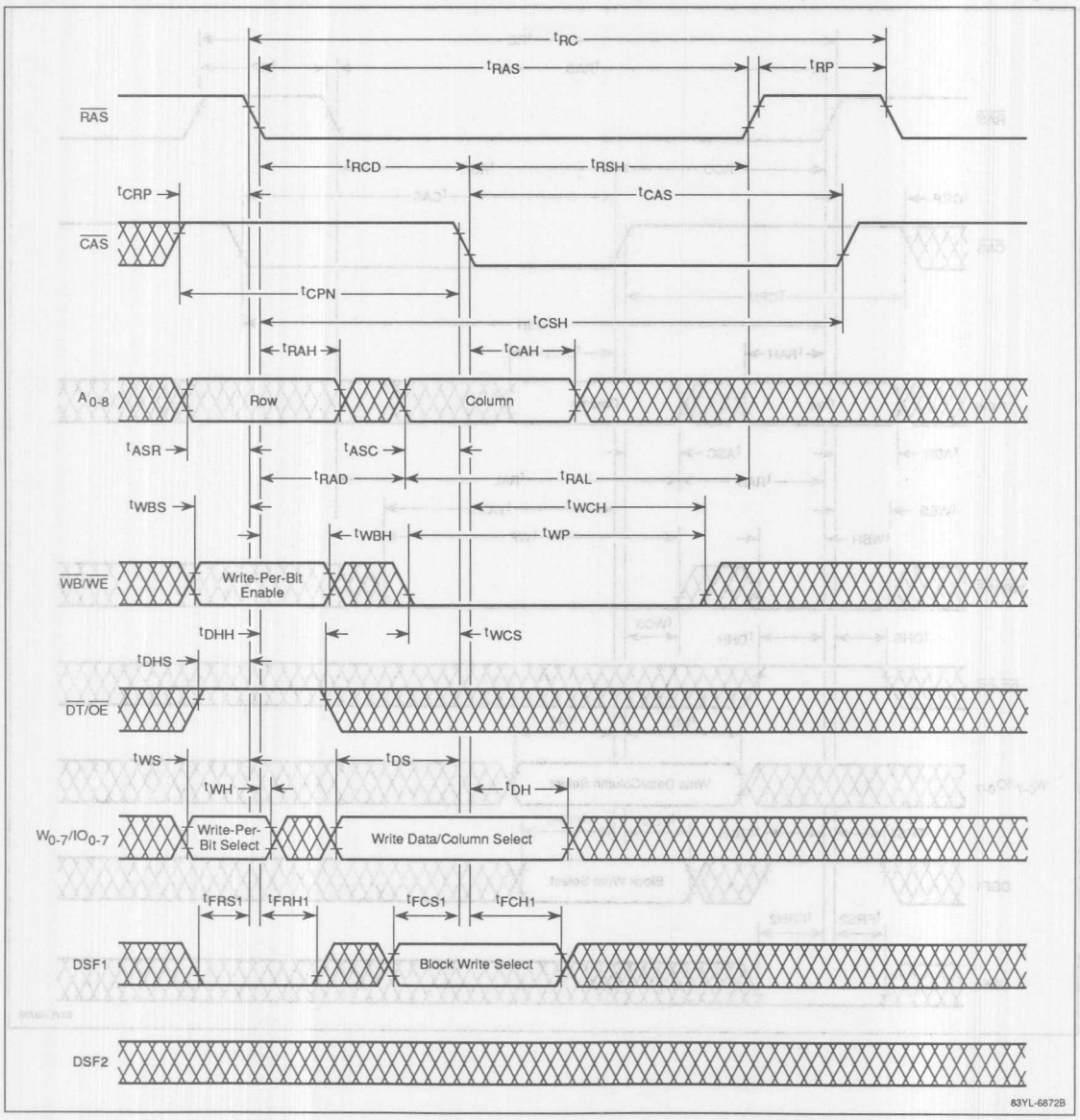
Timing Waveforms

Read Cycle



Timing Waveforms (cont)

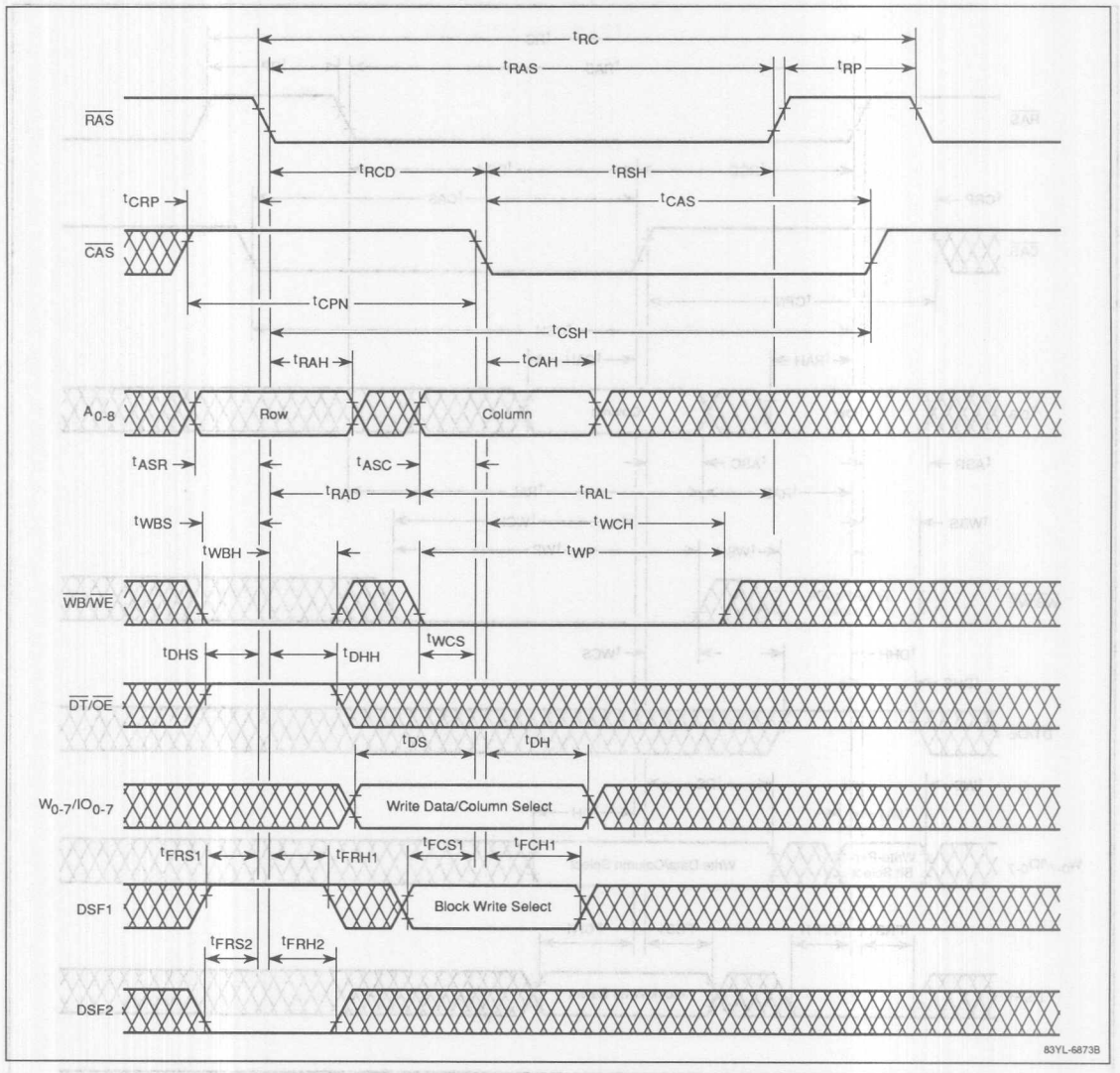
Early Write Cycle and Early Block Write Cycle



3

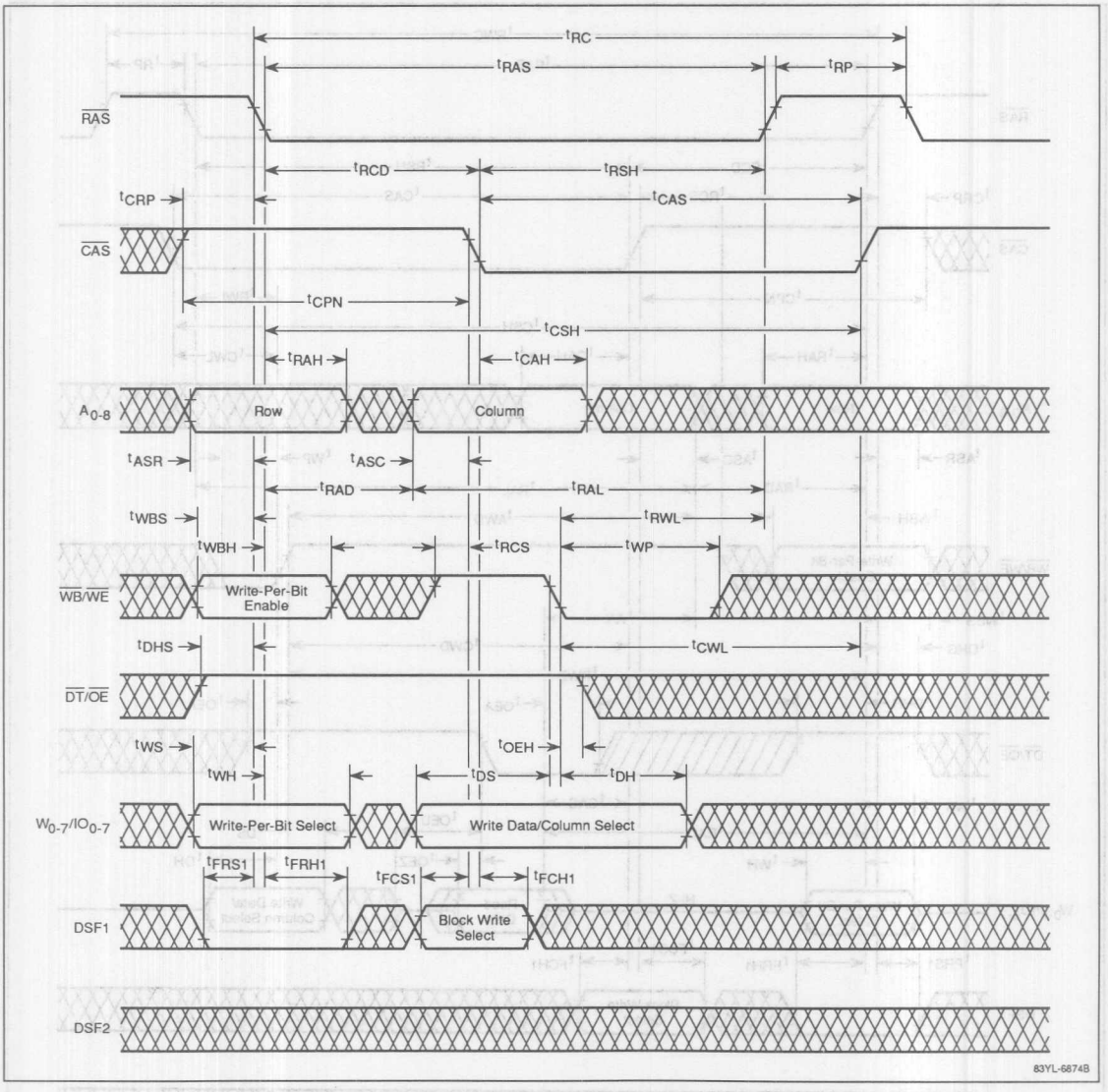
Timing Waveforms (cont)

Early Write Cycle and Early Block Write Cycle With Old Mask



Timing Waveforms (cont)

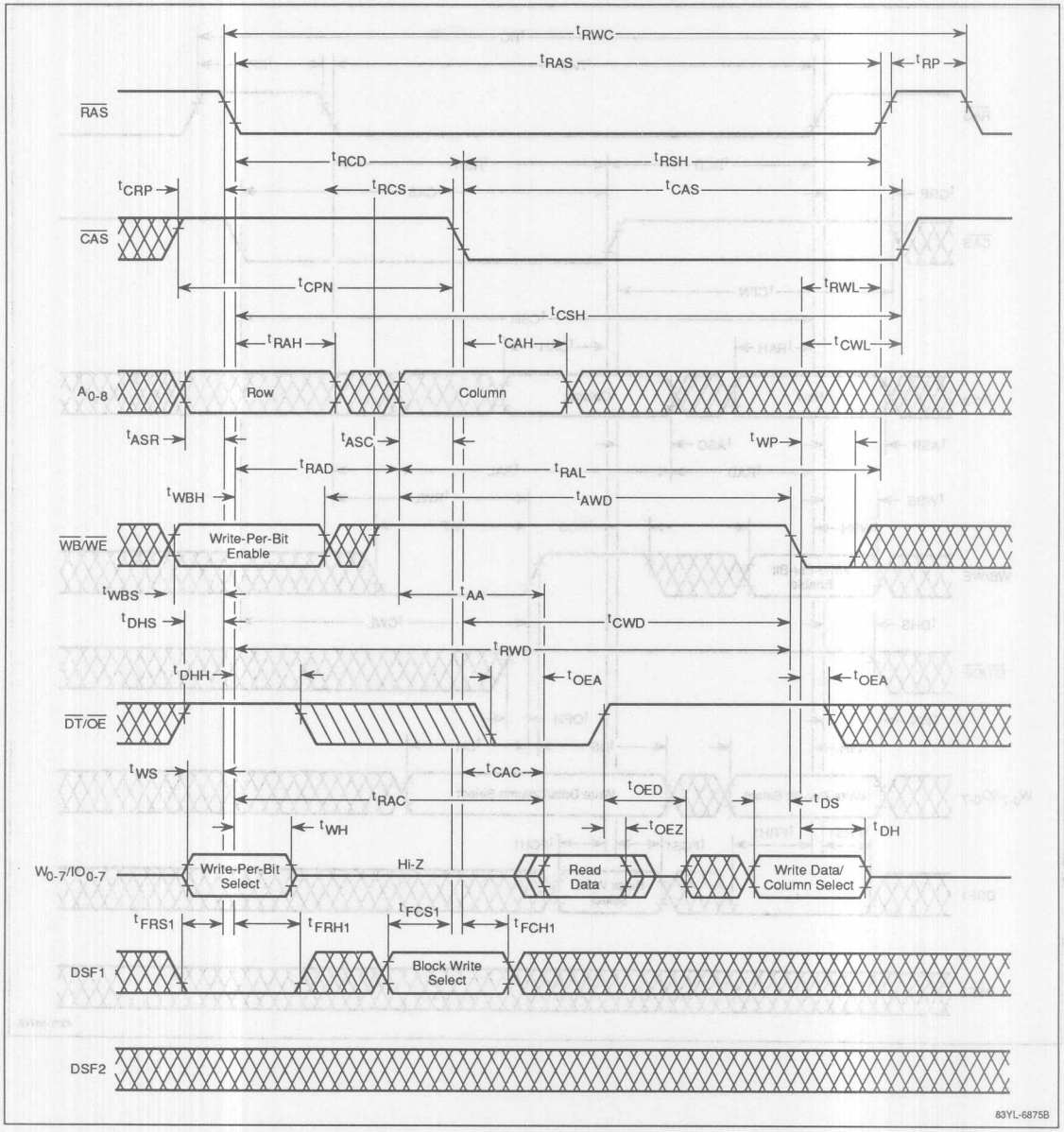
Late Write Cycle and Late Block Write Cycle



3

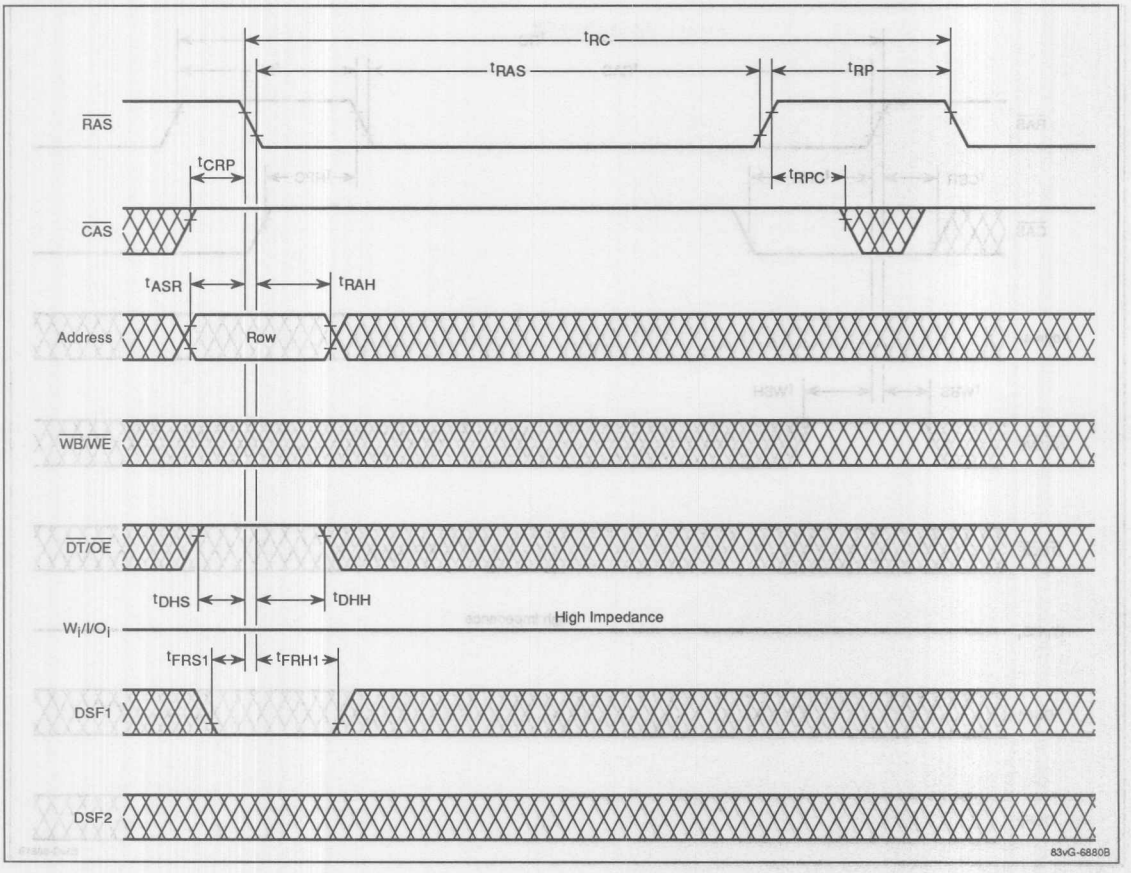
Timing Waveforms (cont)

Read-Write/Read-Modify-Write Cycle



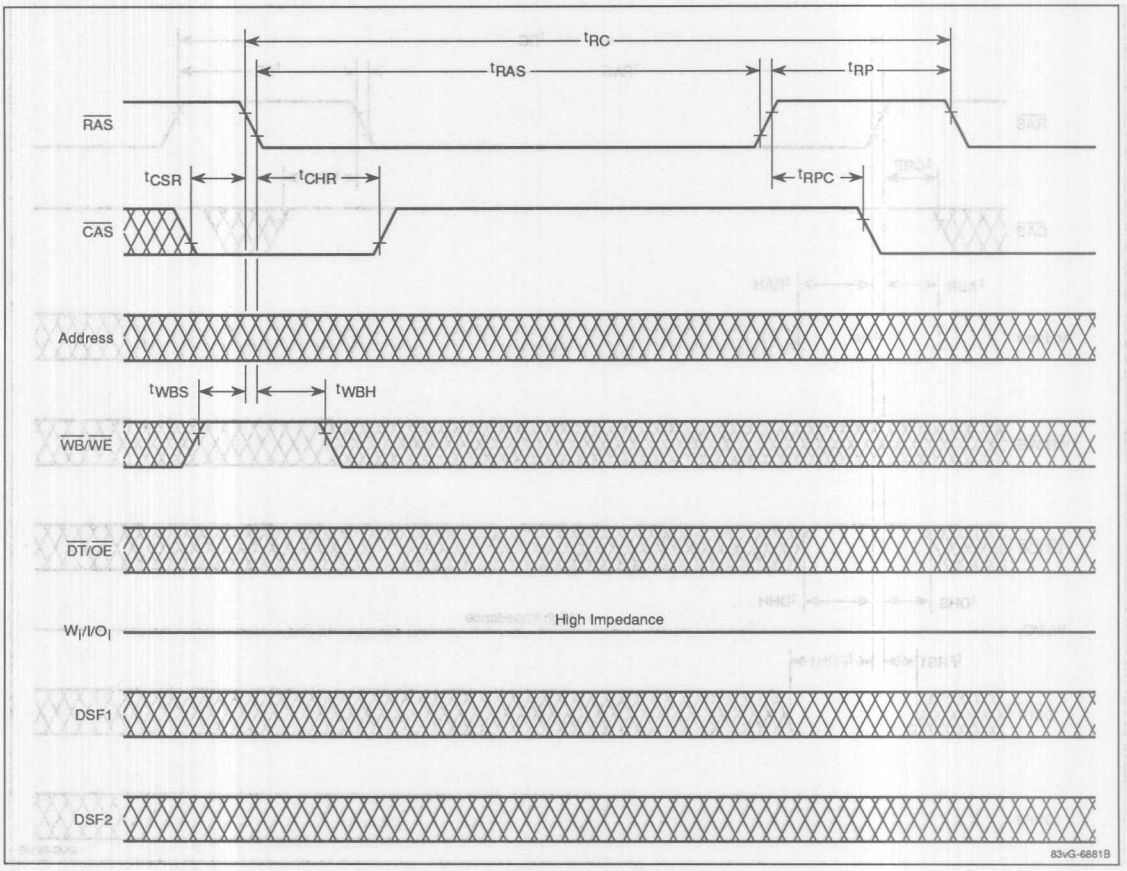
Timing Waveforms (cont)

RAS-Only Refresh Cycle



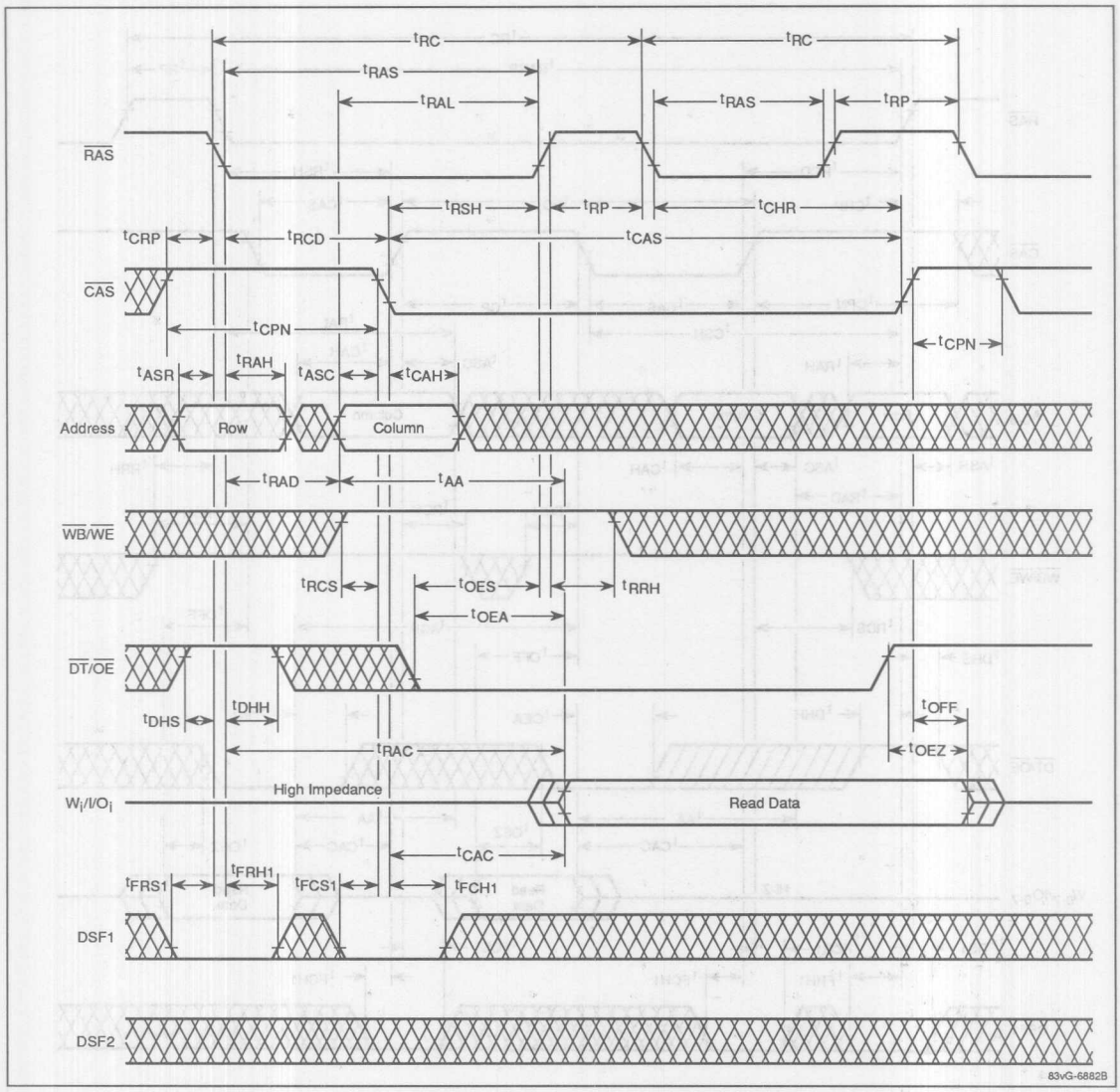
Timing Waveforms (cont)

$\overline{CAS}$ Before $\overline{RAS}$ Refresh Cycle



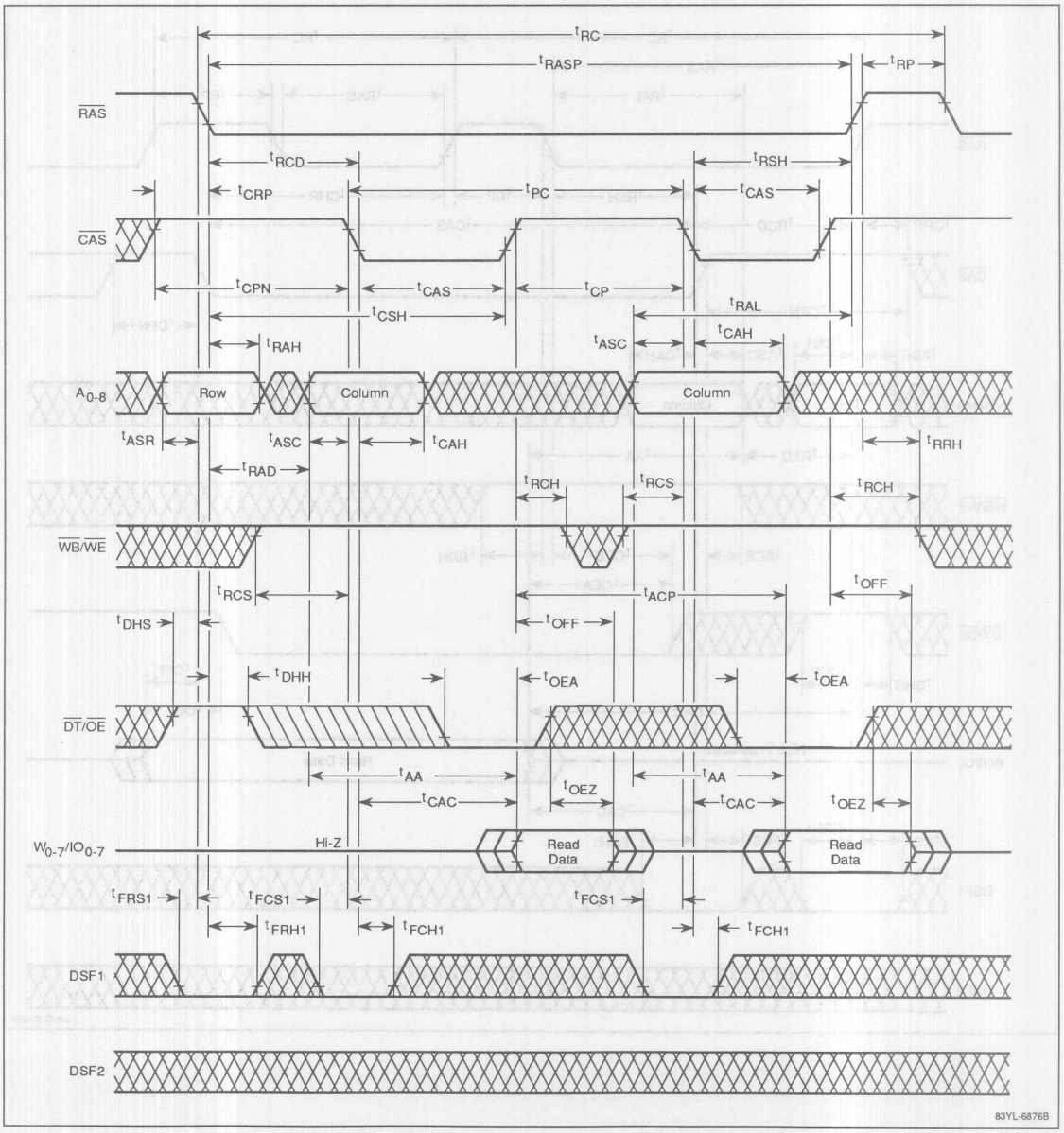
Timing Waveforms (cont)

Hidden Refresh Cycle



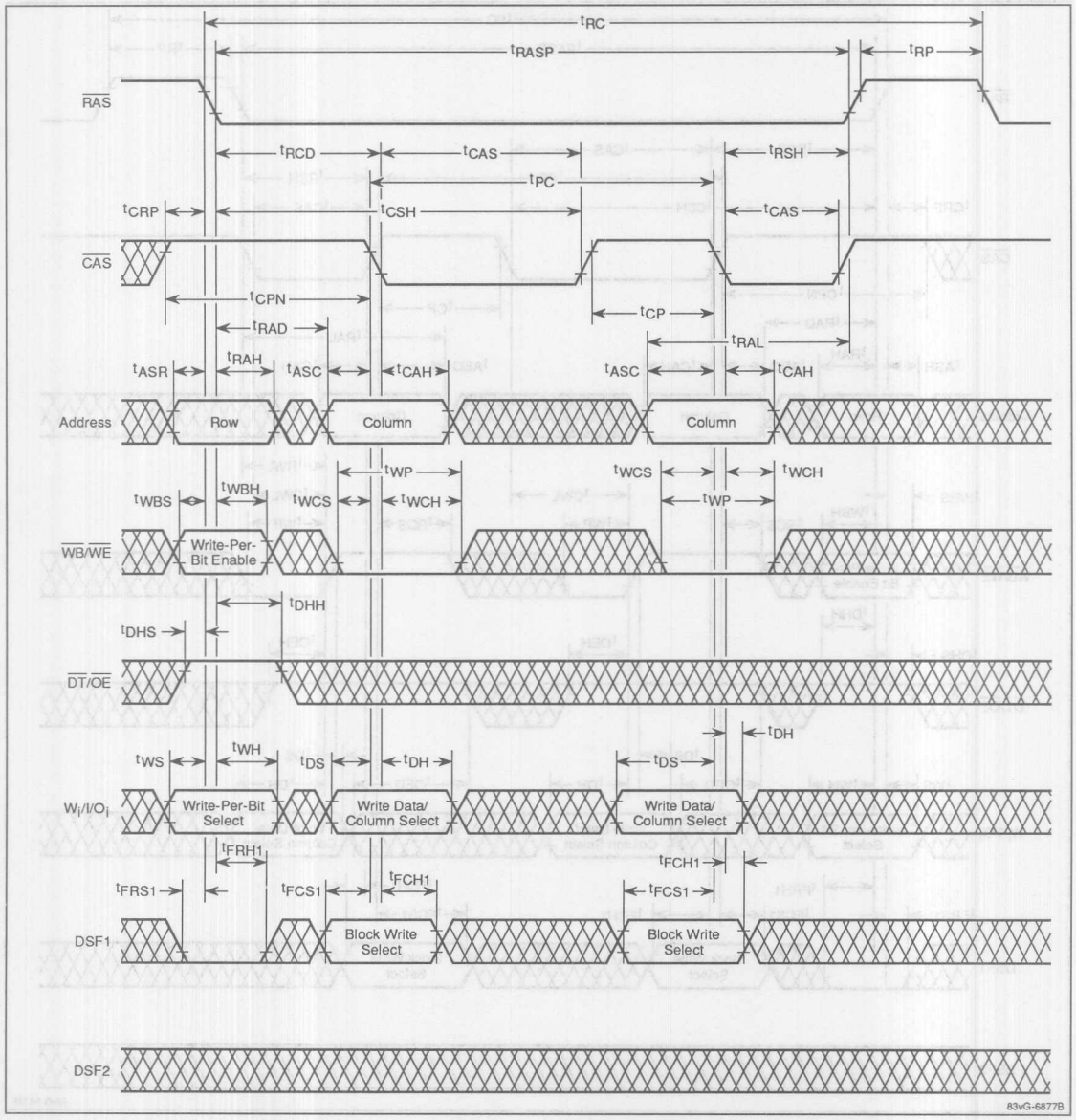
Timing Waveforms (cont)

Fast-Page Read Cycle



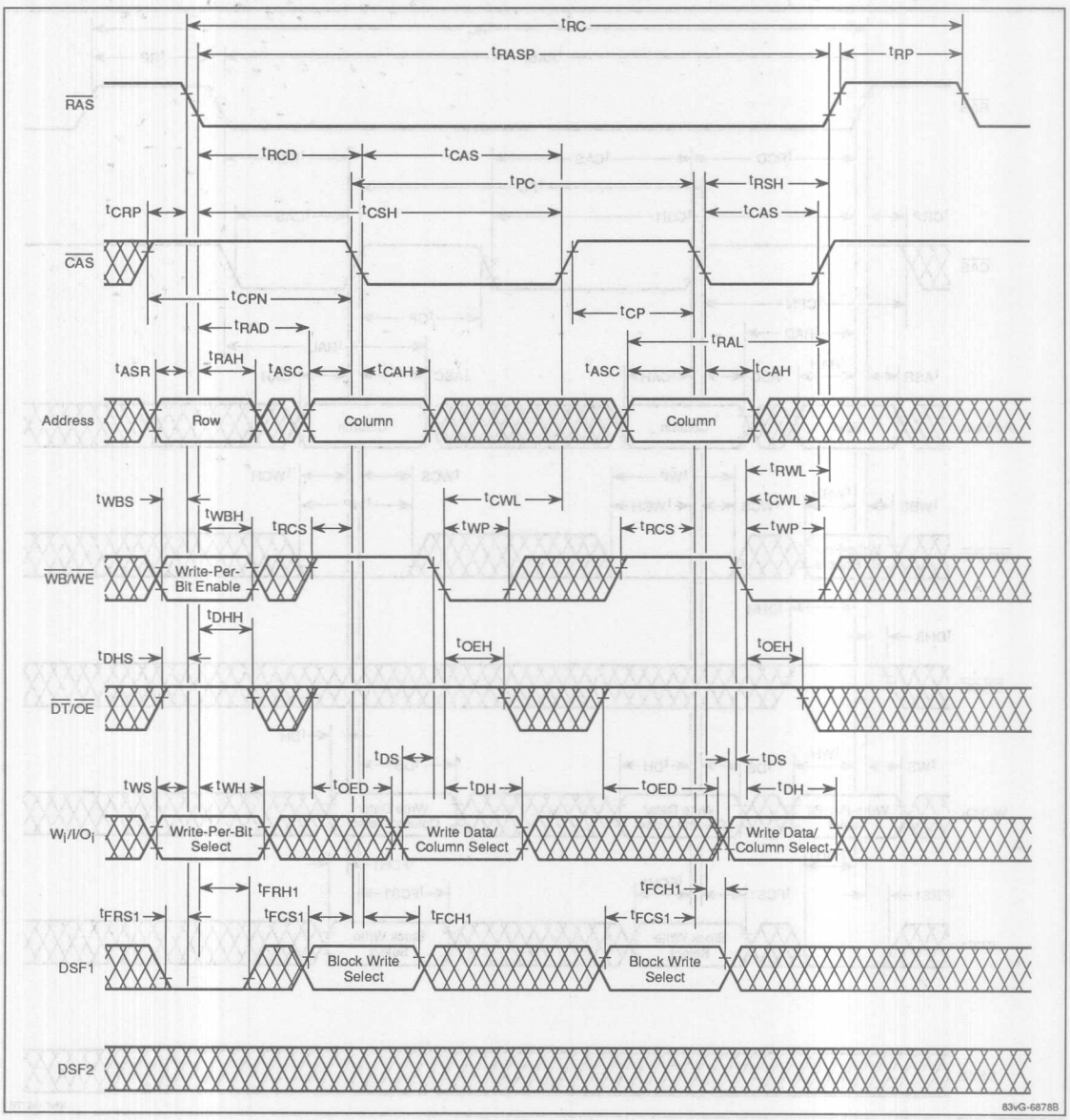
Timing Waveforms (cont)

Fast-Page Early Write Cycle and Fast-Page Early Block Write Cycle



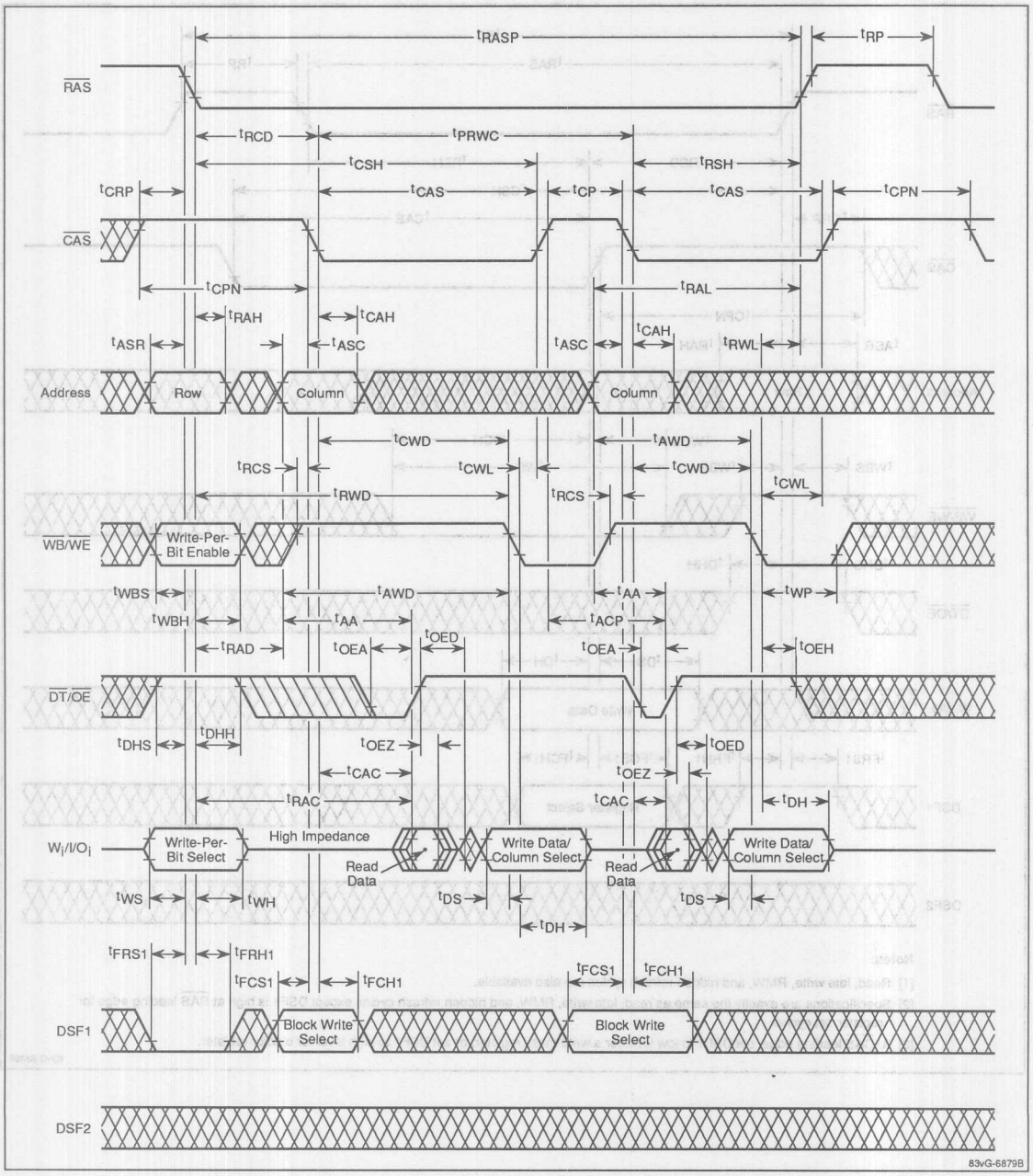
Timing Waveforms (cont)

Fast-Page Late Write Cycle and Fast-Page Late Block Write Cycle



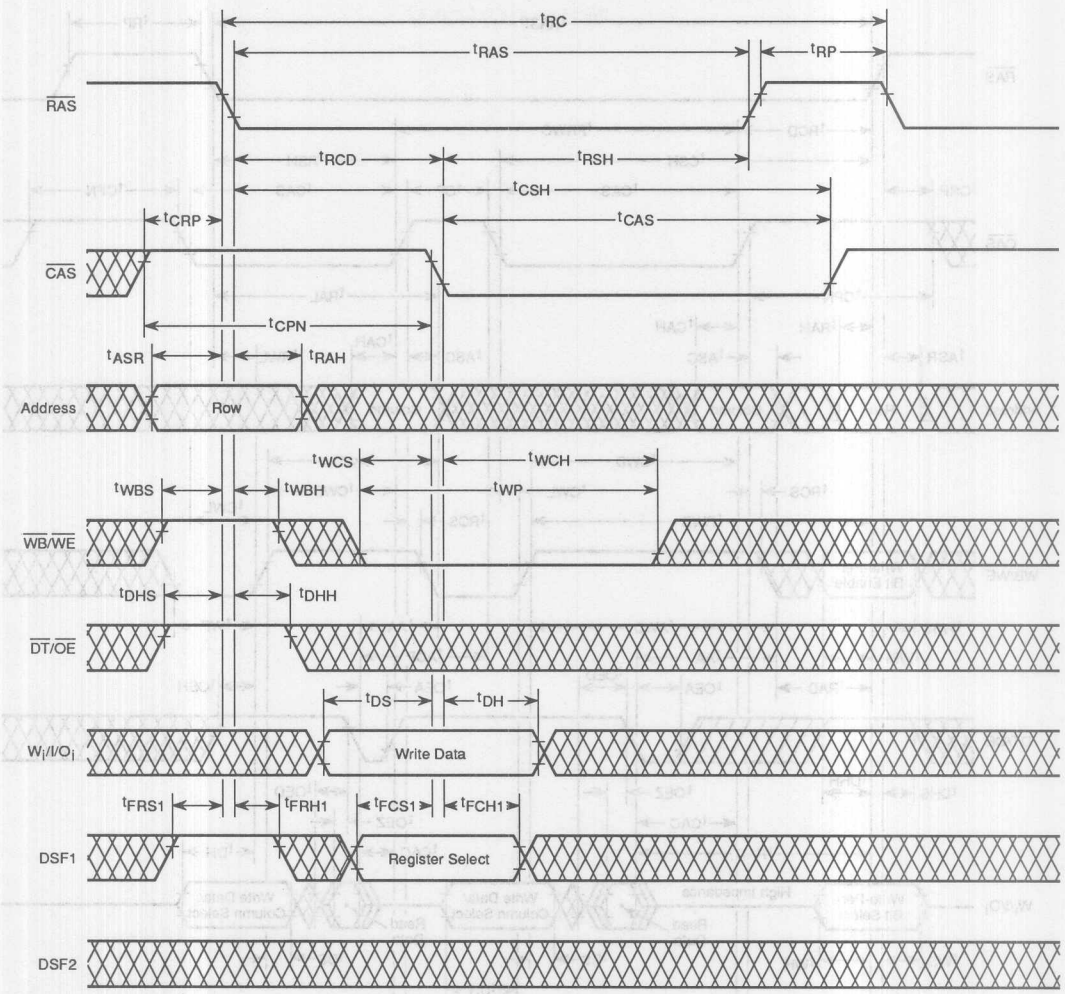
Timing Waveforms (cont)

Fast-Page Read-Modify-Write Cycle



Timing Waveforms (cont)

Color Register Set Cycle



Notes:

[1] Read, late write, RMW, and hidden refresh cycles are also available.

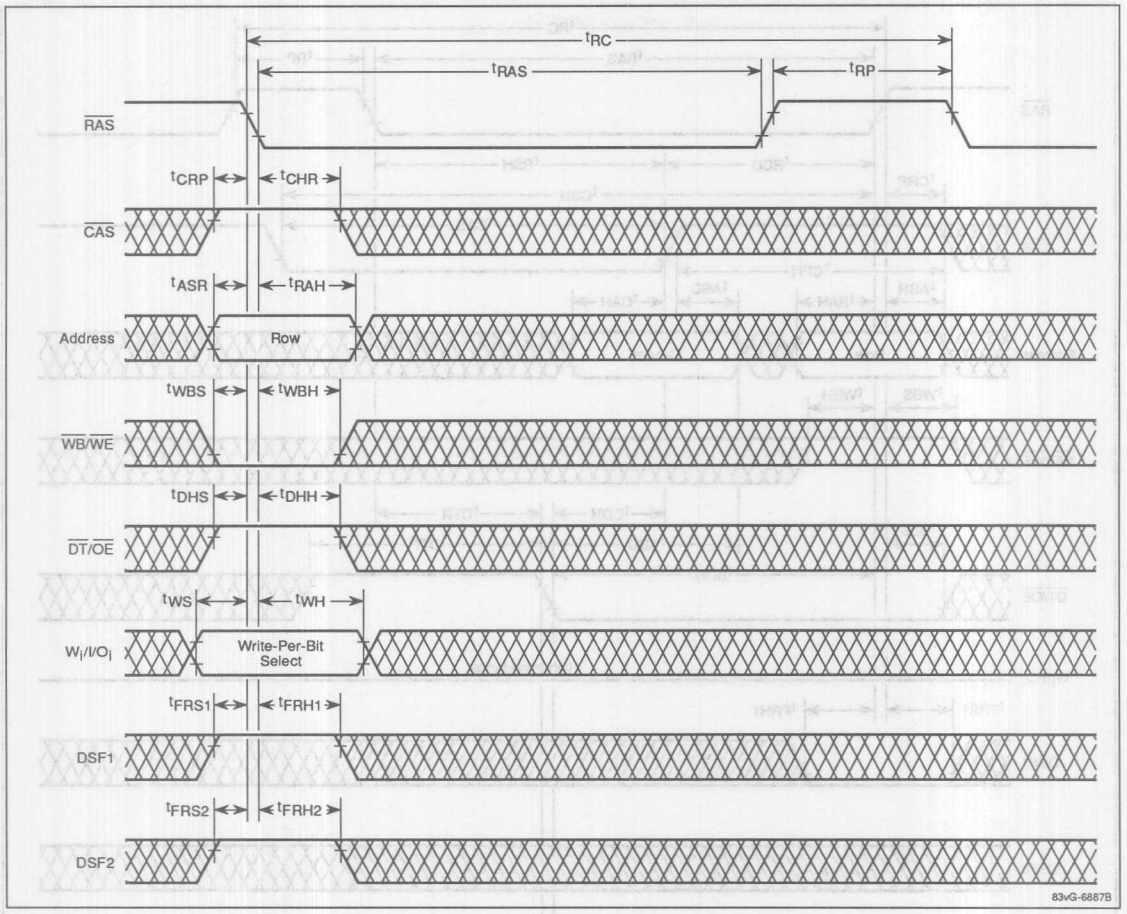
[2] Specifications are exactly the same as read, late write, RMW, and hidden refresh cycles except DSF1 is high at $\overline{RAS}$ leading edge for register set cycles

[3] At $\overline{CAS}$ leading edge, set DSF1 to low level for a write mask register, or set DSF1 to high level for a color register.

83vG-6886B

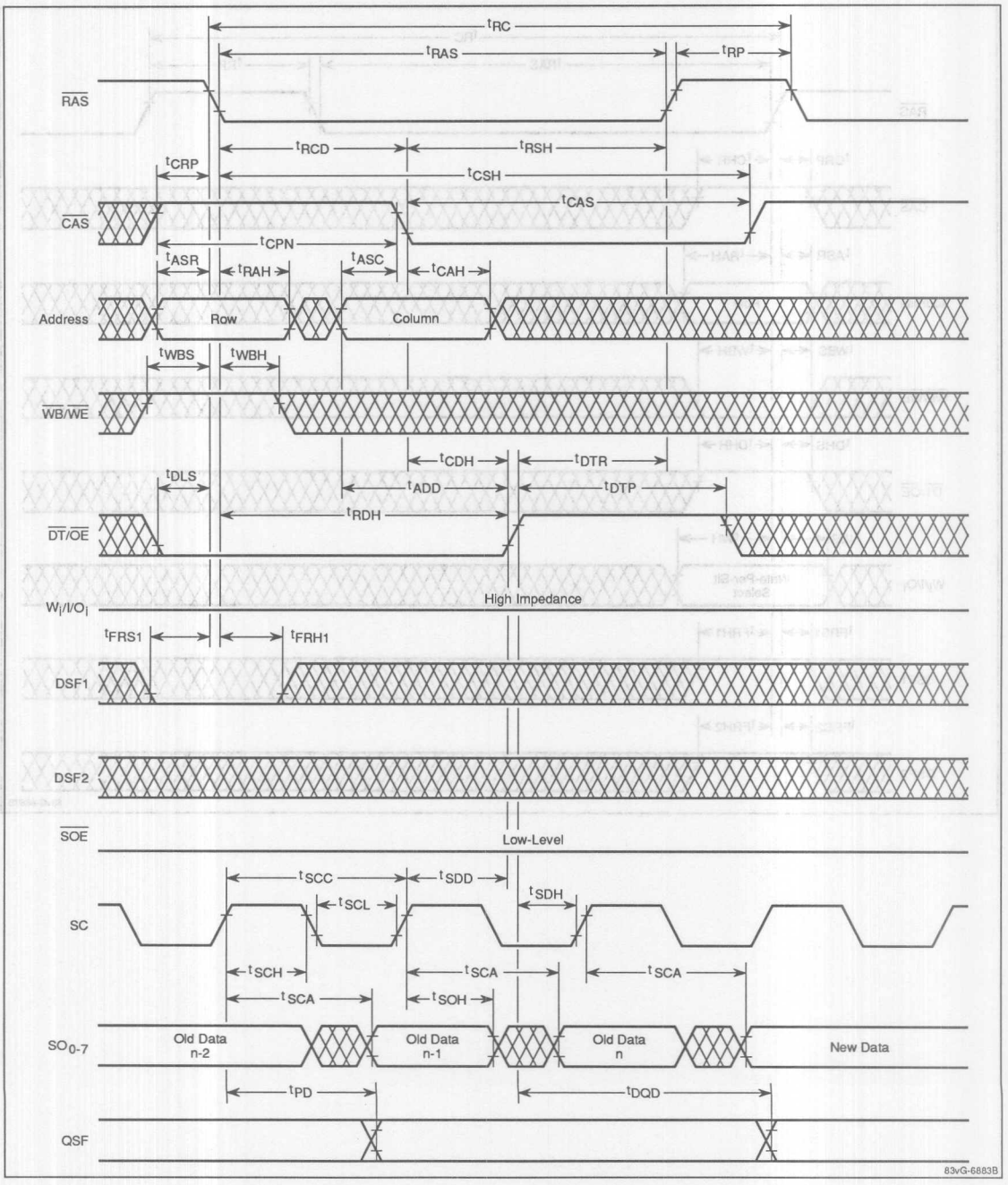
Timing Waveforms (cont)

Flash Write Cycle



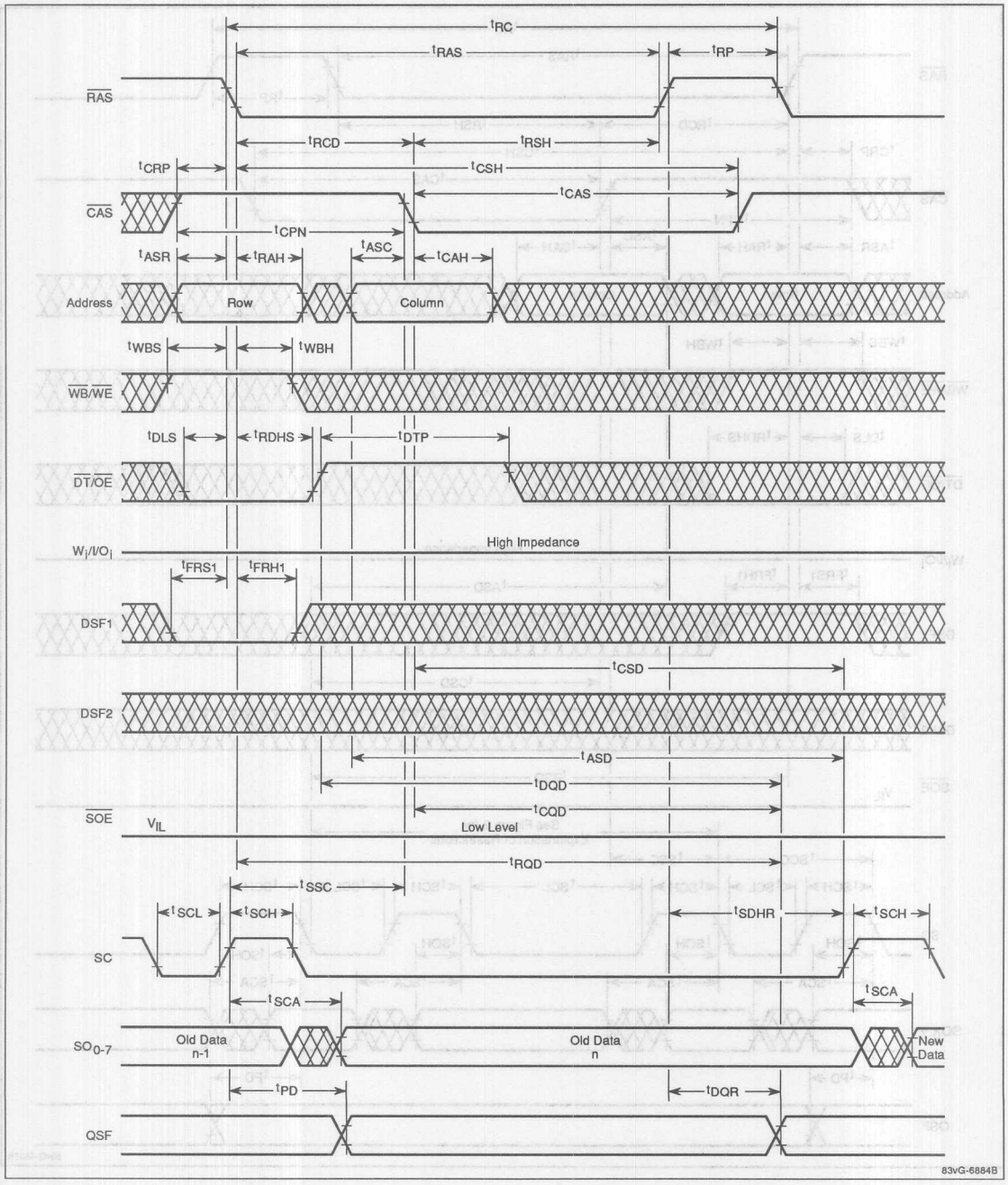
Timing Waveforms (cont)

Data Transfer Cycle with Serial Port Active



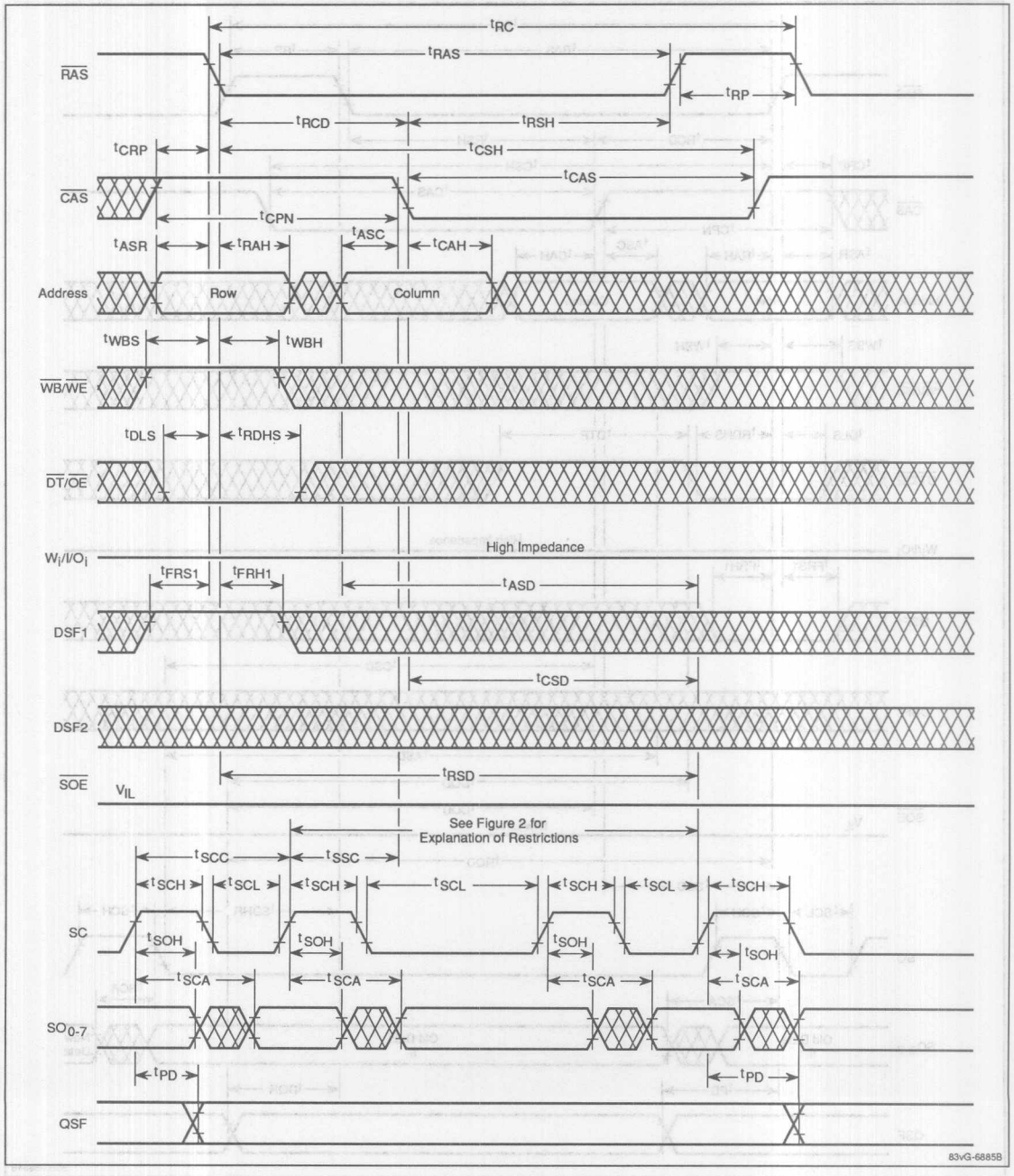
Timing Waveforms (cont)

Data Transfer Cycle with Serial Port in Standby



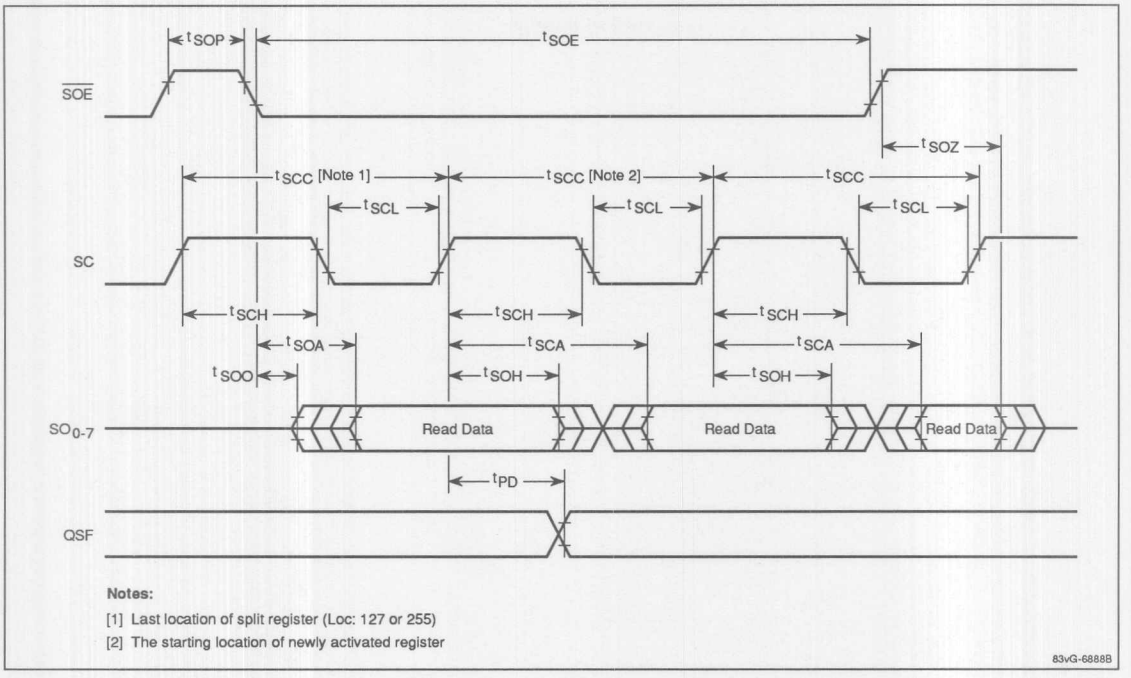
Timing Waveforms (cont)

Split Read Data Transfer Cycle



Timing Waveforms (cont)

Serial Read Cycle

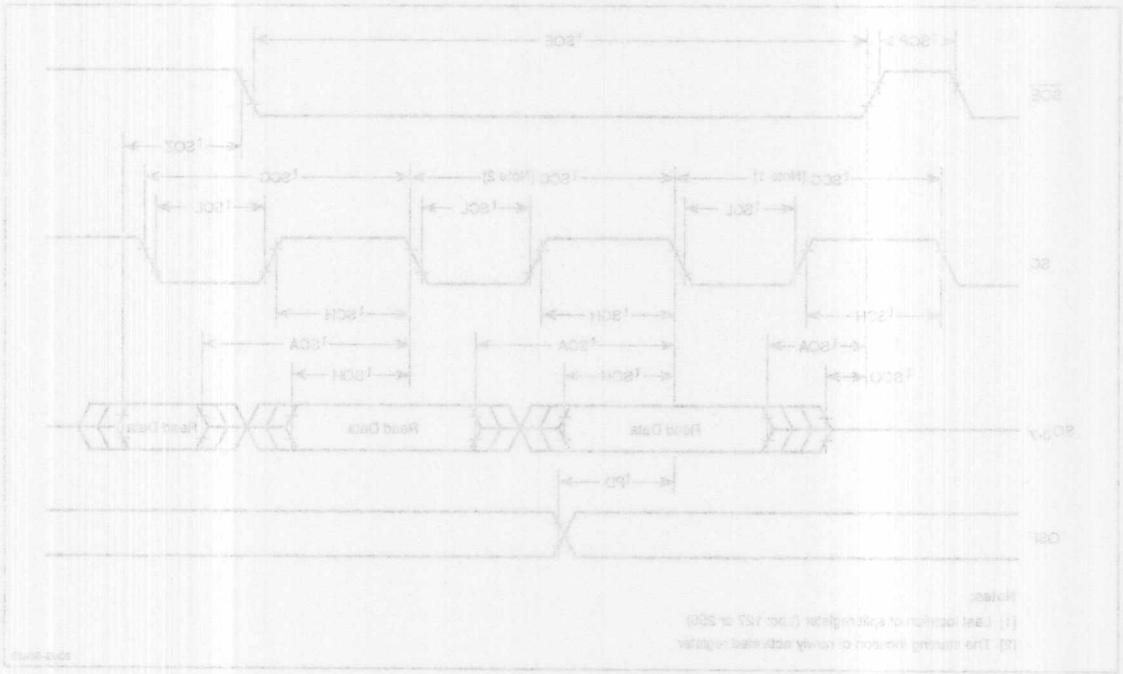


Notes:

[1] Last location of split register (Loc: 127 or 255)

[2] The starting location of newly activated register

83vG-6888B



μPD42101
Line Buffer for NTSC TV

Description

The μPD42101 is a 910-word by 8-bit line buffer fabricated with a CMOS silicon-gate process. The device helps to create an NTSC flicker-free television picture (noninterlaced scan conversion) by providing intermediate storage and very high-speed read and write operation.

The μPD42101 can also be used as a digital delay line. The delay length is variable from 10 bits (at maximum clock speed) to 910 bits.

Features

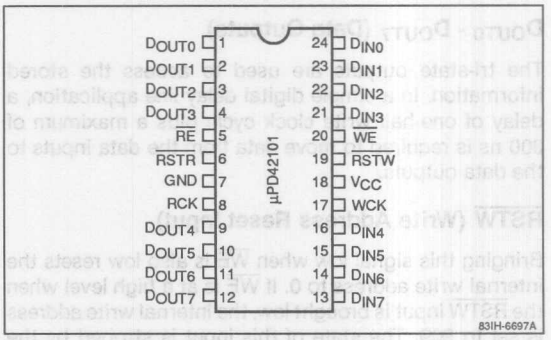
- 910-word x 8-bit organization
- Line buffer for NTSC, $4f_{SC}$ digital television systems
- Asynchronous, simultaneous read/write operation
- 1H (910-bit) delay line capability
- TTL-compatible inputs and outputs
- Three-state outputs
- Single +5-volt power supply
- 24-pin plastic DIP and miniflat packaging

Ordering Information

Part Number		Read Cycle Time (min)	Write Cycle Time (min)	Package
μPD42101	C-3	34 ns	34 ns	24-pin plastic DIP
	C-2	34 ns	69 ns	
	C-1	69 ns	69 ns	
μPD42101	G-3	34 ns	34 ns	24-pin plastic miniflat
	G-2	34 ns	69 ns	
	G-1	69 ns	69 ns	

Pin Configuration

24-Pin Plastic DIP or Miniflat



Pin Identification

Symbol	Function
D_{IN0} - D_{IN7}	Write data inputs
D_{OUT0} - D_{OUT7}	Read data outputs
$\overline{RSTW}$	Write address reset input
$\overline{RSTR}$	Read address reset input
$\overline{WE}$	Write enable input
$\overline{RE}$	Read enable input
WCK	Write clock input
RCK	Read clock input
GND	Ground
V_{CC}	+5-volt power supply

PIN FUNCTIONS

D_{IN0} - D_{IN7} (Data Inputs)

In a digital television application, the digital composite signal, luminance, chrominance, etc. information is written into these inputs.

D_{OUT0} - D_{OUT7} (Data Outputs)

The tri-state outputs are used to access the stored information. In a simple digital delay line application, a delay of one-half write clock cycle plus a maximum of 300 ns is required to move data from the data inputs to the data outputs.

$\overline{RSTW}$ (Write Address Reset Input)

Bringing this signal low when $\overline{WE}$ is also low resets the internal write address to 0. If $\overline{WE}$ is at a high level when the $\overline{RSTW}$ input is brought low, the internal write address is set to 909. The state of this input is strobed by the rising edge of WCK.

$\overline{RSTR}$ (Read Address Reset Input)

This signal is strobed by the rising edge of RCK and resets the internal read address to 0 if $\overline{RE}$ is also low. If $\overline{RE}$ is at a high level when the $\overline{RSTR}$ input is brought low, the internal read address is set to 909.

$\overline{WE}$ (Write Enable Input)

This input controls write operation. If $\overline{WE}$ is low, all write cycles proceed. If $\overline{WE}$ is at a high level, no data is written to storage cells and the write address stops increasing. The state of $\overline{WE}$ is strobed by the rising edge of WCK.

$\overline{RE}$ (Read Enable Input)

This signal is similar to $\overline{WE}$ but controls read operation. If $\overline{RE}$ is at a high level, the data outpus become high impedance and the internal read address stops increasing. The state of $\overline{RE}$ is strobed by the rising edge of RCK.

WCK (Write Clock Input)

All write cycles are executed synchronously with WCK. The states of both $\overline{RSTW}$ and $\overline{WE}$ are strobed by the rising edge of WCK at the beginning of a cycle, and the data inputs are strobed by the rising edge of WCK at the end of a cycle. The internal write address increases with each WCK cycle unless $\overline{WE}$ is at a high level to hold the write address constant. Unless inhibited by $\overline{WE}$, the internal write address will automatically wrap around from 909 to 0 and begin increasing again.

RCK (Read Clock Input)

All read cycles are executed synchronously with RCK. The states of both $\overline{RSTR}$ and $\overline{RE}$ are strobed by the rising edge of RCK at the beginning of a cycle. This same edge of RCK starts internal read operation, and access time is referenced to this edge. The internal read address increases with each RCK cycle unless $\overline{RE}$ is at a high level to hold the read address constant. Unless inhibited by $\overline{RE}$, the internal read address will automatically wrap around from 909 to 0 and begin increasing again.

Absolute Maximum Ratings

Supply voltage, V_{CC}	−1.5 to +7.0 V
Voltages on any input pin, V_I	−1.5 to + 7.0 V
Voltage on any output pin, V_O	−1.5 to +7.0 V
Short-circuit output current, I_{OS}	20 mA
Operating temperature, T_{OPR}	−20 to +70°C
Storage temperature, T_{STG}	−55 to +125°C

Exposure to Absolute Maximum Ratings for extended periods may affect device reliability; exceeding the ratings could cause permanent damage. The device should be operated within the limits specified under DC and AC Characteristics.

Recommended Operating Conditions

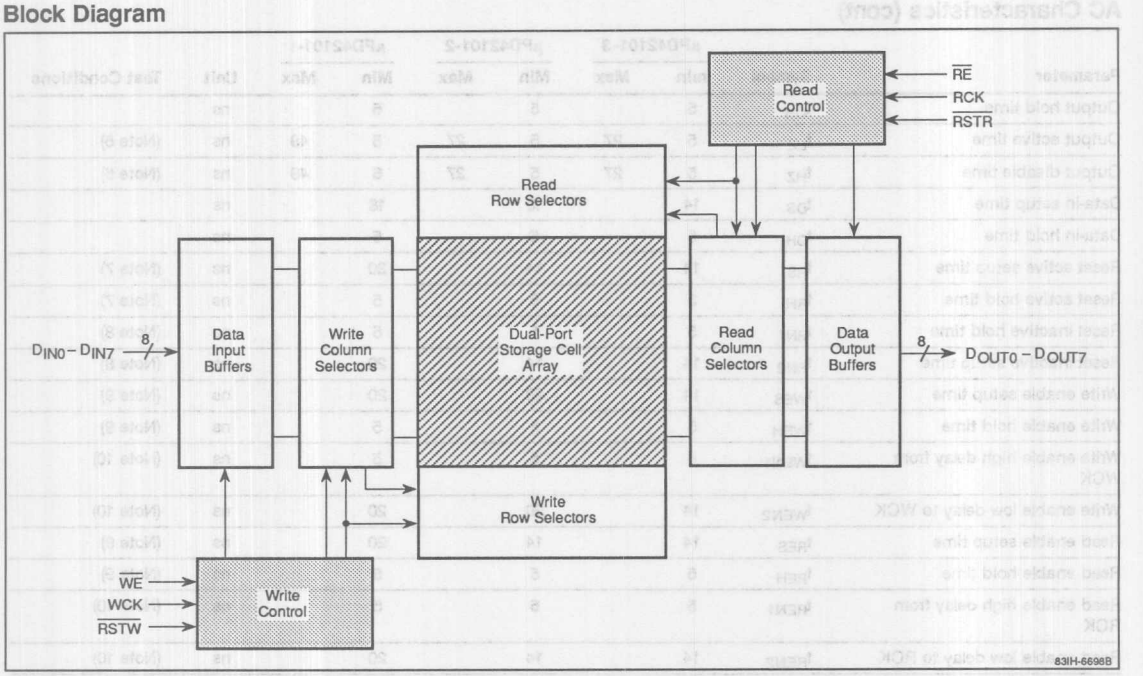
Parameter	Symbol	Min	Typ	Max	Unit
Supply voltage	V_{CC}	4.5	5.0	5.5	V
Input voltage, high	V_{IH}	2.4		5.5	V
Input voltage, low	V_{IL}	−1.5		0.8	V
Operating temperature	T_A	0		70	°C

Capacitance

T_A = 25°C; V_{CC} = +5.0 V ±10%; f = 1 MHz

Parameter	Symbol	Min	Max	Unit	Pins Under Test
Input capacitance	C_I		5	pF	$\overline{WE}$, $\overline{RE}$, WCK, RCK, $\overline{RSTW}$, $\overline{RSTR}$, D_{IN0} - D_{IN7}
Output capacitance	C_O		7	pF	D_{OUT0} - D_{OUT7}

Block Diagram



DC Characteristics

T_A = −20 to +70°C; V_{CC} = +5.0 V ± 10%

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions
Input leakage current	I_I	−10		10	μA	V_{IN} = 0 V to V_{CC}; all other pins not under test = 0 V
Output leakage current	I_O	−10		10	μA	D_{OUT} disabled; V_O = 0 to 5.5 V
Output voltage, high	V_{OH}	2.4			V	I_{OH} = −1 mA
Output voltage, low	V_{OL}			0.4	V	I_{OL} = 2.0 mA

AC Characteristics

T_A = −20 to +70°C; V_{CC} = +5.0 V ± 10%

		μPD42101-3		μPD42101-2		μPD42101-1			
Parameter	Symbol	min	Max	Min	Max	Min	Max	Unit	Test Conditions
Write/read cycle operating current	I_{CC}		70		60		35	mA	t_{WCK} = t_{WCK} (min); t_{RCK} = t_{RCK} (min)
Write clock cycle time	t_{WCK}	34	1090	69	1090	69	1090	ns	
WCK pulse width	t_{WCW}	14		25		25		ns	
WCK precharge time	t_{WCP}	14		25		25		ns	
Read clock cycle time	t_{RCK}	34	1090	34	1090	69	1090	ns	
RCK pulse width	t_{RCW}	14		14		25		ns	
RCK precharge time	t_{RCP}	14		14		25		ns	
Access time	t_{AC}		27		27		49	ns	

AC Characteristics (cont)

Parameter	Symbol	μPD42101-3 min	μPD42101-3 Max	μPD42101-2 Min	μPD42101-2 Max	μPD42101-1 Min	μPD42101-1 Max	Unit	Test Conditions
Output hold time	t_{OH}	5		5		5		ns	
Output active time	t_{LZ}	5	27	5	27	5	49	ns	(Note 5)
Output disable time	t_{HZ}	5	27	5	27	5	49	ns	(Note 5)
Data-in setup time	t_{DS}	14		18		18		ns	
Data-in hold time	t_{DH}	5		5		5		ns	
Reset active setup time	t_{RS}	14		14		20		ns	(Note 7)
Reset active hold time	t_{RH}	5		5		5		ns	(Note 7)
Reset inactive hold time	t_{RN1}	5		5		5		ns	(Note 8)
Reset inactive setup time	t_{RN2}	14		14		20		ns	(Note 8)
Write enable setup time	t_{WES}	14		20		20		ns	(Note 9)
Write enable hold time	t_{WEH}	5		5		5		ns	(Note 9)
Write enable high delay from WCK	t_{WEN1}	5		5		5		ns	(Note 10)
Write enable low delay to WCK	t_{WEN2}	14		20		20		ns	(Note 10)
Read enable setup time	t_{RES}	14		14		20		ns	(Note 9)
Read enable hold time	t_{REH}	5		5		5		ns	(Note 9)
Read enable high delay from RCK	t_{REN1}	5		5		5		ns	(Note 10)
Read enable low delay to RCK	t_{REN2}	14		14		20		ns	(Note 10)
Write disable pulse width	t_{WEW}	0		0		0		ns	(Note 6)
Read disable pulse width	t_{REW}	0		0		0		ns	(Note 6)
Write reset time	t_{RSTW}	0		0		0		ns	(Note 6)
Read reset time	t_{RSTR}	0		0		0		ns	(Note 6)
Transition time	t_T	3	35	3	35	3	35	ns	

Notes:

(1) All voltages are referenced to ground.

(2) After power-up, a read reset cycle and a write reset cycle must be executed before proper device operation is achieved.

(3) Input pulse rise and fall times assume t_T = 5 ns. Input pulse levels = GND to 3 V. Transition times are measured between 3 V and 0 V. See figure 1.

(4) Input timing reference levels = 1.5 V. Output timing reference levels are 0.8 and 2.0 V. See figure 2.

(5) This delay is measured at 200 mV from the steady-state voltage with the load specified in figure 4. Under any conditions, $t_{LZ} \geq t_{HZ}$.

(6) t_{WEW} (max) and t_{REW} (max) must be satisfied by the following equations in 1-line cycle operation:
$t_{WEW} + t_{RSTW} + 910\ (t_{WCK}) \leq 1$ ms
$t_{REW} + t_{RSTR} + 910\ (t_{RCK}) \leq 1$ ms

(7) If either t_{RS} or t_{RH} is less than the specified value, reset operations are not guaranteed.

(8) If either t_{RN1} or t_{RN2} is less than the specified value, internal reset operations may extend to cycles immediately preceding or following the period of desired reset operations.

(9) If either t_{WES} or t_{WEH} (t_{RES} or t_{REH}) is less than the specified value, write (read) disable operations are not guaranteed.

(10) If either t_{WEN1} or t_{WEN2} (t_{REN1} or t_{REN2}) is less than the specified value, internal write (read) disable operations may extend to cycles immediately preceding or following the period of desired disable operations.

(11) Data is guaranteed to remain valid for a minimum of 1 ms after it is written. After this time, the data stored may be discharged, since this device uses a dynamic storage element.

Figure 1. Input Timing

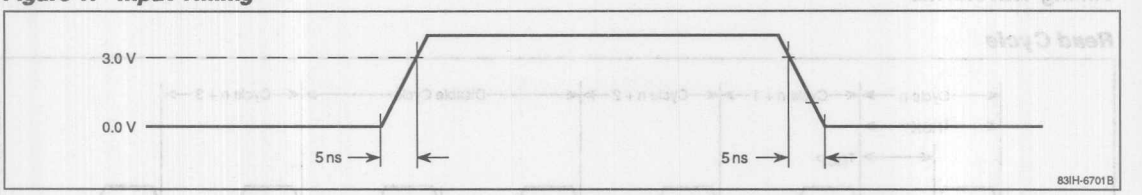
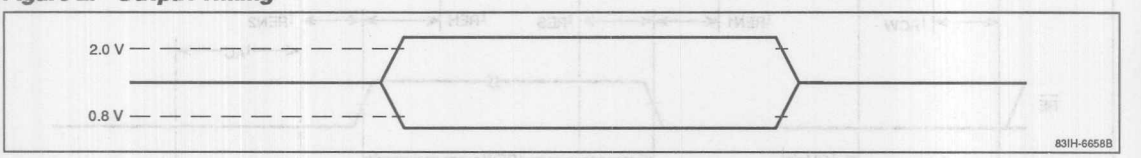


Figure 2. Output Timing



3

Figure 3. Output Load for t_{AC} and t_{OH}

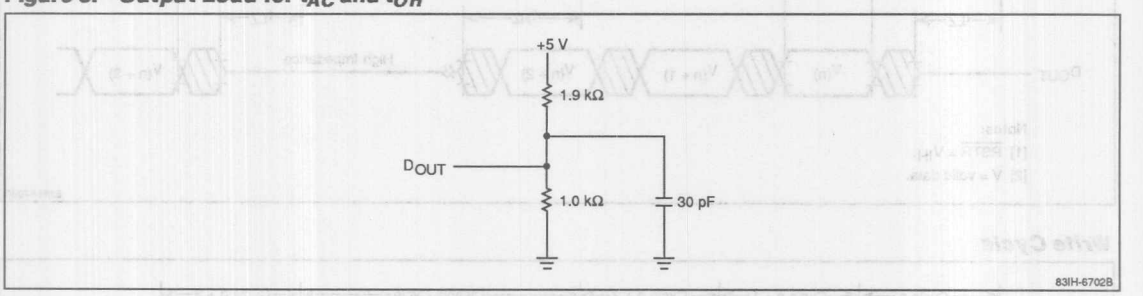
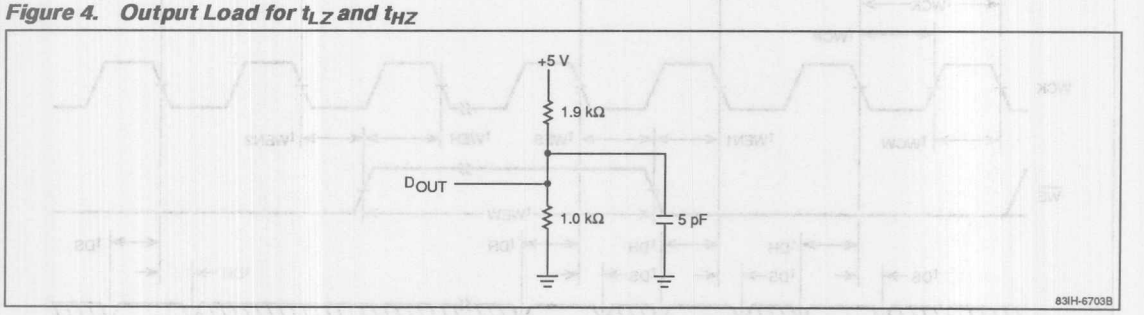
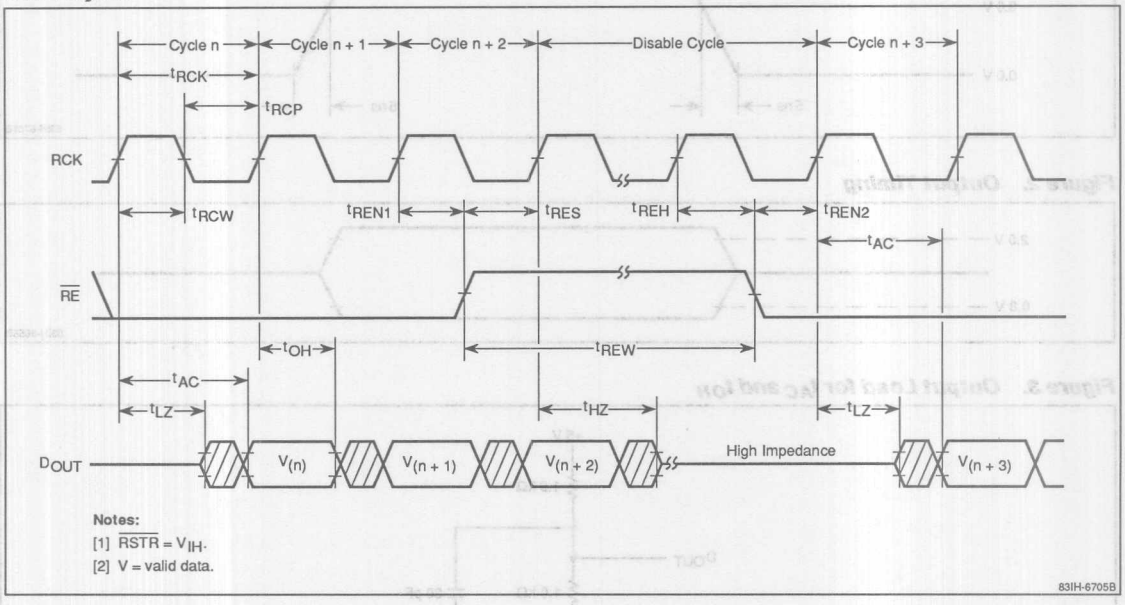


Figure 4. Output Load for t_{LZ} and t_{HZ}



Timing Waveforms

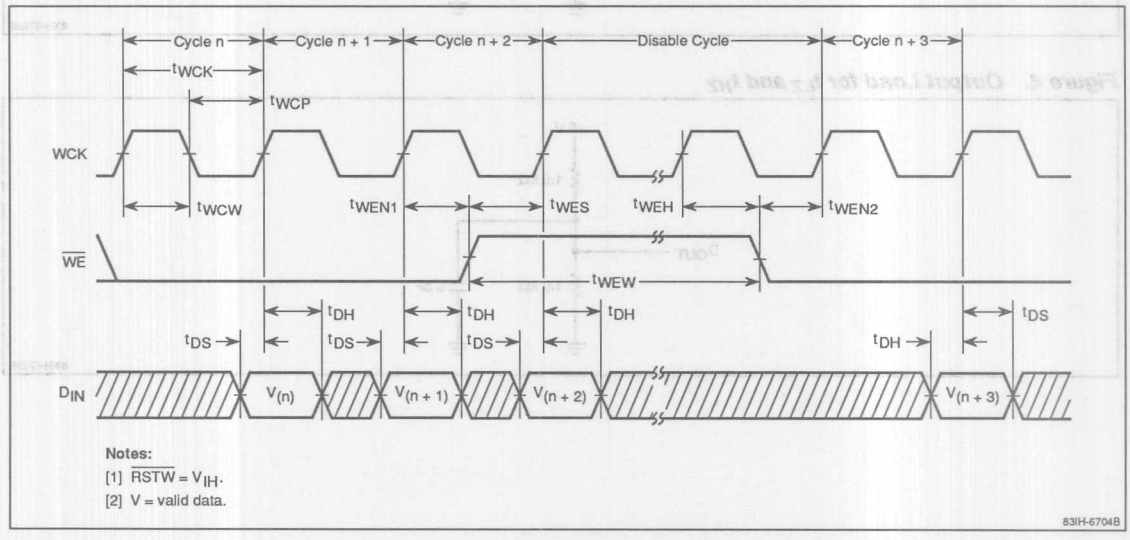
Read Cycle



Notes:
[1] $\overline{RSTR} = V_{IH}$.
[2] V = valid data.

83IH-6705B

Write Cycle

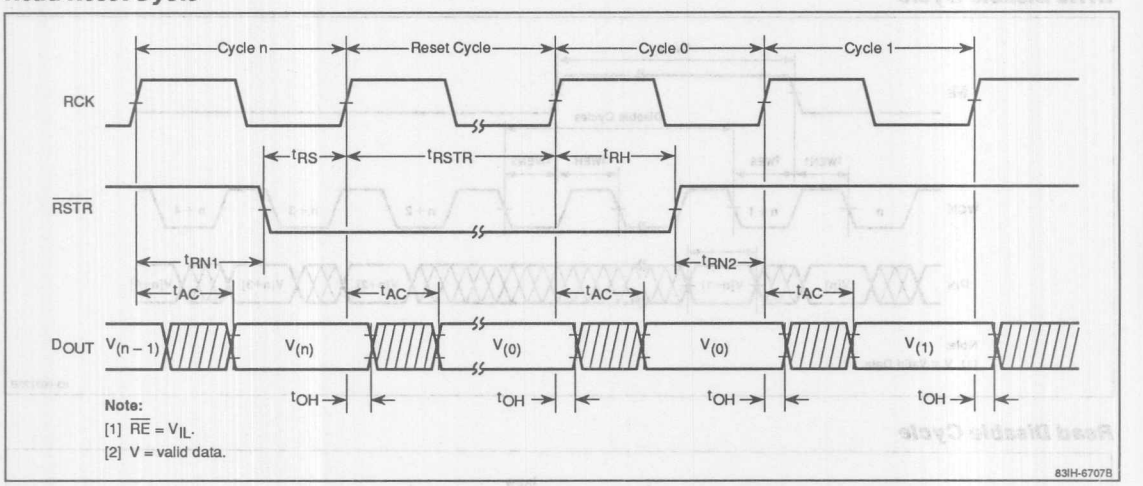


Notes:
[1] $\overline{RSTW} = V_{IH}$.
[2] V = valid data.

83IH-6704B

Timing Waveforms (cont)

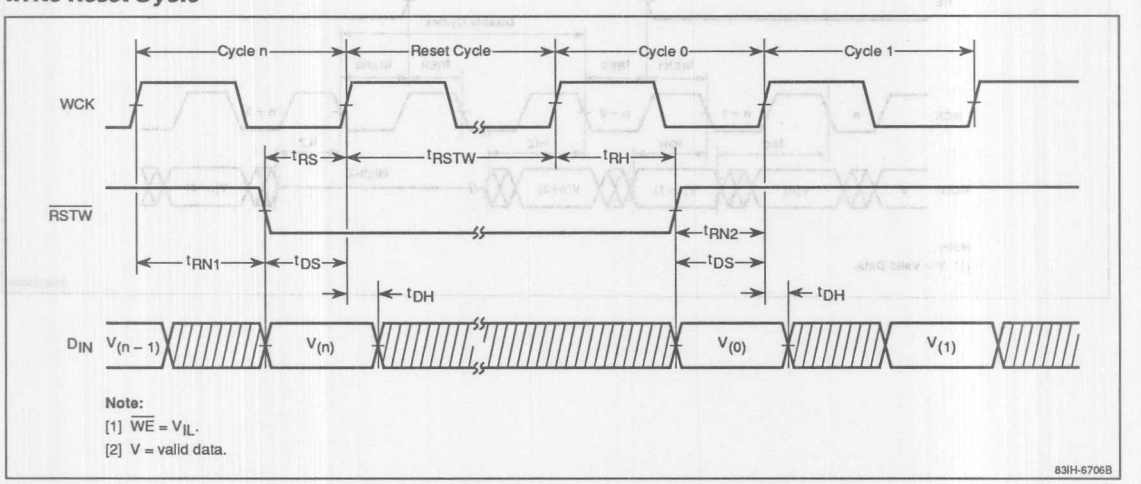
Read Reset Cycle



Note:
[1] $\overline{RE} = V_{IL}$.
[2] V = valid data.

83IH-6707B

Write Reset Cycle

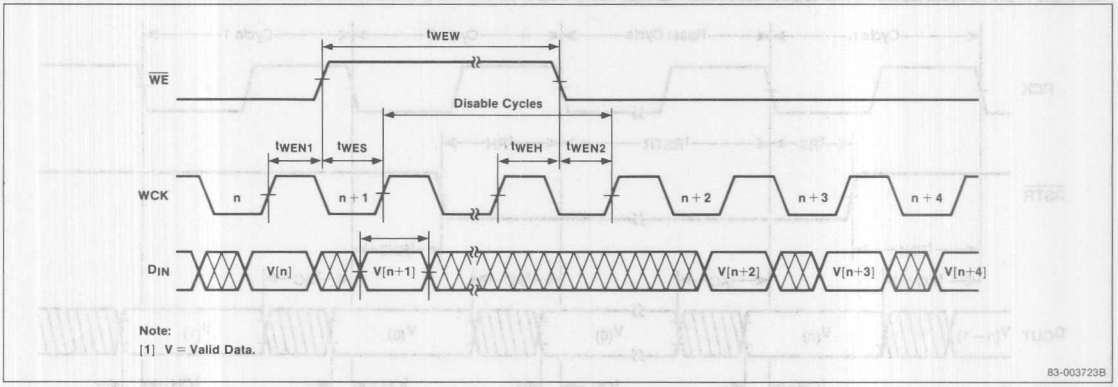


Note:
[1] $\overline{WE} = V_{IL}$.
[2] V = valid data.

83IH-6706B

Timing Waveforms (cont)

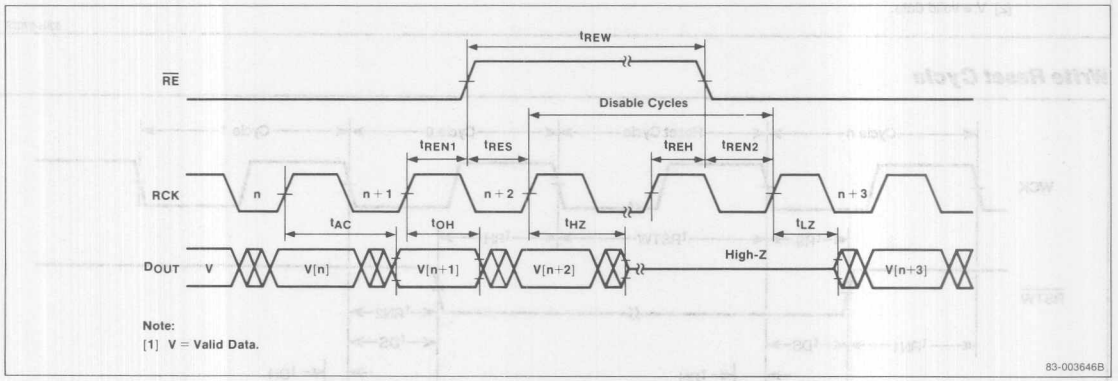
Write Disable Cycle



Note:
[1] V = Valid Data.

83-003723B

Read Disable Cycle

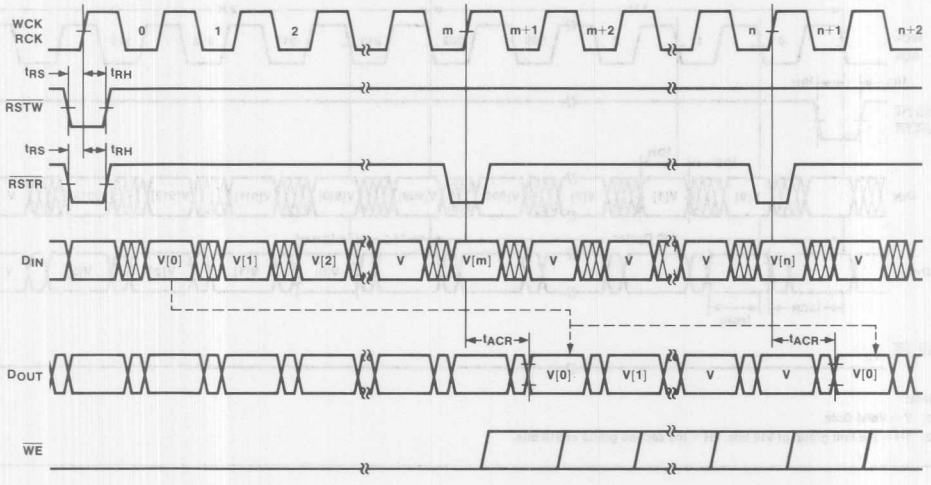


Note:
[1] V = Valid Data.

83-003646B

Timing Waveforms (cont)

Re-Read Cycle



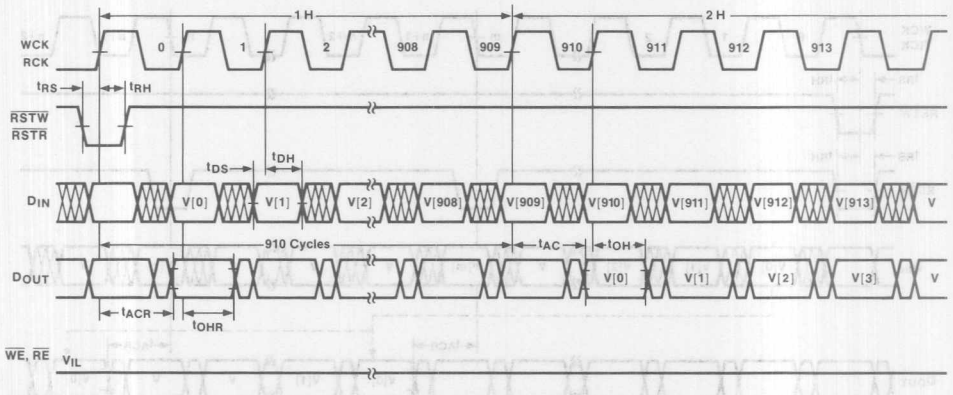
Note:
[1] $\overline{RE} = V_{IL}$.
[2] V = Valid Data.
[3] The data stored in any location can be re-read as many times as desired within a period of 1 ms following the writing of data into that location provided that a second write operation has not re-written new data into that location.

83-003644B

3

Timing Waveforms (cont)

910-Bit Delay Line Cycle

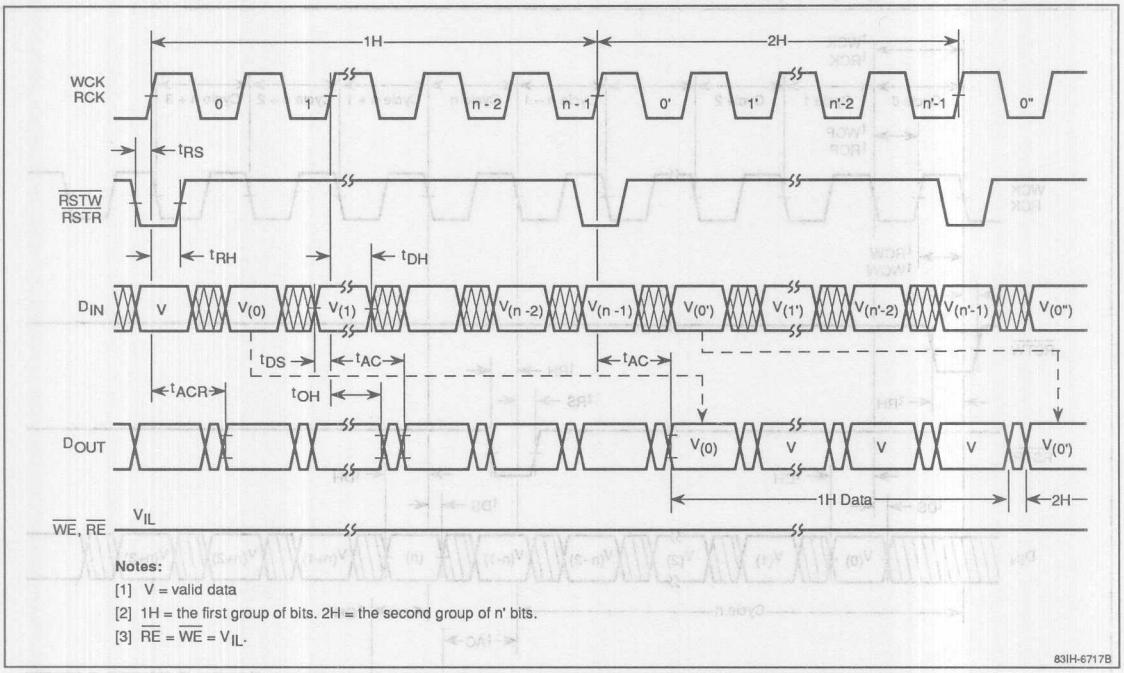


Note:
[1] V = Valid Data.
[2] 1H = the first group of 910 bits. 2H = the second group of 910 bits.

83-003657B

Timing Waveforms (cont)

n-Bit Delay Line Cycle



Notes:

[1] V = valid data

[2] 1H = the first group of bits. 2H = the second group of n' bits.

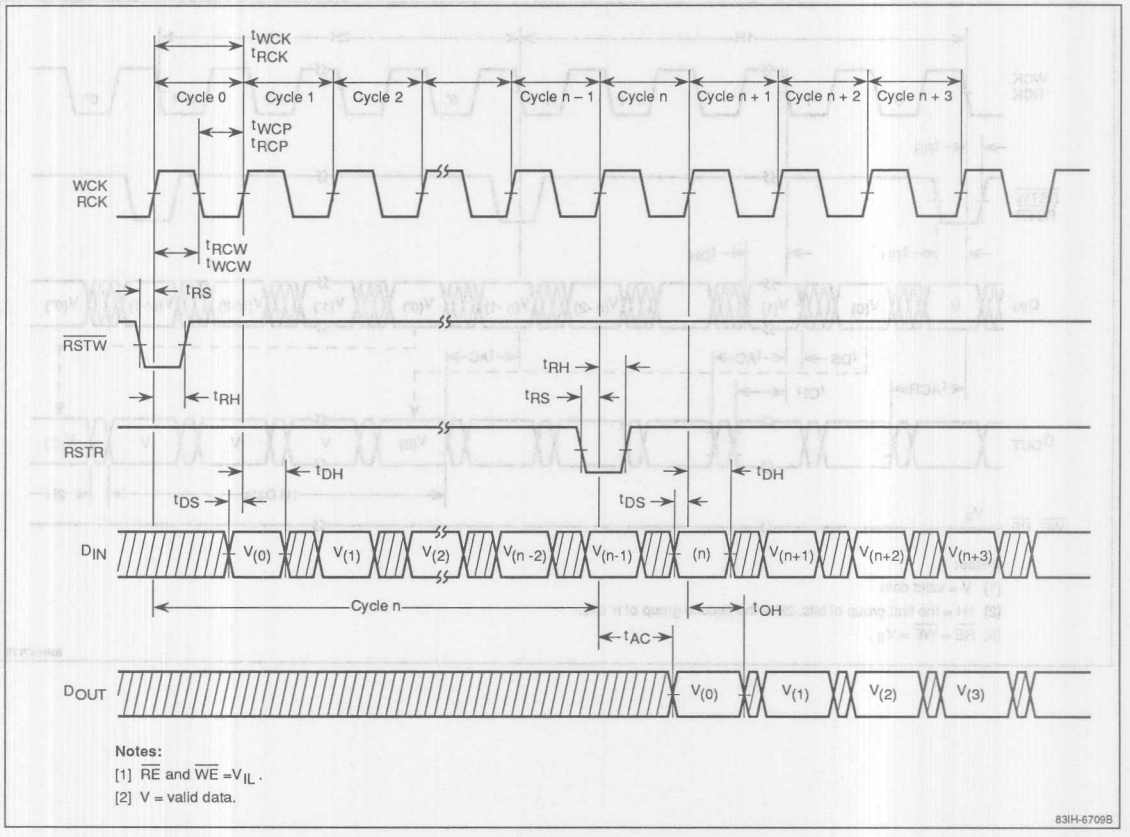
[3] $\overline{RE} = \overline{WE} = V_{IL}$.

83IH-6717B

3

Timing Waveforms (cont)

n-Bit Delay Line Timing Cycle (1)



Notes:

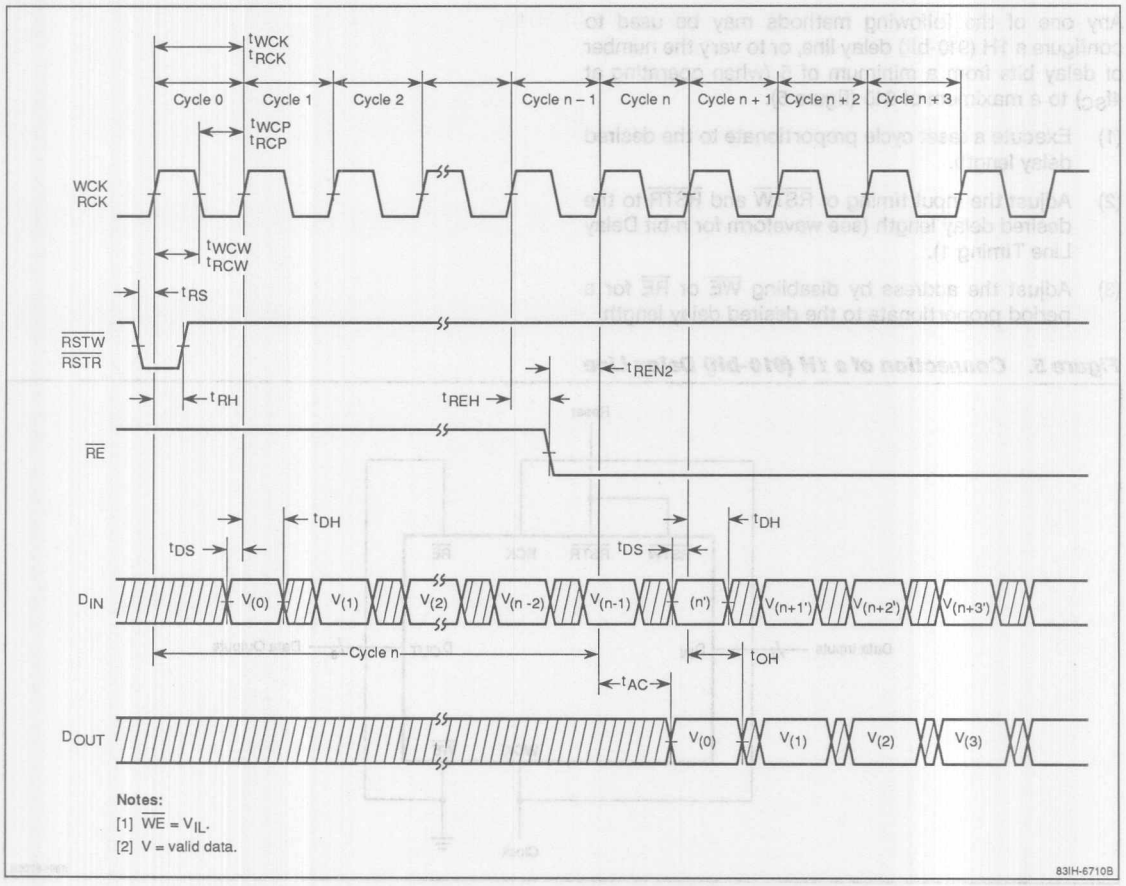
[1] $\overline{RE}$ and $\overline{WE}$ = V_{IL}.

[2] V = valid data.

83IH-6709B

Timing Waveforms (cont)

n-Bit Delay Line Timing Cycle (2)



Notes:
[1] $\overline{WE} = V_{IL}$.
[2] V = valid data.

83IH-6710B

Applications

1H (910-bit) Delay Line

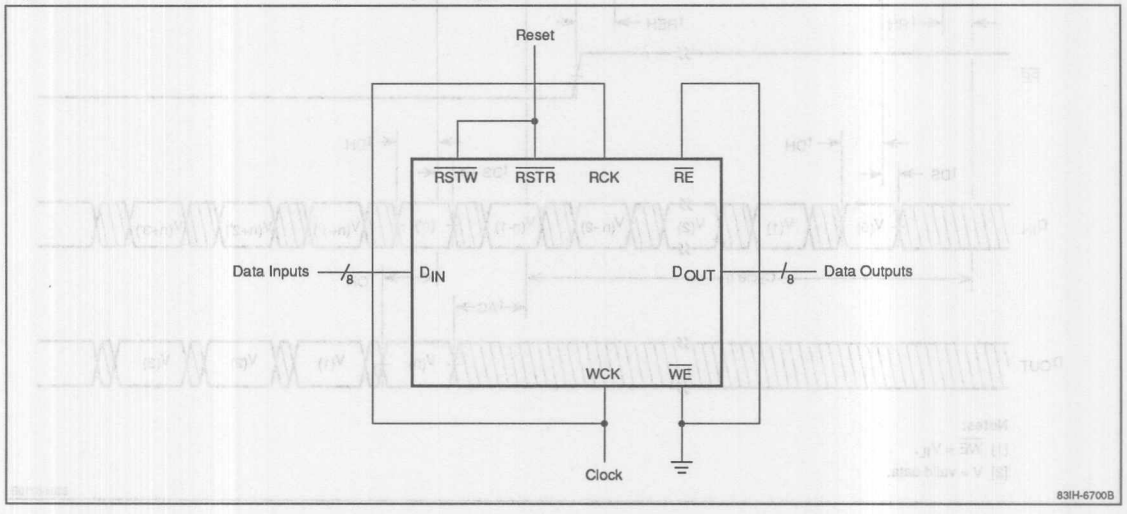
Any one of the following methods may be used to configure a 1H (910-bit) delay line, or to vary the number of delay bits from a minimum of 5 (when operating at $4f_{SC}$) to a maximum of 910 (figure 5).

(1) Execute a reset cycle proportionate to the desired delay length.

(2) Adjust the input timing of $\overline{RSTW}$ and $\overline{RSTR}$ to the desired delay length (see waveform for n-bit Delay Line Timing 1).

(3) Adjust the address by disabling $\overline{WE}$ or $\overline{RE}$ for a period proportionate to the desired delay length.

Figure 5. Connection of a 1H (910-bit) Delay Line

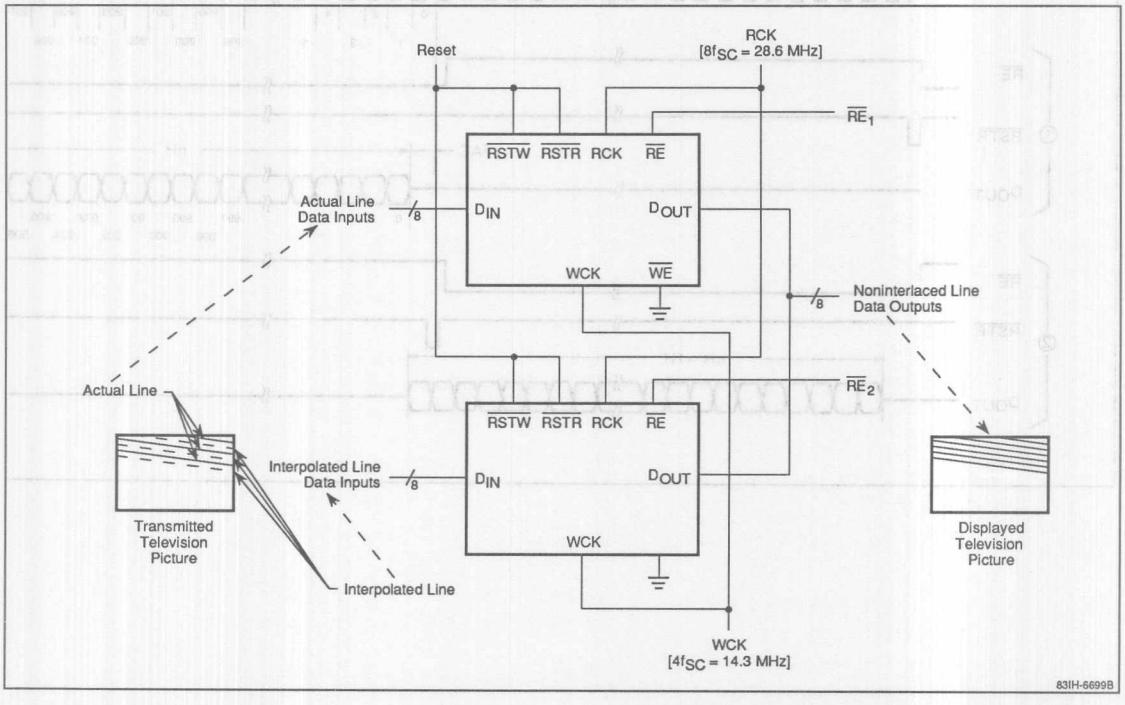


Applications (cont)

Noninterlaced Scan Conversion

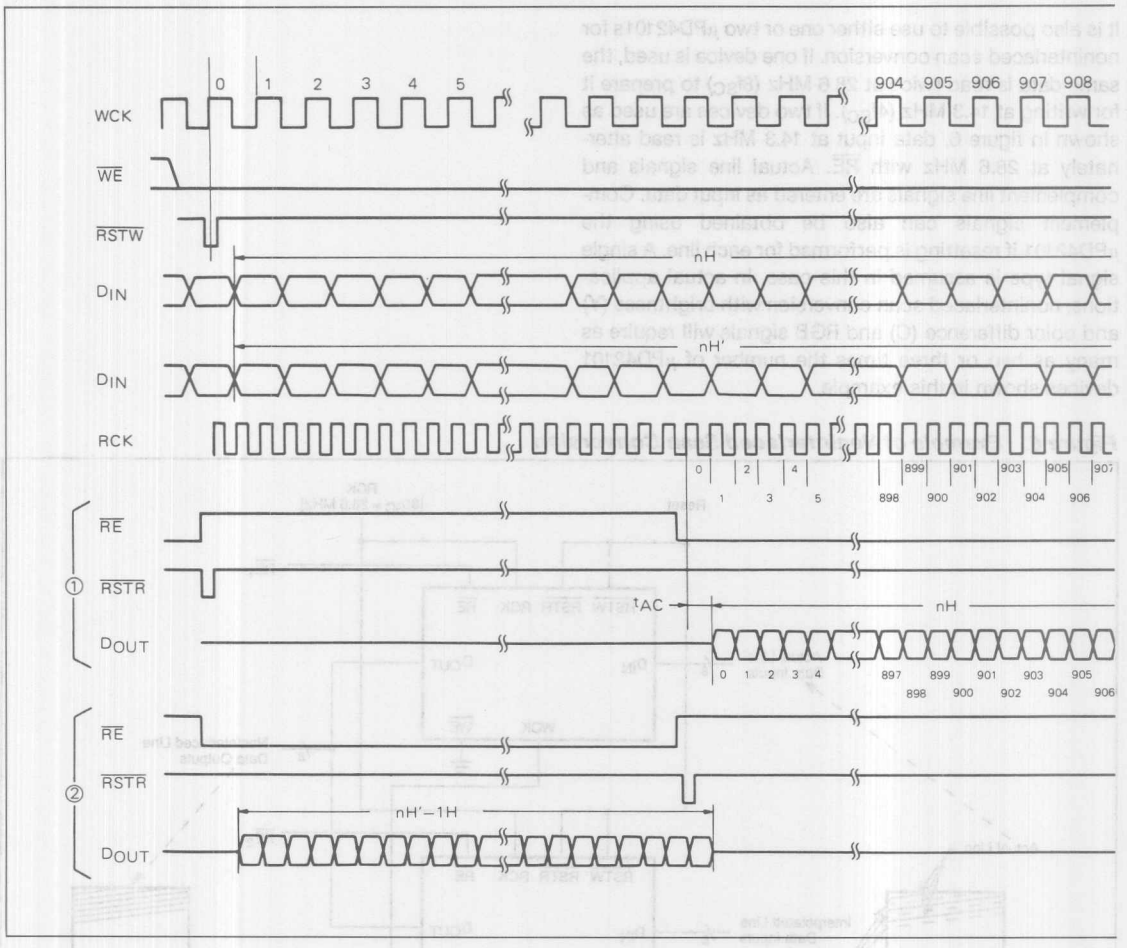
It is also possible to use either one or two μPD42101s for noninterlaced scan conversion. If one device is used, the same data is read twice at 28.6 MHz ($8f_{SC}$) to prepare it for writing at 14.3 MHz ($4f_{SC}$). If two devices are used as shown in figure 6, data input at 14.3 MHz is read alternately at 28.6 MHz with $\overline{RE}$. Actual line signals and complement line signals are entered as input data. Complement signals can also be obtained using the μPD42101 if resetting is performed for each line. A single signal type is assumed in this case. In actual applications, noninterlaced scan conversion with brightness (Y) and color difference (C) and RGB signals will require as many as two or three times the number of μPD42101 devices shown in this example.

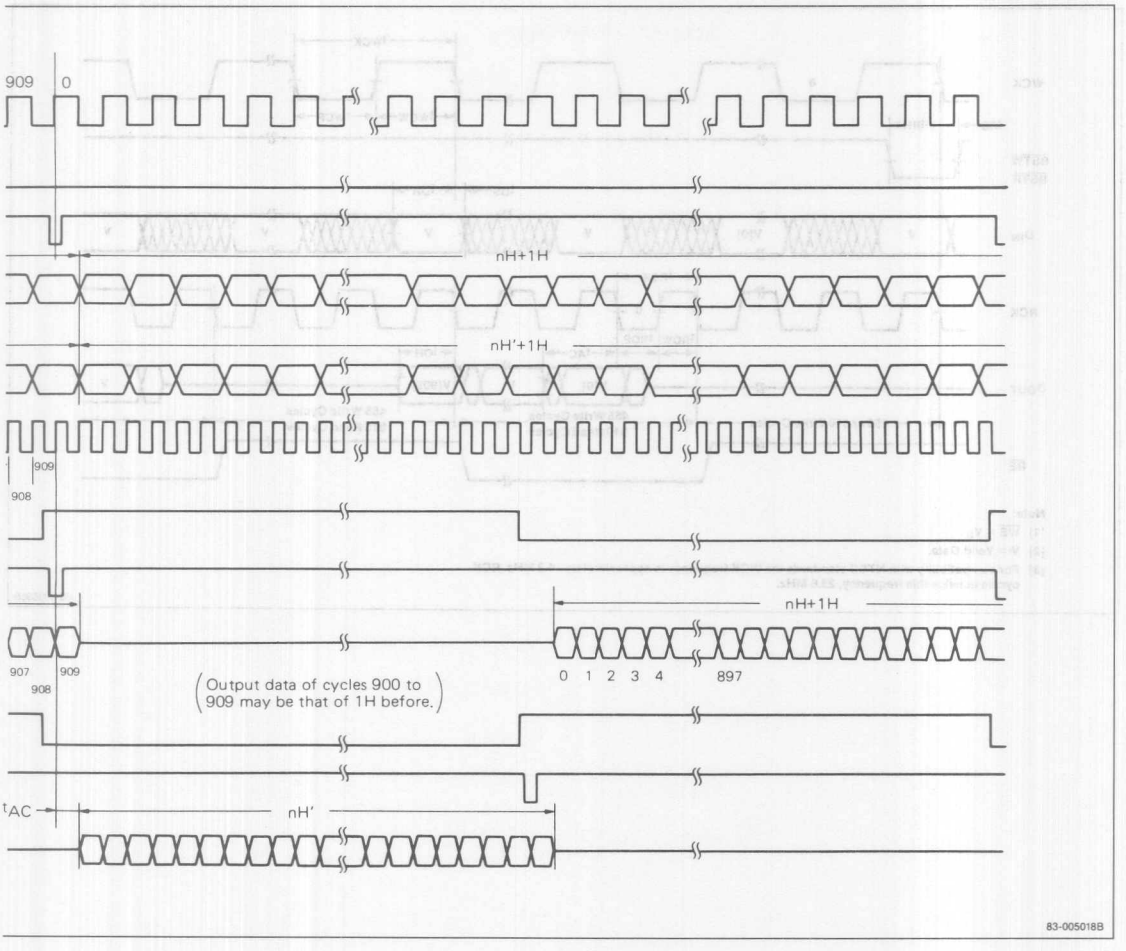
Figure 6. Example of Noninterlaced Scan Conversion



Timing Waveforms (cont)

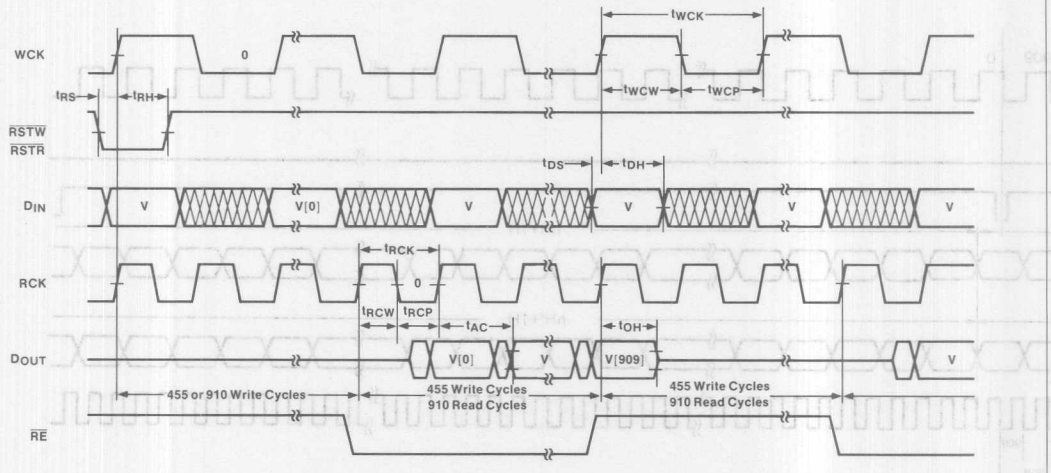
Application Timing for Noninterlaced Scan Conversion




909
0
nH+1H
nH'+1H
908
909
907
908
909
nH+1H
0 1 2 3 4
897
(Output data of cycles 900 to 909 may be that of 1H before.)
tAC
nH'
83-005018B

Timing Waveforms (cont)

Basic Timing for Noninterlaced Scan Conversion



Note:
[1] $\overline{WE}$ = V_{IL}.
[2] V = Valid Data.
[3] For compatibility with NTSC standards the WCK frequency is approximately 14.3 MHz. RCK cycles at twice this frequency, 28.6 MHz.

83-003655B

Description

The μPD42102 is a 1,135-word by 8-bit line buffer fabricated with a CMOS silicon-gate process. The device helps to create a PAL flicker-free television picture (non-interlaced scan conversion) by providing intermediate storage and very high-speed read and write operation.

The μPD42102 can also be used as a digital delay line. The delay length is variable from 2 bits (at maximum clock speed) to 1,135 bits.

Features

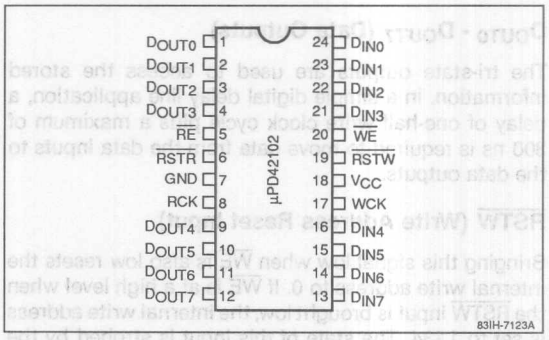
- 1,135-word x 8-bit organization
- Line buffer for PAL, $4f_{SC}$ digital television systems
- Asynchronous, simultaneous read/write operation
- 1H (1,135-bit) delay line capability
- TTL-compatible inputs and outputs
- Three-state outputs
- Single +5-volt power supply
- 24-pin plastic DIP and miniflat packaging

Ordering Information

Part Number	Read Cycle Time (min)	Write Cycle Time (min)	Package
μPD42102C-5	25 ns	25 ns	24-pin plastic DIP
C-3	34 ns	34 ns	
C-2	34 ns	69 ns	
C-1	69 ns	69 ns	
μPD42102G-5	25 ns	25 ns	24-pin plastic miniflat
G-3	34 ns	34 ns	
G-2	34 ns	69 ns	
G-1	69 ns	69 ns	

Pin Configuration

24-Pin Plastic DIP or Miniflat



Pin Identification

Symbol	Function
D_{IN0} - D_{IN7}	Write data inputs
D_{OUT0} - D_{OUT7}	Read data outputs
$\overline{RSTW}$	Write address reset input
$\overline{RSTR}$	Read address reset input
$\overline{WE}$	Write enable input
$\overline{RE}$	Read enable input
WCK	Write clock input
RCK	Read clock input
GND	Ground
V_{CC}	+5-volt power supply

3

PIN FUNCTIONS

D_{IN0} - D_{IN7} (Data Inputs)

In a digital television application, the digital composite signal, luminance, chrominance, etc. information is written into these inputs.

D_{OUT0} - D_{OUT7} (Data Outputs)

The tri-state outputs are used to access the stored information. In a simple digital delay line application, a delay of one-half write clock cycle plus a maximum of 300 ns is required to move data from the data inputs to the data outputs.

$\overline{RSTW}$ (Write Address Reset Input)

Bringing this signal low when $\overline{WE}$ is also low resets the internal write address to 0. If $\overline{WE}$ is at a high level when the $\overline{RSTW}$ input is brought low, the internal write address is set to 1,134. The state of this input is strobed by the rising edge of WCK.

$\overline{RSTR}$ (Read Address Reset Input)

This signal is strobed by the rising edge of RCK and resets the internal read address to 0 if $\overline{RE}$ is also low. If $\overline{RE}$ is at a high level when the $\overline{RSTR}$ input is brought low, the internal read address is set to 1,134.

$\overline{WE}$ (Write Enable Input)

This input controls write operation. If $\overline{WE}$ is low, all write cycles proceed. If $\overline{WE}$ is at a high level, no data is written to storage cells and the write address stops increasing. The state of $\overline{WE}$ is strobed by the rising edge of WCK.

$\overline{RE}$ (Read Enable Input)

This signal is similar to $\overline{WE}$ but controls read operation. If $\overline{RE}$ is at a high level, the data outpus become high impedance and the internal read address stops increasing. The state of $\overline{RE}$ is strobed by the rising edge of RCK.

WCK (Write Clock Input)

All write cycles are executed synchronously with WCK. The states of both $\overline{RSTW}$ and $\overline{WE}$ are strobed by the rising edge of WCK at the beginning of a cycle, and the data inputs are strobed by the rising edge of WCK at the end of a cycle. The internal write address increases with each WCK cycle unless $\overline{WE}$ is at a high level to hold the write address constant. Unless inhibited by $\overline{WE}$, the internal write address will automatically wrap around from 1,134 to 0 and begin increasing again.

RCK (Read Clock Input)

All read cycles are executed synchronously with RCK. The states of both $\overline{RSTR}$ and $\overline{RE}$ are strobed by the rising edge of RCK at the beginning of a cycle. This same edge of RCK starts internal read operation, and access time is referenced to this edge. The internal read address increases with each RCK cycle unless $\overline{RE}$ is at a high level to hold the read address constant. Unless inhibited by $\overline{RE}$, the internal read address will automatically wrap around from 1,134 to 0 and begin increasing again.

Absolute Maximum Ratings

Supply voltage, V_{CC}	−1.5 to +7.0 V
Voltages on any input pin, V_I	−1.5 to + 7.0 V
Voltage on any output pin, V_O	−1.5 to +7.0 V
Short-circuit output current, I_{OS}	20 mA
Operating temperature, T_{OPR}	−20 to +70°C
Storage temperature, T_{STG}	−55 to +125°C

Exposure to Absolute Maximum Ratings for extended periods may affect device reliability; exceeding the ratings could cause permanent damage. The device should be operated within the limits specified under DC and AC Characteristics.

Recommended Operating Conditions

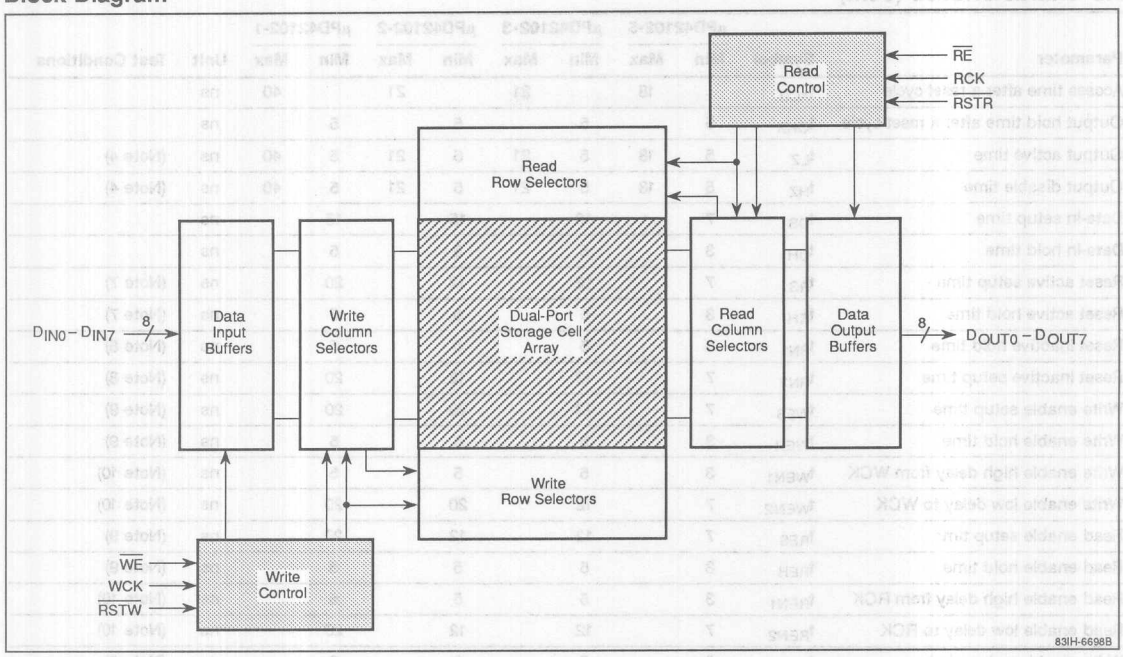
Parameter	Symbol	Min	Typ	Max	Unit
Supply voltage	V_{CC}	4.5	5.0	5.5	V
Input voltage, high	V_{IH}	2.4		5.5	V
Input voltage, low	V_{IL}	−1.5		0.8	V
Operating temperature	T_A	−20		70	°C

Capacitance

T_A = 25°C; V_{CC} = +5.0 V ±10%; f = 1 MHz

Parameter	Symbol	Min	Max	Unit	Pins Under Test
Input capacitance	C_I		5	pF	$\overline{WE}$, $\overline{RE}$, WCK, RCK, $\overline{RSTW}$, $\overline{RSTR}$, D_{IN0} - D_{IN7}
Output capacitance	C_O		7	pF	D_{OUT0} - D_{OUT7}

Block Diagram



DC Characteristics

T_A = −20 to +70°C; V_{CC} = +5.0 V ± 10%

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions
Input leakage current	I_I	−10		10	μA	V_{IN} = 0 V to V_{CC}; all other pins not under test = 0 V
Output leakage current	I_O	−10		10	μA	D_{OUT} disabled; V_O = 0 to 5.5 V
Output voltage, high	V_{OH}	2.4			V	I_{OH} = −1 mA
Output voltage, low	V_{OL}			0.4	V	I_{OL} = 2.0 mA

AC Characteristics

T_A = −20 to +70°C; V_{CC} = +5.0 V ± 10%

		μPD42102-5		μPD42102-3		μPD42102-2		μPD42102-1			
Parameter	Symbol	Min	Max	Min	Max	Min	Max	Min	Max	Unit	Test Conditions
Write/read cycle operating current	I_{CC}		80		80		70		40	mA	t_{WCK} = t_{WCK} (min); t_{RCK} = t_{RCK} (min)
Write clock cycle time	t_{WCK}	25	880	28	880	56	880	56	880	ns	
WCK pulse width	t_{WCW}	10		12		20		20		ns	
WCK precharge time	t_{WCP}	10		12		20		20		ns	
Read clock cycle time	t_{RCK}	25	880	28	880	28	880	56	880	ns	
RCK pulse width	t_{RCW}	10		12		12		20		ns	
RCK precharge time	t_{RCP}	10		12		12		20		ns	
Access time	t_{AC}		18		21		21		40	ns	
Output hold time	t_{OH}	5		5		5		5		ns	

AC Characteristics (cont)

Parameter	Symbol	μPD42102-5 Min	μPD42102-5 Max	μPD42102-3 Min	μPD42102-3 Max	μPD42102-2 Min	μPD42102-2 Max	μPD42102-1 Min	μPD42102-1 Max	Unit	Test Conditions
Access time after a reset cycle	t_{ACR}		18		21		21		40	ns	
Output hold time after a reset cycle	t_{OHR}	5		5		5		5		ns	
Output active time	t_{LZ}	5	18	5	21	5	21	5	40	ns	(Note 4)
Output disable time	t_{HZ}	5	18	5	21	5	21	5	40	ns	(Note 4)
Data-in setup time	t_{DS}	7		12		15		15		ns	
Data-in hold time	t_{DH}	3		5		5		5		ns	
Reset active setup time	t_{RS}	7		12		12		20		ns	(Note 7)
Reset active hold time	t_{RH}	3		5		5		5		ns	(Note 7)
Reset inactive hold time	t_{RN1}	3		5		5		5		ns	(Note 8)
Reset inactive setup time	t_{RN2}	7		12		12		20		ns	(Note 8)
Write enable setup time	t_{WES}	7		12		20		20		ns	(Note 9)
Write enable hold time	t_{WEH}	3		5		5		5		ns	(Note 9)
Write enable high delay from WCK	t_{WEN1}	3		5		5		5		ns	(Note 10)
Write enable low delay to WCK	t_{WEN2}	7		12		20		20		ns	(Note 10)
Read enable setup time	t_{RES}	7		12		12		20		ns	(Note 9)
Read enable hold time	t_{REH}	3		5		5		5		ns	(Note 9)
Read enable high delay from RCK	t_{REN1}	3		5		5		5		ns	(Note 10)
Read enable low delay to RCK	t_{REN2}	7		12		12		20		ns	(Note 10)
Write disable pulse width	t_{WEW}	0		0		0		0		ns	(Note 5)
Read disable pulse width	t_{REW}	0		0		0		0		ns	(Note 5)
Write reset time	t_{RSTW}	0		0		0		0		ns	(Note 5)
Read reset time	t_{RSTR}	0		0		0		0		ns	(Note 5)
Transition time	t_T	3	35	3	35	3	35	3	35	ns	

Notes:

(1) All voltages are referenced to ground.

(2) Input pulse rise and fall times assume t_T = 5 ns. Input pulse levels = GND to 3 V. Transition times are measured between 3 V and 0 V.
For the –5 version only, t_T = 3 ns; input pulse levels = 0.4 to 2.4 V; transition times are measured between 0.4 and 2.4 V. See figures 1 and 2.

(3) Input timing reference levels = 1.5 V. Output timing reference levels are 0.8 and 2.0 V. See figure 3.

(4) This delay is measured at 200 mV from the steady-state voltage with the load specified in figure 5. Under any conditions, $t_{LZ} \geq t_{HZ}$.

(5) t_{WEW} (max) and t_{REW} (max) must be satisfied by the following equations in 1-line cycle operation:
$t_{WEW} + t_{RSTW} + 1{,}135\ (t_{WCK}) \leq 1$ ms
$t_{REW} + t_{RSTR} + 1{,}135\ (t_{RCK}) \leq 1$ ms

(6) This parameter applies when $t_{RCK} \geq t_{ACR}$ (max).

(7) If either t_{RS} or t_{RH} is less than the specified value, reset operations are not guaranteed.

(8) If either t_{RN1} or t_{RN2} is less than the specified value, internal reset operations may extend to cycles immediately preceding or following the period of desired reset operations.

(9) If either t_{WES} or t_{WEH} (t_{RES} or t_{REH}) is less than the specified value, write (read) disable operations are not guaranteed.

(10) If either t_{WEN1} or t_{WEN2} (t_{REN1} or t_{REN2}) is less than the specified value, internal write (read) disable operations may extend to cycles immediately preceding or following the period of desired disable operations.

(11) Data is guaranteed to remain valid for a minimum of 1 ms after it is written. After this time, the data stored may be invalid, since this device uses a dynamic storage element.

Figure 1. Input Timing

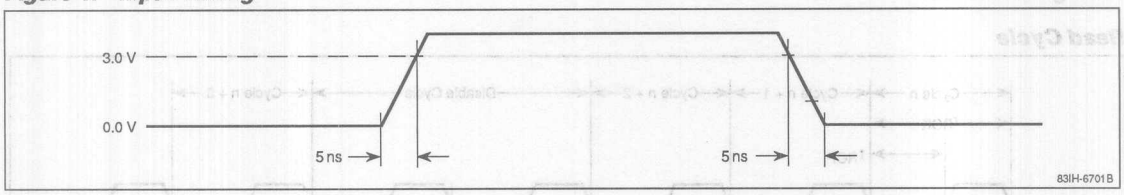


Figure 2. Input Timing for μPD42102-5

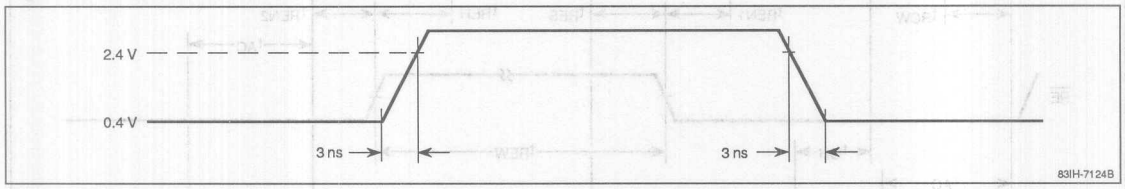


Figure 3. Output Timing

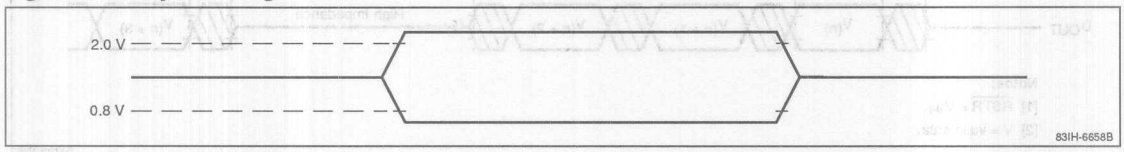


Figure 4. Output Load for t_{AC}, t_{ACR}, t_{OH} and t_{OHR}

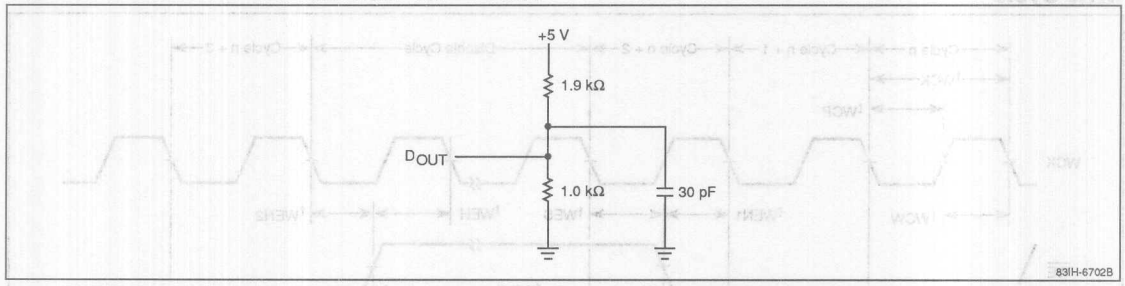
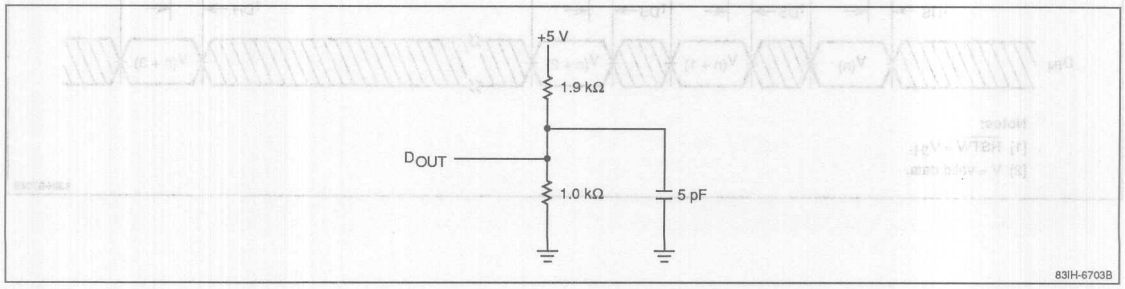


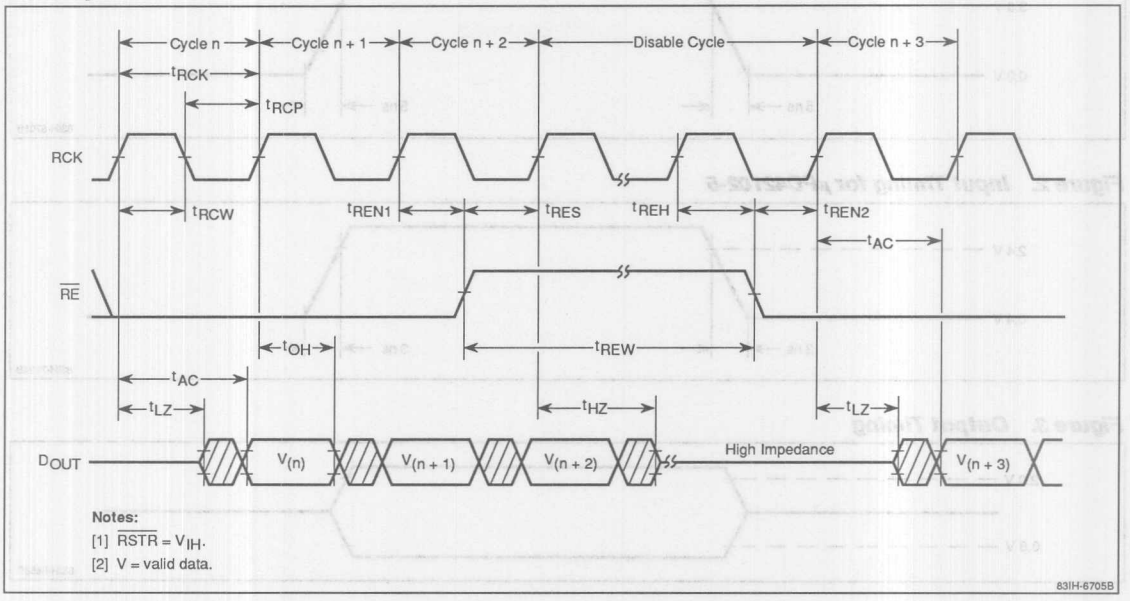
Figure 5. Output Load for t_{LZ} and t_{HZ}



3

Timing Waveforms

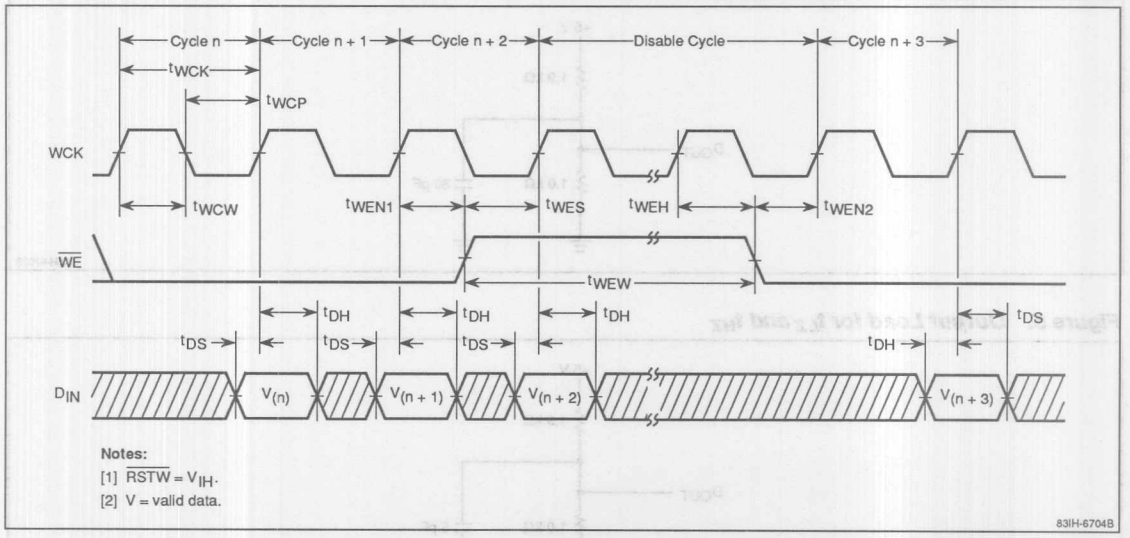
Read Cycle



Notes:
[1] $\overline{RSTR} = V_{IH}$.
[2] V = valid data.

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Write Cycle

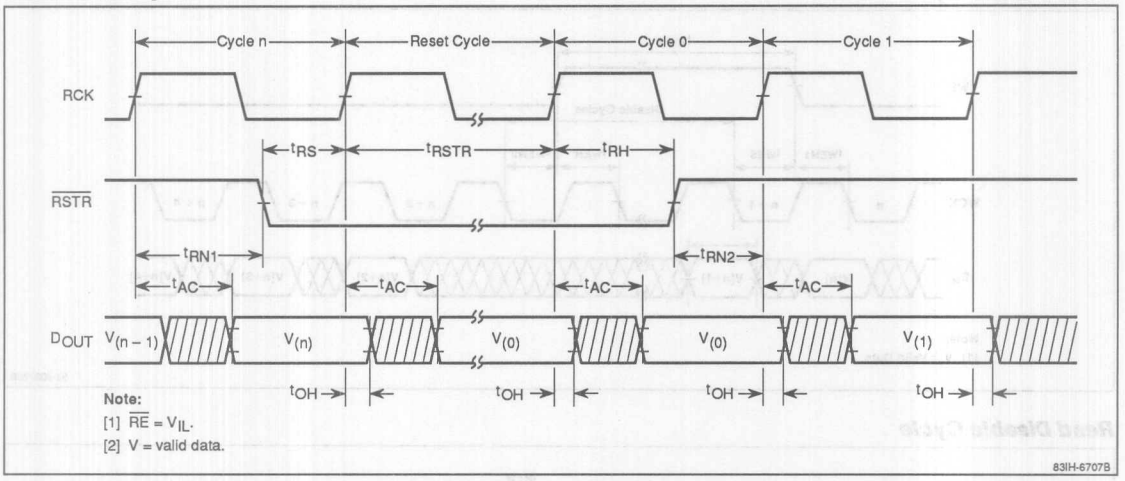


Notes:
[1] $\overline{RSTW} = V_{IH}$.
[2] V = valid data.

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Timing Waveforms (cont)

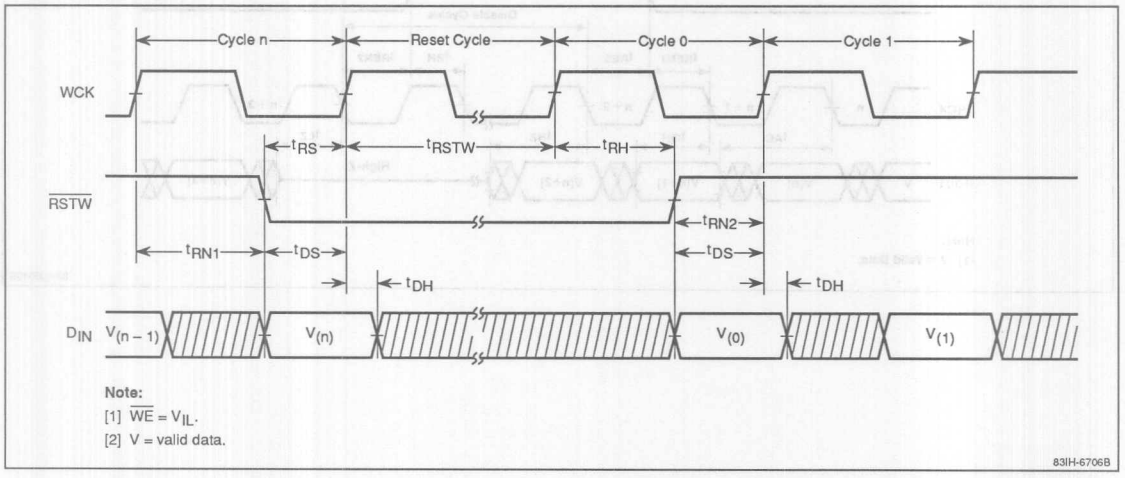
Read Reset Cycle



Note:
[1] $\overline{RE} = V_{IL}$.
[2] V = valid data.

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Write Reset Cycle

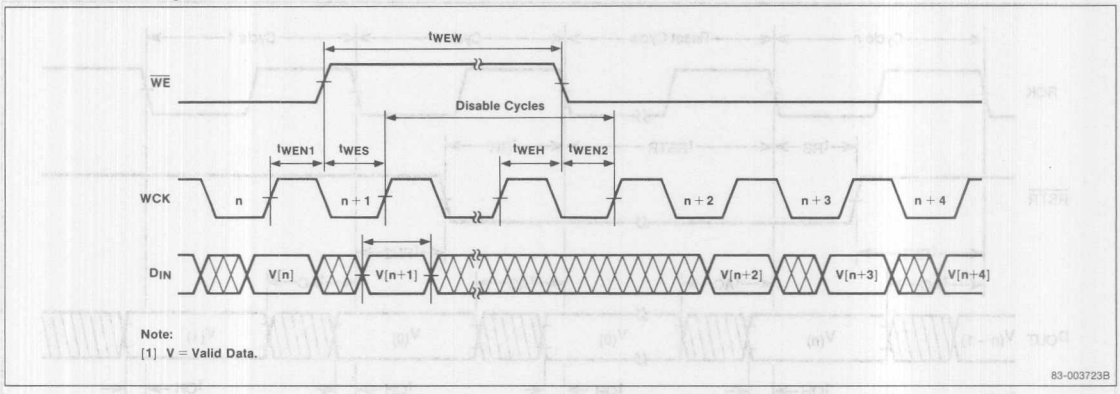


Note:
[1] $\overline{WE} = V_{IL}$.
[2] V = valid data.

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Timing Waveforms (cont)

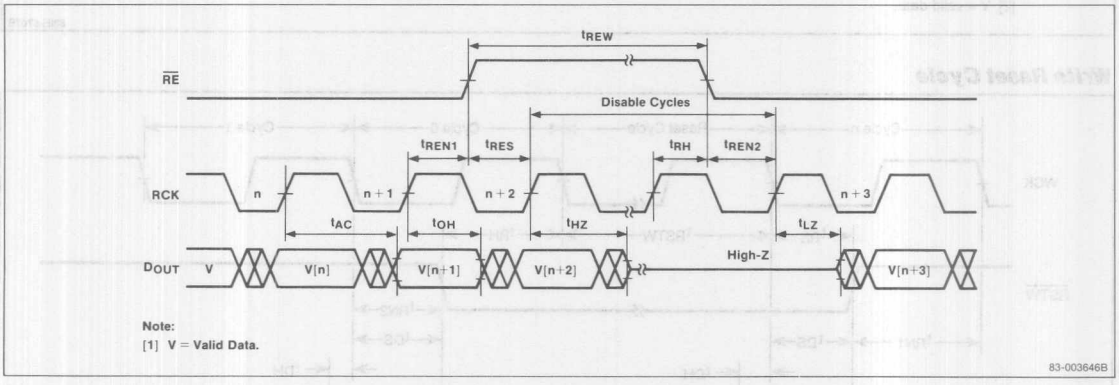
Write Disable Cycle



Note:
[1] V = Valid Data.

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Read Disable Cycle

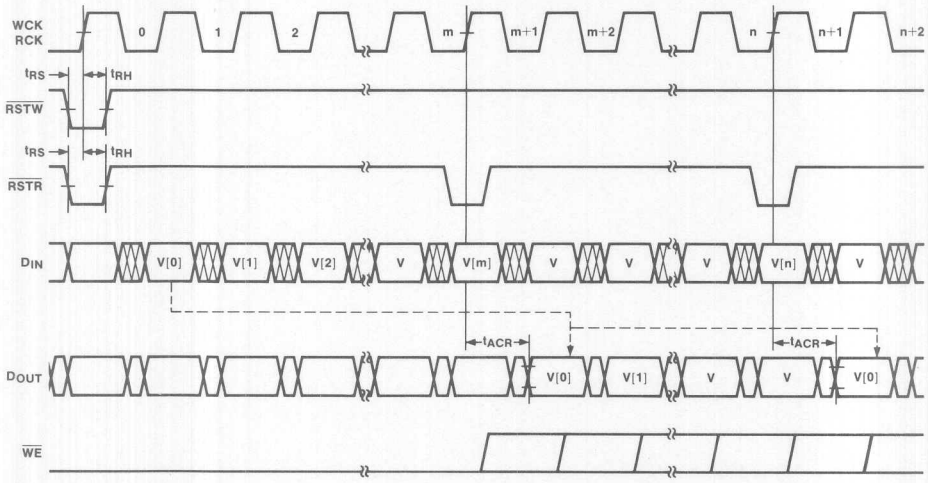


Note:
[1] V = Valid Data.

83-003646B

Timing Waveforms (cont)

Re-Read Cycle



Note:
[1] $\overline{RE} = V_{IL}$.
[2] V = Valid Data.
[3] The data stored in any location can be re-read as many times as desired within a period of 1 ms following the writing of data into that location provided that a second write operation has not re-written new data into that location.

83-003644B

3

Description

The μPD42505 is a 5048-word by 8-bit dual-port line buffer fabricated with a silicon-gate CMOS process. The device is capable of asynchronous read and write operation at high speed, and can be used as a time axis converter or a digital delay line of up to 5048 bits (10 bits minimum at maximum frequency).

Applications include image processing in facsimile machines, plain paper copiers, video systems, and other optical scanners; time base correction in video playback systems; and data communication buffering in multiprocessor systems and local area networks.

Features

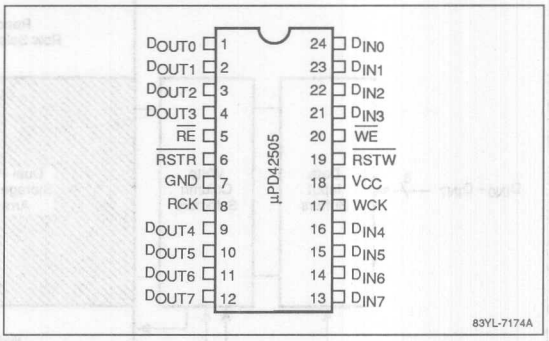
- 5048-word x 8-bit organization
- Dual-port operation
- Image processing and data communications applications
- Asynchronous and simultaneous reading/writing
- 1H (5048-bit) delay line capability
- TTL-compatible inputs and outputs
- Three-state outputs
- Single + 5-volt power supply
- 24-pin plastic DIP and 28-pin plastic ZIP packaging

Pin Identification

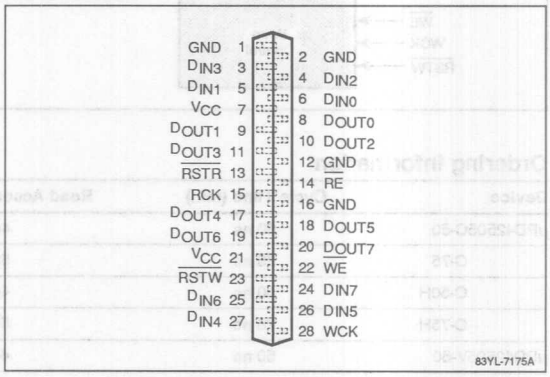
Symbol	Function
D_{IN0} - D_{IN7}	Write data inputs
D_{OUT0} - D_{OUT7}	Read data outputs
RCK	Read clock input
$\overline{RE}$	Read enable input
$\overline{RSTR}$	Read address reset input
$\overline{RSTW}$	Write address reset input
WCK	Write clock input
$\overline{WE}$	Write enable input
GND	Ground
V_{CC}	+5-volt power supply

Pin Configurations

24-Pin Plastic DIP

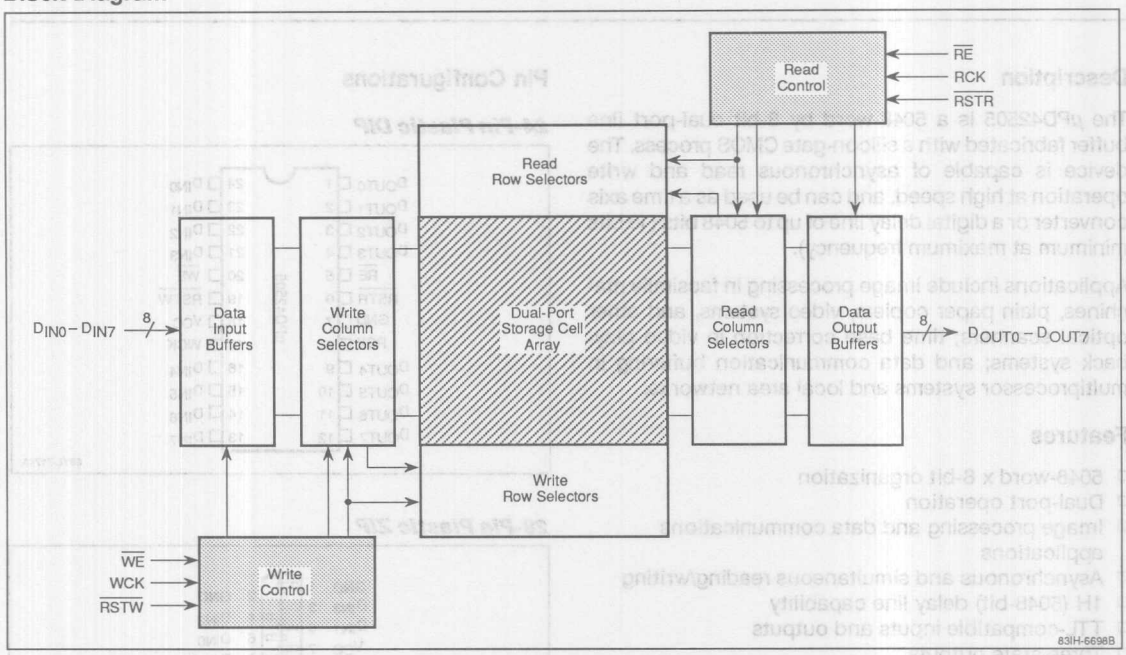


28-Pin Plastic ZIP



3

Block Diagram



Ordering Information

Device	Cycle Time (min)	Read Access Time (max)	Hold Time (min)	Package
μPD42505C-50	50 ns	40 ns	5 ms	24-pin plastic DIP
C-75	75 ns	55 ns		
C-50H	50 ns	40 ns	20 ms	
C-75H	75 ns	55 ns		
μPD42505V-50	50 ns	40 ns	5 ms	28-pin plastic ZIP
V-75	75 ns	55 ns		
V-50H	50 ns	40 ns	20 ms	
V-75H	75 ns	55 ns		

Pin Functions

D_{IN0} through D_{IN7} (Data Inputs). New data is entered on these pins.

D_{OUT0} through D_{OUT7} (Data Outputs). These tri-state outputs are used to access stored information. In a simple digital delay line application, a minimum delay of 10 clock cycles is required to move data from the input pins to the output pins.

RCK (Read Clock Input). All read cycle are executed synchronously with RCK. The states of both $\overline{RSTR}$ and $\overline{RE}$ are strobed by the rising edge of RCK at the beginning of a cycle. This same edge of RCK starts internal read operation, and access time is referenced to this edge. The internal read address increments with each RCK cycle, unless $\overline{RE}$ is high to hold the read address constant. Unless inhibited by $\overline{RE}$, the internal read address will automatically wrap around from 5047 to 0 and begin incrementing again.

$\overline{RE}$ (Read Enable Input). This signal controls read operation. If $\overline{RE}$ is low, all read cycles proceed. If $\overline{RE}$ is at a high level, the data outputs become high impedance and the internal read address stops incrementing. The state of $\overline{RE}$ is strobed by the rising edge of RCK.

$\overline{\text{RSTR}}$ (Read Address Reset Input). This signal is strobed by the rising edge of RCK and resets the internal read address to 0.

$\overline{\text{RSTW}}$ (Write Address Reset Input). Bringing this signal low resets the internal write address to 0. The state of this input is strobed by the rising edge of WCK.

WCK (Write Clock Input). All write cycles are executed synchronously with WCK. The states of both $\overline{\text{RSTW}}$ and $\overline{\text{WE}}$ are strobed by the rising edge of WCK at the beginning of a cycle, and the data inputs are strobed by the rising edge of WCK at the end of a cycle. The internal write address increments with each WCK cycle, unless $\overline{\text{WE}}$ is at a high level to hold the write address constant. Unless inhibited by $\overline{\text{WE}}$, the internal write address will automatically wrap around from 5047 to 0 and begin incrementing again.

$\overline{\text{WE}}$ (Write Enable Input). This input is similar to $\overline{\text{RE}}$ but controls write operation. If $\overline{\text{WE}}$ is at a high level, no data is written to storage cells and the write address does not increment. The state of $\overline{\text{WE}}$ is strobed by the rising edge of WCK.

Operation

Reset Cycle. The μPD42505 requires the initialization of internal circuits using the $\overline{\text{RSTW}}$/$\overline{\text{RSTR}}$ reset signals before starting operation as a time axis converter or a digital delay line.

A reset cycle can be executed at any time and does not depend on the state of $\overline{\text{RE}}$ or $\overline{\text{WE}}$. However, $\overline{\text{RSTW}}$ and $\overline{\text{RSTR}}$ must satisfy required setup and hold times as measured from the rising edges of WCK and RCK.

Write/Read Cycles. Write and read cycles are synchronized to their respective WCK/RCK inputs and executed individually when WCK or RCK is high and $\overline{\text{WE}}$ or $\overline{\text{RE}}$ is low. Write data must satisfy setup and hold times as specified from the rising edge of WCK. New data written to a particular address is available for reading after 1/2 write cycle + 500 ns (maximum).

The access time of a read cycle is measured from the rising edge of RCK, either by t_{ACR} for an access during the first cycle directly after a reset begins, or by t_{AC} for an access under other conditions. Stored data is read nondestructively; data can be read repeatedly within a prescribed time of 5 ms maximum (20 ms maximum for -H versions).

Time Axis Conversion. To use the μPD42505 as a time axis converter, write and read cycles must be controlled independently. Write and read ports must be initialized separately using the reset signals. Write cycles can then be executed in synchronization with WCK and write data can be stored sequentially from address 0 of this device. Afterward, when a read cycle is executed in synchronization with RCK, stored data can be read sequentially from address 0.

Since write and read cycles can be executed independently, data loaded at one arbitrary drive frequency can be read at another arbitrary drive frequency. In this sense, the μPD42505 functions as a time axis converter.

Digital Delay Line. The μPD42505 can be easily used as a digital delay line of 5,048 bits or less. After the internal circuits are initialized using simultaneous $\overline{\text{RSTW}}$/$\overline{\text{RSTR}}$ signals, write/read cycles also may be executed simultaneously by supplying the same pulse to the write (WCK) and read (RCK) clocks. Write data is always read after the full 5,048-bit delay if neither write nor read operation has been inhibited. This is the essential delay line function.

If either $\overline{\text{WE}}$ or $\overline{\text{RE}}$ is set at a nonselected (high) level for several cycles while the other is maintained in a selected (low) level, the delay line length can differ from 5,048 bits.

For example, if only $\overline{\text{WE}}$ is a set to a high level (write disable) for a small number of cycles, read cycles are executed continuously and the delay line length is large (see the waveform for "(5048-m)-Bit Delay Line No. 2"). Alternatively, if only $\overline{\text{RE}}$ is set to a high level (read disable) for a small number of cycles, write cycles are executed continuously and the delay line length is small. Note that the minimum delay line length is 10 bits (for maximum frequency operation) and the maximum is 5,048 bits.

A data delay of 5,048 bits or less can also be obtained by applying the $\overline{\text{RSTW}}$ and $\overline{\text{RSTR}}$ signals at different times. For example, data loaded for "m" cycles after $\overline{\text{RSTW}}$ can then be read after supplying $\overline{\text{RSTR}}$. In this case, since write data can be read from the beginning after a delay of "m" cycles, the device can be used as an "m-bit" digital delay line.

The $\overline{\text{RSTW}}$/$\overline{\text{RSTR}}$ reset signals can also be simultaneously loaded at every 1H (horizontal line) period. In this case, write data loaded in the previous line cycle is read out from the beginning as read data after the reset. Therefore, a delay line length ranging from 10 to 5,048 bits can be obtained according to the length of the reset signals supplied. Refer to the timing waveform for an "n-Bit Delay Line."

Absolute Maximum Ratings

Supply voltage, V_{CC}	−1.5 to +7.0 V
Voltage on any input pin, V_I	−1.5 to +7.0 V
Voltage on any output pin, V_O	−1.5 to +7.0 V
Short-circuit output current, I_{OS}	20 mA
Operating temperature, T_{OPR}	−20 to +70 °C
Storage temperature, T_{STG}	−55 to +125 °C

Exposure to Absolute Maximum Ratings for extended periods may affect device reliability; exceeding the ratings could cause permanent damage. The device should be operated within the limits specified under DC and AC Characteristics.

Recommended Operating Conditions

Parameter	Symbol	Min	Typ	Max	Unit
Supply voltage	V_{CC}	4.5	5.0	5.5	V
Input voltage, high	V_{IH}	2.4		V_{CC}	V
Input voltage, low	V_{IL}	−1.5		0.8	V
Ambient temperature	T_A	−20		70	°C

Capacitance

T_A = 25°C; V_{CC} = +5.0 V ±10%; f = 1 MHz

Parameter	Symbol	Max	Unit	Test Conditions
Input capacitance	C_I	5	pF	$\overline{WE}$, $\overline{RE}$, WCK, RCK, $\overline{RSTW}$, $\overline{RSTR}$, D_{IN0} - D_{IN7}
Output capacitance	C_O	7	pF	D_{OUT0} - D_{OUT7}

Notes:

(1) These parameters are sampled and not 100% tested.

DC Characteristics

T_A = −20 to +70°C; V_{CC} = +5.0 V ±10%

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions
Write/read cycle operating current	I_{CC}			60	mA	
Input leakage current	I_I	−10		10	μA	V_I = 0 V to V_{CC}; all other pins not under test = 0 V
Output leakage current	I_O	−10		10	μA	D_{OUT} disabled; V_O = 0 to 5.5 V
Output voltage, high	V_{OH}	2.4			V	I_{OH} = −1 mA
Output voltage, low	V_{OL}			0.4	V	I_{OL} = 2 mA

AC Characteristics

T_A = −20 to +70°C; V_{CC} = +5.0 V ±10%

		μPD42505-50		μPD42505-75		μPD42505-50H		μPD42505-75H			
Parameter	Symbol	Min	Max	Min	Max	Min	Max	Min	Max	Unit	Test Conditions
Write clock cycle time	t_{WCK}	50	990	75	990	50	3960	75	3960	ns	
WCK pulse width	t_{WCW}	20		30		20		30		ns	
WCK precharge time	t_{WCP}	20		30		20		30		ns	
Read clock cycle time	t_{RCK}	50	990	75	990	50	3960	75	3960	ns	
RCK pulse width	t_{RCW}	20		30		20		30		ns	
RCK precharge time	t_{RCP}	20		30		20		30		ns	
Access time	t_{AC}		40		55		40		55	ns	
Access time after a reset cycle	t_{ACR}		40		55		40		55	ns	
Output hold time	t_{OH}	5		5		5		5		ns	
Output hold time after a reset cycle	t_{OHR}	5		5		5		5		ns	(Note 7)
Output active time	t_{LZ}	5	40	5	55	5	40	5	55	ns	(Note 4)
Output disable time	t_{HZ}	5	40	5	55	5	40	5	55	ns	(Note 4)
Data-in setup time	t_{DS}	15		20		15		20		ns	

AC Characteristics

T_A = −20 to +70°C; V_{CC} = +5.0 V ±10%

Parameter	Symbol	μPD42505-50		μPD42505-75		μPD42505-50H		μPD42505-75H		Unit	Test Conditions
		Min	Max	Min	Max	Min	Max	Min	Max		
Data-in hold time	t_{DH}	5		5		5		5		ns	
Reset active setup time	t_{RS}	15		20		15		20		ns	(Note 8)
Reset active hold time	t_{RH}	5		5		5		5		ns	(Note 8)
Reset inactive hold time	t_{RN1}	5		5		5		5		ns	(Note 9)
Reset inactive setup time	t_{RN2}	15		20		15		20		ns	(Note 9)
Write enable setup time	t_{WES}	15		20		15		20		ns	(Note 10)
Write enable hold time	t_{WEH}	5		5		5		5		ns	(Note 10)
Write enable high delay from WCK	t_{WEN1}	5		5		5		5		ns	(Note 11)
Write enable low delay to WCK	t_{WEN2}	15		20		15		20		ns	(Note 11)
Read enable setup time	t_{RES}	15		20		15		20		ns	(Note 10)
Read enable hold time	t_{REH}	5		5		5		5		ns	(Note 10)
Read enable high delay from RCK	t_{REN1}	5		5		5		5		ns	(Note 11)
Read enable low delay to RCK	t_{REN2}	15		20		15		20		ns	(Note 11)
Write disable pulse width	t_{WEW}	0		0		0		0		ms	(Note 6)
Read disable pulse width	t_{REW}	0		0		0		0		ms	(Note 6)
Write reset time	t_{RSTW}	0		0		0		0		ms	(Note 6)
Read reset time	t_{RSTR}	0		0		0		0		ms	(Note 6)
Transition time	t_T	3	35	3	35	3	35	3	35	ns	

Notes:

(1) All voltages are referenced to ground.

(2) Input pulse rise and fall times assume t_T = 5 ns.

(3) Input pulse levels = GND to 3 V. Transition times are measured between 3 V and 0 V.

(4) This delay is measured at ±200 mv from the steady-state voltage with the load specified in figure 2. Under any conditions, $t_{LZ} \geq t_{HZ}$.

(5) Input timing reference levels = 1.5 V.

(6) t_{WEW} (max) and t_{REW} (max) must be satisfied by the next equations in one line cycle operation:
$t_{WEW} + t_{RSTW} + 5048t_{WCK} \leq 5$ ms (20 ms for -H versions)
$t_{REW} + t_{RSTR} + 5048t_{RCK} \leq 5$ ms (20 ms for -H versions)

(7) This parameter applies when $t_{RCK} \geq t_{ACR}$ (max)

(8) If either t_{RS} or t_{RH} is less than the specified value, reset operations are not guaranteed.

(9) If either t_{RN1} or t_{RN2} is less than the specified value, internal reset operations may extend to cycles immediately preceding or following the period of desired reset operations.

(10) If either t_{WES} or t_{WEH} (t_{RES} or t_{REH}) is less than the specified value, write (read) disable operations are not guaranteed.

(11) If either t_{WEN1} or t_{WEN2} (t_{REN1} or t_{REN2}) is less than the specified value, internal write (read) disable operations may extend to cycles immediately preceding or following the period of desired disable operations.

Figure 1. Output Load for t_{AC}, t_{ACR}, t_{OH}, and t_{OHR}

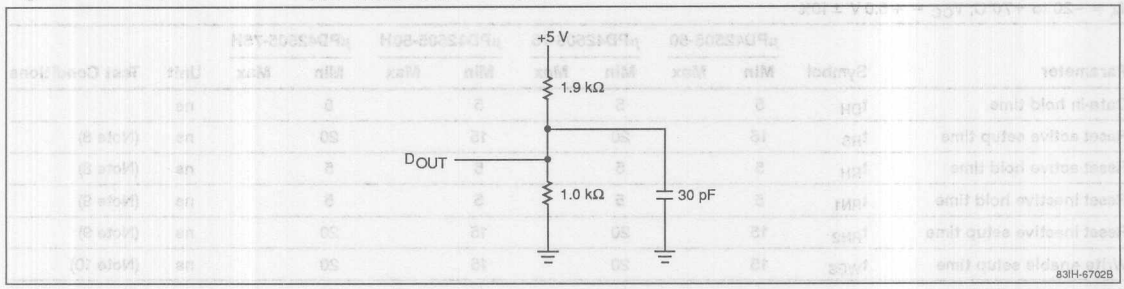


Figure 2. Output Load for t_{LZ} and t_{HZ}

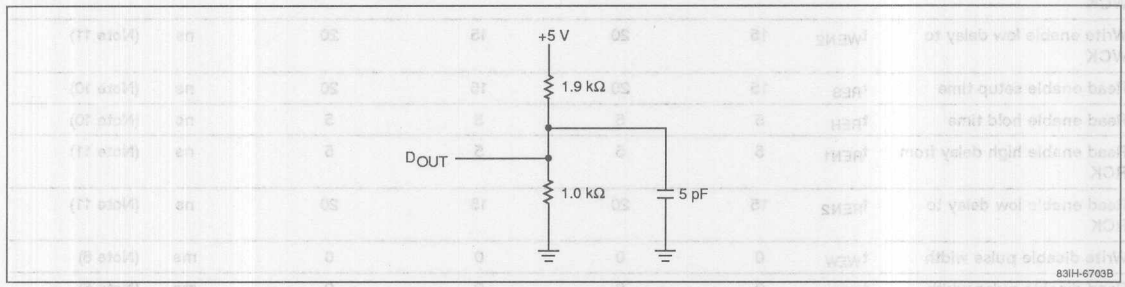


Figure 3. Input Timing

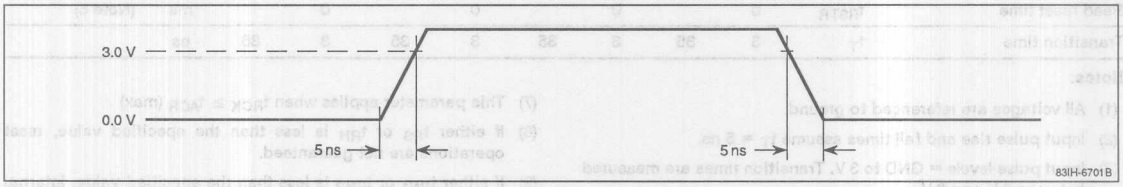
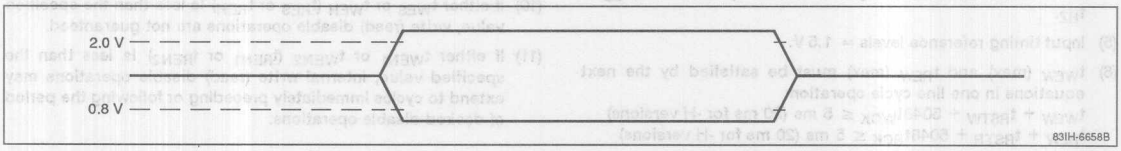
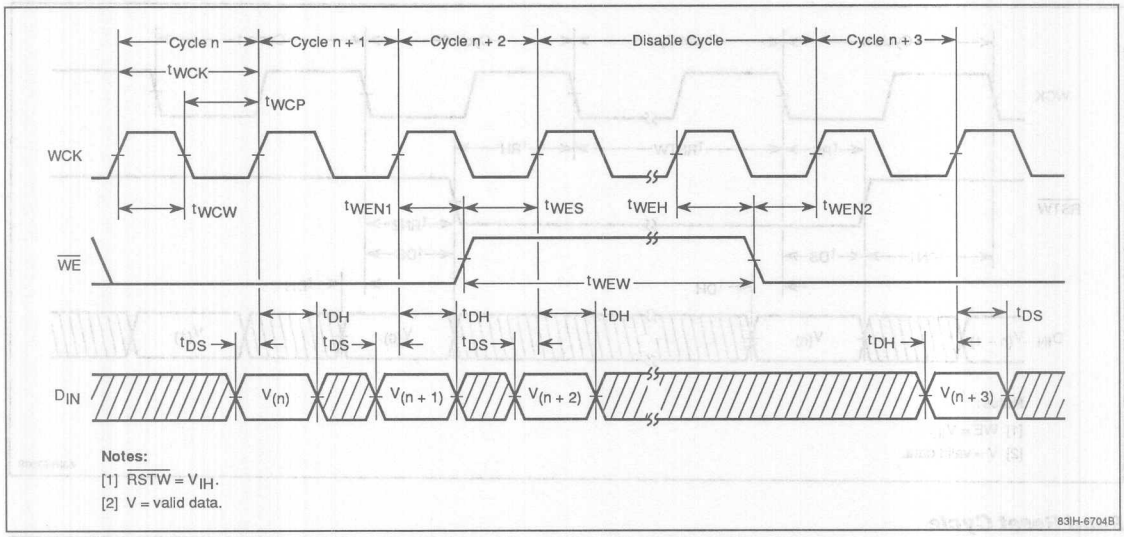


Figure 4. Output Timing



Timing Waveforms

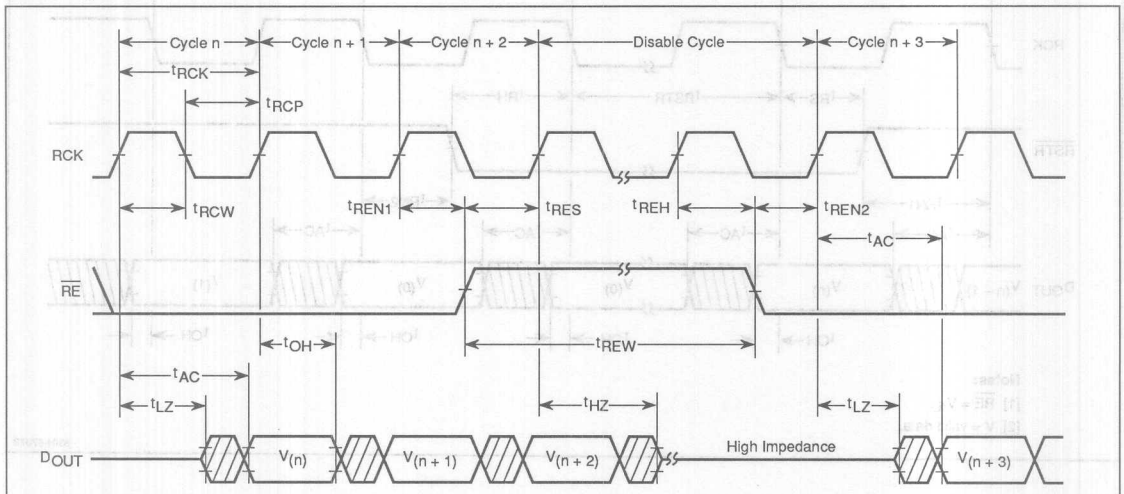
Write Cycle



Notes:
[1] $\overline{RSTW} = V_{IH}$.
[2] V = valid data.

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Read Cycle

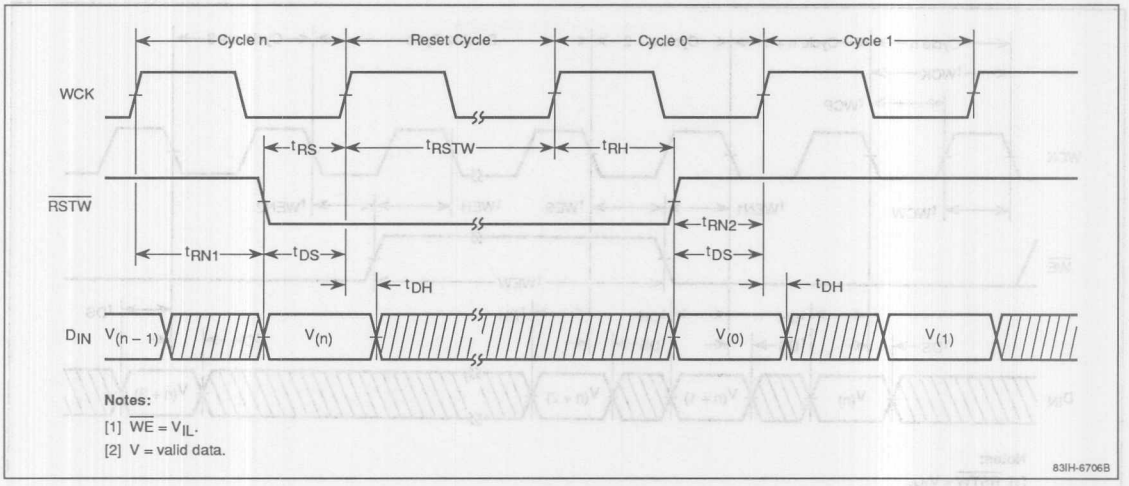


Notes:
[1] $\overline{RSTR} = V_{IH}$.
[2] V = valid data.

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Timing Waveforms (cont)

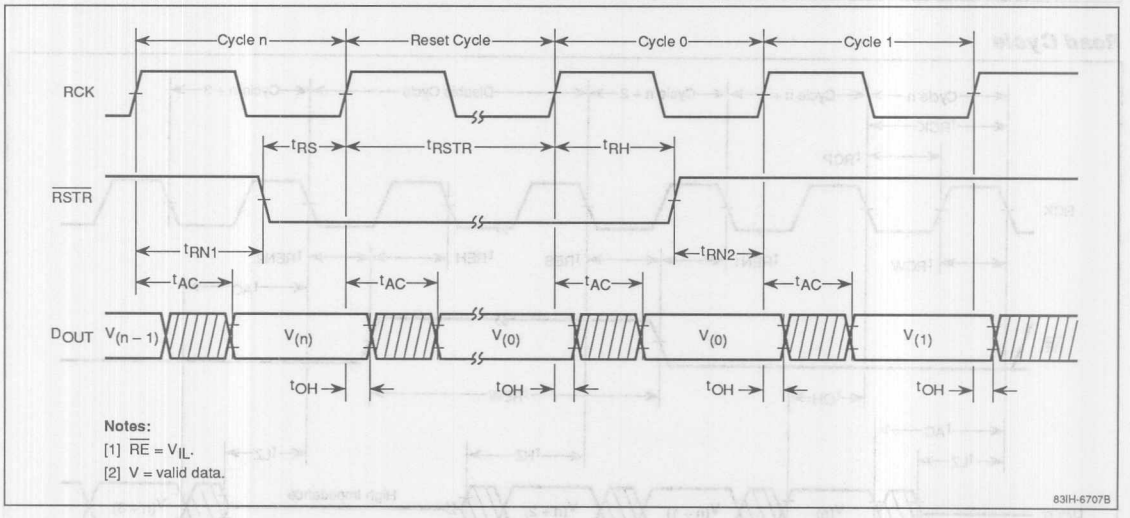
Write Reset Cycle



Notes:
[1] $\overline{WE} = V_{IL}$.
[2] V = valid data.

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Read Reset Cycle

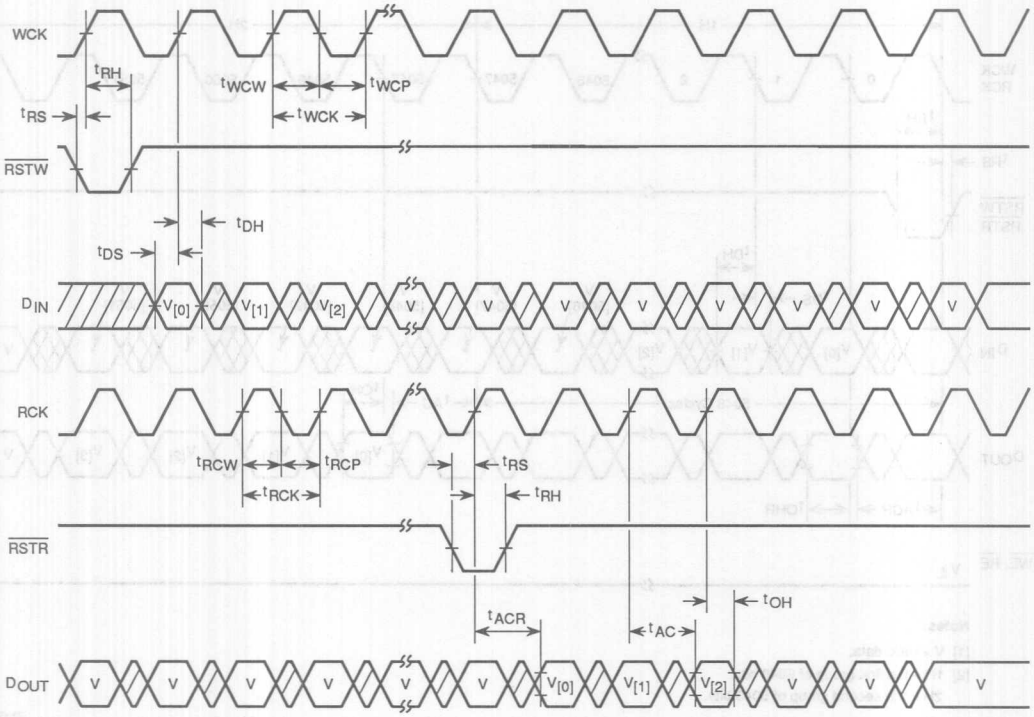


Notes:
[1] $\overline{RE} = V_{IL}$.
[2] V = valid data.

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Timing Waveforms (cont)

Time Axis Conversion Cycle



Notes:

[1] $\overline{WE} = \overline{RE} = V_{IL}$

[2] V = valid data.

[3] Read cycles commence from the rising edge of RCK. For the first cycle in a group of reset cycles, the read access time is defined as t_{ACR}. In all other cycles, t_{AC} defines the read access time.

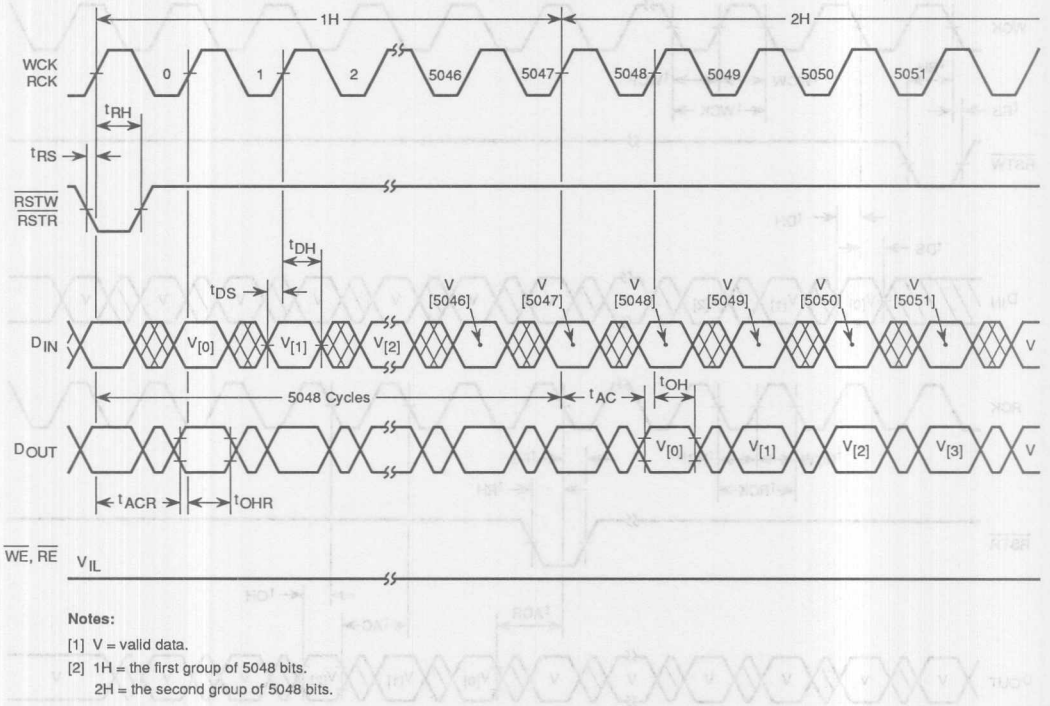
[4] Write data is strobed into the device on the rising edge of WCK at the end of a cycle.

83vG-7177B

3

Timing Waveforms (cont)

5048-Bit Delay Line Cycle



Notes:

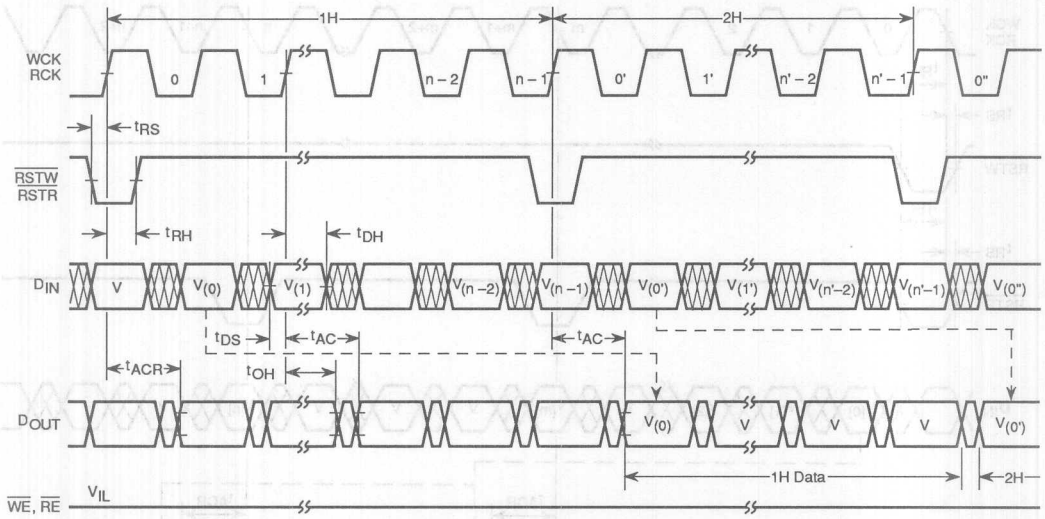
[1] V = valid data.

[2] 1H = the first group of 5048 bits.
2H = the second group of 5048 bits.

83vG-7178B

Timing Waveforms (cont)

n-Bit Delay Line Cycle



Notes:

[1] V = valid data

[2] 1H = the first group of bits. 2H = the second group of n' bits.

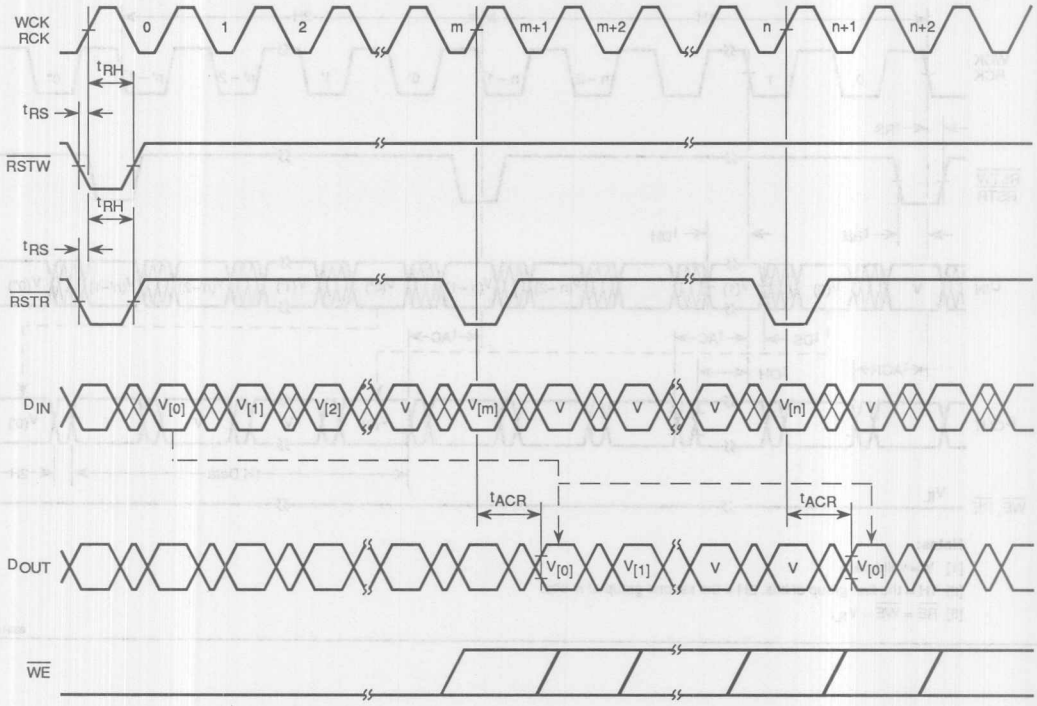
[3] $\overline{RE} = \overline{WE} = V_{IL}$.

83IH-6717B

3

Timing Waveforms (cont)

Re-Read Cycle



Notes:

[1] $\overline{RE} = V_{IL}$

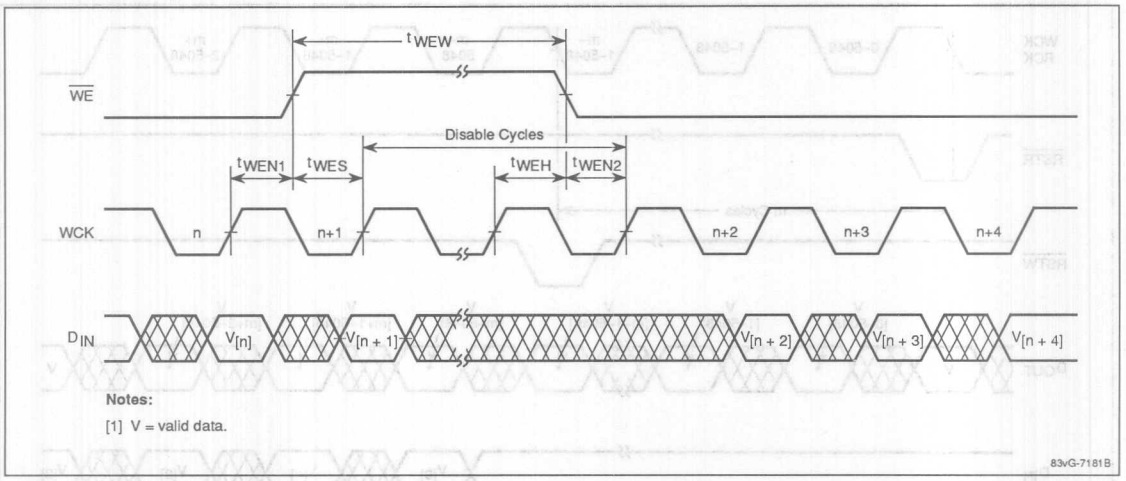
[2] V = valid data.

[3] The data stored in any location can be re-read as many times as desired, within a period of 5 ms following the writing of data into that location, provided that a second write cycle has not rewritten new data into that location.

83vG-7176B

Timing Waveforms (cont)

Write Disable Cycle

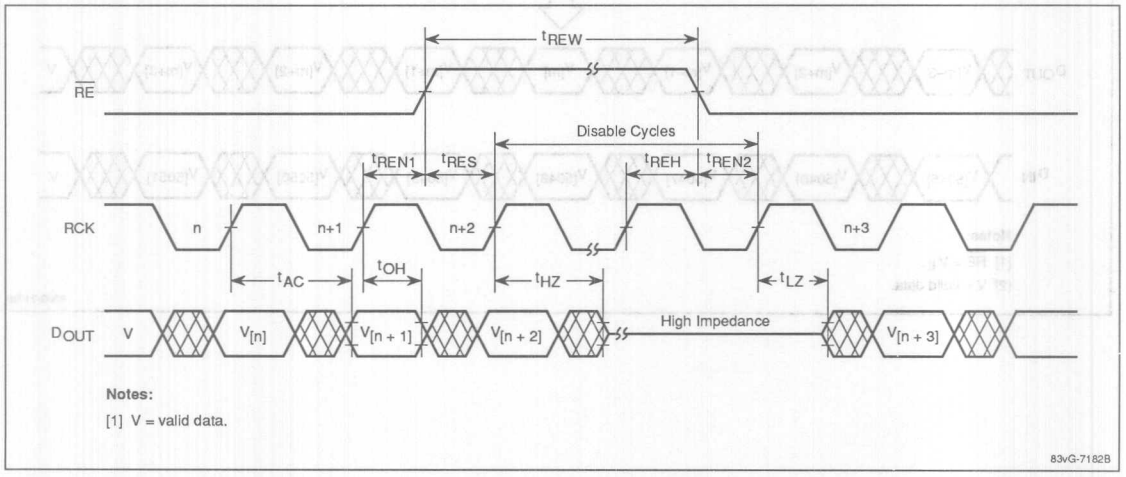


Notes:

[1] V = valid data.

83vG-7181B

Read Disable Cycle



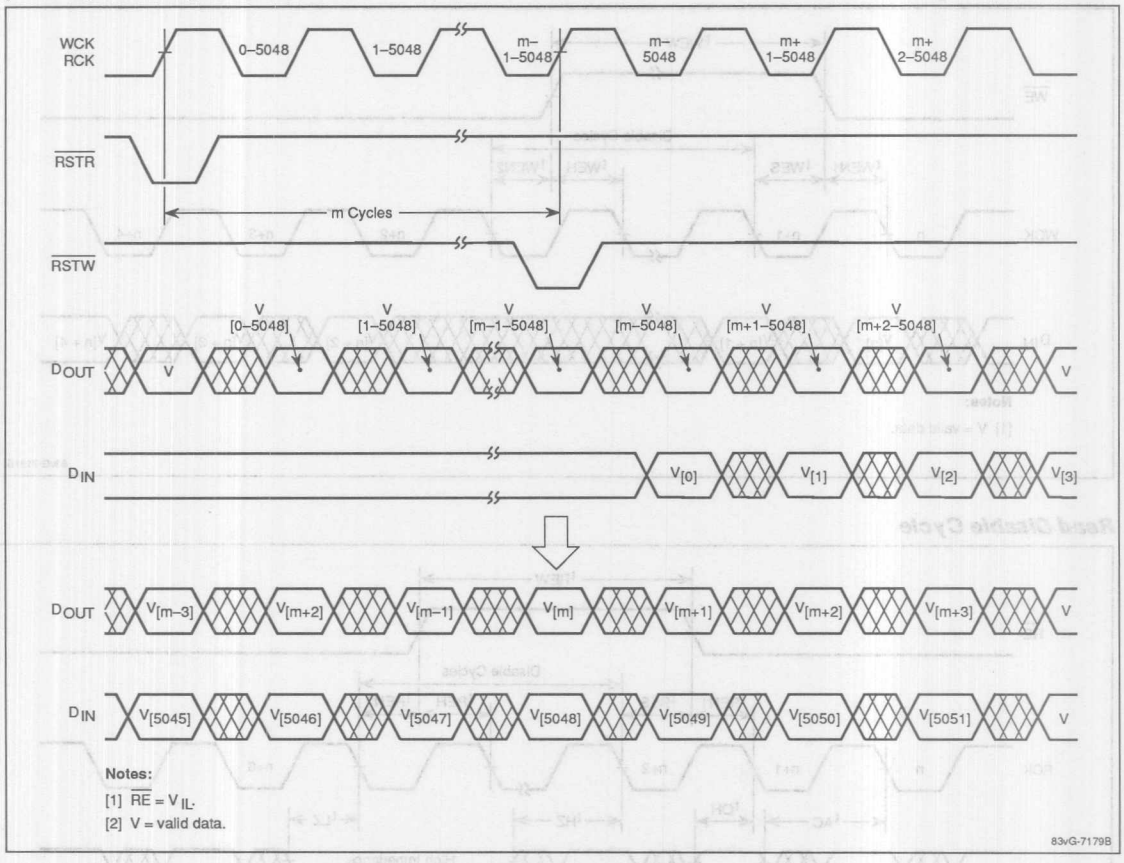
Notes:

[1] V = valid data.

83vG-7182B

Timing Waveforms (cont)

(5048-m)-Bit Delay Line No. 1



Notes:

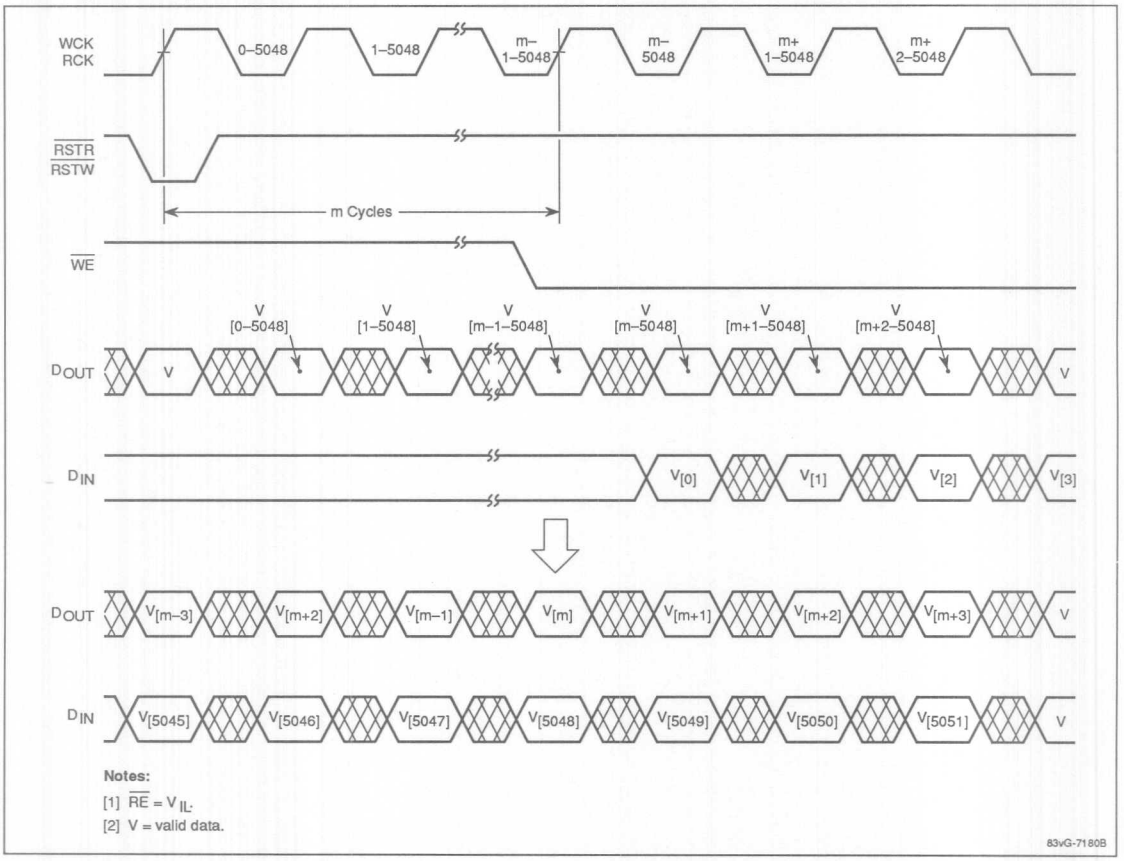
[1] $\overline{RE} = V_{IL}$.

[2] V = valid data.

83vG-7179B

Timing Waveforms (cont)

(5048-m)-Bit Delay Line No. 2



Notes:

[1] $\overline{RE} = V_{IL}$.

[2] V = valid data.

83vG-7180B



Description

The μPD42270 is a field buffer designed for NTSC TV applications and for other applications where serial data is needed. Equipped with four planes of 263-line by 910-bit storage, the μPD42270 can execute serial write and read cycles on any of the 263 lines. Within a line, four planes of 910 bits each may be written or read at the NTSC sampling rate of $4f_{SC}$.

Each of the four planes in the μPD42270 is equipped with two ports, one each for the write and read data registers. Each of the registers is split into two 455-bit segments but functions as if it were organized as one scan line of 910 bits. Independent control of write and read operation makes it possible for the device to operate synchronously or asynchronously at a clock frequency of 14.3 MHz or higher.

The synchronous option simplifies interframe luminance (Y) and chrominance (C) separation and interfield noise reduction and makes it easy to obtain a one-field delay line for digital TV and VCR applications requiring NTSC $4f_{SC}$ sampling. To obtain a very long delay, field length can be configured from 260 to 263 lines and line length of the last line from 896 to 910 bits.

The asynchronous option is useful in applications such as frame synchronization and time base correction, where line jump, line hold, line reset and pointer clear functions are required to support special effects in TV field processing.

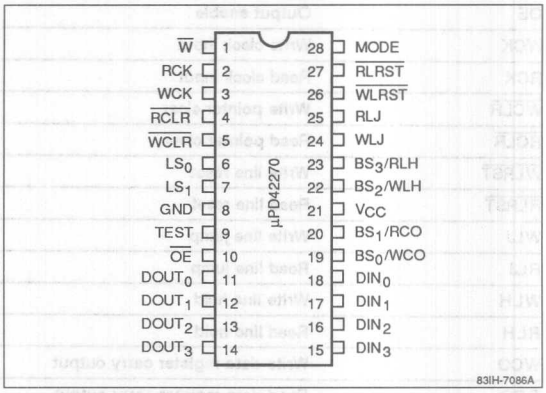
Regular refreshing of the device's dynamic storage cells is performed automatically by an internal circuit. All inputs and outputs, including clocks, are TTL-compatible. The μPD42270 is packaged in a 400-mil, 28-pin plastic DIP and is guaranteed for operation at −20 to +70°C.

Ordering Information

Part Number	Access Time (max)	Cycle Time (min)	Package
μPD42270C-60	40 ns	60 ns	28-pin plastic DIP

Pin Configuration

28-Pin Plastic DIP



Features

- Three functional blocks
  - — Four 263-line x 910-bit storage planes
  - — Four 910-bit write registers, one for each plane
  - — Four 910-bit read registers, one for each plane
- Two data ports: serial write and serial read
- Asynchronous operation
  - — Dual-port accessibility
  - — Carry-out feature to indicate position of scan line
  - — Line jump, line hold, line reset, and pointer clear functions
- Synchronous operation
  - — Variable field length: from 260 to 263 lines
  - — Variable last line length: from 896 to 910 bits
- Automatic refreshing
- CMOS technology
- Fully TTL-compatible inputs, outputs, and clocks
- Three-state outputs
- Single + 5-volt power supply
- On-chip substrate bias generator
- Standard 400-mil, 28-pin plastic DIP packaging

3

Pin Identification

Symbol	Function
D_{IN0} - D_{IN3}	Write data inputs
D_{OUT0} - D_{OUT3}	Read data outputs
$\overline{W}$	Write enable
$\overline{OE}$	Output enable
WCK	Write clock input
RCK	Read clock input
$\overline{WCLR}$	Write pointer clear
$\overline{RCLR}$	Read pointer clear
$\overline{WLRST}$	Write line reset
$\overline{RLRST}$	Read line reset
WLJ	Write line jump
RLJ	Read line jump
WLH	Write line hold
RLH	Read line hold
WCO	Write data register carry output
RCO	Read data register carry output
LS_0 - LS_1	Line select inputs
BS_0 - BS_3	Bit select inputs
MODE	Synchronous/asynchronous control
GND	Ground
V_{CC}	+5-volt power supply
TEST	Test pin (connect to GND in system)

Pin Functions

D_{IN0} - D_{IN3}. These pins function as write data inputs, e.g., for $4f_{SC}$ composite color or brightness signals.

D_{OUT0} - D_{OUT3}. These pins are three-state read data outputs.

$\overline{W}$. A low level on $\overline{W}$ enables write operation. $\overline{W}$ must be kept low throughout the entire scan line to ensure that data is stored serially; if $\overline{W}$ goes high any time during the WCK clock sequencing for a line, write operation will be disabled for the half of the line (455 bits) being written. The write address pointer increments in synchronization with WCK, regardless of $\overline{W}$.

$\overline{OE}$. This signal controls read data output. When $\overline{OE}$ is low, read data is output on D_{OUT0}-D_{OUT3}. When $\overline{OE}$ is high, D_{OUT0} - D_{OUT3} are in a state of high impedance. The read address pointer is incremented by RCK, regardless of the signal level of $\overline{OE}$.

WCK The rising edge of WCK latches write data from D_{IN0} - D_{IN3}. Each time this signal is activated, the write bit pointer increments sequentially and 4 bits of data are sampled and loaded into the write register. Although the register functions as one scan line of 910 bits, data is moved into and out of it in blocks of 455 x 4 bits. While 455 serial write cycles are being executed in one-half of the register, the 455 addresses previously written to the other half are simultaneously transferred to storage. Writing continues in this manner, alternating between the two halves of the register. Automatic refreshing and data transfer timing decisions are made by the internal arbitration circuit after each block of 455 addresses has been written.

RCK. The rising edge of RCK initiates read operation. Each time this signal is activated, the bit pointer increments by 1 and serial read cycles are executed in the read register. Although the register functions as one scan line of 910 bits, data is moved into and out of it in blocks of 455 x 4 bits. While 455 serial read cycles are being executed in one-half of the register, the 455 addresses previously read out of the other half are replaced by data from the storage array. Reading continues in this manner, alternating between the two halves of the register. Automatic refreshing and data transfer timing decisions are made by the arbitration circuit after each block of 455 addresses has been read. In synchronous operation, WCK controls read cycles and RCK is not used.

$\overline{WCLR}$. When $\overline{WLRST}$ is high, $\overline{WCLR}$ can be brought low to clear the write pointers to address 0 of the data register and scan line 0 of the storage array. At least one rising edge of WCK must occur while $\overline{WCLR}$ is held low for a minimum of 3 μs to ensure clearing of both pointers. The clear function ends when $\overline{WCLR}$ goes high. If $\overline{WLRST}$ is still high, the next rising edge of WCK writes the data on D_{IN0} - D_{IN3} into address 0 of the write register.

$\overline{RCLR}$. When $\overline{RLRST}$ is high, $\overline{RCLR}$ can be brought low to clear the read pointers to address 0 of the data register and scan line 0 of the storage array (asynchronous operation only). At least one rising edge of RCK must occur while $\overline{RCLR}$ is held low for a minimum of 3 μs to ensure clearing of both pointers. The clear function ends when $\overline{RCLR}$ goes high. If $\overline{RLRST}$ is still high, the data from address 0 is read out on D_{OUT0} - D_{OUT3} and the next rising edge of RCK initiates data access from address 1.

$\overline{WLRST}$. This pin is used in synchronous or asynchronous operation to reset the bit pointer to address 0 of the line following the one to which the signal is applied. In standard write operation, the scan line pointer increments by 1 whenever the bit pointer reaches the last address of a line. If $\overline{WCLR}$ is high, $\overline{WLRST}$ can be brought low for a minimum of 3 μs to force an end-of-

line condition, whereby write cycles begin executing from address 0 of the next sequential scan line. When used in conjunction with WLH, $\overline{\text{WLRST}}$ resets the current scan line; when combined with WLJ, $\overline{\text{WLRST}}$ begins writing from address 0 of the line to which the scan line pointer is jumped.

$\overline{\text{RLRST}}$. This pin is valid in asynchronous operation and can be used to reset the bit pointer to address 0 of the read line following the one to which the signal is applied. In standard read operation, the scan line pointer increments by 1 whenever the bit pointer reaches the last address of a line. If $\overline{\text{RCLR}}$ is high, $\overline{\text{RLRST}}$ can be brought low for a minimum of 3 μs to force an end-of-line condition, whereby read cycles begin executing from address 0 of the next sequential scan line. When used in conjunction with RLH, $\overline{\text{RLRST}}$ resets the current scan line; when combined with RLJ, $\overline{\text{RLRST}}$ begins reading from address 0 of the line to which the scan line pointer is jumped.

WLJ. Each positive pulse of this signal increments the write scan line pointer by one line (asynchronous operation only). WLJ is sampled at the rising edge of WCK. If WLJ is high, a single jump is executed. If WLJ remains high, no further jumps occur. To jump again, WLJ must go low for at least one rising edge of WCK before going high again. It takes a minimum of two WCK cycles to complete a line jump. The first cycle senses the high level of WLJ and increments the scan line pointer. An additional WCK cycle with WLJ low is required to complete the function. If more than one line jump is needed, then the sequence must be repeated. A line jump occurs either when the current line has been completely filled or after $\overline{\text{WLRST}}$ has reset the write address. The new scan line can be calculated by n+11+1x (where "n" is the current line and "x" equals the number of positive WLJ pulses). Changes in the level of WLJ must be made when the bit pointer is between locations 229 and 909 of the current line and when $\overline{\text{WCLR}}$ and $\overline{\text{WLRST}}$ are high and WLH is low.

RLJ. Each positive pulse of this signal increments the read scan line pointer by one line (asynchronous operation only). RLJ is sampled at the rising edge of RCK. If RLJ remains high, a single line jump is executed. To jump again, RLJ must go low for at least one rising edge of RCK before going high again. It takes a minimum of two RCK cycles to complete a line jump. The first cycle senses the high level of RLJ and increments the scan line pointer. An additional RCK cycle with RLJ low is required to complete the function.If more than one line jump is needed, then this sequence must be repeated.

A line jump occurs either when the current line has been completely read or after $\overline{\text{RLRST}}$ has reset the read address. The new scan line can be calculated by n+1+x (where "n" is the current line and "x" equals the number of positive RLJ pulses).

Changes in the level of RLJ must be made when the bit pointer is between locations 682 and 909 of the previous line, or between 0 and 452 of the current line, and when $\overline{\text{RCLR}}$ and $\overline{\text{RLRST}}$ are high and RLH is low.

WLH. Once this input is applied, the write scan line pointer will hold its position even if successive write clocks are applied. The level of WLH is sampled at the rising edge of WCK and must be applied between locations 229 and 909 of the line to be held. The held line is released after 910 addresses have been rewritten or after $\overline{\text{WLRST}}$ resets the write line address. WLH is multiplexed with BS_2 and is valid in asynchronous operation only. WLH (high) must be input only when $\overline{\text{WCLR}}$ and $\overline{\text{WLRST}}$ are high and WLJ is low.

RLH. Once this input is applied, the read scan line pointer will hold its position even if successive read clocks are applied. The level of RLH is sampled at the rising edge of RCK and must be clocked between locations 682 and 909 of the line preceding the line to hold, or between locations 0 and 452 of the line to hold. The held line is released after 910 addresses have been read or after $\overline{\text{RLRST}}$ resets the read line address. RLH (high) must be input only when $\overline{\text{RCLR}}$ and $\overline{\text{RLRST}}$ are high and RLJ is low. RLH is multiplexed with BS_3 and is valid in asynchronous operation only.

WCO. When the bit pointer reaches address 909 of the write data register, this signal goes high for one WCK cycle. WCO is multiplexed with BS_0 and is valid in asynchronous operation only.

RCO. When the bit pointer reaches address 909 of the read data register, this signal goes high for one RCK cycle. RCO is multiplexed with BS_1 and is valid in asynchronous operation only.

BS_0 - BS_3. These pins control the number of bits in the last line of the field. The combined signals of BS_0-BS_3 set the line length from 896 to 910 bits in one-bit steps (table 1). The length of the last line can change for each field, but all four pins should not be set low. BS_0, BS_1, BS_2 and BS_3 are multiplexed with WCO, RCO, WLH and RLH, respectively, and are valid in synchronous operation only. In asynchronous operation, the line length is fixed at 910 bits.

LS_0 - LS_1. These pins control the number of lines for one field in either synchronous or asynchronous operation. The combined signals of LS_0 and LS_1 set the number of lines to 260, 261, 262, or 263 (table 2). The number of lines can be changed for each field.

MODE. This pin selects the operating mode. A low signal selects synchronous operation and a high signal selects asynchronous operation. If MODE is changed after power has been applied to the μPD42270, it is necessary to clear the address pointers by bringing $\overline{WCLR}$ and $\overline{RCLR}$ low. MODE can be changed at any time; however, data input in one mode may be unreliable in the other (see table 3 for valid pin functions).

Table 1. Line Length Adjustment

BS_3	BS_2	BS_1	BS_0	Number of Bits in the Last Line
L	L	L	L	Prohibited
L	L	L	H	896
L	L	H	L	897
L	L	H	H	898
L	H	L	L	899
L	H	L	H	900
L	H	H	L	901
L	H	H	H	902
H	L	L	L	903
H	L	L	H	904
H	L	H	L	905
H	L	H	H	906
H	H	L	L	907
H	H	L	H	908
H	H	H	L	909
H	H	H	H	910

Notes:

(1) LS_0 - LS_1 and BS_0 - BS_3 must be held at a stable high or low level to maintain the number of bits per scan line and the number of scan lines per field while the line pointer indicates the position between lines 258 and 262.

Table 2. Line Number Adjustment

LS_1	LS_0	Number of Lines
L	L	260
L	H	261
H	L	262
H	H	263

Notes:

(1) LS_0 - LS_1 and BS_0 - BS_3 must be held at a stable high or low level to maintain the number of bits per scan line and the number of scan lines per field while the line pointer indicates a position between lines 258 and 262.

Table 3. Valid Pin Functions According to Mode

Pin Name	Synchronous Mode (Note 1)	Asynchronous Mode (Note 2)
MODE	0	1
BS_0/WCO	BS_0	WCO
BS_1/RCO	BS_1	RCO
BS_2/WLH	BS_2	WLH
BS_3/RLH	BS_3	RLH
$\overline{RCLR}$	Invalid	Valid
RCK	Invalid	Valid
$\overline{RLRST}$	Invalid	Valid
$\overline{WCLR}$	Valid	Valid
WCK	Valid	Valid
$\overline{WLRST}$	Valid	Valid
WLJ	Invalid	Valid
RLJ	Invalid	Valid

Notes:

(1) Write and read cycles are controlled by $\overline{WCLR}$, WCK, and $\overline{WLRST}$ in synchronous operation.

(2) In asynchronous operation, write and read cycles are controlled independently.

Capacitance

T_A = 25°C; V_{CC} = +5.0 V ±10%; GND = 0 V; f = 1 MHz

Parameter	Symbol	Min	Typ	Max	Unit	Pins Under Test
Input capacitance	C_I			5	pF	D_{IN0} - D_{IN3}, $\overline{W}$, $\overline{OE}$, WCK, RCK, $\overline{WCLR}$, $\overline{RCLR}$, $\overline{WLRST}$, $\overline{RLRST}$, WLJ, RLJ, LS_0 - LS_1, BS_2/WLH, BS_3/RLH, MODE
I/O capacitance	$C_{I/O}$			8	pF	BS_0/WCO, BS_1/RCO
Output capacitance	C_O			7	pF	D_{OUT} - D_{OUT}

DEVICE OPERATION

The μPD42270 supports two operating modes to accommodate various NTSC TV applications. Depending on the logic level of the MODE pin, the device will execute either synchronous or asynchronous write and read cycles on the addresses specified by the internal address pointers. When selecting the mode after power-on, it is necessary to reset these pointers to starting address 0 using $\overline{WCLR}$ and $\overline{RCLR}$. The level of MODE may be changed at any time.

Synchronous Mode

In synchronous mode, write and read cycles are executed simultaneously by $\overline{WCLR}$, $\overline{WLRST}$, WCK, $\overline{W}$ and $\overline{OE}$ to create a delay line, which means that write and read addresses always coincide. After all lines within a field have been written, they then are read out as the device begins overwriting new data to the same addresses again. Field length may be configured from 260 to 263 lines and last line length from 896 to 910 bits by means of the LS and BS pins, respectively. Synchronous operation is useful in applications where a very long delay line is required and may be selected by setting MODE low.

Asynchronous Mode

In asynchronous mode, $\overline{WCLR}$, $\overline{WLRST}$, WCK and $\overline{W}$ control write cycles, while read cycles are controlled independently by $\overline{RCLR}$, $\overline{RLRST}$, RCK and $\overline{OE}$. Field length may be configured from 260 to 263 lines using LS_0 - LS_1. Line length remains fixed at 910 bits and BS_0-BS_3 are disabled to provide for the register carry out, line hold, and line jump functions. Asynchronous operation is useful for frame synchronization or time base correction and may be selected by setting MODE high.

Address Clear. Setting $\overline{WCLR}$ and $\overline{RCLR}$ low for a minimum of 3 μs during successive WCK and RCK cycles initializes the internal pointers to starting address 0 of the first scan line ($\overline{RCLR}$ is disabled in synchronous mode). Although address clear signals must meet the specifications for setup and hold times as measured from the rising edges of WCK and RCK, they are not dependent on the status of $\overline{W}$ or $\overline{OE}$. An address clear cycle cannot occur in conjunction with $\overline{WLRST}$ or $\overline{RLRST}$ line reset cycles.

Write Operation. Write cycles are executed in synchronization with WCK as $\overline{W}$ is held low. Bits are input sequentially into one of the two halves of the data register before being transferred to the storage array. Since data is transferred into the array in blocks of 455 x 4 bits, no data transfer occurs if $\overline{W}$ goes high to disable write operation before all 455 bits are written. Despite write operation being disabled, the internal bit pointer continues to increment with each successive write clock.

Read Operation. Read cycles are executed in synchronization with RCK (asynchronous operation only) or WCK (synchronous operation only) as $\overline{OE}$ is held low. If $\overline{OE}$ goes high any time during a cycle, the outputs are in a state of high impedance until OE returns low. Since the internal bit pointer increments by 1 in spite of read operation being disabled, it is always important to reset the write and read pointers using $\overline{WCLR}$ and $\overline{RCLR}$ prior to beginning or resuming operation at the first address location in the array.

Special Functions

Line Reset. A line reset is similar to an address clear cycle, except that it only affects the bit pointers within a line. While $\overline{WCLR}$ and $\overline{RCLR}$ are held high, $\overline{WLRST}$ or $\overline{RLRST}$ can be brought low for a minimum of 3 μs during successive WCK or RCK cycles to reset the bit pointer to address 0 of the scan line. At the completion of the reset cycle, the next sequential scan line will be selected unless line hold (WLH or RLH) or line jump (WLJ or RLJ) are also used. See $\overline{WLRST}$ and $\overline{RLRST}$ for more detail.

A combination of line reset and an address clear cycle must be separated by at least one serial clock cycle. The timing relationship of WCLR, $\overline{WLRST}$ and WCK (or RCLR, $\overline{RLRST}$ and RCK) is shown in figure 1.

In asynchronous operation, $\overline{WLRST}$ and $\overline{RLRST}$ independently reset the write and read bit pointers. During synchronous operation, $\overline{WLRST}$ resets both pointers.

Line Jump. With the line jump function, it is possible to advance the current write or read line position according to the number of positive WLJ or RLJ pulses applied (see descriptions for the WLJ and RLJ pins). In this cycle, which is valid in asynchronous mode only, the scan line pointer resets to address 0 if the number of positive pulses causes the resulting line number (n+11+1x, where "n" is the current line number and "x" is the number of positive WLJ or RLJ pulses) to exceed the maximum line number (number of lines minus 1) specified by the LS_0 and LS_1 pins (table 2).

Line Hold. The line hold feature is available in asynchronous mode only and can be used to prevent the internal scan line pointers from incrementing to the next sequential address. The read and write line pointers may be held independently; however, restrictions pertaining to when this function can be initiated, detailed in the descriptions for the WLH and RLH pins, should be carefully followed.

Block Diagram

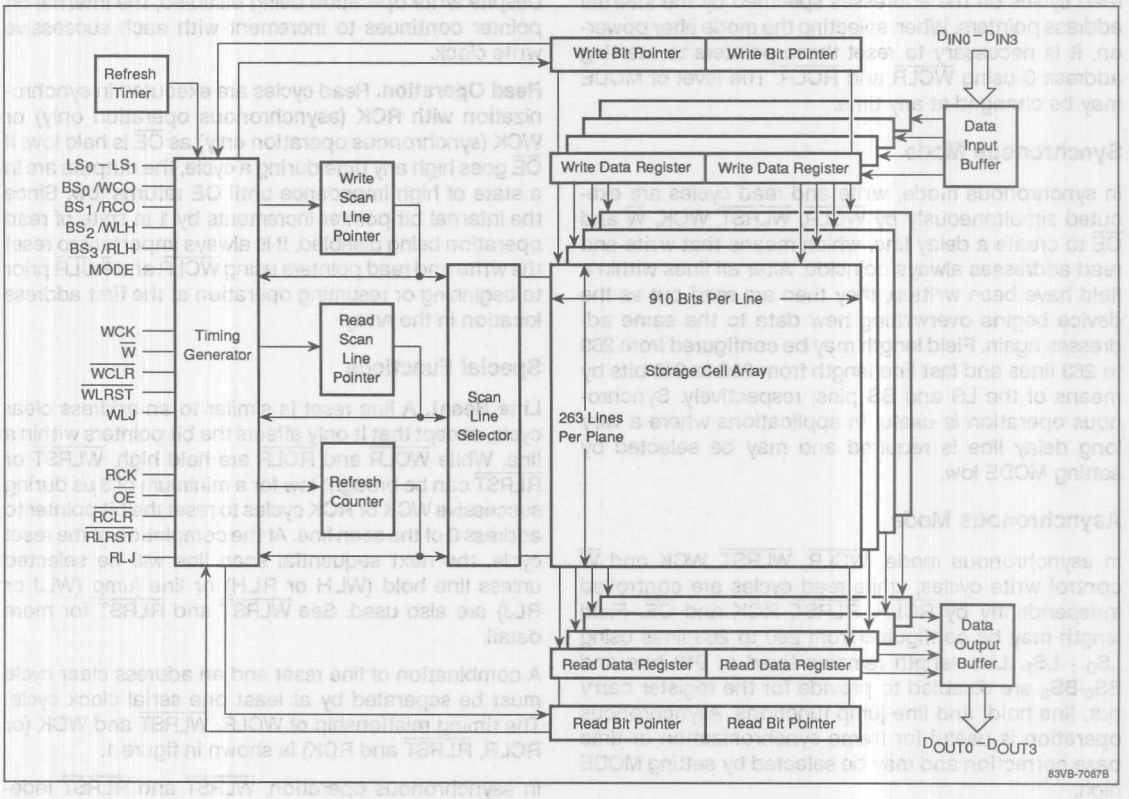
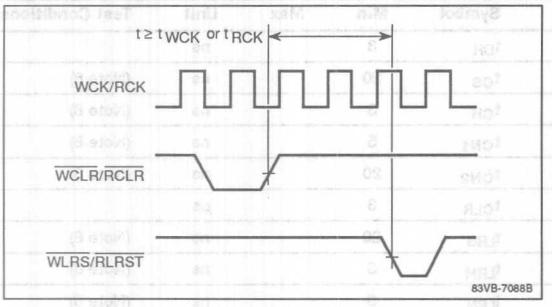


Figure 1. Separation of Clear and Reset Signals



Absolute Maximum Ratings

Supply voltage on any pin except V_{CC} relative to GND, V_{R1}	−1.5 to +7.0 V
Supply voltage on V_{CC} relative to GND, V_{R2}	−1.5 to +7.0 V
Operating temperature, T_{OPR}	−20 to +70°C
Storage temperature, T_{STG}	−55 to +125°C
Short-circuit output current, I_{OS}	50 mA
Power dissipation, P_D	1.5 W

Exposure to Absolute Maximum Ratings for extended periods may affect device reliability; exceeding the ratings could cause permanent damage. The device should be operated within the limits specified under DC and AC Characteristics.

3

Recommended Operating Conditions

Parameter	Symbol	Min	Typ	Max	Unit
Supply voltage	V_{CC}	4.5	5.0	5.5	V
Input voltage, high	V_{IH}	2.4		V_{CC}	V
Input voltage, low	V_{IL}	−1.5		0.8	V
Ambient temperature	T_A	−20		70	°C

DC Characteristics

T_A = −20 to +70°C; V_{CC} = +5.0 V ±10%; GND = 0 V

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions
Input leakage current	I_{IL}	−10		10	μA	V_{IN} = 0 V to V_{CC}; all other pins not under test = 0 V
Output leakage current	I_{OL}	−10		10	μA	D_{OUT} disabled; V_{OUT} = 0 V to V_{CC}
Output voltage, high	V_{OH}	2.4			V	I_{OH} = −1 mA
Output voltage, low	V_{OL}			0.4	V	I_{OL} = 2 mA
Standby current	I_{CC1}		6	20	mA	WCK, RCK = V_{IL}
Operating current	I_{CC2}		40	80	mA	t_{WCK} = t_{WCK} (min); t_{RCK} = t_{RCK} (min)

AC Characteristics

T_A = −20 to +70°C; V_{CC} = +5.0 V ±10%; GND = 0 V

Parameter	Symbol	Min	Max	Unit	Test Conditions
Access time from RCK	t_{AC}		40	ns	
Write clock cycle time	t_{WCK}	60		ns	(Note 5)
Write clock active pulse width	t_{WCW}	20		ns	
Write clock precharge time	t_{WCP}	20		ns	
Read clock cycle time	t_{RCK}	60		ns	(Note 5)
Read clock active pulse width	t_{RCW}	20		ns	
Read clock precharge time	t_{RCP}	20		ns	
Output hold time	t_{OH}	5		ns	
Output low impedance delay	t_{LZ}	5	40	ns	(Note 6)
Data output buffer high impedance delay	t_{HZ}	5	40	ns	(Note 7)
Input data setup time	t_{DS}	15		ns	

AC Characteristics (cont)

Parameter	Symbol	Min	Max	Unit	Test Conditions
Input data hold time	t_{DH}	3		ns	
$\overline{WCLR}$ ($\overline{RCLR}$) setup time before the rising edge of WCK (RCK)	t_{CS}	20		ns	(Note 8)
$\overline{WCLR}$ ($\overline{RCLR}$) hold time after the rising edge of WCK (RCK)	t_{CH}	3		ns	(Note 8)
$\overline{WCLR}$ ($\overline{RCLR}$) invalid hold time after the rising edge of WCK (RCK)	t_{CN1}	5		ns	(Note 8)
$\overline{WCLR}$ ($\overline{RCLR}$) invalid setup time before the rising edge of WCK (RCK)	t_{CN2}	20		ns	(Note 8)
$\overline{WCLR}$ ($\overline{RCLR}$) low level valid time	t_{CLR}	3		μs	
$\overline{WLRST}$ ($\overline{RLRST}$) setup time before the rising edge of WCK (RCK)	t_{LRS}	20		ns	(Note 8)
$\overline{WLRST}$ ($\overline{RLRST}$) hold time after the rising edge of WCK (RCK)	t_{LRH}	3		ns	(Note 8)
$\overline{WLRST}$ ($\overline{RLRST}$) invalid hold time after the rising edge of WCK (RCK)	t_{LRN}	5		ns	(Note 8)
$\overline{WLRST}$ ($\overline{RLRST}$) invalid setup time before the rising edge of WCK (RCK)	t_{LRN}	20		ns	(Note 8)
$\overline{WLRST}$ ($\overline{RLRST}$) low level valid time	t_{LRST}	3		μs	
$\overline{W}$ setup time before the rising edge of WCK	t_{WS}	20		ns	(Note 9)
$\overline{W}$ hold time after the rising edge of WCK	t_{WH}	3		ns	(Note 9)
$\overline{W}$ valid hold time after subline (1/2) switch	t_{WN1}	5		ns	(Note 9)
$\overline{W}$ valid setup time before subline (1/2) switch	t_{WN2}	20		ns	(Note 9)
WLH (RLH) setup time before the rising edge of WCK (RCK)	t_{LHS}	20		ns	
WLH (RLH) hold time after the rising edge of WCK (RCK)	t_{LHH}	3		ns	
WLH invalid hold time measured from the end of write cycle 227	t_{WHN1}	5		ns	
WLH invalid setup time measured before write cycle 0	t_{WHN2}	20		ns	
RLH invalid hold time measured from the end of read cycle 681	t_{RHN1}	5		ns	
RLH invalid setup time measured before read cycle 453	t_{RHN2}	20		ns	
WLJ (RLJ) setup time before the rising edge of WCK (RCK)	t_{LJS}	20		ns	
WLJ (RLJ) hold time after the rising edge of WCK (RCK)	t_{LJH}	3		ns	
WLJ hold time measured from the end of write cycle 227	t_{WJN1}	5		ns	
WLJ setup time measured before write cycle 0	t_{WJN2}	20		ns	
RLJ hold time measured from the end of read cycle 681	t_{RJN1}	5		ns	
RLJ setup time measured before read cycle 453	t_{RJN2}	20		ns	
$\overline{OE}$ setup time before the rising edge of RCK (WCK)	t_{OES}	20		ns	(Note 9)
$\overline{OE}$ hold time after the rising edge of RCK (WCK)	t_{OEH}	3		ns	(Note 9)
$\overline{OE}$ valid hold time after the rising edge of RCK (WCK)	t_{OEN1}	5		ns	(Note 9)
$\overline{OE}$ valid setup time before the rising edge of RCK (WCK)	t_{OEN2}	20		ns	(Note 9)
LS, BS setup time before WCK (RCK), line 258	t_{FSS}	0		ns	
LS, BS hold time after WCK (RCK), line 0	t_{FSH}	3		μs	
Write carry output high level delay	t_{WCLH}		40	ns	

AC Characteristics (cont)

Parameter	Symbol	Min	Max	Unit	Test Conditions
Write carry output low level delay	t_{WCHL}		40	ns	
Read carry output high level delay	t_{RCLH}		40	ns	
Read carry output low level delay	t_{RCHL}		40	ns	
Transition time	t_T	3	35	ns	(Note 4)

Notes:

(1) All voltages are referenced to GND

(2) Ac measurements assume t_T = 5 ns.

(3) Input timing reference levels = 1.5 V; input levels are measured between GND and 3.0 V; output levels are measured between 0.8 and 2.0 V. See figures 2 and 3.

(4) V_{IH} (min) and V_{IL} (max) are reference levels for measuring the timing of input signals. Transition times are measured between V_{IH} and V_{IL}.

(5) The minimum specifications are used only to indicate the cycle time at which proper operation over the full temperature range (T_A = −20 to 70°C) is assured.

(6) This delay is measured at −200 mV from the steady-state voltage with the load specified in figure 5.

(7) This delay is measured at the maximum steady-state output high voltage −200 mV or the minimum steady-state output low voltage +200 mV with the load specified in figure 5.

(8) For proper execution of the pointer clear and line reset functions, specifications for t_{CS}, t_{CH}, t_{CN1}, t_{CN2}, t_{LRS}, t_{LRH}, t_{LRN1} and t_{LRN2} must be met; otherwise, these functions may not affect the desired cycles or may affect adjacent cycles erroneously.

(9) If a $\overline{W}$ (or $\overline{OE}$) pulse does not satisfy the specifications for t_{WS}, t_{WH}, t_{WN1} and t_{WN2} (or t_{OES}, t_{OEH}, t_{OEN1} and t_{OEN2}), the write disable function (output high impedance) being executed may not affect the desired cycles or may affect adjacent cycles erroneously.

(10) For the μPD42270 to read new data, read operation must be delayed from write operation by at least 920 cycles. In those cases where the delay is less than 920 cycles, read data will vary as shown below:

Source of Read Data	Delay Between Write and Read Operation
Old data	0 to 450 cycles
Indeterminate (either old or new data)	451 to 919 cycles
New data	920 or more cycles

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Figure 2. Input Timing

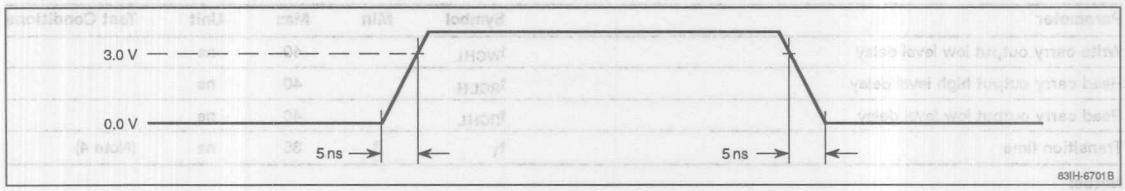


Figure 3. Output Timing

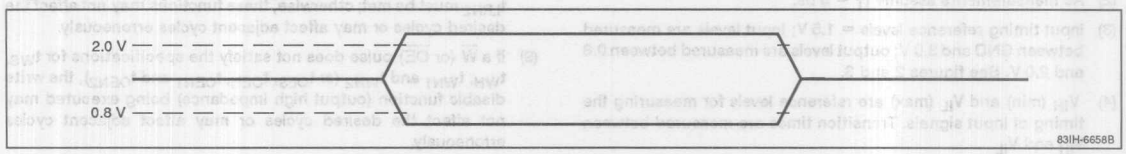


Figure 4. Output Loading for t_{AC}, t_{OH}, t_{WCLH}, t_{WCHL}, t_{RCLH}, t_{RCHL}

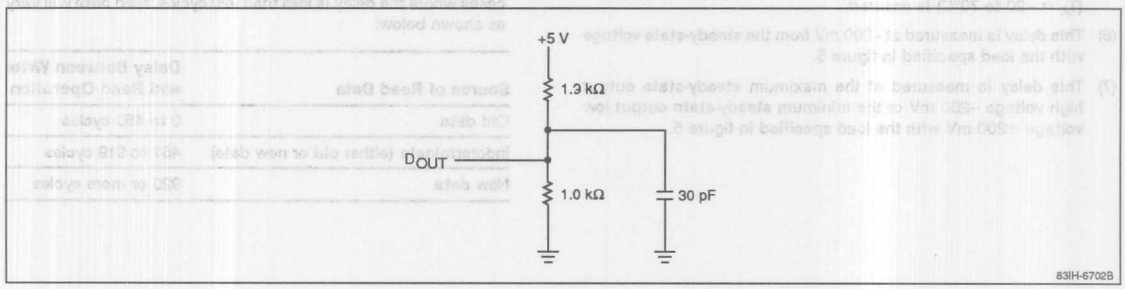
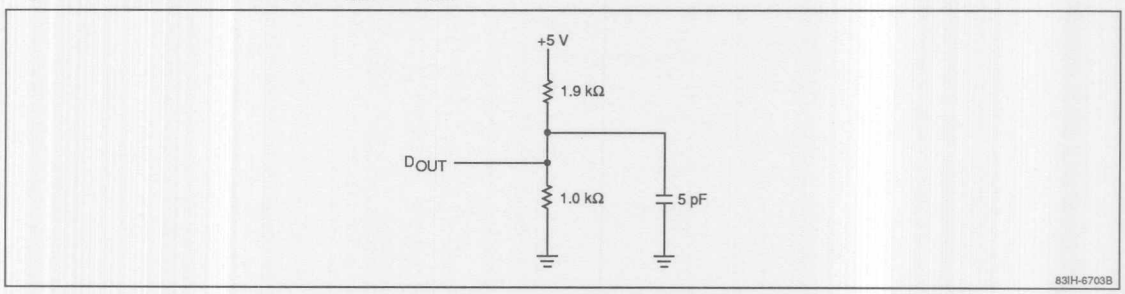
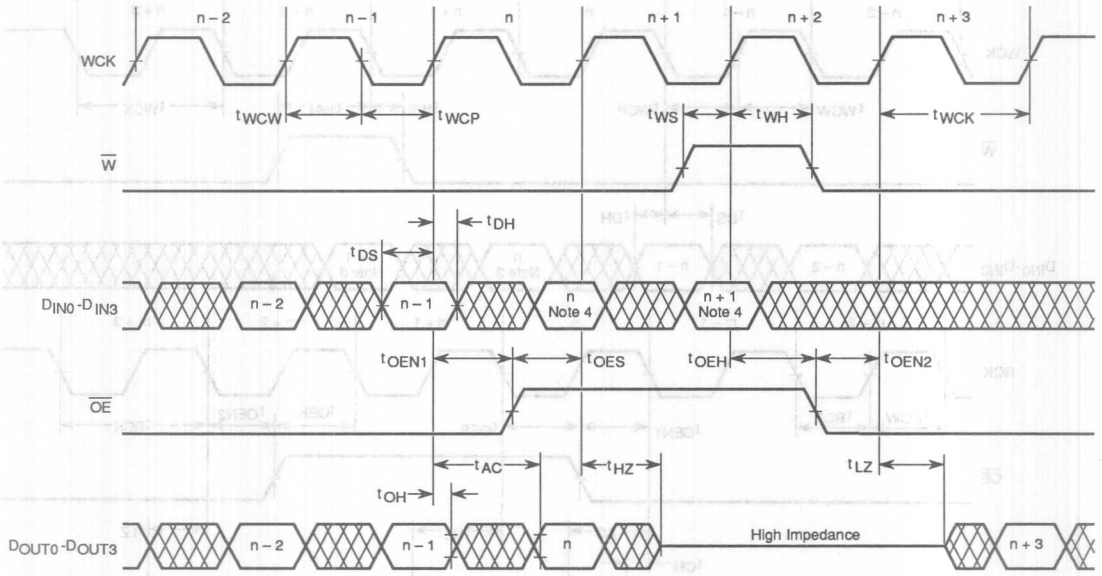


Figure 5. Output Loading for t_{LZ} and t_{HZ}



Timing Waveforms

Synchronous Write/Read Cycle



Notes:

[1] In synchronous mode, output data is delayed by one field from the input data.

[2] $\overline{WLRST}$ = $\overline{WCLR}$ = V_{IH}. MODE = V_{IL}. LS_0 and LS_1 = V_{IH} or V_{IL}. $\overline{RLRST}$, $\overline{RCLR}$, and RCK are "don't care" inputs.

[3] BS_0 - BS_3 = V_{IH} or V_{IL}.

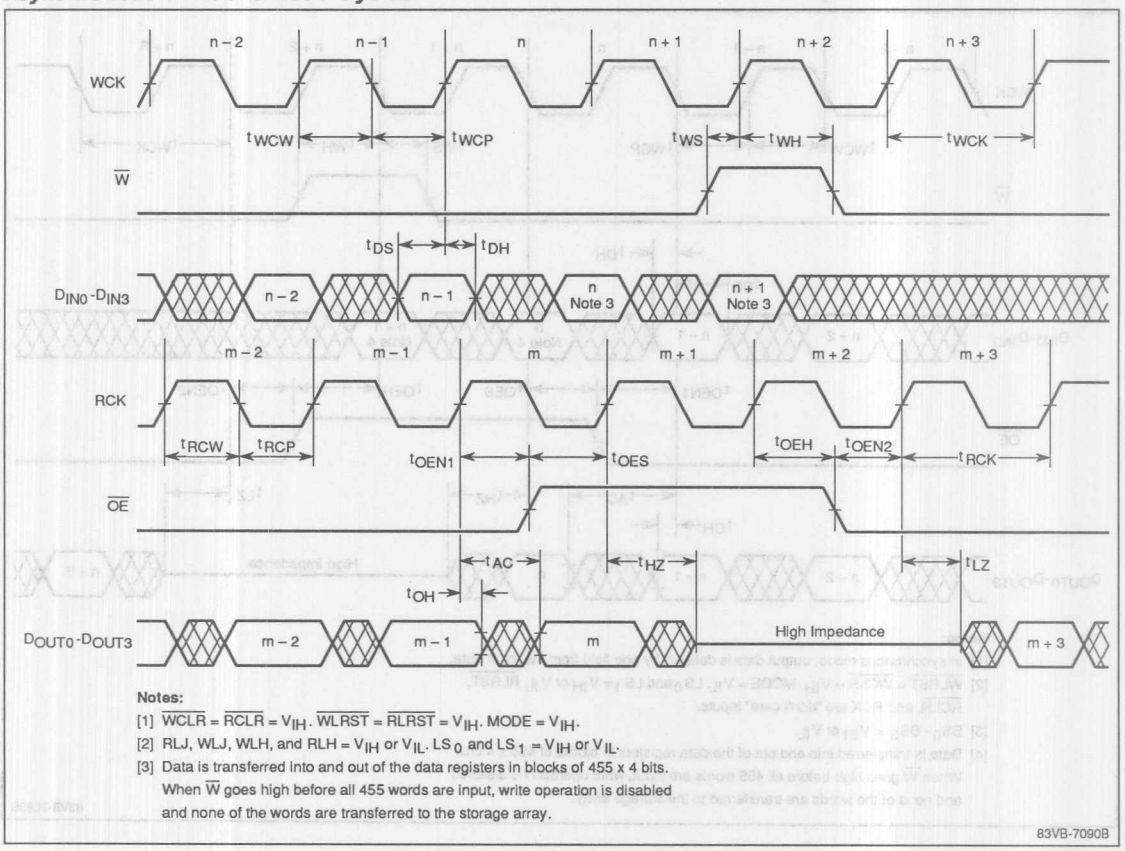
[4] Data is transferred into and out of the data registers in blocks of 455 x 4 bits. When $\overline{W}$ goes high before all 455 words are input, write operation is disabled and none of the words are transferred to the storage array.

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Timing Waveforms (cont)

Asynchronous Write and Read Cycles



Notes:

[1] $\overline{WCLR} = \overline{RCLR} = V_{IH}$. $\overline{WLRST} = \overline{RLRST} = V_{IH}$. MODE = V_{IH}.

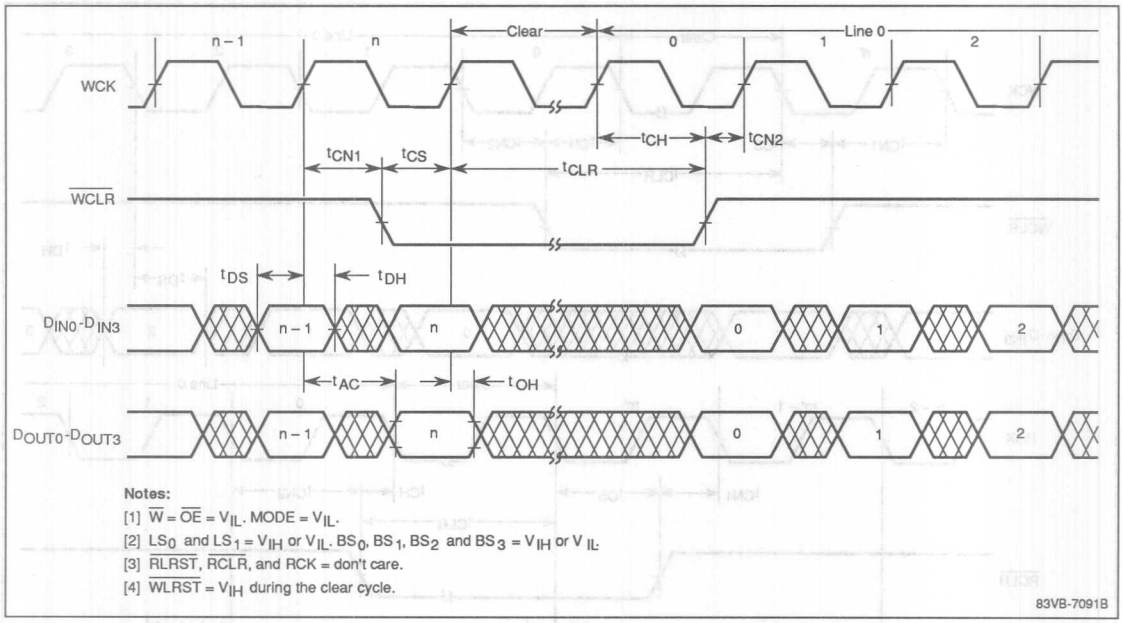
[2] RLJ, WLJ, WLH, and RLH = V_{IH} or V_{IL}. LS_0 and LS_1 = V_{IH} or V_{IL}.

[3] Data is transferred into and out of the data registers in blocks of 455 x 4 bits. When $\overline{W}$ goes high before all 455 words are input, write operation is disabled and none of the words are transferred to the storage array.

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Timing Waveforms (cont)

Synchronous Pointer Clear Cycle



Notes:

[1] $\overline{W} = \overline{OE} = V_{IL}$. MODE = V_{IL}.

[2] LS_0 and $LS_1 = V_{IH}$ or V_{IL}. BS_0, BS_1, BS_2 and $BS_3 = V_{IH}$ or V_{IL}.

[3] $\overline{RLRST}$, $\overline{RCLR}$, and RCK = don't care.

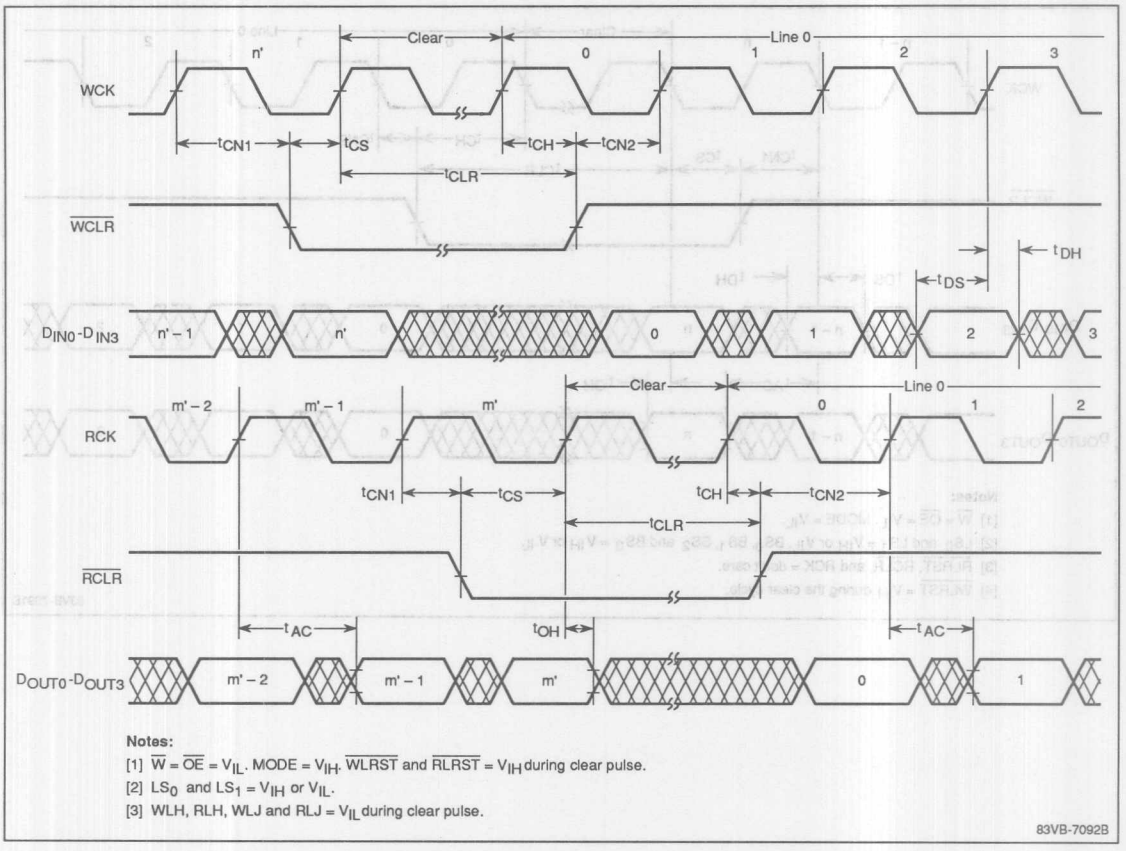
[4] $\overline{WLRST} = V_{IH}$ during the clear cycle.

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Timing Waveforms (cont)

Asynchronous Pointer Clear Cycle



Notes:

[1] $\overline{W} = \overline{OE} = V_{IL}$. MODE = V_{IH}. $\overline{WLRST}$ and $\overline{RLRST}$ = V_{IH} during clear pulse.

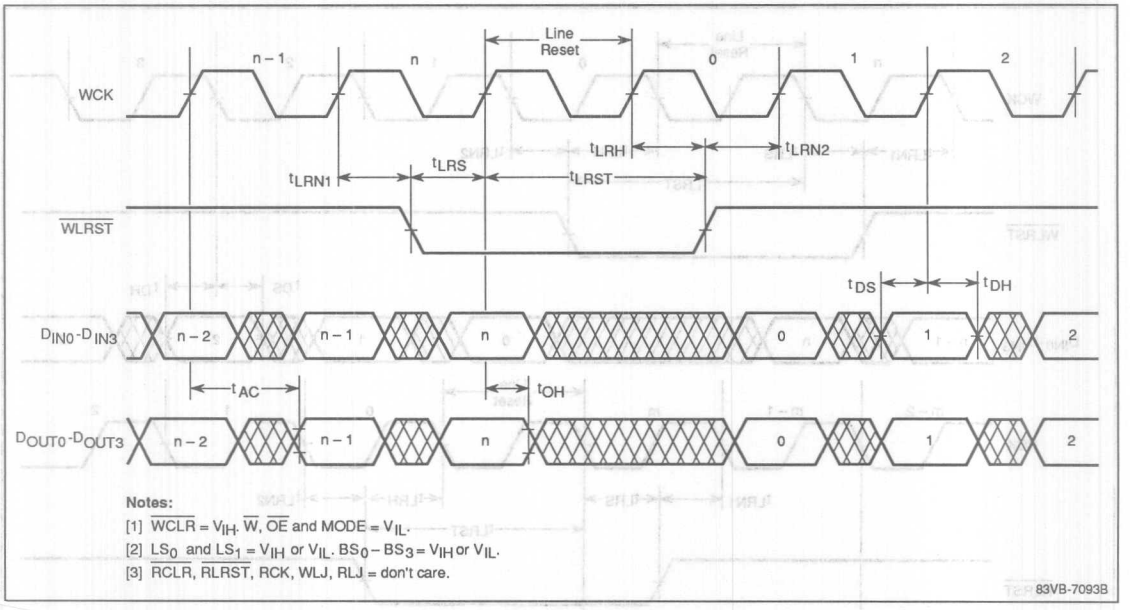
[2] LS_0 and LS_1 = V_{IH} or V_{IL}.

[3] WLH, RLH, WLJ and RLJ = V_{IL} during clear pulse.

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Timing Waveforms (cont)

Synchronous Line Reset Cycle



Notes:

[1] $\overline{WCLR} = V_{IH}$. $\overline{W}$, $\overline{OE}$ and MODE = V_{IL}.

[2] LS_0 and $\overline{LS_1} = V_{IH}$ or V_{IL}. $BS_0 - BS_3 = V_{IH}$ or V_{IL}.

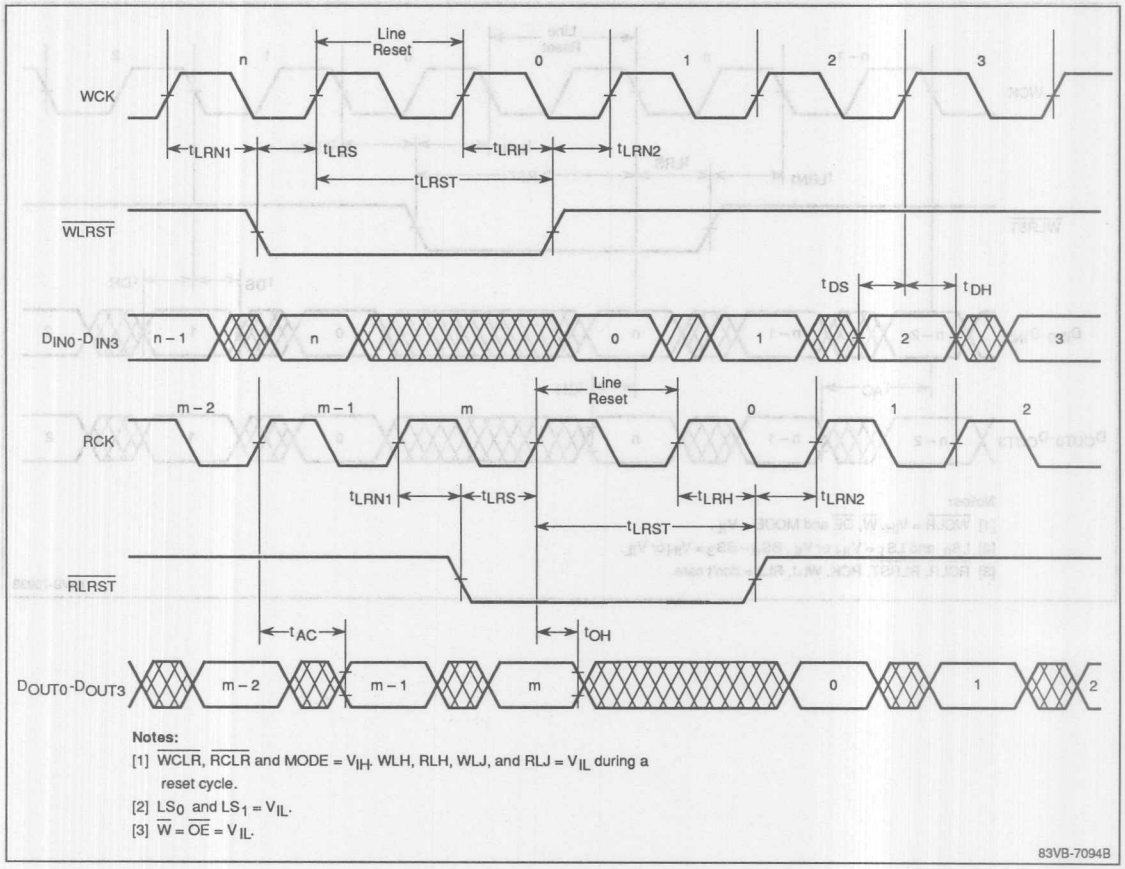
[3] $\overline{RCLR}$, $\overline{RLRST}$, RCK, WLJ, RLJ = don't care.

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Timing Waveforms (cont)

Asynchronous Line Reset Cycle



Notes:

[1] $\overline{WCLR}$, $\overline{RCLR}$ and MODE = V_{IH}. WLH, RLH, WLJ, and RLJ = V_{IL} during a reset cycle.

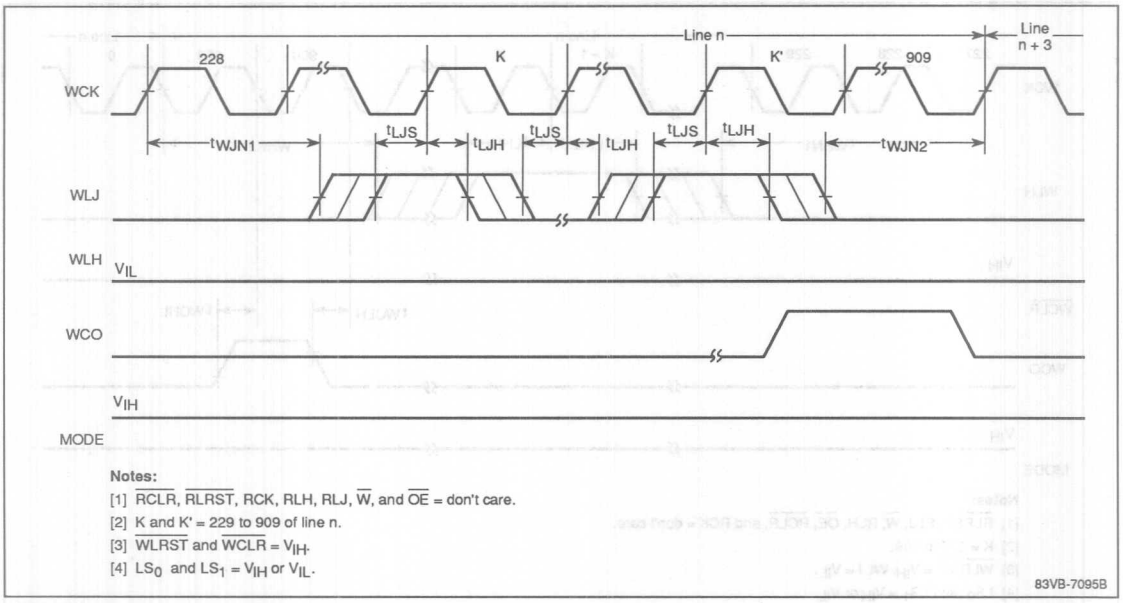
[2] LS_0 and LS_1 = V_{IL}.

[3] $\overline{W}$ = $\overline{OE}$ = V_{IL}.

83VB-7094B

Timing Waveforms (cont)

Write Line Jump Cycle



Notes:

[1] $\overline{RCLR}$, $\overline{RLRST}$, RCK, RLH, RLJ, $\overline{W}$, and $\overline{OE}$ = don't care.

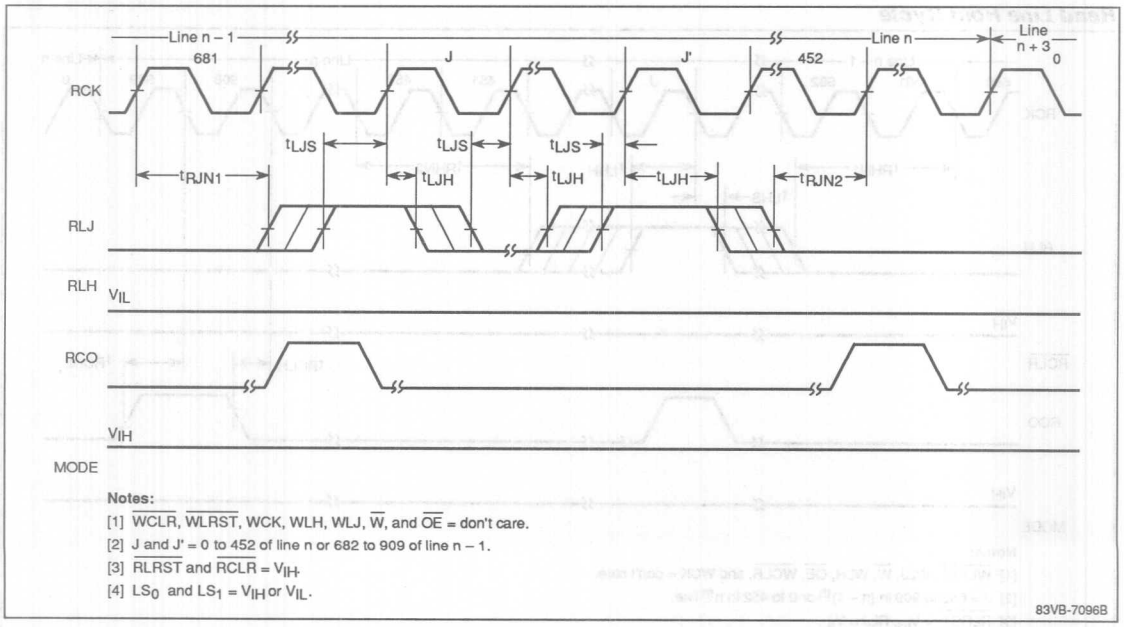
[2] K and K' = 229 to 909 of line n.

[3] $\overline{WLRST}$ and $\overline{WCLR}$ = V_{IH}.

[4] LS_0 and LS_1 = V_{IH} or V_{IL}.

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Read Line Jump Cycle



Notes:

[1] $\overline{WCLR}$, $\overline{WLRST}$, WCK, WLH, WLJ, $\overline{W}$, and $\overline{OE}$ = don't care.

[2] J and J' = 0 to 452 of line n or 682 to 909 of line n – 1.

[3] $\overline{RLRST}$ and $\overline{RCLR}$ = V_{IH}.

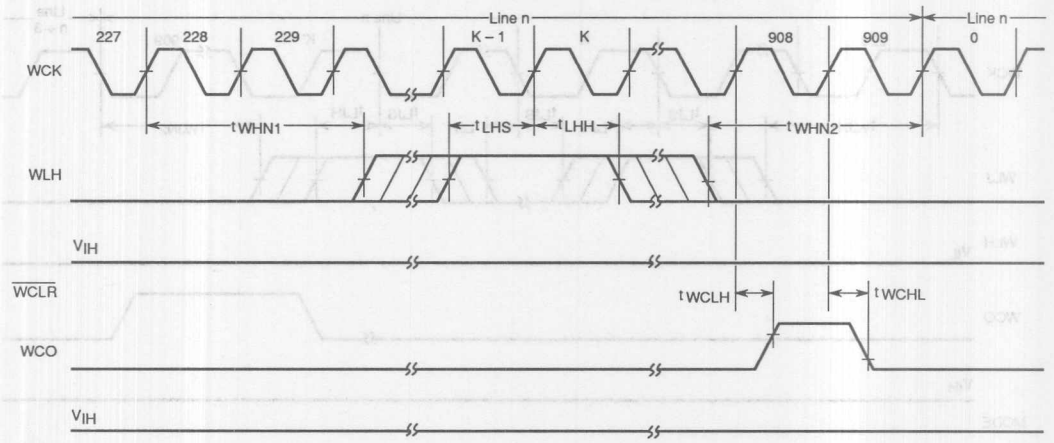
[4] LS_0 and LS_1 = V_{IH} or V_{IL}.

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Timing Waveforms (cont)

Write Line Hold Cycle



Notes:

[1] $\overline{RLRST}$, RLJ, $\overline{W}$, RLH, $\overline{OE}$, $\overline{RCLR}$, and RCK = don't care.

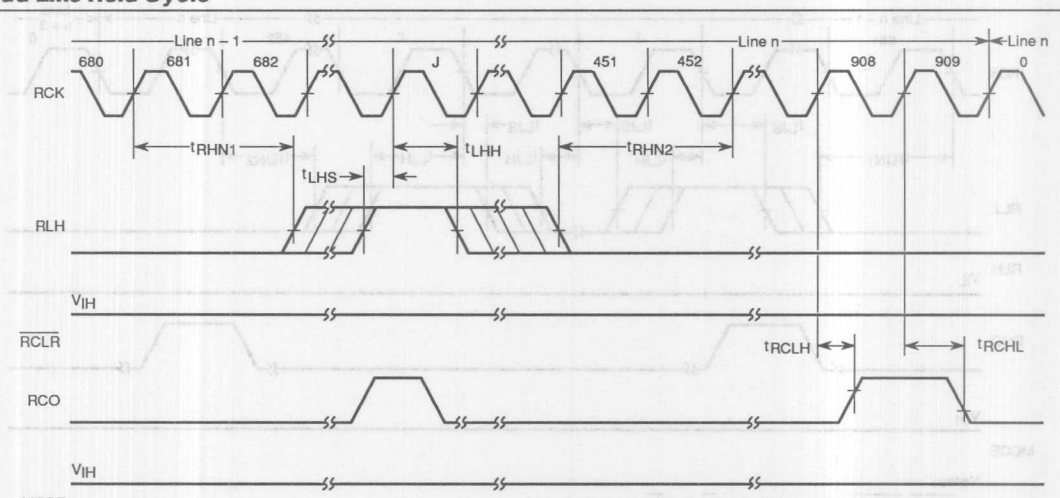
[2] K = 229 to 909.

[3] $\overline{WLRST}$ = V_{IH}. WLJ = V_{IL}.

[4] LS_0 and LS_1 = V_{IH} or V_{IL}.

83VB-7097B

Read Line Hold Cycle



Notes:

[1] $\overline{WLRST}$, WLJ, $\overline{W}$, WLH, $\overline{OE}$, $\overline{WCLR}$, and WCK = don't care.

[2] J = 682 to 909 in $(n-1)^{th}$ or 0 to 452 in n^{th} line.

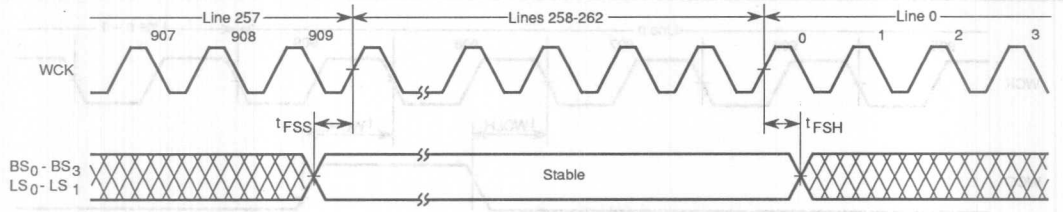
[3] $\overline{RLRST}$ = V_{IH}. RLJ = V_{IL}.

[4] LS_0 and LS_1 = V_{IH} or V_{IL}.

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Timing Waveforms (cont)

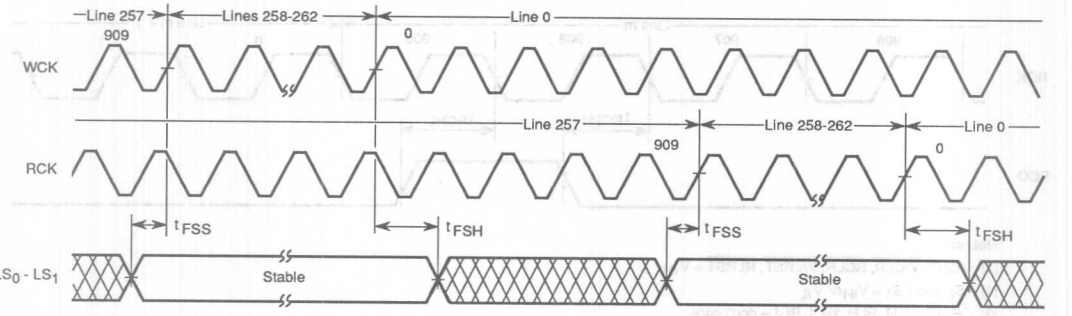
Synchronous Field Buffer Size Adjustment



Notes:
[1] $\overline{WLRST}$ and $\overline{WCLR}$ = V_{IH}.
[2] MODE = V_{IL}.
[3] $\overline{RLRST}$, $\overline{W}$, RCK, $\overline{RCLR}$, and $\overline{OE}$ = don't care.

83VB-7099B

Asynchronous Field Buffer Size Adjustment

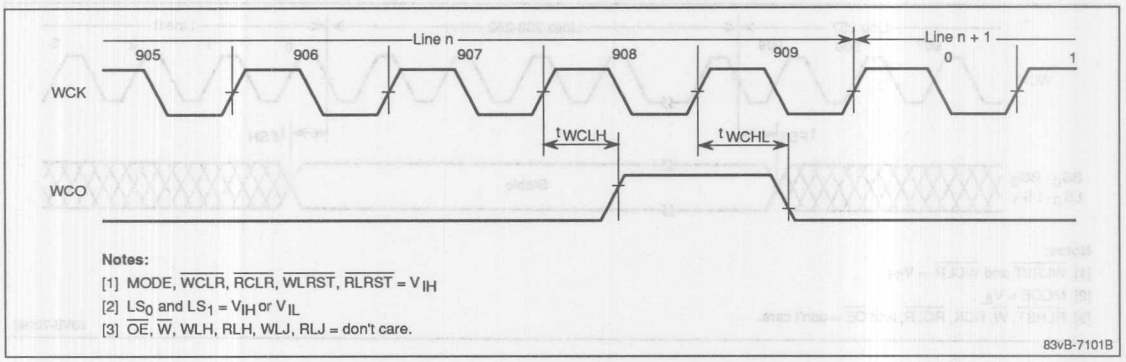


Notes:
[1] $\overline{WCLR}$, $\overline{RCLR}$, $\overline{WLRST}$, and $\overline{RLRST}$ = V_{IH}.
[2] MODE = V_{IH}. WLJ and RLJ = V_{IL}.
[3] $\overline{W}$, $\overline{OE}$, WLH, and RLH = don't care.

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Timing Waveforms (cont)

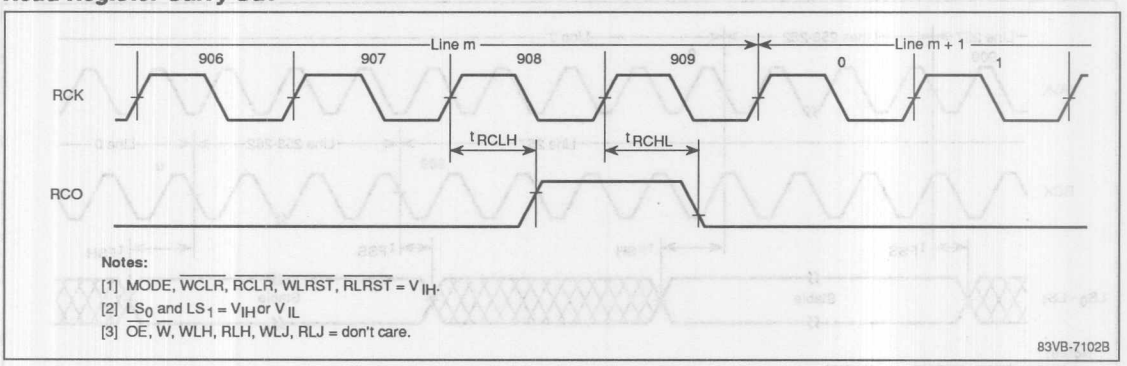
Write Register Carry Out



Notes:
[1] MODE, $\overline{WCLR}$, $\overline{RCLR}$, $\overline{WLRST}$, $\overline{RLRST}$ = V_{IH}
[2] LS_0 and LS_1 = V_{IH} or V_{IL}
[3] $\overline{OE}$, $\overline{W}$, WLH, RLH, WLJ, RLJ = don't care.

83vB-7101B

Read Register Carry Out



Notes:
[1] MODE, $\overline{WCLR}$, $\overline{RCLR}$, $\overline{WLRST}$, $\overline{RLRST}$ = V_{IH}.
[2] LS_0 and LS_1 = V_{IH} or V_{IL}
[3] $\overline{OE}$, $\overline{W}$, WLH, RLH, WLJ, RLJ = don't care.

83VB-7102B

APPLICATION EXAMPLES

Delay Line

The synchronous mode may be used to create a full-field delay line with a fixed length (figures 6 and 7). Useful video applications include field interpolation, interframe noise reduction, and separation of luminance (Y) and chrominance (C) signals. In these applications, field buffer size is determined by the logic levels applied to pins LS_0 - LS_1 and BS_0 - BS_3. The former allows variation of the number of lines from 260 to 263, while the latter controls the actual line length at 896 to 910 bits for the last line. The actual delay between data being written into D_{IN} and read on D_{OUT} is controlled by the WCK clock period and the con figured size of the buffer.

Frame Synchronization or Time Base Correction

The μPD42270 has the capability of executing asyn chronous write and read cycles by independently clocking WCK and RCK, respectively. The feature is useful in applications requiring frame synchronization, time base correction or buffering, where WCK, RCK, $\overline{WCLR}$ and $\overline{RCLR}$ may all have variable time periods. In addition, the write carry out (WCO) and read carry out (RCO) options give a positive indication when the bit pointer reaches the end of the line.

Vertical or Horizontal Image Compression and Expansion

Vertical compression and expansion of the video image may be accomplished by means of the line jump or line hold functions. Compression occurs when WLJ or RLJ are used to jump over lines that are not to be displayed. Expansion occurs when the WLH or RLH line hold signals are used to display a line multiple times.

Horizontal compression and expansion can be achieved by modifying the cycle time of the WCK and RCK clocks, and by using the $\overline{WLRST}$ and $\overline{RLRST}$ line reset signals.

Figure 6. Example of Delay Line

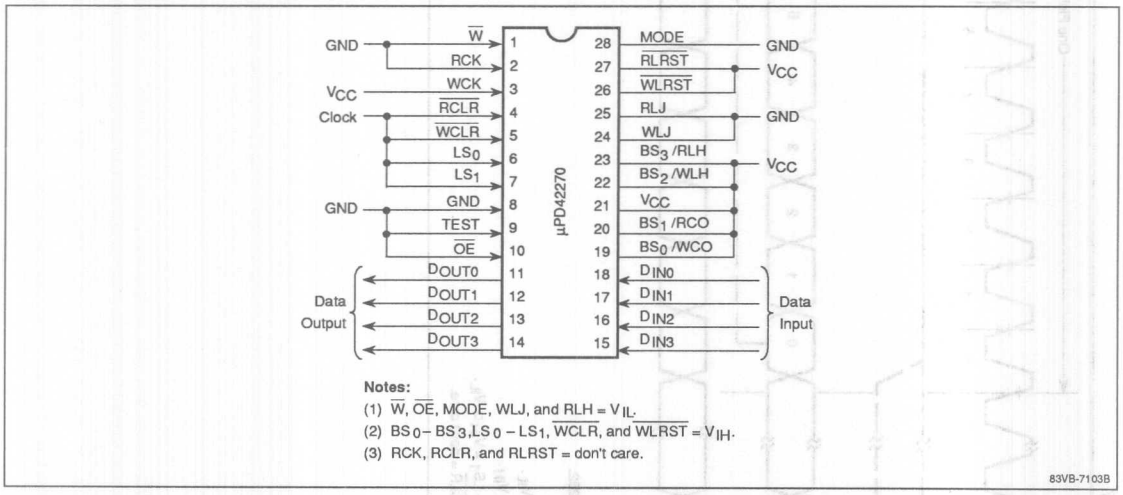


Figure 7. Delay Line Timing

Notes:

[1] J = 910 n + m.

[2] n = 259, 260, 261, or 262.

[3] m = 896 to 910.

[4] MODE, $\overline{W}$, and $\overline{OE}$ = V_{IL}.

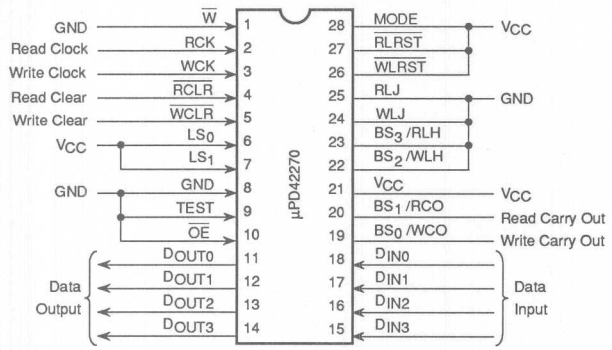
[5] $\overline{WLRST}$ and $\overline{WCLR}$ = V_{IH}.

[6] $BS_0 - BS_3$ and $LS_0 - LS_1$ = V_{IH} or V_{IL}.

[7] $\overline{RLRST}$, RCK, and $\overline{RCLR}$ = don't care.

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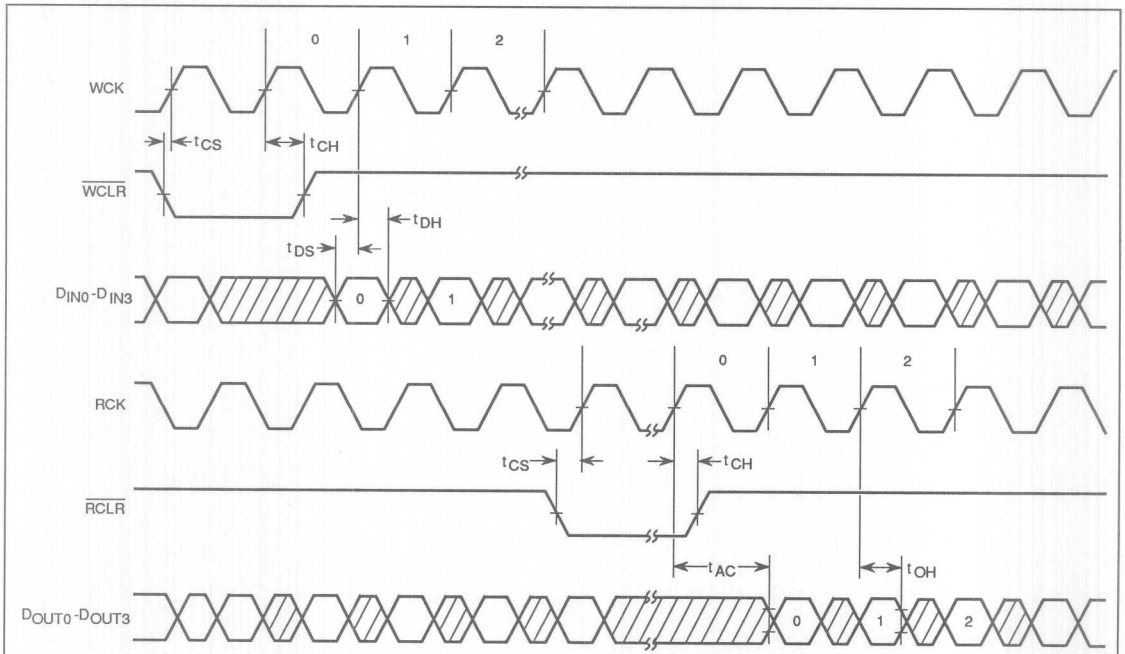
Figure 8. Example of Frame Synchronization/Time Base Correction



Notes:
(1) $\overline{W}$, $\overline{OE}$, WLJ, RLJ, WLH, and RLH = V_{IL}.
(2) LS_0 – LS_1, MODE, $\overline{WLRST}$, and $\overline{RLRST}$ = V_{IH}.

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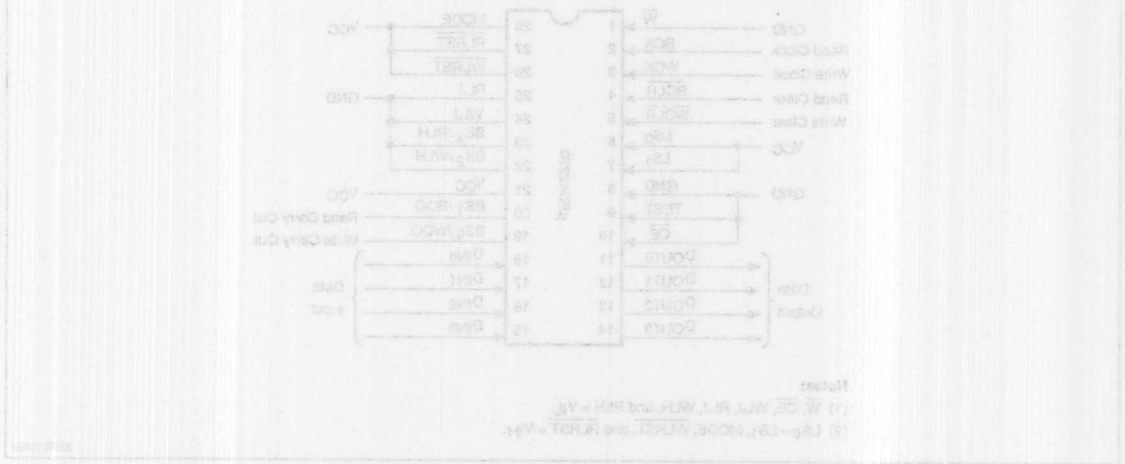
Figure 9. Asynchronous Read/Write Timing for Frame Synchronization or Time Base Correction

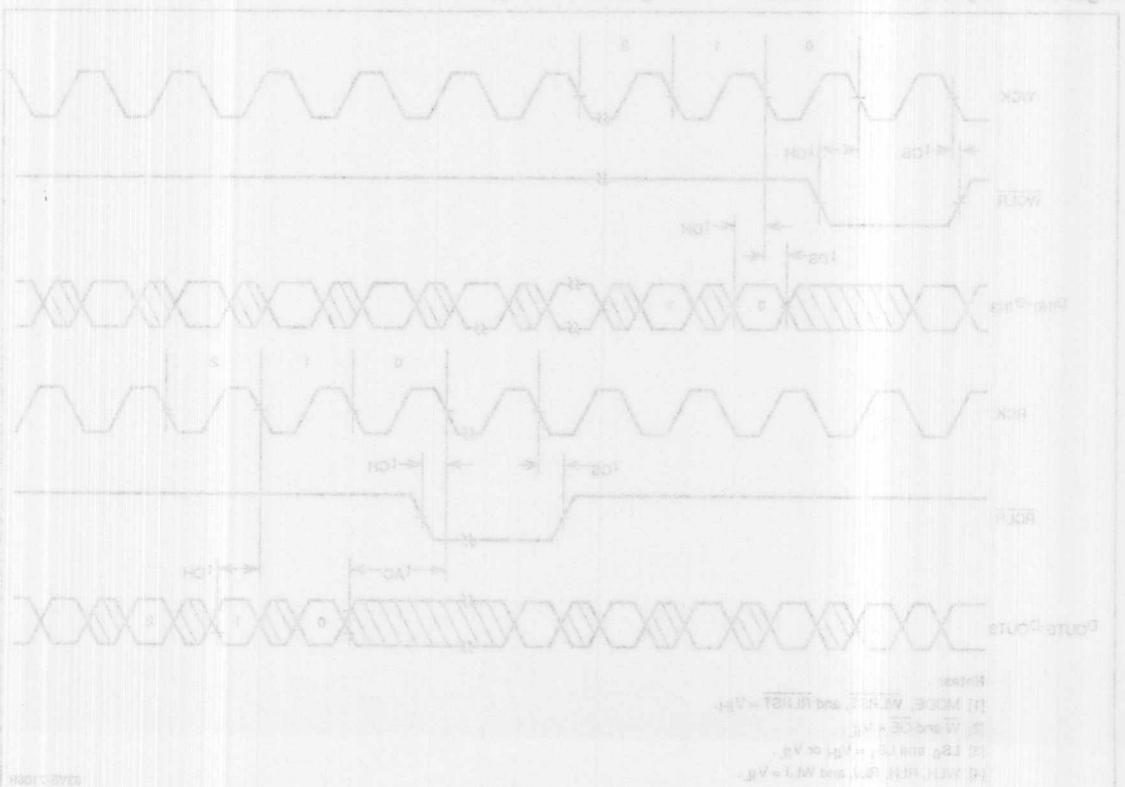


Notes:
[1] MODE, $\overline{WLRST}$, and $\overline{RLRST}$ = V_{IH}.
[2] $\overline{W}$ and $\overline{OE}$ = V_{IL}.
[3] LS_0 and LS_1 = V_{IH} or V_{IL}.
[4] WLH, RLH, RLJ, and WLJ = V_{IL}.

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Description

The μPD42272 is a picture-in-picture generator designed for use in NTSC and PAL broadcasting systems. Picture-in-picture describes the device's ability to combine multiple video signals into a single signal for display on a television monitor, for input to a VCR, or for use in any manner that a single video signal is used. The format may be selected so that one primary picture is displayed over the entire picture area. The other subpicture(s) can then be superimposed onto the primary one to allow multiple picture sources to be viewed simultaneously.

The μPD42272 has an onboard controller, field storage, buffer storage, two line buffers, and two oscillators. The controller sets the timing, performs vertical filtering, and stores and retrieves subpicture signal(s) for insertion into the primary picture signal. A line of the subpicture signal is placed in buffer storage before being written into field storage, which contains that portion of the signal to be displayed. The line buffers store a weighted average of three lines of the subpicture signal to provide vertical filtering, while the onboard oscillators facilitate interfacing to the μPD42272.

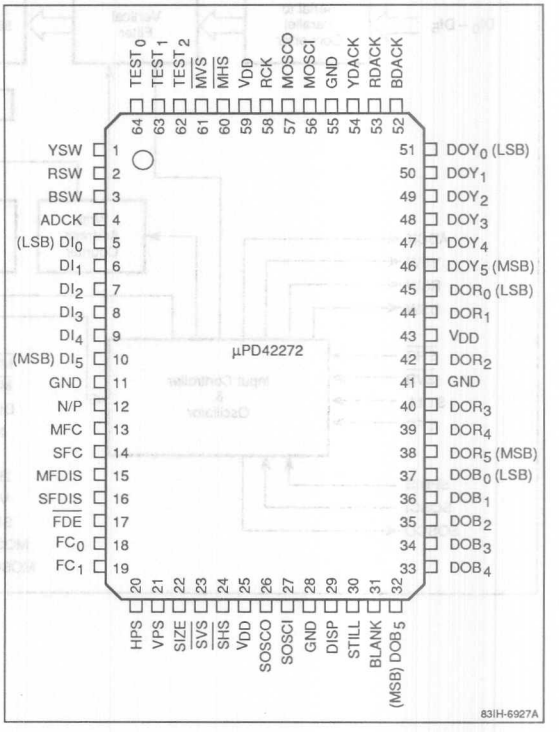
The level of integration provided by the μPD42272 means that picture-in-picture can be achieved more quickly and easily than with standard video buffers and control circuitry.

Features

- NTSC and PAL compatibility
- Built-in vertical filter
- Selectable subpicture display size
- 134,676-bit field buffer
- Two line buffers
- Built-in input and output oscillators
- Four selectable screen positions
- Four-color selection of subpicture frame border
- Selectable freeze-frame display
- Automatic self-refreshing
- 6-bit resolution of Y, R-Y and B-Y signals
- Low power consumption of 75 mA max
- CMOS silicon-gate fabrication process
- Three-state outputs
- Fully TTL-compatible inputs and outputs
- Single +5-volt power supply
- 64-pin quad flatpack (QFP) packaging

Pin Configuration

64-Pin Plastic QFP



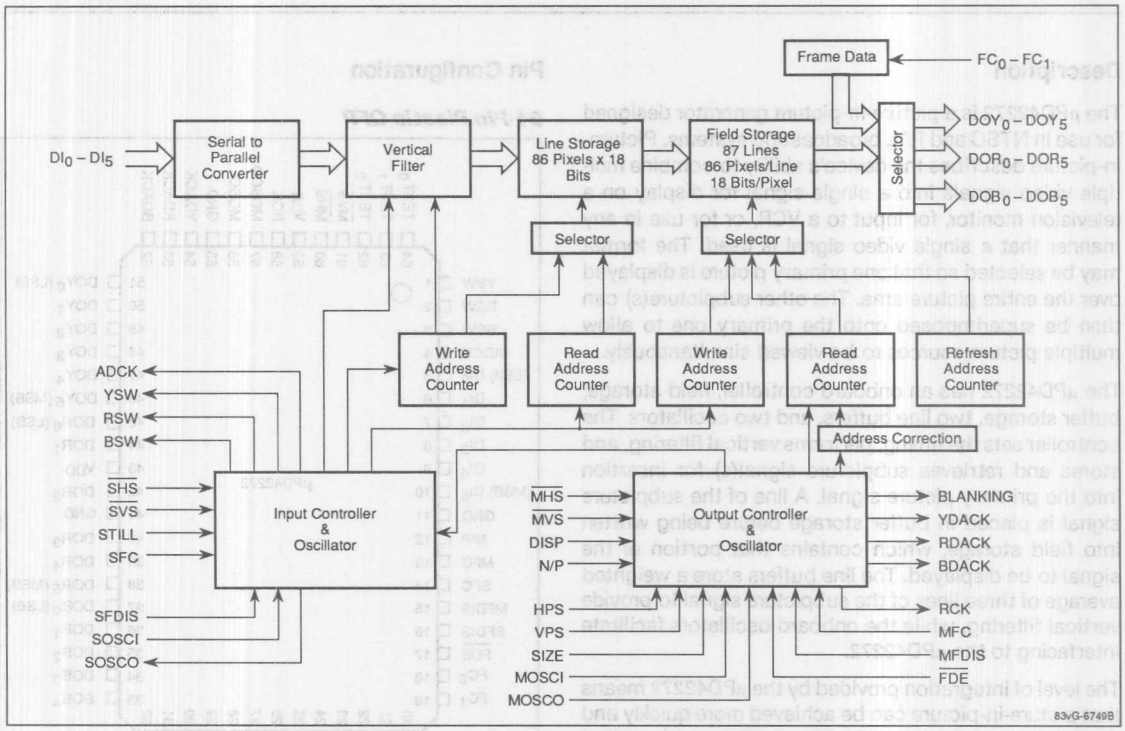
Ordering Information

Part Number	Package
μPD42272AGF-3BE	64-pin plastic quad flatpack

Contact your NEC sales representative for a copy of the complete data sheet.

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Block Diagram



Pin Identification

Symbol	Function
ADCK	Analog/digital clock output
BDACK	Digital/analog clock for B-Y component signal output
BLANK	Main picture blanking output
BSW	DI_0 - DI_5 output enable for B-Y component signals
DI_0 - DI_5	Multiplexed B-Y, R-Y, and Y data inputs
DISP	Subpicture on/off input
DOB_0 - DOB_5	B-Y data outputs
DOR_0 - DOY_5	R-Y data outputs
DOY_0 - DOY_5	Y data outputs
FC_0 and FC_1	Frame color selection input
$\overline{FDE}$	Field distinction data enable input
HPS	Horizontal position input
MFC	Main picture field correction input
MFDIS	Main picture field distinction input
$\overline{MHS}$	Main picture horizontal synchronous input
MOSCI	Main picture oscillator input
MOSCO	Main picture oscillator output
$\overline{MVS}$	Main picture vertical synchronous input
N/P	NTSC/PAL switching input
RCK	Read clock output
RDACK	Digital/analog clock for R-Y component signal output
RSW	DI_0 - DI_5 output enable for R-Y component signals
SFC	Subpicture field correction input
SFDIS	Subpicture field distinction input
$\overline{SHS}$	Subpicture horizontal synchronous input
SIZE	Size selection input
SOSCI	Subpicture oscillator clock input
SOSCO	Subpicture oscillator clock output
STILL	Freeze frame input
$\overline{SVS}$	Subpicture vertical synchronous input
$TEST_0$ - $TEST_2$	Test terminals
VPS	Vertical position input
YDACK	Digital/analog clock for Y component signal output
YSW	DI_0 - DI_5 output enable for Y component signals
V_{DD}	+5-volt power supply
GND	Ground

Pin Functions

ADCK. Y, R-Y and B-Y component signals selected with the analog switch are converted from analog to digital data in synchronization with this 6 MHz sampling clock. Digitized component signals are sequentially input to the DI_0 - DI_5 pins, also in synchronization with this clock.

BDACK. Digitized B-Y component signals are output from the DOB_0 - DOB_5 pins in synchronization with this 2.25 MHz sampling clock.

BLANK. When high, this output signal blanks the main picture, enabling the subpicture to be displayed.

BSW. A high logic level on BSW (while RSW and YSW are low) enables the DI_0 - DI_5 pins to be used for receiving 6-bit B-Y data from the A/D converter.

DI_0 through DI_5. These multiplexed pins are used for 6-bit digitized subvideo input, either B-Y, R-Y or Y, depending on the levels of BSW, RSW and YSW. DI_0 is the least significant bit and DI_5 is the most significant bit.

DISP. This pin controls the BLANK signal. A high logic level enables BLANK, while DISP low inhibits it. The level of DISP has no effect on the DOB_0 - DOB_5, DOR_0 - DOR_5, and DOY_0 - DOY_5 pins.

DOB_0 through DOB_5. These pins are used for 6-bit B-Y color difference output and depend on the status of BDACK. When no B-Y data is being output, the pins are in high impedance.

DOR_0 through DOR_5. These pins are used for 6-bit R-Y color difference output and depend on the status of RDACK. When no R-Y data is being output, the pins are in high impedance.

DOY_0 through DOY_5. These pins are used for 6-bit Y luminance output and depend on the status of YDACK. When no Y data is being output, the pins are in high impedance.

FC_0 and FC_1. The combination of signals from these pins is used to specify subvideo frame color, as shown below:

Pin	White	Light Blue	Yellow	Green
FC_0	high	low	high	low
FC_1	high	high	low	low

FDE. This pin is used to select external or internal field distinction. FDE high enables external field distinction, while FDE low inhibits the MFDIS and SFDIS pins and causes field distinction to be executed internally.

HPS and VPS. These horizontal and vertical input pins specify positioning of the subpicture. One of the four corners on the main picture can be selected by combining the input levels on HPS and VPS, as shown below.

Pin	Top Left	Bottom Left	Top Right	Bottom Right
HPS	high	high	low	low
VPS	high	low	high	low

MFC. Fields of the main picture are distinguished by the μPD42272 based on the phase relationship of the $\overline{MHS}$ and $\overline{MVS}$ signals. Field distinction may therefore be distorted if the signals are not in proper phase. In these cases, a high logic level on MFC can be used to reverse field distinction. MFC low has no effect on field distinction.

MFDIS. The even and odd fields of the main picture signal are distinguished based on the phase relationship of $\overline{MHS}$ and $\overline{MVS}$. MFDIS can be used to provide an external signal indicating either an odd (high) or even (low) field.

$\overline{MHS}$. This pin is used to input a horizontal synchronization signal for the main picture. The internal read clock oscillator is synchronized to the rising edge of $\overline{MHS}$ and increments the field buffer's read address counter, which is used to determine the horizontal display size and position of the sub picture.

MOSCI. This pin is used as an oscillator input for the main picture read clock. To use the internal oscillator, an external coil and capacitor must be installed. Alternatively, an 18 MHz external clock may be input to MOSCI.

MOSCO. This pin is used as an output for the feedback circuit of the main picture's internal oscillator.

$\overline{MVS}$. This pin is used to input a vertical synchronization signal for the main picture. The falling edge of $\overline{MVS}$ resets the field buffer's internal read address counter, which is used to determine the vertical display size and position of the sub picture.

N/P. A high logic level on this pin selects NTSC compatibility and a low selects PAL.

RCK. This pin is used as an output for the subpicture read clock, which is derived from MOSCI and MOSCO.

RDACK. Digital R-Y component signals are output from the DOR_0 - DOR_5 pins in synchronization with this 2.25 MHz sampling clock.

RSW. A high logic level on RSW (while BSW and YSW are low) enables the DI_0 - DI_5 pins to be used for receiving 6-bit R-Y data from the A/D converter.

SFC. The μPD42272 distinguishes subpicture fields based on the phase relationship of the $\overline{SHS}$ and $\overline{SVS}$ signals. Field distinction of the subpicture may therefore be distorted if the signals are not in phase. SFC high can be used to reverse field distinction. SFC low has no effect on field distinction.

SFDIS. The even and odd fields of the subpicture signal(s) are distinguished based on the phase relationship of the $\overline{SHS}$ and $\overline{SVS}$ signals. This pin can be used to provide an external signal indicating either an odd (high) or even (low) field.

$\overline{SHS}$. This pin is used to input the horizontal synchronization for the subpicture. The rising edge of this clock is used to synchronize the internal write clock oscillator which is then used to increment the write address counters for the line buffers and the field buffer.

SIZE. This input is used to specify size of the subpicture display area. SIZE high sets a full screen display and occupies 1/9 of the main picture. SIZE low displays 80% of the subpicture and occupies 1/12 of the main picture.

SOSCI. This pin is used as an oscillator input for the subpicture write clock. To use the internal oscillator, an external coil and capacitor must be installed. Alternatively, an 6 MHz external clock may be input to SOSCI.

SOSCO. This pin is used as an output for the feedback circuit of the subpicture's internal oscillator.

STILL. A high logic level selects a still picture, while STILL low selects a moving picture.

$\overline{SVS}$. This pin is used to input the vertical synchronization signal for the subpicture. The falling edge of this signal resets the internal write address counters for the line buffers and the field buffer.

$TEST_0$ - $TEST_2$. These are test pins and must be open.

YDACK. Digital Y component signals are output from the DOY_0 - DOY_5 pins in synchronization with this 9 MHz sampling clock.

YSW. A high logic level on YSW (while BSW and RSW are low) enables the DI_0 - DI_5 pins to be used for receiving 6-bit Y data from the A/D converter.

Application

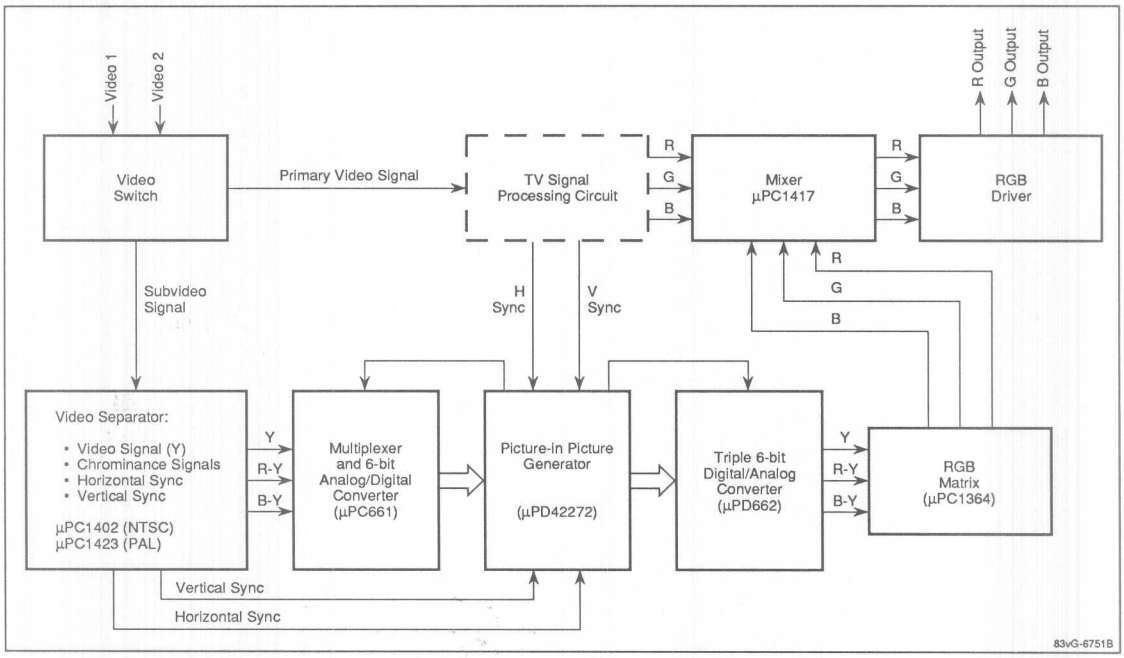
The following block diagram illustrates one application for the μPD42272 in an NTSC television system.

The video signals for the subpicture are separated into Y, B-Y, and R-Y component signals and horizontal and vertical synchronization signals by the μPC1402 decoder. The Y, B-Y, and R-Y component signals are input in parallel to the μPC661 A/D converter, after which they are switched to the sequence Y, R-Y, Y, -, Y, B-Y, Y, - using time-division multiplexing and converted to digital signals. In this instance, timing for the Y, R-Y, and B-Y conversion process is regulated by the μPD42272.

After the μPD42272 receives the 6-bit digital data output by the μPC661, it compresses the subpicture data and stores one field. The output signals are sent by the μPD42272 to the μPC662, which contains three D/A converters assigned respectively to the Y, R-Y, and B-Y signals. If the analog component signals output by the D/A converters are to be used by the TV, they then are converted to an RGB signal by the μPC1364 matrix circuit. If they are to be used by the VCR, they are combined with the main picture signal after being converted into composite signals in the encoder circuit.

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Application Example



NEC

NEC Electronics Inc.

μPD42532
32,768 x 8-BIT BIDIRECTIONAL DATA BUFFER

Description

The μPD42532 bidirectional data buffer features 32,768-word by 8-bit organization and CMOS dynamic circuitry that provides for high-speed, asynchronous, simultaneous write and read operation at a minimum cycle time of 100 ns. Two sets of write and read registers between the I/O pins and the storage cells enable all data to be parallel-transmitted as a single register group when the registers are either full or empty. The device's main application is data transmission between devices having different processing speeds, such as between a central processor and a disk.

Automatic refreshing by means of an internal capability is performed regularly for the μPD42532—without any influence on write and read operation. A built-in arbitration circuit performs each required read, write, or refresh operation sequentially (even if transparent refreshing overlaps with the transmission of data) to simplify the device's external timing requirements.

The μPD42532 operates from a single +5-volt power supply and is packaged in a 600-mil, 40-pin plastic DIP. Four FLAG pins, plus $\overline{\text{FULL}}$ and $\overline{\text{EMPTY}}$ pins, are provided to monitor the amount of data accumulated in storage.

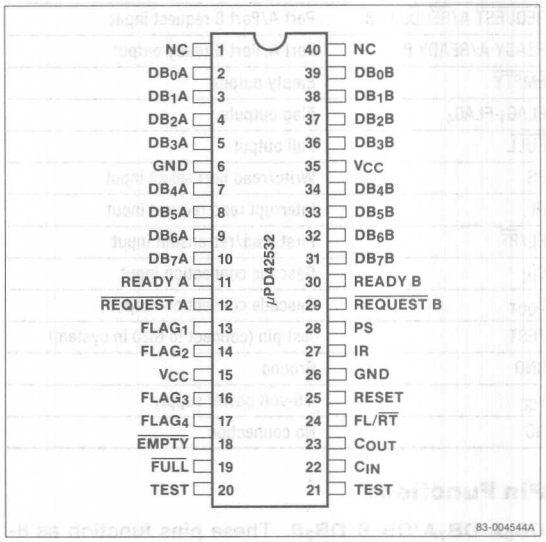
The μPD42532 is capable of bidirectional input/output by means of a port select function. Input and output pins are also supplied for cascade connection. Cascade connection allows any number of μPD42532s to be linked together so as to expand word width and length without limit.

Features

- ☐ 32,768-word by 8-bit organization
- ☐ CMOS technology
- ☐ Single +5-volt power supply
- ☐ Independent, asynchronous write/read operation
- ☐ Bidirectional transmission of input and output data (exchange of port functions)
- ☐ Automatic, regular refreshing
- ☐ Internal addressing
- ☐ Flag pin monitoring of accumulated data
- ☐ Unlimited expansion of word width and depth (cascade connection)
- ☐ Retransmit (re-read) function
- ☐ High-speed operation
  - — Access time: 50 ns maximum
  - — Cycle time: 100 ns minimum
- ☐ 600-mil, 40-pin plastic DIP packaging

Pin Configuration

40-Pin Plastic DIP



Ordering Information

Part Number	Access Time (max)	Cycle Time (min)	Package
μPD42532C-10	50 ns	100 ns	40-pin plastic DIP

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Pin Identification

Symbol	Function
DB_0A-DB_7A	Port A input/output data buses
DB_0B-DB_7B	Port B input/output data buses
RESET	Reset input
$\overline{\text{REQUEST}}$ A/$\overline{\text{REQUEST}}$ B	Port A/Port B request input
READY A/READY B	Port A/Port B ready output
$\overline{\text{EMPTY}}$	Empty output
$FLAG_1$-$FLAG_4$	Flag outputs
$\overline{\text{FULL}}$	Full output
PS	Write/read port select input
IR	Interrupt read request input
FL/$\overline{\text{RT}}$	First load/retransmit input
C_{IN}	Cascade connection input
C_{OUT}	Cascade connection output
TEST	Test pin (connect to GND in system)
GND	Ground
V_{CC}	+5-volt power supply
NC	No connection

Pin Functions

DB_0A-DB_7A/DB_0B-DB_7B. These pins function as 8-bit data buses for write input or read output depending on the status of the PS pin. The output drivers are three-state outputs.

RESET. This pin initializes the internal counters and pointers.

$\overline{\text{REQUEST}}$ A/$\overline{\text{REQUEST}}$ B. Depending on the status of PS, one pin corresponds to the read port and the other to the write port. To initiate a write or read cycle, the signal goes low for the respective port (if READY A or READY B is low, the corresponding $\overline{\text{REQUEST}}$ input is ignored internally). These pins can be connected to the WR and RD pins of a CPU.

READY A/READY B. Depending on the status of PS, one pin corresponds to the read port and the other to the write port. When a write or read cycle is possible, the READY signal is high for the respective port. These pins can be connected to the READY pins of a CPU or DMA controller.

$\overline{\text{EMPTY}}$. The signal from this pin is low whenever the amount of data accumulated is exactly 0 bytes, and high in all other cases.

$FLAG_1$-$FLAG_4$. These pins reflect the amount of data accumulated in the storage array. By combining the output signals, it is possible to monitor (in 2K byte steps) data quantities of up to 32K bytes.

$\overline{\text{FULL}}$. The signal from this pin is low when the storage cells are full of accumulated data, and high in all other cases.

PS. This pin is used to specify the direction of data transfer. When PS is high, Port A serves as the write port and Port B as the read port. When PS is low, the functions of the two ports are reversed.

IR. If the data accumulated in storage is less than 64 bytes (i.e., one register's capacity), the READY signal for the read port goes low to inhibit reading. However, forcing IR high makes it possible to read all stored data.

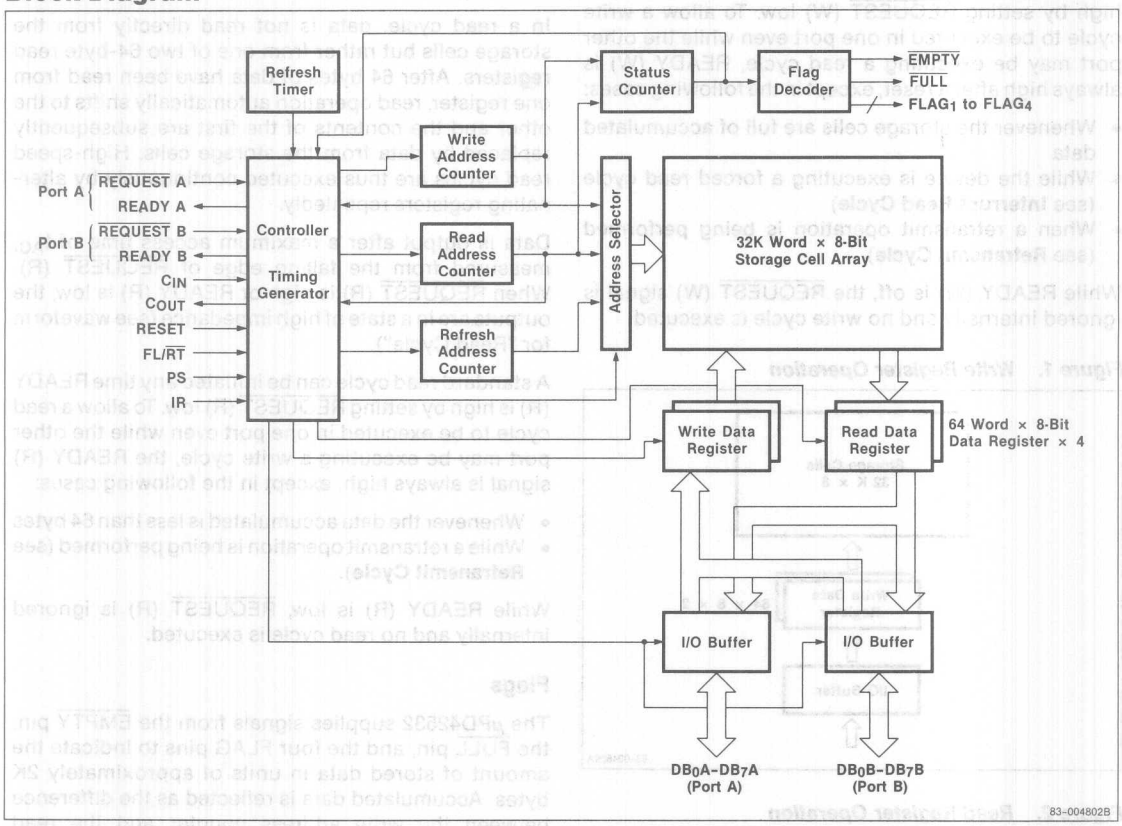
Read cycles are normally executed so as to maintain the stored data volume at levels above 2K bytes. If the data volume drops below 2K bytes for devices with process code K, all remaining data must be read using the interrupt read option.

FL/$\overline{\text{RT}}$. This pin designates the lead device when multiple devices are cascade connected. It is high only for that device and low for all others. If the device is not cascaded, a low FL/$\overline{\text{RT}}$ controls the retransmit (re-read) function; other than during retransmission, FL/$\overline{\text{RT}}$ must be high.

C_{IN}. This pin is used to expand word depth and is connected to the C_{OUT} pin of the device preceding it in cascade connections. If word depth is not expanded, C_{IN} is connected to C_{OUT} of the same device.

C_{OUT}. This pin is used to expand word depth and is connected to the C_{IN} pin of the device following it in cascade connections. If word depth is not expanded, C_{OUT} is connected to C_{IN} of the same device.

Block Diagram



Operation

Reset Cycle

After power is applied to the μPD42532, it is necessary to clear the internal counters and initialize the write and read address pointers by executing a reset cycle. A reset cycle can be executed at any time by setting the RESET pin to a high logic level. However, once this cycle is initiated, RESET, $\overline{\text{REQUEST}}$, and FL/$\overline{\text{RT}}$ must be kept high for a minimum time of t_{SW} before the RESET signal goes low again (see waveform for "Reset Cycle"). The RESET, $\overline{\text{REQUEST}}$, and FL/$\overline{\text{RT}}$ signals are all high at the start of a reset, except in cascade connections, in which case a high FL/$\overline{\text{RT}}$ is required only in the first stage.

After a reset, the READY signal for the write port, READY (W), is driven high to prepare for a write cycle. Subsequently, the $\overline{\text{REQUEST}}$ signal for the write port, $\overline{\text{REQUEST}}$ (W), can be set low to commence writing.

A standard read cycle can be executed once data written to one of the 64-byte registers has filled that register and been transferred to the storage cells. The READY signal for the read port, READY (R), goes high to prepare for the cycle. Subsequently, the $\overline{\text{REQUEST}}$ signal for the read port, $\overline{\text{REQUEST}}$ (R), can be set low to commence reading.

Write Cycle

In a write cycle, data is written to one of two 64-byte write registers before being transferred to the storage cells. Whenever 64 bytes have been written into one register, write operation automatically shifts to the other and the contents of the first are transferred to storage. High-speed write cycles are thus executed continuously by alternating registers repeatedly. Write data must satisfy the requirements for setup and hold times as measured against the rising edge of $\overline{\text{REQUEST}}$ (W) [see waveform for "Write Cycle"].

A write cycle can be initiated any time READY (W) is high by setting $\overline{\text{REQUEST}}$ (W) low. To allow a write cycle to be executed in one port even while the other port may be executing a read cycle, READY (W) is always high after a reset, except in the following cases:

- Whenever the storage cells are full of accumulated data
- While the device is executing a forced read cycle (see **Interrupt Read Cycle**)
- When a retransmit operation is being performed (see **Retransmit Cycle**)

While READY (W) is off, the $\overline{\text{REQUEST}}$ (W) signal is ignored internally and no write cycle is executed.

Figure 1. Write Register Operation

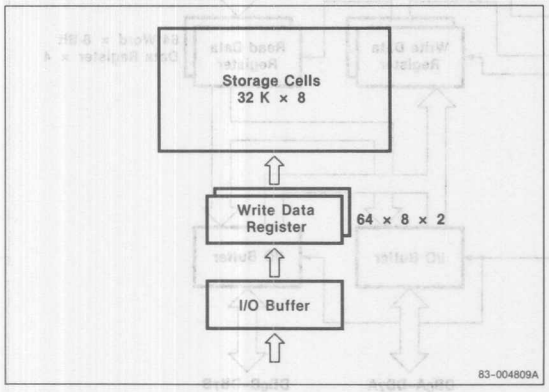
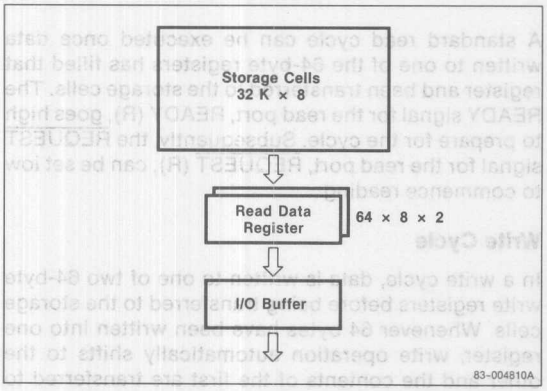


Figure 2. Read Register Operation



Read Cycle

In a read cycle, data is not read directly from the storage cells but rather from one of two 64-byte read registers. After 64 bytes of data have been read from one register, read operation automatically shifts to the other and the contents of the first are subsequently replaced by data from the storage cells. High-speed read cycles are thus executed continuously by alternating registers repeatedly.

Data is output after a maximum access time of t_{AC}, measured from the falling edge of $\overline{\text{REQUEST}}$ (R). When $\overline{\text{REQUEST}}$ (R) is high or READY (R) is low, the outputs are in a state of high impedance (see waveform for "Read Cycle").

A standard read cycle can be initiated any time READY (R) is high by setting $\overline{\text{REQUEST}}$ (R) low. To allow a read cycle to be executed in one port even while the other port may be executing a write cycle, the READY (R) signal is always high, except in the following cases:

- Whenever the data accumulated is less than 64 bytes
- While a retransmit operation is being performed (see **Retransmit Cycle**).

While READY (R) is low, $\overline{\text{REQUEST}}$ (R) is ignored internally and no read cycle is executed.

Flags

The μPD42532 supplies signals from the $\overline{\text{EMPTY}}$ pin, the $\overline{\text{FULL}}$ pin, and the four FLAG pins to indicate the amount of stored data in units of approximately 2K bytes. Accumulated data is reflected as the difference between the write address counter and the read address counter. Thus, if a total of 16K bytes have been read while 32K bytes have been written since the most recent reset, the amount of data in storage is 16K bytes.

The $\overline{\text{FULL}}$ and $\overline{\text{EMPTY}}$ pins are used to prevent overwriting and overreading. To control write operation on data units of register length (64 bytes), the $\overline{\text{FULL}}$ pin outputs a low signal when stored data reaches the 32,705- to 32,768-byte range. Whenever write cycles are executed continuously and the storage cells become full, $\overline{\text{REQUEST}}$ (W) is ignored and the signals of $\overline{\text{FULL}}$ and READY (W) are driven low to inhibit writing. Meanwhile if read cycles are executed and the data decreases to 32,704 bytes or less, READY (W) goes high again to enable write operation.

The $\overline{\text{EMPTY}}$ pin goes low whenever stored data is exactly 0 bytes. Since standard read cycles cannot be executed if the quantity of data drops below 64 bytes, READY (R) goes low to inhibit read operation. Whenever write cycles are executed and stored data increases to 64 bytes or more, READY (R) goes high again to enable read operation.

The status of the FLAG pins depends on the internal status of the write and read address counters. These counters are incremented as data is transferred to or from the storage array. Since the logic levels of the FLAG pins reflect movement of blocks of data on a 64-byte-register basis rather than on a single-byte basis, the status indicated by these pins can be in error by a maximum of 255 bytes with respect to the actual amount of data accumulated [i.e., the sum of the write register (63 bytes), the read registers (128 bytes), and the 64 bytes currently being transferred]. This discrepancy means that two adjacent ranges of stored data, as indicated by the FLAGs, can overlap by up to 191 bytes.

The following table shows the combination of signals output from these pins.

Table 1. Stored Data as Indicated by Flag Pins

Amount of Stored Data (bytes)	$\overline{\text{FULL}}$	$\overline{\text{EMPTY}}$	FLAG 1	FLAG 2	FLAG 3	FLAG 4
32705 to 32768	0	1	1	1	1	1
30721 to 32767	1	1	1	1	1	1
28673 to 30911	1	1	0	1	1	1
26625 to 28863	1	1	1	0	1	1
24577 to 26815	1	1	0	0	1	1
22529 to 24767	1	1	1	1	0	1
20481 to 22719	1	1	0	1	0	1
18433 to 20671	1	1	1	0	0	1
16385 to 18623	1	1	0	0	0	1
14337 to 16575	1	1	1	1	1	0
12289 to 14527	1	1	0	1	1	0
10241 to 12479	1	1	1	0	1	0
8193 to 10431	1	1	0	0	1	0
6145 to 8383	1	1	1	1	0	0
4097 to 6335	1	1	0	1	0	0
2049 to 4287	1	1	1	0	0	0
1 to 2239	1	1	0	0	0	0
0	1	0	0	0	0	0

Notes:

(1) 1 = high level

(2) 0 = low level

Interrupt Read Cycle

Whenever the amount of stored data drops below 64 bytes (i.e., one register's capacity), or 2K bytes for devices with process code K, READY (R) is driven low to inhibit reading. Any data remaining in a write register can only be read by means of an interrupt (or forced) read cycle.

An interrupt read cycle can be executed by forcing the IR pin high. At this point, data is transferred from the write register to one of the read registers via the storage array, and write operation is disabled until all stored data has been read. If this cycle is initiated after READY (R) goes low, read operation will be delayed until all data has been transferred to one of the read registers.

Once the device completes reading of its last address, the $\overline{\text{EMPTY}}$ and READY (R) signals are driven low and READY (W) goes high to enable write operation again (unless a retransmit cycle has been requested). Read cycles will be executed only after 64 bytes or more have been written and transferred to storage.

Retransmit Cycle

The μPD42532 will execute a retransmit cycle whenever a low-level pulse is applied to $\overline{\text{RT}}$. A retransmit cycle initializes the read address counter to starting address 0. Although retransmission can be executed at any time, $\overline{\text{REQUEST}}$ (W) and $\overline{\text{REQUEST}}$ (R) must be high before and after the low $\overline{\text{RT}}$ signal is applied.

During this cycle, the READY signals are pulsed low to temporarily inhibit writing and reading, and the FLAG and $\overline{\text{EMPTY}}$ signals vary in accordance with the amount of data in storage. After READY (W) goes high again, the retransmit preparation cycle is complete. Write operation can resume after an extra delay to ensure stability of the FLAG and $\overline{\text{EMPTY}}$ pins. If an interrupt read signal is applied during retransmission, the interrupt read cycle is executed after termination of the retransmit cycle.

The retransmit function is only useful in systems where less than 32K bytes of data are written between resets. If a retransmit cycle is executed after more than 32K bytes are written, old data cannot be retransmitted.

Since the $\overline{\text{RT}}$ pin is multiplexed as the first load (FL) pin in cascade connections, cascaded devices cannot be used for retransmission. In single-device configuration, this pin is always high except during a retransmit cycle.

Port Select Function

The μPD42532 is able to change the direction of data transfer according to the logical level of the signal applied to the PS pin. When a high-level input is applied to PS, Port A becomes the write port and Port B the read port. When PS is low, the functions of the two ports are reversed. While port functions are being assigned, the $\overline{\text{REQUEST}}$ signals must be kept high.

Since register and storage cell data are preserved during port selection, data written to a particular port can also be read from that same port.

Cascade Connection

The μPD42532 can be used in a single-device, 32K by 8-bit configuration or it can be cascade connected by means of the C_{IN} and C_{OUT} pins to allow unlimited expansion of word width and length.

Single-Device Configuration. When using the μPD42532 as a single 32K by 8-bit data buffer, connect C_{OUT} to C_{IN} and set the FL pin to a high logic level (see figure 3).

Expanded Word Width. When using multiple devices to expand word width, connect RESET, $\overline{\text{REQUEST}}$, PS, and IR to the corresponding pins of each μPD42532 in parallel and apply common control signals. Each C_{OUT} pin should be connected to its own C_{IN} pin (as in the single-device configuration) and a high-level input applied to each FL. The flag pins of a single μPD42532 can be used to represent the entire system (see figure 4).

Expanded Word Length. When using multiple devices to expand word length, set a high-level input to FL of the lead μPD42532 and a low-level input to FL of all the others. Each C_{OUT} pin should be connected to C_{IN} of the device following it; C_{OUT} on the last device should be connected to C_{IN} of the lead device. Connect RESET, $\overline{\text{REQUEST}}$, PS, and IR to the corresponding pins of each μPD42532 in parallel and apply common control signals.

The $\overline{\text{EMPTY}}$, $\overline{\text{FULL}}$, and READY pins of each device, respectively, can be ORed together by external logic. 'OR' outputs are composite $\overline{\text{EMPTY}}$, $\overline{\text{FULL}}$, and READY signals for all data buffers (see figure 5).

Operation. To enable operation of μPD42532s in cascade connection, set the RESET signal(s) high to clear the internal counters and initialize the write and read address pointers. When the reset is complete, start writing to the lead device. While data is being written to the first, all other devices output low READY signals and ignore the $\overline{\text{REQUEST}}$ signals. When write operation in the first μPD42532 (n) reaches the last address, its C_{OUT} pin outputs a high-level signal and forces C_{IN} of the next device high. Write operation shifts to the next device in succession (n + 1). The READY (W) signal of the first device (n) is driven low, and the READY (W) signal of the succeeding device (n + 1) goes high.

If only write cycles are being executed, each data buffer outputs a low $\overline{\text{FULL}}$ signal as writing is completed for that device. At the point where the last device finishes writing to its last address, all μPD42532s output low-level $\overline{\text{FULL}}$ and READY (W) signals. The ORed composite of these signals should be used to inhibit write operation.

If write and read cycles are being executed simultaneously, and the storage cells in the lead device are not full of accumulated data when the last device completes writing to its last address, write operation shifts to the lead μPD42532 again. Writing continues in this manner until every data buffer is full.

Read cycles also begin with the lead device (n) and shift to the next (n + 1) once the last address has been read. When all devices have been completely emptied of data, the ORed composite of the $\overline{\text{EMPTY}}$ signals is low. If the expanded word length configuration has less than 64 bytes of data in a write register, $\overline{\text{EMPTY}}$ will not be at a low level; READY (R) will be low to indicate that standard read operation may not proceed. Forced read or dummy write cycles will be required to continue reading any accumulated data of less than 64 bytes.

Figure 3. Single-Device Configuration Block Diagram

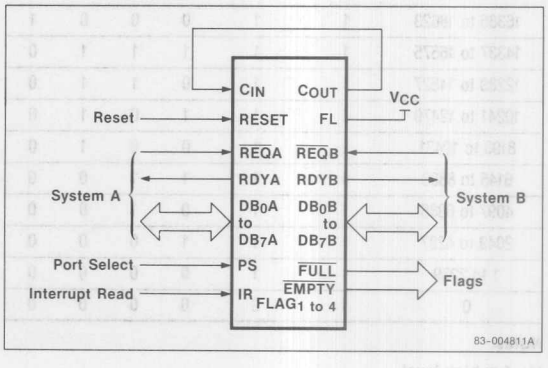


Figure 4. Expanded Word Width Block Diagram

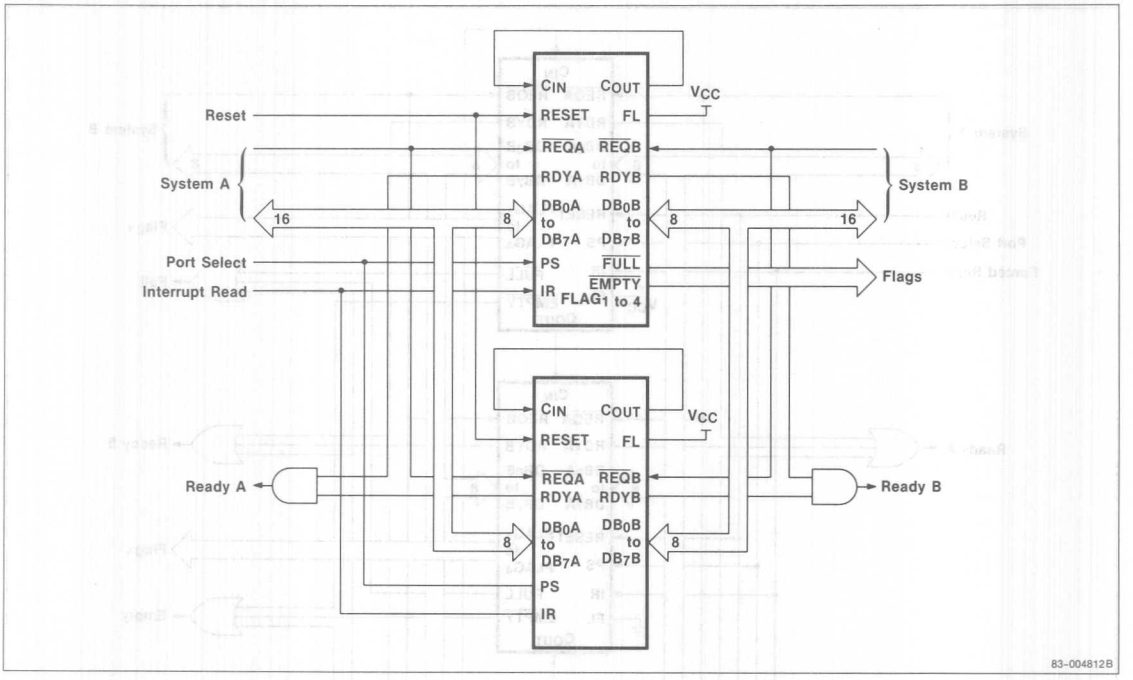
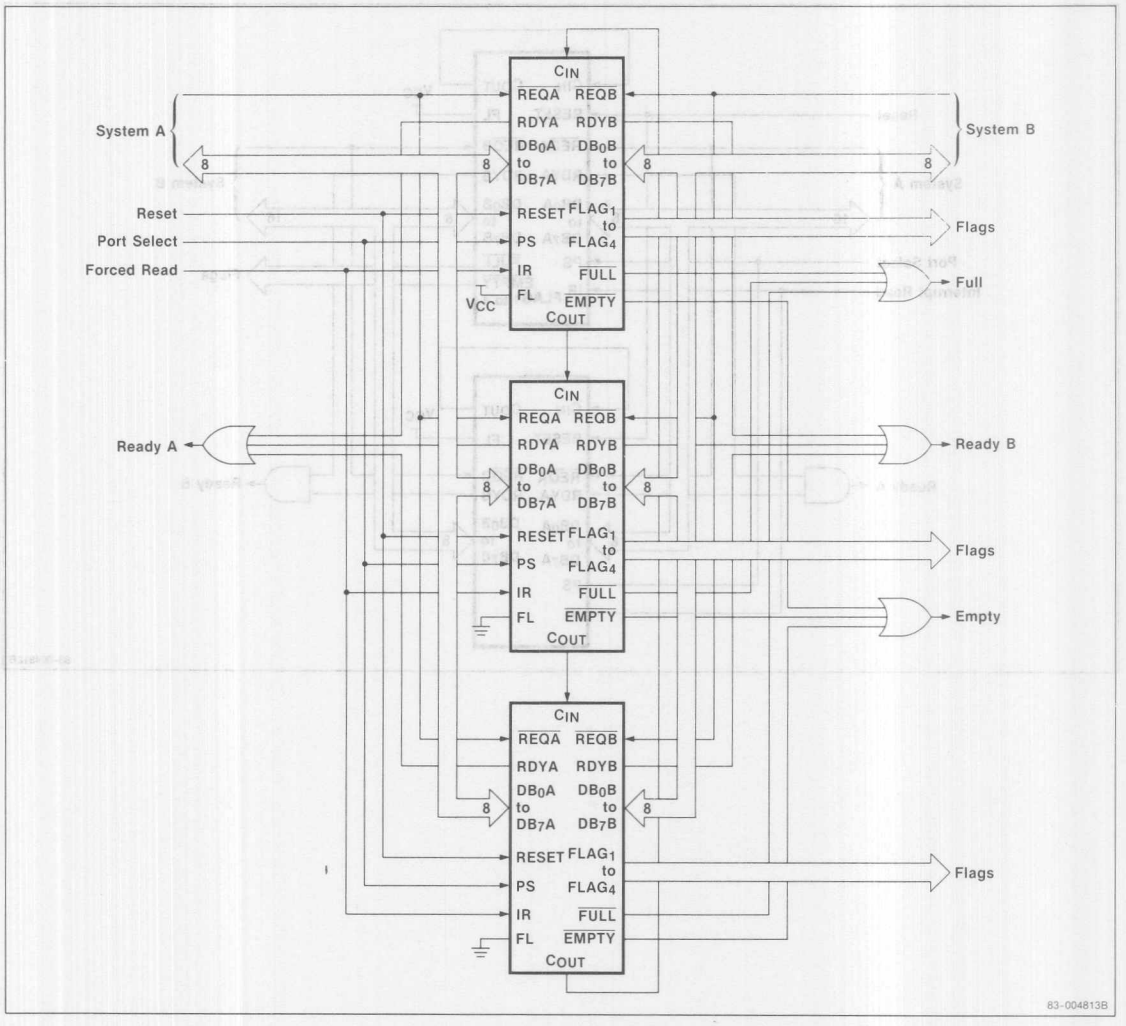


Figure 5. Expanded Word Length Block Diagram



Absolute Maximum Ratings

Terminal voltage, V_T	−1.5 to +7.0 V
Operating temperature, T_{OPR}	0 to +70°C
Storage temperature, T_{STG}	−55 to +125°C
Output current, I_O	50 mA
Power supply voltage, V_{CC}	−1.5 to +7.0 V

Comment: Exposure to Absolute Maximum Ratings for extended periods may affect device reliability; exceeding the ratings could cause permanent damage. The device should be operated within the limits specified under DC and AC Characteristics.

Recommended DC Operating Conditions

$T_A = 0$ to +70°C; $V_{CC} = +5.0$ V ±10%

Parameter	Symbol	Min	Typ	Max	Unit
Input voltage, high	V_{IH}	2.4		V_{CC}	V
Input voltage, low	V_{IL}	−1.0		0.8	V

DC Characteristics

$T_A = 0$ to +70°C; $V_{CC} = +5.0$ V ±10%

		Limits				
Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions
Standby supply current	I_{CC1}			20	mA	$\overline{\text{REQUEST}}$ A, B = V_{IH}
Write/read cycle supply current	I_{CC2}			80	mA	$t_{WC} = 100$ ns; $t_{RC} = 100$ ns
Write cycle supply current	I_{CC3}			60	mA	$t_{WC} = 100$ ns; $\overline{\text{REQUEST}}$ (R) = V_{IH}
Read cycle supply current	I_{CC4}			60	mA	$t_{RC} = 100$ ns; $\overline{\text{REQUEST}}$ (W) = V_{IH}
Input leakage current	I_I	−10		10	μA	$V_I = 0$ to V_{CC}; other inputs = 0 V
Output leakage current	I_O	−10		10	μA	$V_O = 0$ to V_{CC}; output disabled
Output voltage, high	V_{OH}	2.4			V	$I_{OH} = -1$ mA
Output voltage, low	V_{OL}			0.4	V	$I_{OL} = 4$ mA

Capacitance

$T_A = 0$ to +70°C; $V_{CC} = +5.0$ V ±10%

		Limits				
Parameter	Symbol	Min	Typ	Max	Unit	Pins Under Test
Input capacitance	C_I			10	pF	$\overline{\text{REQUEST}}$, RESET, PS, C_{IN}, IR, FL/$\overline{\text{RT}}$
Output capacitance	C_O			10	pF	READY, $FLAG_1$-$FLAG_4$, C_{OUT}, $\overline{\text{FULL}}$, $\overline{\text{EMPTY}}$
Input/output capacitance	$C_{I/O}$			10	pF	DB_0-DB_7

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AC Characteristics

T_A = 0 to +70°C; V_{CC} = +5.0 V ±10%

Parameter	Symbol	Limits Min	Limits Max	Unit	Test Conditions
Read cycle time	t_{RC}	100		ns	
$\overline{\text{REQUEST}}$ (R) pulse width	t_{RQW}	50	10000	ns	(Note 5)
$\overline{\text{REQUEST}}$ (R) precharge time	t_{RQP}	30		ns	
$\overline{\text{REQUEST}}$ (R) low hold time after READY (R) high	t_{RQN}	50	10000	ns	(Note 6)
READY (R) low output time	t_{RRF}		30	ns	(Note 14)
Access time	t_{AC}		50	ns	
Access time after READY (R) high	t_{ACR}		50	ns	
Output data hold time	t_{OH}	10		ns	
Output data off time	t_{OFF}		40	ns	
Low-impedance output delay	t_{LZ}	5		ns	
Low-impedance output delay after READY (R) high	t_{LZR}	0		ns	
READY (R) low time when empty	t_{SRR}		$4800 + 64\ t_{WC}$	ns	(Note 8)
READY (R) low time when almost empty	t_{EMR}	0	$4800 + 63\ t_{WC}$	ns	(Note 8)
Write cycle time	t_{WC}	100		ns	
$\overline{\text{REQUEST}}$ (W) pulse width	t_{WQW}	50	10000	ns	(Note 5)
$\overline{\text{REQUEST}}$ (W) precharge time	t_{WQP}	30		ns	
$\overline{\text{REQUEST}}$ (W) low hold time after READY (W) high	t_{WQN}	50	10000	ns	(Note 6)
READY (W) low output time	t_{WRF}		30	ns	
Write data setup time	t_{DW}	30		ns	
Write data hold time	t_{DH}	10		ns	
$\overline{\text{REQUEST}}$ high setup time	t_{QRP}	$t_T + 30$		ns	(Note 6)
READY (W) low time when full	t_{FLW}	0	$3200 + 64\ t_{RC}$	ns	
$FLAG_1$-$FLAG_4$ output times	t_{FLO}		4800	ns	
$\overline{\text{EMPTY}}$ and $\overline{\text{FULL}}$ output valid times	t_{EFO}		40	ns	
$\overline{\text{EMPTY}}$ and $\overline{\text{FULL}}$ output hold times	t_{EFH}	0		ns	
$\overline{\text{FULL}}$ output off time	t_{FOF}		3200	ns	(Note 9)
C_{OUT} output off time when read request is executed	t_{COR}		40	ns	
C_{OUT} output on time when write request is executed	t_{COW}		40	ns	
C_{IN} setup time for $\overline{\text{REQUEST}}$ (R)	t_{CIR}	10		ns	
C_{IN} setup time for $\overline{\text{REQUEST}}$ (W)	t_{CIW}	10		ns	
Reset pulse width	t_{SW}	100		ns	
READY, $\overline{\text{FULL}}$, and $\overline{\text{EMPTY}}$ output times after reset	t_{SWR}		80	ns	
$FLAG_1$-$FLAG_4$ output times after reset	t_{SSF}		100	ns	
$\overline{\text{REQUEST}}$ precharge hold time after reset	t_{SWQ}	30		ns	
$\overline{\text{RT}}$ disable hold time after reset	t_{SRT}	800		ns	

AC Characteristics (cont)

Parameter	Symbol	Limits Min	Limits Max	Unit	Test Conditions
C_{OUT} output low time after reset	t_{SWC}		100	ns	
READY (R) on time after interrupt read is executed	t_{FRR}	0	6400	ns	(Note 7)
READY (W) off time after interrupt read is executed	t_{FWR}		50	ns	(Note 7)
READY (W) on time after interrupt read	t_{IRW}		100	ns	(Note 11)
$\overline{\text{REQUEST}}$ (W) hold time after IR input	t_{FQA}	60		ns	(Note 13)
$\overline{\text{REQUEST}}$ (W) setup time before IR input	t_{FQB}	60		ns	
IR pulse width	t_{FW}	50	2000	ns	(Notes 4, 12, 13)
$\overline{\text{REQUEST}}$ hold time after PS input	t_{PAQ}	100		ns	
$\overline{\text{REQUEST}}$ setup time before PS input	t_{PBQ}	100		ns	
READY output time after port selection	t_{PSR}		50	ns	
$\overline{\text{RT}}$ pulse width	t_{RTW}	50	2000	ns	(Note 4)
$\overline{\text{REQUEST}}$ setup time before $\overline{\text{RT}}$ input	t_{BRT}	60		ns	(Note 10)
$\overline{\text{REQUEST}}$ hold time after $\overline{\text{RT}}$ input	t_{RTQ}	60		ns	
READY (R) on time after retransmit is executed	t_{RTR}		6400	ns	(Note 7)
READY (W) on time after retransmit is executed	t_{WRT}		4800	ns	(Note 7)
READY off time after retransmit is executed	t_{RRT}		50	ns	
$\overline{\text{EMPTY}}$ and $\overline{\text{FULL}}$ output hold times after retransmit is executed	t_{FSRT}	0		ns	
$\overline{\text{EMPTY}}$ reset time after retransmit is executed	t_{RTE}		3200	ns	
$FLAG_1$-$FLAG_4$ output valid times after retransmit is executed	t_{RTF}		8000	ns	
Input transition time	t_T	5	50	ns	

Notes:

(1) All voltages are referenced to GND.

(2) All ac measurements assume input pulse rise and fall times of 5 ns.

(3) The input voltage reference levels for timing ratings are V_{IH} (min) and V_{IL} (max). Transition time t_T is defined between V_{IH} and V_{IL}.

(4) IR and $\overline{\text{RT}}$ inputs cannot be applied simultaneously. A timing delay of at least 100 ns is required. See figures 6 and 7 for acceptable input methods.

(5) The maximum pulse width of 10,000 ns applies only when the READY signal is on.

(6) $\overline{\text{REQUEST}}$ cannot be raised to a high level during the t_{QRP} + t_{RQN} (or t_{WQN}) interval.

(7) If an $\overline{\text{RT}}$ (IR) pulse is applied during IR ($\overline{\text{RT}}$) operation, the $\overline{\text{RT}}$ (IR) operation is delayed until IR ($\overline{\text{RT}}$) operation is released.

(8) "Empty" is defined as the state where the amount of stored data is zero, and "almost empty" is defined as the state where the amount of data is 1 to 63 bytes.

(9) t_{FOF} is defined from the rising edge of the $\overline{\text{REQUEST}}$ (R) signal when the amount of stored data reaches the prescribed value (that is, the value at which the FULL signal changes from a low level to a high level as defined in Table 1).

(10) t_{BRT} = 4800 ns minimum for the devices with process code K.

Figure 6. Input Timing for IR and $\overline{\text{RT}}$: Method 1

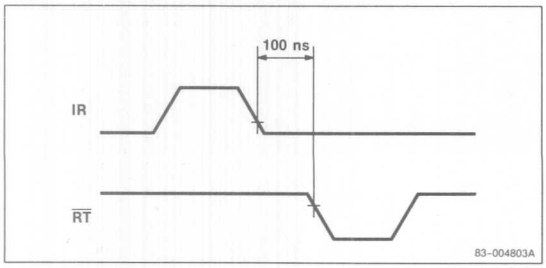
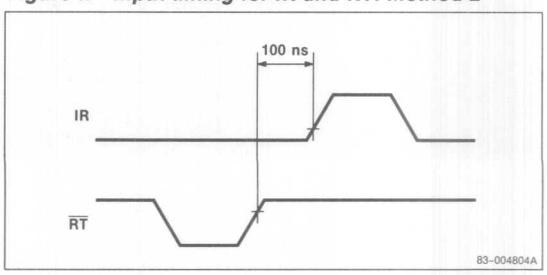


Figure 7. Input timing for IR and $\overline{\text{RT}}$: Method 2



AC Characteristics (cont)

Notes [cont]:

(11) After all data has been read in an IR cycle for devices with process code K, always input a $\overline{\text{RESET}}$ signal to initialize the internal circuitry before proceeding to the next operation. See figure 8.

(12) The IR signal is invalid whenever the $\overline{\text{EMPTY}}$ signal is low on devices with process code K.

(13) If an IR input signal is applied in a cascade connection for devices with process code K, the $\overline{\text{REQUEST}}$ (W) signal must stay at a high level until all data has been read.

(14) Read cycles are normally executed so as to maintain the stored data volume at levels above 2K bytes. If the data volume drops below 2K bytes for devices with process code K, read all of the remaining data using the interrupt read option.

Figure 8. Reset Pulse After IR Operation

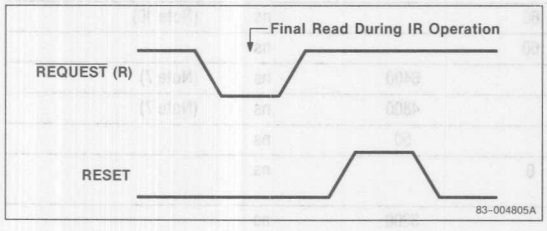


Figure 9. Input Timing

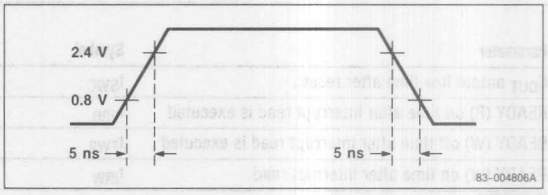


Figure 10. Output Timing

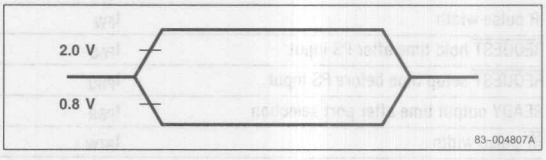
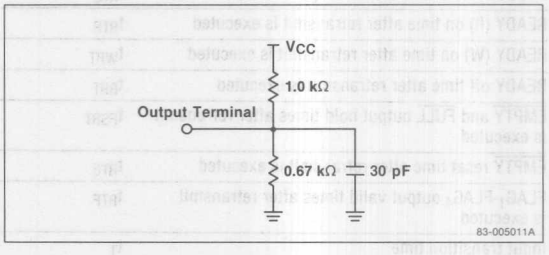
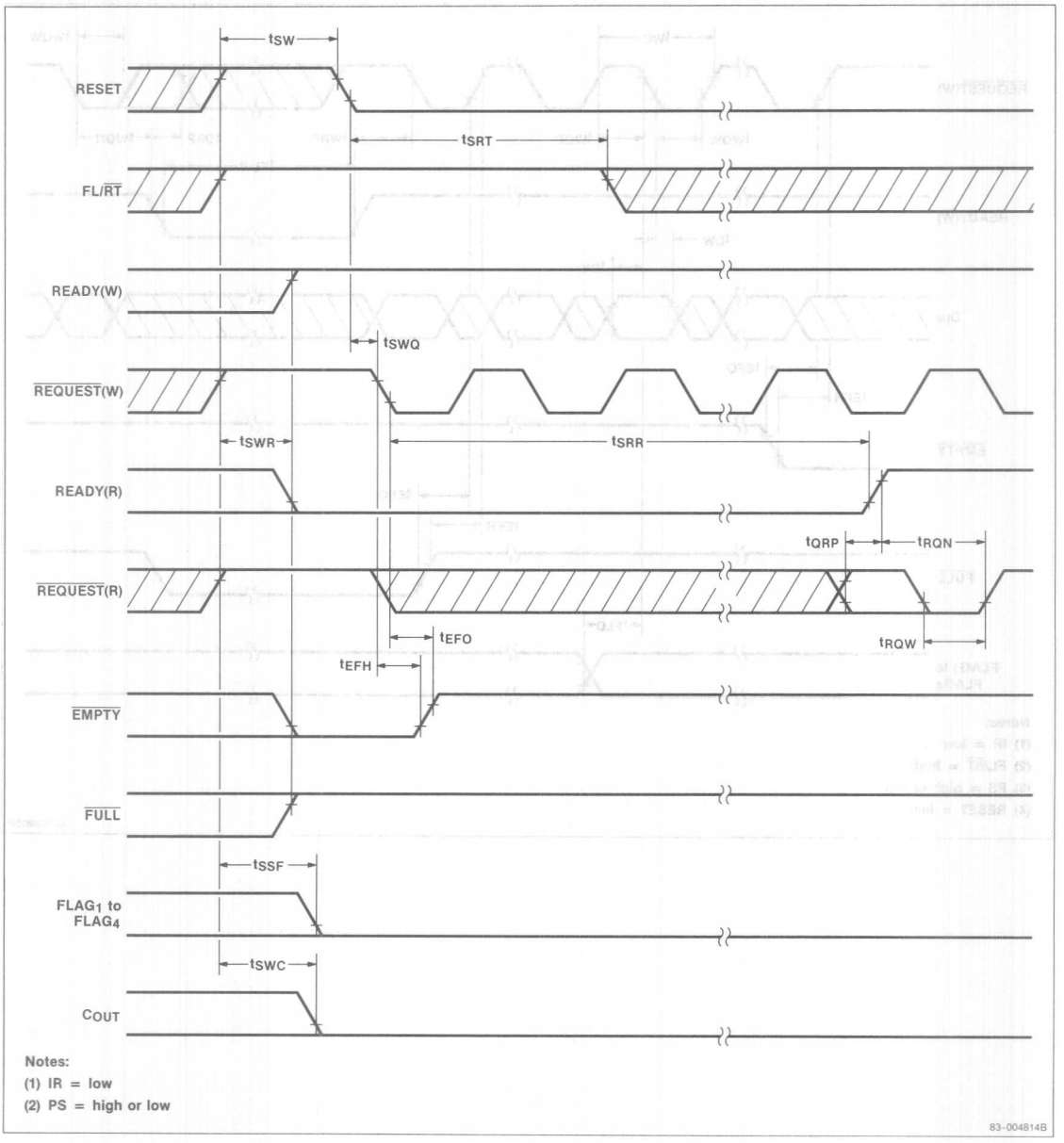


Figure 11. Output Loads



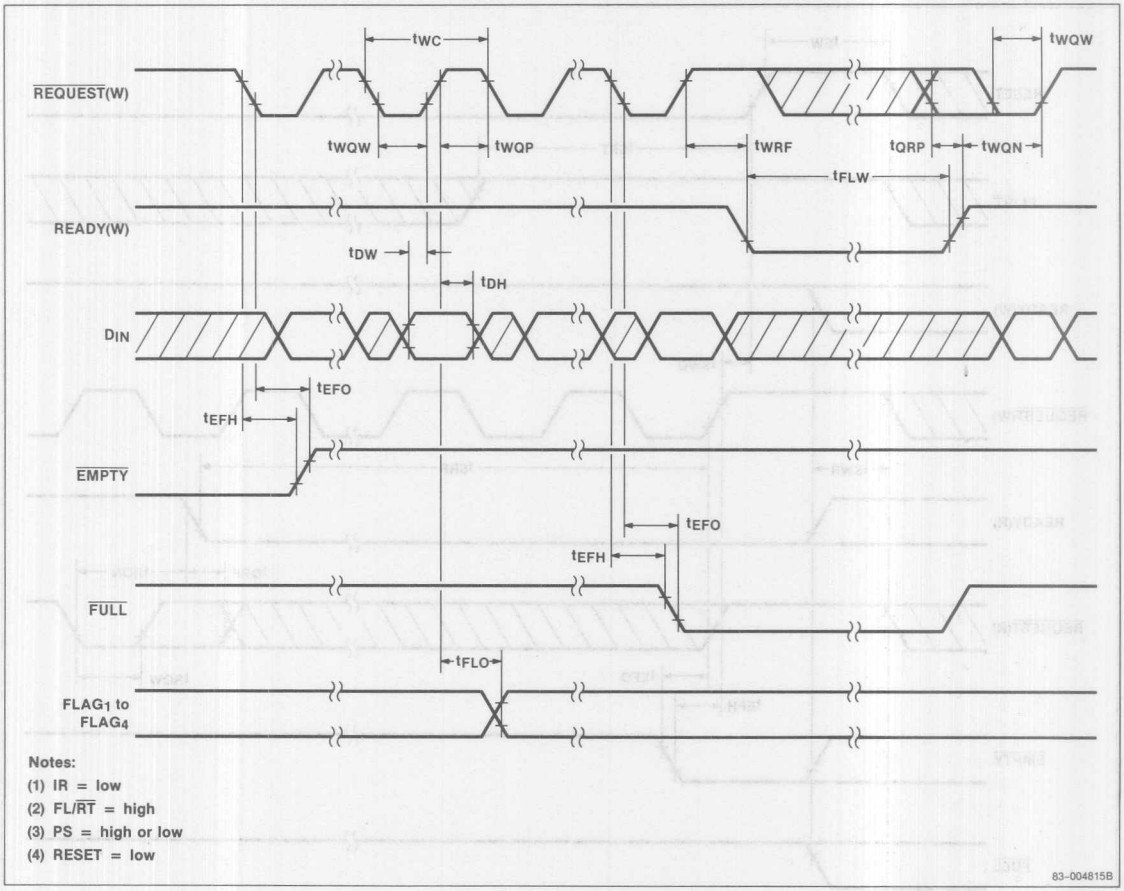
Timing Waveforms

Reset Cycle



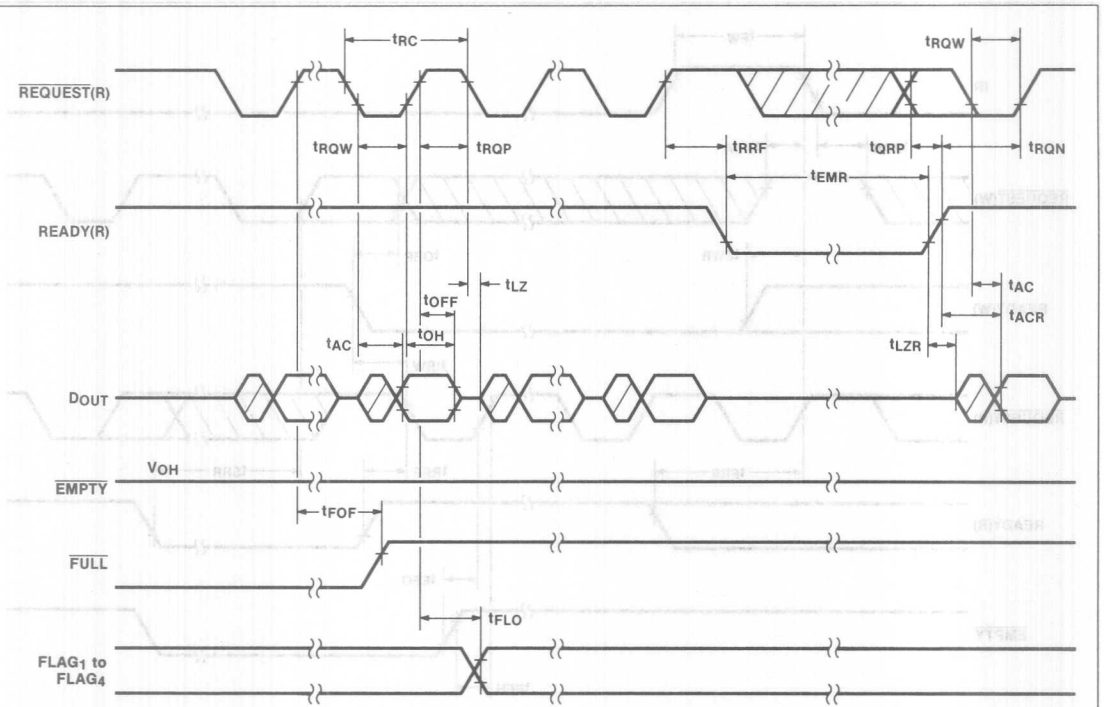
Timing Waveforms (cont)

Write Cycle



Timing Waveforms (cont)

Read Cycle



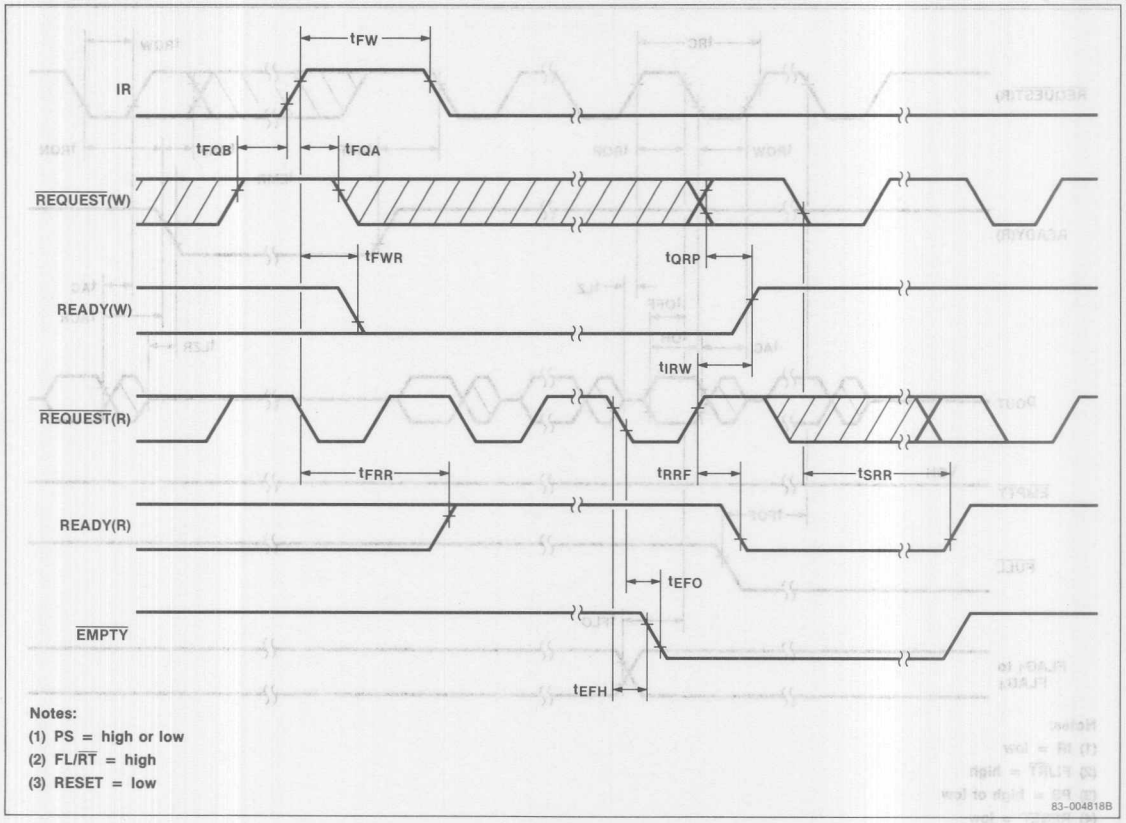
Notes:
(1) IR = low
(2) FL/$\overline{RT}$ = high
(3) PS = high or low
(4) RESET = low

83-004816B

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Timing Waveforms (cont)

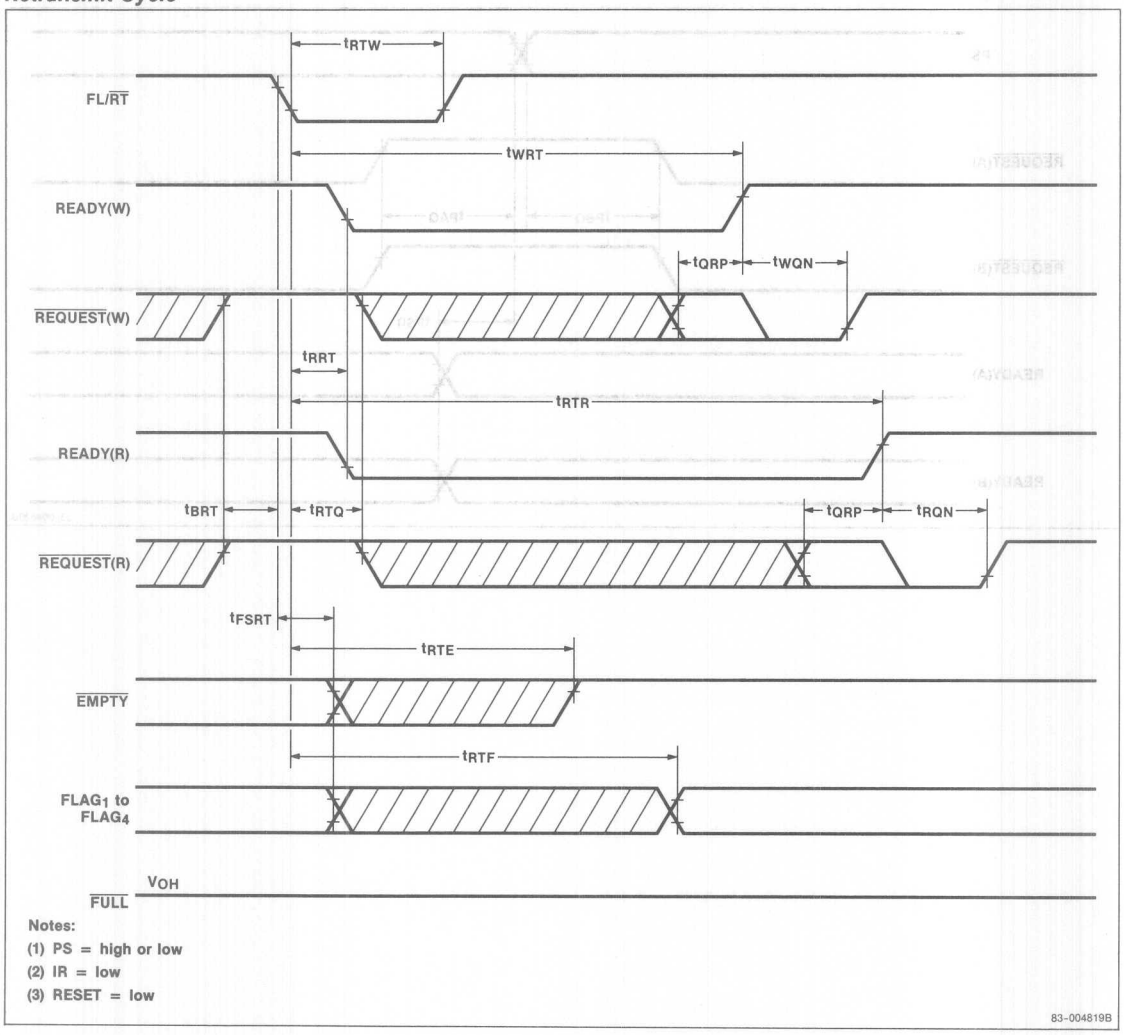
Interrupt Read Cycle



Notes:
(1) PS = high or low
(2) FL/$\overline{RT}$ = high
(3) RESET = low

Timing Waveforms (cont)

Retransmit Cycle

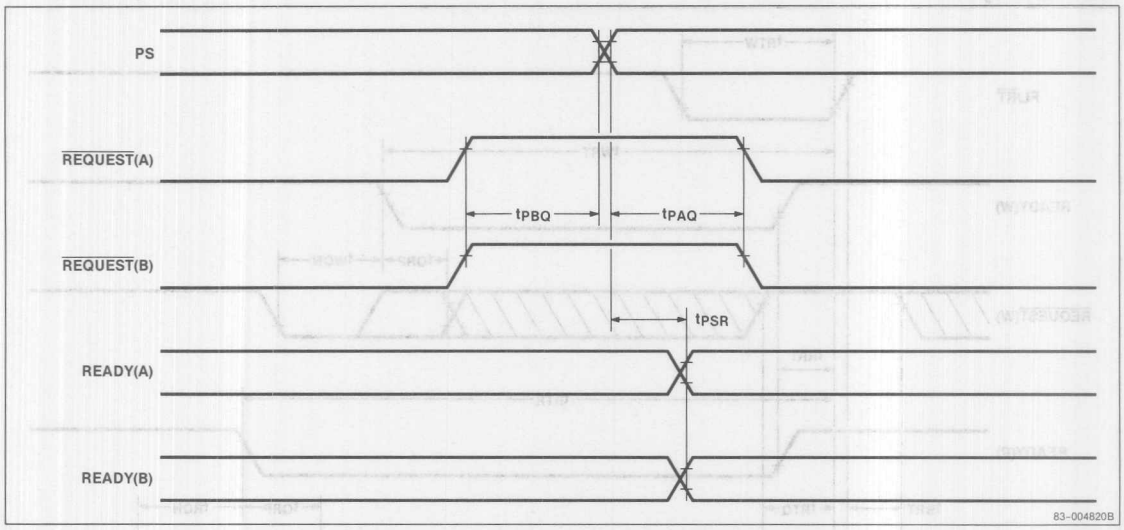


Notes:
(1) PS = high or low
(2) IR = low
(3) RESET = low

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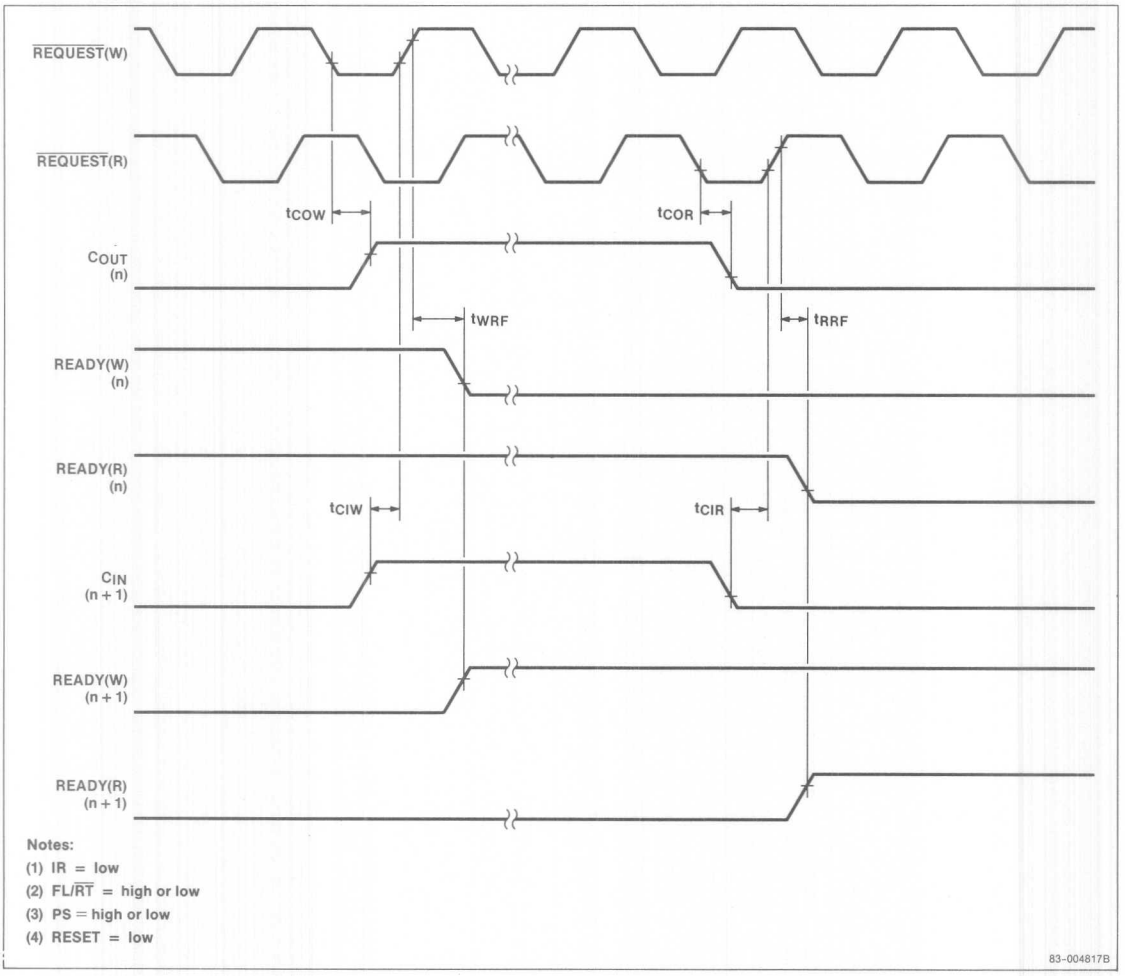
Timing Waveforms (cont)

Port Select Cycle



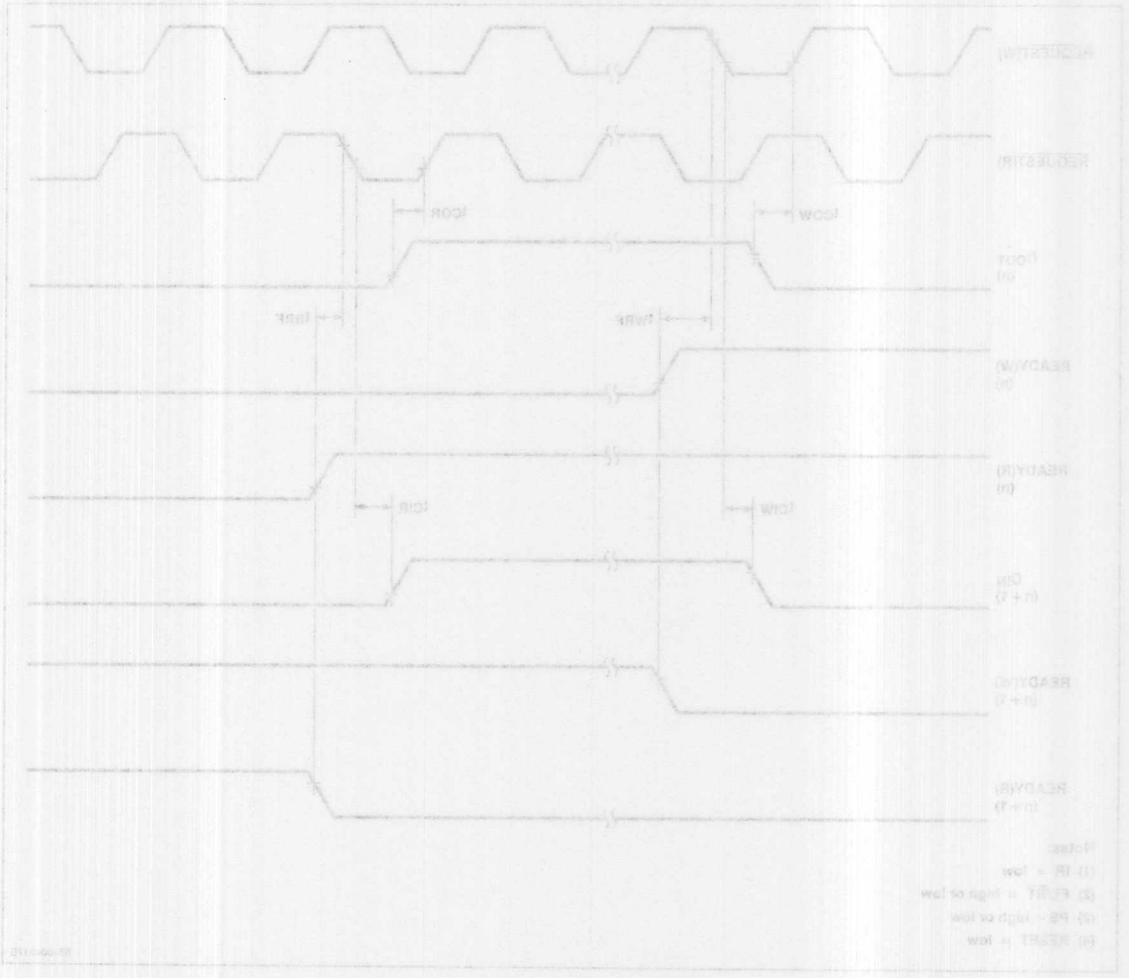
Timing Waveforms (cont)

Cascade Cycle



Notes:
(1) IR = low
(2) FL/$\overline{RT}$ = high or low
(3) PS = high or low
(4) RESET = low

83-004817B



Description

The μPD42601 silicon file is an economical mass storage device specifically designed to replace magnetic disk drives in silicon disk, solid-state recording, and system backup applications in a variety of computer systems. Organized as 1,048,576 words by 1 bit, the μPD42601 provides a battery backup feature for enhanced system performance and a substantial savings in power consumption.

The device is capable of executing standard access or page-mode write and read cycles. Refreshing is accomplished by means of $\overline{CAS}$ before $\overline{RAS}$ refresh cycles, $\overline{RAS}$-only refresh cycles, self-refresh cycles, or by normal read or write cycles on the 512 address combinations of A_0 through A_8 during a 32-ms period.

The μPD42601 is uniquely suitable for battery backup systems because it requires a very low power supply current for extended periods of self-refresh operation. If ambient temperature is limited to 50°C (max), as little as 30 μA (max) is required to maintain all data.

The μPD42601 is available in high-density 20-pin plastic ZIP or 26/20-pin plastic SOJ packaging.

Features

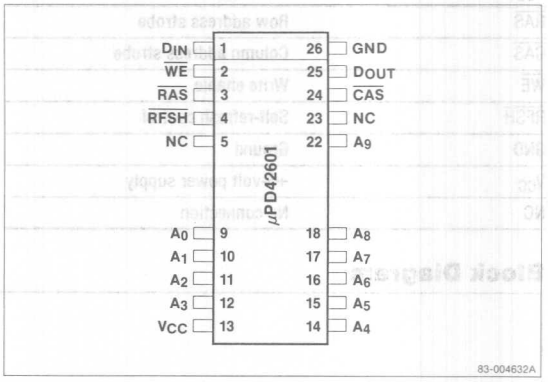
- ☐ 1,048,576-word by 1-bit organization
- ☐ Single +5-volt ±10% power supply
- ☐ CMOS technology
- ☐ Low operating power: 12 mA maximum
- ☐ 30 μA maximum self-refresh current at 0 to 50°C
- ☐ Read or write cycle time: 1000 ns minimum
- ☐ Page-mode cycle time: 200 ns minimum
- ☐ $\overline{CAS}$ before $\overline{RAS}$ refreshing
- ☐ 512 refresh cycles during 32-ms period
- ☐ Automatic self-refreshing by $\overline{RAS}$ input cycling

Ordering Information

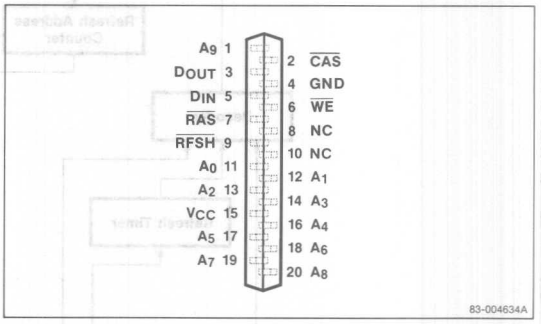
Part Number	Page-Mode Cycle (min)	Self-Refresh Current (max, 50°C)	Package
μPD42601LA-60	200 ns	120 μA	26/20-pin plastic SOJ
LA-60L	200 ns	30 μA	
μPD42601V-60	200 ns	120 μA	20-pin plastic ZIP
V-60L	200 ns	30 μA	

Pin Configurations

26/20-Pin Plastic SOJ



20-Pin Plastic ZIP



New 4 Mb density and 80 ns speed will be available first half of 1991.

Pin Identification

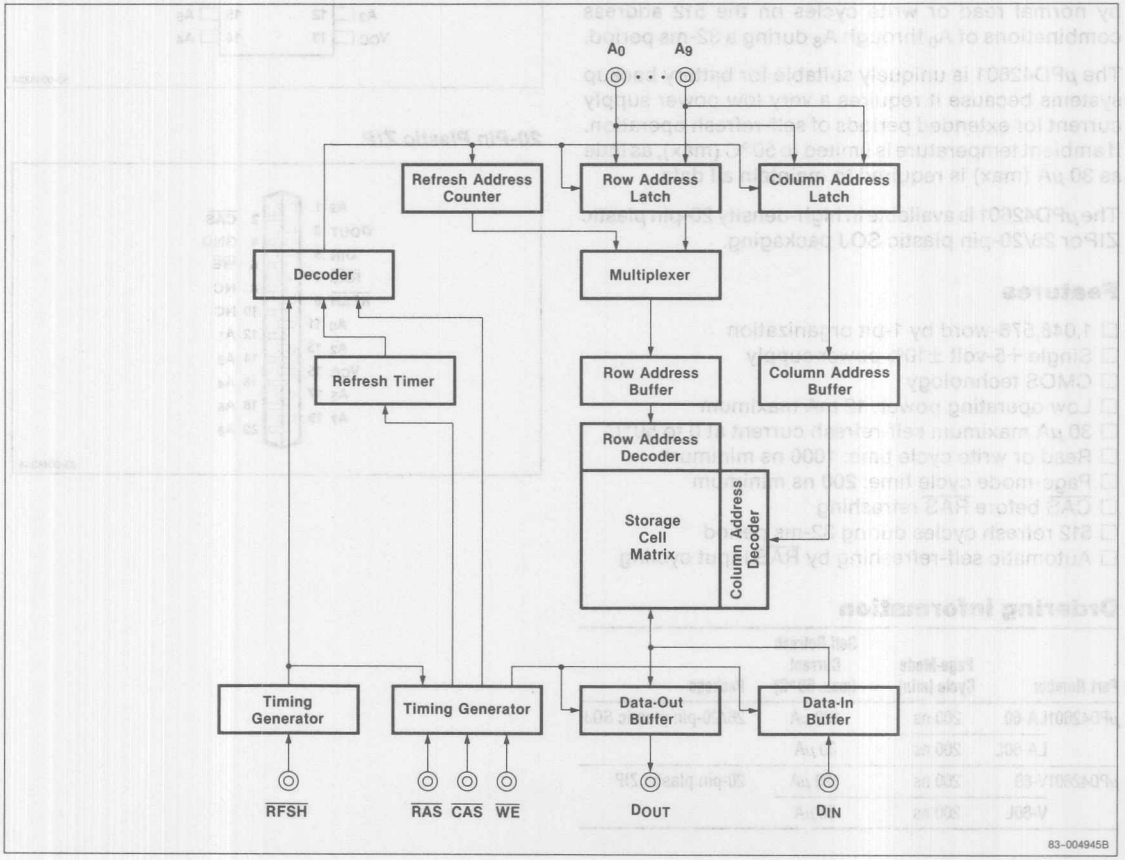
Name	Function
A_0 - A_9	Address inputs
D_{IN}	Data input
D_{OUT}	Data output
$\overline{RAS}$	Row address strobe
$\overline{CAS}$	Column address strobe
$\overline{WE}$	Write enable
$\overline{RFSH}$	Self-refresh control
GND	Ground
V_{CC}	+5-volt power supply
NC	No connection

Absolute Maximum Ratings

Voltage on any pin relative to GND, V_T	−1.0 to +7.0 V
Operating temperature, T_{OPR}	0 to +70°C
Storage temperature, T_{STG}	−55 to +125°C
Short-circuit output current, I_{OS}	50 mA
Power dissipation, P_D	1.0 W
Supply voltage, V_{CC}	−1.0 to +7.0 V

Comment: Exposure to Absolute Maximum Ratings for extended periods may affect device reliability; exceeding the ratings could cause permanent damage. The device should be operated within the limits specified under DC and AC Characteristics.

Block Diagram



Operation

Write and Read Operation

The μPD42601 is capable of standard write and read operation as well as page-mode operation. The ten row address bits are set up on pins A_0 through A_9 and latched onto the chip by $\overline{RAS}$. Subsequently, ten column address bits are set up on pins A_0 through A_9 and latched onto the chip by $\overline{CAS}$. An appropriate write or read cycle is executed according to the logical level of $\overline{WE}$: a high $\overline{WE}$ initiates a read cycle and low $\overline{WE}$ initiates a write cycle.

Page-mode operation may be executed by pulsing $\overline{CAS}$ repeatedly while maintaining a low $\overline{RAS}$. The first word is accessed in the same manner as in standard write and read operation, with row addresses latched onto the chip by $\overline{RAS}$ and column addresses latched by $\overline{CAS}$. Subsequent column addresses are accessed for each $\overline{CAS}$ cycle, repeated during a period up to the maximum $\overline{RAS}$ pulse width.

Refresh Operation

$\overline{CAS}$ before $\overline{RAS}$ Refreshing. This cycle may be initiated by bringing $\overline{CAS}$ low before $\overline{RAS}$ and holding it low after $\overline{RAS}$ falls. A built-in address counter makes external addressing unnecessary.

$\overline{RAS}$-Only Refreshing. $\overline{RAS}$-only refreshing is executed by holding $\overline{CAS}$ high as the row addresses are latched onto the chip by $\overline{RAS}$. Using this cycle, all storage cells are refreshed by the 512 address combinations of A_0 through A_8 during a 32-ms period.

Self-Refreshing. A self-refresh cycle is initiated for the addresses generated by the internal counter whenever $\overline{RFSH}$ is active low and the $\overline{RAS}$ input is cycling (see figure 1). Since the minimum required $\overline{RAS}$ cycling frequency depends on ambient temperature, power consumption will also vary with temperature as shown in the AC and DC Characteristics. For extended periods of self-refresh operation, a low supply current is required; e.g., if ambient temperature is limited to 50°C (max), as little as 30 μA (max) is required to maintain all data.

3

Recommended DC Operating Conditions

$T_A = 0$ to +70°C; GND = 0 V

		Limits			
Parameter	Symbol	Min	Typ	Max	Unit
Supply voltage	V_{CC}	4.5	5.0	5.5	V
Input voltage, high	V_{IH}	2.4		5.5	V
Input voltage, low	V_{IL}	−1.0		0.8	V

Capacitance

$T_A = 25$°C; f = 1 MHz

Parameter	Symbol	Max	Unit	Pins Under Test
Input capacitance	C_{I1}	5	pF	Address, D_{IN}
	C_{I2}	8	pF	$\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$, $\overline{RFSH}$
Output capacitance	C_D	7	pF	D_{OUT}

DC Characteristics

$T_A = 0$ to $+70°C$; $V_{CC} = +5.0\ V \pm 10\%$

Parameter	Symbol	Limits Min	Typ	Max	Unit	Test Conditions
Operating current, average	I_{CC1}			12	mA	$\overline{RAS}$, $\overline{CAS}$ cycling; $I_O = 0$ mA; $t_{RC} = t_{RC}$ (min)
Standby current	I_{CC2}			2.0	mA	$\overline{RAS} = \overline{CAS} = \overline{RFSH} = V_{IH}$
				0.5	mA	$\overline{RAS} = \overline{CAS} = \overline{RFSH} \geq V_{CC} - 0.4$; A_0-A_9, D_{IN} and $\overline{WE} \geq V_{CC} - 0.4$ or ≤ 0.4 V
Operating current, $\overline{RAS}$-only refresh, average	I_{CC3}			10	mA	$t_{RC} = t_{RC}$ (min); $I_O = 0$ mA
Operating current, $\overline{CAS}$ before $\overline{RAS}$ refresh, average	I_{CC4}			10	mA	$t_{RC} = t_{RC}$ (min); $I_O = 0$ mA
Operating current, self-refresh mode, average	I_{CC5}			30	μA	$\overline{RAS}$ cycling at 50 kHz (Notes 1, 2, 3, 4)
				60	μA	$\overline{RAS}$ cycling at 100 kHz (Notes 1, 2, 3, 4)
				120	μA	$\overline{RAS}$ cycling at 200 kHz (Notes 1, 2, 3)
Operating current, page mode, average	I_{CC6}			12	mA	$t_{PC} = t_{PC}$ (min); $I_O = 0$ mA
Input leakage current	I_{IL}	−1		1	μA	$V_{IN} = 0$ to V_{CC}; all other pins not under test = 0 V
Output leakage current	I_{OL}	−1		1	μA	D_{OUT} disabled; $V_{OUT} = 0$ to V_{CC}
Output voltage, low	V_{OL}			0.4	V	$I_O = 4.2$ mA
Output voltage, high	V_{OH}	2.4			V	$I_O = -5$ mA

Notes:

(1) When $t_{FAS} \leq 2.5$ ms, I_{CC5} does not depend on the $\overline{RAS}$ clock; I_{CC5} (max) = 500 μA. When $t_{FAS} \geq 2.5$ ms, I_{CC5} (max) = 500 μA in the first 2.5 ms after $\overline{RFSH}$ falls (it does not depend on the $\overline{RAS}$ clock). Subsequently, I_{CC5} is 120 μA for the μPD42601 or is as shown in the following table for the μPD42601-L.

Operating Temperature [T_A]	Clock Frequency [min]	Self-Refresh Current [max]
0 to 50°C	50 kHz	30 μA at 50 kHz
0 to 60°C	100 kHz	60 μA at 100 kHz
0 to 70°C	200 kHz	120 μA at 200 kHz

(2) t_{RCF} depends on operating temperature as reflected in the table below (see figures 2 and 3).

Operating Temperature [T_A]	t_{RCF} [max] μPD42601-L	μPD42601
0 to 50°C	20 μs	5 μs
0 to 60°C	10 μs	5 μs
0 to 70°C	5 μs	5 μs

(3) Average power supply current required for self refreshing is measured according to the following conditions: $\overline{RAS}$ is cycling at 50, 100 or 200 kHz; $V_{IH} \geq V_{CC} - 0.4$ V; $V_{IL} \leq 0.4$ V; $t_T \leq 50$ ns; A_0 to A_9, D_{IN}, $\overline{WE}$ and $\overline{CAS} = V_{CC}$ to GND; RFSH = V_{IL}. When $\overline{RFSH} = V_{IL}$ (≤ 0.4 V), the $\overline{RAS}$ input must be cycled at or exceeding the minimum frequency requirements.

(4) This specification applies to the μPD42601-L only. For the non-L version, I_{CC5} is 120 μA, maximum, at all T_A.

AC Characteristics

$T_A = 0$ to $+70°C$; $V_{CC} = +5.0\ V \pm 10\%$

Parameter	Symbol	Limits Min	Max	Unit	Test Conditions
Random read or write cycle time	t_{RC}	1000		ns	(Note 5)
Page-mode cycle time	t_{PC}	200		ns	(Notes 5, 15)
Access time from $\overline{RAS}$	t_{RAC}		600	ns	(Notes 6, 7)
Access time from $\overline{CAS}$ (falling edge)	t_{CAC}		100	ns	(Notes 6, 8)
Output buffer turnoff delay	t_{OFF}	0	100	ns	(Note 9)
Transition time (rise and fall)	t_T	3	50	ns	(Notes 3, 4)
$\overline{RAS}$ precharge time	t_{RP}	390		ns	
$\overline{RAS}$ pulse width	t_{RAS}	600	100000	ns	
$\overline{RAS}$ hold time	t_{RSH}	100		ns	
$\overline{CAS}$ pulse width	t_{CAS}	100	10000	ns	
$\overline{CAS}$ hold time	t_{CSH}	600		ns	
$\overline{RAS}$ to $\overline{CAS}$ delay time	t_{RCD}	150	500	ns	(Note 10)
$\overline{CAS}$ to $\overline{RAS}$ precharge time	t_{CRP}	30		ns	(Note 11)
$\overline{CAS}$ precharge time (non-page cycle)	t_{CPN}	90		ns	
$\overline{CAS}$ precharge time (page cycle)	t_{CP}	90		ns	(Note 15)
$\overline{RAS}$ precharge $\overline{CAS}$ hold time	t_{RPC}	0		ns	

AC Characteristics (cont)

$T_A = 0$ to +70°C; $V_{CC} = +5.0$ V ±10%

Parameter	Symbol	Limits Min	Limits Max	Unit	Test Conditions
Row address setup time	t_{ASR}	0		ns	
Row address hold time	t_{RAH}	90		ns	
Column address setup time	t_{ASC}	0		ns	
Column address hold time	t_{CAH}	90		ns	
Column address hold time referenced to $\overline{RAS}$	t_{AR}	590		ns	
Read command setup time	t_{RCS}	0		ns	
Read command hold time referenced to $\overline{RAS}$	t_{RRH}	75		ns	(Note 12)
Read command hold time referenced to $\overline{CAS}$	t_{RCH}	0		ns	(Note 12)
Write command hold time	t_{WCH}	90		ns	
Write command hold time referenced to $\overline{RAS}$	t_{WCR}	590		ns	
Write command pulse width	t_{WP}	90		ns	
Data-in setup time	t_{DS}	0		ns	(Note 14)
Data-in hold time	t_{DH}	90		ns	(Note 14)
Data-in hold time referenced to $\overline{RAS}$	t_{DHR}	590		ns	
Write command setup time	t_{WCS}	0		ns	
$\overline{CAS}$ setup time for $\overline{CAS}$ before $\overline{RAS}$ refresh	t_{CSR}	30		ns	
$\overline{CAS}$ hold time for $\overline{CAS}$ before $\overline{RAS}$ refresh	t_{CHR}	105		ns	
Refresh period	t_{REF}		32	ms	Addresses A_0-A_8
Self-Refresh Cycle					
$\overline{RFSH}$ pulse width	t_{FAS}	810		ns	(Note 13)
$\overline{RAS}$ to $\overline{RFSH}$ delay time	t_{RFD}	100		ns	
$\overline{RAS}$ setup time to $\overline{RFSH}$	t_{FRS}	200		ns	
$\overline{RAS}$ cycle time in self-refresh mode	t_{RCF}	1000		ns	(Note 16)
$\overline{RAS}$ precharge time in self-refresh mode	t_{RPF}	390		ns	
$\overline{RAS}$ pulse width in self-refresh mode	t_{RSF}	600		ns	
$\overline{RFSH}$ to $\overline{RAS}$ delay time	t_{FRD}	100		ns	
$\overline{RAS}$ hold time in self-refresh mode	t_{FRH}	200		ns	

Notes:

(1) All voltages are referenced to GND.

(2) An initial pause of 100 μs is required after power-up (V_{CC} = +5.0 V ±10%), followed by any eight $\overline{RAS}$ cycles, before proper device operation is achieved. $\overline{RAS}$, $\overline{CAS}$, and $\overline{RFSH}$ must equal V_{IH} during the initial pause.

(3) Ac measurements assume $t_T = 5$ ns.

(4) V_{IH} (min) and V_{IL} (max) are reference levels for measuring timing of input signals. Transition times are measured between V_{IH} and V_{IL}.

(5) The minimum specifications are used only to indicate the cycle time at which proper operation over the full temperature range (T_A = 0 to +70°C) is assured.

(6) Load = 2 TTL loads and 100 pF (V_{OH} = 2.4 V, V_{OL} = 0.4 V).

(7) Assumes that $t_{RCD} \leq t_{RCD}$ (max). If t_{RCD} is greater than the maximum recommended value in this table, t_{RAC} increases by the amount that t_{RCD} exceeds the value shown.

(8) Assumes that $t_{RCD} \geq t_{RCD}$ (max).

(9) t_{OFF} (max) defines the time at which the output achieves the open-circuit condition and is not referenced to V_{OH} or V_{OL}.

(10) Operation within the t_{RCD} (max) limit assures that t_{RAC} (max) can be met. t_{RCD} (max) is specified as a reference point only; if t_{RCD} is greater than t_{RCD} (max), access time is controlled exclusively by t_{CAC}.

(11) The t_{CRP} requirement should be applicable for $\overline{RAS}$/$\overline{CAS}$ cycles preceded by any cycle.

(12) Either t_{RRH} or t_{RCH} must be satisfied for a read cycle.

(13) When $t_{FAS} \leq 2.5$ ms, I_{CC5} does not depend on the $\overline{RAS}$ clock; I_{CC5} (max) = 500 μA. When $t_{FAS} \geq 2.5$ ms, I_{CC5} (max) = 500 μA for the first 2.5 ms after $\overline{RFSH}$ falls (it does not depend on the $\overline{RAS}$ clock). Subsequently, I_{CC5} is 120 μA for the μPD42601 or is as shown in the following table for the μPD42601-L.

Operating Temperature [T_A]	Clock Frequency [min]	Self-Refresh Current [max]
0 to 50°C	50 kHz	30 μA at 50 kHz
0 to 60°C	100 kHz	60 μA at 100 kHz
0 to 70°C	200 kHz	120 μA at 200 kHz

3

Notes [cont]:

(14) These parameters are referenced to the falling edge of $\overline{CAS}$ for early write cycles.

(15) This parameter is applicable to page-mode operation.

(16) t_{RCF} depends on operating temperature as reflected in the table below (see figures 2 and 3).

Operating Temperature [T_A]	t_{RCF} [max]	
	μPD42601-L	μPD42601
0 to 50°C	20 μs	5 μs
0 to 60°C	10 μs	5 μs
0 to 70°C	5 μs	5 μs

Figure 1. Internal Address Generation in Self-Refresh Operation

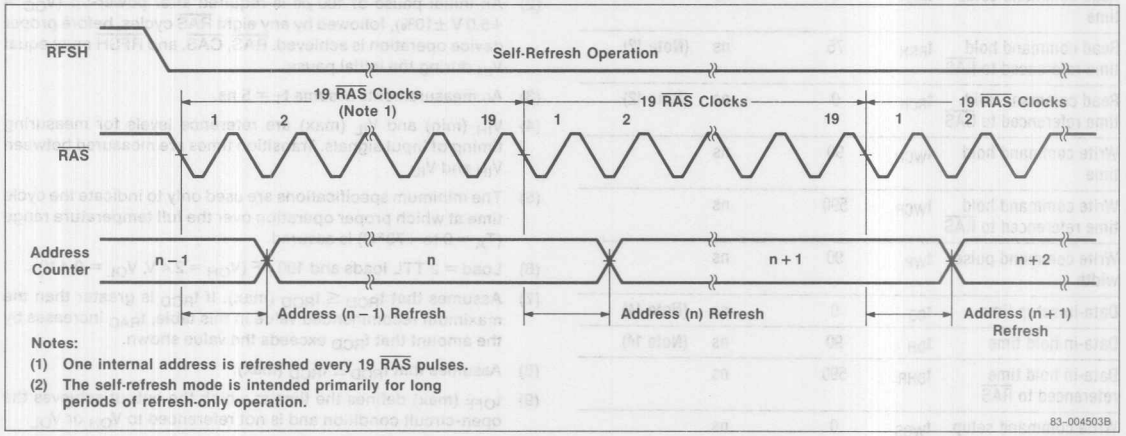
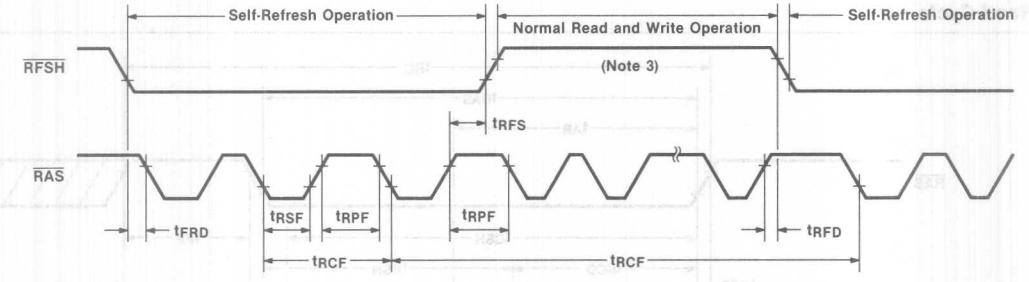


Figure 2. Special Requirement for t_{RCF} Near Periods of Limited Standard Refresh Cycles



Notes:

[1] The value for t_{RCF} [min] is specified in AC Characteristics. The value for t_{RCF} [max] is dependent upon temperature and shown in the table below.

	t_{RCF} [max]	
T_A	μPD42601-L	μPD42601
50 °C	20 μs	5 μs
60 °C	10 μs	5 μs
70 °C	5 μs	5 μs

[2] When exiting self-refresh to a period of read and write operation which includes CBR refresh cycles, t_{RCF} is the delay between the last self-refresh pulse and the first CBR cycle. When entering self-refresh operation, t_{RCF} is the delay between the last CBR cycle and the first self-refresh pulse.

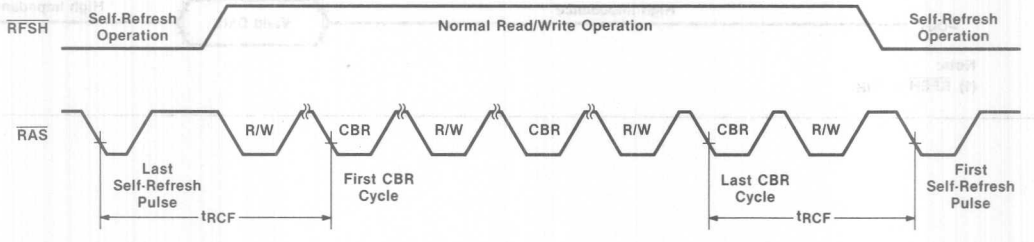
[3] In this period of normal read/write operation, there are no CBR refresh cycles or less than 512 $\overline{RAS}$-only refresh cycles.

[4] The time delay between the last self-refresh pulse in one self-refresh cycle, and the first self-refresh pulse in the next cycle, is defined by t_{RCF} [max] when the intervening period of read and write operation meets the conditions in Note 3.

[5] The built-in counter generates the refresh address in self-refresh and CBR refresh cycles. Since this address increments sequentially from the last cycle in either self-refresh or CBR operation to the first cycle in the alternate refresh mode, CBR refreshing should be used during normal read and write operation to refresh one address location every 62 μs or less. If some other means of refreshing is used, it is necessary to do a burst refresh of all storage cells just before changing to and just after exiting self-refresh operation.

83-004502B

Figure 3. Timing Restrictions for Entering and Exiting Self-Refresh Operation



Notes:

[1] The value for t_{RCF} [min] is specified in AC Characteristics. The value for t_{RCF} [max] is dependent upon temperature and shown in the table below.

	t_{RCF} [max]	
T_A	μPD42601-L	μPD42601
50 °C	20 μs	5 μs
60 °C	10 μs	5 μs
70 °C	5 μs	5 μs

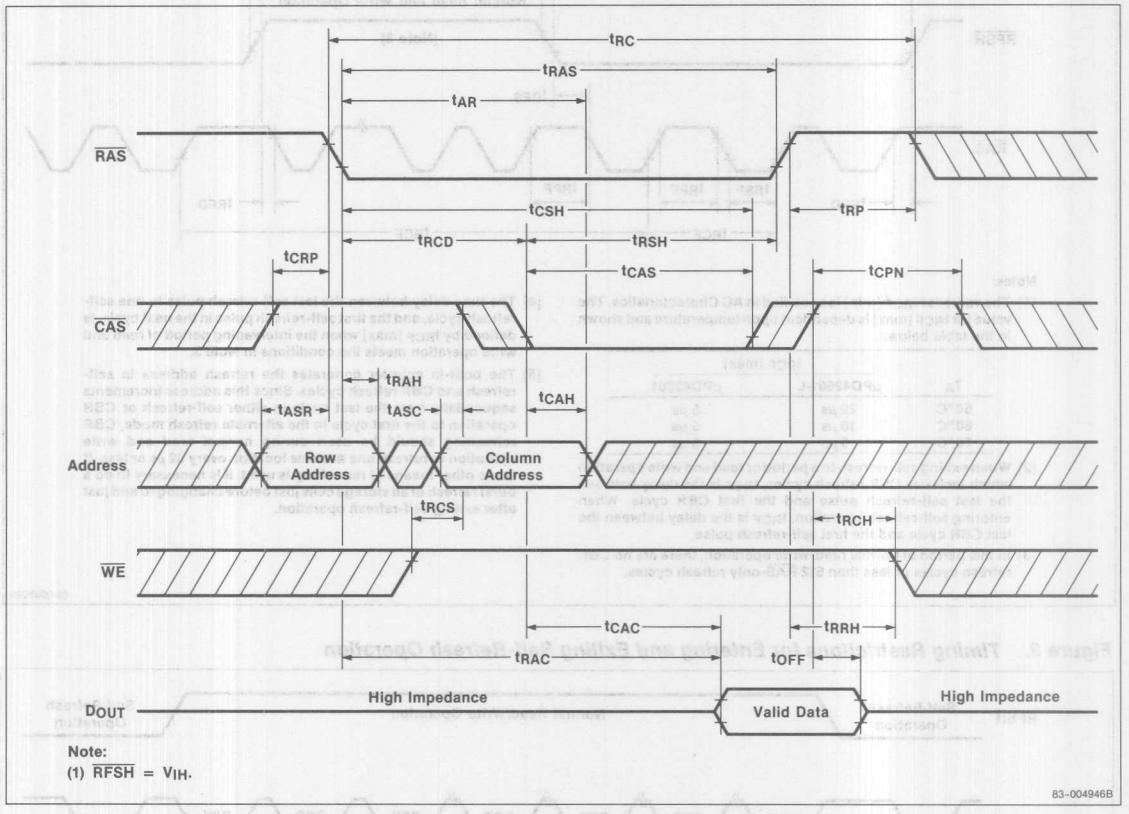
[2] When exiting self-refresh to a period of read and write operation which includes CBR refresh cycles, t_{RCF} is the delay between the last self-refresh pulse and the first CBR cycle. When entering self-refresh operation, t_{RCF} is the delay between the last CBR cycle and the first self-refresh pulse.

[3] The built-in counter generates the refresh address in self-refresh and CBR refresh cycles. Since this address increments sequentially from the last cycle in either self-refresh or CBR operation to the first cycle in the alternate refresh mode, CBR refreshing should be used during normal read and write operation to refresh one address location every 62 μs or less. If some other means of refreshing is used, it is necessary to do a burst refresh of all storage cells just before changing to and just after exiting self-refresh operation.

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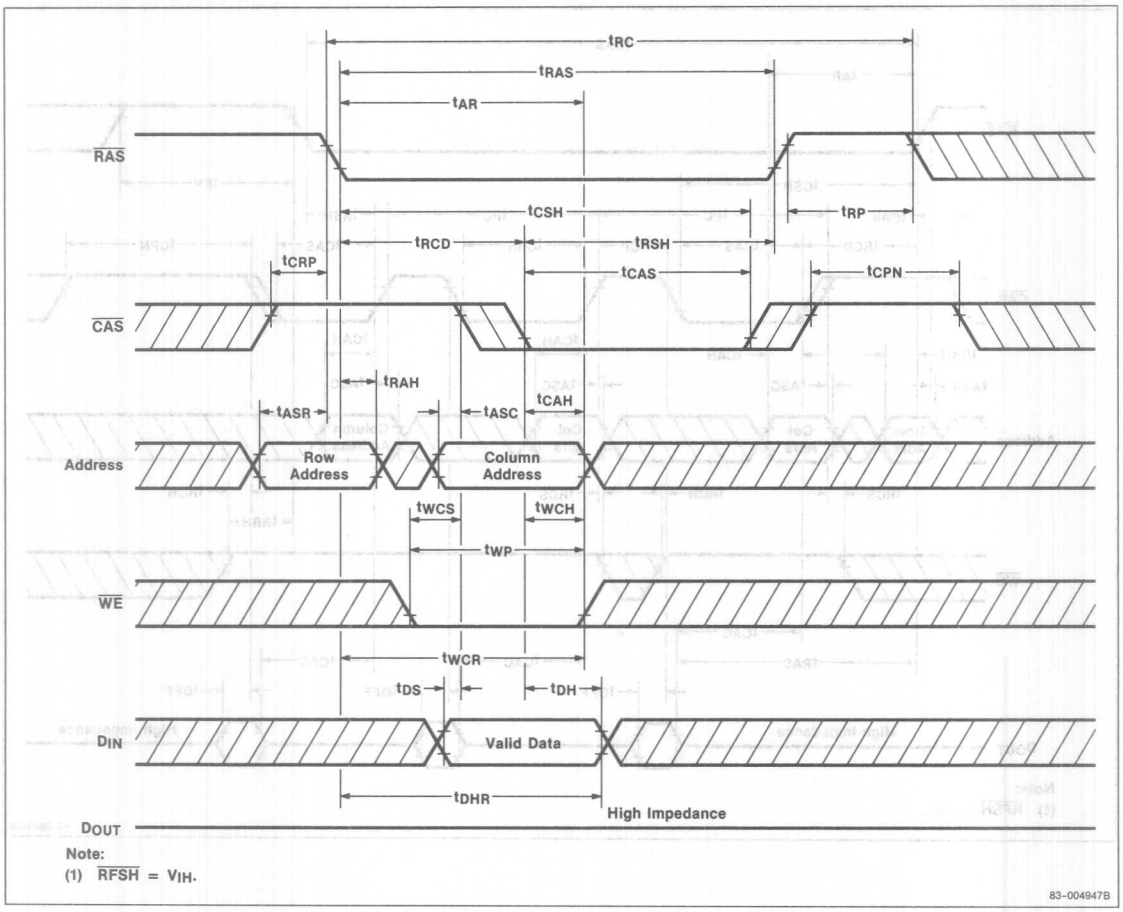
Timing Waveforms

Read Cycle



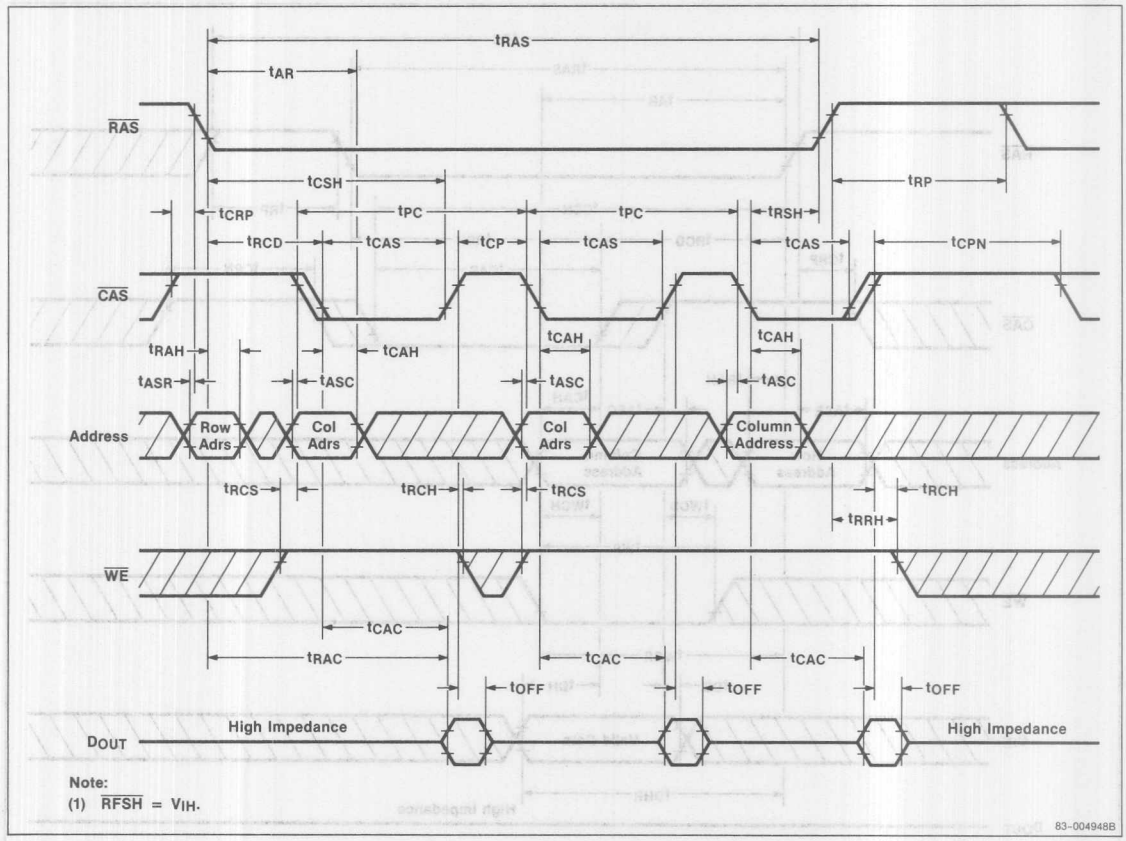
Timing Waveforms (cont)

Write Cycle (Early Write)



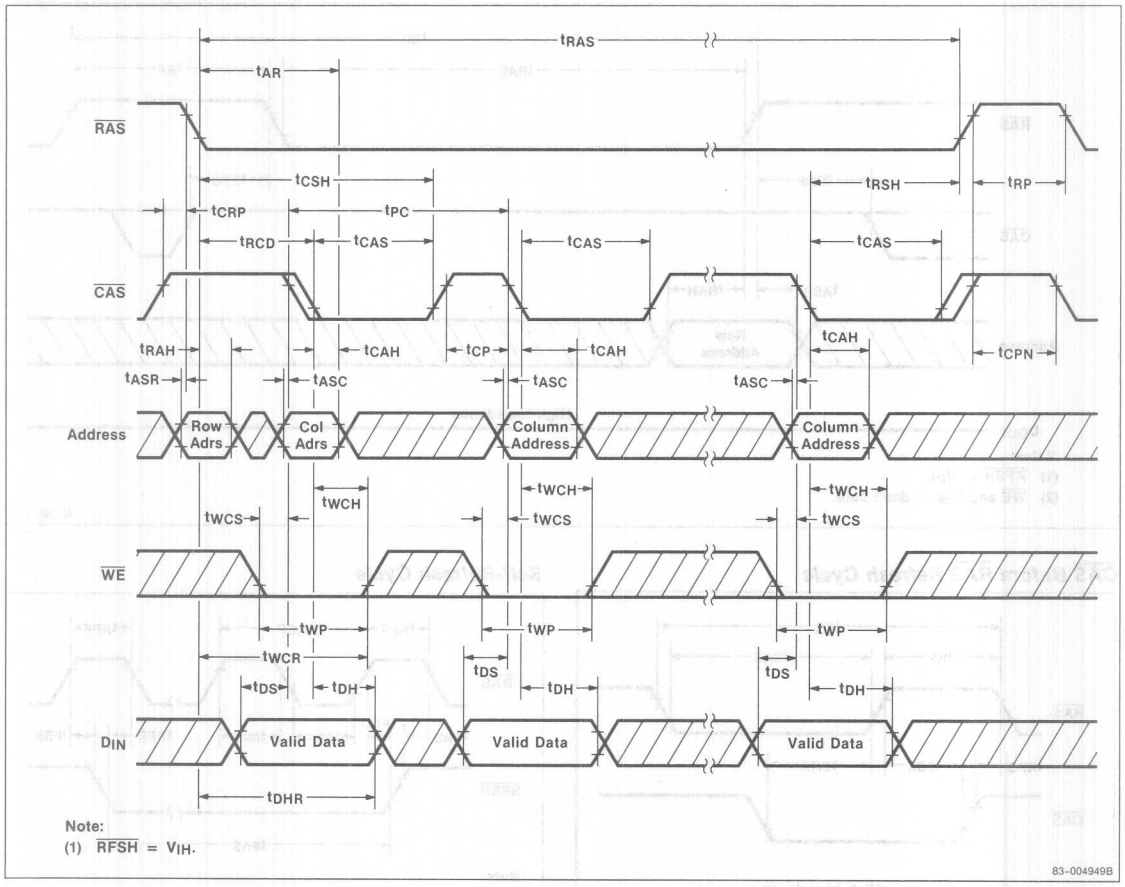
Timing Waveforms (cont)

Page-Mode Read Cycle



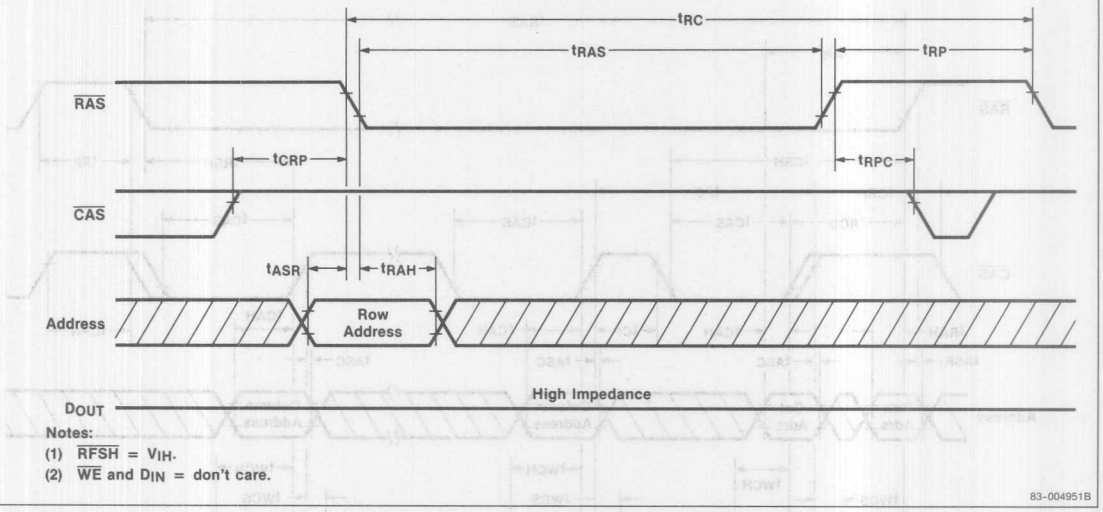
Timing Waveforms (cont)

Page-Mode Write Cycle (Early Write)



Timing Waveforms (cont)

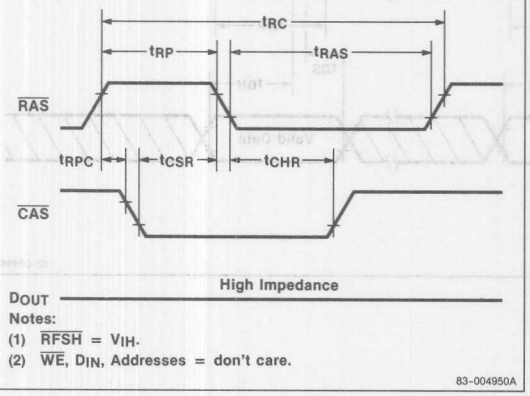
$\overline{RAS}$-Only Refresh Cycle



Notes:
(1) $\overline{RFSH}$ = V_{IH}.
(2) $\overline{WE}$ and D_{IN} = don't care.

83-004951B

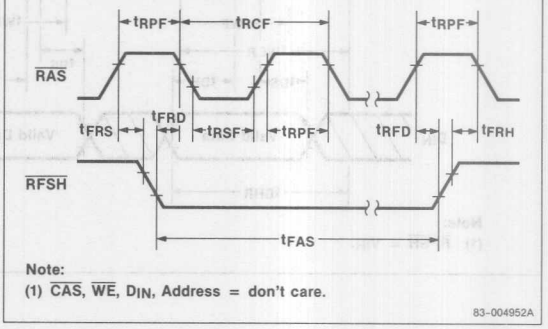
$\overline{CAS}$ Before $\overline{RAS}$ Refresh Cycle



Notes:
(1) $\overline{RFSH}$ = V_{IH}.
(2) $\overline{WE}$, D_{IN}, Addresses = don't care.

83-004950A

Self-Refresh Cycle



Note:
(1) $\overline{CAS}$, $\overline{WE}$, D_{IN}, Address = don't care.

83-004952A

NEC Electronics Inc.

μPD43501
1,024-CHANNEL TIME DIVISION SWITCH

Description

The μPD43501 is a time-switch device designed for use in a high-performance digital communications network. Features include a time-switch function by which up to 1,024 channels can be exchanged using a 16-bit data width, and a tone output function by which an 8-bit tone signal can be output to an arbitrary channel.

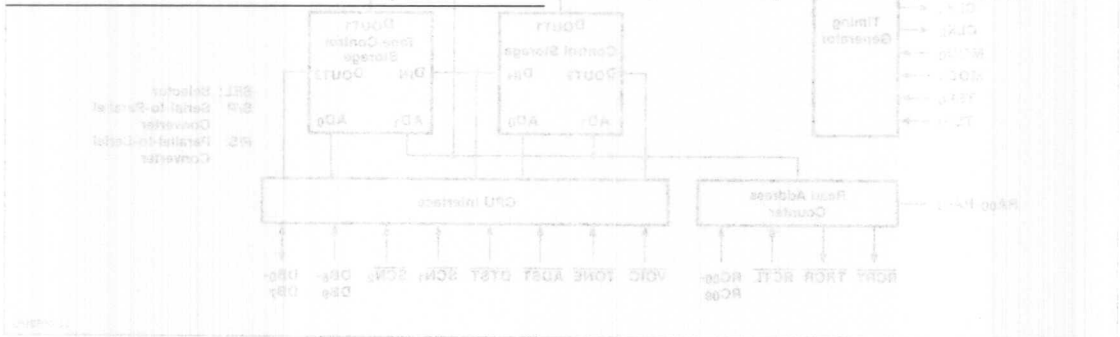
Two planes of 1-kword by 8-bit storage area and one plane of 1-kword by 10-bit control storage area for the time-switch function enable the μPD43501 to realize switching modes in which arbitrary 1,024 or 512 input channels can be connected to arbitrary 1,024 or 512 output channels. The configuration of the tone signal output section, one plane of 64-word by 8-bit tone storage area and one plane of 1-kword by 8-bit tone control storage area, allows the device to output up to 64 different tone signals to an arbitrary output channel as 8-bit voice/tone data.

Ordering Information

Part Number	Data Transfer Rate (max)	Package
μPD43501R	8.192 Mbps	132-pin ceramic pin grid array (PGA)

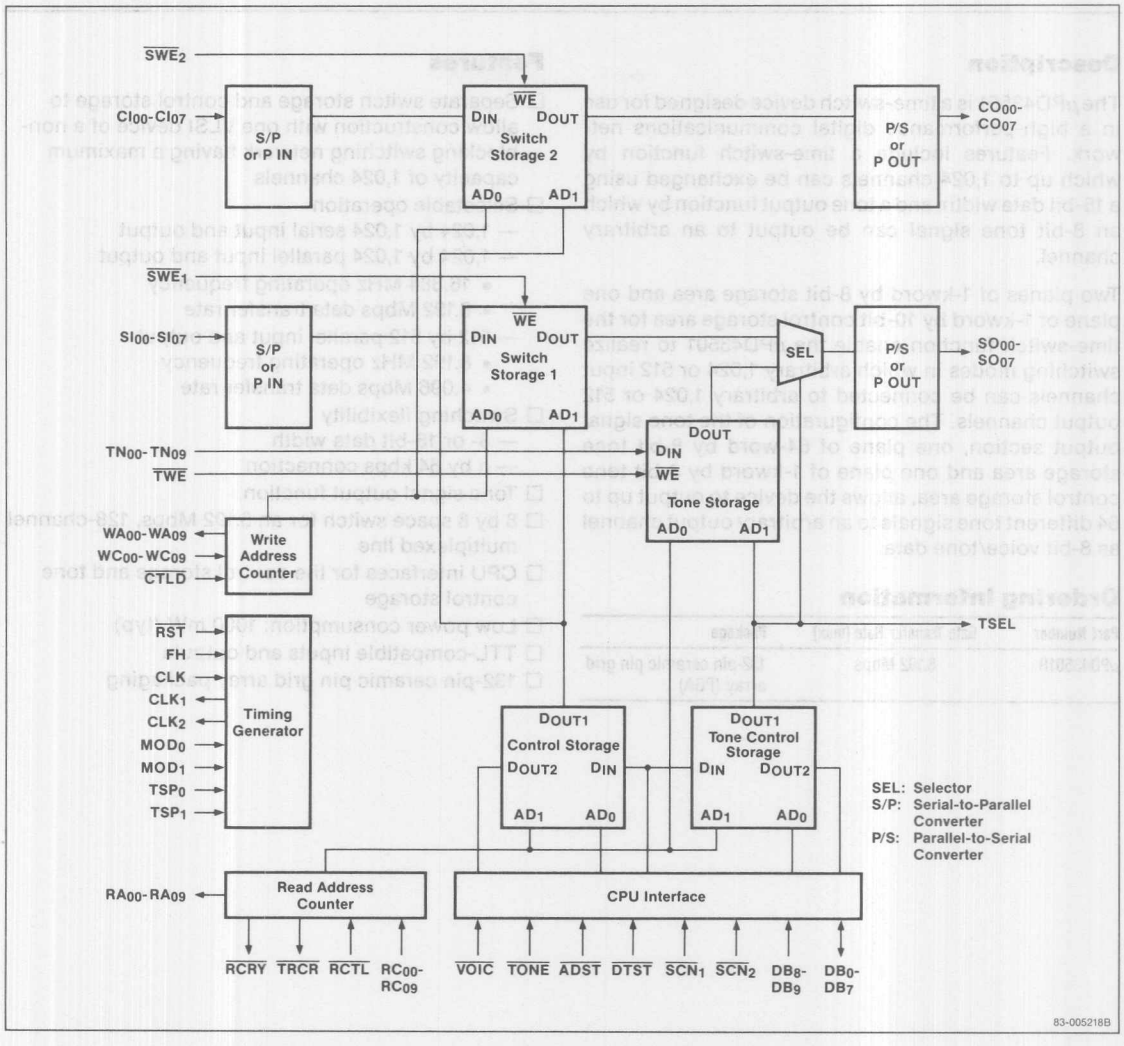
Features

- ☐ Separate switch storage and control storage to allow construction with one VLSI device of a non-blocking switching network having a maximum capacity of 1,024 channels
- ☐ Selectable operation
  - — 1,024 by 1,024 serial input and output
  - — 1,024 by 1,024 parallel input and output
    - • 16.384 MHz operating frequency
    - • 8.192 Mbps data transfer rate
  - — 512 by 512 parallel input and output
    - • 8.192 MHz operating frequency
    - • 4.096 Mbps data transfer rate
- ☐ Switching flexibility
  - — 8- or 16-bit data width
  - — n by 64 kbps connection
- ☐ Tone signal output function
- ☐ 8 by 8 space switch for an 8.192 Mbps, 128-channel multiplexed line
- ☐ CPU interfaces for the control storage and tone control storage
- ☐ Low power consumption: 1000 mW (typ)
- ☐ TTL-compatible inputs and outputs
- ☐ 132-pin ceramic pin grid array packaging



Contact your NEC sales representative for a copy of the complete data sheet.

Block Diagram



Switching Functions

Mode 0

In this mode, the μPD43501 inputs eight 128-channel multiplexed lines from ports SI_{00} through SI_{07} (or from CI_{00} through CI_{07}) and outputs eight 128-channel multiplexed lines to ports SO_{00} through SO_{07} (or CO_{00} through CO_{07}). Refer to figure 1 for a functional pin diagram.

Serial input data from the input ports first is converted to parallel data by the serial-to-parallel converters in the receive section, and then multiplexed and sent to the input section of the switch storage area. Since the write address counter is synchronized with input data, the write address of the switch storage area corresponds to the time slot number of the input signal. Writing multiplexed data to the switch address specified by the write address counter causes input data in the time slot corresponding to the switch address always to be stored at that address (figure 2).

Conversely, a control storage address corresponds to an output-side time slot number, and the data in control storage indicates the switch storage address, i.e., the input-side time slot number is stored at the control storage address corresponding to the output-side time slot to which the input-side is transferred.

The address signal is sent from the read address counter to control storage in synchronization with each output-side time slot. Data read out by this operation is then sent to the switch storage area as the address signal, and the data in the specified address (input-side time slot) is then read out on the output side and switched. Switched data is sent to the parallel-to-serial converters in the transmission section, where it is converted to serial data and then output to the appropriate output ports.

With this switching function, the data in an arbitrary time slot on the input side can be output as data in an arbitrary time slot on the output side. Furthermore, in addition to the time division switch function, a space switch function enables switching time slots on any of the eight input ports to be output on any of the eight output ports. This means that a nonblocking 8 x 8 space switch for 128-channel multiplexed lines can be realized.

Mode 1

Mode 1 makes it possible for the μPD43501 to input 512-channel multiplexed lines (4.096 Mbps by 8 bits), 8 bits in parallel, and output 512-channel multiplexed lines, 8 bits in parallel. The input signals received on the input ports are sent to the switch storage area in parallel, after which the same switching functions described in Mode 0 are then performed.

Mode 2

In Mode 2, the μPD43501 inputs 1,024-channel multiplexed lines (8.192 Mbps by 8 bits), 8 bits in parallel, and outputs 1,024-channel multiplexed lines, 8 bits in parallel. The input signals received on the input ports are sent to the switch storage area in parallel, after which the same switching functions described in Mode 0 are performed.

Figure 1. Functional Pin Diagram

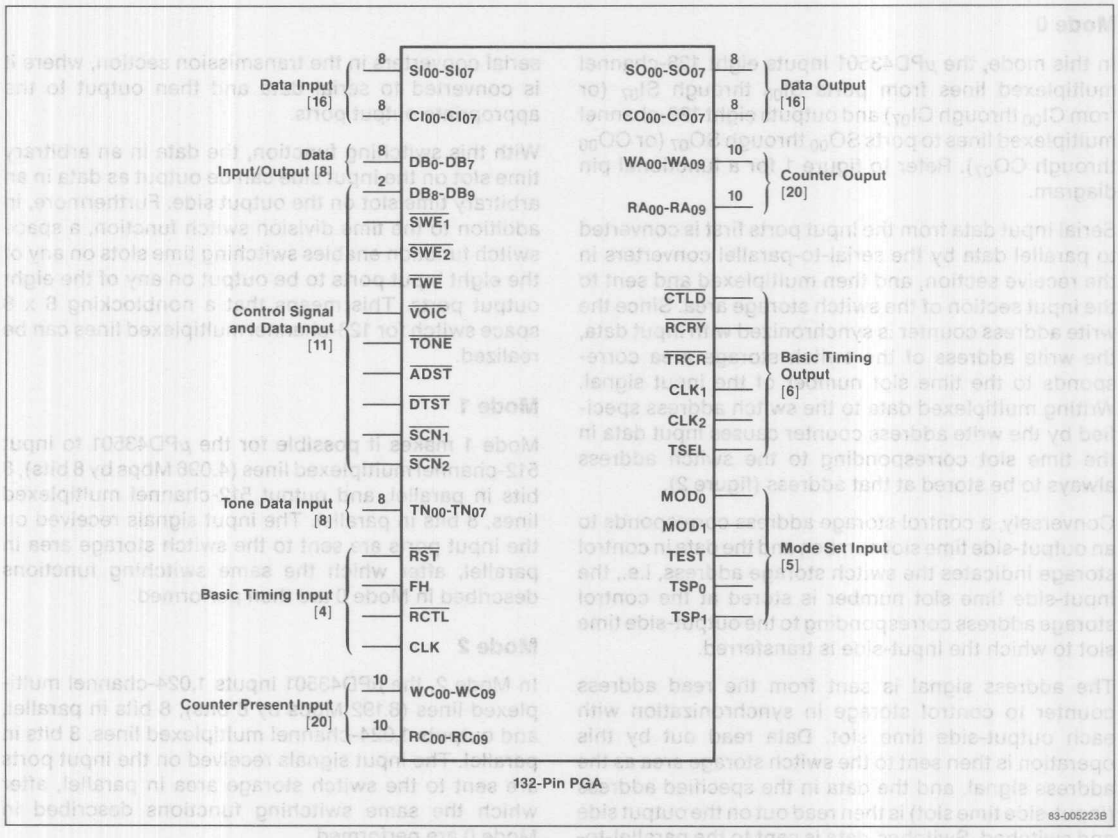
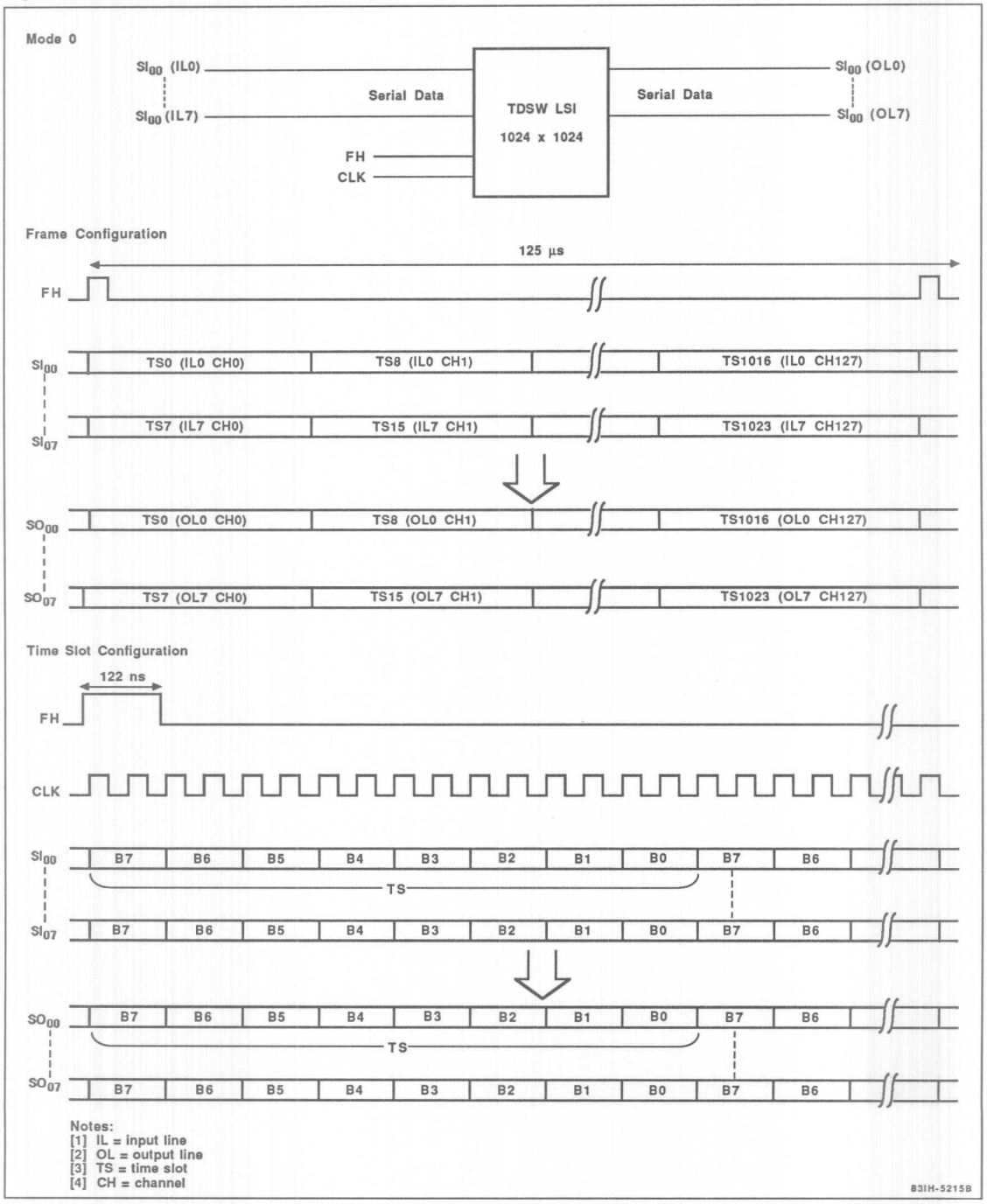
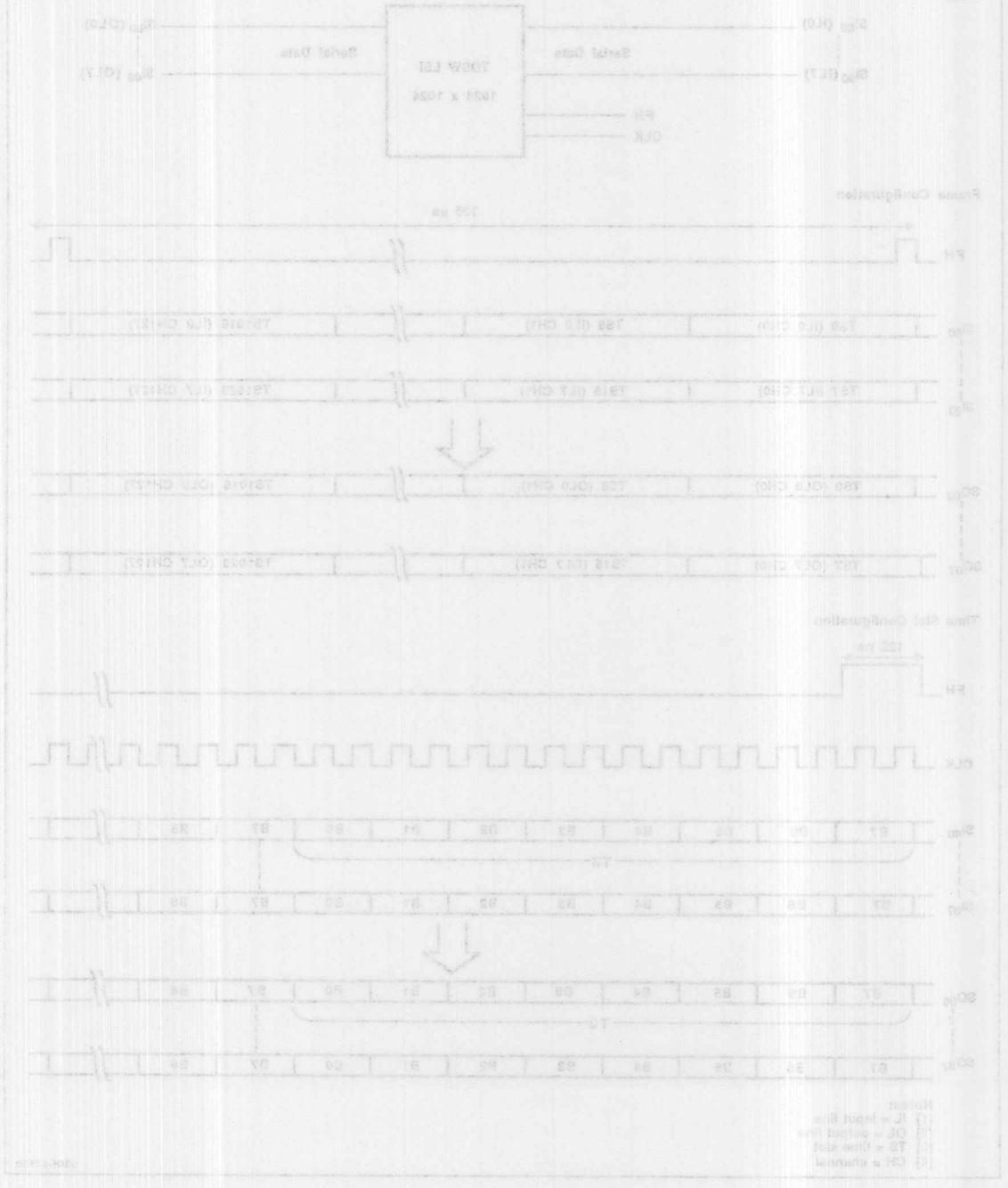


Figure 2. Time Slot Versus Frame Configuration





μPD43608
SINGLE-CHIP CACHE SUBSYSTEM

Description

The μPD43608 is an integrated cache subsystem that provides the microprocessor system designer with a high-performance, single-chip, general-purpose cache solution. The μPD43608 consists of a CPU interface, directory storage (including address tag and validity bit storage), 8K bytes of on-chip data storage, 128 x 6-bit least recently used (LRU) replacement storage, internal address and data paths for cache bypass operations, an asynchronous 32-bit system bus interface, and several features optimizing cache write and miss operations. The μPD43608 is also able to interface with a number of 16- and 32-bit general-purpose microprocessors operating at 16 or 20 MHz.

Features

- ☐ High-performance 16- and 20-MHz operation
- ☐ 16- and 32-bit microprocessor interface capability
- ☐ Integrated cache architecture
  - — 8K bytes of on-chip data storage
  - — 16-byte cache block size
  - — 4-way set associative placement algorithm
- ☐ Bus monitoring circuit
- ☐ LRU replacement algorithm
- ☐ Prefetch on miss—one block lookahead
- ☐ Fetch bypass and wraparound load
- ☐ Asynchronous 32-bit system bus interface
- ☐ Multichip configuration increases cache size
- ☐ Write-through storage update policy with one-level write buffer
- ☐ 132-pin ceramic pin grid array packaging
- ☐ CMOS circuit technology

Ordering Information

Part Number	Ready Output Time (max)	Cycle Time (min)	Package
μPD43608R-2	70 ns	125 ns	132-pin ceramic pin grid array
R-3	50 ns	100 ns	

Organization

The μPD43608 is organized as a 4-way set associative cache, with 8K bytes of on-chip data storage organized as 128 sets by four 16-byte data blocks. When the CPU executes a read cycle, the address tag field of the physical CPU address is compared to the address tag in the cache directory. If a hit occurs, the selected data is sent to the CPU. Otherwise, the μPD43608 initiates a miss cycle to access main storage and update the cache with the replacement block. This architecture ensures a high hit ratio of 95% in most microprocessor applications.

Optimizing the Miss Cycle

The hit rate is an important parameter for measuring performance. Since a high hit rate of 95% requires that the μPD43608 access the main storage array for 5% of all read cycles, the penalty in system performance incurred during a miss cycle may be significant. The μPD43608 provides a number of on-chip features that optimize system performance during a miss cycle.

Data Transfer Cycles

The μPD43608 cache subsystem provides two data transfer modes for accessing main storage during a miss cycle: (1) burst data transfer mode uses the nibble access feature of a DRAM in main storage to optimize system bus bandwidth; (2) in single data transfer mode, an address is transmitted with each read cycle to main storage for systems that don't use nibble access DRAMs.

Block Load and Fetch Bypass Buffers

Once the replacement block has been read from main storage, the block load buffer is used to reduce the replacement block transfer time by providing a temporary buffer for storing the replacement block while the cache data storage is being updated.

Contact your NEC sales representative for a copy of the complete data sheet.

Concurrently, the CPU throughput is optimized by loading the missed word into the fetch bypass buffer as soon as it is read from main storage. The CPU directly accesses the fetch bypass buffer and can fetch the missed word without having to wait for the replacement block to be stored in cache data storage. If the CPU attempts to read the next word in the replacement block, the cache searches the directory and the block load buffer to determine whether or not a hit has occurred. Once the entire replacement block is loaded into the block load buffer, the data is wraparound-loaded into cache data storage.

Prefetch on Miss

On cache miss cycles, the μPD43608 implements a one-block lookahead algorithm that prefetches the next sequential cache data block, thus increasing the cache hit rate. Although prefetching can improve cache performance, a check must be made to determine that the block is not currently stored in the cache. The μPD43608 performs this check during each prefetch cycle, searching the cache directory for the desired prefetch block. If a hit occurs, the prefetch logic aborts the cycle. This function, which ensures that the cache is not polluted with duplicate data, can be enabled or disabled by controlling the cache status code signals during each read cycle.

Replacement Algorithm

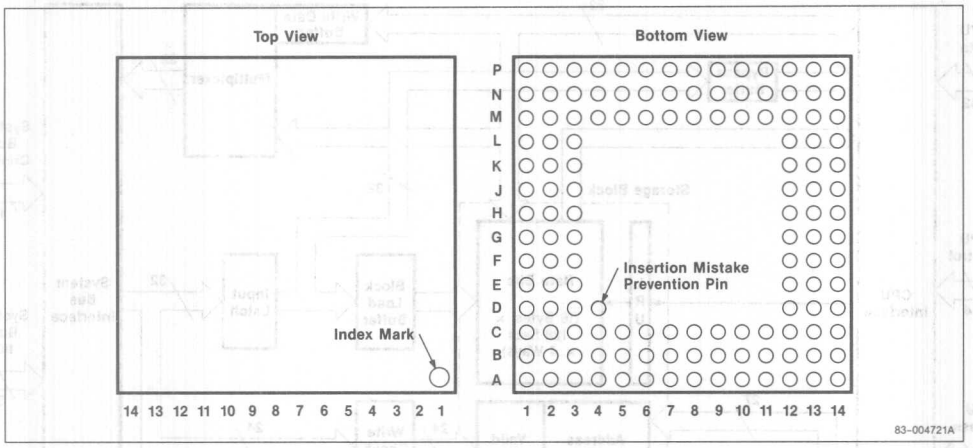
The μPD43608 uses a least recently used (LRU) replacement algorithm to determine which data block should be overwritten during a cache miss cycle. This algorithm improves cache performance by choosing the data block with the least usage to optimize the hit rate.

Main Storage Update Policies

To maintain data consistency in the storage hierarchy during each cache write cycle, the μPD43608 uses a write-through method that updates the main storage as soon as the CPU writes data to cache storage. CPU throughput is optimized by means of a one-level write buffer, which temporarily stores write data and initiates the write cycle to main storage, allowing the CPU to concurrently execute the next instruction.

Pin Configuration

132-Pin Ceramic Pin Grid Array



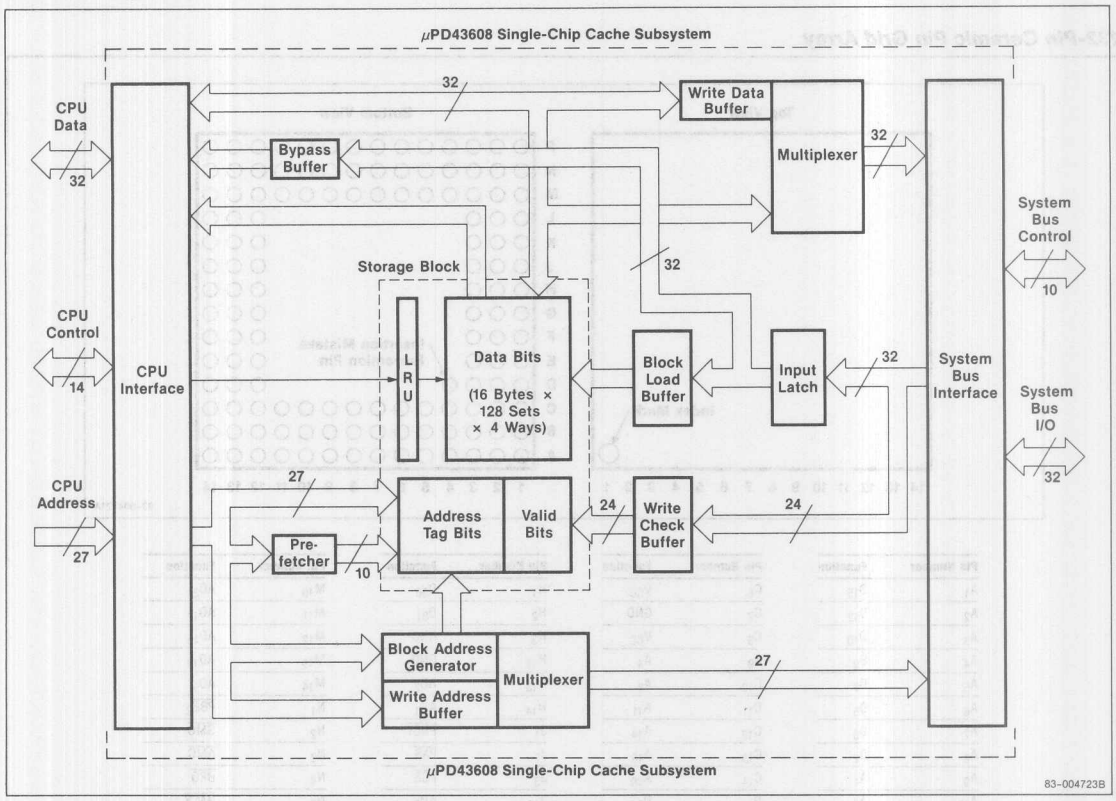
Pin Number	Function
A_1	D_{15}
A_2	D_{12}
A_3	D_{10}
A_4	D_9
A_5	D_7
A_6	D_5
A_7	D_3
A_8	D_2
A_9	A_1
A_{10}	A_2
A_{11}	A_5
A_{12}	A_7
A_{13}	A_{10}
A_{14}	A_{12}
B_1	D_{20}
B_2	D_{17}
B_3	D_{13}
B_4	D_{11}
B_5	D_8
B_6	D_6
B_7	D_4
B_8	D_1
B_9	D_0
B_{10}	A_3
B_{11}	A_6
B_{12}	A_9
B_{13}	A_{13}
B_{14}	A_{17}
C_1	D_{22}
C_2	D_{19}
C_3	D_{16}
C_4	D_{14}
C_5	GND

Pin Number	Function
C_6	V_{CC}
C_7	GND
C_8	V_{CC}
C_9	A_4
C_{10}	A_8
C_{11}	A_{11}
C_{12}	A_{14}
C_{13}	A_{16}
C_{14}	A_{20}
D_1	D_{24}
D_2	D_{21}
D_3	D_{18}
D_{12}	A_{15}
D_{13}	A_{19}
D_{14}	A_{21}
E_1	D_{25}
E_2	D_{23}
E_3	V_{CC}
E_{12}	A_{18}
E_{13}	A_{22}
E_{14}	A_{24}
F_1	D_{27}
F_2	D_{26}
F_3	GND
F_{12}	A_{23}
F_{13}	A_{25}
F_{14}	A_{26}
G_1	D_{29}
G_2	D_{28}
G_3	GND
G_{12}	GND
G_{13}	AD_0
G_{14}	A_{27}

Pin Number	Function
H_1	D_{30}
H_2	D_{31}
H_3	GND
H_{12}	GND
H_{13}	AD_2
H_{14}	AD_1
J_1	$\overline{PRDY}$
J_2	$\overline{PAS}$
J_3	$\overline{PCS}$
J_{12}	AD_7
J_{13}	AD_4
J_{14}	AD_3
K_1	PRD/$\overline{PWT}$
K_2	$\overline{CAEN}$
K_3	ST_2
K_{12}	AD_{11}
K_{13}	AD_6
K_{14}	AD_5
L_1	ST_1
L_2	ST_0
L_3	$\overline{PBE_0}$
L_{12}	AD_{14}
L_{13}	AD_{10}
L_{14}	AD_8
M_1	$\overline{PBE_3}$
M_2	$\overline{PBE_1}$
M_3	PCLK
M_4	$\overline{RST}$
M_5	BCLK
M_6	$\overline{MDS}$
M_7	V_{CC}
M_8	GND
M_9	V_{CC}

Pin Number	Function
M_{10}	AD_{21}
M_{11}	AD_{17}
M_{12}	AD_{15}
M_{13}	AD_{13}
M_{14}	AD_9
N_1	$\overline{PBE_2}$
N_2	$\overline{SMC}$
N_3	$\overline{AMC}$
N_4	$\overline{BRQ}$
N_5	$\overline{BACK}$
N_6	$\overline{MBE_2}$/$\overline{WAIT}$
N_7	AD_{31}
N_8	AD_{29}
N_9	AD_{27}
N_{10}	AD_{24}
N_{11}	AD_{22}
N_{12}	AD_{19}
N_{13}	AD_{16}
N_{14}	AD_{12}
P_1	$\overline{ERR}$
P_2	$\overline{WBSY}$
P_3	MAS/$\overline{MBS}$
P_4	$\overline{MBE_0}$/$\overline{EOC}$
P_5	$\overline{MBE_1}$/$\overline{UERR}$
P_6	$\overline{MBE_3}$/$\overline{CERR}$
P_7	$\overline{MWA}$
P_8	AD_{30}
P_9	AD_{28}
P_{10}	AD_{26}
P_{11}	AD_{25}
P_{12}	AD_{23}
P_{13}	AD_{20}
P_{14}	AD_{18}

Block Diagram



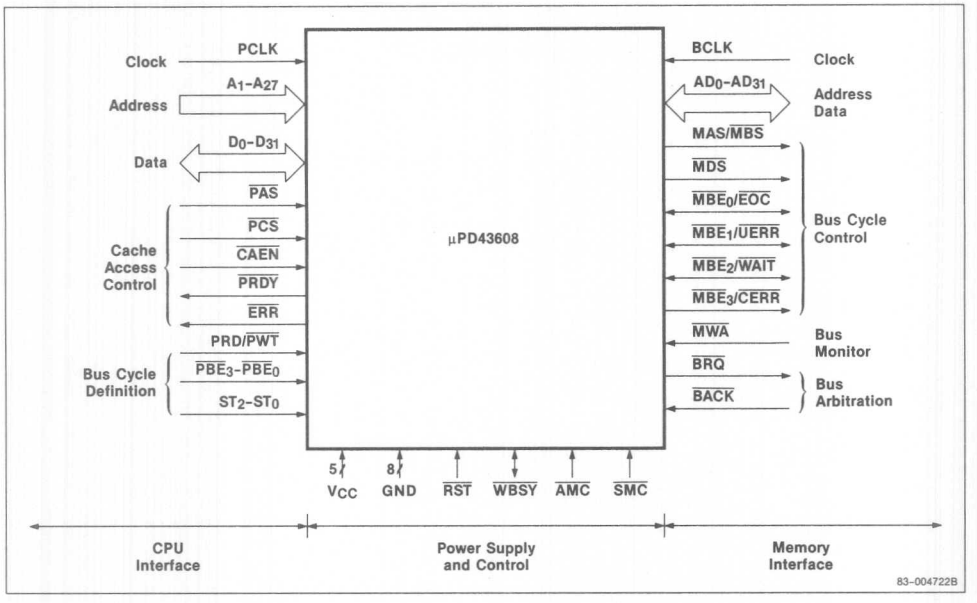
System Bus Interface

The integrated system bus interface provides an interface to contemporary microprocessor system bus architectures. The interface circuit consists of a 32-bit multiplexed address and data bus, asynchronous bus control signals, a bus lock signal, a wait signal, a correctable error function, two data transfer modes—burst and single, and a system bus clock signal. The size of the cache can be increased by connecting additional μPD43608 devices in parallel. A write buffer busy signal is daisy-chained between the parallel devices and automatically controls data transfers in multichip configurations.

Bus Monitoring

In multiprocessor system applications, maintaining data consistency is a major concern. In such a system architecture, an integrated circuit is required to monitor the system bus for any updates to main storage. When a bus master updates a location in its cache storage and writes that change to main storage, all slave processors must invalidate any stale cache data. The monitoring circuit latches all write addresses on the system bus and invalidates any cache data blocks that are not consistent with main storage.

Functional Pin Diagram



Signal Summary

CPU Interface

Signal Name	Input/ Output	Signal Function
PCLK	I	Processor clock
A_1–A_{27}	I	Address bus
D_0–D_{31}	I/O	Data bus
$\overline{PAS}$	I	Address strobe
$\overline{PCS}$	I	Command strobe
$\overline{CAEN}$	I	Cache output enable
PRD/$\overline{PWT}$	I	Read/write
$\overline{PBE_3}$–$\overline{PBE_0}$	I	Byte enable
ST_2–ST_0	I	Status
$\overline{PRDY}$	O	Ready
$\overline{ERR}$	O	Error

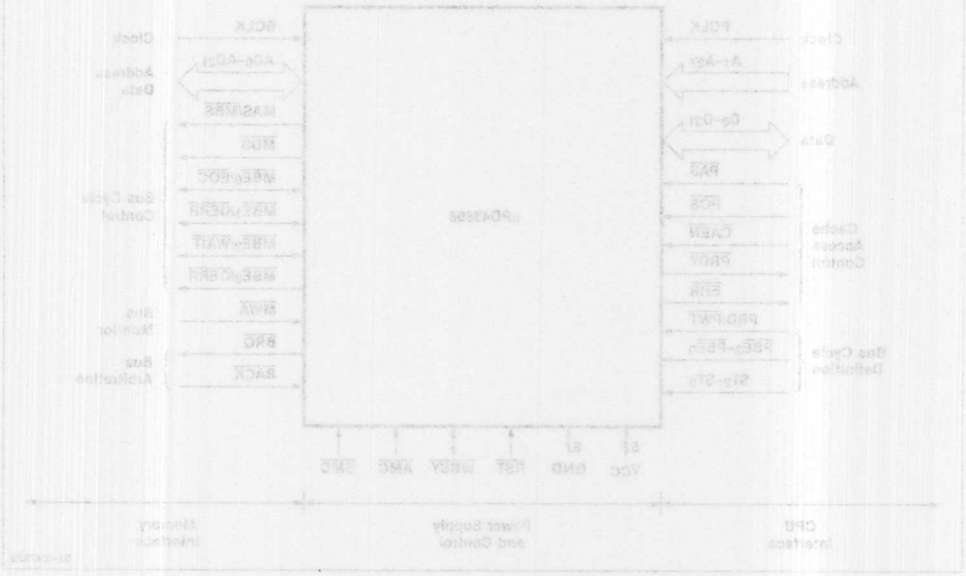
Control

$\overline{RST}$	I	Reset
$\overline{WBSY}$	I/O	Write buffer busy
$\overline{AMC}$	I	Test pin
$\overline{SMC}$	I	Scan path mode

Memory Interface

Signal Name	Input/ Output	Signal Function	
AD_0–AD_{31}	I/O	Address/data bus	
AD_{31} = MEM/$\overline{IO}$	O	Memory/IO	During an address cycle
AD_{30} = MRD/$\overline{MWT}$		Read/write	
AD_{29} = LOCK		Bus lock	
AD_{28} = PRF		Prefetch	
MAS/$\overline{MBS}$	O	Address strobe/bus strobe	
$\overline{MDS}$	O	Data strobe	
$\overline{MBE_0}$/$\overline{EOC}$	O	Byte enable 0/end of cycle	
$\overline{MBE_1}$/$\overline{UERR}$	I/O	Byte enable 1/uncorrectable error	
$\overline{MBE_2}$/$\overline{WAIT}$	I/O	Byte enable 2/wait	
$\overline{MBE_3}$/$\overline{CERR}$	I/O	Byte enable 3/correctable error	
$\overline{MWA}$	I	Main memory write check address	
$\overline{BRQ}$	O	Bus request	
$\overline{BACK}$	I	Bus acknowledge	
BCLK	I	Bus clock	

3



3

μPD71641
Cache Memory Controller

Description

The μPD71641 is an LSI cache controller chip offering advanced features, unequaled flexibility, and built-in reliability to system designers. The μPD71641 makes it practical and economical to use sophisticated caches in microprocessor-based systems.

The implementation of μPD71641 is transparent to the application program. The μPD71641 is configurable from direct-mapped to 4-way set-associative mapping. The μPD71641 allows up to 128K bytes of cache memory. Cache updating is made efficient with sub-block partition and burst mode features.

The μPD71641 can be easily used with many general-purpose, high-performance 32-bit or 16-bit microprocessors. Its architecture is suitable for multiprocessors and multimaster environments. Cache data consistency is ensured by bus monitoring and dual comparator techniques. The μPD71641 uses a write-through strategy to update main memory, which guarantees the best cache consistency in a multiprocessor and multimaster system. External data storage is flexible in size and organization. The μPD71641 will work with any word width.

The μPD71641 is unique in offering features to implement a highly reliable cache memory subsystem. The μPD71641 provides built-in reliability checks, such as address tag parity check, multiple hit detection, and self-diagnosis for directory faults. Upon detection of an erroneous condition, the μPD71641 can either be disabled, or continue to operate in a functionally degraded mode.

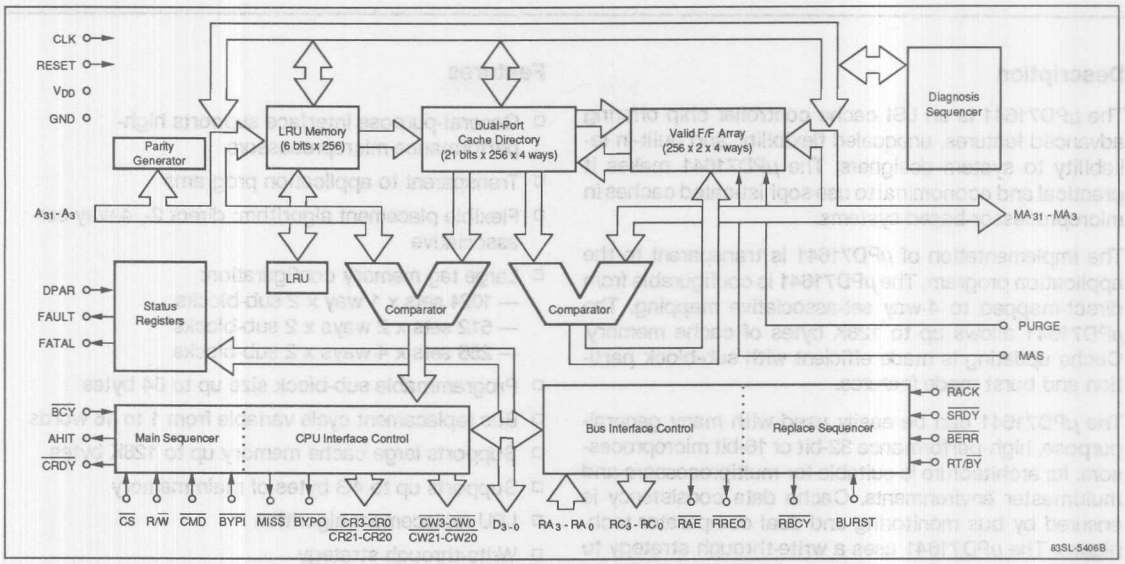
Features

- General-purpose interface supports high-performance microprocessors
- Transparent to application programs
- Flexible placement algorithm: direct 2-, 4-way set-associative
- Large tag memory configuration:
  - 1024 sets x 1 way x 2 sub-blocks
  - 512 sets x 2 ways x 2 sub-blocks
  - 256 sets x 4 ways x 2 sub-blocks
- Programmable sub-block size up to 64 bytes
- Bus replacement cycle variable from 1 to 16 words
- Supports large cache memory up to 128K bytes
- Supports up to 4G bytes of main memory
- LRU replacement algorithm
- Write-through strategy
- Data consistency check by bus monitoring
- External PURGE input to flush tag store
- Increased reliability through internal error detection
  - Parity check on tag store
  - Incorrect match check
  - Multiple hit check
  - LRU output check
- Unique level degradation feature to maximize cache system up time
- 16- and 20-MHz operation
- 132-pin PGA package

Ordering Information

Part Number	Max Clockout Frequency	Package
μPD71641R	20 MHz	132-pin Ceramic PGA

Block Diagram



Description

The μPD72120 Advanced Graphics Display Controller (AGDC) displays characters and graphics on a raster scan device from commands and parameters received from a host processor or CPU. Features of the AGDC include high-speed graphics drawing capabilities, video timing signal generation, large capacity display memory control (including video RAMs), and a versatile CPU interface. These features allow the AGDC to control graphics drawing and display of bit-mapped systems.

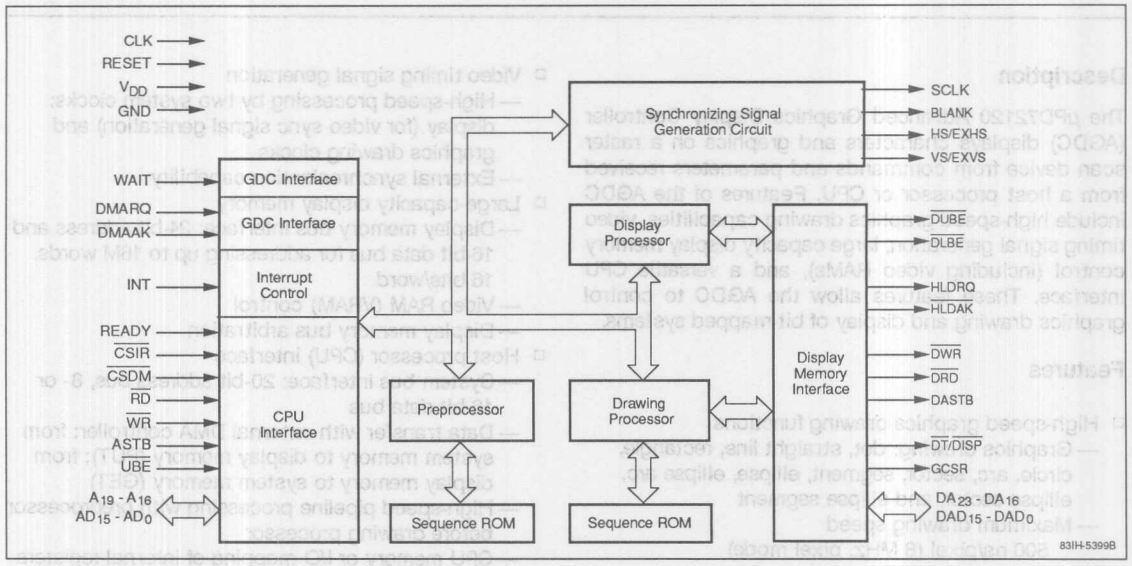
Features

- High-speed graphics drawing functions
  - Graphics drawing: dot, straight line, rectangle, circle, arc, sector, segment, ellipse, ellipse arc, ellipse sector, and ellipse segment
  - Maximum drawing speed
    500 ns/pixel (8 MHz, pixel mode)
    500 ns/dot (8 MHz, plane mode)
  - Area filling (high-speed processing in word units): triangle, trapezoid, circle, ellipse, and rectangle
  - Painting: filling of any arbitrary enclosed area (bit boundary retrieval)
  - Data transfers in display memory: multiplane transfers; data transformation (90°/180°/270° rotation and reversal); multiwindow transfers; maximum transfer speed of 500 ns/word
  - Image processing: slant, arbitrary angle rotation, 16/N enlargement, and N/16 shrinkage (N any integer from 1 to16)
  - Position specification by X-Y coordinates
  - Logical operations between planes
- Video timing signal generation
  - High-speed processing by two system clocks: display (for video sync signal generation) and graphics drawing clocks
  - External synchronization capability
- Large-capacity display memory
  - Display memory bus interface: 24-bit address and 16-bit data bus for addressing up to 16M words, 16 bits/word
  - Video RAM (VRAM) control
  - Display memory bus arbitration
- Host processor (CPU) interface
  - System bus interface: 20-bit address bus, 8- or 16-bit data bus
  - Data transfer with external DMA controller: from system memory to display memory (PUT); from display memory to system memory (GET)
  - High-speed pipeline processing with preprocessor before drawing processor
  - CPU memory or I/O mapping of internal registers and display memory for efficient system interface
- 8-MHz system clock
- CMOS technology
- Single + 5-volt power supply
- Packages: 84-pin PLCC, 94-pin plastic miniflat

Ordering Information

Part No	Package
μPD72120L	84-pin PLCC
μPD72120GJ-5BG	94-pin plastic miniflat

Block Diagram



NEC Electronics Inc.

μPD72123
Advanced Graphics Display Controller II

Description

The μPD72123 Advanced Graphics Display Controller II (AGDC II) is an enhanced version of the μPD72120 AGDC. It executes bit map graphics processing at high speed as a peripheral to a host CPU, reducing the host's workload and improving processing efficiency.

Features

- Compatible with μPD72120 AGDC
- Higher speed drawing
  - 10-MHz drawing clock
- Large command set
  - Line drawing with graphics pen
  - Painting arbitrary or defined areas with tiling patterns
  - Enlarge, shrink, and arbitrary-angle rotate copy commands
  - Data transfer between system and display memory
- Flexible system configurations
  - Drawing can be performed on display or system memory space
  - Data bus can be used with most microprocessors
  - Independent drawing and display clocks
  - VRAM control
  - Laser printer interface controls
- Versatile drawing environment
  - Pipelined processing
  - Two X-Y coordinate systems can be defined
  - Conversion between one-dimensional and two-dimensional data arrays
  - Clipping/picking
- Improved painting performance
- Bit search command
- Vertical blank interrupt
- Bit reversal
- Drawing wait/retry timing
- CMOS technology
- Single + 5-volt power supply

Ordering Information

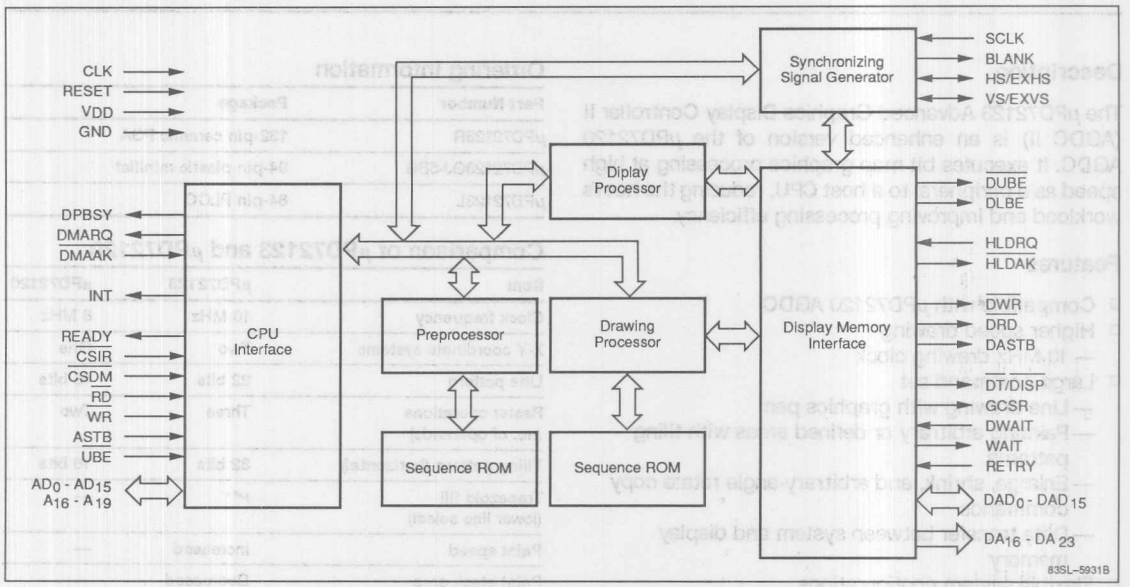
Part Number	Package
μPD72123R	132-pin ceramic PGA
μPD72123GJ-5BG	94-pin plastic miniflat
μPD72123L	84-pin PLCC

Comparison of μPD72123 and μPD72120

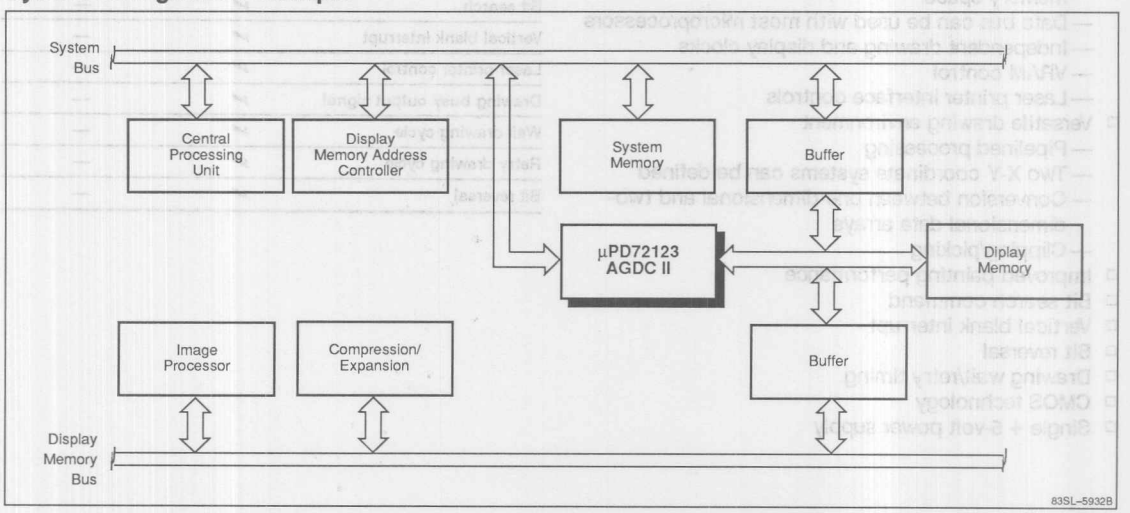
Item	μPD72123	μPD72120
Clock frequency	10 MHz	8 MHz
X-Y coordinate systems	Two	One
Line pattern	32 bits	16 bits
Raster operations (no. of operands)	Three	Two
Tiling pattern (horizontal)	32 bits	16 bits
Trapezoid fill (lower line select)	✓	—
Paint speed	Increased	—
Paint stack area	Decreased	—
Graphics pen	✓	—
Bit search	✓	—
Vertical blank interrupt	✓	—
Laser printer control	✓	—
Drawing busy output signal	✓	—
Wait drawing cycle	✓	—
Retry drawing cycle	✓	—
Bit reversal	✓	—

3

μPD72123 Block Diagram



System Configuration Example



μPD72185
Advanced Compression/ Expansion Engine

Description

The μPD72185 Advanced Compression/Expansion Engine (ACEE) is a dedicated high-speed processor that performs binary image data compression and expansion using CCITT Group 3 and Group 4 algorithms. The μPD72185 supports all the coding methods specified in the CCITT T.4 and T.6 recommendations.

The μPD72185 ACEE operates on 8- or 16-bit-wide data residing in memory. It can compress image data into reduced codes and also expand reduced codes into an image. Compressed codes can be transferred to or from a separate processor or parallel peripheral through an I/O port.

The μPD72185 has a high-performance, four-stage pipelined architecture. It has separate host CPU and image data buses for maximum data throughput. The on-chip DMA controller manages all data transfer on the image bus.

The μPD72185 is designed for high-performance image compression applications, such as facsimile machines, PC FAX boards, scanners, printers, image workstations, electronic document storage systems, and magnetic and optical disk based electronic filing systems.

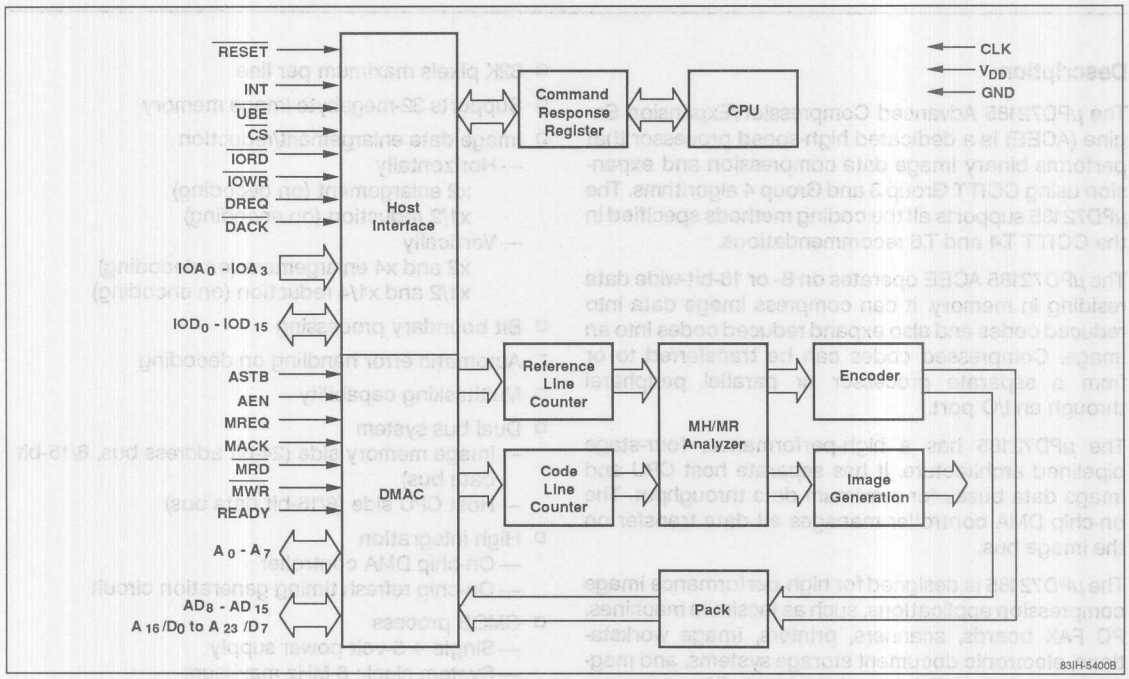
Features

- High-speed processing
  - — Compression/expansion of CCITT standard test chart (A4 size, 400 PPI x 400 LPI) in under 1 second
    Internal four-stage pipelined CPU
- Handles a variety of encoding/decoding methods: CCITT standard MH, MR, and MMR
- 32K pixels maximum per line
- Supports 32-megabyte image memory
- Image data enlargement/reduction
  - — Horizontally
    x2 enlargement (on decoding)
    x1/2 reduction (on encoding)
  - — Vertically
    x2 and x4 enlargement (on decoding)
    x1/2 and x1/4 reduction (on encoding)
- Bit boundary processing
- Automatic error handling on decoding
- Multitasking capability
- Dual bus system
  - — Image memory side (24-bit address bus, 8/16-bit data bus)
  - — Host CPU side (8/16-bit data bus)
- High integration
  - — On-chip DMA controller
  - — On-chip refresh timing generation circuit
- CMOS process
  - — Single + 5-volt power supply
  - — System clock: 8 MHz maximum

Ordering Information

Part No.	Package
μPD72185CW	64-pin plastic shrink DIP (750 mil)
μPD72185L	68-pin PLCC (plastic leaded chip carrier)

Block Diagram



μPD7220A
High-Performance Graphics Display Controller

Description

The μPD7220A high-performance graphics display controller (HGDC) is an intelligent microprocessor peripheral designed to be the heart of a high-performance raster scan computer graphics and character display system. Positioned between the video display memory and the microprocessor bus, the HGDC performs the tasks needed to generate the raster display and manage the display memory. Processor software overhead is minimized by the HGDC's sophisticated instruction set, graphics figure drawing, and DMA transfer capabilities. The display memory supported by the HGDC can be configured in any number of formats and sizes up to 256K 16-bit words. The display can be zoomed and panned, while partitioned screen areas can be independently scrolled. With its light pen input and multiple controller capability, the HGDC is ideal for advanced computer graphics applications.

For a more detailed description of the HGDC's operation, please refer to the 7220/7220A design manuals.

System Considerations

The HGDC is designed to work with a general purpose microprocessor to implement a high-performance computer graphics system. Through the division of labor established by the HGDC's design, each of the system components is used to the maximum extent through a six-level hierarchy of simultaneous tasks. At the lowest level, the HGDC generates the basic video raster timing, including sync and blanking signals. Partitioning areas on the screen and zooming are also accomplished at this level. At the next level, video display memory is modified during the figure drawing operations and data moves. Third, display memory addresses are calculated pixel by pixel as drawing progresses. Outside the HGDC at the next level, preliminary calculations are done to prepare drawing parameters. At the fifth level, the picture must be represented as a list of graphics figures drawable by the HGDC. Finally, this representation must be manipulated, stored, and communicated. By handling the first three levels, the HGDC takes care of the high-speed and repetitive tasks required to implement a graphics system.

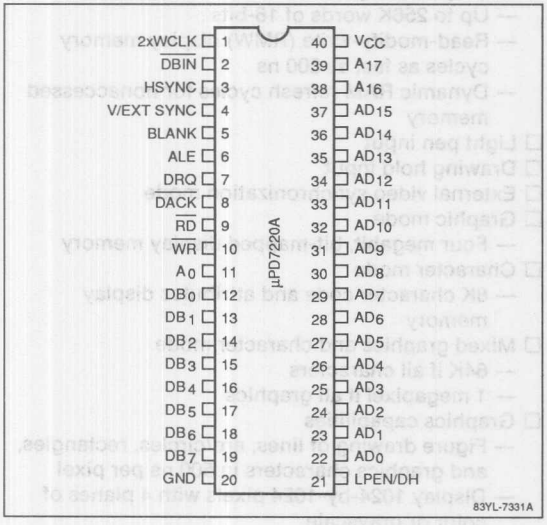
Features

- ☐ Microprocessor interface
  - — DMA transfers with 8257- or 8237-type controllers
  - — FIFO command buffering
- ☐ Display memory interface
  - — Up to 256K words of 16-bits
  - — Read-modify-write (RMW) display memory cycles as fast as 500 ns
  - — Dynamic RAM refresh cycles for nonaccessed memory
- ☐ Light pen input
- ☐ Drawing hold input
- ☐ External video synchronization mode
- ☐ Graphic mode
  - — Four megabit, bit-mapped display memory
- ☐ Character mode
  - — 8K character code and attributes display memory
- ☐ Mixed graphics and character mode
  - — 64K if all characters
  - — 1 megapixel if all graphics
- ☐ Graphics capabilities
  - — Figure drawing of lines, arc/circles, rectangles, and graphics characters in 500 ns per pixel
  - — Display 1024-by-1024 pixels with 4 planes of color or grayscale
  - — Two independently scrollable areas
- ☐ Character capabilities
  - — Auto cursor advanced
  - — Four independently scrollable areas
  - — Programmable cursor height
  - — Characters per row: up to 256
  - — Character rows per screen: up to 100
- ☐ Video display format
  - — Zoom magnification factors of 1 to 16
  - — Panning
  - — Command-settable video raster parameters
- ☐ NMOS technology
- ☐ Single +5 V power supply
- ☐ DMA capability
  - — Bytes or word transfers
  - — 4 clock periods per byte transferred
- ☐ On-chip pull-up resistor for VSYNC/EXT, HSYNC and DACK, and a pull-down resistor for LPEN/DH

Ordering Information

Part Number	Package Type	Max Frequency of Operation
μPD7220AD	40-pin ceramic DIP	6 MHz
μPD7220AD-1	40-pin ceramic DIP	7 MHz
μPD7220AD-2	40-pin ceramic DIP	8 MHz

Pin Configuration



Character Mode Pin Utilization

Pin No.	Pin Symbol	Function
35-37	AD_{13}-AD_{15}	Line counter bits 0 to 2 outputs
38	AD_{16}	Line counter bit 3 output
39	AD_{17}	Cursor output and line counter bit 4

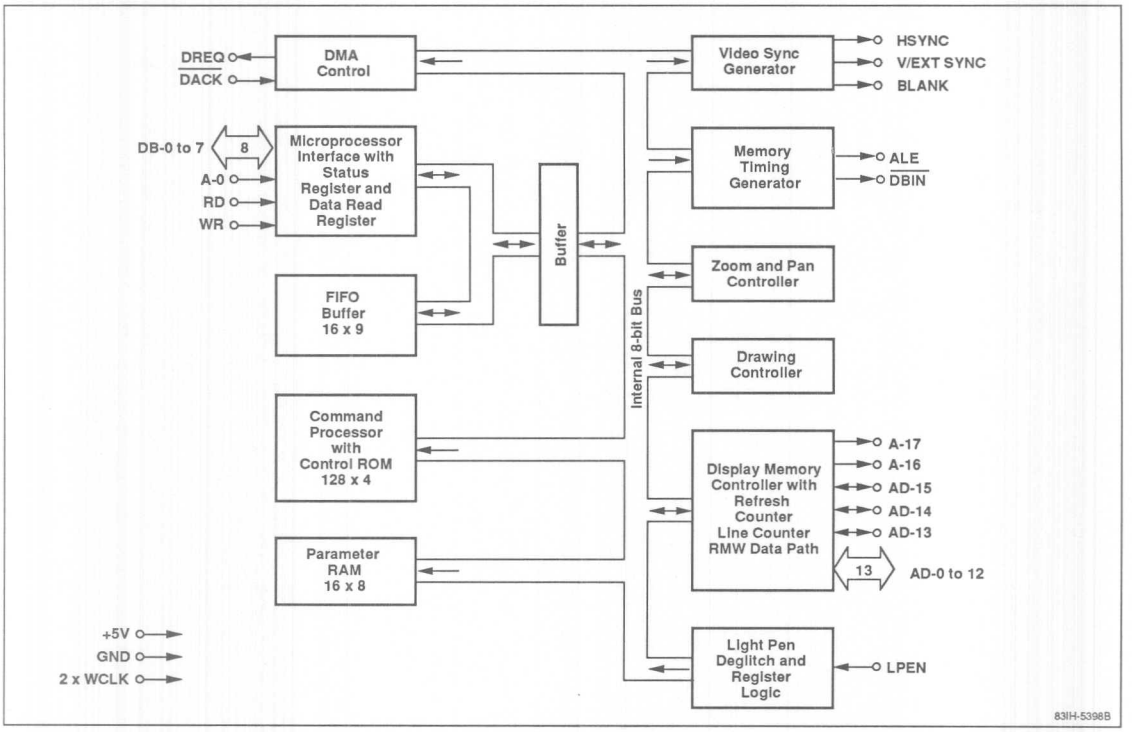
Mixed Mode Pin Utilization

Pin No.	Pin Symbol	Function
35-37	AD_{13}-AD_{15}	Address and data bits 13 to 15
38	A_{16}	Attribute blink and clear line counter output
39	A_{17}	Cursor and bit-map area flag output

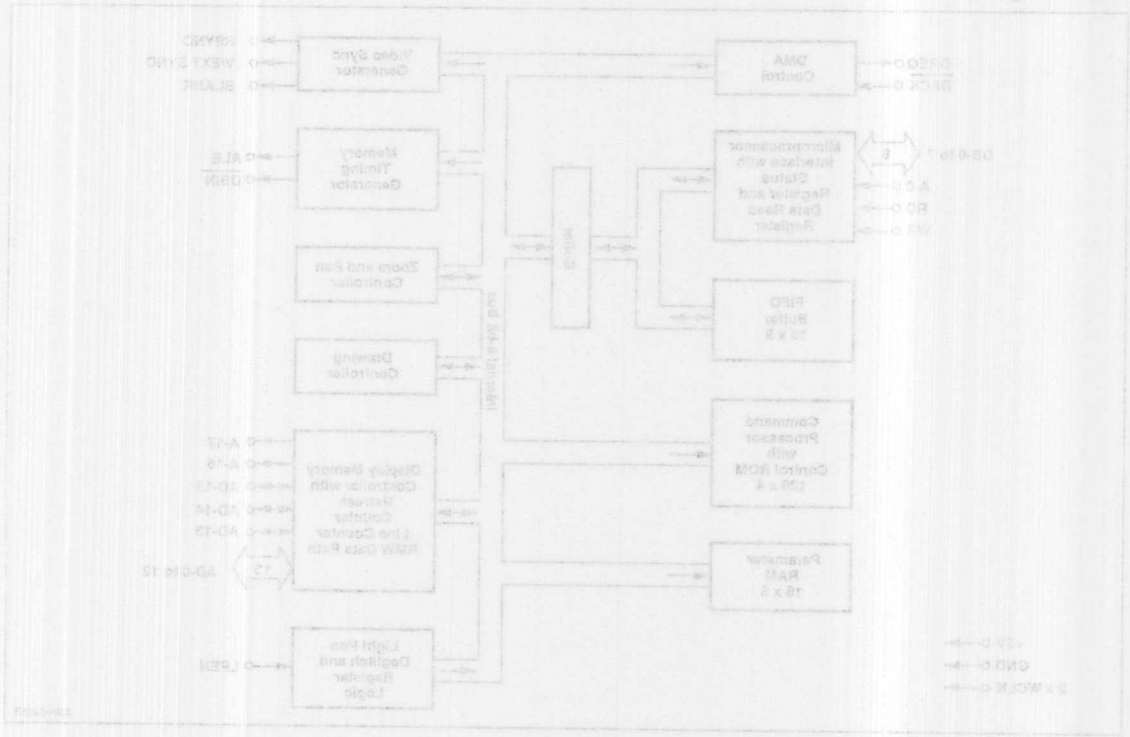
Pin Identification

Pin No.	Pin Symbol	Function
1	2xWCLK	Clock input
2	DBIN	Display memory read input flag
3	HSYNC	Horizontal video sync output
4	V/EXT SYNC	Vertical video sync output or external VSYNC input
5	BLANK	CRT blanking output
6	ALE	Address latch enable output
7	DRQ	DMA request output
8	DACK	DMA acknowledge input
9	RD	Read strobe input for microprocessor interface
10	WR	Write stobe input for microprocessor interface
11	A_0	Address select input for microprocessor interface
12-19	DB_0-DB_7	Bidirectional data bus to host microprocessor
20	GND	Ground
21	LPEN/DH	Light pen detect input drawing hold input
22-34	AD_0-AD_{12}	Address data lines to display memory
35-37	AD_{13}-AD_{15}	Utilization varies with mode of operation
38	A_{16}	Utilization varies with mode of operation
39	A_{17}	Utilization varies with mode of operation
40	V_{CC}	+5 V ±10% power supply

Block Diagram



3



NEC Electronics Inc.

APPLICATION NOTE 54
μPD42505
LINE BUFFER FOR COMMUNICATIONS SYSTEMS

Introduction

The current trend in storage devices is toward larger, faster, better-performing products. There is a complementary trend toward the development of storage devices designed for specific purposes. The video buffer is an example of a dedicated device. Line buffers, field (frame) buffers for TV and broadcast equipment, and graphics buffers for computers are examples of video storage devices. Table 1 shows some of NEC's dedicated video buffers.

Table 1. Video Buffers

Function	Product	Storage Configuration	Serial Cycle Time	Application in Video/Optical Systems
Line buffers	μPD42505	5048 x 8	50 or 75 ns	Line storage in facsimile machines, copiers, and scanners
	μPD41101/μPD42101	910 x 8	34 or 69 ns	Double-speed scan conversion for NTSC TV, luma/chroma separation
	μPD41102/μPD42102	1135 x 8	28 or 56 ns	Double-speed scan conversion for PAL TV, luma/chroma separation
Field buffer	μPD42270	263 x 910 x 4	60 ns	Image field storage
Dual-port graphics buffers	μPD41264	64K x 4/256 x 4	40 or 60 ns	High-speed drawing device
	μPD42274/μPD42273	256K x 4/512 x 4	30 or 40 ns	
Triple-port graphics buffer	μPD42232	32K x 8/256K x 1/128 x 8	40 or 60 ns	High-speed drawing/image processing device
Bidirectional data buffer	μPD42532	32K x 8	100 ns	Data transfer rate conversion

This application note introduces the μPD42505, a high-speed serial access device with the same general interface specifications as those of the μPD41101. The μPD42505 was developed specifically for office automation equipment that handles a large amount of data in each horizontal line, equipment such as G3 and G4 digital facsimile machines, high-performance copiers, and image scanners.

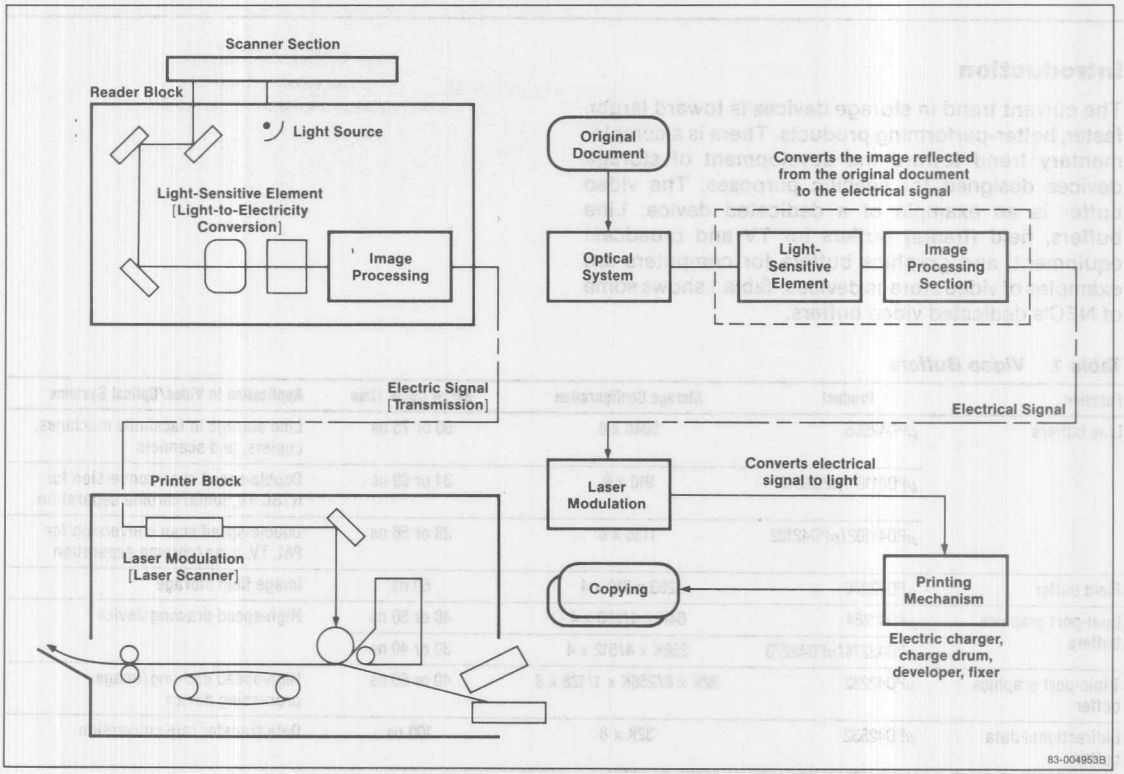
There has been a great deal of technical progress toward higher quality and performance in the development of this image-processing equipment. For example, there are already advances in image quality using two-dimensional filtering, image contraction and expansion, and high-speed video signal transfer. The μPD42505 achieves optimal processing with a storage array of 5048 x 8 bits, and by use of an internal algorithm to read out data in the order in which it was input. The fast cycle time of 50 ns allows the μPD42505 to perform various types of image processing.

Figure 1 shows a typical application for the μPD42505 using a digital copier as an example.

A digital copier mainly consists of a reader and a printer section. The image reflected from the original document placed in the scanner section is input to an image sensor (e.g., a CCD or contact-type image sensor) and photoelectrically converted to a digital signal. The digital signal is then input to the image processing section for image quality improvement and processing. The electronic image signal processed in the reader block is sent to the printer block, converted to light in the laser modulation section, developed, fixed, and printed out. If a communication facility is added to this copier, it can function as a facsimile machine.

Digital copiers and facsimile machines configured in this way can use dedicated video buffers in the image processing or transmission section.

Figure 1. Configuration and Data Flow in a Digital Copier

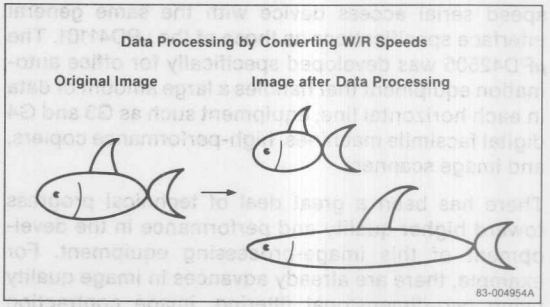


Uses for the μPD42505

The following discussion describes the types of applications for which the μPD42505 was developed: frequency (speed) conversion, a data delay line for one horizontal scanning line, and buffering for data transfer operations in a simple configuration with simple control.

Consider the need for a device that asynchronously converts the read and write speed for frequency conversion, e.g., a serial access device used for image contraction or expansion, with a word length of one to two horizontal lines. The buffer must be written to and read from asynchronously and at different rates. High speed is also a requirement. Figure 2 illustrates a frequency conversion application.

Figure 2. Frequency Conversion



Another application might require a data delay line with a delay length of one to two lines. This type of buffer could be used for image quality improvement in two-dimensional filtering, especially for filtering in the vertical direction, because it could be written to and read from simultaneously in synchronization with a single clock signal. Figure 3 illustrates two-dimensional filtering.

A third application is a buffer for data transfer operations. This application requires a device large enough to store the amount of data handled, with the capability to read and write asynchronously, simultaneously, and at different speeds. An output such as a flag to indicate the amount of data in the storage array might also be required. Figure 4 illustrates buffering for data transfer.

Figure 3. Two-Dimensional Filtering

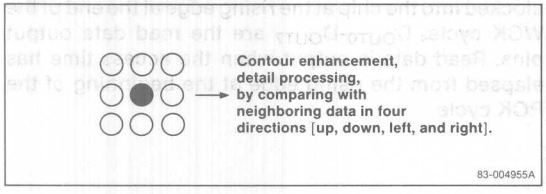
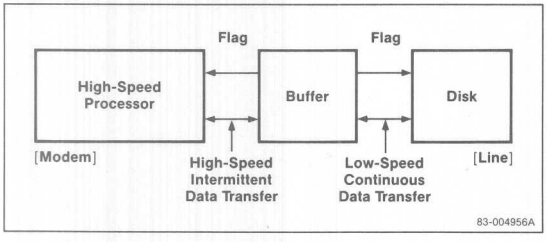


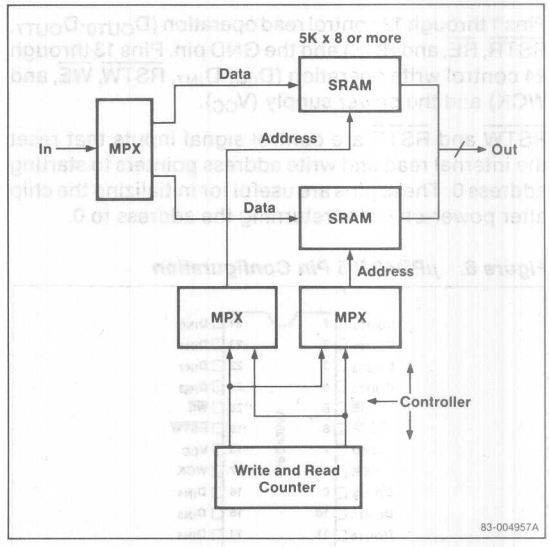
Figure 4. Data Transfer Buffering



These applications typically require a double-buffer configuration using high-speed SRAMs for data storage in bits, as shown in figure 5.

In the first phase, data is written to the first SRAM while data in the second SRAM is read simultaneously, alternating operations between the two SRAMs. However, this operation requires components such as read and write address counters, a multiplexer to switch address signals according to the read and write state of each device, a multiplexer to switch write data input and read data output, and a sophisticated controller to control the SRAMs and the other components. The μPD42505, by performing some of these functions itself, considerably simplifies these applications.

Figure 5. Typical System Using High-Speed SRAMs



Features of the μPD42505

The μPD42505 is a 5048-word x 8-bit high-speed serial access device that uses 1.5-μm CMOS processing and dual-port storage cell circuits allowing simultaneous, asynchronous read and write cycles at different speeds. An internal algorithm makes an external address signal unnecessary.

Read and write operations are fully and independently controlled by their own set of control signals. The storage array length of 5048 words meets the size required to sample one line of JIS A3-size paper on the shorter side (297 mm) with a sampling rate of 16 dots/mm (400 dots/in). On the longer side (418 mm), the sampling rate is 12 dots/mm (300 dots/in). The μPD42505 can easily process document data for each line. The configuration of 8 bits to 1 word corresponds to the number of bits for one sampling point, which allows the device to process natural-looking images.

The μPD42505 can be used in video applications that require high-speed processing because of its minimum simultaneous write/read cycle time of 50 ns and maximum access time of 40 ns. For example, the cycle time of 50 ns is fast enough to digitally process an NTSC or PAL composite video signal at a sampling rate of four times the color subcarrier frequency ($4f_{SC}$).

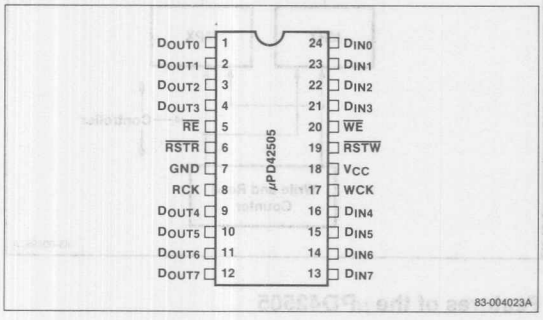
The μPD42505 is particularly suitable for use as a digital delay line with a delay length of up to 5048 cycles in one-cycle steps. The device is mounted in a 300-mil, 24-pin plastic slim DIP. The 300-mil width allows high-density mounting.

μPD42505 Pinout

Pins 1 through 12 control read operation (D_{OUT0}-D_{OUT7}, $\overline{RSTR}$, $\overline{RE}$, and RCK) and the GND pin. Pins 13 through 24 control write operation (D_{IN0}-D_{IN7}, $\overline{RSTW}$, $\overline{WE}$, and WCK) and the power supply (V_{CC}).

$\overline{RSTW}$ and $\overline{RSTR}$ are control signal inputs that reset the internal read and write address pointers to starting address 0. These pins are useful for initializing the chip after power-on or for returning the address to 0.

Figure 6. μPD42505 Pin Configuration



$\overline{WE}$ and $\overline{RE}$ are control signals that enable (low) or disable (high) write and read operation. When $\overline{WE}$ is high, write operation is disabled and the write address stops at the current value. When $\overline{RE}$ is high, read operation is disabled, the read address stops at the current value, and the output goes to high impedance. $\overline{WE}$ and $\overline{RE}$ may be input at any time, but they are latched in each cycle at the rising edge of WCK or RCK, respectively.

WCK and RCK are the write and read system clock inputs. One write or read cycle is executed in synchronization with each WCK or RCK input when $\overline{WE}$ or $\overline{RE}$ is low. The write or read address is incremented internally in single steps and wraps around automatically from 5047 to 0.

D_{IN0}-D_{IN7} are the write data input pins. Write data is clocked into the chip at the rising edge at the end of the WCK cycle. D_{OUT0}-D_{OUT7} are the read data output pins. Read data is output when the access time has elapsed from the rising edge at the beginning of the RCK cycle.

Read and Write Timing

Input a low-level signal to $\overline{RSTW}$ (for writing) or $\overline{RSTR}$ (for reading) to satisfy the setup and hold times measured from the rising edge at the beginning of the WCK or RCK cycle. This returns the cycle to starting address 0. Figure 7 shows read and write timing for the μPD42505.

As the figure shows, the $\overline{RSTW}$ or $\overline{RSTR}$ signal can end in one write or read cycle or can be repeated for successive write or read cycles. Repeating the reset cycle holds the address at 0. The address is incremented to address 1 only in a cycle when $\overline{RSTW}$ or $\overline{RSTR}$ is set high at the rising edge of the WCK (RCK) cycle. For write reset, the write data clocked in the last reset cycle is written to address 0. For read reset, the data in address 0 is output continuously. After the reset, write or read operation continues as the address is incremented by 1 for each cycle in synchronization with its appropriate clock. When the internal address reaches 5,047 (i.e., when write or read cycles are executed 5,048 times), the address returns to address 0 and the write or read operation starts over at that point.

Speed Conversion. Independently controlling the read and write operations of the μPD42505 allows you to perform speed conversion. For example, when the read and write addresses are initialized by $\overline{RSTW}$ and $\overline{RSTR}$, data is written in synchronization with WCK and the write data is written to the chip from device address 0. Data written can be read out from address 0. In this case, the reset signal input timing and the clock signal speed (cycle time) can be independently controlled for read and write operation. The μPD42505 can be used for speed (frequency or time axis) conversion by outputting the data previously input with an arbitrary drive frequency and time at a different drive frequency and time.

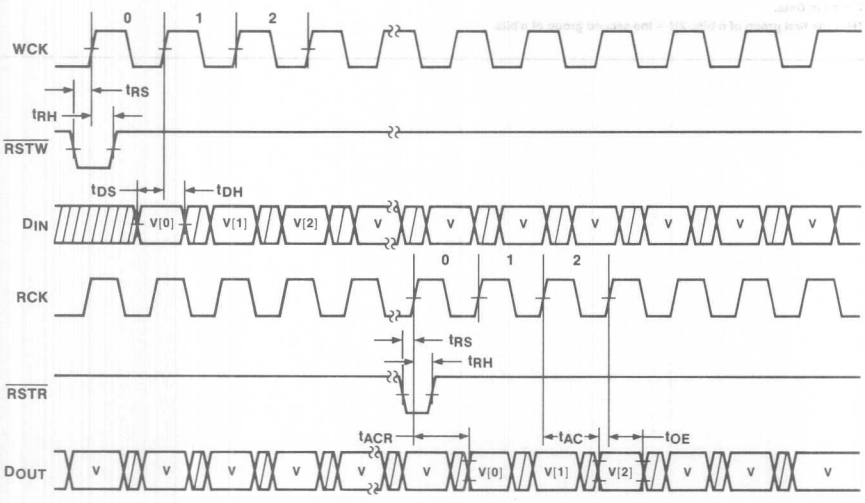
Digital Delay Line. To use the μPD42505 as a digital delay line, input the same clock to WCK and RCK and reset the read and write cycles in parallel. Written data is read out after 5,048 cycles to provide a 5,048-cycle digital delay line.

There are three ways to control the delay length:

- By controlling the $\overline{WE}$ and $\overline{RE}$ signals
- By inputting $\overline{RSTW}$ and $\overline{RSTR}$ at different times (the delay length is determined by the offset between the signals)
- By changing the reset signal interval when $\overline{RSTW}$ and $\overline{RSTR}$ are concurrently controlled (the delay length is determined by the reset signal input interval)

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Figure 7. Read and Write Timing



Notes:
[1] $\overline{WE} = \overline{RE} = V_{IL}$.
[2] V = Valid data.

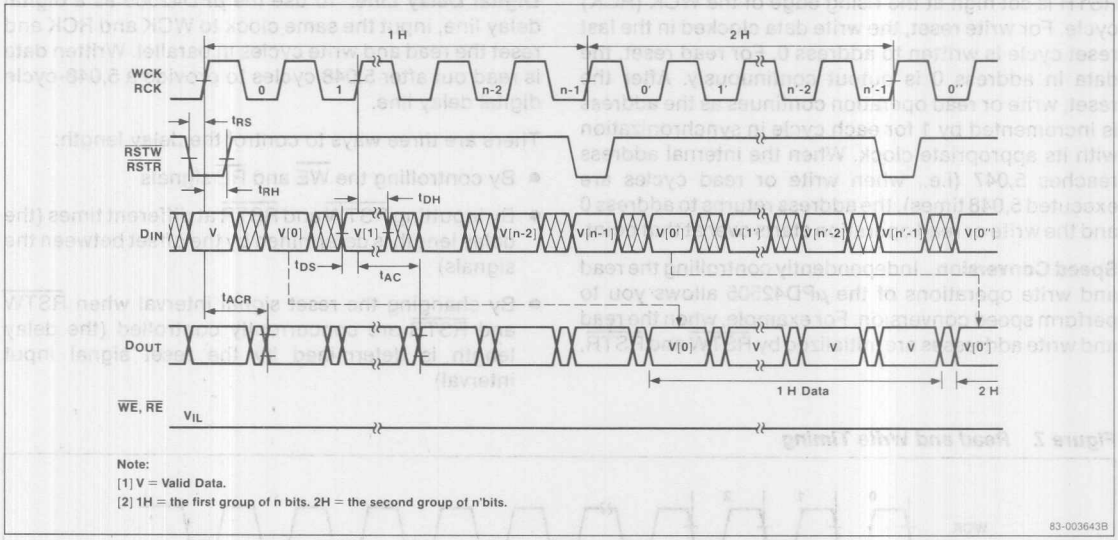
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The delay length can be changed in one-cycle steps by controlling $\overline{WE}$ and $\overline{RE}$. When $\overline{WE}$ and $\overline{RE}$ are high, write and read operation is disabled. The write and read addresses remain where they were when the operations were disabled, regardless of WCK and RCK.

When $\overline{RSTW}$ and $\overline{RSTR}$ are used to control the delay length, the data written at address 0 when $\overline{RSTW}$ is input is read out from address 0 when $\overline{RSTR}$ is next input. The offset between $\overline{RSTW}$ and $\overline{RSTR}$ determines the delay length.

In the third method, changing the reset signal input interval, the same signal is used for WCK and RCK so that $\overline{RSTW}$ and $\overline{RSTR}$ are controlled together. The data, written after a reset signal, is read out after the next reset signal in the order it was written. This interval determines the delay length. For example, if the reset signal is input every 4,800 cycles, the delay length is 4,800 cycles. Figure 8 shows the timing for this method.

Figure 8. Controlling Delay Length with the Reset Interval



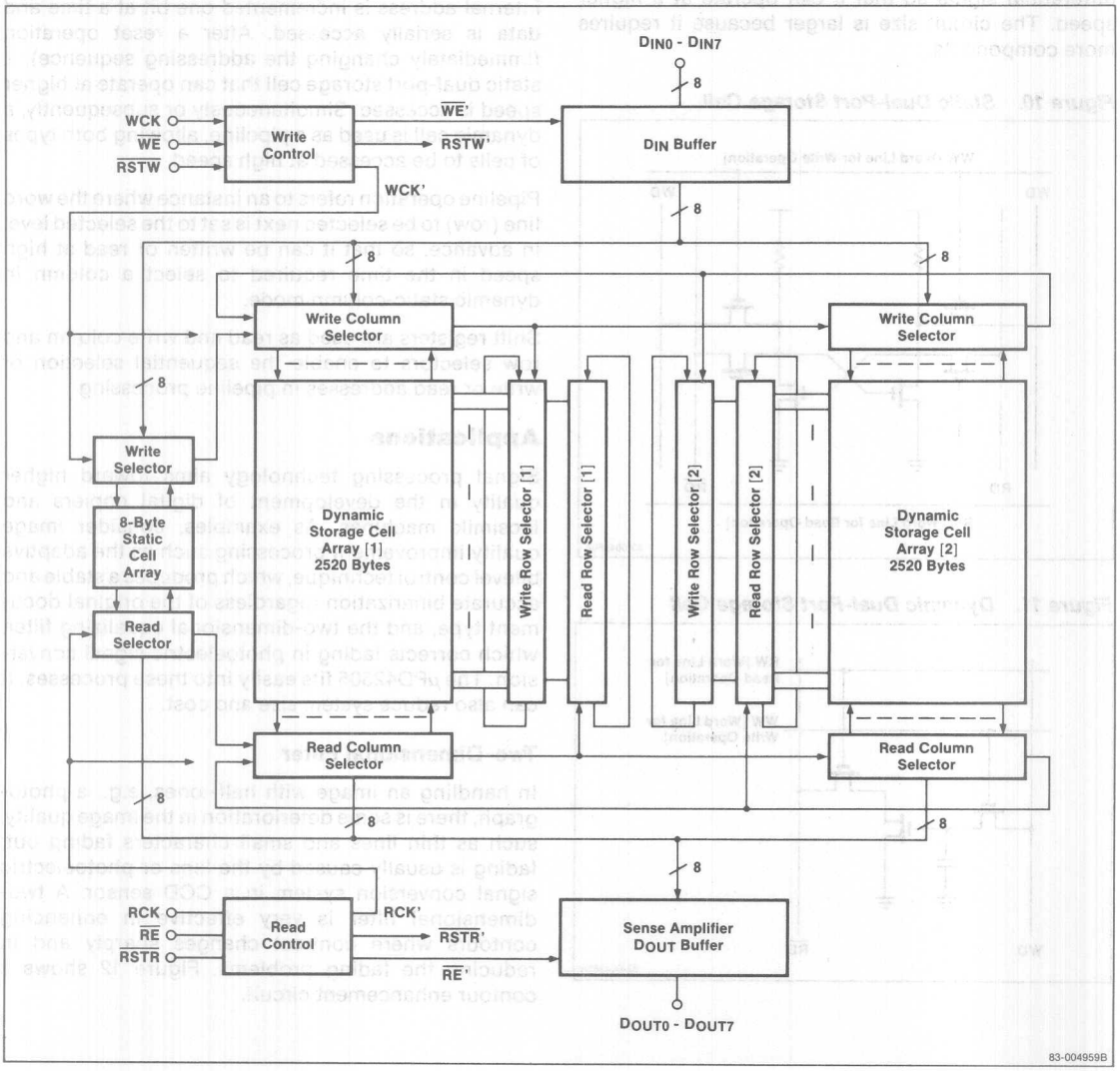
Note:
[1] V = Valid Data.
[2] 1H = the first group of n bits. 2H = the second group of n'bits.

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Functional Blocks

The write data input from pins D_{IN0}-D_{IN7} goes through the D_{IN} buffer and is serially written to either a static cell in an 8-byte configuration, or a dynamic cell in a 5,040-byte configuration, one byte (8 bits) at a time, in synchronization with WCK. The data read out from these cells is serially output from the D_{OUT} pins through the sense amplifier and the D_{OUT} buffer, one byte at a time, in synchronization with RCK. The read and write control circuits control these operations.

Figure 9. μPD42505 Block Diagram



Storage Cells

The μPD42505 uses dual-port storage cells to allow read and write cycles to be executed asynchronously and at different speeds. Figure 10 shows a circuit diagram of a static dual-port storage cell, and figure 11 shows a dynamic dual-port storage cell.

In the static cell, read and write data are input as a differential signal so that it can operate at a higher speed. The circuit size is larger because it requires more components.

Figure 10. Static Dual-Port Storage Cell

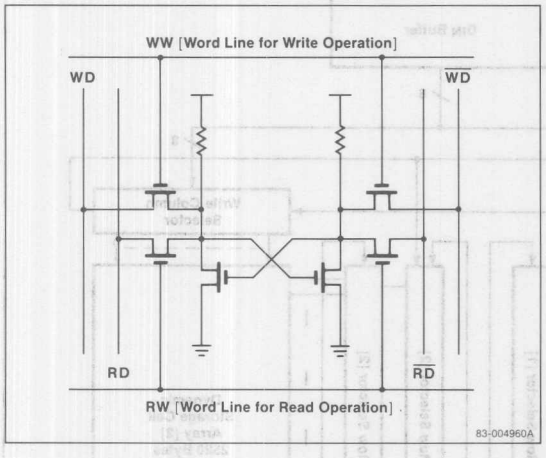
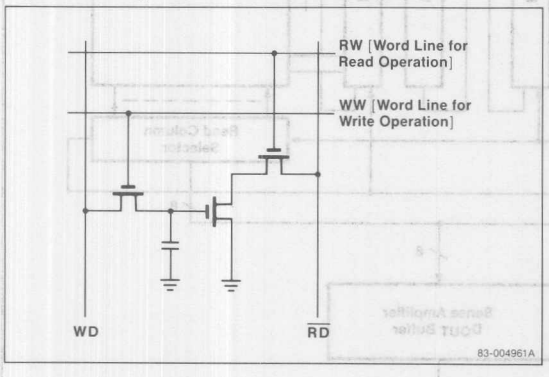


Figure 11. Dynamic Dual-Port Storage Cell



The dynamic cell has only one bit line for read operation and one for write operation. It requires a longer data sense phase, reducing the speed. However, it can be configured with fewer components.

Both types of cells are used in the μPD42505 to exploit the advantages of each. Other than initializing the internal address pointer to the starting address with the reset signal, the μPD42505 is configured so that the internal address is incremented one bit at a time and data is serially accessed. After a reset operation (immediately changing the addressing sequence), a static dual-port storage cell that can operate at higher speed is accessed. Simultaneously or subsequently, a dynamic cell is used as a pipeline, allowing both types of cells to be accessed at high speed.

Pipeline operation refers to an instance where the word line (row) to be selected next is set to the selected level in advance, so that it can be written or read at high speed in the time required to select a column in dynamic static-column mode.

Shift registers are used as read and write column and row selectors to enable the sequential selection of write or read addresses in pipeline processing.

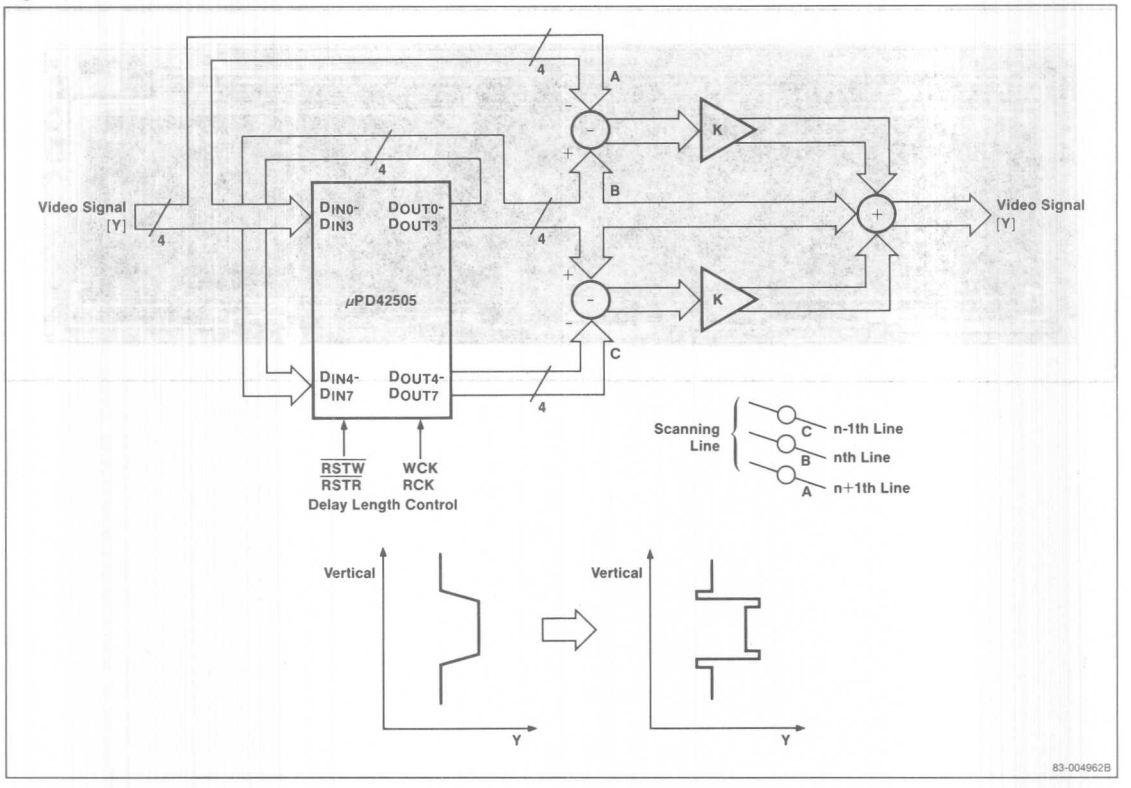
Applications

Signal processing technology aims toward higher quality in the development of digital copiers and facsimile machines. As examples, consider image quality improvement processing such as the adaptive bilevel control technique, which produces a stable and accurate binarization regardless of the original document type, and the two-dimensional equalizing filter, which corrects fading in photoelectric signal conversion. The μPD42505 fits easily into these processes. It can also reduce system size and cost.

Two-Dimensional Filter

In handling an image with half-tones, e.g., a photograph, there is some deterioration in the image quality, such as thin lines and small characters fading out; fading is usually caused by the lens or photoelectric signal conversion system in a CCD sensor. A two-dimensional filter is very effective in enhancing contours where contrast changes sharply and in reducing the fading problems. Figure 12 shows a contour enhancement circuit.

Figure 12. Contour Enhancement Circuit

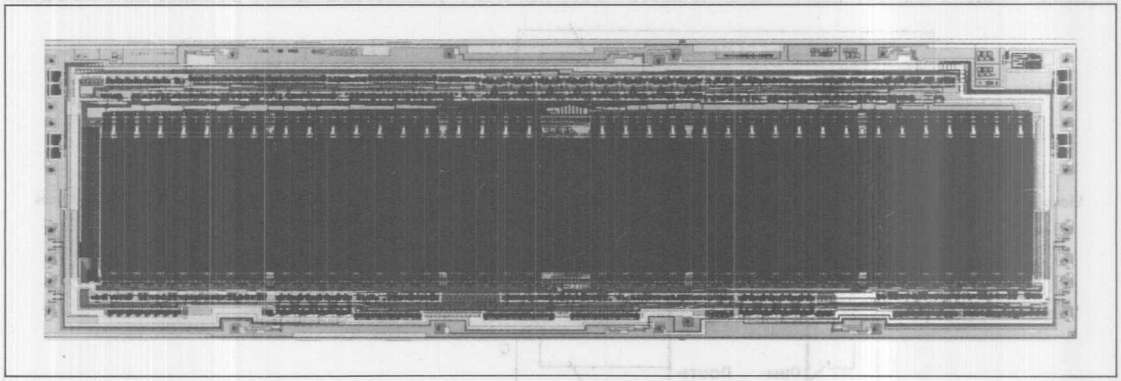


In this example, the video input is handled as a 4-bit signal so that a circuit with a delay length equal to two scanning lines can be configured with a single μPD42505. Adding adders or subtractors and multipliers to the μPD42505 completes the contour enhancement configuration.

The video signal of the n+1th line (delayed by one scanning line) is input to D_{IN0}-D_{IN3} and output from D_{OUT0}-D_{OUT3} as the nth line. Applying this output directly to D_{IN4}-D_{IN7} delays the video signal another scanning line before it is output from D_{OUT4}-D_{OUT7} as the n−1th line. There is a delay of one scanning line between the signal input to D_{IN0}-D_{IN3} and the signal output from D_{OUT0}-D_{OUT3}, and a delay of another scanning line between the signal input to D_{IN4}-D_{IN7} and the signal output from D_{OUT4}-D_{OUT7}. Processing these signals in the adders and multipliers provides contour enhancement in the vertical direction. You can control the delay length by controlling the reset signals ($\overline{RSTW}$ and $\overline{RSTR}$) and the clock signals (WCK and RCK) in common, and by controlling the reset signal input interval.

The delay length of one scanning line is used in various applications for two-dimensional data processing. The μPD42505 can also be used in applications such as VTR jitter compensation (time axis variation) caused by the variance in head drum rotation rate or the expansion or shrinkage of the tape, applications requiring variable-length delay lines to contract or expand a video image in the horizontal direction, applications involving the synchronization of two or more digital signal inputs, and as a line buffer in data transfer operations between devices using different data transfer rates.

Figure 13. μPD42505 5048 x 8 Line Buffer



NEC Electronics Inc.

APPLICATION NOTE 55
μPD41101/μPD41102
HIGH-SPEED LINE BUFFERS

Introduction

The μPD41101 and μPD41102 are high-speed serial access line buffers organized as 910 words x 8 bits and as 1135 words x 8 bits, respectively. An algorithm that enables data to be read out in the order in which it was input makes these devices suitable for use as data delay lines or for converting data transfer rates, e.g., as buffer storage used for data transfer between devices with different data processing rates.

The μPD41101 can process an NTSC composite video signal (the TV system used in Japan and North America) that has been previously digitized. The fast access times of the device allow a sampling frequency of four times the color signal subcarrier frequency (where f_{SC} = 3.58 MHz and $4f_{SC}$ = 14.32 MHz) for each scanning line to be used. This means that 910 addresses are required for each scanning line when sampling at $4f_{SC}$.

The μPD41102 can process a PAL composite video signal (the TV system used in European countries other than France) that has been previously digitized. This device also uses a sampling frequency of four times the color signal subcarrier frequency (where f_{SC} = 4.43 MHz and $4f_{SC}$ = 17.72 MHz) for each scanning line, which means that 1135 addresses are required for each scanning line when sampling at $4f_{SC}$.

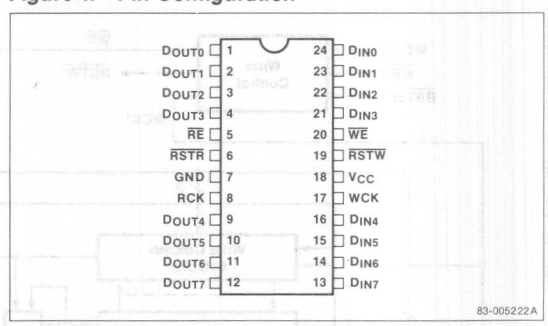
Figure 1 shows the pin configuration for these devices. The D_{IN0}-D_{IN7}, $\overline{RSTW}$, $\overline{WE}$, and WCK pins control write operation, while D_{OUT0}-D_{OUT7}, $\overline{RSTR}$, $\overline{RE}$, and RCK control read operation. The pins are organized to operate asynchronously and at different speeds simultaneously. A built-in serial address generator automatically generates read and write addresses so that an address need not be supplied externally.

High-Speed Operation

Write and Read Operation

Write and read cycles are executed identically. One address of data (8 bits) is written or read in one cycle in synchronization with WCK or RCK when $\overline{WE}$ or $\overline{RE}$ is low. The write or read address is incremented by 1 at the falling edge of each write or read clock. Write data must satisfy setup and hold times as measured from the rising edge of WCK.

Figure 1. Pin Configuration



The $\overline{RSTW}$ and $\overline{RSTR}$ reset signals initialize the write and read address pointers to 0. A reset signal must be input to satisfy the setup and hold times as measured from the rising edge of WCK or RCK. Once the address is initialized, a write or read cycle is executed in synchronization with its respective clock and the pointer is incremented by 1. In the μPD41101, the pointer returns to 0 after address 909. In the μPD41102, the pointer returns to 0 after address 1134.

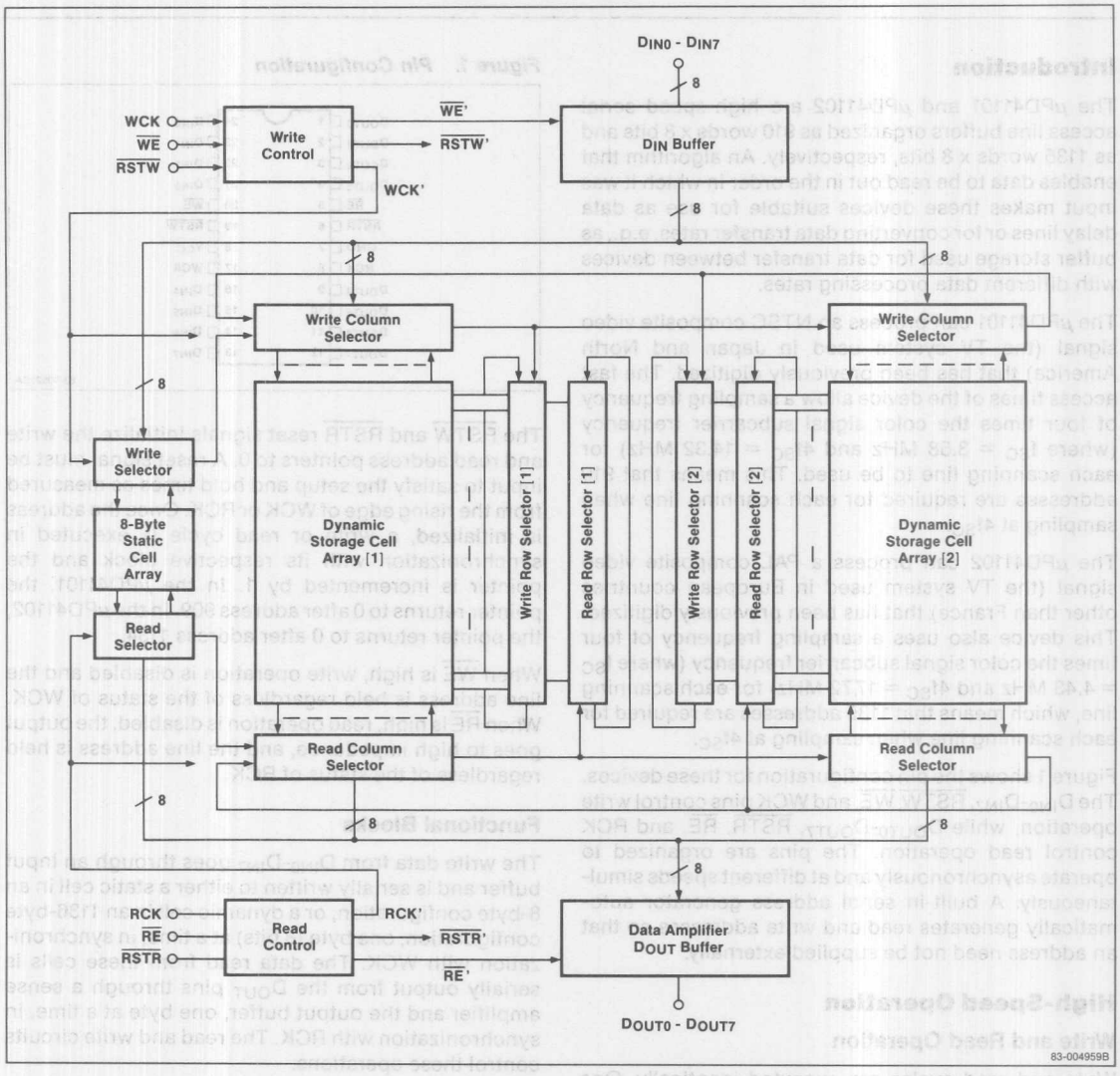
When $\overline{WE}$ is high, write operation is disabled and the line address is held regardless of the status of WCK. When $\overline{RE}$ is high, read operation is disabled, the output goes to high impedance, and the line address is held regardless of the status of RCK.

Functional Blocks

The write data from D_{IN0}-D_{IN7} goes through an input buffer and is serially written to either a static cell in an 8-byte configuration, or a dynamic cell in an 1136-byte configuration, one byte (8 bits) at a time, in synchronization with WCK. The data read from these cells is serially output from the D_{OUT} pins through a sense amplifier and the output buffer, one byte at a time, in synchronization with RCK. The read and write circuits control these operations.

WCK, $\overline{WE}$, and $\overline{RSTW}$ are input to the write control circuit. RCK, $\overline{RE}$, and $\overline{RSTR}$ are input to the read control circuit. These segments are composed of simple gate circuits (figure 2).

Figure 2. Block Diagram of the μPD41101 and μPD41102



The μPD42101 and μPD42102 exactly replace the μPD41101 and μPD41102.

Storage Cells

The μPD41101 and μPD41102 use dual-port storage cells to execute read and write cycles asynchronously and at different speeds (figures 3 and 4).

Static Cell Organization. In the static cell, two pairs of transfer gates (one pair each for read and write operation) are connected to the flip-flop in the middle. The other end is connected to a pair of bit lines for read operation (RD, $\overline{RD}$), and another pair for write operation (WD, $\overline{WD}$). One word line each for RW and WW are connected to the transfer gate pins.

When the word line for a write cycle (WW) goes to the selected level, and write data is applied to the pair of bit lines (WD, $\overline{WD}$) of the selected column, a write cycle is executed on the cell where the row (word line) and column (bit line) intersect.

A read cycle is executed independently. When the word line goes to the selected level (RW), data is transferred to the bit line pair (RD, $\overline{RD}$) through a transfer gate. Data is selected by the column signal and read externally. Data in the storage cell at the intersection of the selected row and column is also read.

Read and write data are input as a differential signal so that the static dual-port cell can operate at a higher speed. The circuit size is larger because it requires more components.

Dynamic Cell Organization. Each dynamic array in the μPD41101 and μPD41102 consists of two subarrays with 71 rows apiece. Each row of the subarray consists of 8 (number of bits) x 8 addresses (bytes). Each row of each subarray therefore has 8 subword lines. Figure 5 shows the organization of a dynamic array.

Figure 3. Dual-Port Static Storage Cell

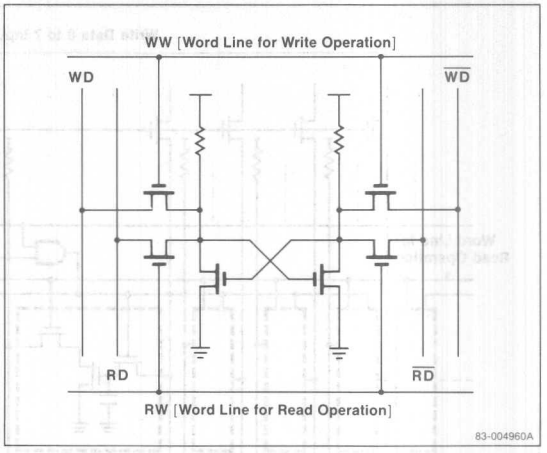
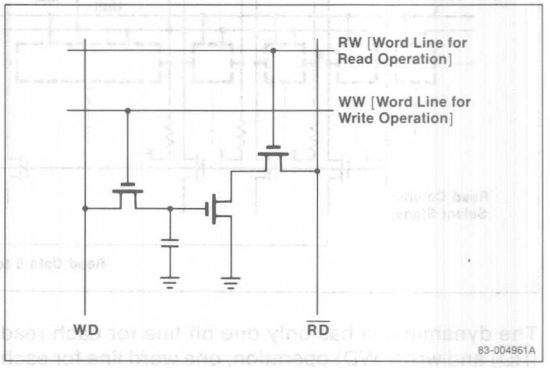
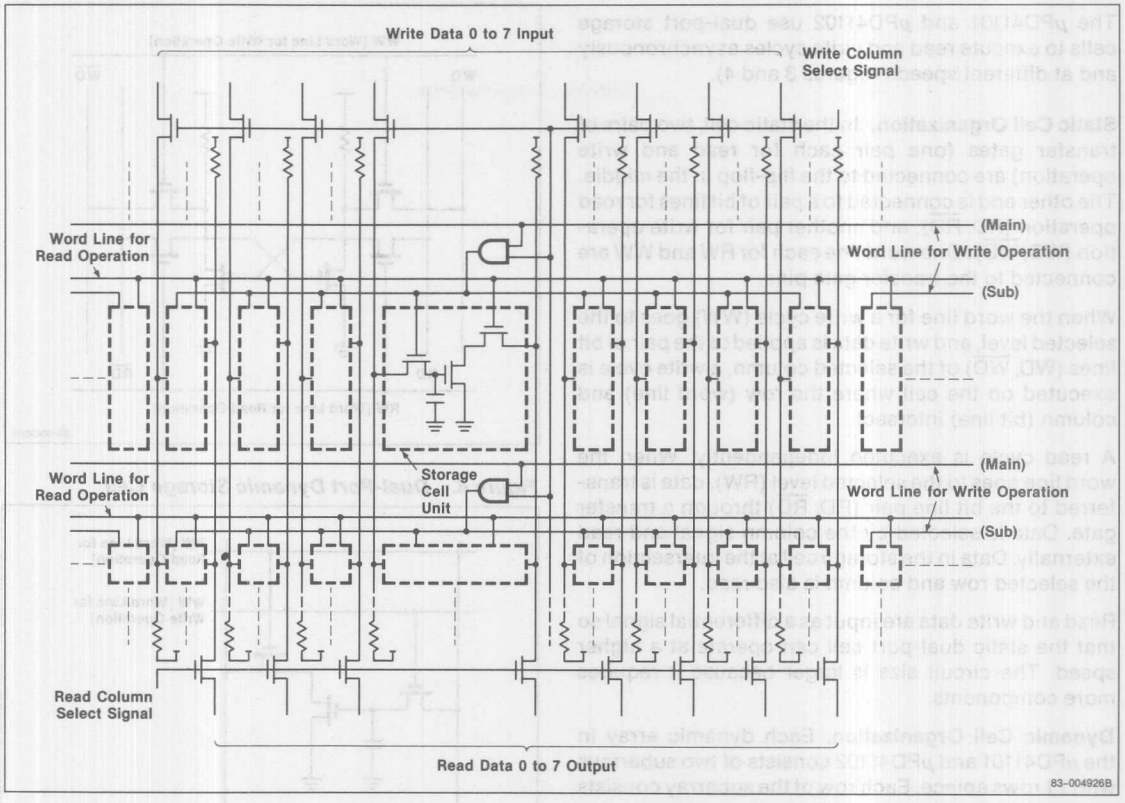


Figure 4. Dual-Port Dynamic Storage Cell



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Figure 5. Organization of Dynamic Storage Array



The dynamic cell has only one bit line for each read ($\overline{RD}$) and write (WD) operation, one word line for each read (RW) and write (WW) operation, three transistors, and one capacitor. Although the longer data sense phase reduces its speed, a dynamic cell can be configured with fewer components and used for high-density integration.

In a write cycle, write data input through the bit line (WD) is guided through a transfer gate made conductive by the word line (WW). The gate charges or discharges the storage capacitor.

In a read cycle, the transistor with the gate connected to one end of the storage capacitor is turned on or off depending on whether or not the capacitor is charged. Data is transferred to the bit line ($\overline{RD}$) through the transfer gate, made conductive by the word line (RW), and then read externally. Word and bit lines for each operation are independent of each other so that read and write cycles can be executed asynchronously.

Data Transfer

The μPD41101 and μPD41102 are configured so that the internal address is incremented one bit at a time and data is accessed serially. After a reset signal initializes the device, a static cell that can operate at higher speed is accessed. Simultaneously or later, a dynamic cell is used as a pipeline, allowing access to both types of cells at high speed.

Stored information is defined by the state of the storage capacitor. When the word line for the write cycle goes to a selected level, the write transfer gate of each storage cell connected to the word line becomes conductive, and the data (electrical level) given to the bit line is rewritten to the capacitor connected to the end of the transfer gate. The precharge level of the write bit line (typically a high level) is rewritten to the storage cells on the selected word line, other than the one to which the column signal applies data, thereby destroying data stored there.

The μPD41101 and μPD41102 prevent this destruction of data by using a main word line and a subword line. The subword line is driven by the ANDed signals of the main word line and the write column. The transfer gate of each cell corresponding to each address is connected to a subword line. Therefore, the write word line of the storage cells at the selected row and column address is the only one which goes to a high level, preventing the destruction of data in other cells on the same write line.

Address Selection

A dynamic storage array consists of subarrays 1 and 2, each of which is 568 (71 x 8) bytes. A column selector and a row selector circuit are provided for independent read and write operation for each subarray.

The first step of address selection involves the accessing of an 8-byte static cell immediately after a reset cycle. The address selector moves to the first row of the subarray, and subarray 1 is accessed from left to right, one byte at a time. When 8 bytes of subarray 1 have been accessed, the address selector moves to the first row of subarray 2, also accessed from left to right, one byte at a time. When 8 bytes of subarray 2 have been accessed, the address selector alternately selects 8 bytes from addresses in both subarrays, so that rows are selected from the higher row to the lower row.

When the number of access cycles to the static cell array (8 addresses) and the dynamic cell array reaches 910 (for the μPD41101) or 1135 (for the μPD41102), the pointer moves to address 0 of the static array.

This method of sequential address selection increases the access speed of the dynamic cell by selecting row addresses in the pipeline method. Pipeline operation occurs when the word line (row) to be selected next is set to the selected level in advance so that it can be written or read at high speed, i.e., in the time required to select one column in static-column mode.

After a reset cycle, when 8 bytes of the static cell are being accessed, the first row of subarray 1, which is accessed next, is set to the selected level in advance. When the selected address moves to the first row of subarray 1 (after 8 bytes of static storage are accessed), a read or write cycle can be executed at high speed for that row. The first row of subarray 1 can be accessed at high speed even after the static array is selected. This process continues with the first row of subarray 2, the second row of subarray 1, and so on.

While the static cell is being accessed immediately after a reset cycle, the address on the dynamic cell is held on the first column and row of subarray 1. The dynamic array is not accessed at this time. Pipeline operation is performed independently for write and read cycles by the row and column selectors for each subarray.

Shift registers are used as read and write column and row selectors for the sequential selection of write or read addresses and pipeline processing. Shift registers are provided for each column and row, and each node level is set in advance so that when reset, each shift register outputs a high signal for the first column or row and a low signal for other columns or rows.

The column selector (shift register) is driven by WCK or RCK and the address is incremented by 1 for each clock cycle, i.e., the node that outputs a high signal changes in synchronization with the clock, and the column selector changes with it.

The row selector (shift register) is related to pipeline control and is driven by the pulse generated when the column address selector moves from subarray 1 to subarray 2 or vice versa. The row selector is incremented by one row address after the change from one subarray to another.

Each shift register used as a column or row selector is configured as a ring counter so that when the last column or row is reached, it automatically returns to the first column or row.

Applications

For the most part, the applications described below pertain to noninterlaced digital TV. The descriptions apply to NTSC systems, unless otherwise specified.

Comb Filter

A composite TV signal (output of a TV tuner) is the sum of the luminance (Y) and chrominance (R-Y, B-Y) color signals. The Y, R-Y, and B-Y signals must be separated, and the R, G, and B signals input to the picture tube generated from them.

A comb filter with line buffers derives the color or luminance signal by cancelling it from the composite signal, using the correlation between neighboring lines. This filtering fully separates the color and luminance signals, especially when there is a strong correlation between lines, to produce a clear picture.

If the signals are not well separated, the color signal may interfere with the luminance signal and cause dot crawl. The luminance signal may also interfere with the color signal and cause cross-color. This interference degrades the picture quality, especially where color or luminance changes sharply. Figure 6 shows a typical comb filter using line correlation.

This example compares target line B with neighboring lines A and C. Two μPD41101s are used as 910-bit delay lines. The color signal (C = R-Y, B-Y) is separated by subtracting the data of the upper and lower lines (A + C) from the target line data (B) and filtering the separated signal through the 3.58-MHz bandpass filter. The luminance signal is the result of subtracting the separate color signal from the original data (B). See the description of the "Variable-Length Delay Line" application for information on controlling a delay line of 910 bits or less.

Double-Speed Scan Conversion

The current NTSC and PAL TV systems use interlaced scanning to eliminate the flickering caused by field transition. Scanning is performed every two lines, reducing the pixel density and doubling the field frequency (number of fields-per-second), as illustrated in figure 7.

In interlaced scanning in the NTSC system, a complete frame consists of two fields of 262.5 scanning lines each. The field frequency is 60 Hz, i.e., the sum of 30 first fields-per-second and 30 second fields-per-second. In the PAL system, a complete frame is comprised of two fields of 312.5 scanning lines each. The field frequency is 50 Hz, the sum of 25 first fields-per-second and 25 second fields-per-second. In both cases, interlaced scanning reduces the flicker in motion scenes caused by field transition. The pixel density in the vertical direction is also reduced, diminishing the level of detail.

Figure 6. Interline Y/C Separation with a Comb Filter

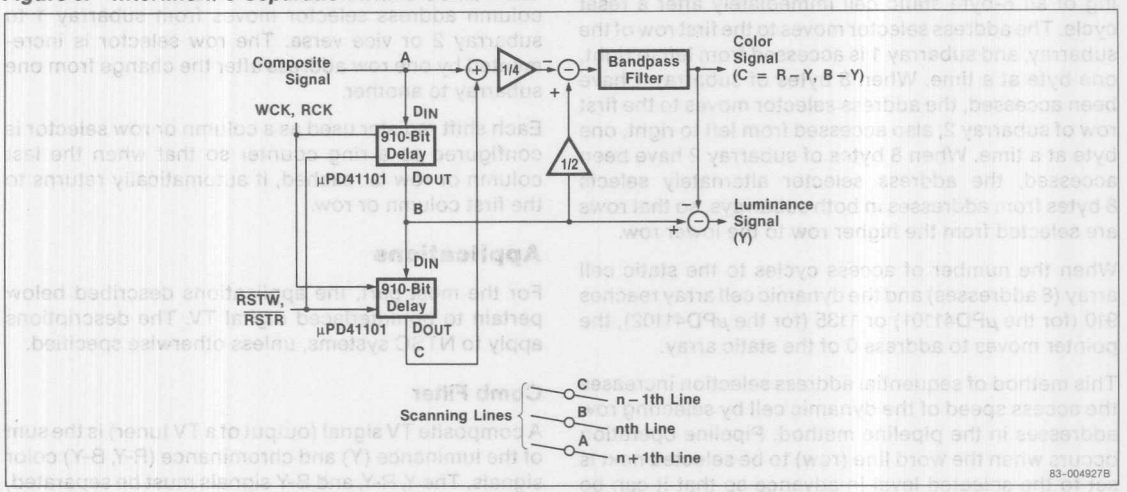
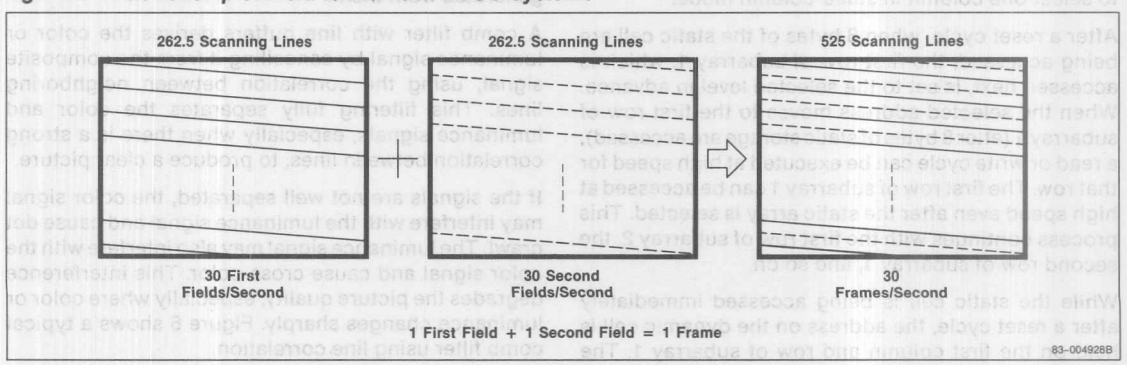


Figure 7. Relationship of Field to Frame in NTSC Systems



The μPD42101 and μPD42102 exactly replace the μPD41101 and μPD41102.

The μPD41101 or μPD41102 can be used to convert interlaced scanning to noninterlaced scanning. Doubling the pixel density (number of scanning lines) in the vertical direction without changing the field frequency produces clear and precise images (figure 8). In interlaced scanning, the first field of solid lines and the second field of broken lines are scanned alternately at 30 fields-per-second (25 fields-per-second in PAL). In noninterlaced scanning, the number of scanning lines per field is doubled, and 60 fields-per-second are scanned (50 fields-per-second in PAL).

In noninterlaced scanning, the data of the skipped line is created using the buffer. It is read at twice the sampling frequency of interlaced scanning (8 f_{SC} if the interlaced sampling rate is 4 f_{SC}). Noninterlaced scanning scans two lines in the time that one line is scanned in interlaced scanning. The horizontal frequency of the CRT must also be doubled for noninterlaced scanning.

The data of the skipped line can be created

- Using the data of the previous line (reading out the same data twice)
- Using the average value of the lines before and after the skipped line
- Using data that is one-field-old (the data for 262 lines before for NTSC, or 312 lines before for PAL)

In the first option, one μPD41101 (or one μPD41102 for PAL) is used for one input signal. The data is written at 4 f_{SC} and read out at 8 f_{SC}. Reading starts when data is written to half of the line (455 bytes). The same data is read twice (910 bytes x 2) at 8 f_{SC}. Data read in the latter half is used as interpolated data (figure 9).

In the second method, one μPD41101 delays the data of one line, and two μPD41101s convert the current data and the interpolated data for double-speed scanning.

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Figure 8. Interlaced and Noninterlaced Scanning

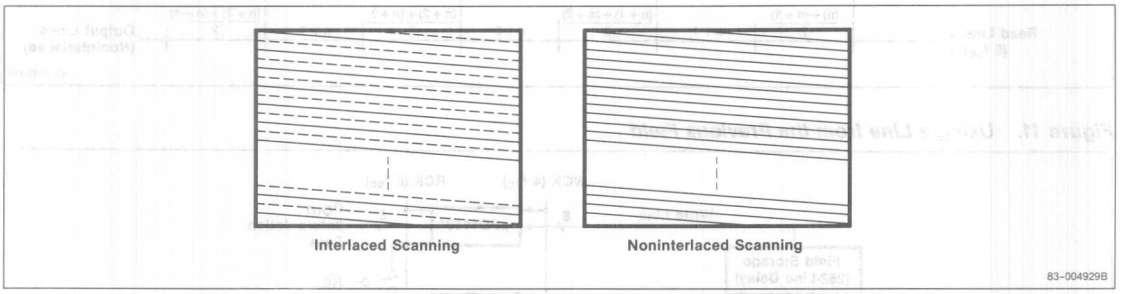
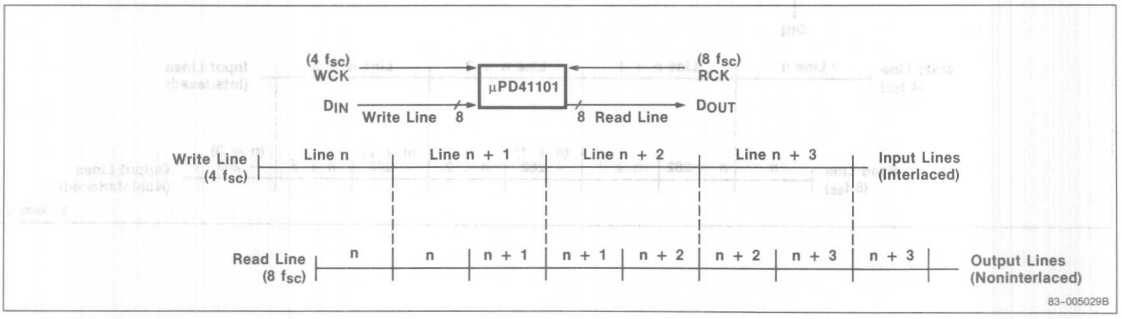


Figure 9. Using the Previous Line as Interpolated Data



The two μPD41101s used for scan conversion are written at 4 f_{SC} and read at 8 f_{SC}. The $\overline{RE}$ signal is controlled to first read the μPD41101 to which the current line data is written, and then read the μPD41101 to which the interpolated data is written (figure 10).

In the last option, as in the previous one, one buffer delays the data for one field and two other μPD41101s perform scan conversion. The control sequence is the same as described in the second method. Using data from a line of the previous field produces a clear image, especially in a still scene (figure 11).

Figure 10. Using the Average of the Previous and Following Lines

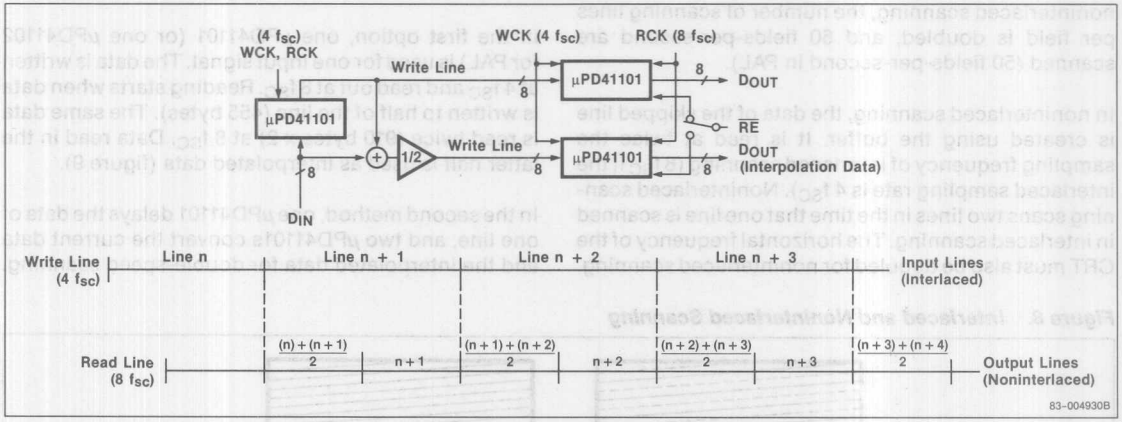
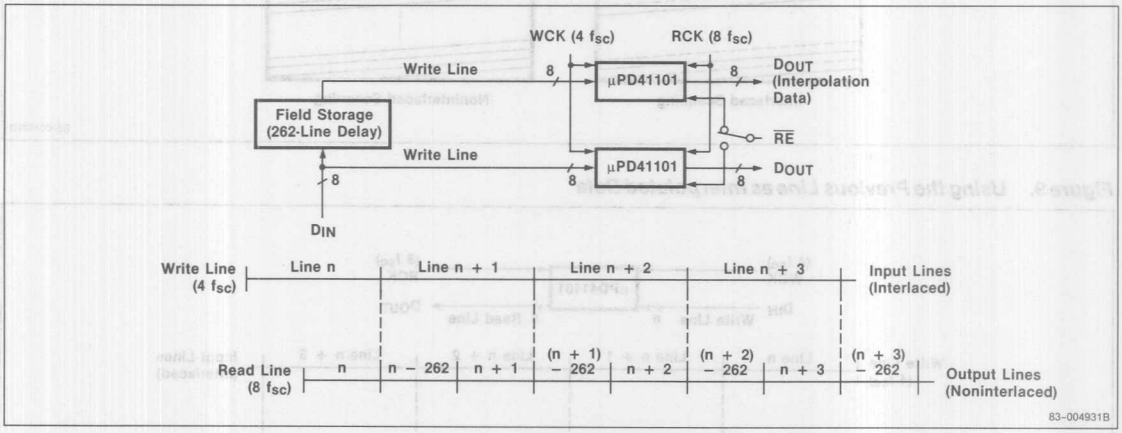


Figure 11. Using a Line from the Previous Field

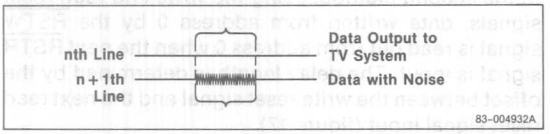


The μPD42101 and μPD42102 exactly replace the μPD41101 and μPD41102.

Dropout Compensation

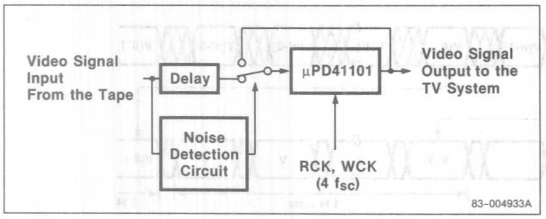
Dropout compensation cancels the noise in a VTR picture reproduction. If a line contains noise, the portion of the previous line in the same position as the noise is reproduced instead, eliminating the noise from the reproduced image (figure 12).

Figure 12. Example of Dropout Compensation



Video data from a tape normally is written to the μPD41101, delayed for one scanning line (910 bits), and then used as image data to a TV system. The noise-detection circuit senses noise in the video signal. When data containing noise is input to the μPD41101, the input is switched to the data already in the buffer so that the previous data line is written again. Data containing the noise is not output to the TV system (figure 13).

Figure 13. Dropout Compensation Circuit

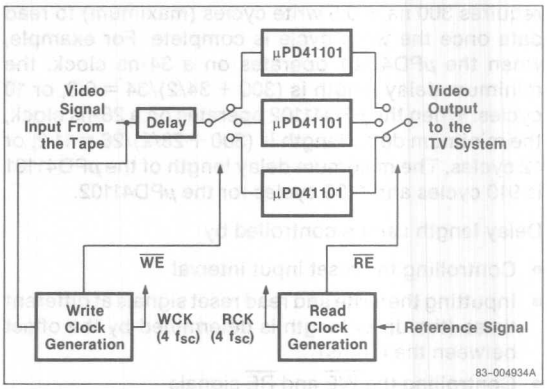


The μPD41101 can also be used as a 910-bit (one scanning line) delay. If the write data fed back by switching is delayed, the delay length must be reduced to compensate for it. For example, if switching causes two bits of delay, the delay length must be adjusted to 908 bits.

Jitter Compensation [Time Base Correction]

In a VTR, variation in head drum rotation speed or tape contraction or expansion can cause jitter in the reproduced image. The image can be reproduced clearly when jitter is adjusted and the image is reproduced with accurate clocks (figure 14).

Figure 14. Basic Jitter Compensation Circuit

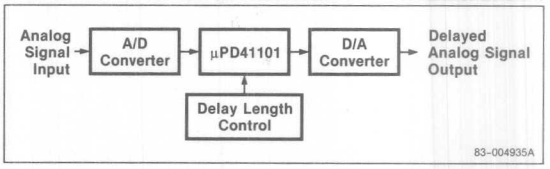


The video signal input from the tape is written to the μPD41101 with a clock that can be accurately slaved to the time axis variation of the input video signal. Video data with the same time axis is reproduced by reading data using the synchronized read clock as a reference. If a jitter compensation circuit is configured so that the device to which the data is written, or from which it is read, is selected from among two or more devices by the $\overline{RE}$ or $\overline{WE}$ signal, the circuit can have a delay length of two or more lines.

Variable-Length Delay Line

The μPD41101, driven at 8 f_{SC}, can be used as a variable-length delay line with a delay length of 10 to 910 bits (12 to 1135 bits for the μPD41102). Driven at 4 f_{SC}, it can produce a delay of 5 to 910 bits (6 to 1135 bits for the μPD41102). If an analog-to-digital (A/D) and a digital-to-analog (D/A) converter are connected to the input and output sides, respectively, it can also be used as an analog signal delay line (figure 15).

Figure 15. Analog Signal Delay Line



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When reading data at a certain address, the μPD41101 requires 300 ns + 0.5 write cycles (maximum) to read data once the write cycle is complete. For example, when the μPD41101 operates on a 34-ns clock, the minimum delay length is (300 + 34/2)/34 = 9.3, or 10 cycles. When the μPD41102 operates on a 28-ns clock, the minimum delay length is (300 + 28/2)/28 = 11.2, or 12 cycles. The maximum delay length of the μPD41101 is 910 cycles and 1135 cycles for the μPD41102.

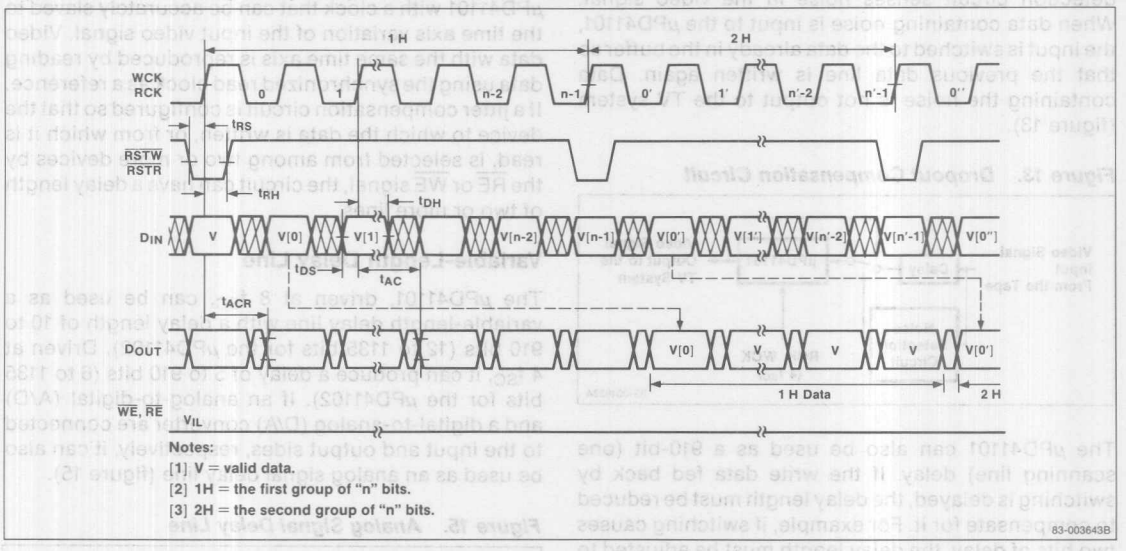
Delay length can be controlled by

- Controlling the reset input interval
- Inputting the write and read reset signals at different times (the delay length is determined by the offset between the inputs)
- Controlling the $\overline{WE}$ and $\overline{RE}$ signals

In the first method, the same signal is used for WCK and RCK. $\overline{RSTW}$ and $\overline{RSTR}$ are controlled together. Data written after a reset signal is read after the next reset interval. If the reset signal is input every 900 cycles, the delay length is 900 bits. This option produces a delay length determined by the reset interval to control the delay length (figure 16).

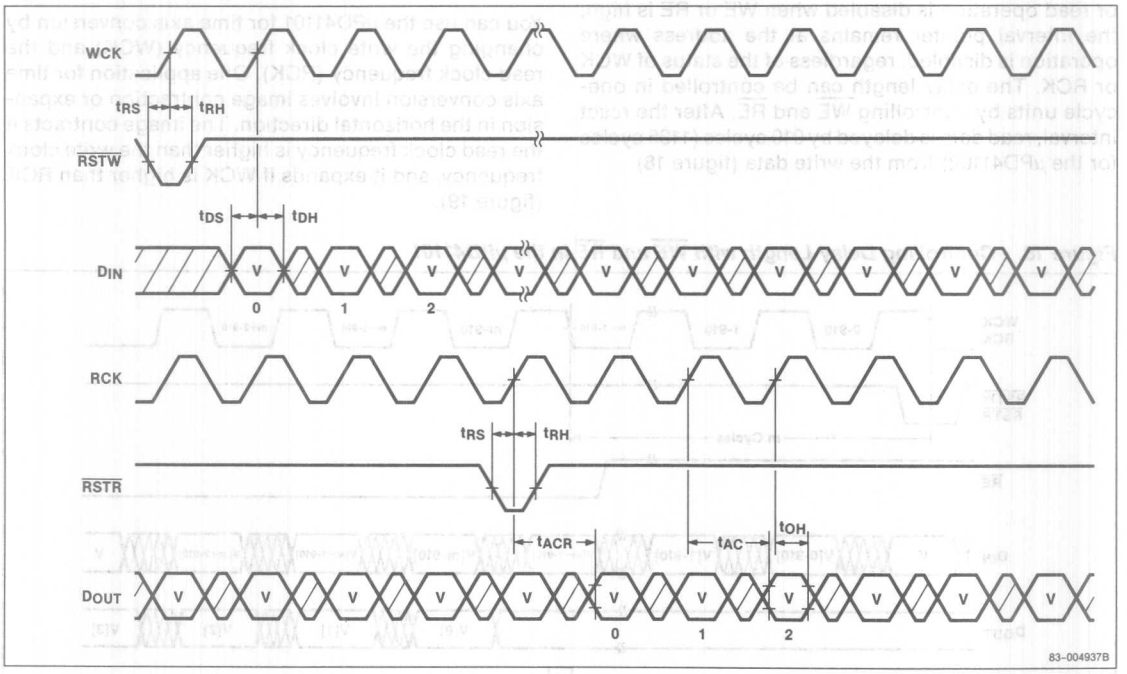
In the second method, using the write and read reset signals, data written from address 0 by the $\overline{RSTW}$ signal is read out from address 0 when the next $\overline{RSTR}$ signal is input. The delay length is determined by the offset between the write reset signal and the next read reset signal input (figure 17).

Figure 16. Controlling Delay Length with the Reset Interval



The μPD42101 and μPD42102 exactly replace the μPD41101 and μPD41102.

Figure 17. Controlling Delay Length with $\overline{RSTW}$ and $\overline{RSTR}$



In the third method, using the $\overline{WE}$ and $\overline{RE}$ signals, write or read operation is disabled when $\overline{WE}$ or $\overline{RE}$ is high; the interval pointer remains at the address where operation is disabled, regardless of the status of WCK or RCK. The delay length can be controlled in one-cycle units by controlling $\overline{WE}$ and $\overline{RE}$. After the reset interval, read data is delayed by 910 cycles (1135 cycles for the μPD41102) from the write data (figure 18).

Time Axis Conversion

You can use the μPD41101 for time axis conversion by changing the write clock frequency (WCK) and the read clock frequency (RCK). One application for time axis conversion involves image contraction or expansion in the horizontal direction. The image contracts if the read clock frequency is higher than the write clock frequency, and it expands if WCK is higher than RCK (figure 19).

Figure 18. Controlling Delay Length with $\overline{WE}$ and $\overline{RE}$ in the μPD41101

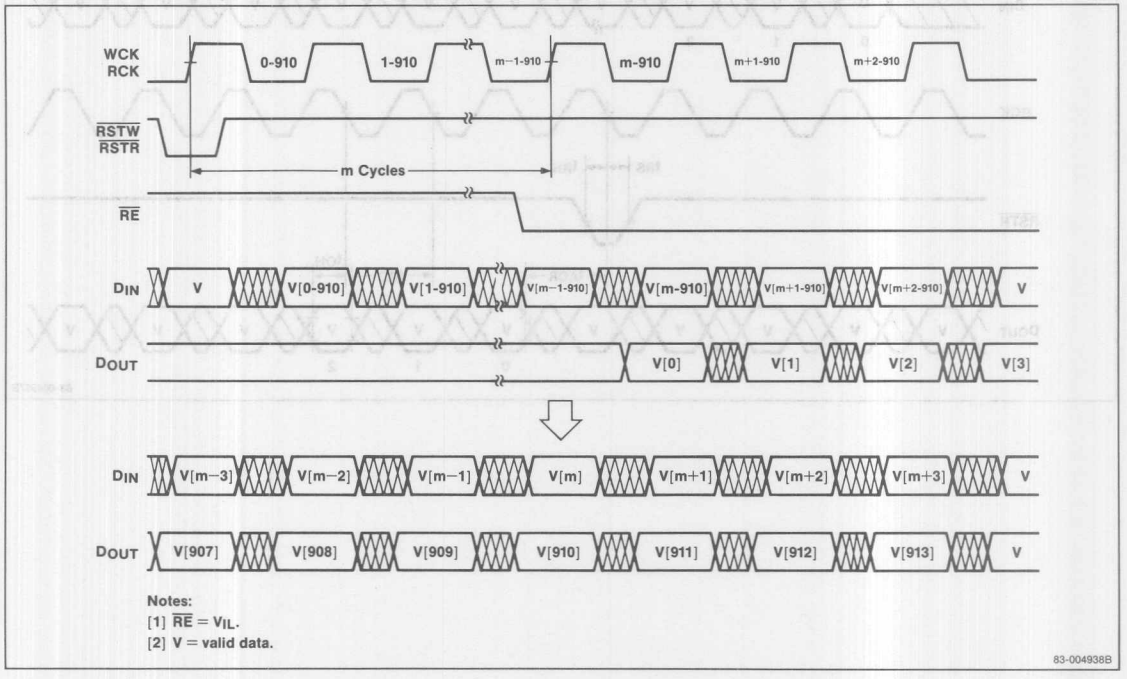
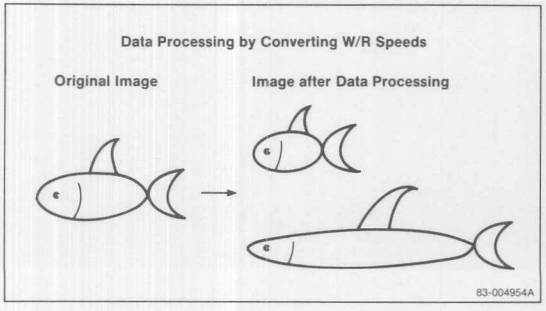


Figure 19. Time Access Conversion Application



The μPD42101 and μPD42102 exactly replace the μPD41101 and μPD41102.

Digital Signal Input Synchronization

When performing timeshared data processing in an electronic telephone exchanger or in a star-configured local area network, the phase between input streams may be offset because of differences between the terminal and the central line exchange module. The μPD41101 can be used to correct the phase offset (figure 20).

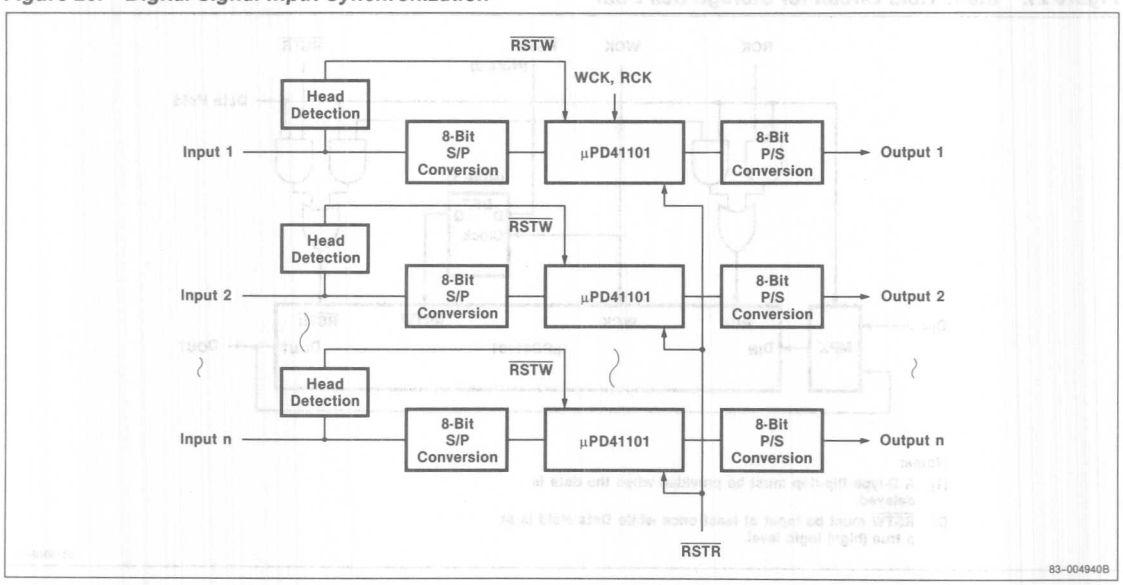
Inputs 1 to n are serial data input streams. However, the frame heads (flags indicating the beginning of the data) of each input stream are not synchronized.

The solution requires controlling write operation for each stream. When a frame head is detected, the write address is reset to 0. A clock extracted from each input can be used as the clock for that write cycle. When data is written to all μPD41101s, the read address is reset to 0 by inputting $\overline{\text{RSTR}}$ with appropriate timing. All data streams then can be read out in the same phase by reading all μPD41101s simultaneously, even if the input streams are not synchronized.

The serial-to-parallel and parallel-to-serial conversion circuits shown in figure 20 may be used only when serial data is handled at each input and output.

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Figure 20. Digital Signal Input Synchronization



General Application

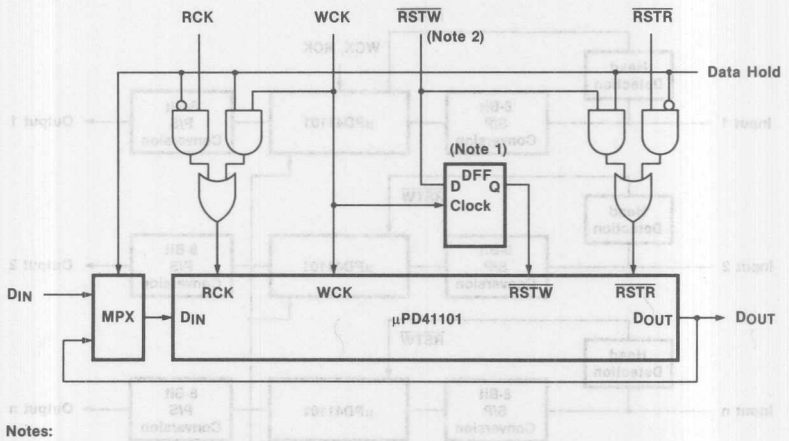
The μPD41101 and μPD41102 are suitable for use as buffer storage in data transfer operations between devices of different speeds. Because they use dynamic circuits, the maximum hold time for storage cell data is 1 ms. To hold data longer than 1 ms, you must rewrite it to the same address within 1 ms (figure 21).

The read and write addresses must coincide when rewriting data. If the feedback data is not delayed by a multiplexer, input the $\overline{\text{RSTW}}$ and $\overline{\text{RSTR}}$ signals simultaneously so that the output data of address n is fed back to the input as it is, and then written again to address n.

If the feedback data is delayed, adjust the input timing of $\overline{\text{RSTW}}$ and $\overline{\text{RSTR}}$, depending on the delay (number of cycles) of the feedback data. $\overline{\text{RSTR}}$ must be advanced according to the feedback data delay.

In either case, WCK and RCK must be the same. To read the data written to an address after the write cycle for that address is complete, 300 ns + one-half write cycle is required.

Figure 21. Static Hold Circuit for Storage Cell Data



Notes:

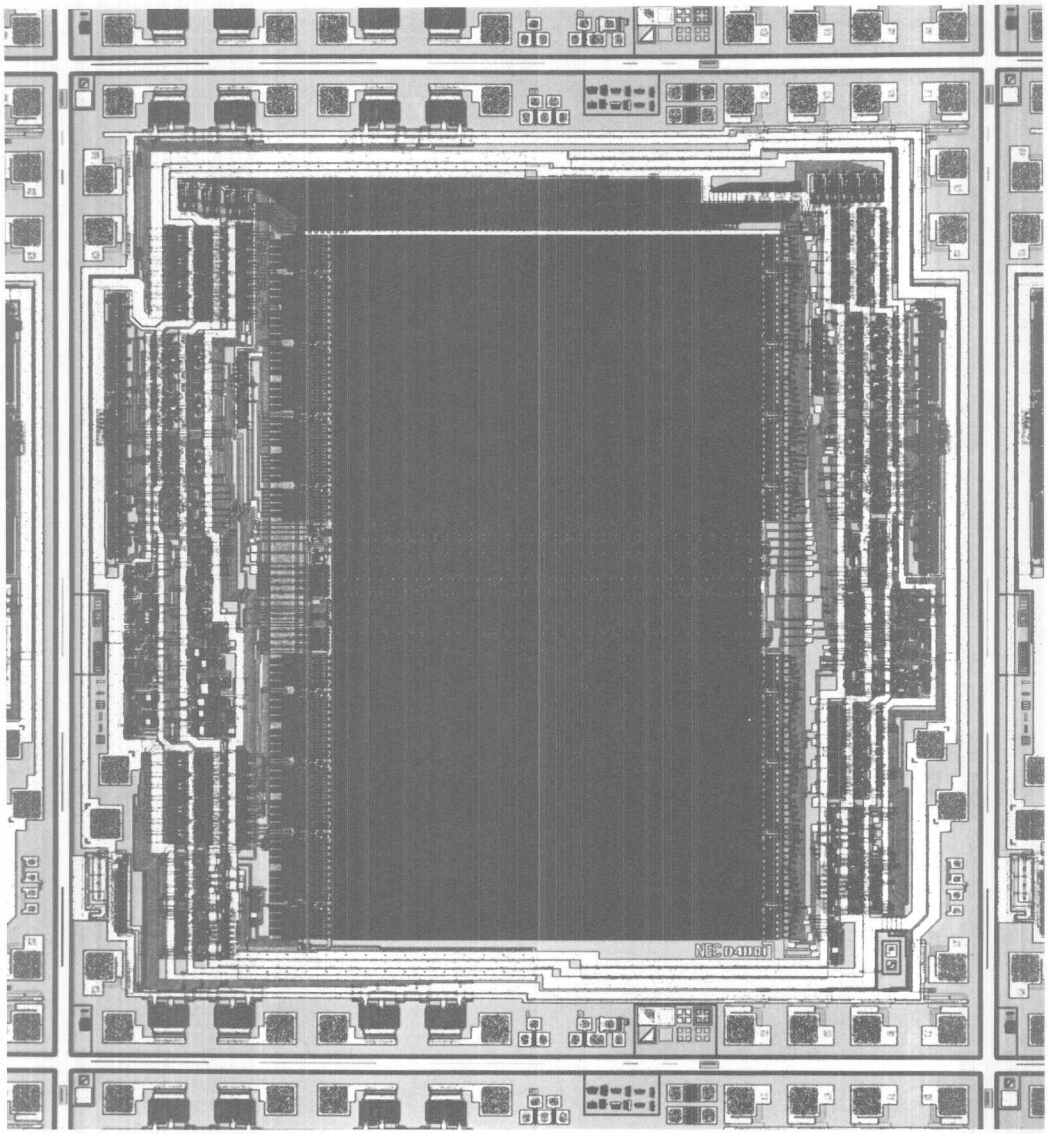
[1] A D-type flip-flop must be provided when the data is delayed.

[2] $\overline{\text{RSTW}}$ must be input at least once while Data Hold is at a true (high) logic level.

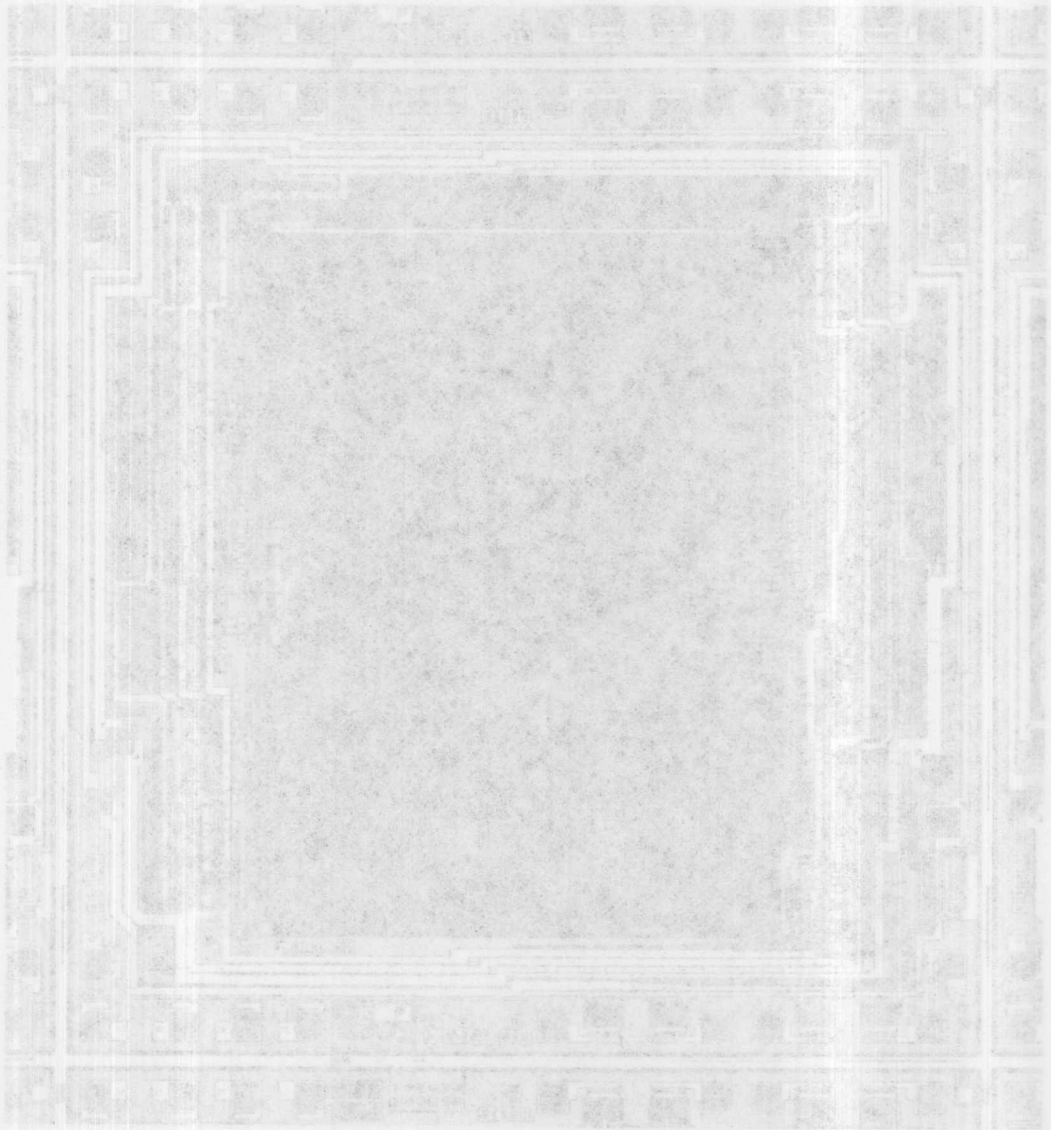
83-004941A

The μPD42101 and μPD42102 exactly replace the μPD41101 and μPD41102.

Figure 22. μPD41101/μPD41102 High-Speed Line Buffer



The μPD42101 and μPD42102 exactly replace the μPD41101 and μPD41102.



Introduction

In the field of computer-aided design and manufacturing (CAD/CAM), running software with many utility programs results in time-consuming disk accesses. Workstations operating in a local area network (LAN) also are performance-limited by the heavy burden on magnetic disks serving multiple users. These systems receive a performance boost when the magnetic disk is replaced with a solid-state disk.

NEC developed the μPD42601 silicon file, a 1,048,576 x 1-bit semiconductor disk, precisely for such applications. The CMOS-fabricated μPD42601 operates much faster than hard disks, with simplified circuitry and fewer sense amplifiers than standard DRAMs. Although access times from $\overline{RAS}$ (t_{RAC}) and $\overline{CAS}$ (t_{CAC}) of 600 ns and 100 ns, respectively, make this device slower than standard DRAMs such as NEC's μPD421000, the use of word-width system architecture and page-cycle accesses achieves very high data transfer rates and can therefore improve system efficiency.

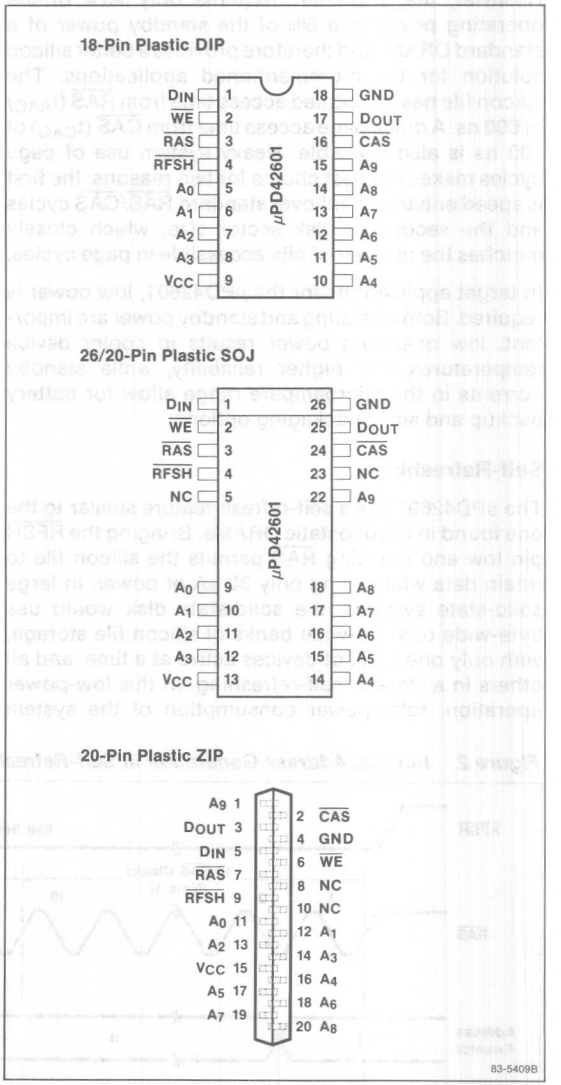
Applications

Because the device's high capacity, battery-supportable nonvolatility, and environmental hazard resistance are expected to challenge the niche previously defined by bubble devices, the μPD42601 should find its major market in large solid-state disk applications. However, as shown in table 1, other potential markets exist. For example, the μPD42601's very low data retention current, which reduces heat buildup and simplifies thermal design, means that a cool die operating in a 300-mil SOJ offers greater flexibility in packaging and stimulates new ideas for other product applications (see figure 1 for packaging options and pin assignments of the μPD42601).

Table 1. Potential Markets for μPD42601 Silicon File

Market	Requirements	Applications
Solid-state disks	High capacity Reliability Battery backup	High-end engineering workstation (100 Mbytes to 1 Gbyte)
Portable handheld products	Light weight Low power Small size	Personal computers Retail point-of-sale terminals
Industrial	Immunity to a hazardous environment: vapors, dust, vibration	Process control Robotics

Figure 1. Pin Configurations



Power and Speed Enhancements

All access cycles and timing specifications for the μPD42601 are similar to those of generic DRAMs. However, the μPD42601 requires only 25% of the operating power and 5% of the standby power of a standard DRAM, and therefore provides a better silicon solution for the aforementioned applications. The silicon file has a specified access time from $\overline{RAS}$ (t_{RAC}) of 600 ns. A quick page access time from $\overline{CAS}$ (t_{CAC}) of 100 ns is also available. Heavy system use of page cycles makes the best choice for two reasons: the first is speed enhancement over standard $\overline{RAS}$/$\overline{CAS}$ cycles and the second is disk sector size, which closely matches the number of bits accessible in page cycles.

In target applications for the μPD42601, low power is required. Both operating and standby power are important: low operating power results in cooler device temperatures and higher reliability, while standby currents in the microampere range allow for battery backup and small packaging options.

Self-Refreshing

The μPD42601 has a self-refresh feature similar to the one found in pseudostatic DRAMs. Bringing the $\overline{RFSH}$ pin low and clocking $\overline{RAS}$ permits the silicon file to retain data while using only 30 μA of power. In large solid-state systems, the solid-state disk would use byte-wide or word-wide banks of silicon file storage, with only one bank of devices active at a time, and all others in a state of self-refreshing. In this low-power operation, total power consumption of the system would be very low, making battery backup possible with compact batteries.

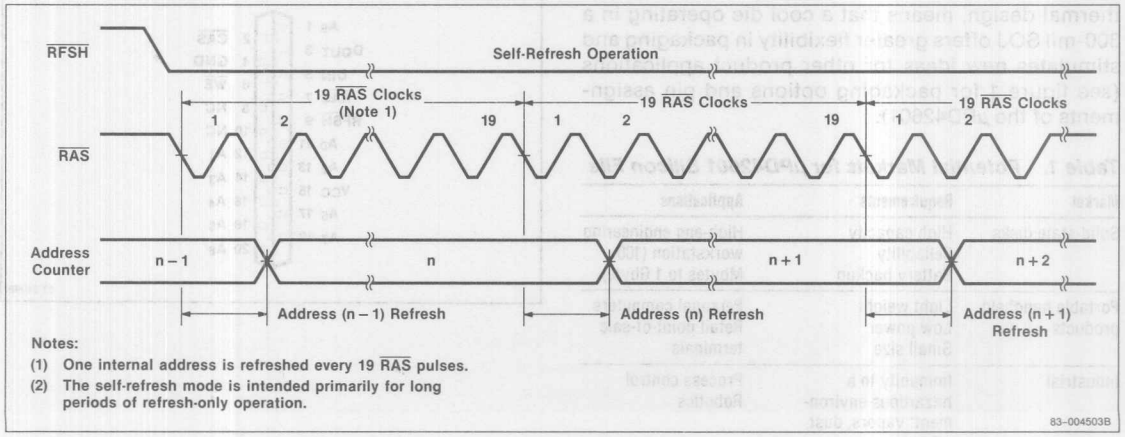
During self-refresh cycles, a relatively slow $\overline{RAS}$ clock can be applied and data integrity still be maintained. To enter this power-down quiescent state, the user can pull $\overline{RFSH}$ low and start the $\overline{RAS}$ clock at a slow cycle time (t_{RCF}). Since data loss is caused by leakage, and leakage current increases with temperature, NEC has specified the t_{RCF} rating at 50 °C, 60 °C and 70 °C. Each temperature rating has a corresponding refresh current (directly proportional to the refresh rate) which is required to maintain data, with faster rates required for higher temperatures (table 2).

Table 2. Self-Refresh Conditions

T_A	t_{RCF} (max)	Self-Refresh Current (max)
50 °C	20 μs	30 μA
60 °C	10 μs	60 μA
70 °C	5 μs	120 μA

It is important to make a distinction between self-refresh cycles and the more familiar $\overline{CAS}$ before $\overline{RAS}$ refresh cycles. When low, the $\overline{RFSH}$ pin enables self-refreshing and disables most of the internal circuits. Only those circuits required for self-refresh operation are active. Because of the rate of t_{RCF} required for substrate bias generation, nineteen $\overline{RAS}$ clocks are used in the μPD42601 to refresh one row (figure 2).

Figure 2. Internal Address Generation in Self-Refresh Operation



Notes:
(1) One internal address is refreshed every 19 $\overline{RAS}$ pulses.
(2) The self-refresh mode is intended primarily for long periods of refresh-only operation.

Figure 3 shows a simplified block diagram of the μPD42601 during self-refresh operation. The low level of $\overline{RFSH}$ disables the ring oscillator and initializes the $\overline{RAS}$ buffer and 19-bit counter. The external $\overline{RAS}$ clock is reduced in frequency by the 19-bit counter. The outputs of the counter and the timing generator are then used to generate the slow-speed timing, decoding, and sensing operations, while the substrate bias generator functions at a reduced frequency to keep the substrate stabilized but minimize power consumption.

Figure 4 shows the transition and delay times for I_{DD1}, I_{DD2}, I_{DD3}, and I_{DD5}. When $\overline{RFSH}$ goes low, a 2.5-ms delay occurs before the device enters true self-refreshing. The timing shown in figure 4 depends on internal temperature-compensated delay circuits and is required to allow the die to stabilize at a lower temperature. During this 2.5-ms period, the standby current is specified as I_{DD3}, or 500 μA. After the die cools, the substrate bias generator operates at a lower frequency and power consumption is composed of five components: the $\overline{RAS}$ buffer, the 19-bit counter, the decoder, the substrate bias generator, and the sense amplifiers. All other peripheral circuits are disabled.

Figure 4. Transition and Delay Timing in Self-Refresh Operation

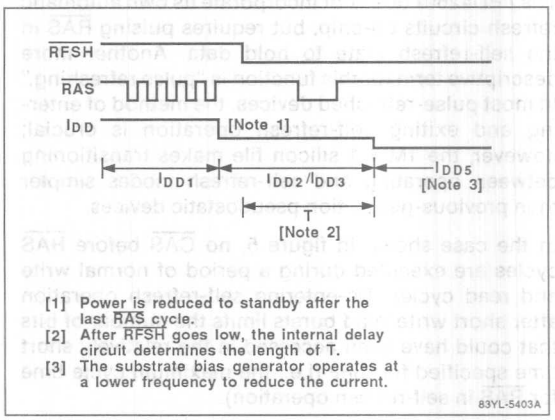
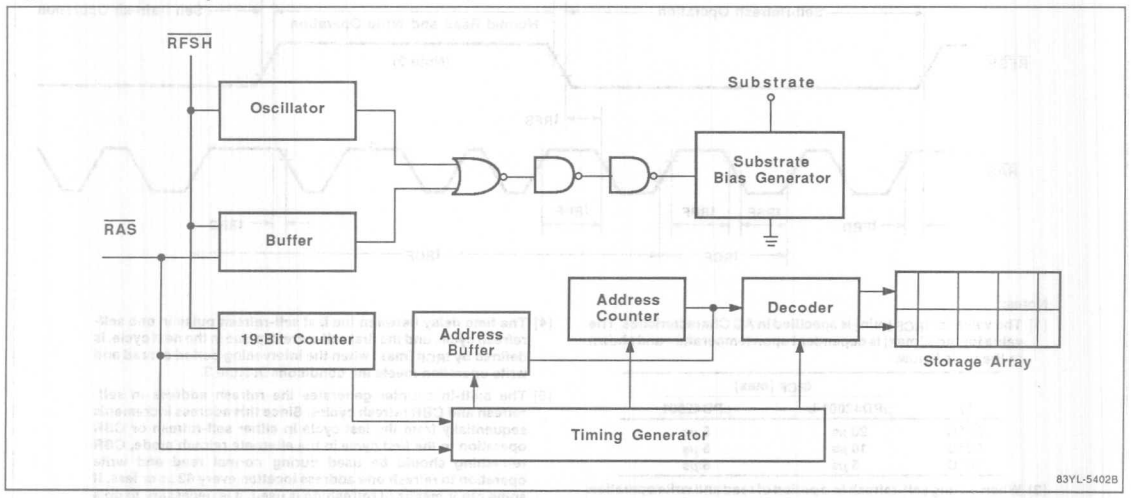


Figure 3. Circuit Operation in Self-Refresh Operation



$\overline{CAS}$ Before $\overline{RAS}$ Refreshing

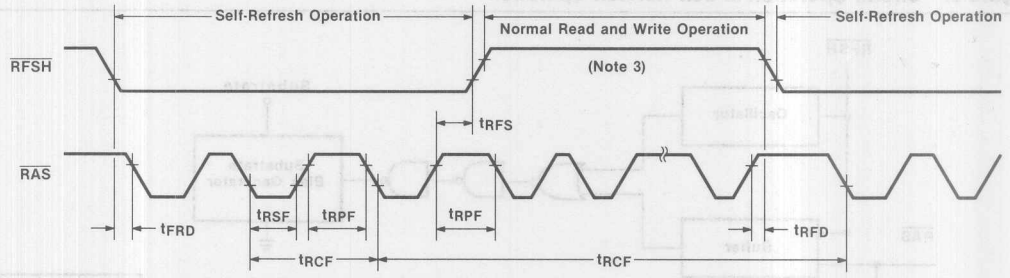
The μPD42601 does not incorporate its own automatic refresh circuits on-chip, but requires pulsing $\overline{RAS}$ in the self-refresh state to hold data. Another more descriptive term for this function is "pulse refreshing." In most pulse-refreshed devices, the method of entering and exiting self-refresh operation is crucial; however, the 1M x 1 silicon file makes transitioning between operating and self-refresh modes simpler than previous-generation pseudostatic devices.

In the case shown in figure 5, no $\overline{CAS}$ before $\overline{RAS}$ cycles are executed during a period of normal write and read cycles. Re-entering self-refresh operation after short write/read bursts limits the number of bits that could have been accessed in the relatively short time specified for t_{RCF} (i.e., the maximum cycle time for $\overline{RAS}$ in self-refresh operation).

If system timing remains in normal write or read operation longer than t_{RCF} (max), then refresh logic is needed to control $\overline{CAS}$ before $\overline{RAS}$ refreshing. Every 32 ms, 512 refresh cycles are needed to refresh the 512 row addresses, an average rate of one every 62 μs. Because of the reduced operating current and the resultant lower die temperature, the refresh period can be extended to four times the 8-ms value specified for most 1M x 1 DRAMs.

In $\overline{CAS}$ before $\overline{RAS}$ cycles, addresses need not be supplied because an internal counter supplies them to the decoders. Since the clocks for both $\overline{CAS}$ before $\overline{RAS}$ refresh cycles and self-refresh cycles increment the same internal address counter, there are orderly and sequential transitions from self-refreshing to $\overline{CAS}$ before $\overline{RAS}$ refreshing and back to self-refreshing. Ensuring that the row addresses are refreshed in a timely fashion is the function of the refresh counter, which is clocked by $\overline{CAS}$ before $\overline{RAS}$ during normal cycles and at the rate of $1/(19 \times t_{RCF})$ during self-refresh cycles. The μPD42601 runs cooler than other self-refreshing devices and does not require a burst of extra $\overline{CAS}$ before $\overline{RAS}$ cycles before self-refreshing to ensure data integrity.

Figure 5. Special Requirements for t_{RCF} Near Periods of Limited Standard Refresh Cycles



Notes:

[1] The value for t_{RCF} [min] is specified in AC Characteristics. The value for t_{RCF} [max] is dependent upon temperature and shown in the table below.

	t_{RCF} [max]	
T_A	μPD42601-L	μPD42601
50°C	20 μs	5 μs
60°C	10 μs	5 μs
70°C	5 μs	5 μs

[2] When exiting self-refresh to a period of read and write operation which includes CBR refresh cycles, t_{RCF} is the delay between the last self-refresh pulse and the first CBR cycle. When entering self-refresh operation, t_{RCF} is the delay between the last CBR cycle and the first self-refresh pulse.

[3] In this period of normal read/write operation, there are no CBR refresh cycles or less than 512 $\overline{RAS}$-only refresh cycles.

[4] The time delay between the last self-refresh pulse in one self-refresh cycle, and the first self-refresh pulse in the next cycle, is defined by t_{RCF} [max] when the intervening period of read and write operation meets the conditions in Note 3.

[5] The built-in counter generates the refresh address in self-refresh and CBR refresh cycles. Since this address increments sequentially from the last cycle in either self-refresh or CBR operation to the first cycle in the alternate refresh mode, CBR refreshing should be used during normal read and write operation to refresh one address location every 62 μs or less. If some other means of refreshing is used, it is necessary to do a burst refresh of all storage cells just before changing to and just after exiting self-refresh operation.

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As discussed earlier, a lower die temperature permits both a relaxed refresh rate and simplified transition timing between self-refresh and normal write and read cycles. The die temperature is a function of the ambient temperature, operating power, and the junction-to-ambient thermal resistance (θ_{JA}). The calculations showing the increase of junction temperature (T_J) over ambient temperature (T_A) at maximum power consumption (P_D max) are shown in the sequence below.

(1) $T_J = (\theta_{JA} \times P_D) + T_A$

(2) $T_J = [95\,°C/W \times (5.5\,V \times 12\,mA)] + 55\,°C$

(3) $T_J = 61.27\,°C$

In a solid-state disk system where the air temperature stabilizes at 55 °C, the silicon file chip temperature would not exceed 61.27 °C, comparing favorably with the die temperature of 81 °C or more for a standard DRAM encapsulated in a plastic SOJ and operating in similar conditions.

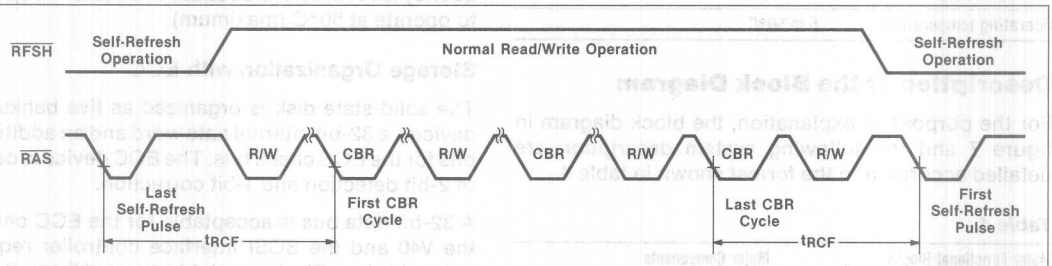
Figure 6 shows the maximum specification for t_{RCF}, the critical parameter when transitioning between $\overline{CAS}$ before $\overline{RAS}$ and self-refresh cycles. When exiting self-refresh operation, t_{RCF} (max) is measured between the falling edges of $\overline{RAS}$, from the last self-refresh cycle to the first $\overline{CAS}$ before $\overline{RAS}$ refresh cycle. After transitioning from self-refresh operation to a period of normal write or read cycles, writing and reading can proceed for only 5 μs (at 70 °C) before a $\overline{CAS}$ before $\overline{RAS}$ refresh cycle is required. When transitioning from write and read operation to self-refresh operation, the process is simply reversed, with t_{RCF} (max) referenced between the last $\overline{CAS}$ before $\overline{RAS}$ refresh cycle and the first self-refresh cycle.

$\overline{RAS}$-only refreshing does not increment the refresh counter, complicating the procedure for moving between refresh modes. In refresh methods other than $\overline{CAS}$ before $\overline{RAS}$, a burst of 512 refresh cycles is required before entering and also after exiting self-refresh operation. Complete refreshing of all rows is needed since, in refresh modes other than $\overline{CAS}$ before $\overline{RAS}$, the status of the refresh counter is unknown and the maximum specification for t_{RCF} may be exceeded. When the self-refresh capability is used, then $\overline{CAS}$ before $\overline{RAS}$ refreshing is recommended.

Soft Error Performance

Like the 1M x 1 DRAM, the μPD42601 uses the trench cell for a small die size and excellent immunity to alpha particles. Accelerated soft error results are less than 1000 FITs (Failures In Time, or errors in 10^9 device-hours) . With low manufacturing cost as an objective, the device includes no error correction circuit (ECC), parity, or data checking functions on-chip. Most customers prefer to implement these functions off-chip.

Figure 6. Timing Restrictions Entering and Exiting Self-Refresh Operation



Notes:

[1] The value for t_{RCF} [min] is specified in AC Characteristics. The value for t_{RCF} [max] is dependent upon temperature and shown in the table below.

	t_{RCF} [max]	
T_A	μPD42601-L	μPD42601
50 °C	20 μs	5 μs
60 °C	10 μs	5 μs
70 °C	5 μs	5 μs

[2] When exiting self-refresh to a period of read and write operation which includes CBR refresh cycles, t_{RCF} is the delay between the last self-refresh pulse and the first CBR cycle. When entering self-refresh operation, t_{RCF} is the delay between the last CBR cycle and the first self-refresh pulse.

[3] The built-in counter generates the refresh address in self-refresh and CBR refresh cycles. Since this address increments sequentially from the last cycle in either self-refresh or CBR operation to the first cycle in the alternate refresh mode, CBR refreshing should be used during normal read and write operation to refresh one address location every 62 μs or less. If some other means of refreshing is used, it is necessary to do a burst refresh of all storage cells just before changing to and just after exiting self-refresh operation.

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3

Silicon File-Based Solid-State Disk System

To assist our customers in the design-in of the μPD42601, NEC undertook a 20-Mbyte solid-state disk hardware project, a block diagram of which appears in figure 7 and a photograph in figure 8 (the hardware enclosure was designed for expansion to 40 Mbytes). Contained within the same package form factor as a 5.25-inch Winchester, the solid-state disk system includes batteries, a power supply, and the necessary power fail logic to provide complete nonvolatility for up to one month. The error correction device is a gate array developed at NEC and is not commercially available. A specification summary of this application project is shown in table 3.

Table 3. Specification Summary

Parameter	Specification
Capacity	20 Mbytes
Interface	SCSI (host)
Data transfer rate	1.5 Mbytes/sec (max)
Access time	0.1 ms (max)
Error correction	1-bit correction and 2-bit detection
Sector size	256 or 512 bytes
Power supply	5 volts, 2 amps
Package size	5.25-inch disk
Battery voltage	4.8 volts
Battery backup	One month
Operating temperature	5 to 50°C

Description of the Block Diagram

For the purpose of explanation, the block diagram in figure 7 and the following system description are detailed according to the format shown in table 4.

Table 4.

Major Functional Blocks	Major Components
Power source/switch	Battery, power control circuits
Silicon file and ECC	μPD42601LA, ECC gate array
Timing generator circuits	$\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$ logic
Data/address control	V40™, WD33C93™, RAM, ROM

Power Supply and Power Fail Circuits

The upper left corner of the block diagram consists of the battery, power switch, voltage detector, and power fail circuits. Included in the power switch is a 5-volt switching regulator and the power conversion circuits. When the detector senses the falling power supply voltage, the power switch supplies the battery voltage to the components shown within the shaded block (battery backup). At the same time, the power fail logic sends a nonmaskable interrupt (NMI) to the V40, which initiates an internal subroutine and places the microprocessor in the low-current HALT mode.

When system power is restored, the rising voltage is detected. After a delay, the power switch disconnects the battery source and allows the 5-volt supply to power the system. Once the V40 receives the second NMI and resets the processor, $\overline{RFSH}$ goes inactive and normal timing resumes.

To ensure nonvolatility and reduced battery current drain, the silicon file devices must be placed in self-refresh operation when system power fails. In figure 7, the power fail logic has two outputs: one called self-refresh, which pulls $\overline{RFSH}$ low on all the storage chips, and a second output connected to the control pins of the V40 and the timing generator block. This output is actually two lines: one for the V40 NMI input initializing HALT mode and the second for initializing the timing generator circuits. When this output signal is active, the power fail logic switches the timing for $\overline{RAS}$ from normal read/write/refresh timing to the self-refresh oscillator. For this application, the self-refresh frequency is set at 50 kHz because this system is specified to operate at 50°C (maximum).

Storage Organization with ECC

The solid-state disk is organized as five banks of 39 devices, a 32-bit internal data word and an additional 7 bits for the ECC check bits. The ECC device is capable of 2-bit detection and 1-bit correction.

A 32-bit data bus is acceptable for the ECC chip, but the V40 and the SCSI interface controller require a byte-wide bus. The lower right corner of figure 7 shows a four-section register to accomplish this 32- to 8-bit conversion. This register is composed of eight octal bus transceivers with eight enable lines generated in the timing generator block. Four of these transceivers are used for the input side and four are used for the output side. The four octal bus transceivers (4 x 8 bits) comprise the 32-bit-wide data bus. The enable signals select one of the four transceivers receiving and sending each byte to or from the 8-bit data bus.

V40 is a trademark of NEC Corporation.
WD33C93 is a trademark of Western Digital.

Figure 7. Block Diagram of Silicon File Disk

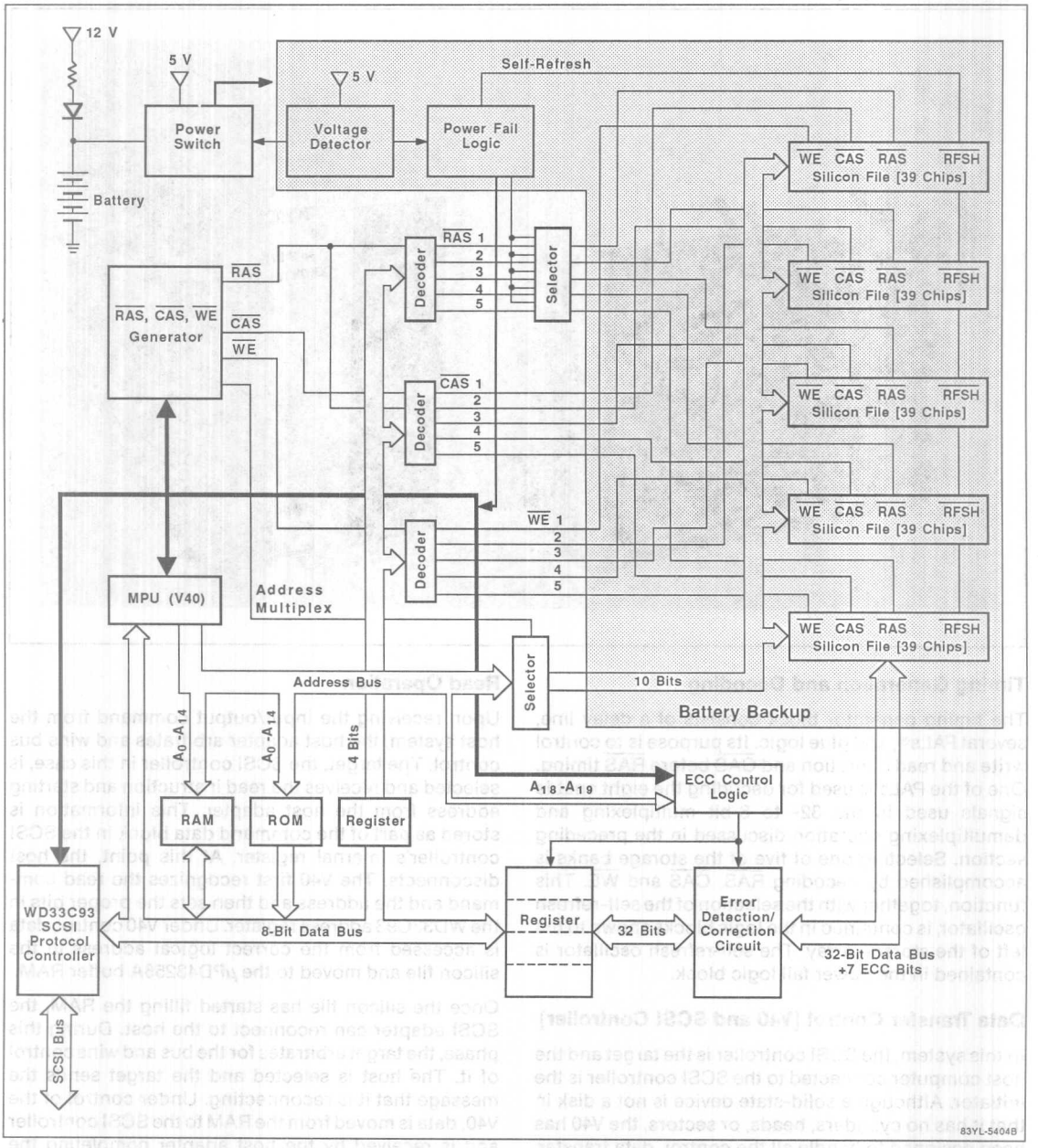
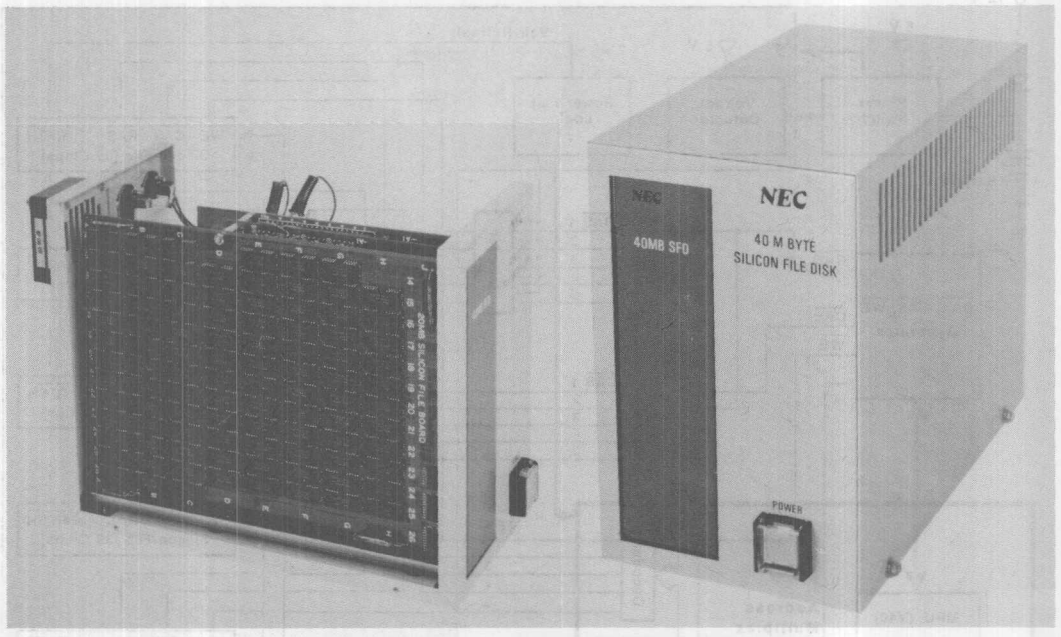


Figure 8. Photograph of Silicon File Disk



Timing Generation and Decoding

The timing generator block consists of a delay line, several PALs®, and glue logic. Its purpose is to control write and read operation and $\overline{CAS}$ before $\overline{RAS}$ timing. One of the PALs is used for decoding the eight enable signals used in the 32- to 8-bit multiplexing and demultiplexing operation discussed in the preceding section. Selecting one of five of the storage banks is accomplished by decoding $\overline{RAS}$, $\overline{CAS}$ and $\overline{WE}$. This function, together with the selection of the self-refresh oscillator, is contained in the logic blocks shown to the left of the storage array. The self-refresh oscillator is contained in the power fail logic block.

Data Transfer Control [V40 and SCSI Controller]

In this system, the SCSI controller is the target and the host computer connected to the SCSI controller is the initiator. Although a solid-state device is not a disk in that it has no cylinders, heads, or sectors, the V40 has been designed to handle all the control, data transfer, and address translation functions. Used as a microcontroller, the V40 makes the silicon disk look like a magnetic disk to the WD33C93.

Read Operation

Upon receiving the input/output command from the host system, the host adapter arbitrates and wins bus control. The target, the SCSI controller in this case, is selected and receives the read instruction and starting address from the host adapter. This information is stored as part of the command data block in the SCSI controller's internal register. At this point, the host disconnects. The V40 first recognizes the read command and the address and then sets the proper bits in the WD33C93 address register. Under V40 control, data is accessed from the correct logical address in the silicon file and moved to the μPD43256A buffer RAM.

Once the silicon file has started filling the RAM, the SCSI adapter can reconnect to the host. During this phase, the target arbitrates for the bus and wins control of it. The host is selected and the target sends the message that it is reconnecting. Under control of the V40, data is moved from the RAM to the SCSI controller and is received by the host adapter completing the operation. With this fast semiconductor disk, the data transfer rate depends more on arbitration time than on device access time.

PAL is a registered trademark of Advanced Micro Devices, Inc.

NEC Electronics Inc.

APPLICATION NOTE 57
μPD41101/μPD41102/μPD42505
HIGH-SPEED LINE BUFFERS

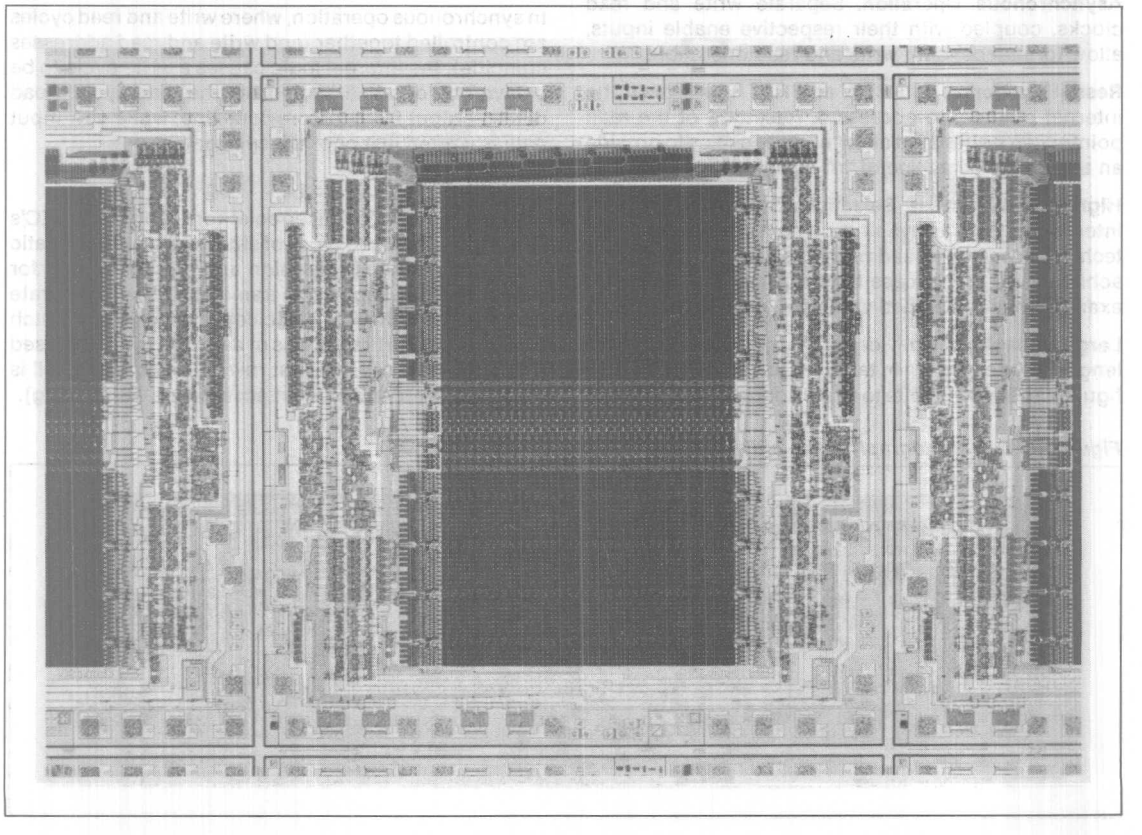
Introduction

The need for storage devices to provide delay and speed conversion in a variety of computer, telecommunication, and consumer applications has led to NEC's development of several new high-speed line buffers. The synchronous or asynchronous operation of these devices allows them to be used as elastic storage to synchronize data flow between two asynchronous parts of a system, e.g., between communication and microcomputer chips.

In graphics systems, line storage devices can act as high-speed source and destination registers during raster operations. In television and VCR products, the 1K x 8 buffers provide the raster line storage required for luminance and chrominance separation and non-interlaced scan conversion. The larger 5K x 8 devices are perfectly suited for facsimile and printer applications because they can store a line of information or a page of text at high speed.

This application note describes NEC's μPD41101, μPD41102 and μPD42505, three functionally equivalent buffers with different capacities and speeds. Each device has independent, 1-byte write and read ports with separate write and read clocks. High-speed performance is achieved by means of unique circuitry rather than a submicron process. Fast access times

Figure 1. Die Photograph of the μPD41101 and μPD41102



The μPD42101 and μPD42102 exactly replace the μPD41101 and μPD41102.

and low cost are possible because of specialized dynamic circuit designs using the best of MOS technology (figures 1 and 2).

Features

The μPD41101, μPD41102, and μPD42505 are identical except in organization and cycle times (table 1). The following discussion applies to the three devices collectively, unless noted otherwise.

Serial Addressing. Addresses are generated automatically by an internal address counter and need not be supplied externally. The clocks provided by the WCK and RCK signals increment the respective write and read address counters, enabling data to be read out in the order in which it was input.

Wraparound Addresses. The internal address pointers are implemented as ring counters; they return to address 0 after the last byte in a line has been accessed.

Asynchronous Operation. Separate write and read clocks, coupled with their respective enable inputs, allow for independent write and read operation.

Reset Function. The $\overline{\text{RSTW}}$ and $\overline{\text{RSTR}}$ pins reset the internal pointers to address 0. Resetting of the read pointer can be initiated after "n" write cycles to provide an adjustable delay line of "n" cycles.

High-Speed Address Selection. By interleaving the internal storage arrays and using a novel pipelining technique for high-speed address selection, the devices achieve very fast access times. The μPD41102-3, for example, has a specified minimum cycle time of 28 ns.

Large Capacity. All devices are 1-byte wide. Their line lengths vary as shown in table 1. The μPD42505 is configured as 5048 by 8 bits to store a page of information.

Table 1. Configurations and Cycle Times

Part Number	Organization	Cycle Times
μPD41101	910 x 8 bits	34 or 69 ns
μPD41102	1135 x 8 bits	28, 34, or 56 ns
μPD42505	5048 x 8 bits	50 or 75 ns

Functional Description

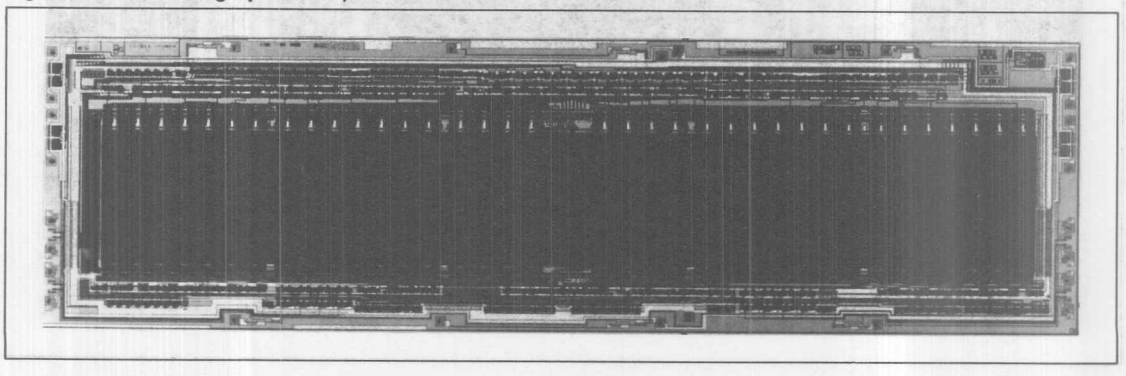
Historically, line buffers were designed with shift registers that suffered from fall-through delay as data tumbled down the stack. With NEC's new generation of buffers, which provide independent write and read clocks for asynchronous writing and reading, the write data requires a delay of at least 10 or 11 cycles before appearing at the output. The minimum line delay (specified in the individual data sheets for each device) is not a problem in most applications because the required delay is usually longer than the specified minimum delay.

In synchronous operation, where write and read cycles are controlled together (and write and read addresses coincide), the internal logic causes a write cycle to be delayed by one-half cycle from the read cycle. Read data is output from the previous line, while new input data is written just one-half cycle later.

Storage Arrays

Unlike other devices based solely on static cells, NEC's line buffers have two types of storage elements: a static cell for high-speed operation and a dynamic cell for achieving large capacity in a small die area. To operate at high speed, the fast static cell is used as a prefetch buffer. While the first 8 bytes of data are being accessed from the static cell, the first row of the dynamic cell is preselected for subsequent access (see **Addressing**).

Figure 2. Die Photograph of the μPD42505



The μPD42101 and μPD42102 exactly replace the μPD41101 and μPD41102.

Figure 3. Dual-Port Static Storage Cell Array

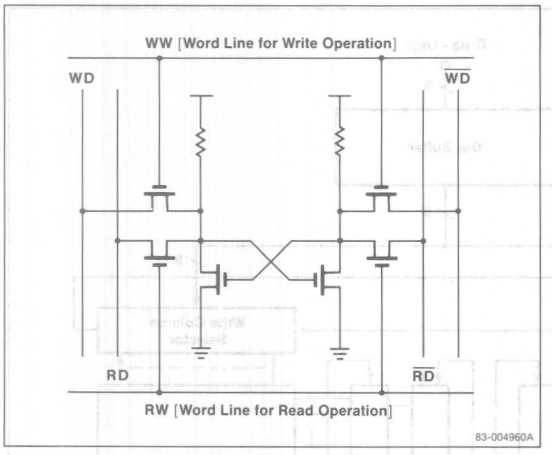
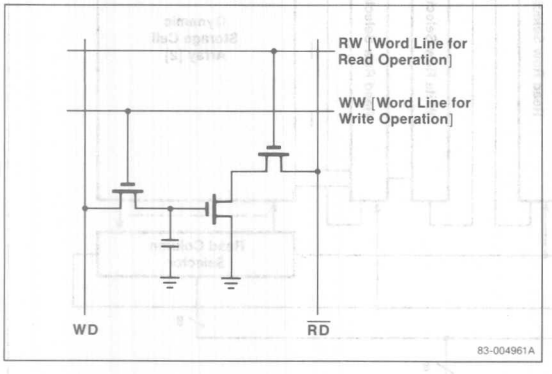


Figure 4. Dual-Port Dynamic Storage Cell Array



The static storage cell has separate word lines for write and read cycles (RW and WW), as well as differential data inputs (RD/$\overline{RD}$ and WD/$\overline{WD}$) for high-speed operation (figure 3). The three-transistor, one-capacitor dynamic storage cell contains separate write and read data and word lines, two access transistors, and a third transistor for cell signal pre-amplification (figure 4). Pre-amplification is required since there are only eight data amplifiers, one each for the eight input/output ports.

Unlike the static cell, the dynamic cell uses only one write and read data line and cannot take advantage of differential sensing. Although the speed is slower, its fewer components make this cell more suitable for compact layout and high device integration. The success of these high-speed buffers lies in the matching of the static and dynamic cells to achieve high performance at a low cost (figure 5).

Addressing

On a cold start, initial writing and reading to the device requires fast access times from the six-transistor static cell. While the first eight bytes are being accessed from the static cell, the first row of the dynamic cell is preselected. To achieve relatively fast dynamic access, the dynamic array is split into two segments and storage interleaving is employed.

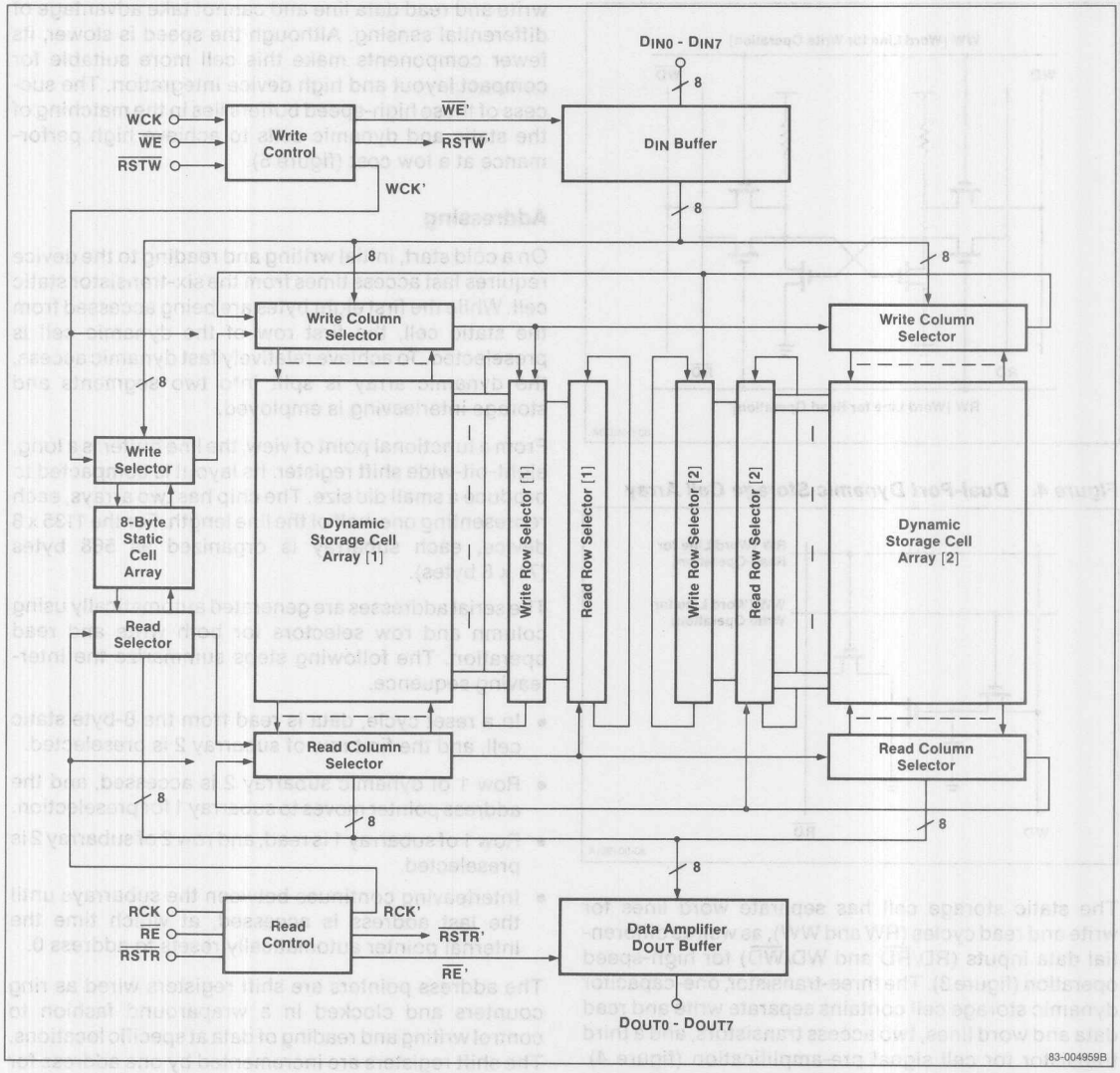
From a functional point of view, the line buffer is a long, eight-bit-wide shift register. Its layout is compacted to produce a small die size. The chip has two arrays, each representing one-half of the line length. For the 1135 x 8 device, each subarray is organized as 568 bytes (71 x 8 bytes).

The serial addresses are generated automatically using column and row selectors for both write and read operation. The following steps summarize the interleaving sequence.

- In a reset cycle, data is read from the 8-byte static cell, and the first row of subarray 2 is preselected.
- Row 1 of dynamic subarray 2 is accessed, and the address pointer moves to subarray 1 for preselection.
- Row 1 of subarray 1 is read, and row 2 of subarray 2 is preselected.
- Interleaving continues between the subarrays until the last address is accessed, at which time the internal pointer automatically resets to address 0.

The address pointers are shift registers wired as ring counters and clocked in a wraparound fashion to control writing and reading of data at specific locations. The shift registers are incremented by one address for each WCK or RCK clock. Separate write and read address pointers are required to execute write and read cycles independently and at different speeds.

Figure 5. Block Diagram



The μPD42101 and μPD42102 exactly replace the μPD41101 and μPD41102.

Write and Read Timing

The μPD41101, μPD41102, and μPD42505 are equipped with the following pins: D_{IN0} through D_{IN7}, $\overline{RSTW}$, $\overline{WE}$, and WCK for write operation and D_{OUT0} through D_{OUT7}, $\overline{RSTR}$, $\overline{RE}$, and RCK for read operation (figures 6 and 7). Serial addresses are automatically generated by an internal address counter. When $\overline{WE}$ is low, one byte is written to each address in synchronization with the WCK write clock (refer to the individual data sheets for timing diagrams); the internal write address pointer increments by 1 with each falling edge of WCK. Write data must meet the specified setup and hold times as measured from the rising edge of WCK.

Figure 6. Configuration of 24-Pin Plastic DIP (and Miniflat for μPD41101, μPD41102 only)

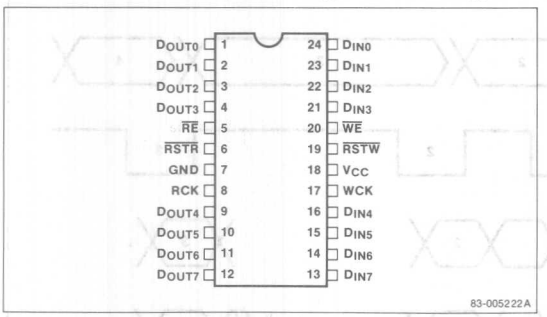
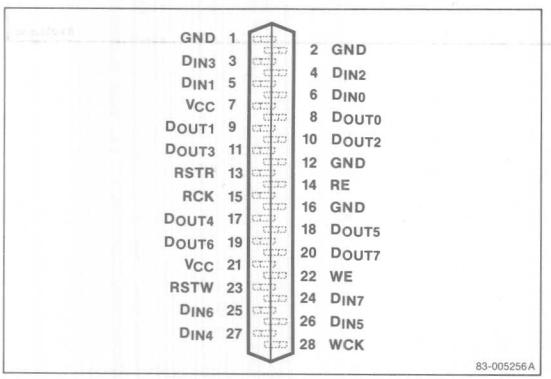


Figure 7. Configuration of 28-Pin Plastic ZIP (μPD42505 only)



The signal on $\overline{RSTW}$, which is used to reset the write address pointer to 0, also has setup and hold requirements with respect to the write clock.

When the signal on the read enable ($\overline{RE}$) pin is low, one byte of data is read out of the device for each RCK clock cycle, and the read address pointer increments by 1. The read address pointer is totally independent of the write address pointer.

The control functions of $\overline{WE}$ and $\overline{RE}$ are shown in figure 8. Bringing these two signals high (inactive) stops the internal address pointers; activating them again causes the internal pointers to increment to the next sequential address.

Synchronous Operation

Figure 8 shows the internal timing sequences, including those for address transitions and write cycles, during synchronous operation of these devices. With a common write and read clock, the internal write period is delayed from the write address. This delay, required when the write and read addresses are identical, allows a read cycle and then a write cycle to be executed to the same cell location. Read data is taken from the previously written line.

Designing with NEC's Line Buffers

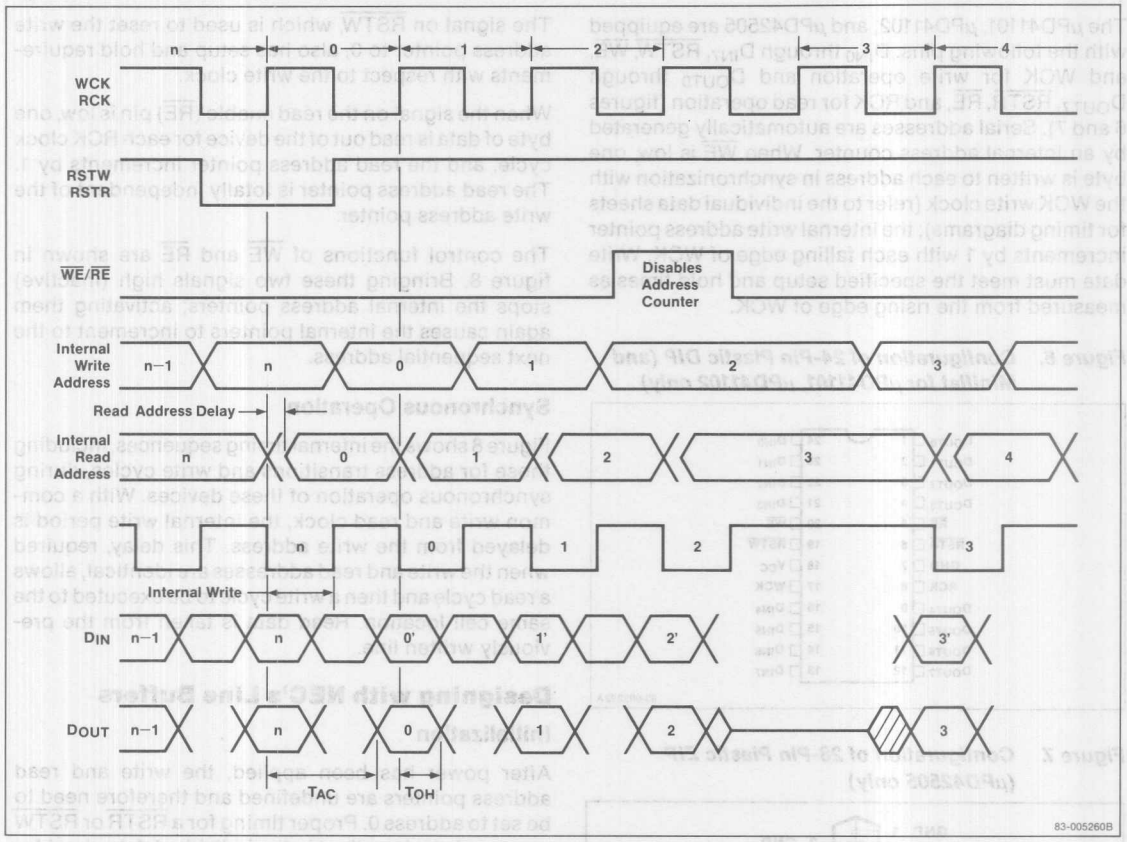
Initialization

After power has been applied, the write and read address pointers are undefined and therefore need to be set to address 0. Proper timing for a $\overline{RSTR}$ or $\overline{RSTW}$ reset cycle is described in the individual data sheet for each device.

Refreshing

Refreshing of the dynamic storage cells must be performed at regular intervals. Data remains valid for 1 or 5 ms, depending on the line length of the device (1 ms for the μPD41101 or μPD41102 and 5 ms for the μPD42505). Since NEC's line buffers contain only data amplifiers and no sense amplifiers, a standard read cycle does not refresh the storage cell. If longer hold times are required, the original data must be rewritten to the same address.

Figure 8. Internal Timing for Synchronous Operation



The μPD42101 and μPD42102 exactly replace the μPD41101 and μPD41102.

Minimum Delay Length

Unlike register-based line buffers, which use a data flow-through cycle, NEC's line storage elements are not capable of reading data immediately after it has been written. Each device requires a minimum delay, as calculated by the equations shown in table 2.

Table 2. Calculating Minimum Delay

Part Number	Equation
μPD41101	1/2 write cycle + 300 ns (34 ns/2 + 300 ns)/34 = 9.3 or 10 cycles
μPD41102	1/2 write cycle + 300 ns (28 ns/2 + 300 ns)/28 = 11.2 or 12 cycles
μPD42505	1/2 write cycle + 500 ns (50 ns/2 + 500 ns)/50 = 10.5 or 11 cycles

Delay length, as measured by the number of cycles, is dependent on the speed of the clock, i.e., at 14.3 MHz, the minimum delay for the μPD41101 would be 5 cycles.

Storage Contention

In asynchronous operation, when write and read cycles contend for the same line, the last "n" bytes (where "n" may be 5-12 bytes) of line output are taken from the previous line. This type of contention occurs most frequently when executing continuous write and read cycles at different rates, such as when converting video images from interlaced to noninterlaced scanning. In this case, the read clock operates at twice the speed of the write clock. Near the end of the line, the read cycle catches up and contends with the write cycle.

Setting Delay Length

Varying the Reset Interval in Synchronous Operation. Depending on the application, some schemes for implementing delay length suit system timing better than others (see individual data sheets for timing). In synchronous operation, the delay is set simply by varying the interval between the reset pulses. In this case, the reset clocks are tied together. Since write and read clocks are common, line delay is determined by the offset between resets.

Varying the Reset Interval in Asynchronous Operation. In asynchronous operation, the reset interval can be varied using independent clocks and reset signals. Delay length is calculated as the timing difference between the write and read reset pulses.

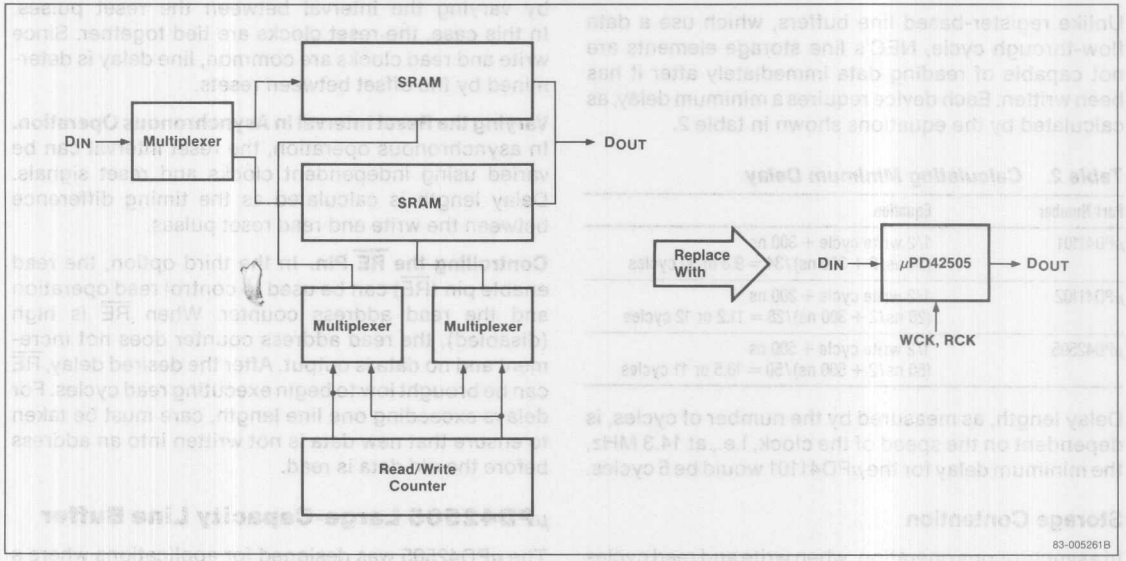
Controlling the $\overline{RE}$ Pin. In the third option, the read enable pin ($\overline{RE}$) can be used to control read operation and the read address counter. When $\overline{RE}$ is high (disabled), the read address counter does not increment and no data is output. After the desired delay, $\overline{RE}$ can be brought low to begin executing read cycles. For delays exceeding one line length, care must be taken to ensure that new data is not written into an address before the old data is read.

μPD42505 Large-Capacity Line Buffer

The μPD42505 was designed for applications where a large amount of data is handled per line, e.g., in high-performance digital copiers and G3 or G4 facsimile machines requiring buffer storage for image compression, expansion, data transmission, and in some cases, image enhancement using filtering techniques for digital signal processing. The 5K x 8 line length has also been used in some designs to hold the data tokens in digital filtering arrays.

Although line buffering can be achieved using fast static RAMs as shown in figure 9, the need for two devices and other complicated peripheral circuits necessarily increases the cost of a system and makes it more difficult to implement. The μPD42505 eliminates the complexity and high cost by providing the same functions and more advantages in one package.

Figure 9. System Design Using Static RAMs Versus High-Speed Line Buffer



The μPD42101 and μPD42102 exactly replace the μPD41101 and μPD41102.

Figure 10. Line Buffering in Local Area Networks

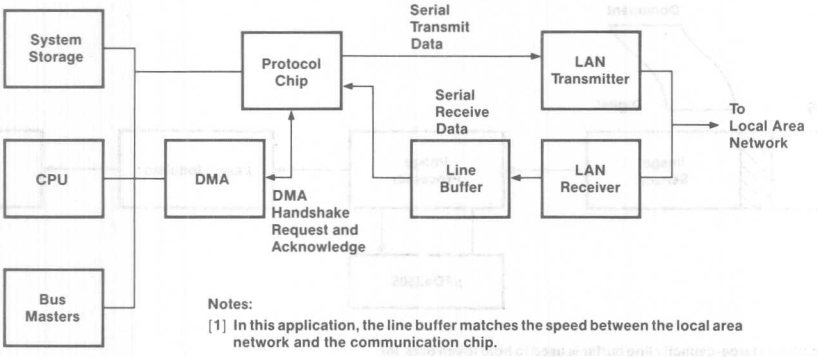
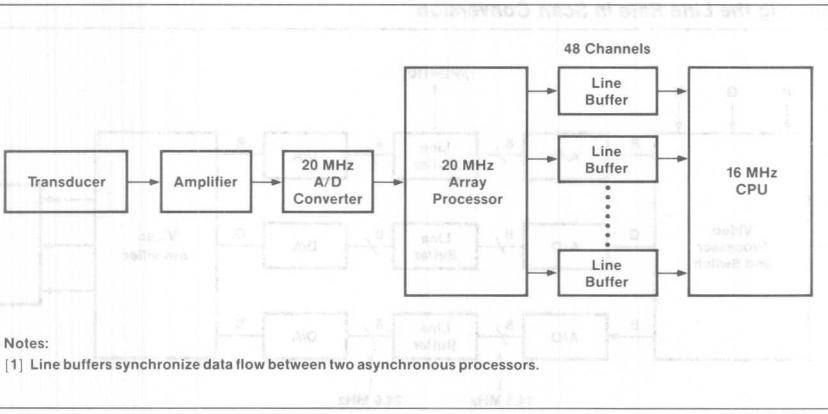
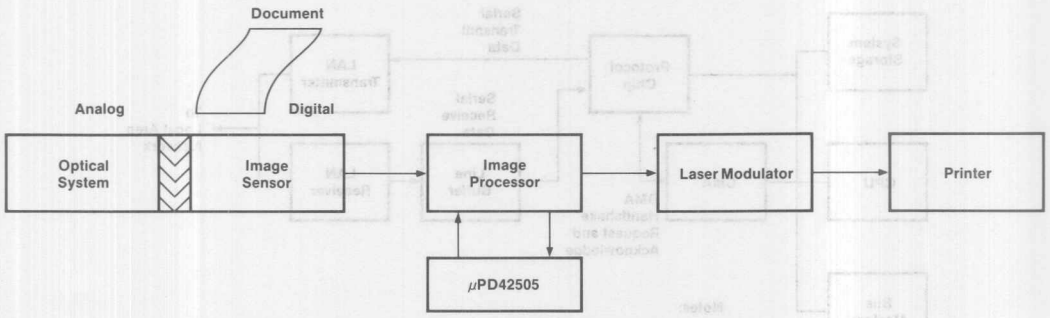


Figure 11. Elastic Storage for Digital Signal Processing Applications



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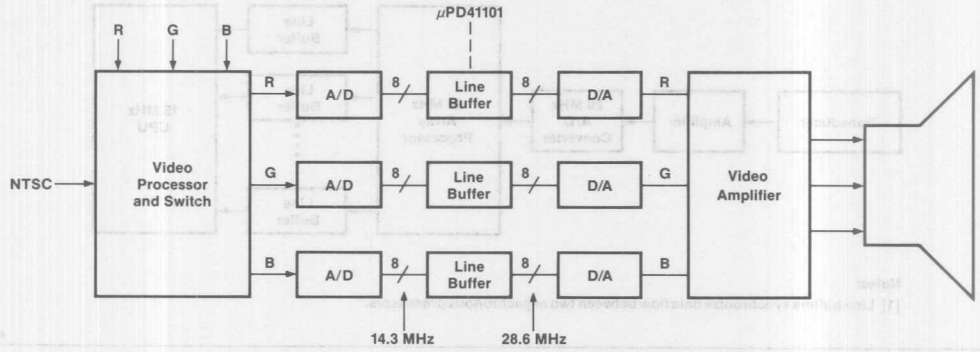
Figure 12. Image Enhancement Techniques in High-Performance Digital Copiers



Notes:
[1] In this application, a large-capacity line buffer is used to hold token data for digital signal processing.

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Figure 13. Doubling the Line Rate in Scan Conversion



Notes:
[1] In high-definition TV applications, the line buffer is used to double the scan rate by reading at twice the write frequency.

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The μPD42101 and μPD42102 exactly replace the μPD41101 and μPD41102.

NEC Electronics Inc.

APPLICATION NOTE 58
INTERLACED TO NONINTERLACED VIDEO SCANNING USING THE μPD41101 HIGH-SPEED LINE BUFFER

Introduction

Interlaced scanning is used in television, videotape, and videocassette recording applications to reduce bandwidth and maintain an acceptable amount of screen flicker in video signals. The procedure involves lowering the vertical resolution and doubling the number of fields so that one complete frame is formed from the first and second fields. When a video signal subsequently is decoded and ready for display on a monitor or TV, bandwidth generally is no longer a problem and the higher vertical resolution of a noninterlaced signal may be used to produce a sharper image on the screen.

In NTSC TV systems, there are 262.5 scan lines per field, 2 fields per frame, and 30 frames per second (figure 1). With the resolution per field in the vertical direction lowered by interlaced scanning, the lines become rougher and the gap between scanned lines more visible. This drawback becomes all the more conspicuous in larger-screen TVs.

Vertical resolution problems caused by interlaced scanning can be resolved by first repeating the signal of each scan line. The number of scan lines per field then can be doubled by doubling the horizontal frequency and keeping the vertical frequency intact. Subsequently, an interlaced signal can be converted to a noninterlaced signal to increase the resolution of the picture in the vertical direction (figure 2).

The conversion from interlaced to noninterlaced scanning can be achieved by temporarily storing each line in a buffer and then displaying it twice to double the number of lines per field (figure 3).

Figure 1. Relationship of Field to Frame in Interlaced Scanning

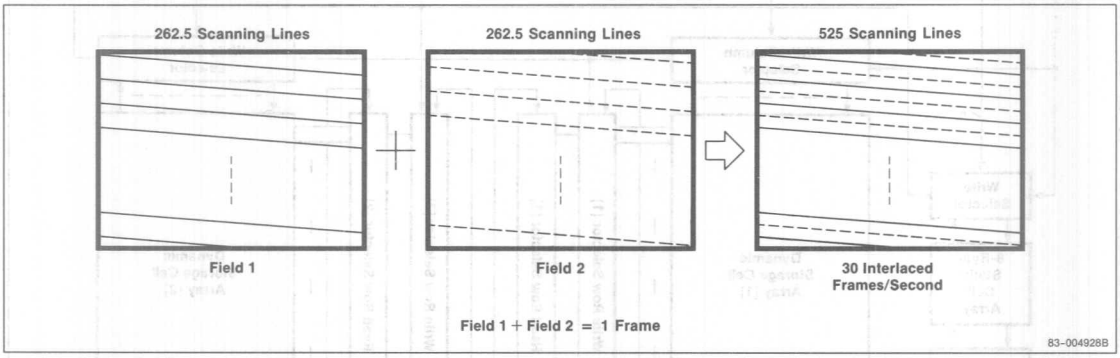
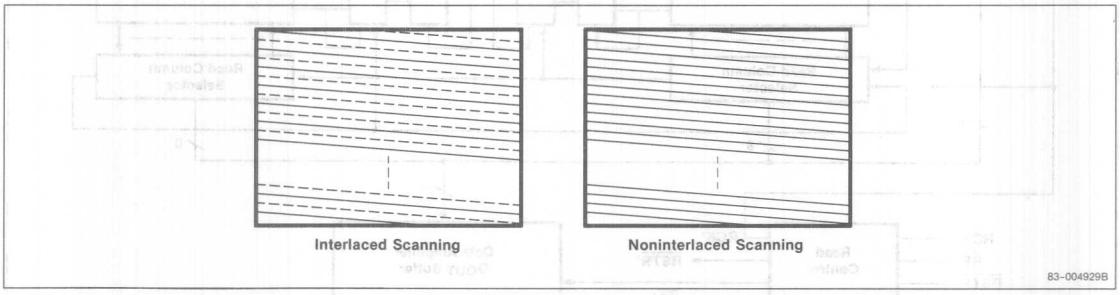


Figure 2. Difference Between Interlaced and Noninterlaced Scanning



The μPD42101 and μPD42102 exactly replace the μPD41101 and μPD41102.

Figure 3. Doubling the Line Rate

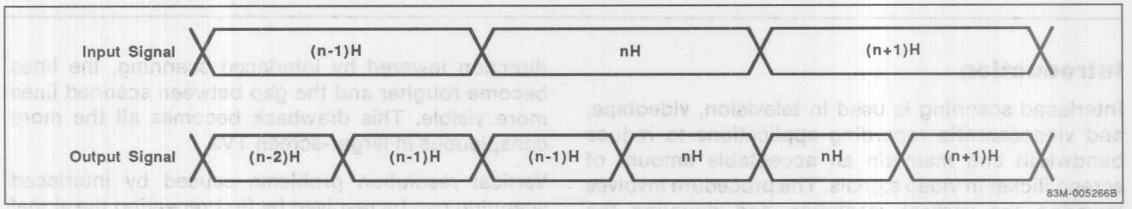
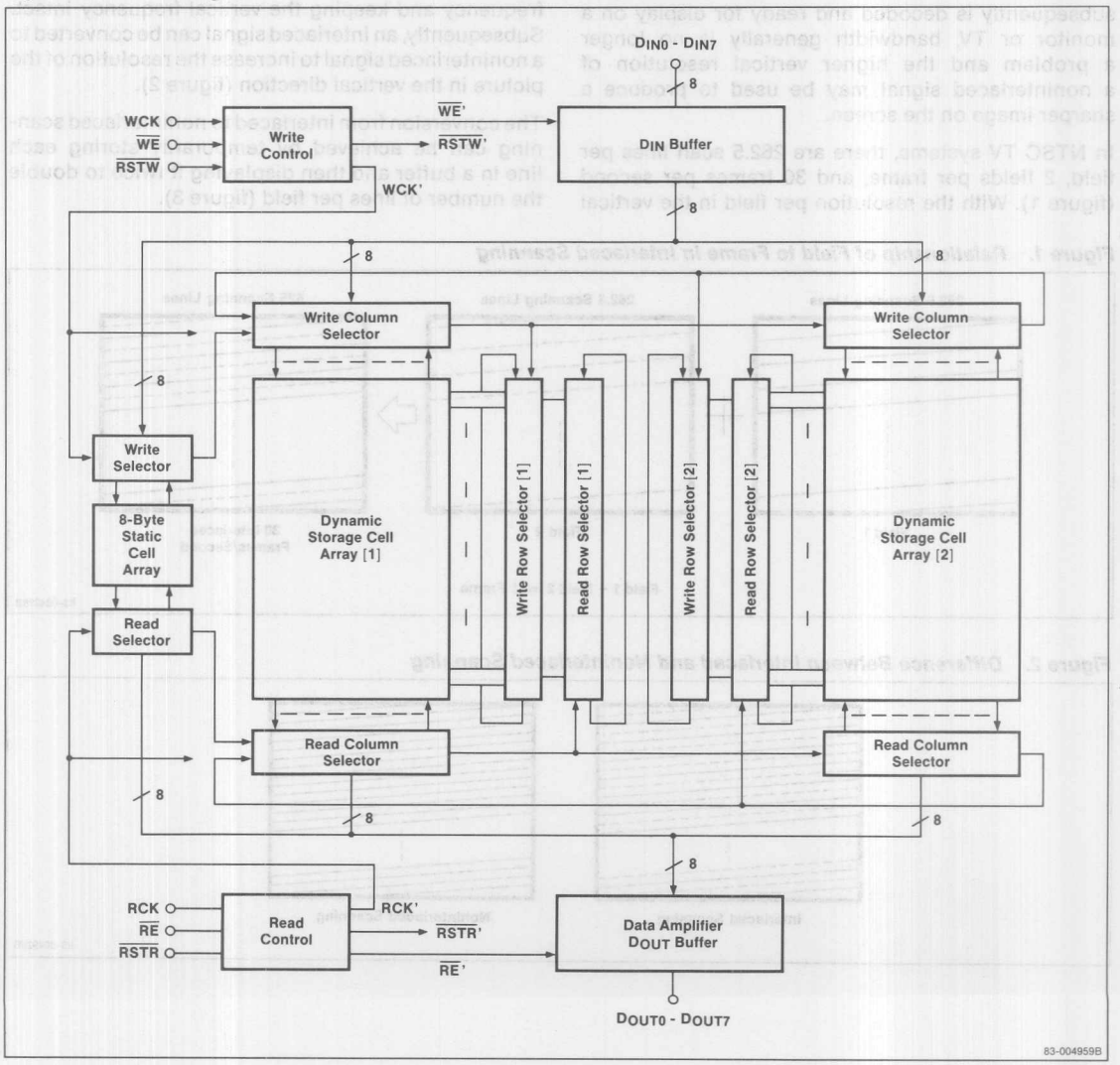


Figure 4. Block Diagram



The μPD42101 and μPD42102 exactly replace the μPD41101 and μPD41102.

The μPD41101 High-Speed Line Buffer

The type of scan conversion described in this application note requires buffer storage for each line. Required storage is calculated by dividing the scanning period per line by the sampling period to determine the number of samples per line. Required storage for NTSC systems is computed as shown in the following sequence.

(1) Scanning period per line:

$$\frac{1}{\frac{(525 \text{ lines}}{\text{frame}} \times \frac{30 \text{ frames})}{\text{second}}} = 63.5\ \mu s$$

(2) Minimum sampling frequency:

$$3.58 \text{ MHz} \times 4 = 14.32 \text{ MHz} = 69.83 \text{ ns}$$

(3) Samples per line:

$$63.5\ \mu s / 69.8 \text{ ns} = 909.7 \text{ samples}$$

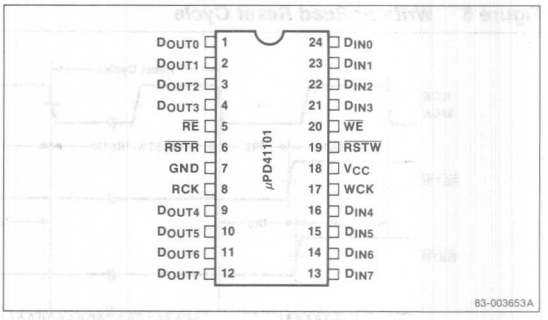
This application requires the storing of 910 words, exactly one horizontal scanning line of data. NEC's μPD41101 high-speed line buffer, configured as 910 words by 8 bits, is ideally suited for the digital processing of video signals because one-line delays and time axis conversions can be executed easily.

The μPD41101 differs from general-purpose static devices in that it doesn't require a double-buffer configuration (figure 4). Writing and reading can be executed independently and asynchronously. Since an internal address pointer eliminates the need for external address generation, the only external controls required are those for the WCK and RCK write and read clocks and the $\overline{\text{RSTW}}$ and $\overline{\text{RSTR}}$ write and read reset signals (see figure 5 for pin assignments). As shown in table 1, three versions of the μPD41101 are available.

Table 1. Access and Cycle Times of the μPD41101

Part Number	Access Time (max)	Write Cycle Time (min)	Read Cycle Time (min)
μPD41101-3	27 ns	34 ns	34 ns
μPD41101-2	27 ns	69 ns	34 ns
μPD41101-1	49 ns	69 ns	69 ns

Figure 5. μPD41101 Pin Configuration



Operation

Write and Read Reset Cycles. After power is applied to the μPD41101, its internal address pointers are undefined and must be initialized to address 0. As shown in figure 6, the inputs on $\overline{RSTW}$ and $\overline{RSTR}$ have required setup and hold times as measured from the rising edges of WCK and RCK, respectively.

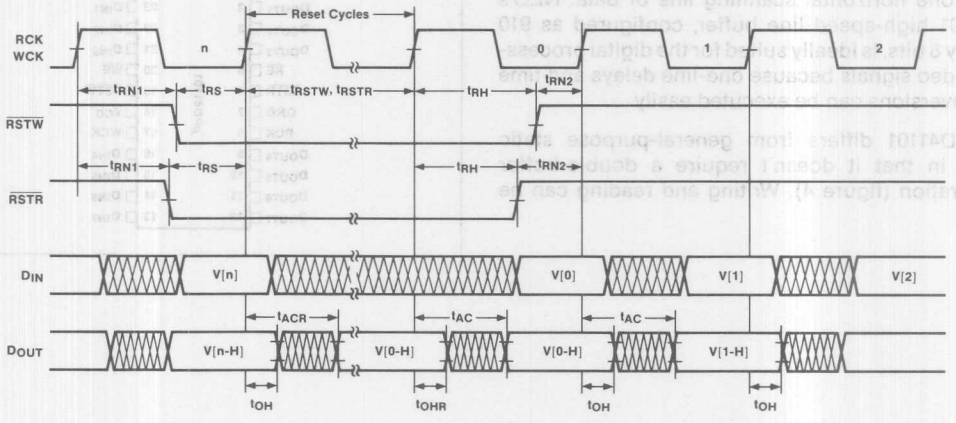
Write Cycles. Write cycles are executed in synchronization with the WCK clock (figure 7). When $\overline{WE}$ is low, 8 bits of data are sampled from D_{IN0}-D_{IN7} at the rising edge of WCK and the internal write pointer increments to the next sequential address. When the pointer reaches the last address, it wraps around to address 0 again. When high, $\overline{WE}$ disables write operation and inhibits the write address pointer. Write data must satisfy required setup and hold times as specified from the rising edge of WCK.

Read Cycles. When $\overline{RE}$ is low, read cycles are executed in synchronization with the RCK clock (figure 7). Read data is output from D_{OUT0}-D_{OUT7} after a specified access time as measured from the rising edge of RCK. The internal read pointer functions identically to the write pointer, except that the read address increments sequentially with each RCK clock.

Example of System Configuration

The block diagram in figure 8 shows a hardware system designed to convert a standard NTSC interlaced video signal to a noninterlaced signal. In this configuration, described on the following pages, the input signals derive either from an NTSC composite signal (video input), from a TV/VTR/VCR, or from the R-G-B signal output of a personal computer.

Figure 6. Write or Read Reset Cycle

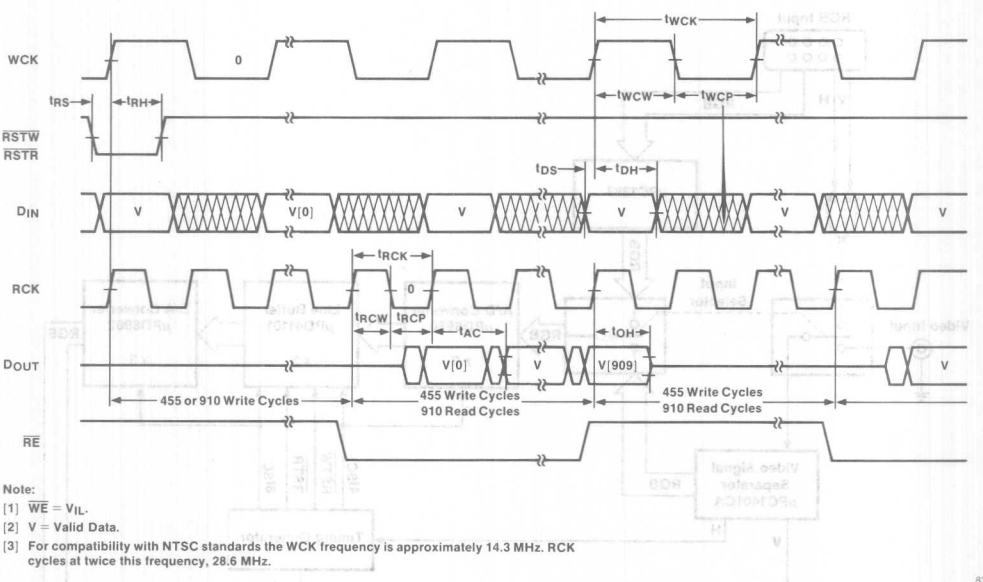


Note:
[1] $\overline{WE} = \overline{RE} = V_{IL}$.
[2] V = Valid Data.
[3] Read operations commence from the rising edge of RCK at the beginning of a cycle. For the first cycle in a group of reset cycles, the read access time is defined as t_{ACR}. In all other cycles, t_{AC} defines the read access time.
[4] H = 910 cycles.
[5] Write data is strobed into the device on the rising edge of WCK at the end of a cycle.

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The μPD42101 and μPD42102 exactly replace the μPD41101 and μPD41102.

Figure 7. Write or Read Cycle

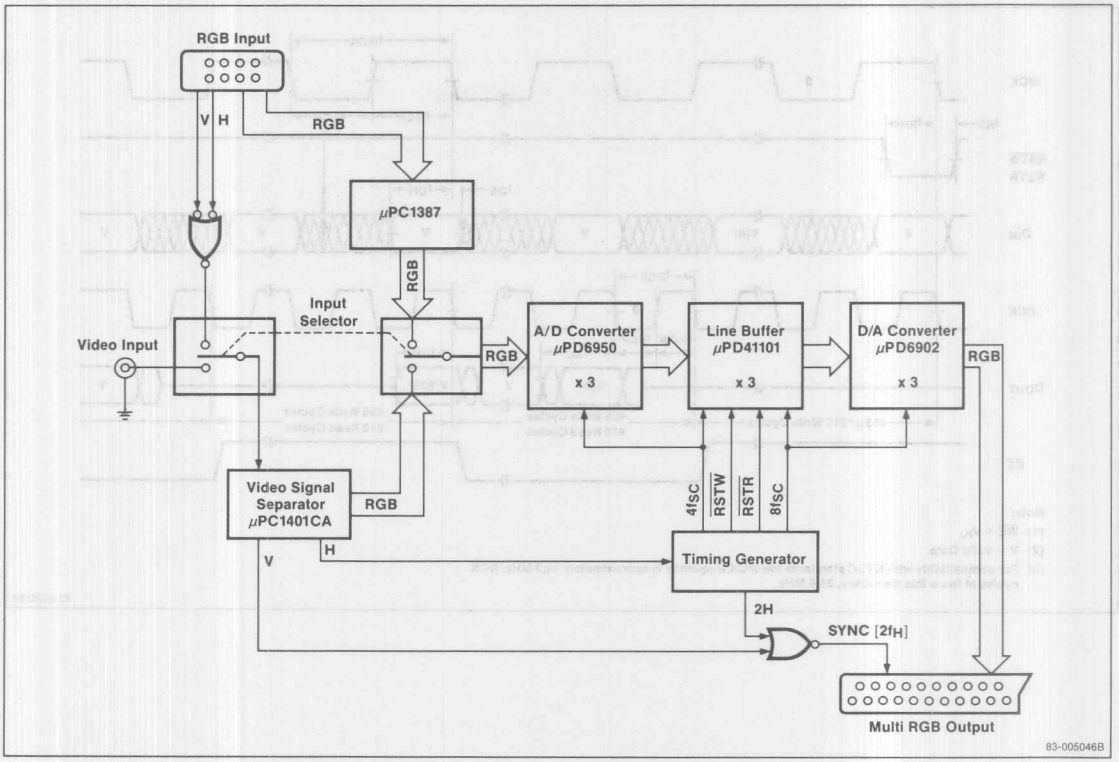


Note:
[1] $\overline{WE} = V_{IL}$.
[2] V = Valid Data.
[3] For compatibility with NTSC standards the WCK frequency is approximately 14.3 MHz. RCK cycles at twice this frequency, 28.6 MHz.

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Figure 8. Scan Converter Block Diagram



The μPD42101 and μPD42102 exactly replace the μPD41101 and μPD41102.

Video Signal Processor

The video signal is decoded from the R-G-B inputs by NEC's μPC1401, a device specifically designed to process the color, video, and synchronizing signals used in NTSC color TV systems (figures 9 and 10). By separating the signals, the μPC1401 can independently control them and thereby reduce the number of peripheral devices usually required in this phase.

Figure 9. μPD1401 Block Diagram

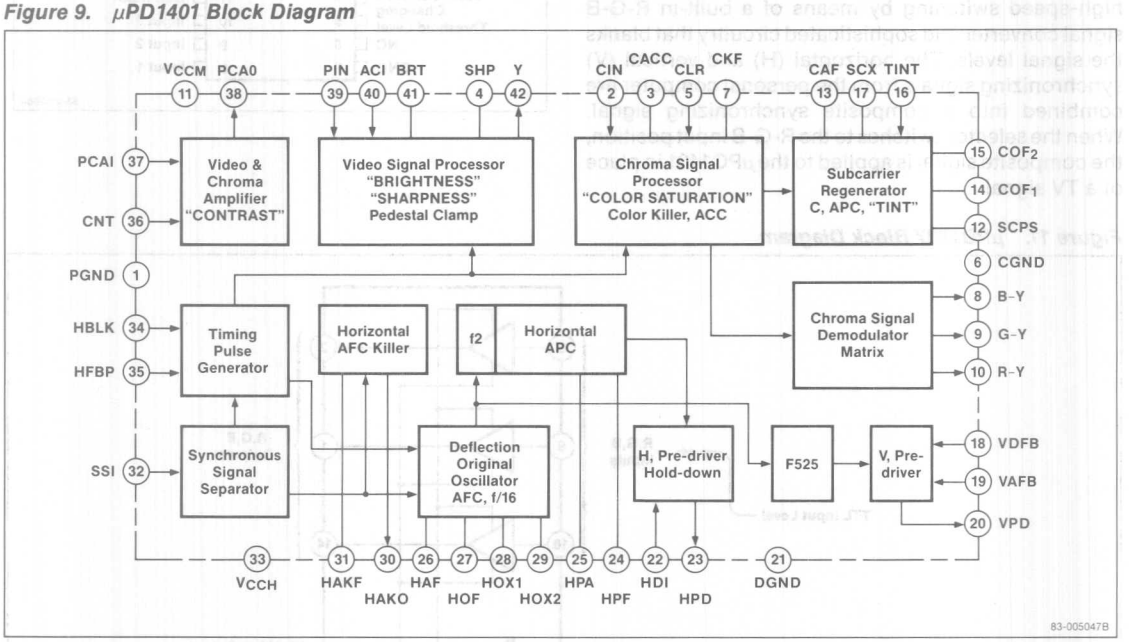
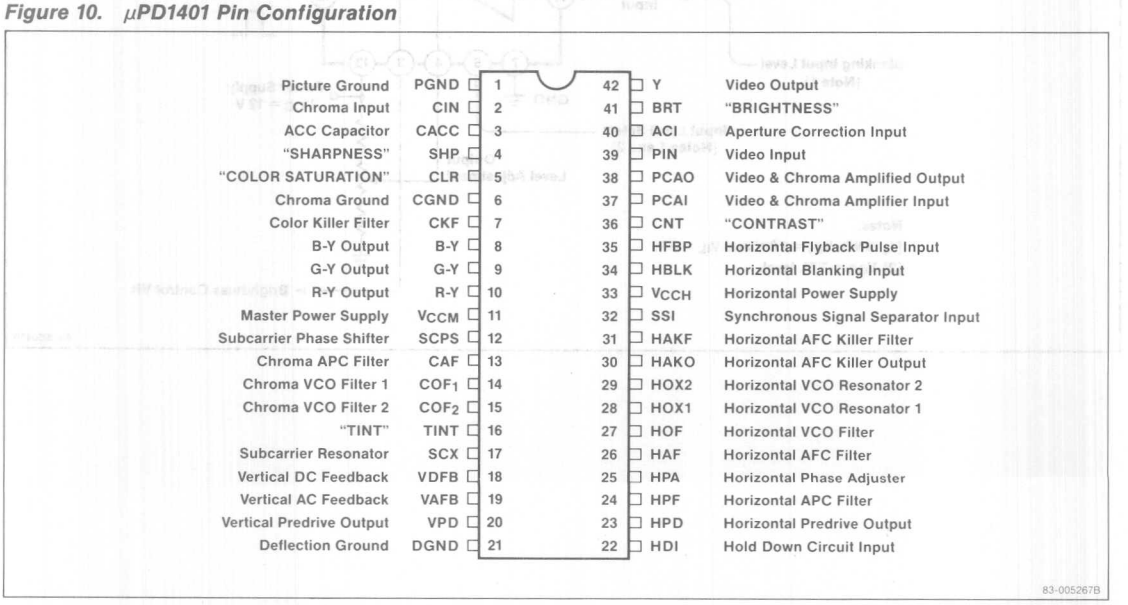


Figure 10. μPD1401 Pin Configuration



The μPD42101 and μPD42102 exactly replace the μPD41101 and μPD41102.

R-G-B Signal Processor

The level of the R-G-B output signals from the personal computer are adjusted by a μPC1387 (figures 11 and 12). An interface between the digital R-G-B signals and the TV color signal output, the μPC1387 provides high-speed switching by means of a built-in R-G-B signal converter and sophisticated circuitry that blanks the signal levels. The horizontal (H) and vertical (V) synchronizing signals from the personal computer are combined into a composite synchronizing signal. When the selector switches to the R-G-B input position, the composite signal is applied to the μPC1401 in place of a TV signal.

Figure 12. μPD1387 Pin Configuration

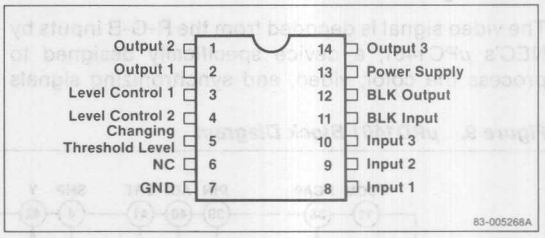
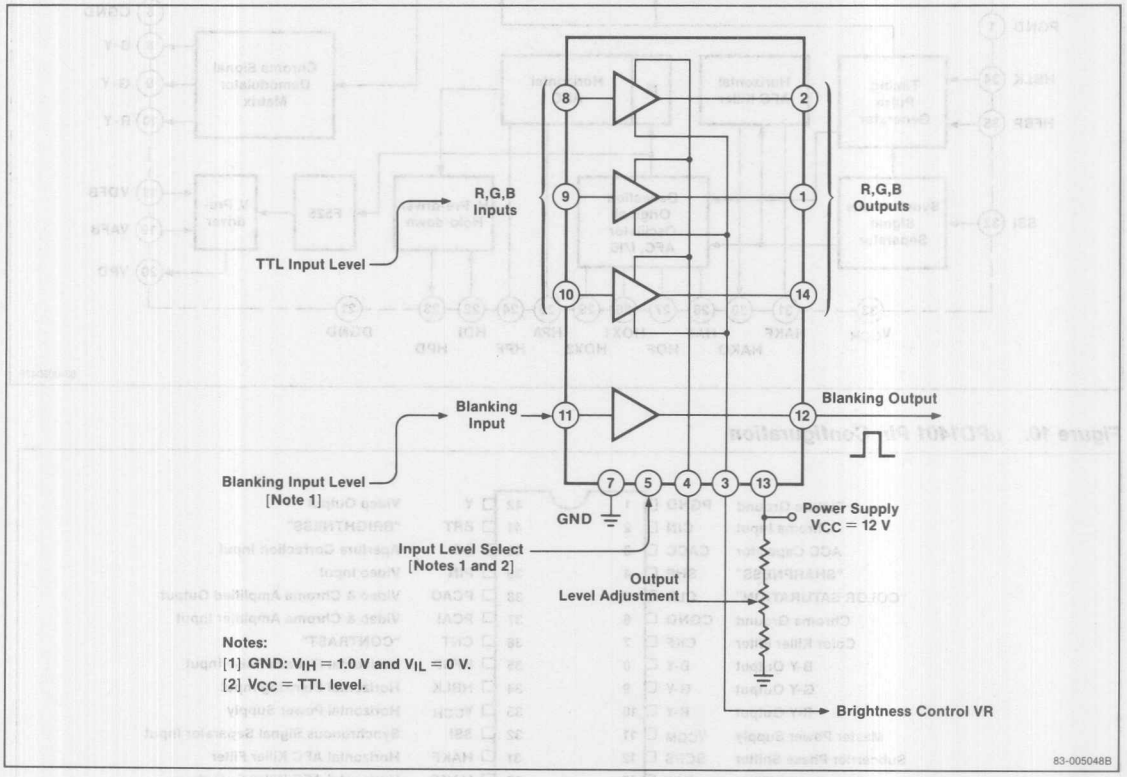


Figure 11. μPD1387 Block Diagram



The μPD42101 and μPD42102 exactly replace the μPD41101 and μPD41102.

Analog-to-Digital Converter

The input selector chooses one of the two R-G-B signals from the μPC1401 and μPC1387 and passes it to the μPD6950, where it first is sampled at a clock frequency equal to $4f_{sc}$ (14.3 MHz) and then written to the μPD41101 line buffer. The CMOS-fabricated μPD6950 is an analog-to-digital (A/D) converter whose high speed and low power consumption are particularly suited to video applications (figures 13 and 14).

Figure 13. μPD6950 Pin Configuration

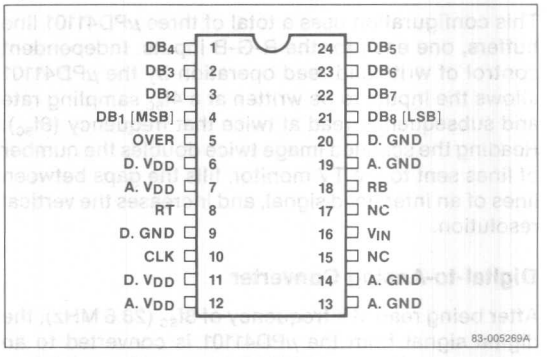
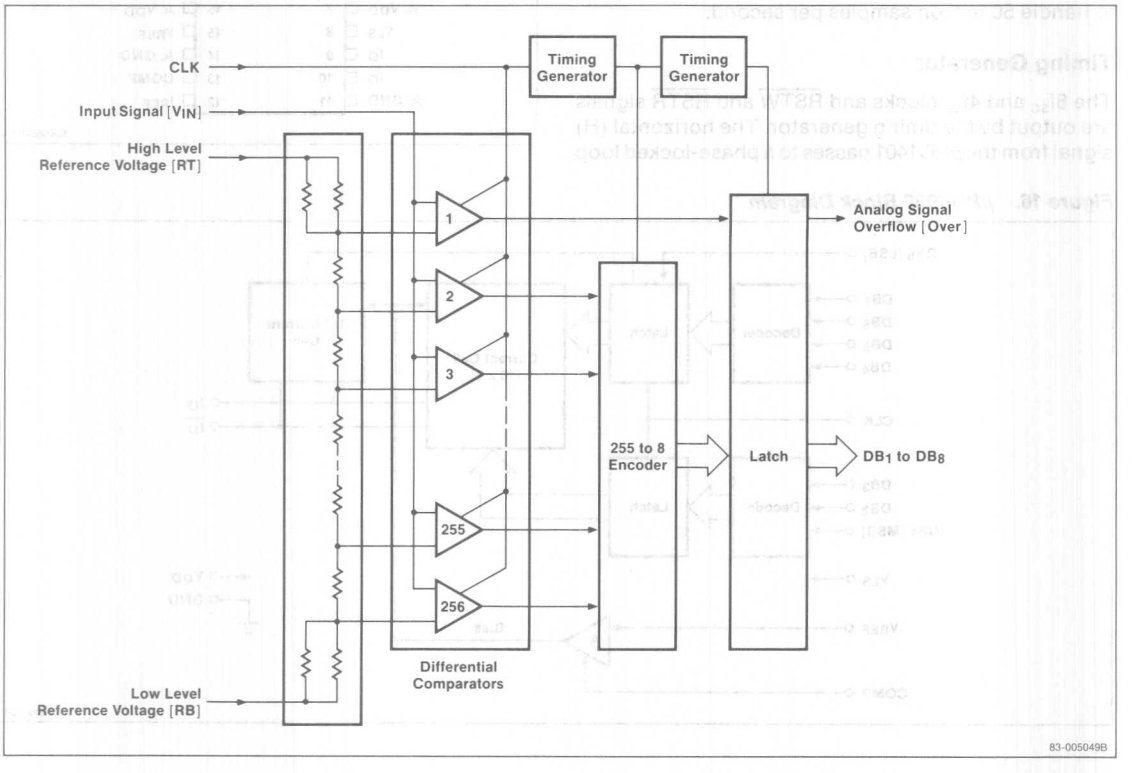


Figure 14. μPD6950 Block Diagram



Line Buffer

This configuration uses a total of three μPD41101 line buffers, one each for the R-G-B inputs. Independent control of write and read operation by the μPD41101 allows the inputs to be written at a $4f_{sc}$ sampling rate and subsequently read at twice that frequency ($8f_{sc}$). Reading the scanned image twice doubles the number of lines sent to the TV monitor, fills the gaps between lines of an interlaced signal, and increases the vertical resolution.

Digital-to-Analog Converter

After being read at a frequency of $8f_{sc}$ (28.6 MHz), the digital signal from the μPD41101 is converted to an analog signal by the μPC6902 (figures 15 and 16). The CMOS-fabricated μPC6902 D/A converter is designed to handle 50 million samples per second.

Timing Generator

The $8f_{sc}$ and $4f_{sc}$ clocks and $\overline{RSTW}$ and $\overline{RSTR}$ signals are output by the timing generator. The horizontal (H) signal from the μPC1401 passes to a phase-locked loop circuit, where it is compared and locked with a horizontal signal obtained by dividing the $8f_{sc}$ clock. After the horizontal frequency has been multiplied by 2 (2H), this signal is combined with the vertical drive signal (V) from the μPC1401 for use as the composite synchronizing signal in noninterlaced scanning. Together with the R-G-B output signals, it is then passed to the TV monitor.

Figure 15. μPD6902 Pin Configuration

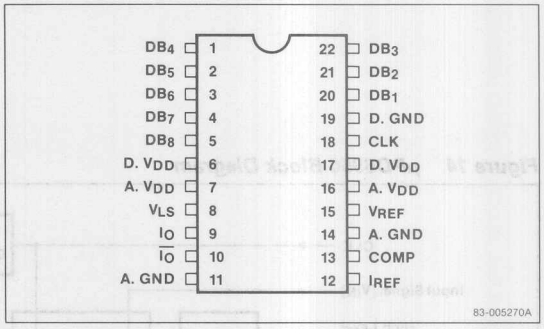
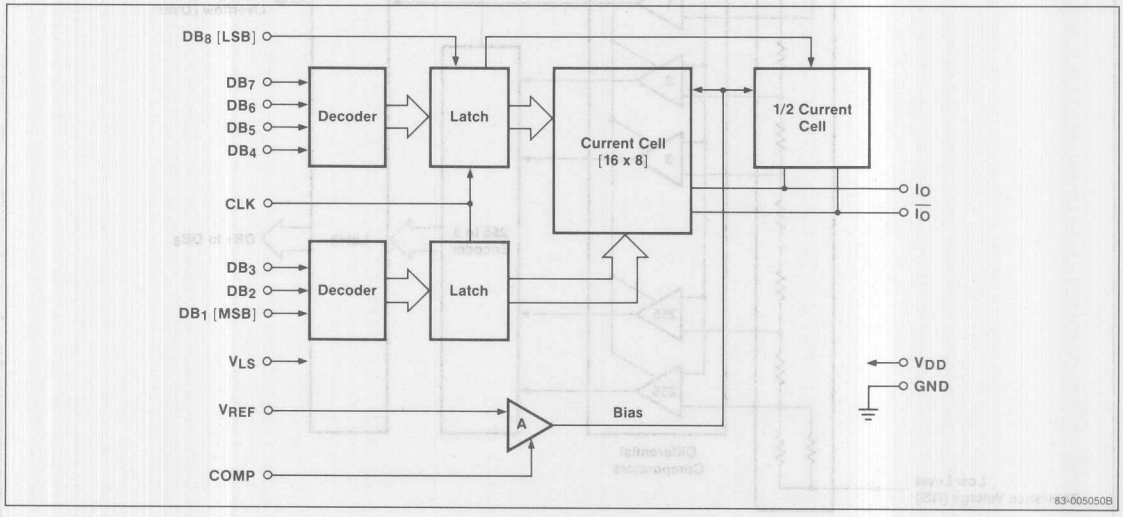


Figure 16. μPD6902 Block Diagram



The μPD42101 and μPD42102 exactly replace the μPD41101 and μPD41102.

Operation

A circuit diagram for the scan converter is shown in figure 17. The operation in each block is described below.

Video Signal Input Stage

Switch SW_1 selects the NTSC video signal and applies it to the μPC1401, which decodes the composite signal and outputs R-G-B horizontal and vertical synchronizing signals. The μPC1401 integrated circuit separates color types (Y, R-Y, B-Y, G-Y) to form a matrix using three external transistors (Tr_3-Tr_5) to produce the R-G-B signal.

A 4528BC one-shot multivibrator sets the horizontal synchronizing signal to a suitable pulse width. One of the pulse signals is applied to pins 34 and 35 of the μPC1401 as the burst gate and blanking pulses; the other signal is applied to the MC4044 phase comparator for clock generation comparison purposes.

R-G-B Signal Input Stage

The R-G-B input signal passes to a 74LS08 two-input positive AND gate and then to the μPC1387 which, together with Tr_6 and the 74LS08, ensures that no signal is applied during the horizontal retracing period.

The R-G-B signal applied to the μPC1387 is adjusted to a suitable level prior to being output from that device. Conversely, the vertical and horizontal synchronizing signals are combined in the 74LS08 to form the composite synchronizing signal passed to the μPC1401 by selection switch SW_1.

A/D Conversion Stage

The R-G-B signal selected by SW_1 is passed to the μPC6950 through a 7-MHz low-pass filter to cut frequencies in excess of one-half the sampling frequency of 14.3 MHz (figure 18). This analog signal is converted by the 14.3-MHz clock and then passed to the μPC1401 as an 8-bit digital signal.

Line Buffer Stage

The 8-bit digital input is written at 14.3 MHz before being passed to the μPC6902 for D/A conversion at 28.6 MHz. The WCK, RCK, $\overline{RSTW}$, and $\overline{RSTR}$ controls for the line buffer are supplied from the timing generator (figure 19).

D/A Conversion Stage

The digital input from the μPD41101 is converted to an analog signal by the 28.6-MHz clock to reproduce an R-G-B signal of twice the horizontal line frequency.

Timing Generation Stage

An LC oscillator circuit uses a 74F04 inverter to generate the 28.6-MHz signals required for driving the line buffer and D/A converter clocks, as well as the 14.3-MHz signals required for driving the line buffer and A/D converter clocks.

The horizontal signal from the μPC1401 is passed to the MC4044 phase frequency detector for phase comparison with the horizontal signal obtained by dividing the clock from the clock generator. The resultant signal is then transferred through a low-pass filter to the 1SV164 varactor diode of a voltage-controlled oscillator to adjust the oscillating frequency (figure 20).

Three 74LS163 synchronous 4-bit counters divide the 14.3-MHz clock by a factor of 455. The resultant 31.5-kHz clock ($2f_H$) is timed by the 28.6-MHz clock and passed to the line buffer as the $\overline{RSTR}$ signal.

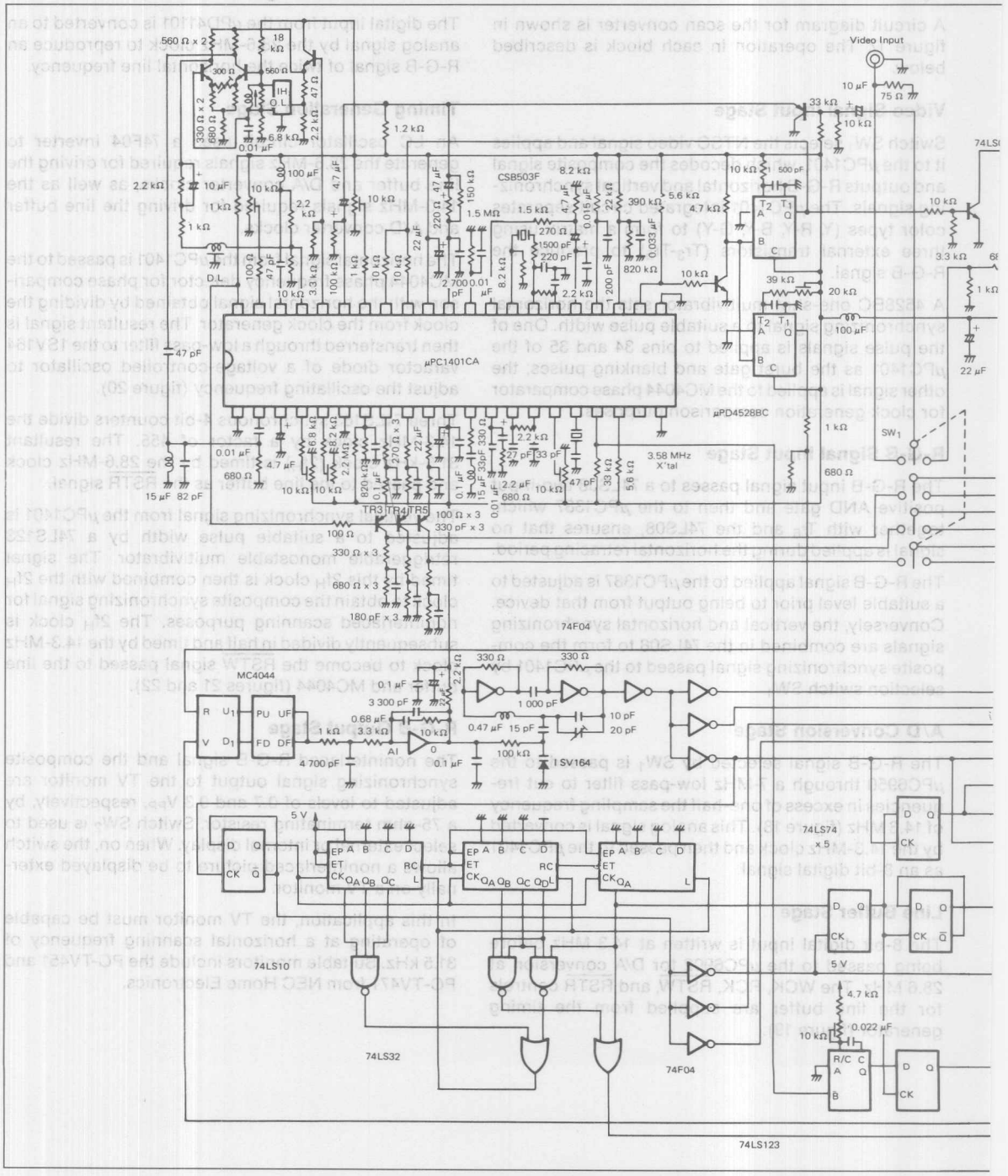
The vertical synchronizing signal from the μPC1401 is adjusted to a suitable pulse width by a 74LS123 retriggerable monostable multivibrator. The signal timed by this $2f_H$ clock is then combined with the $2f_H$ clock to obtain the composite synchronizing signal for noninterlaced scanning purposes. The $2f_H$ clock is subsequently divided in half and timed by the 14.3-MHz clock to become the $\overline{RSTW}$ signal passed to the line buffer and MC4044 (figures 21 and 22).

R-G-B Output Stage

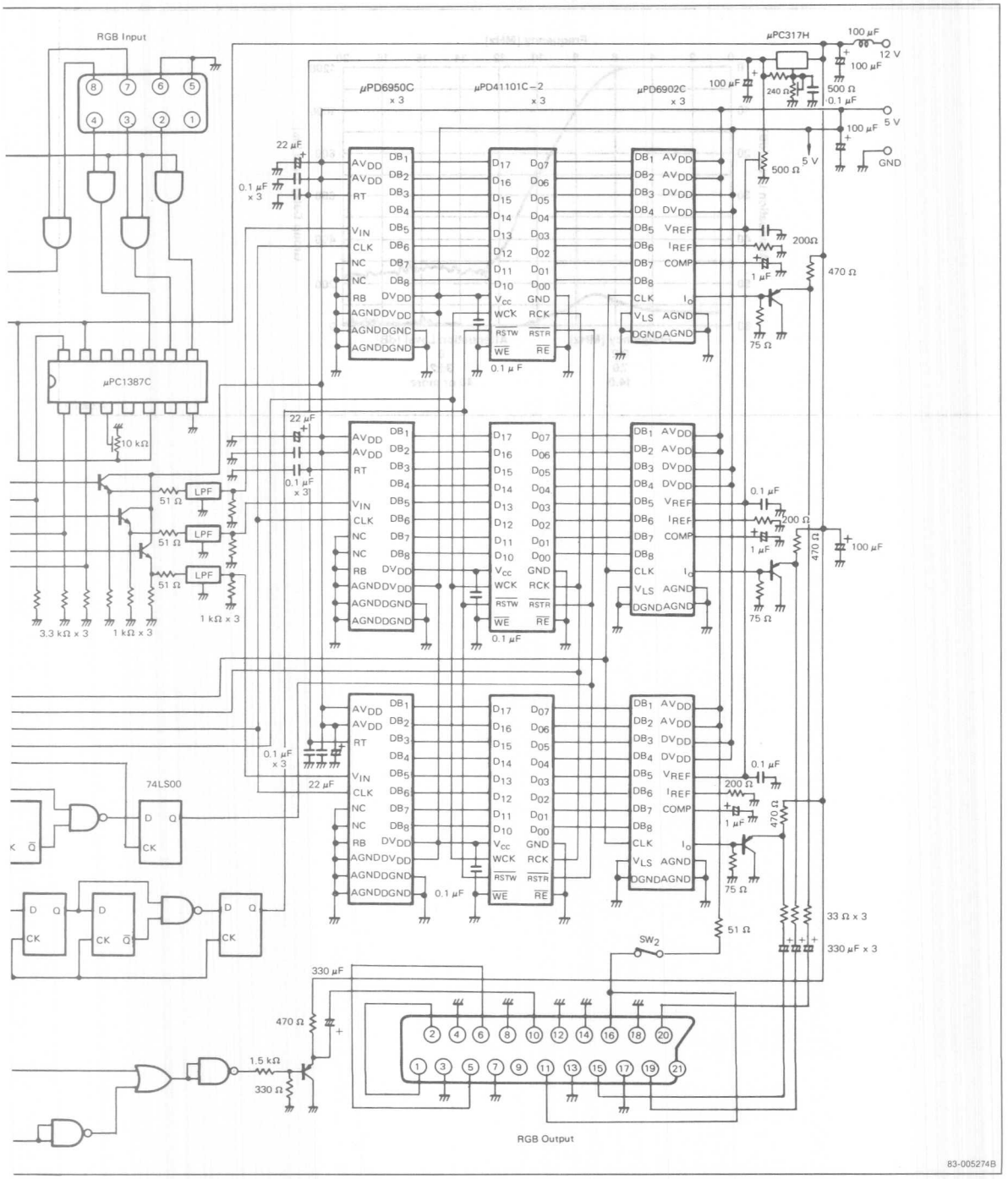
The noninterlaced R-G-B signal and the composite synchronizing signal output to the TV monitor are adjusted to levels of 0.7 and 0.3 V_{PP}, respectively, by a 75-ohm terminating resistor. Switch SW_2 is used to select external or internal display. When on, the switch allows a noninterlaced picture to be displayed externally on a TV monitor.

In this application, the TV monitor must be capable of operating at a horizontal scanning frequency of 31.5 kHz. Suitable monitors include the PC-TV451 and PC-TV471 from NEC Home Electronics.

Figure 17. μPD41101 Composite Schematic

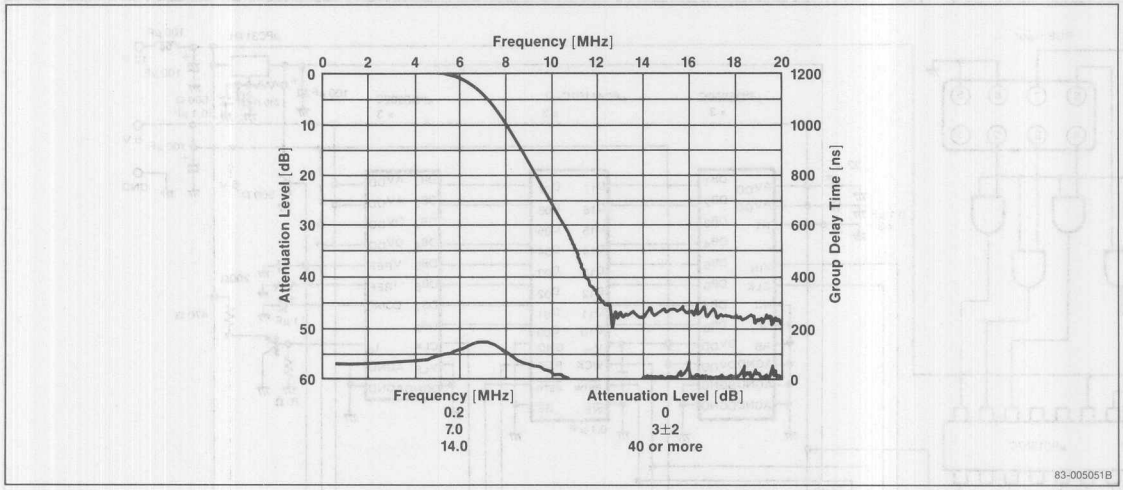


The μPD42101 and μPD42102 exactly replace the μPD41101 and μPD41102.



The μPD42101 and μPD42102 exactly replace the μPD41101 and μPD41102.

Figure 18. Characteristics of LT15LP7.0M01-32 Low-Pass Filter



The μPD42101 and μPD42102 exactly replace the μPD41101 and μPD41102.

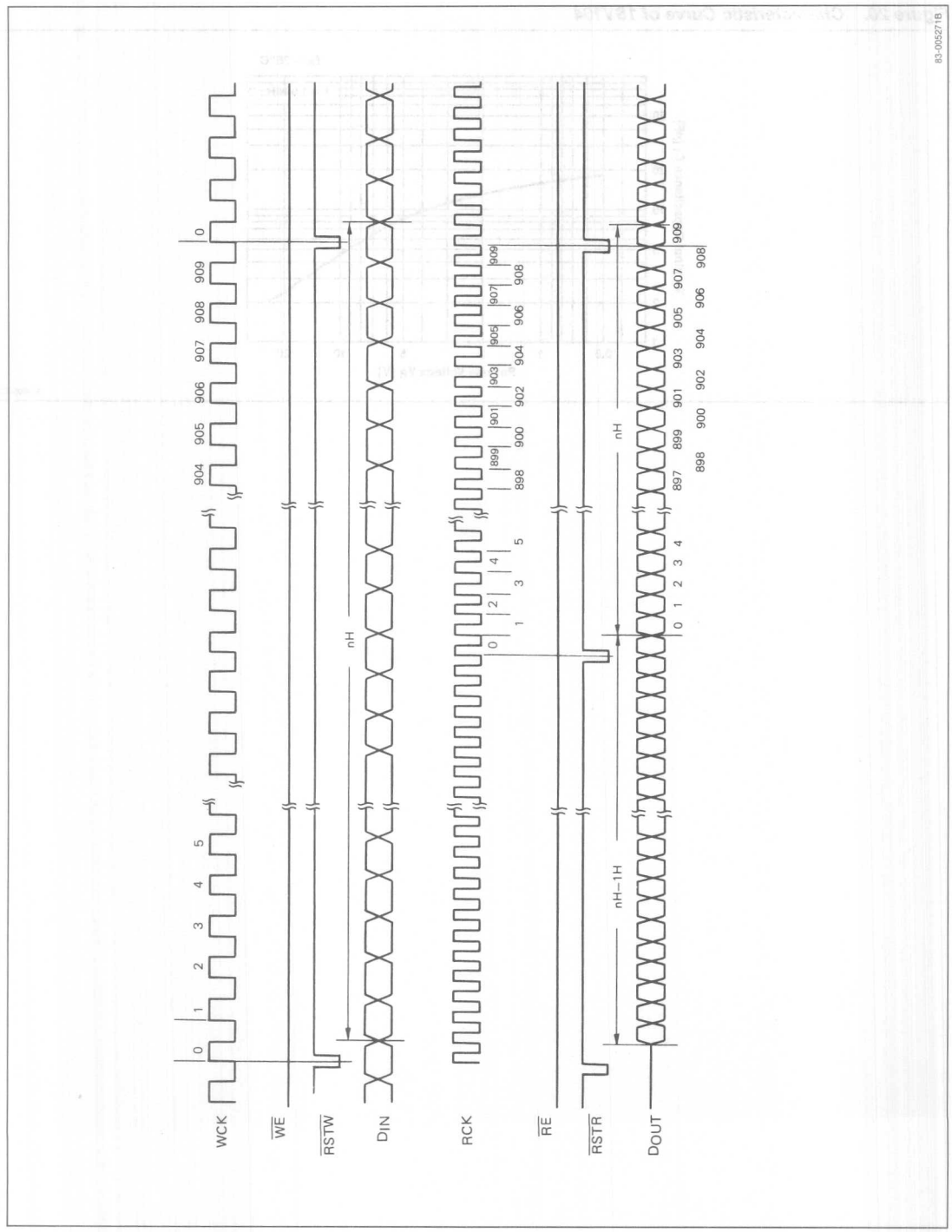
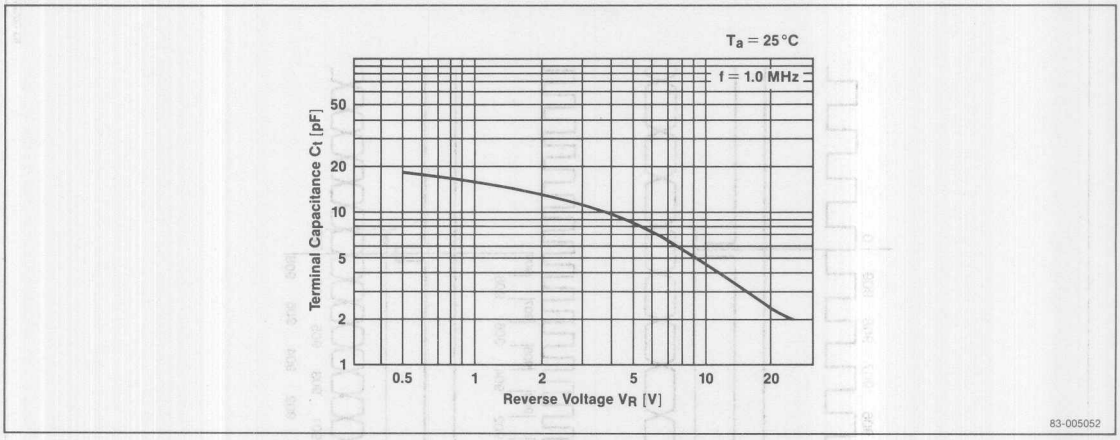


Figure 19. Scan Conversion Timing

Figure 20. Characteristic Curve of 1SV164



The μPD42101 and μPD42102 exactly replace the μPD41101 and μPD41102.

Figure 21. Counter Stage of Timing Generator

Figure 22. Synchronizing Signal Generator

INTRODUCTION

A computer graphics system is comprised of hardware and software, the organization of which depends upon the specific requirements of each application. While individual designs may differ from one application to another, the design objective essentially remains the same: to define a device-independent, general-purpose sequence of operations (or pipeline) that transforms the geometric model of an object into an image on a display screen.

This application note provides an overview of the concepts and methodologies used in the design of computer graphics systems. The intent here is to introduce the basics, building the foundation for more vigorous study later.

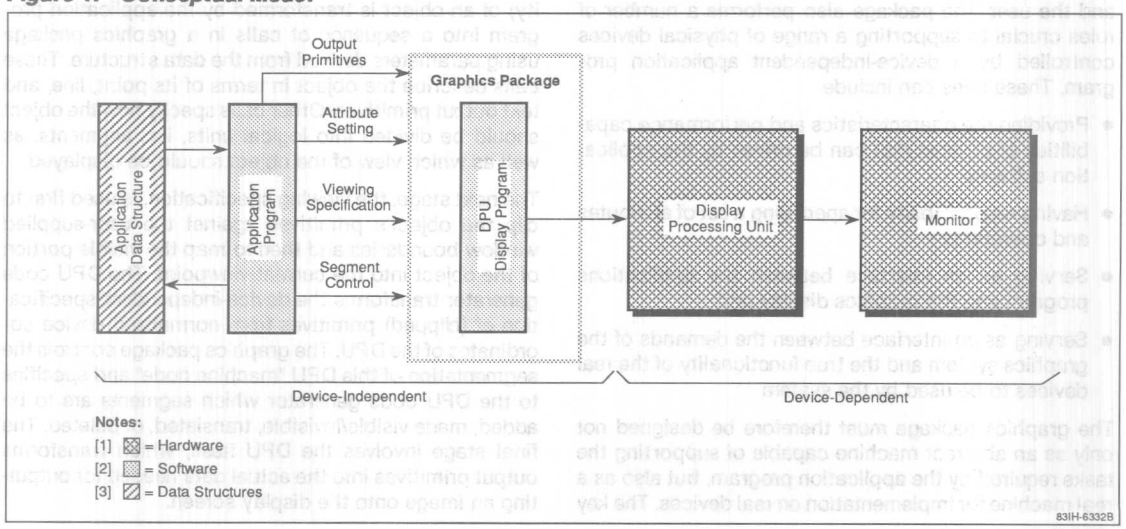
FUNDAMENTALS OF A GRAPHICS SYSTEM

The task of a graphics system is to transform real-world information into a perceptible image for display on an output device. While systems in the past typically used software designed for particular kinds of hardware, contemporary systems use device-independent software designed for compatibility with a variety of hardware.

This latter type involves a sequence of operations that begins with a model of the image to be rendered. As shown in figure 1, the program portion of the model has three elements—the application data structure (data base), the application program, and the display program. These are transmitted to the hardware component, in this case a host computer connected to a graphics display terminal, in terms that the computer can understand. At the same time, the original model structure is preserved. As a conceptual framework, this model is useful in showing how an abstract description of a two- or three-dimensional "world" having one or more objects is transformed into a view or picture of that world.

The functions represented by the conceptual model need to be more than device-independent; they also must be sufficiently general-purpose to support a variety of applications. No strict definition of this requirement exists. At one extreme, the system may be entirely incorporated into a host computer, with the graphics reduced to a single monitor. Another system might incorporate all graphics functions into a standalone workstation. The point is that the implementation of VLSI and concurrent technologies may differ, but the basic sequence of functions must remain the same.

Figure 1. Conceptual Model



One of the tasks of the application program is to support interactive input devices that allow the user to specify how objects are to be constructed and modified and which views are to be displayed. The application program decodes user-supplied input and uses it to direct the system to change the viewing specification or to alter the model in the data structure. Once the application program has developed the data structure, the objects contained therein are described to the graphics system so that it can calculate and display the particular view desired.

The application program describes in geometric terms that portion of the world in which the picture should appear. This data is presented in the form of output primitives such as points, lines, polygons, or character strings geometrically oriented in a two- or three-dimensional world. The application program also specifies the part of the object to be rendered, the vantage point to be displayed, and the part of the viewing surface on which the image should appear.

Problems inherent to the design of graphics software are solved by a graphics package that reinforces a general-purpose, device-independent approach to graphics design by providing basic subroutines or primitives that allow portability with the application program.

The graphics package is a small but functionally complete set of application-independent facilities for creating arbitrary views of two-dimensional objects and for supporting interaction between the application program and the user. The package also performs a number of roles crucial to supporting a range of physical devices controlled by a device-independent application program. These roles can include

- Providing the characteristics and performance capabilities of devices that can be driven by the application software
- Having responsibility for specifying a set of attributes and operations
- Serving as an interface between the applications program and the graphics display unit
- Serving as an interface between the demands of the graphics system and the true functionality of the real devices to be used by the system

The graphics package must therefore be designed not only as an abstract machine capable of supporting the tasks required by the application program, but also as a real machine for implementation on real devices. The key to device-independence is that only the implementation of the graphics package (and not the rest of the application program) is device-dependent.

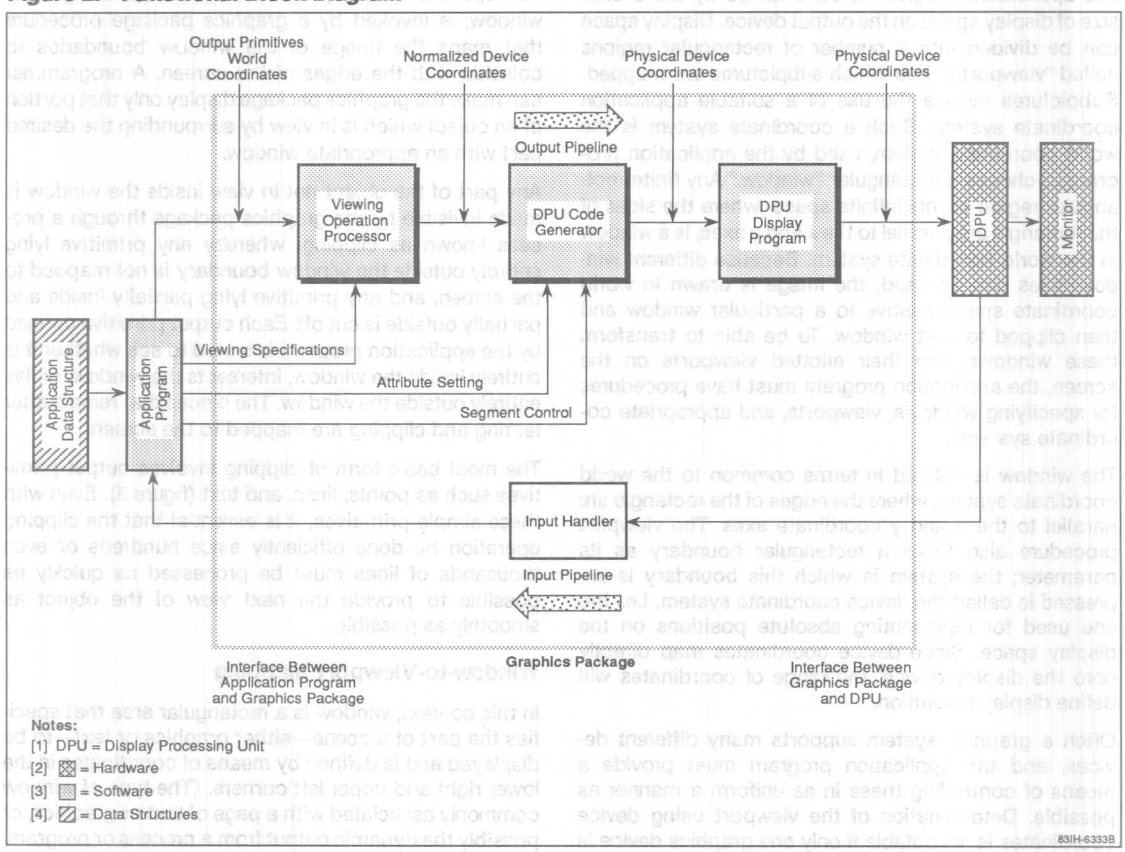
The two principal hardware components are the host computer and the display processing unit, or DPU. The two important data modules shown are both stored in shared memory (to simplify the diagram, the host's CPU and the memory shared by the CPU and DPU are not shown in figure 2). The first is the DPU display program (also called the display file or list), which is written by the graphics package and read by the DPU as it refreshes the image on the screen. The second is the application data structure, which contains a description of the objects whose images are to be displayed and is a tool to model the objects.

The three major stages shown as software modules in figure 2 could also be implemented as hardware or firmware modules in other systems. Their interaction is characterized by two major data flows moving in opposite directions within the system: one is from a data structure description of an object to its image on the screen, and the other is from user-supplied input to the data structure and/or display program.

The object-to-image transformation sequence begins at the output pipeline, a four-stage pipeline that transforms a description of the object into successively more machine-dependent representations, and finally, into an image on a screen. The portion of the data structure that models the geometry (layout) and topology (connectivity) of an object is transformed by the application program into a sequence of calls in a graphics package using parameters derived from the data structure. These calls describe the object in terms of its point, line, and text output primitives. Other calls specify how the object should be divided into logical units, i.e., segments, as well as which view of the object should be displayed.

The next stage, the viewing specification, is used first to clip the object's primitives against the user-supplied window boundaries and then to map the visible portion of the object into the current viewpoint. The DPU code generator transforms the device-independent specification of (clipped) primitives from normalized device coordinates of the DPU. The graphics package controls the segmentation of this DPU "machine code" and specifies to the DPU code generator which segments are to be added, made visible/invisible, translated, or deleted. The final stage involves the DPU itself, which transforms output primitives into the actual data needed for outputting an image onto the display screen.

Figure 2. Functional Block Diagram



The input pipeline has fewer stages. The DPU records input device usage and either interrupts the CPU or transfers data on request. Input data is collected from the DPU by the input handler, which typically passes it to the application program. This data changes the flow of the application program, and may also cause the application program to either modify the data structure or change the viewing operation parameters. The input may also be used directly by the code generator to manipulate segment operations.

THE VIEWING OPERATION

The viewing operation is a sequence of steps that transforms a device-independent description of an object into a device-dependent display program generating a particular view of an image. In the viewing operation processor and DPU code generator stages, functions such as clipping, window-to-viewpoint mapping, and display code generation in device-dependent physical screen coordinates are performed. The first two steps are usually considered part of the viewing operation, while the third step is part of the DPU code generation process.

OUTPUT PRIMITIVES

Coordinate Systems

In a basic graphics system, the only graphical primitives needed by the application program are those to define points, lines, and displayed text strings. These are described in terms of positions and measurements in a Cartesian coordinate system. The coordinates are inherently dimensionless, and thus the application program can define objects in terms of units that are natural to the application and to the user.

The application program is constrained by the overall size of display space on the output device. Display space can be divided into a number of rectangular regions called "viewports," into which subpictures are mapped. Subpictures require the use of a suitable application coordinate system. Such a coordinate system is the world coordinate system, used by the application program to choose a rectangular "window." Any finite rectangular region of this infinite space, where the sides of the rectangle are parallel to the x and y axes, is a window in the world coordinate system. Because different window sizes can be used, the image is drawn in world coordinate space relative to a particular window and then clipped to that window. To be able to transform these windows into their allotted viewports on the screen, the application program must have procedures for specifying windows, viewports, and appropriate coordinate systems.

The window is defined in terms common to the world coordinate system, where the edges of the rectangle are parallel to the x and y coordinate axes. The viewport procedure also takes a rectangular boundary as its parameter; the system in which this boundary is expressed is called the device coordinate system, i.e., the one used for representing absolute positions on the display space. Since device coordinates map directly onto the display device, the range of coordinates will define display resolution.

Often a graphics system supports many different devices, and the application program must provide a means of controlling these in as uniform a manner as possible. Determination of the viewport using device coordinates is acceptable if only one graphics device is used, or if all graphics devices have exactly the same coordinate systems to represent their display spaces. A better solution to device disparity requires a uniform method of addressing different display spaces. The standard solution is to introduce an intermediate system called normalized device coordinates, where (0,0) is at the bottom left corner and (1,1) is at the top right, i.e., a unit square.

Windows and Clipping

The viewing operation, or pipeline, has been defined as a journey of a coordinate through the graphics system. It starts as a world coordinate point generated by a call to an output primitive procedure, continues through the normalized transformation stage, and finally passes through the device transformation stage, after which it is expressed in normalized device coordinates.

During this procedure, the graphics package must know what portion of the essentially unbound world coordinate space is to be displayed. This rectangular region, or window, is invoked by a graphics package procedure that maps the image of the window boundaries to coincide with the edges of the screen. A programmer can make the graphics package display only that portion of an object which is in view by surrounding the desired part with an appropriate window.

Any part of the object not in view inside the window is made invisible by the graphics package through a process known as clipping, whereby any primitive lying entirely outside the window boundary is not mapped to the screen, and any primitive lying partially inside and partially outside is cut off. Each output primitive defined by the application program is tested to see whether it is entirely inside the window, intersects the window, or lies entirely outside the window. The pieces that remain after testing and clipping are mapped to the screen.

The most basic form of clipping involves output primitives such as points, lines, and text (figure 3). Even with these simple primitives, it is essential that the clipping operation be done efficiently since hundreds or even thousands of lines must be processed as quickly as possible to provide the next view of the object as smoothly as possible.

Window-to-Viewport Mapping

In this context, window is a rectangular area that specifies the part of a scene—either graphics or text—to be displayed and is defined by means of coordinates in the lower right and upper left corners. (The type of window commonly associated with a page of text or graphics, or possibly the dynamic output from a process or program, does not apply to this discussion.)

A window defines what is to be displayed but not where it is to be displayed. Therefore, each window requires a corresponding viewport that defines the space into which the window is to be displayed. In figure 4, the window is clipped to its boundary in world coordinates, and then subsequently mapped to the viewport boundaries in device coordinates. A few windows appear whole, while some are obscured by other windows. A viewport obscures another viewport when it has a higher priority than the obscured viewport. Viewports may be moved around the display area without affecting their information content, except when they are moved relative to an obscuring viewport.

The movement of a window about the scene gives the effect of changing the observer's view of the picture. Adjusting the size of the window relative to the size of the objects being displayed produces arbitrary scaling effects. Thus, moving the window and selecting smaller

or larger window sizes creates the cinematic effect of panning in or zooming out. In theory, one can zoom in on a single primitive until it touches the boundaries, or zoom out until the entire scene blurs together as a single port.

If the graphics package supports only a single DPU, then it is most efficient to convert directly from world coordinates to physical coordinates. For packages that support multiple display devices, it is convenient to produce a low-level, machine-dependent, normalized device coordinate representation of the image that can then be translated by multiple DPU code generators to the appropriate physical device coordinates. Therefore, window-to-viewport mapping is a conversion process in which the window, defined in world coordinates, is converted into device or normalized device coordinates for input into the next phase of the viewing pipeline (figure 5).

Figure 3. Example of Two-Dimensional Clipping

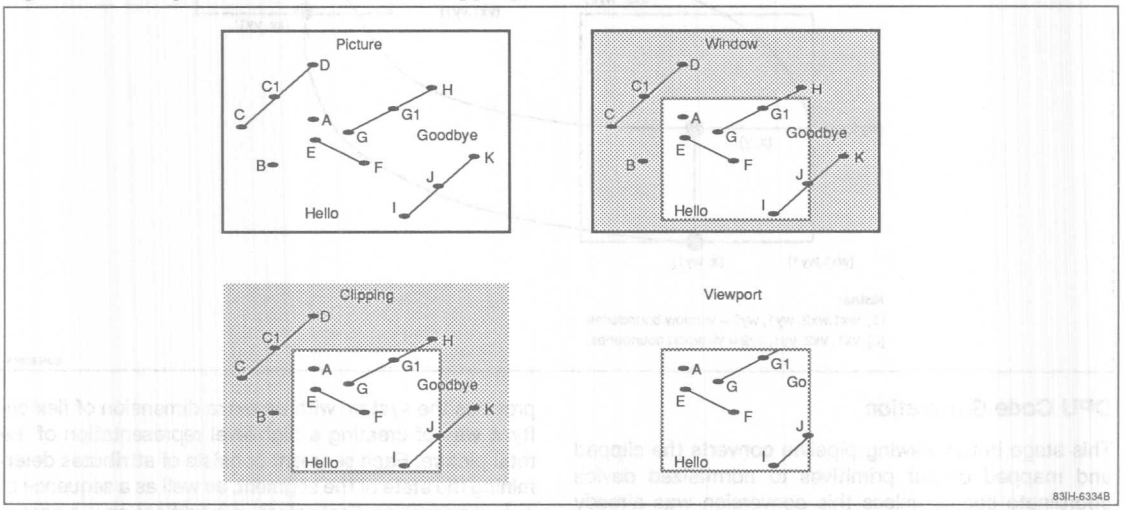


Figure 4. Window-to-Viewport Mapping

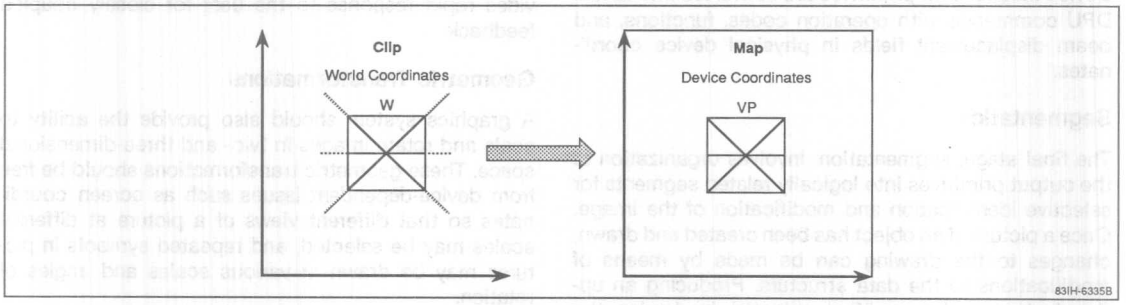
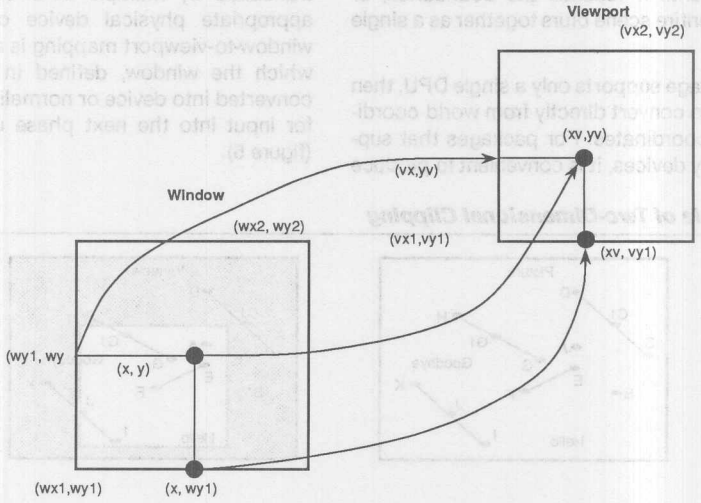


Figure 5. Window Boundaries Mapped to Viewport Boundaries



DPU Code Generation

This stage in the viewing pipeline converts the clipped and mapped output primitives to normalized device coordinate space, unless this conversion was already performed in the window-to-viewport mapping phase. Device-independent primitives are converted into actual DPU commands with operation codes, functions, and beam displacement fields in physical device coordinates.

Segmentation

The final stage, segmentation, involves organization of the output primitives into logically related segments for selective identification and modification of the image. Once a picture of an object has been created and drawn, changes to the drawing can be made by means of modifications to the data structure. Producing an updated view of the modified object(s) by having the application program redescribe everything to the graphics package, even though only a portion has been changed, would be very wasteful because of the computations required to clip and map world coordinates into device-dependent coordinates.

Segmentation, where the object's description is partitioned into segments that are individually displayed, provides the system with an extra dimension of flexibility, a way of creating a high-level representation of the total picture. Each segment consists of attributes determining the state of the segment, as well as a sequence of output primitives. Fast selective modification is a necessity of high-quality interactive graphics because it provides rapid response to the user for closely coupled feedback.

Geometric Transformations

A graphics system should also provide the ability to scale and rotate images in two- and three-dimensional space. These geometric transformations should be free from device-dependent issues such as screen coordinates so that different views of a picture at different scales may be selected, and repeated symbols in pictures may be drawn at various scales and angles of rotation.

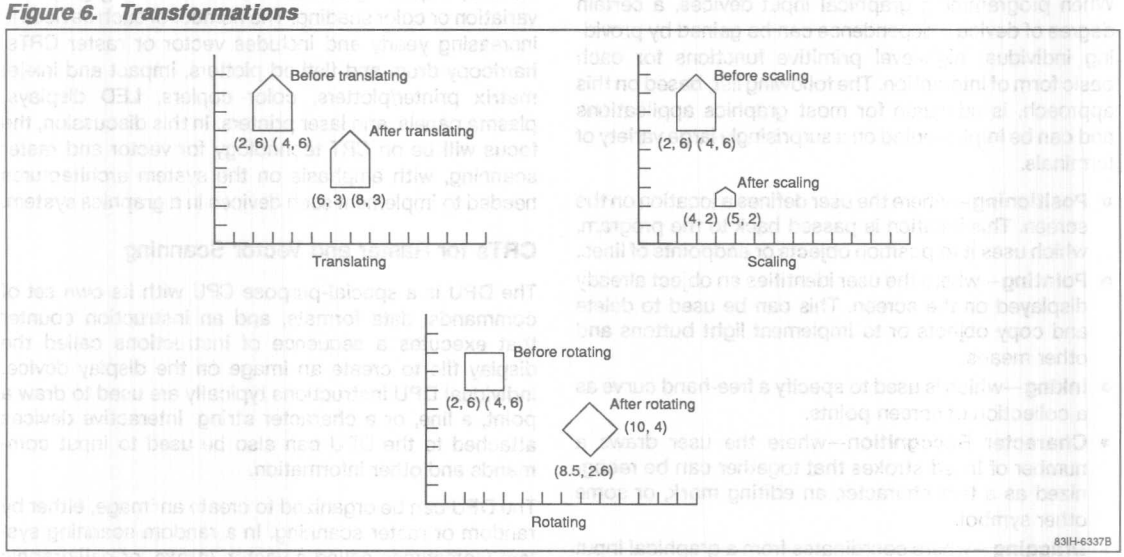
The most common way to view transformations is with 4 by 4 matrix multiplication. However, matrix multiplication requires many intermediate steps, making the transformation of object coordinates one of the most time-consuming steps in the entire graphics output sequence.

Arbitrary two- and three-dimensional transformations such as object rotations, translations, scaling, and per-

spective and orthographic projection may precede the clipping function in the graphics pipeline, and may also include the ability to transform the image into viewport coordinates (figure 6). Because matrix representations for translating, scaling and rotating differ (scaling requires an additional matrix and rotation uses a multiplication matrix), it is more efficient to treat these functions in a consistent way. For example, if they are expressed in homogeneous coordinates, all three transformations could be expressed as multiplications.

Homogeneous coordinates were developed in geometry and have subsequently been applied in graphics (figure 6). Numerous graphics subroutine packages and some display processors work with homogeneous coordinates and transformations. In some cases, they are used directly by the application program in passing parameters to the graphics package. In other cases, they are applied only within the package and are invisible to the programmer.

Figure 6. Transformations



INTERACTIVE GRAPHICS TECHNIQUES

One of the principal goals of interactive systems, graphics or otherwise, is the symbiosis between man and machine. When a user is able to interact with a computer, this interaction is said to be conversational. Working together on a single task merges the capabilities of the two partners, man and computer.

Of all the possibilities for graphics input hardware, the keyboard is certainly the most familiar. Many graphics systems have little more. There are five basic logical input devices: the locator to indicate a position and/or orientation, the pick to select a display entity, the valuator to input a single value in the space of real numbers, the keyboard to input a character string, and a button to select from a set of possible alternative actions or choices. Logical input devices are rather like logical files in an operating system. A sequential input file may be implemented physically by means of a card reader, a magnetic tape drive, a disk drive, or a terminal keyboard. The application program doesn't care because the operating system makes them functionally alike, despite their physical differences.

Many graphics systems simulate the logical functions of another class, although some of the simulations can be rather awkward. These implementations are sometimes part of the graphics package. For example, since a direct-view storage tube cannot be used with a light pen, the cross-hair cursor locator might be used as a pick.

In addition to interactive devices and device simulations, interaction techniques are used as the basic building blocks from which complete interactive dialogues are designed. Interactive techniques are higher-level functions implemented through the basic device simulations already discussed. These techniques, which are general application-independent ways of interfacing with a computer, are routinely used in many graphics packages and include the following:

- **Construction Techniques**—where the physical appearance of an object is indirectly manipulated by means of dragging or rubberbanding.
- **Command Techniques**—where menus and programmed function keyboards are used to input commands.
- **Picking Techniques**—where a hierarchical object structure allows the user to pick a basic object, a collection of basic objects, or perhaps a collection of collections.

When programming graphical input devices, a certain degree of device independence can be gained by providing individual high-level primitive functions for each basic form of interaction. The following list, based on this approach, is adequate for most graphics applications and can be implemented on a surprisingly large variety of terminals.

- **Positioning**—where the user defines a location on the screen. This location is passed back to the program, which uses it to position objects or endpoints of lines.
- **Pointing**—where the user identifies an object already displayed on the screen. This can be used to delete and copy objects or to implement light buttons and other means.
- **Inking**—which is used to specify a free-hand curve as a collection of screen points.
- **Character Recognition**—where the user draws a number of inked strokes that together can be recognized as a text character, an editing mark, or some other symbol.
- **Dragging**—where coordinates from a graphical input device are used to specify the location of some object on the screen. Repositioning is performed rapidly enough so that the user can "rag"the object around the screen until it is correctly positioned, at which time it is fixed again.

Device independence is just as troublesome here as it is in graphical output. The problem is not that input devices have such different characteristics, but that each input technique demands a specific form of immediate feedback on the screen. The popular rubberband line drawing technique, for example, depends on the dynamic display of a line with one endpoint fixed and the other following the coordinate input device. It is difficult to provide this sort of effect without modifying the graphical output process. Therefore, meddling with the output process should be avoided in the interest of device independence.

DISPLAY HARDWARE

Without special hardware for producing output, there would be little interest in computer graphics. Useful pictures can be produced using only a line printer or a normal hardcopy alphanumeric terminal, but what most people expect from a graphics system is something much more.

Most graphics hardware has options for moving in two dimensions, plotting or intensifying certain points on a surface, displaying characters, and providing gray-level variation or color shading. The number of such devices is increasing yearly and includes vector or raster CRTs, hardcopy drum and flatbed plotters, impact and ink-jet matrix printer/plotters, color copiers, LED displays, plasma panels, and laser printers. In this discussion, the focus will be on CRT technology for vector and raster scanning, with emphasis on the system architectures needed to implement such devices in a graphics system.

CRTs for Raster and Vector Scanning

The DPU is a special-purpose CPU with its own set of commands, data formats, and an instruction counter that executes a sequence of instructions called the display file to create an image on the display device. Individual DPU instructions typically are used to draw a point, a line, or a character string. Interactive devices attached to the DPU can also be used to input commands and other information.

The DPU can be organized to create an image, either by random or raster scanning. In a random scanning system (sometimes called a vector, stroke, or calligraphic scanning system), parts of the drawing can be depicted in any order on the display. For example, the house in figure 6 was drawn by moving (detecting) the beam to the starting point, turning it on, and continuously deflecting it between successive endpoints to trace the house outline. In a raster scanning (TV-type) system, all parts of the drawing in the first line are reproduced in left-to-right order, followed by all parts of the drawing in the second line, and so on. Hardcopy devices operate in either a random or raster scanning system. The printer, a simple hardcopy device, has a print head that moves from left to right and top to bottom. The pen plotter, which uses a pen that can be moved in any direction over a piece of paper, is a random scanning device.

Figure 7 shows basic display techniques. Starting in the upper left of the screen, the intensity is modulated during the left-to-right sweep to create different shades of gray. At the right edge, the beam is blanked (turned off), repositioned (indicated by the dashed line) at the left edge one unit down from the previous scan line, and

unblanked. After all scan lines have been drawn, the beam returns to the upper-left corner. Broadcast television in the United States operates with 525 scan lines, but common raster graphics systems use anywhere from 256 to 1024 lines. The more lines used, the higher the picture quality.

Display Processing Unit for Random Scanning

Figure 8 shows a very simple DPU capable of randomly plotting under CPU control individual discrete points on a grid of 1024 by 1024 lines. This feature requires that 10-bit x and y values be made available to the DPU. The computer uses input/output commands to load the x and y registers with coordinate values, while the analog (voltage) equivalents of the coordinate values go to the deflection system. The current amplifiers for the magnetic deflection coil produce the appropriate current. Once this current has stabilized, the electron beam is unblanked (turned on) for a few microseconds, and then blanked again to detect and draw the next point. The whole process can take from 5 to 20 μs per point with a fast deflection system, or as much as 50 μs per point with a slow deflection system. In a given system, the time between the display of successive points is usually nearly proportional to the distance between them. A refresh rate of 30 cycles per second allows 33,000 microseconds per refresh cycle, resulting in display capacities from 33,000/50 = 660 to 33,000/5 = 6600 points.

The system in figure 8 has no facilities for concurrent program execution and display of screen refresh capabilities. Most contemporary DPUs provide the same functions as a general-purpose CPU, functions such as an instruction counter, instruction register, and control logic that allow the DPU to execute instructions as well as to refresh the display.

3

Figure 7. Display Techniques

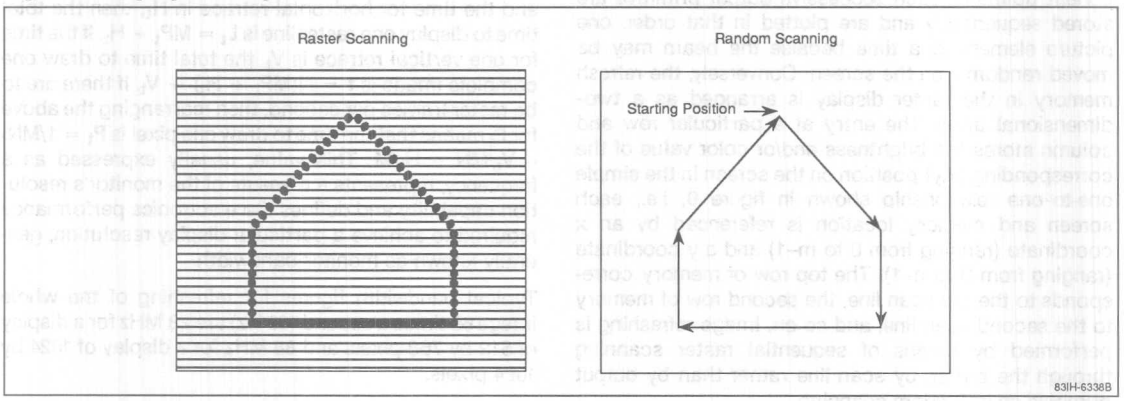
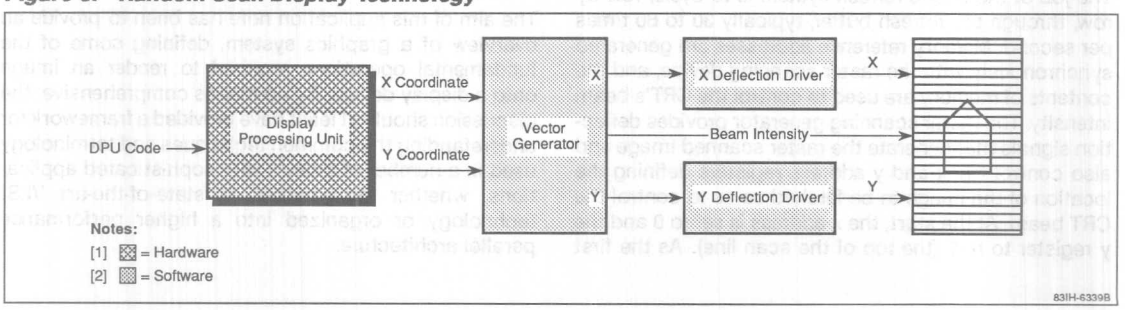


Figure 8. Random Scan Display Technology



Display Processing Unit for Raster Scanning

The DPU illustrated in figure 9 provides a number of features to enhance operation. The CPU loads a DPU program into main memory, loads the DPU with the starting address, and tells the DPU to start the execution of the DPU program. The DPU cycle "steals" from the CPU's memory whenever it needs a new instruction. Thus, converting the display to an autonomous processor relieves the CPU of the refresh task.

Images to be displayed by a random scanning system are encoded as commands to draw each output primitive using endpoints of lines as coordinate data values. The encoding for raster scanning systems is much simpler: output primitives are separated into their constituent points for display.

The major differences in simple point plotters, random scanners, and raster scanners occur in their organization of stored bits. In point plotting displays, the component points of each successive output primitive are stored sequentially and are plotted in that order, one picture element at a time becaise the beam may be moved randomly on the screen. Conversely, the refresh memory in the raster display is arranged as a two-dimensional array. The entry at a particular row and column stores the brightness and/or color value of the corresponding (x,y) position on the screen in the simple one-to-one relationship shown in figure 9, i.e., each screen and memory location is referenced by an x coordinate (ranging from 0 to m–1) and a y coordinate (ranging from 0 to n–1). The top row of memory corresponds to the top scan line, the second row of memory to the second scan line, and so on. Image refreshing is performed by means of sequential raster scanning through the buffer, by scan line rather than by output primitive as in random scanning.

The job of the image refresh system is to cycle, row by row, through the refresh buffer, typically 30 to 60 times per second. Memory reference addresses are generated synchronously with the raster scanning device, and the contents of memory are used to control the CRT's beam intensity. The raster scanning generator provides deflection signals that generate the raster scanned image and also control the x and y address registers defining the location of the image to be fetched so as to control the CRT beam. At the start, the x address is set to 0 and the y register to n–1 (the top of the scan line). As the first scan line is generated, the x address increments from m–1. Each point is fetched and used to control the intensity of the CRT beam. After the first scan line, the x address is reset to 0 and the y address decrements by 1. The process continues until the last scan line (y = 0) is generated.

Display Resolution

The number of raster lines capable of being displayed on a monitor depends not only on the speed at which the electronic beam can be moved across the screen, but also on the quality of the electronics controlling the beam. Similarly, the number of horizontal points that can be plotted depends on the speed at which the beam can be switched on and off. The more raster lines and horizontal points that can be drawn, the greater the total number of points that can be displayed, and hence, the greater the resolution of the display.

Consider a CRT monitor with m pixels on each line and n raster lines. If the time required to draw one pixel is P_t and the time for horizontal retrace in H_t, then the total time to display one raster line is $L_t = MP_t + H_t$. If the time for one vertical retrace is V_t, the total time to draw one complete image is $t = N(MP_t + H_t) + V_t$. If there are to be raster frames per second, then rearranging the above for P_t means that the time to draw one pixel is $P_t = 1/MN_r - V_t/MN - H_t/M$. This value, usually expressed as a frequency, represents a measure of the monitor's resolution capability and defines the electronics performance required to achieve a particular display resolution, generally known as monitor bandwidth.

Typical bandwidth figures for refreshing of the whole image 60 times a second (60 Hz) are 28 MHz for a display of 512 by 768 pixels and 88 MHz for a display of 1024 by 1024 pixels.

SUMMARY

The aim of this application note has been to provide an overview of a graphics system, defining some of the fundamental operations required to render an image onto a display device. By no means comprehensive, the discussion should at least have provided a framework for understanding the common techniques and terminology used in a number of today's very sophisticated applications, whether implemented in state-of-the-art VLSI technology or organized into a higher performance parallel architecture.

Figure 9. Raster Scanning Display Technology

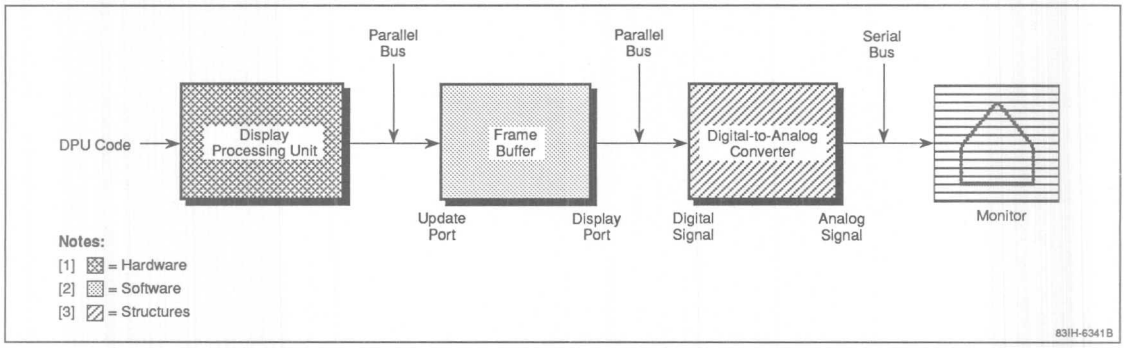
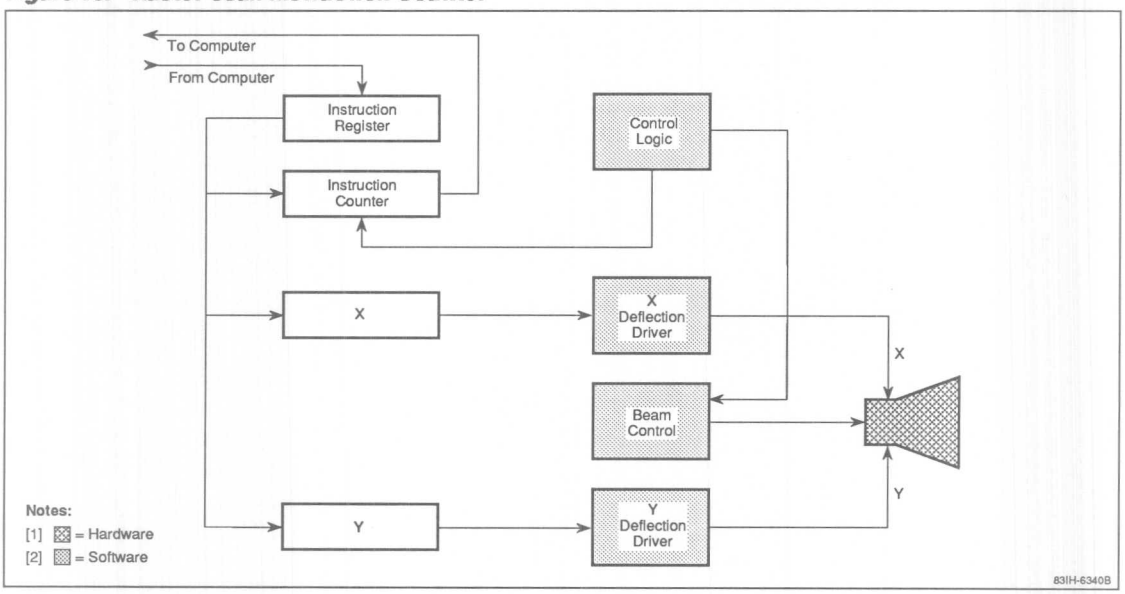
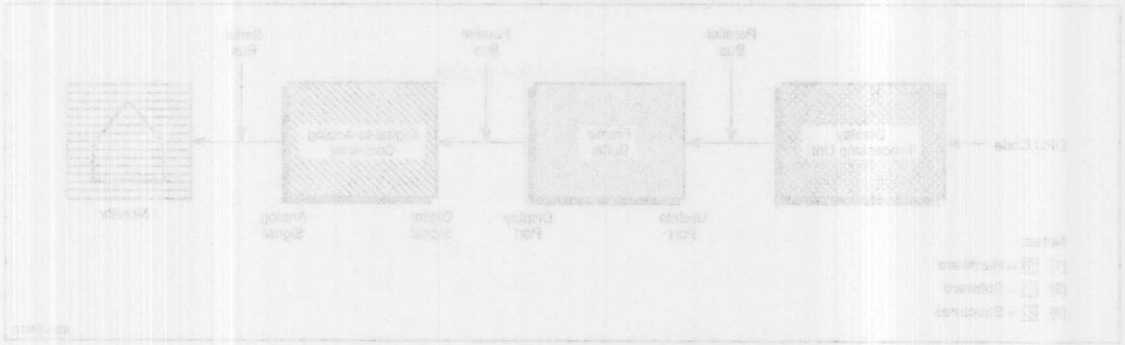
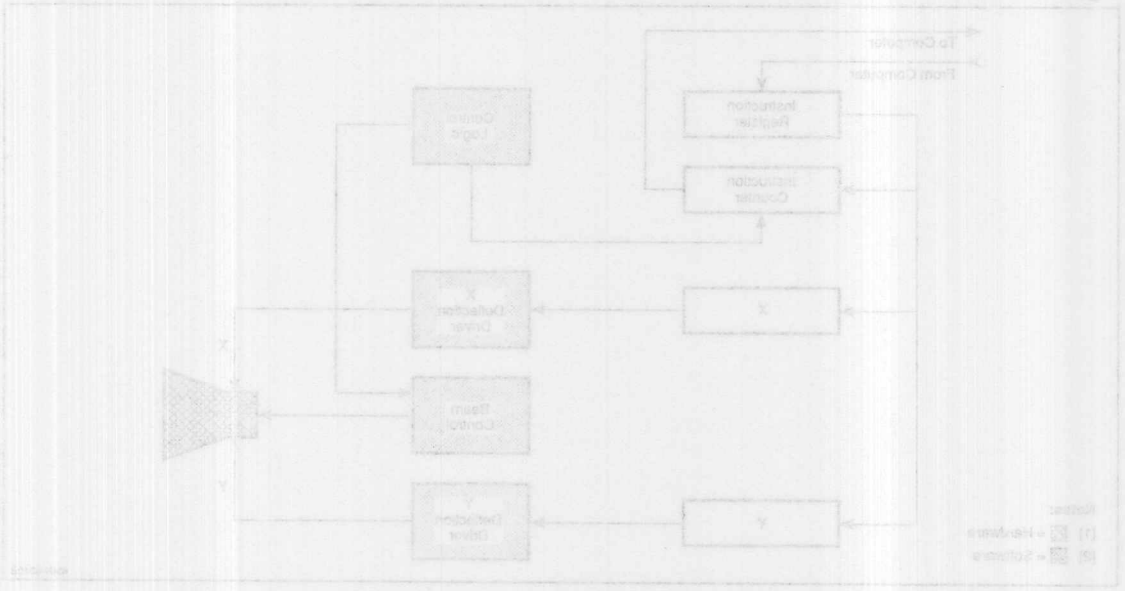


Figure 10. Raster Scan Instruction Counter



3





Introduction

The growth of computer graphics is directly attributed to the availability of reasonably priced, high quality display hardware. The technology most successfully addressing this feature is called raster scanning, a type of graphics found in television applications and one that makes it possible for complex, flicker-free images to be displayed.

Frame buffer architecture is important in determining the performance of the entire raster display system. For example, although frame buffer architecture is restricted by the refresh requirements of the display (i.e., how fast a new image can be generated in response to user input), architecture of the entire graphics system is affected as well. This application note discusses some of the design techniques inherent to frame buffer architecture.

Raster Scanning

A raster display system constructs an image as a series of horizontal lines, each composed of picture elements (pixels) whose intensity is controlled by a bit map generated on the display processing unit (DPU) in accordance with graphics primitives defining the unit. The device buffering the bit-mapped image is called the frame buffer, or image memory, and is usually designed with dynamic RAMs (figure 1). Each storage cell in the frame buffer corresponds to a pixel that maps to a point on the display screen. Data stored in the frame buffer is systematically read by the DPU (video controller) and then used to refresh the CRT monitor displaying the image.

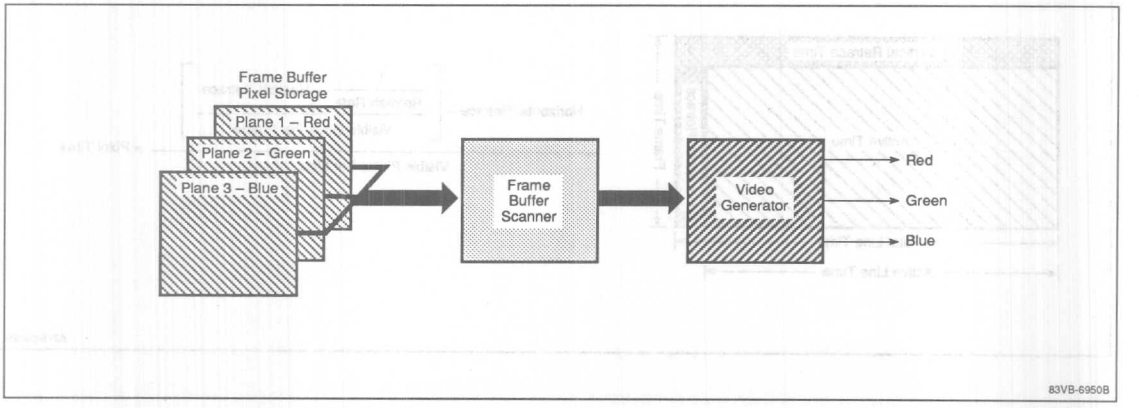
Frame buffers are usually sized in the horizontal and vertical directions as a power of 2, in particular 256 by 256 (2^8), 512 by 512 (2^9), or 1024 by 1024 (2^{10}) pixels. Sizes based on the aspect ratio of the screen (e.g., 768 by 512 or 1536 by 1024) are also common. These dimensions then become device coordinates of the raster scanning display system.

The bits in the frame buffer are scanned by the DPU in a left-to-right, top-to-bottom sequence. They are then read in parallel and serialized by a scanner that outputs the pixels to the video generator. The pixels modulate the CRT beam signal in proportion to the values in the frame buffer.

Refresh Requirements

The design of frame buffers is determined in large part by the requirements of the application. A stable display is generally the foremost requirement of a graphics system. Therefore, the first design consideration should focus on how the video's refresh controller will supply data to the output hardware when pixel time is less than a buffer cycle.

Figure 1. Frame Buffer Organization



The frame or image buffer stores a bit map representing the image to be displayed. The size of the frame buffer, often 512 by 512 or 1024 by 1024, is the resolution of the memory, with each element being one pixel. The DPU must update the frame buffer with the bit-mapped image and periodically refresh the display. Refresh requirements are determined by a number of factors, including the DPU's refresh rate, vertical and horizontal retrace time, screen resolution, and access time of the memory used in the frame buffer. When all of these factors are established, the architecture of the frame buffer can be determined.

Two standards developed by the Electronic Industries Association (EIA) define the timing of video signals. EIA standard RS-170-A specifies interlaced video signals at 30 frames of 525 lines per second each for typical television applications, RS-343-A specifies 30 frames of 1024 by 1024 noninterlaced images per second or 30 frames of 512 by 512 noninterlaced images per second for high-resolution television applications.

Knowing how often a new pixel must be supplied to the output device is crucial to determining how quickly image memory must be accessed to support the refresh requirement. Pixel time, the active line time divided by the number of visible pixels per line, can be derived from either the refresh rate, the vertical or horizontal blanking interval, the number of lines displayed per frame, or the number of pixels displayed per line (figure 2).

Table 1 gives the values used to derive pixel times for several popular display formats. Pixel times will vary from system to system, depending on the number of visible lines and the number of pixels per scan line. However, these figures are typical: (1) 100 ns for 512 x 512 at 30 Hz; (2) 45 ns for 512 x 512 at 60 Hz; (3) 25 ns for 1024 x 1024 at 30 Hz; and (4) 10 ns for 1024 x 1024 at 60 Hz.

The storage cell is the principal element in a frame buffer, which is why advances in frame buffer architectures have been paced by advances in the cost, performance and structure of these chips. Storage bandwidth is of primary concern in the design of frame buffers, and while dynamic devices have historically evolved to deeper and deeper organizations, the width of the access port (e.g., 1M x 1 or 256K x 4) has experienced almost no change.

The trend toward deeper organization meets the needs of main buffer designs, but doesn't provide a solution for potential bandwidth requirements. Furthermore, resolution isn't expected to grow significantly beyond the 1280 by 1024 now used in most applications, which means the need for higher density video buffers is limited (figure 3). Consequently, for a 1K x 1K display operating at 60 Hz, a pixel rate of 10 ns (as well as parallel accessing of the frame buffer) is required.

Figure 2. Pixel Time

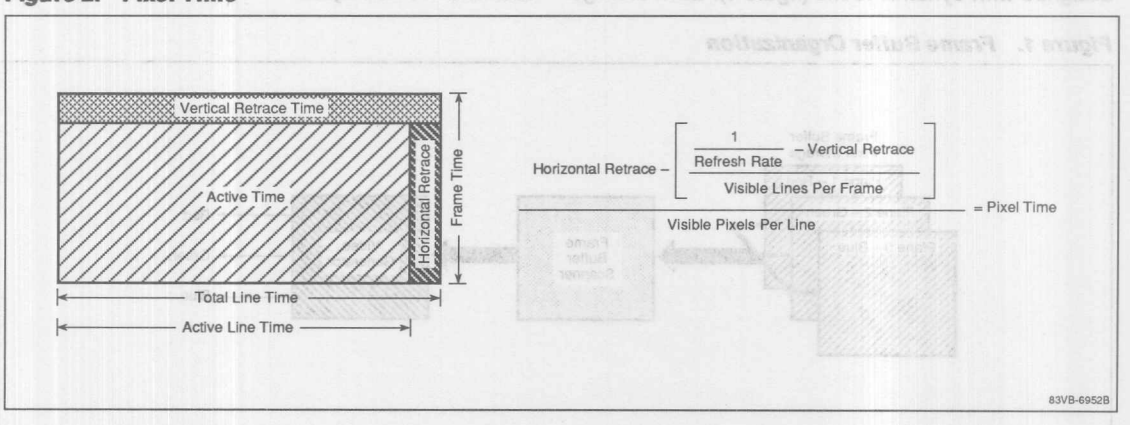


Table 1. Video Timing for Various Display Formats

Visible Area Pixels x Lines	Refresh Rate (Hz)	Interlaced	Vertical Retrace Time (μs)	Horizontal Retrace Time (μs)	Total Line Time (μs)	Pixel Time (μs)
512 x 485	30	Yes	1271	10.9	63.56	102.80
640 x 485	30	Yes	1271	10.9	63.56	82.30
512 x 512	30	Yes	1203	10.9	60.40	96.70
1024 x 768	30	Yes	1250 [1]	7.0 [1]	40.10	32.37
1024 x 1024	30	Yes	1250	7.0	30.11	22.57
1280 x 960	30	Yes	1250	7.0	32.12	19.62
512 x 485	60	No	1250	7.0	31.79	48.41
640 x 485	60	No	1250	7.0	31.79	38.73
512 x 512	60	No	1250	7.0	30.11	45.14
1024 x 0768	60	No	600 [2]	4.0 [2]	20.92	16.52
1024 x 1024	60	No	600	4.0	15.69	11.42
1280 x 960	60	No	600	4.0	16.74	9.95
1280 x 1024	60	No	600	4.0	15.69	9.13

Notes:

(1) Nominal RS-343-A specifications.

(2) Typical high-performance monitor specifications.

Figure 3. Color Monitor Standards

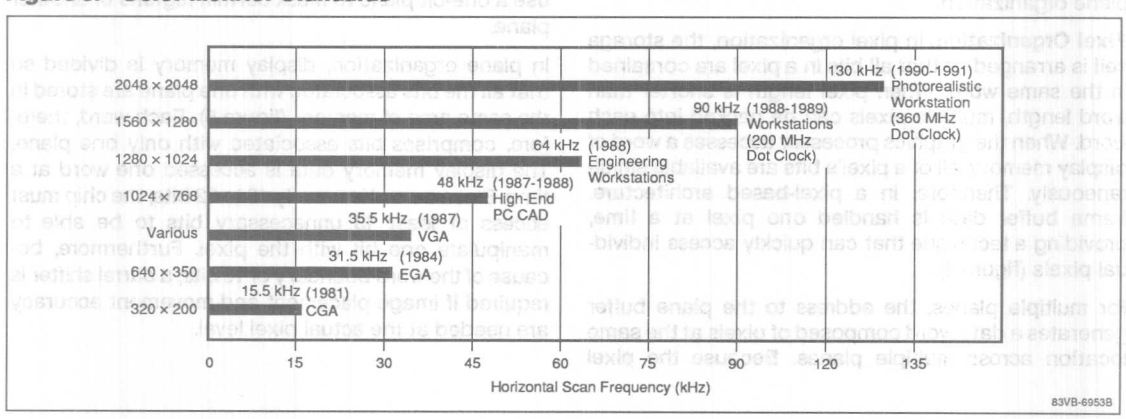


Table 2 shows the effect of using a device with a 4-bit organization, which can read and write four bits in a single cycle and provide four times the bandwidth of a 1-bit chip of equal capacity. This wider organization has figured prominently in frame buffer design, and as system performance requirements increase, ever wider organization may be required.

Table 2. Performance of Storage Chip

Organization	Time to Fill (ms)
4K x 1	1.6
16K x 1	6.6
64K x 1	26.2
256K x 1	105.0
16K x 4	6.6
64K x 4	26.2

tion toward 16-bit devices will be prohibitive because of pin configuration and package size. Therefore, in order to meet the required pixel rate of high performance graphics systems, the frame buffer must be designed with organizations and features that can best support the increasing performance requirements. Over the years, a number of different design solutions have been proposed. One is to separate the device into a double buffer, one for refreshing the display and the other for updating the image. Another approach is to incorporate the functions needed to update and refresh a display into a VLSI DRAM architecture. Both of these architectures are important in determining overall performance, but the organization of the frame buffer also plays an important role in optimizing its performance in various applications.

Organization

How pixel values are mapped into the update processor's address space has a substantial impact on the speed with which the processor can alter the memory. Two basic types of organization are commonly used to store and access pixels in display memory: pixel and plane organization.

Pixel Organization. In pixel organization, the storage cell is arranged so that all bits in a pixel are contained in the same word. When pixel length is shorter than word length, multiple pixels can be packed into each word. When the graphics processor accesses a word of display memory, all of a pixel's bits are available simultaneously. Therefore, in a pixel-based architecture, frame buffer data is handled one pixel at a time, providing a technique that can quickly access individual pixels (figure 4).

For multiple planes, the address to the plane buffer generates a data word composed of pixels at the same location across multiple planes. Because the pixel organization addresses individual pixels, there are no problems regarding word alignment during image transfers. This architecture is often found in image processing and solid modeling applications, where the value of each pixel is very computation-intensive because of color value or shading variations.

Plane Organization. In plane organization, the frame buffer may be viewed as a number of separate planes, where the number of planes in the frame buffer is equal to the number of bits in a pixel. In a two-dimensional display memory, each pixel consists of one bit, which can be either on or off, indicating the presence or absence of a dot. Such a display memory supports a monochrome, single-intensity display. In a color display, additional bits at each pixel add color and control the intensity. A four-bit pixel, for instance, can control the CRT's red, blue and green color guns, as well as the pixel's intensity. Each bit with the pixel corresponds to a separate plane.

Planes can provide information other than color. For example, one plane can show a static picture, while another displays an icon that the user can drag around the screen with a mouse. Alternatively, it is possible to use a one-bit plane to mask certain regions of another plane.

In plane organization, display memory is divided so that all the bits associated with one plane are stored in the same area of memory (figure 5). Each word, therefore, comprises bits associated with only one plane. The display memory data is accessed one word at a time. Since a word is usually 16 to 32 bits, the chip must access at least 15 unnecessary bits to be able to manipulate one bit with the pixel. Furthermore, because of the word boundary of 16 bits, a barrel shifter is required if image placement and movement accuracy are needed at the actual pixel level.

Figure 4. Pixel Access

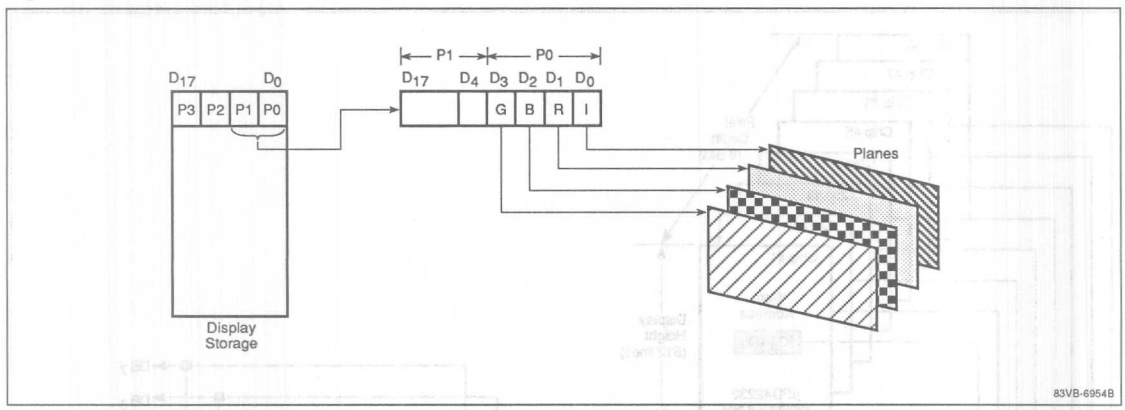
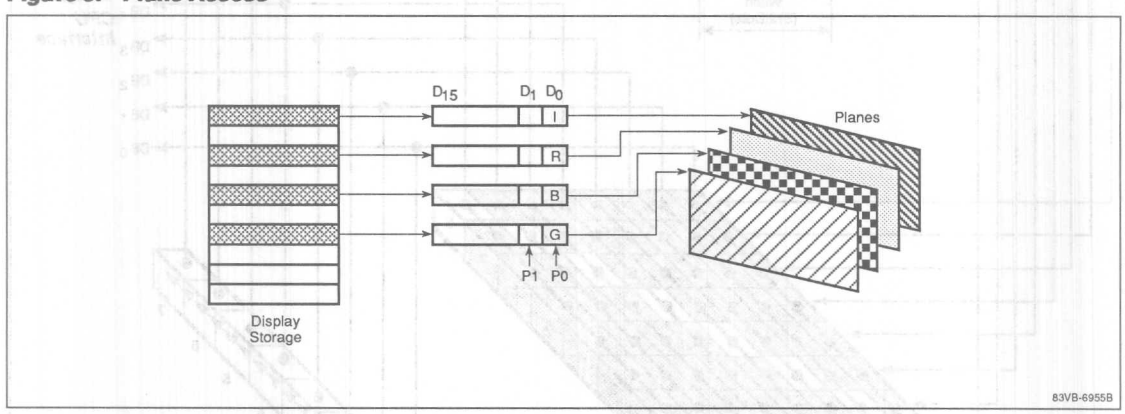


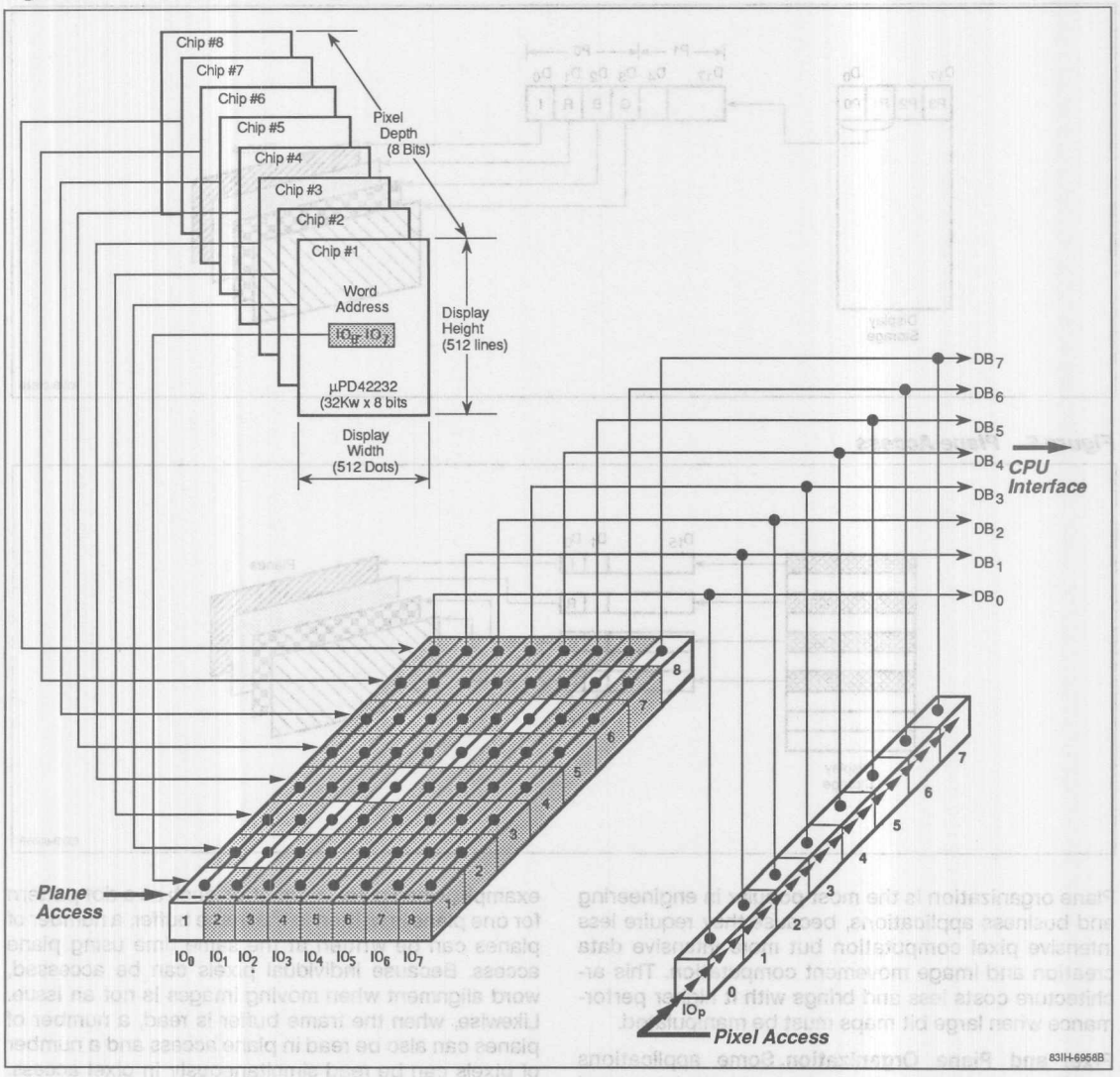
Figure 5. Plane Access



Plane organization is the most popular in engineering and business applications, because they require less intensive pixel computation but more intensive data creation and image movement computation. This architecture costs less and brings with it higher performance when large bit maps must be manipulated.

Pixel and Plane Organization. Some applications need both types of access, in which case the integrated organization shown in figure 6 may be implemented. Access to the frame buffer can be either at word width or pixel depth, providing the best of both types. For example, when pixel information such as a dot pattern for one plane is written to the frame buffer, a number of planes can be written at the same time using plane access. Because individual pixels can be accessed, word alignment when moving images is not an issue. Likewise, when the frame buffer is read, a number of planes can also be read in plane access and a number of pixels can be read simultaneously in pixel access. This enhances comparison functions such as color detection (pixel access) and pattern detection (plane access).

Figure 6. Plane and Pixel Access



Word Alignment

Although plane organization is implemented in a number of popular graphics systems, restrictions associated with word boundary constraints have limited the flexibility and performance of these systems. The pixel and plane combination solves this problem by providing the ability to first access each pixel individually and then switch to plane access.

At the graphic processor level, a number of manufacturers have provided the ability to switch between pixel and plane access or provide a function to align word boundaries. For example, NEC's μPD72120 Advanced Graphics Display Controller™ provides both plane and pixel access. National Semiconductor's graphics chip set uses a plane organization, but takes another approach to this issue by including a BITBLT (bit-boundary block transfer) processing unit chip that is a slave to the raster graphics processor and performs all the masking, word alignment, barrel shifting, data transfer, and Boolean logic necessary for BITBLT operations.

Access Modes

The plane and pixel organizations provide a means of organizing the frame buffer in such a way that its performance is optimized for a number of applications. Also, by providing logical and arithmetic functions that operate on arrays of data, the transfer of data between the graphics processor and the frame buffer can be optimized. These logical and arithmetic functions can be implemented in the instruction set of the graphics buffer or in the architecture of the frame buffer, depending on the application.

BITBLT Operation

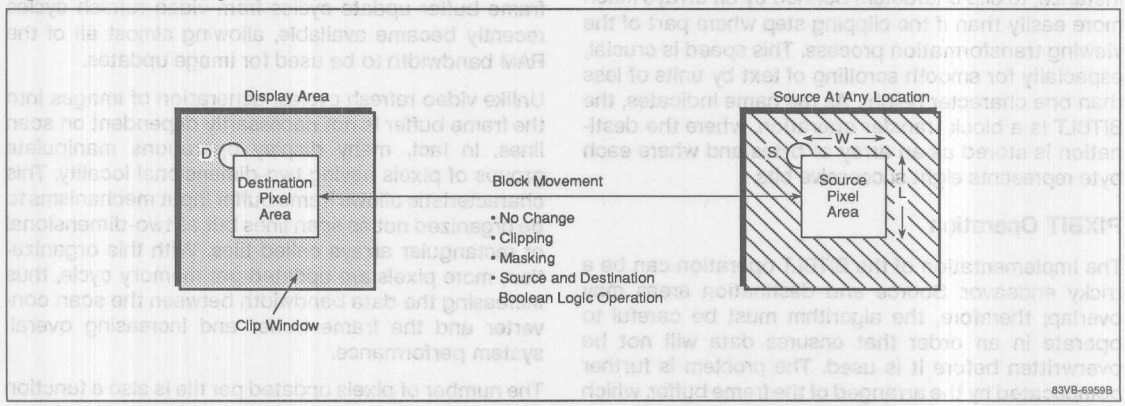
The BITBLT instruction, first developed on the Alto system, provides a powerful capability for bit operation on rectangular areas having the same heights and widths:

- Moves rectangular regions of pixels and is not restricted to contiguous linear arrays
- Operates at any pixel boundary and is not restricted to byte or word boundaries
- Is able to mix the source and destination pixels with a Boolean logical operation and is not restricted to a simple replace destination with source transfer

The instruction copies a source array into a destination array, where the destination array is derived by applying a given logical operation called the *combining rule* to pairs of bits in corresponding positions in the two arrays (figure 7).

The original concept of BITBLT entails a set of 16 specific combining rules that are one of the 16 Boolean operations defined in table 3. The AND function uses its source as a mask to selectively clear parts of the destination, while the OR function selectively sets parts of the destination. Thus the OR can be used to paint shapes into the refresh buffer, perhaps under control of a mouse or tablet. Another use of the OR function is to place text characters defined by bit arrays into a refresh buffer without changing the background pixels around those that form the character itself.

Figure 7. BITBLT Operation



μPD72120 Advanced Graphics Display Controller is a trademark of NEC Corporation.

Table 3. BITBLT Combination Rules

Bit Pattern	Boolean Expression	Operation
0000	d := 0	CR_*0*
0001	d := s • d	CR_*AND*
0010	d := s • $(\overline{d})$	CR_*SND*
0011	d := s	CR_*S*
0100	d := $(\overline{s})$ • d	CR_*DNS*
0101	d := d	CR_*D*
0110	d := s ⊕ d	CR_*XOR*
0111	d := s + d	CR_*OR*
1000	d := $\overline{(s + d)}$	CR_*NOR*
1001	d := $\overline{(s \oplus d)}$	CR_*NXOR*
1010	d := $\overline{d}$	CR_*ND*
1011	d := $(\overline{(s)} \cdot d)$	CR_*NDNS*
1100	d := $\overline{s}$	CR_*NS*
1101	d := $\overline{(s \cdot (d))}$	CR_*NSND*
1110	d := $\overline{(s \cdot d)}$	CR_*NAND*
1111	d := 1	CR_*1*

Notes:

(1) s and d are the source and destination bits.

(2) •, $\overline{\ }$, ⊕, and + are Boolean AND, NOT, XOR, OR operators, respectively.

Some versions of BITBLT also use a 16 by 16 pixel halftone or pattern array that functions as an addition mask (figure 8). The halftone array can be used in place of the source or can be ANDed with the source prior to being combined with the destination. This same version of BITBLT also allows a clipping region to be associated with the destination. This can be used, for instance, to clip characters defined by bit arrays much more easily than if the clipping step where part of the viewing transformation process. This speed is crucial, especially for smooth scrolling of text by units of less than one character height. As the name indicates, the BITBLT is a block transfer operation, where the destination is stored as an array of bytes and where each byte represents eight successive bits.

PIXBIT Operation

The implementation of the BITBLT operation can be a tricky endeavor. Source and destination areas may overlap; therefore, the algorithm must be careful to operate in an order that ensures data will not be overwritten before it is used. The problem is further complicated by the arranged of the frame buffer, which is often arranged with 16 or 32 horizontally adjacent pixels in a single word. Because regions do not necessarily fall on word boundaries, corresponding pixels in source and destination words may fall at different bit positions with the words. In order to operate on several pixels within each memory word in parallel, two source words must be available to be aligned with the data within the destination data word. The logical operation is then applied to the aligned words, and the result written to the destination location. This must be repeated for each word containing a destination pixel.

The PIXBLT operation eliminates the need to align operands on word boundaries, because the PIXBLT operation accesses pixels and not words or bytes. The basic PIXBLT algorithm supports combination rules (similar to those found in BITBLT operation) and automatically aligns the source and destination arrays. PIXBLTs operate on multibit pixels, which gives them a speed advantage over BITBLTs in color systems because they perform the operation on all planes at once. They can perform logical and arithmetic operations, transparency detection, plane masking, and color expansion. Because PIXBLTs perform arithmetic operations that require the processor to have the ability to handle carries between bits, a PIXBLT can only be implemented with a frame buffer that has pixel organization. PIXBLTs are useful for performing the Bresenham anti-aliasing algorithm for line drawing primitives.

TILE Organization

Traditional frame buffers are designed so that sequential memory locations lie along a scan line. To refresh a raster scan display, the sequential pixels must be provided at a very high speed. In the past, display refreshing required a significant percentage of the available RAM bandwidth. Video RAMs that separate frame buffer update cycles from video refresh cycles recently became available, allowing almost all of the RAM bandwidth to be used for image updates.

Unlike video refresh cycles, generation of images into the frame buffer is not necessarily dependent on scan lines. In fact, many display operations manipulate groups of pixels having two-dimensional locality. This characteristic allows frame buffer input mechanisms to be organized not as scan lines but as two-dimensional or rectangular arrays called tiles. With this organization, more pixels are updated per memory cycle, thus increasing the data bandwidth between the scan converter and the frame buffer and increasing overall system performance.

The number of pixels updated per tile is also a function of tile organization and the type of operation being performed. In a pixel/plane architecture, tile organizations can be readily handled because packed pixels

can be sequentially accessed. For randomly oriented vectors, a square tile organization gives the highest average number of pixel updates per memory cycle. For horizontal vectors that include polygon fill, a tile organization linearly in the horizontal dimension gives the highest number of pixel updates per cycle.

- A tile is the maximum, simultaneous work area for the graphics processor.
- The more pixels updated per cycle, the higher the pixel performance.
- The number of pixels updated per cycle is a function of tile size.
- The number of pixels updated per tile is also a function of tile organization and the type of operation being performed.

Figure 9 shows an example of a one-plane buffer that supports 4 x 4 tiles and 16 x 1 tiles. The RAM has 16 data lines, with each of the four groups of data lines (A, B, C and D) able to receive a different address. The illustration shows how data lines in the storage array map into the display. Note that for any 16 consecutive pixels in the horizontal direction, each comes from a different data line. Also, in any 4 x 4 group of pixels, each of the 16 comes from a different data line in the array, allowing access of 16 pixels to originate from either a 16 x 1 or 4 x 4 tile, based on the addresses supplied to the different groups of RAM. To access a 16 x 1 tile, all groups of RAM receive the same address. To access a 4 x 4 tile, each group of RAM receives a different address, namely ADDR, ADDR+ M, ADDR+ 2M, and ADDR+ 3M (where M = consecutive memory addresses). Which group of RAM gets each of these addresses depends on the particular 4 x 4 tile being accessed. The fact that the four data lines within a group always have the same address fixes the tiles on four-bit boundaries.

Figure 8. Examples of Combination Rules

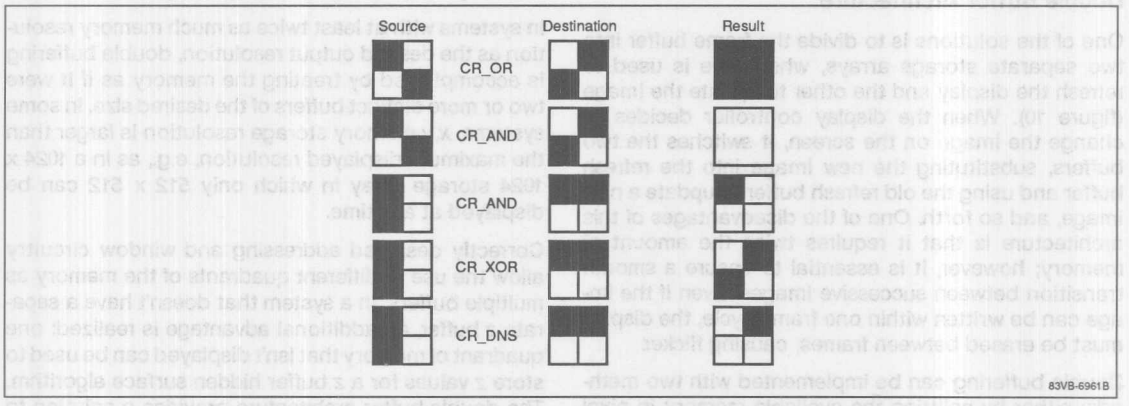
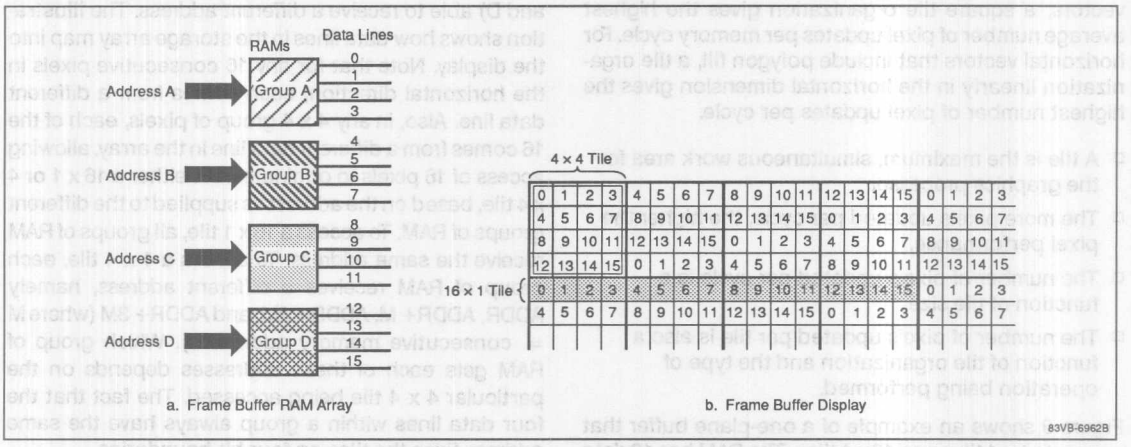


Figure 9. Tile Organization



FRAME BUFFER ARCHITECTURES

Double Buffer Architecture

One of the solutions is to divide the frame buffer into two separate storage arrays, where one is used to refresh the display and the other to update the image (figure 10). When the display controller decides to change the image on the screen, it switches the two buffers, substituting the new image into the refresh buffer and using the old refresh buffer to update a new image, and so forth. One of the disadvantages of this architecture is that it requires twice the amount of memory; however, it is essential to ensure a smooth transition between successive images. Even if the image can be written within one frame cycle, the display must be erased between frames, causing flicker.

Double buffering can be implemented with two methods: either by splitting the available memory in pixel depth and using two buffers with reduced color resolution, or by splitting the *x,y* resolution of the memory and retaining full pixel depth. When the two buffers use entirely separate sets of memory chips, the display processor and the video refresh processor have complete access to their respective memories. If the buffers must share memory chips, little or no access improvement results, but image transition is smoothed.

A 512 x 512 x 32-bit frame buffer can be treated as two 512 x 512 x 16-bit buffers. In some cases, the lost color resolution can be regained in the video output chain. The advantage of the pixel depth-splitting approach is that the system can be used as a single-buffer system for full color applications, and as a double-buffered system with reduced color resolution for applications that may not need full-color capability.

In systems with at least twice as much memory resolution as the desired output resolution, double buffering is accomplished by treating the memory as if it were two or more distinct buffers of the desired size. In some systems, *x,y* memory storage resolution is larger than the maximum displayed resolution, e.g., as in a 1024 x 1024 storage array in which only 512 x 512 can be displayed at any time.

Correctly designed addressing and window circuitry allow the use of different quadrants of the memory as multiple buffers. In a system that doesn't have a separate *z* buffer, an additional advantage is realized: one quadrant of memory that isn't displayed can be used to store *z* values for a *z* buffer hidden surface algorithm. The double-buffer architecture provides a solution to the display processor/frame buffer bandwidth problem, but at the expense of additional cost and complexity. A much more classical solution to this bandwidth problem is found in dual-port architectures. Such an architecture is provided by a dual-port graphics buffer, which consists of a random access port (similar to a typical DRAM) and a serial output port.

Dual-Port Graphics Buffer

The fundamental structure of a frame buffer is that of a dual-port memory in which one port is used to read memory values at high speed for displaying and the other port is used by an update processor to change the display image by changing the memory contents

(figure 11). To update the processor, the frame buffer behaves like all other memory in the system. It responds to each request to read or write a byte, a word, or multiple words as required. The display port is controlled by a video generator, which reads from memory the pixel values that correspond to the raster scanning pattern used on the display. The size and speed of the frame buffer must be chosen to match the properties of the display.

The display processor accesses the dual-port graphics buffer via the random access port, and it performs a data transfer from the random access port to the serial port when the display needs to be refreshed. The serial port consists of a large video shift register. The addressing of the memory is arranged so that a row of the memory chip contains bits that describe adjacent pixels on a scan line. The shift register is loaded at the beginning of the scan line, and then shifted to obtain the values of subsequent pixels. Because the shift register can only operate at 33 MHz, several chips are usually operated in parallel, and a final high-speed video multiplexer produces values at pixel rates.

Figure 10. Double-Buffer Architecture

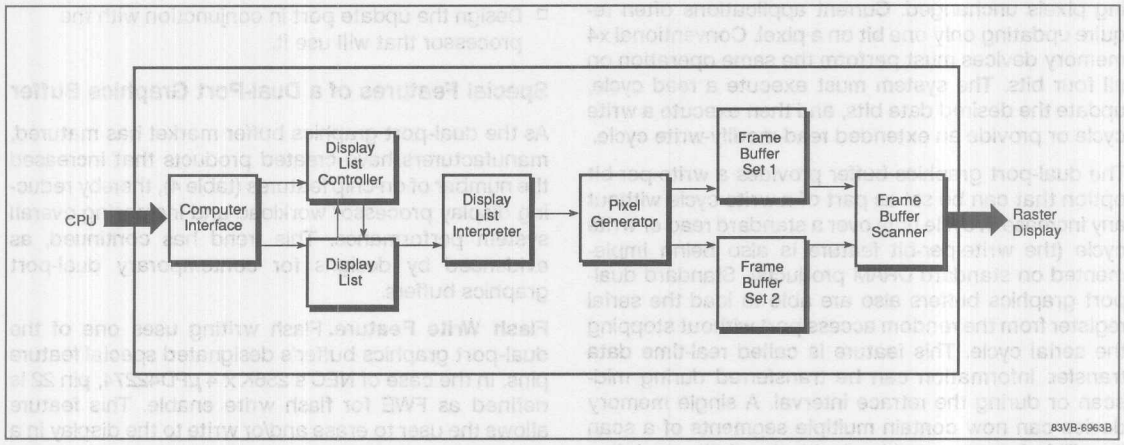
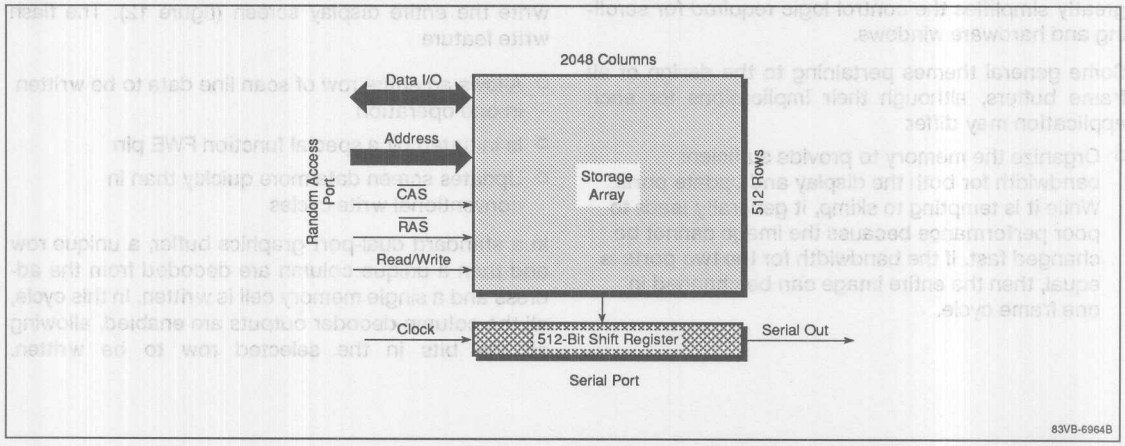


Figure 11. Dual-Port Graphics Buffer Architecture



The shift register in a dual-port graphics buffer increases the bandwith available relative to a typical RAM chip by a factor of 6 to 8 in a way that directly benefits frame buffer display designs. For display refresh cycles, 512 bits are obtained with a single row access cycle, and therefore almost 100% of the normal row/column accesses can be devoted to the update port. Only infrequently must the update accesses be suspended so that a row address can reload the shift register.

Several system-oriented features were incorporated into the 64K x 4 dual-port graphics buffer architecture, including a mask function that provides the ability to alter some of the pixel values while leaving the remaining pixels unchanged. Current applications often require updating only one bit on a pixel. Conventional x4 memory devices must perform the same operation on all four bits. The system must execute a read cycle, update the desired data bits, and then execute a write cycle or provide an extended read-modify-write cycle.

The dual-port graphics buffer provides a write-per-bit option that can be set as part of a write cycle without any increase in cycle time over a standard read or write cycle (the write-per-bit feature is also being implemented on standard DRAM products). Standard dual-port graphics buffers also are able to load the serial register from the random access port without stopping the serial cycle. This feature is called real-time data transfer. Information can be transferred during mid-scan or during the retrace interval. A single memory device can now contain multiple segments of a scan line. This feature, combined with the ability to define the starting location of the serial port (pointer control) greatly simplifies the control logic required for scrolling and hardware windows.

Some general themes pertaining to the design of all frame buffers, although their implications for each application may differ.

- Organize the memory to provide sufficient bandwidth for both the display and update ports. While it is tempting to skimp, it generally leads to poor performance because the image cannot be changed fast. If the bandwidth for the two ports is equal, then the entire image can be changed in one frame cycle.
- Organize the update port to access the pixel data required. For example, if an application often alters only a single plane of memory at a time, a pixel access architecture is inefficient because each memory access yields all bits of a pixel rather than just the plane needing to be changed.
- Organize the memory so that the spatial organization of the update port accesses those pixels that often need to be changed. The conventional organization, which alters a horizontal group of pixels in one access, is inefficient for writing thin vertical lines in the frame buffer.
- Design the update port in conjunction with the processor that will use it.

Special Features of a Dual-Port Graphics Buffer

As the dual-port graphics buffer market has matured, manufacturers have created products that increased the number of on-chip features (table 4), thereby reducing display processor workload and increasing overall system performance. This trend has continued, as evidenced by designs for contemporary dual-port graphics buffers.

Flash Write Feature. Flash writing uses one of the dual-port graphics buffer's designated special feature pins. In the case of NEC's 256K x 4 μPD42274, pin 22 is defined as FWE for flash write enable. This feature allows the user to erase and/or write to the display in a much faster time than is required using the conventional method, thus enhancing applications that clear/write the entire display screen (figure 12). The flash write feature

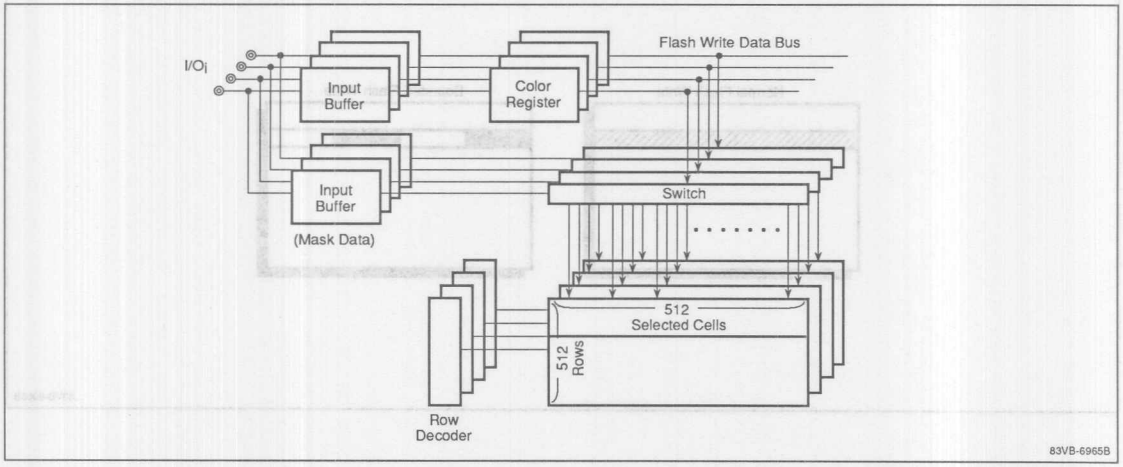
- Allows an entire row of scan line data to be written in one operation
- Is initiated by a special function FWE pin
- Updates screen data more quickly than in conventional write cycles

In a standard dual-port graphics buffer, a unique row and then a unique column are decoded from the address and a single memory cell is written. In this cycle, all the column decoder outputs are enabled, allowing all the bits in the selected row to be written.

Table 4. Feature Comparison

Device Features	μPD42273/ μPD42274	μPD42275	TC524256	TC524256A/258A TC528128A			TMX44C251	MB81C4251/3	HM534252	HM534253	M5M442256
Vendor	NEC	NEC	Toshiba	Toshiba			TI	Fujitsu	Hitachi	Hitachi	Mitsubishi
Configuration	x4	x8	x4	x4		x8	x4	x4	x4	x4	x4
				256A	258A	128A					
Fast-Page	Yes	Yes	No	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes
Flash Write	No/Yes	Yes	No	No	Yes	Yes	No	Yes	No	Yes	Yes
Serial Buffer	Single	Split	Single	Single	Split	Split	Split	Single	Single	Double	Split
Serial Input	No	No	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes
Block Write	No	Yes	No	No	Yes	Yes	Yes	No	No	No	Yes
Raster Operation	No	No	No	No	No	No	No	No	Yes	No	No
600-mil, 28-pin DIP	No	N/A	No	No		No	No	Yes	No	No	No
400-mil, 28-pin ZIP	Yes	N/A	Yes	Yes		N/A	Yes	Yes	Yes	Yes	Yes
400-mil, 28-pin SOJ	Yes	N/A	Yes	Yes		N/A	Yes	No	Yes	Yes	Yes
600-mil, 40-pin DIP	N/A	No	N/A	N/A		Yes	N/A	N/A	N/A	N/A	N/A
400-mil, 40-pin SOJ	N/A	Yes	N/A	N/A		Yes	N/A	N/A	N/A	N/A	N/A

Figure 12. Flash Write Operation



Bounded Flash Write Feature. Although flash writing provides a means for clearing/writing a screen very quickly, it can't be used in the window environment popular in today's graphics market. In conventional flash writing, no option exists to write to only a segment of the row that will be needed in a window environment. The bounded flash write feature can provide this function by allowing the user to specify the segment of the scan line to be accessed (figure 13). Bounded flash writing has not been implemented in dual-port graphics buffer architecture, but it deserves some consideration in today's x-window era.

Block Write Feature. Many frame buffer designs address specific performance requirements, but the problem lies in optimizing the architecture of the display processor with the kinds of features that may be needed for a general-purpose dual-port graphics buffer architecture. For example, the BITBLT operation that many graphics processors use to implement windowing applications is used to transfer blocks of data from a source array to a destination array of equal height and width. Because this operation moves a square block of data, system bus performance can be enhanced if the graphics buffer was able to store data in a block format, rather than in four separate sequential scan lines (figure 14). Unlike bounded flash writing, the block move feature has been implemented in several dual-port graphics buffer architectures.

Persistent Write-Per-Bit Feature. The write-per-bit feature is a standard option of dual-port graphics buffers, but in some applications, system timing considerations prohibit the use of this function because of the additional overhead required to supply the mask data on each write cycle. The persistent write-per-bit feature solves this problem by permitting mask data to be written only once (figure 15).

Extended Fast-Page Cycle. The display processor-to-frame buffer bandwidth is a key issue in determining performance of a graphics system. The trend in dual-port graphics buffers has been to follow standard DRAM evolution, expanding memory capacity with each new generation. In many cases, organization and not capacity determines bandwidth of the frame buffer. Therefore, a wider x8 organization would enhance system bandwidth and reduce the number of dual-port buffers needed in frame buffer design.

Another approach is to provide high-speed access such as the fast-page cycle implemented on the 256K x 4-bit generation of dual-port graphics buffers. Bandwidth requirements of fast-page cycles may be inadequate in some applications. The popularity of RISC architectures has created a demand for synchronous pipeline operation, for which extended fast-page access is being proposed. This feature interlaces the internal accesses of the dual-port graphics buffer and latches the data on-chip so that it can then be accessed synchronously, reducing the page access time from 60 ns to 30 ns. Extended fast-page access means that frame buffer designs will be able to increase bandwidth without increasing the size or cost of the device.

Figure 13. Bounded Flash Write Operation

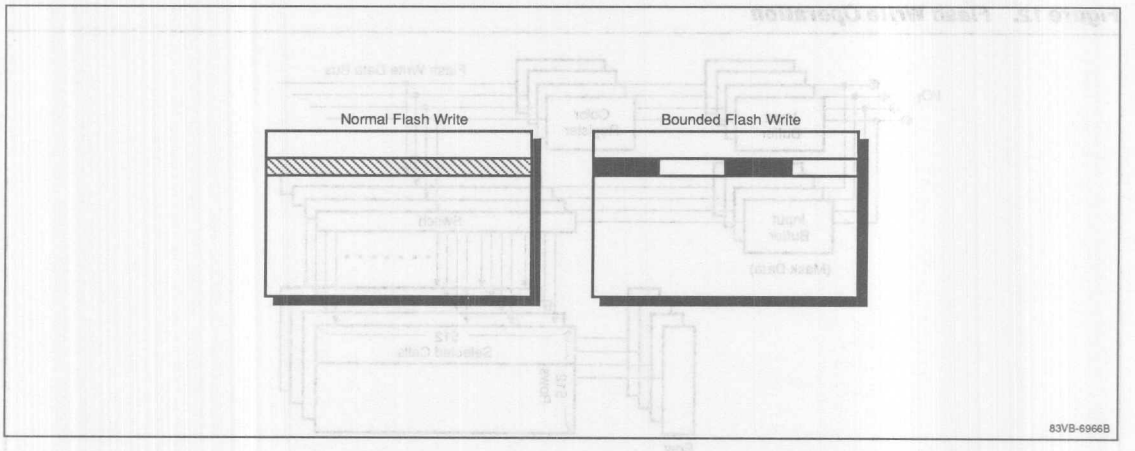


Figure 14. Block Write Feature

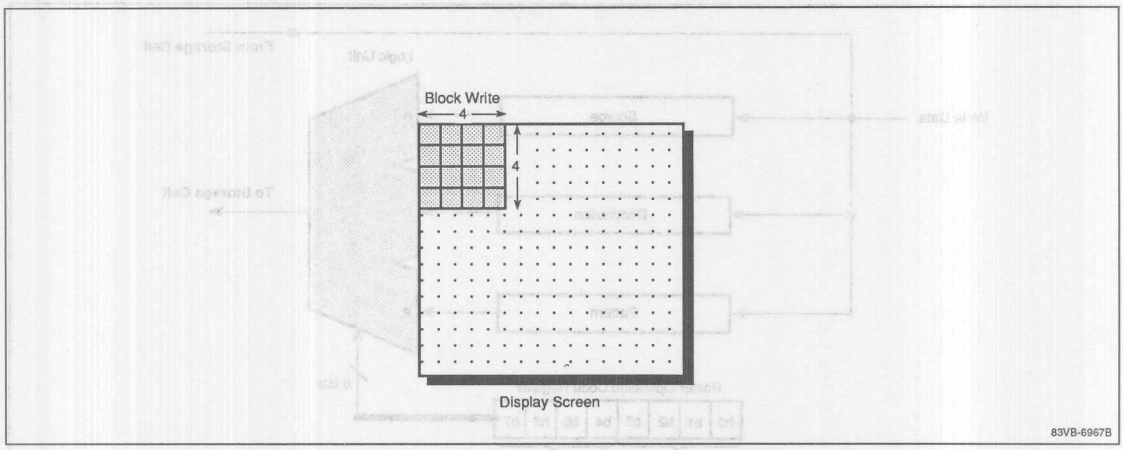
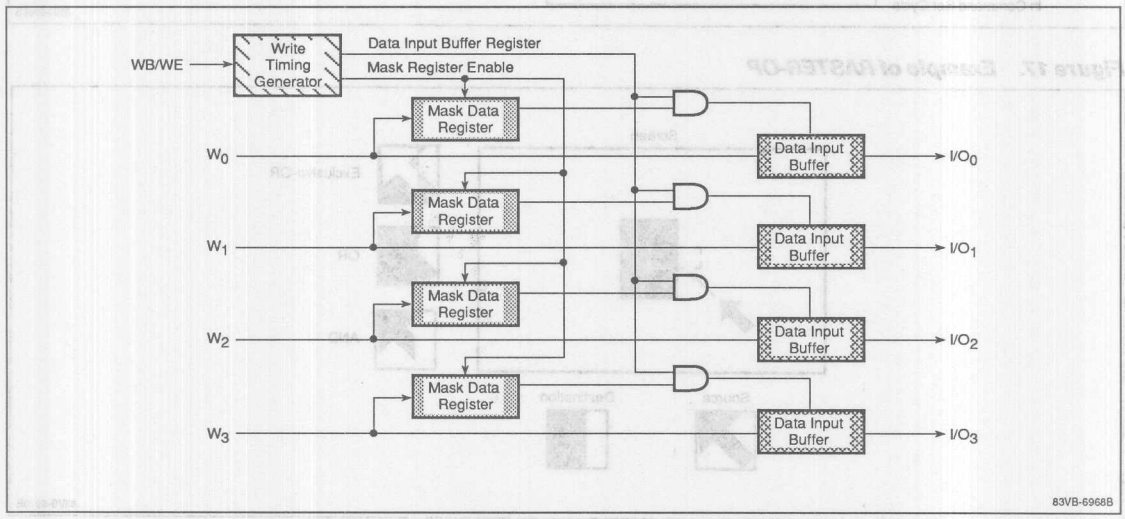


Figure 15. Persistent Write-Per-Bit



Logic and Arithmetic Functions

The BITBLT operation has been defined as a means of copying an array of equal height and width from a source array to a destination array. Additionally, there are a number of combination rules that define how the source data is combined with the destination data to form the new values. There is also a third form called a pattern array that can be combined with the source toproduce a replicate pattern over the destination. Another name for BITBLT is RASTER-OP (figure 16). This nomenclature is pertinent to dual-port graphics buffers because it has been implemented in devices such as the NEC μPD42232™ and the Hitachi HM53462™ (in which it was first introduced).

μPD42232 is a trademark of NEC Corporation.
HM53462 is a trademark of Hitachi.

Figure 16. RASTER-OP Functions

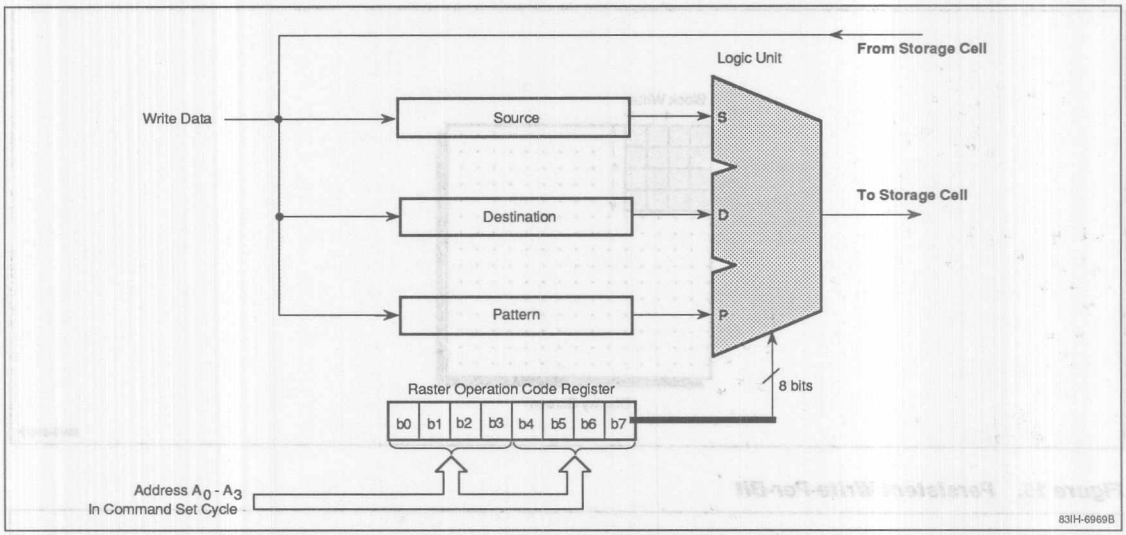
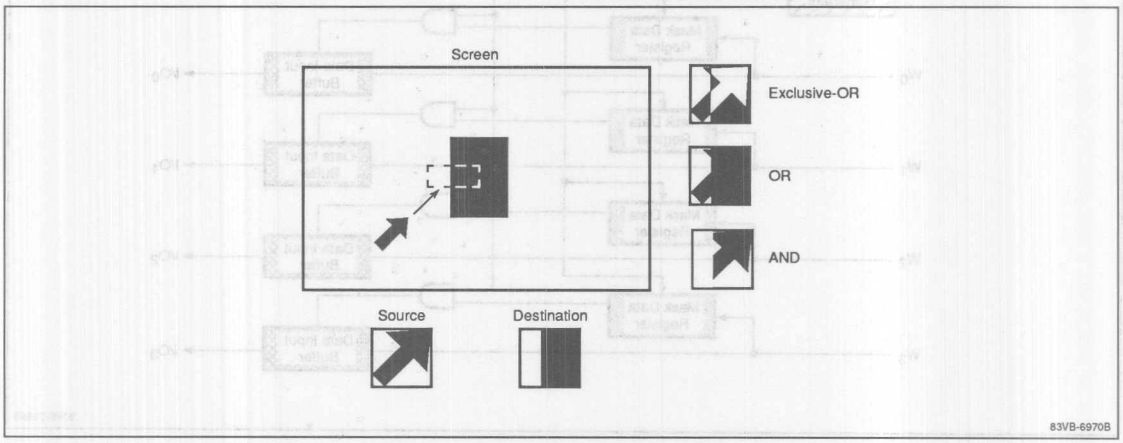


Figure 17. Example of RASTER-OP



The function can be implemented by inserting a logic unit between the input/output buffers and the internal input/output bus amplifier (figure 17). The logic unit is controlled by a 4-bit code that defines one of the 16 combination functions. NEC's μPD42232 approach to on-chip RASTER-OP involves the addition of a third input to the logic unit, a pattern function. This approach is compatible with the classical implementation of BITBLT, but the number of combination functions has been increased from 16 to 256 on the NEC device.Logic functions provided by the RASTER-OP operation are useful in two-dimensional graphics systems, but with the increasing development of three-dimensional systems that require hidden surface removal, three-dimensional polygon filling, etc., there is a requirement for much more powerful computational functions. Several contemporary graphics processors provide a number of pixel processing operations intended to address the requirements of three-dimensional systems.

One example is the pixel-planes graphics engine architecture, which replaces the rasterizer, frame buffer, and video controller of a conventional system. Its main

component is a "smart frame buffer" composed of custom VLSI enhanced memory chips that address the computational problem with a highly parallel processor that mimics a processor per pixel. The memory bandwidth bottleneck is overcome by intimately connecting processing circuitry and memory. Figure 18 shows a block diagram of the arithmetic logic unit, where logical operations are performed by a one-bit address with a multiplier on each of its three inputs. The pixel-planes architecture represents a trend in high-end graphics architectures that optimizes the graphics pipeline primitives by creating a smart frame buffer capable of performing computational functions and using concurrent operations.

Word Alignment in Dual-Port Graphics Buffers

An important issue in plane-organized graphics systems is aligning word boundaries. Although alignment functions exist in contemporary graphics processors, graphics systems designed for the low-end market may not be able to justify the cost of a high-end processor. One solution is to provide a dual-port graphics buffer with both plane and pixel access capabilities. An alternative solution is to include a barrel shifter function (figures 19 and 20). Both approaches are nonstandard but could be considered for an application-specific design that distributes some of the processor's functions to the frame buffer.

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Figure 18. Smart Frame Buffer

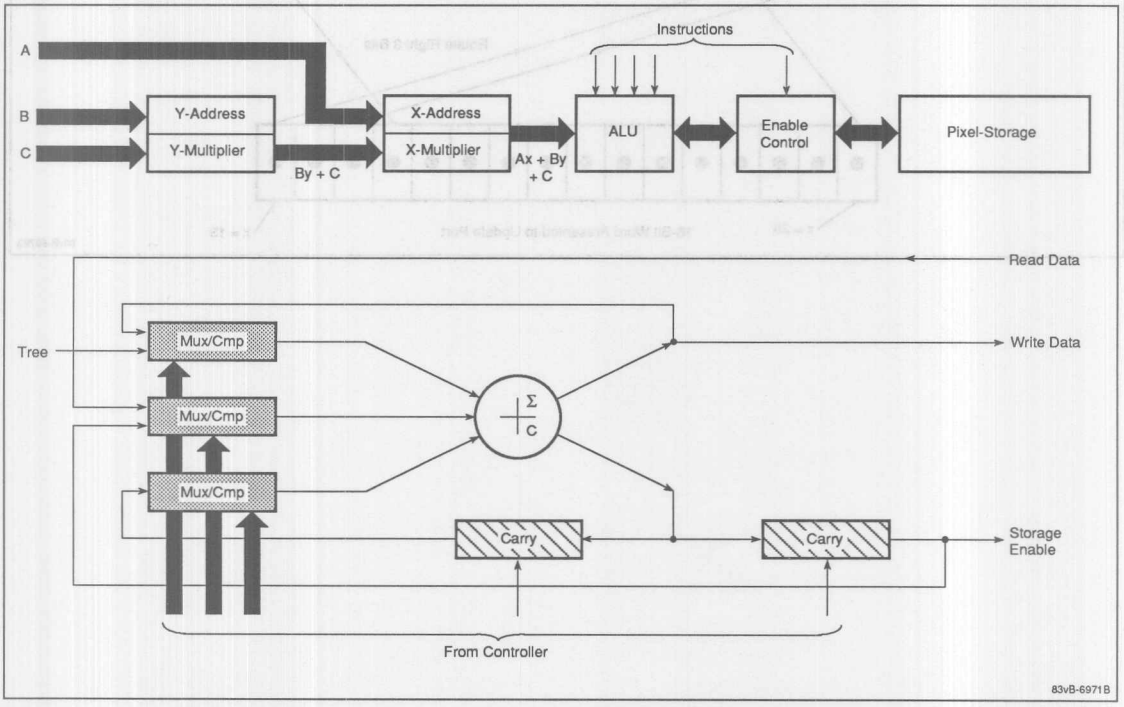


Figure 19. Chip Addressing to Cross Word Boundaries

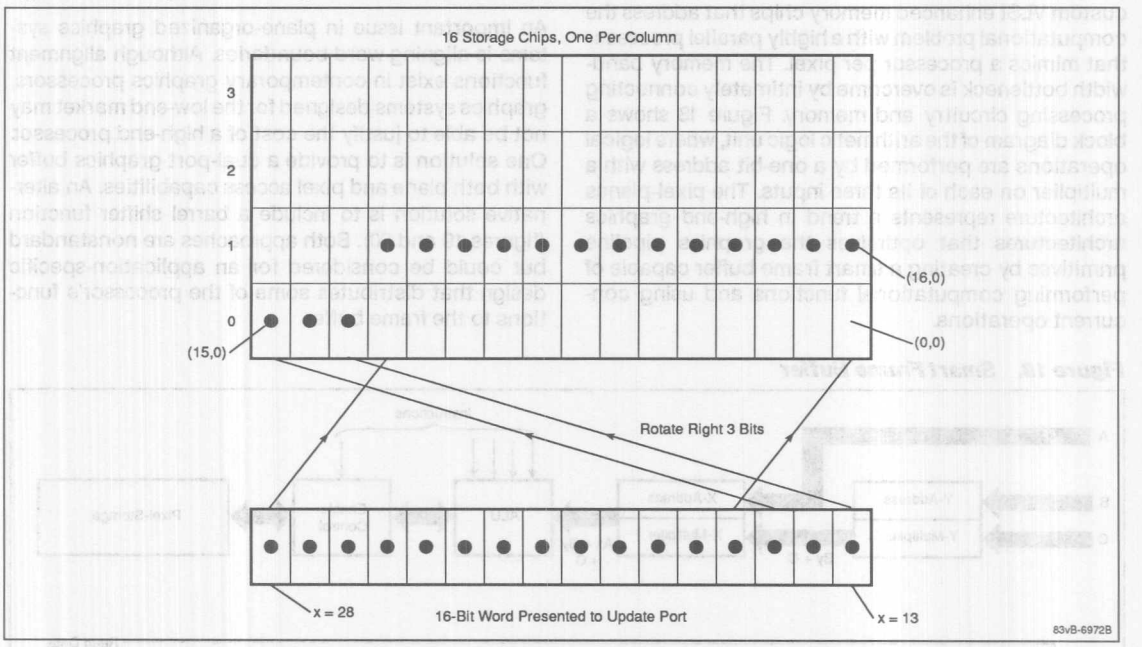
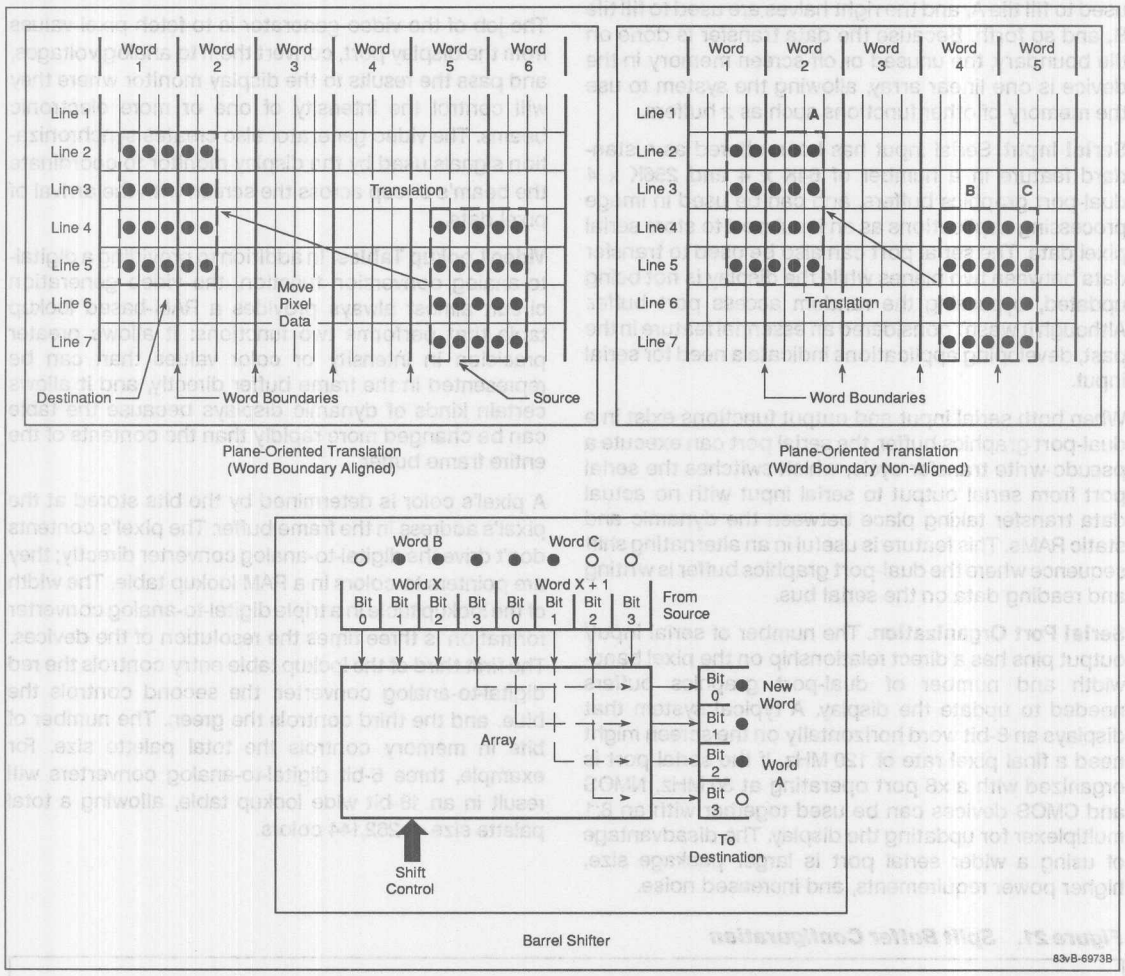


Figure 20. Barrel Shifter Function



Special Serial Port Features

High performance graphics applications require screen refresh rates in the range of 60 to 72 Hz; also full-resolution stereoscopic displays require twice this refresh rate, 120 Hz. In order to be able to accommodate these high rates, a very fast serial access cycle is required. A data transfer cycle to load data from the dual-port graphics buffer into its serial access memory requires use of the random access port. For example, a fast-page cycle must be in progress before a data transfer cycle can occur, which means it would be good to reduce the number of times that serial access memory must be loaded.

Alternatively, if the data from the random access port could be loaded into an idle part of the serial access port, the serial access port would not be interrupted. This could be accomplished with the use of a split-buffer serial port architecture, which separates the serial port into two equal halves, allowing concurrent data transfers from the random access port while the serial port transfers data to the display, thus increasing pixel bandwidth.

Another advantage of using a split-buffer architecture is that tile boundaries can be crossed in real time. For example, a frame buffer organized into 16 x 16 tile can be access by two dual-port graphics buffers. The left

half of the split buffers of devices 1 and 2 (figure 21) is used to fill tile A, and the right halves are used to fill tile B, and so forth. Because the data transfer is done on tile boundary, the unused or off-screen memory in the device is one linear array, allowing the system to use the memory of other functions such as *z* buffers.

Serial Input. Serial input has been offered as a standard feature in a number of 64K x 4 and 256K x 4 dual-port graphics buffers, and can be used in image processing applications as an input port to store serial pixel data. The serial port can also be used to transfer data between two planes while the display is not being updated, bypassing the random access port buffer. Although it wasn't considered an essential feature in the past, developing applications indicate a need for serial input.

When both serial input and output functions exist in a dual-port graphics buffer, the serial port can execute a pseudo-write transfer cycle, which switches the serial port from serial output to serial input with no actual data transfer taking place between the dynamic and static RAMs. This feature is useful in an alternating shift sequence where the dual-port graphics buffer is writing and reading data on the serial bus.

Serial Port Organization. The number of serial input/output pins has a direct relationship on the pixel bandwidth and number of dual-port graphics buffers needed to update the display. A typical system that displays an 8-bit word horizontally on the screen might need a final pixel rate of 120 MHz. If the serial port is organized with a x8 port operating at 30 MHz, NMOS and CMOS devices can be used together with an 8:1 multiplexer for updating the display. The disadvantage of using a wider serial port is larger package size, higher power requirements, and increased noise.

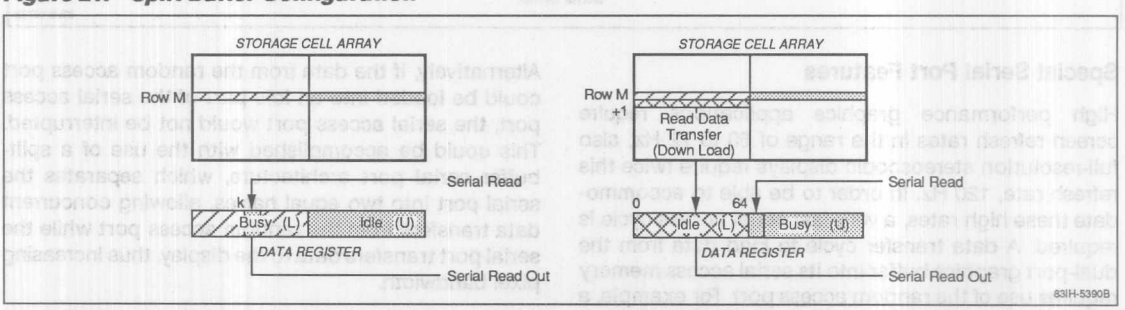
Video Generation

The job of the video generator is to fetch pixel values from the display port, convert them to analog voltages, and pass the results to the display monitor where they will control the intensity of one or more electronic beams. The video generator also creates synchronization signals used by the display monitor to coordinate the beam's sweep across the screen with the arrival of pixel data.

Video Lookup Tables. In addition to providing a digital-to-analog conversion function, the video generation circuit almost always provides a RAM-based lookup table that performs two functions: it allows greater precision in intensity or color values than can be represented in the frame buffer directly, and it allows certain kinds of dynamic displays because the table can be changed more rapidly than the contents of the entire frame buffer.

A pixel's color is determined by the bits stored at the pixel's address in the frame buffer. The pixel's contents don't drive the digital-to-analog converter directly; they are pointers to colors in a RAM lookup table. The width of the lookup table in a triple digital-to-analog converter formation is three times the resolution of the devices. The first third of the lookup table entry controls the red digital-to-analog converter, the second controls the blue, and the third controls the green. The number of bits in memory controls the total palette size. For example, three 6-bit digital-to-analog converters will result in an 18-bit wide lookup table, allowing a total palette size of 262,144 colors.

Figure 21. Split Buffer Configuration



Color resolution is determined by the number of bits per pixel. Eight bits per pixel gives a markedly better picture than four bits per pixel; however, 24 bits per pixel provides true color. More than 256 colors can be displayed on the screen at once by changing the color associated with each address in the lookup table. The colors can be changed as often as once every scan line. This technique is called "pseudocolor."

Lookup tables may have separate registers for generating overlays, which provide a means of generating an image separate from the frame buffer. The overlay registers are controlled by the system processor, and allow the system software to control the system graphics elements independently from the application software graphics. System software displays basic, relatively unchanging graphics elements such as cursors, screen frames, and system messages. Application software manipulates a variety of changing graphical information. By overlaying one or more separate graphics planes displaying system information, the time-consuming task of updating the frame buffer can be avoided (figure 22).

Digital-To-Analog Converters. The digital-to-analog conversion portion of the video generation circuit converts the digital output of the lookup table into analog circuits that are used to drive the display monitor. These converters are specified regarding their organization (e.g., triple 6-bit, single 8-bit, etc.) and the speed at which they can operate. Figure 23 shows the relationship between screen resolution and digital-to-analog converter bandwidth. A number of manufacturers produce both triple and single converters, up to a speed of 360 MHz. If greater speed is required, a discrete bipolar circuit needs to be designed.

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Figure 22. Overlaying of One or More Planes

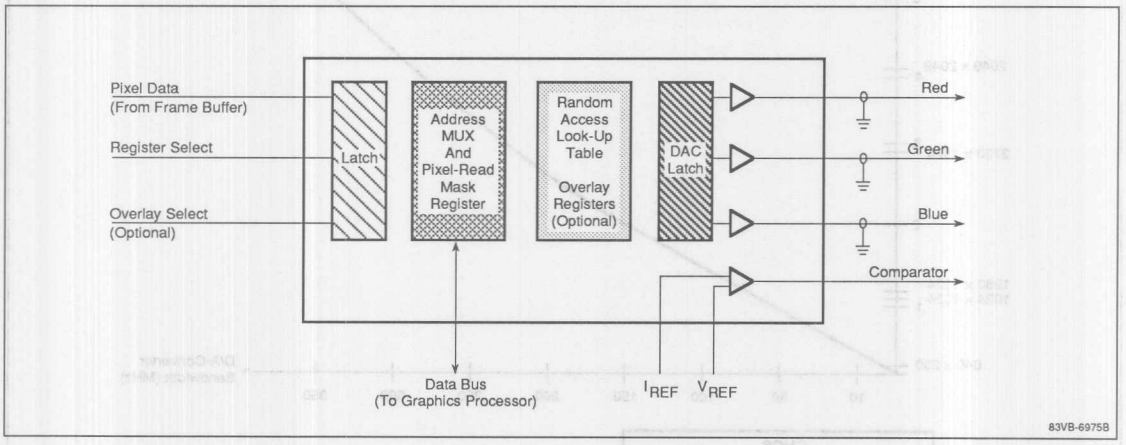
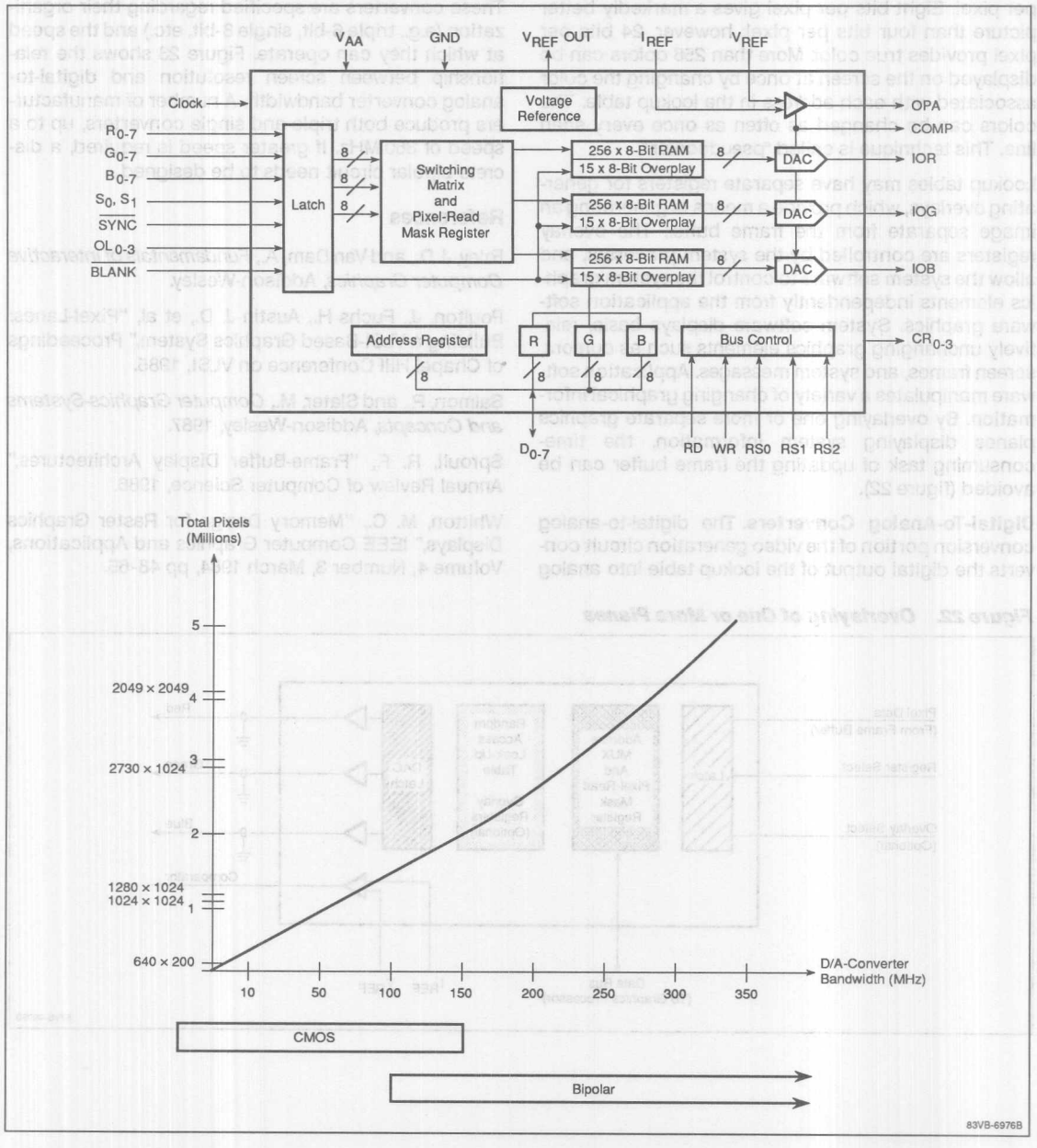


Figure 23. Relationship Between Screen Resolution and Bandwidth of the Digital-to-Analog Converter



Introduction

Computer-generated images that rival color photography in all of its nuances of color, shading, reflectance and translucency is in demand by a growing number of users. This application note will discuss the algorithms able to generate these effects, which have been integrated into a variety of systems with impressive results.

Three-Dimensional Graphics System

In a three-dimensional system, the object rendered is described as a mathematical model that holds primitives such as lines, polylines, and polygons in a display list. Traversing the display list produces a sequence of data in world coordinates. Often this data represents polygon vertices, but it can also represent control points for parametric surfaces and other data that must be converted to a polygonal approximation of the surface. Polygons expressed in three-dimensional world coordinates transform geometrically into a form suitable for display on a two-dimensional raster device. Transformations include three-dimensional to two-dimensional projection, translation, scaling, rotation, perspective projection, and clipping. The result is a series of polygon vertices supplied in coordinates for a specific CRT.

The polygon vertices and their associated color data are interpolated to determine the pixels to be illuminated and the color to be displayed, while depth (*z* axis) information is interpolated to determine which polygons are obscured from the observer's view. Color values are written to the frame buffer and depth values to the *z* buffer which, with its associated hardware, supplies hidden surface removal. Finally, each pixel from the frame buffer is sequenced in the line as required by the CRT and converted to an analog signal.

Although a basic three-dimensional system can render a realistic image, special functions are required to produce subtleties of color, shading, shape and translucency. These functions must be able to model the behavior of light with different levels of complexity, provide methods for creating realistic surface textures, compensate for the limitations of the display technology, and provide techniques for rendering natural effects such as terrain and clouds.

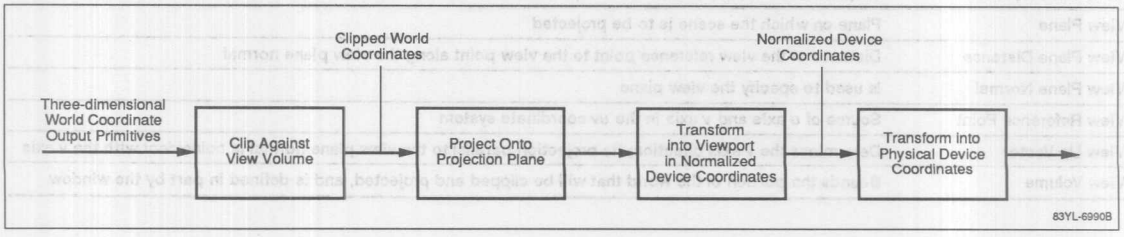
Two- and Three-Dimensional Image Processing

Three-dimensional graphics is an order of magnitude more complex than two-dimensional graphics, and while a detailed description of its specifics is beyond the scope of this paper, some aspects pertain to this discusssion.

The viewing pipeline in two-dimensional graphics involves transformations from two-dimensional coordinates, world coordinates, normalized device coordinates, and device coordinates. Moreover, the objects may be transformed at one of the stages by some combination of translation, scaling, and rotation.

In three-dimensional graphics, the pipeline is more complex because there is a projection stage, where the three-dimensional world coordinates in which the scene is described are projected onto a two-dimensional projection plane. Conceptually, objects in the three-dimensional world are clipped against the three-dimensional view volume and then projected. A view volume is specified in world coordinates, in a projection onto the projection plane, and in a viewport on the surface. The contents of the window, which is itself the projection of the view volume onto the projection plane, are then mapped into the viewport for display. Figure 1 shows this process, which is the model used in numerous three-dimensional graphics subroutine packages. As with two-dimensional viewing, a variety of models can be used for actual implementation of the viewing process.

Figure 1. Basic Three-Dimensional Pipeline

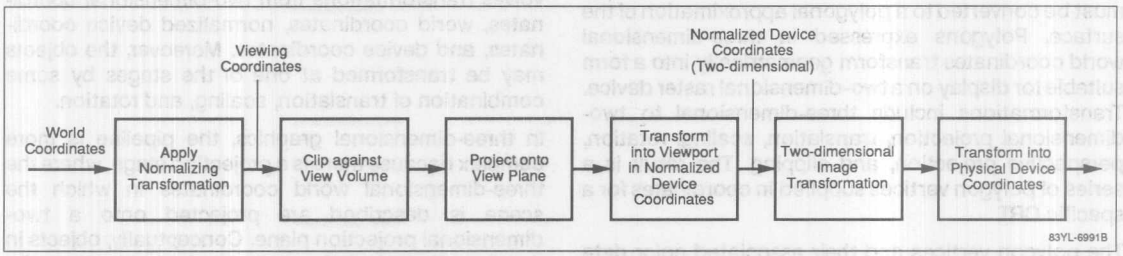


Given the specification of a view volume and a projection, there is a need to understand how the clipping actually is done and how the projection is applied. It is possible to clip lines against the view volume by first calculating their intersection with each of the six planes defining the view volume. Lines remaining after the clipping process would be projected onto the view plane by simultaneously calculating the intersection of the projectors through their end points with the view plane. The coordinates would then be transformed from three- into two-dimensional world coordinates.

To be able to include three-dimensional viewing operations in a standard graphics package, two sets of capabilities must be added: output primitives in three-dimensional coordinates, and specifications of planar geometric projections. Output primitives in three-dimensional world coordinates are straightforward extensions from the two-dimensional primitives. A third parameter, the *z* coordinate, is added to the procedure call. The perspective projections in a graphics package allow viewing from a number of perspectives, including from the center of a projection, from a view plane, from a window on the view plane, and from a viewport on the view surface.

The extra complexity introduced with three-dimensional viewing is caused by the fact that the display devices are only two-dimensional. The solution to the mismatch between three-dimensional objects and two-dimensional displays is solved by introducing projections, which transform three-dimensional objects onto a two-dimensional projection plane (figure 2). The large number of calculations required for this process, repeated for many lines, calls for considerable computing.

Figure 2. Three-Dimensional Viewing Process Extended to Include Two-Dimensional Image Transformations



Three-Dimensional Projections

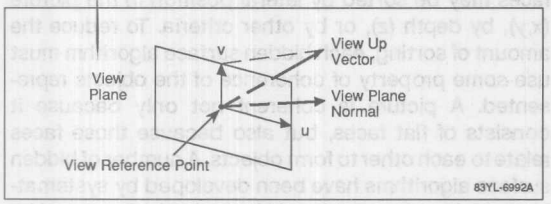
Table 1 identifies and defines the specifications for a three-dimensional projection. Figures 3, 4 and 5 are corresponding examples.

Table 1. Parameters for a Three-Dimensional Projection

Parameter	Description
uv Coordinate System	System by which a window is defined
u Axis Direction	The direction of *u*, *v* and the view plane normal when positioned to form a left-hand coordinate system
v Axis Direction	Coincident with the projection of the view up vector parallel to the view plane normal onto the view plane
Center of Projection	Helps define the view volume and is specified in world coordinates relative to the view reference point
View Plane	Plane on which the scene is to be projected
View Plane Distance	Distance of the view reference point to the view point along the view plane normal
View Plane Normal	Is used to specify the view plane
View Reference Point	Source of *u* axis and *v* axis in the *uv* coordinate system
View Up Vector	Determines the *v* axis direction; its projection parallel to the view plane normal is coincident with the *v* axis
View Volume	Bounds the portion of the world that will be clipped and projected, and is defined in part by the window

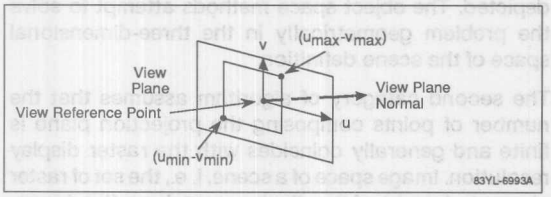
Figure 3 illustrates how the *v*-axis direction on the view plane is determined. The *v*-axis direction coincides with the projection of the view up vector parallel to the view plane normal.

Figure 3. uv System in the View Plane



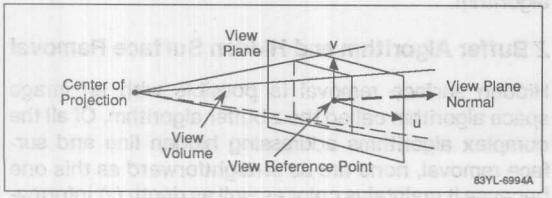
The view reference point, view up vector, and view plane normal are specified in the left-hand world coordinate system. With the *uv* system defined on the view plane, it is possible to specify the window's minimum and maximum *u* and *v* values, as shown in figure 4. Notice that the window need not be symmetrical about the view reference point.

Figure 4. Window in uv Coordinates



For perspective projections, the center of projection also helps to define the view volume. The center of projection is specified in world coordinates relative to the view reference point. The view volume is a semi-infinite pyramid that slides through the window, with its apex at the center of projection. Figure 5 shows the perspective projection view volumes. Positions behind the center of projection are not included in the view volume and will not be projected.

Figure 5. Semi-Infinite Pyramid View Volume for Perspective Projection



Anti-Aliasing

No matter how sophisticated the object model, it cannot overcome the consequences of sampling a continuous scene with a finite number of elements. Such sampling is an inevitable outcome of the very raster graphics technology that has made shaded image generation possible. A raster display consists of a rectangular array of spots, each of which can be controlled in intensity by the CPU. The actual image is a continuous intensity function of *x* and *y* on the screen; the pixels are regularly spaced samples of this continuous function. In any sampled data system, problems arise if the resolution of the continuous function is the same as or smaller than the spacing between samples. This phenomenon, known as aliasing, is visible on CRT screens as jagged lines, or jaggies. It is particularly apparent on lines and curves angled close to the horizontal and vertical axes, and often appears in images displayed on screens with low to moderate resolution (figures 6 and 7).

Figure 6. Vertical Aliasing

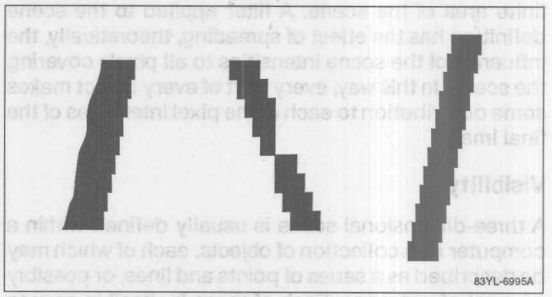
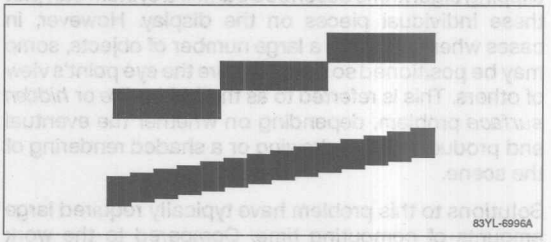


Figure 7. Horizontal Aliasing



Generally, aliasing can be found in at least three types of graphics: (1) in jagged edges of straight lines and polygon boundaries, (2) in objects smaller than pixel size or in objects containing very thin lines or polygons, or (3) in complex scenes containing a lot of fine detail. Unless special measures are taken, the fine detail is either totally lost or distorted beyond recognition.

The solution is to eliminate high frequency information before sampling the picture. Visually this means blurring the picture. Mathematically it means the intensity of a picture should be more than just the point to which it corresponds in the continuous picture; it should be some weighted average of the intensities surrounding the point. The anti-aliasing process requires the weighting function at each pixel to be multiplied by the ideal intensity function, the results integrated, and the result used as the displayed intensity. Perhaps the most obvious anti-aliasing technique is to sample the image at a resolution higher than the one used for display, and average down to the true pixel level. Elementary statistical theory shows that the average values contain more information about the true image than if the sampling had been performed at display resolution size.

Aliasing occurs especially when the intensities in the scene change sharply within a region, for it is in precisely such regions that the sampling rate is not high enough to capture the changes. The idea of filtering is directly based on the idea of a pixel covering a finite area of the scene. A filter applied to the scene definition has the effect of spreading, theoretically, the influence of the scene intensities to all pixels covering the scene. In this way, every part of every object makes some contribution to each of the pixel intensities of the final image.

Visibility

A three-dimensional scene is usually defined within a computer as a collection of objects, each of which may be described as a series of points and lines, or possibly as a set of polygons. Each of these by itself is easy to display. Using the transformation, perspective, and clipping algorithms described earlier, a system can plot these individual pieces on the display. However, in cases where there are a large number of objects, some may be positioned so as to obscure the eye point's view of others. This is referred to as the *hidden line* or *hidden surface* problem, depending on whether the eventual end product is a line drawing or a shaded rendering of the scene.

Solutions to this problem have typically required large amounts of computing time. Compared to the work involved in computing transformation, perspective and clipping algorithms, the hidden surface calculation is usually the dominant cost in such a program. The former calculations depend only on an individual object, not on its relationship to the other objects in a scene. Thus the amount of work is roughly proportional to the number of objects within the scene. However, hidden surface removal requires that each object be compared to every other object.

The various surfaces of an object to be shown in hidden surface or hidden line form must be sorted to find which ones are visible at various places on the screen. Surfaces may be sorted by lateral position in the picture (x,y), by depth (z), or by other criteria. To reduce the amount of sorting, each hidden surface algorithm must use some property of coherence of the objects represented. A picture is coherent not only because it consists of flat faces, but also because those faces relate to each other to form objects. A number of hidden surface algorithms have been developed by systematically looking for additional kinds of coherence and by sorting orders and types.

Hidden line or hidden surface removal algorithms have been separated into three categories. First, there are the algorithms operating in object space independent of the type of device used, whose different steps operate directly on the vertices of the face. The object space of an image is the set of primitives such as lines, polygons and spheres that compose the scene to be depicted. The object space methods attempt to solve the problem geometrically in the three-dimensional space of the scene definition.

The second category of algorithm assumes that the number of points composing the projection plane is finite and generally coincides with the raster display resolution. Image space of a scene, i. e., the set of raster elements (pixels) of the display, contains a fixed number of elements equaling the resolution of the display. Image space algorithms are specifically designed for modern raster graphics image generation and are more popular and widely used than the object space algorithms.

The last category, the so-called "list priority" algorithms, are generally characterized by a sorting step in object space and a display in image space. The simplest and fastest hidden surface algorithm is known as the z buffer algorithm. Other examples are the polygon scan conversion algorithm and the divide and conquer algorithm.

Z Buffer Algorithm and Hidden Surface Removal

Hidden surface removal is possible with an image space algorithm called the z buffer algorithm. Of all the complex algorithms addressing hidden line and surface removal, none are as straightforward as this one because it maintains color as well as depth (z) information at each pixel. A refresh buffer stores intensity

values, and the *z* buffer array stores depth values corresponding to the pixels currently set.

The *z* buffer must have the same dimensions as the display frame buffer. All locations in the *z* buffer are initialized to the value perceived by the viewer to be the farthest behind the screen, while the corresponding display pixels are set to the required background color. As each polygon is rasterized, the *z* values for the resulting pixels are compared individually with the previously stored *z* values. The new *z* value is written to the *z* buffer, and the new associated color is written to the frame buffer. If the new *z* value is larger (i.e., farther away), then neither buffer is modified.

The obvious advantage of this algorithm is that it is computationally simple, and its performance is independent of the complexity of the scene in terms of visibility. Its running time is proportional to the number of polygons to be processed, and not to the relationship between the polygons. A disadvantage of the method is that it requires a large amount of memory to maintain the *z* buffer. For example, for a 512 by 512 display, the *z* buffer size is a megabyte of memory if the *z* value precision of 16 to 20 bits would suffice. In any case, the relatively low cost of memory allows the realistic marketing of fast access *z* buffer hardware memory boards, which is perhaps the ideal solution.

Scan Line and Area Subdivision Algorithms

Scan line algorithms operate in image space to create an image one scan line at a time. This approach is an extension of the polygon scan conversion algorithm and thus uses scan line coherence and edge coherence. The difference between the two methods is that all the polygons that define an object are involved. The algorithm performs a *y* sort, and then an *x* sort, and finally a *z* depth search to establish the visible face. In the scan line method, the dimensions are first reduced to two at the intersection of the plane through the scan line, parallel to where the *z* axis intersects the scene, and then reduced to one by considering only the line segments on the plane with minimum *z* values. A *z* buffer based on polyhedral surfaces also makes use of depth coherence to improve speed of computation, whereas the scan line method is based on edge and scan line coherence.

Another method, the area subdivision or divide and conquer algorithm departs from strategies used in other algorithms in that it is based on area coherence and solves the general sorting problem by attempting to avoid it altogether. An area of the projection plane image is examined, and if it is easy to decide which polygon or polygons are visible in the area, the appropriate ones are displayed. Otherwise the area is subdivided into smaller areas and the decision logic is recursively applied to each of the smaller areas. As the areas become smaller, fewer and fewer polygons will overlap, and ultimately a decision will be possible.

This algorithm clearly takes an image space approach by exploiting area coherence, i.e., the tendency for at least the small areas of an image to be contained in a single polygon at most. Area coherence means that pixels close together are likely to correspond to the same object and have a similar color, which is the underlying assumption of the algorithm. This algorithm generally performs less efficiently than the scan line method, because it involves more work to sort things out when projections of polygons overlap.

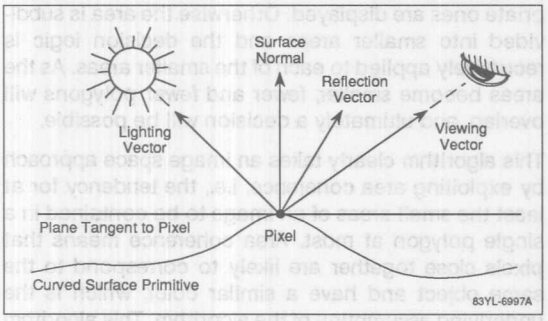
Shading

After hidden surfaces have been removed, the next step in creating a realistic image is to shade the visible surfaces, taking into account the light source, surface characteristics, and positions and orientations of the surfaces and sources. Graphics system designers have been developing lighting and shading models for rendering graphics images at different levels of realism. This involves some understanding of the fundamental properties of the humam vision system. Unlike a photograph of a real world scene, a computer-generated shaded picture is made from a numerical model stored in the computer as an objective model. The goal of the shading model is to provide realistic images of surfaces for which the illumination of a surface depends on its orientation. If it is normal to the incident light rays, the surface is brightly illuminated. The more oblique the surface is to the light rays, the less the illumination. This variation in illumination is a powerful cue to the three-dimensional structure of an object. It would be a waste of modern day computer graphics resources if color-generation techniques were not used to their full capacity. Shading is one of these techniques.

Light Models

In 1975, Bui-Tuong Phong proposed a light model for specular reflection that has since been termed *Phong shading*. This model specified how light reflects from glossy surfaces such as billiard balls, apples, china, and as an extreme, mirrors. Before this model, light was modeled on how it reflected from a perfectly diffused surface, i.e., one that reflects light equally in all directions (figure 8).

Figure 8. Basic Lighting Model for Shading



When planar polygons are used to approximate curved surfaces, greater realism can be achieved by an interpolation scheme introduced by Gouraud. This scheme is called *Gouraud smooth shading,* or *intensity-interpolation shading.* In flat shading, a single intensity value for shading the entire polygon face is calculated, a single surface-normal vector is defined for each represented polygon, and each polygon is shaded with a single color. This is a reasonable approach to shading flat surfaces where the intensity of the light reflected from the surface is held constant over the entire surface.

Gouraud shading provides smooth shading through a linear interpolation technique in which surface-normal vectors are computed at the vertices or corners of each face of a polyhedron. First, surface normals are calculated. Subsequently, vertex normals are computed by averaging the surface normals of all the polygon faces common to the vertex. Each of these vertex normals are used to compute a vertex shade, and then the shade inside the particular polygon face is interpolated from the vertex shades. Each polygon is shaded along each edge and then between edges along each scan line.

Phong shading is a complex algorithm that computes the intensity value of each pixel of a polygon face according to how that point is oriented to the light source(s). Phong's was the first shading model to achieve realistic highlights using interpolation of surface normals and an approximation of specular reflection. The Phong shading model entails interpolated surface-normal vectors across the polygon face—as opposed to Gouraud shading—and using the interpolated surface normal to calculate the intensity values for each pixel on the polygon surface. The intensity contribution for each light is modeled as the sum of diffuse and specular components. Because the Phong technique requires extensive computer power to execute the complex calculations needed to shade each pixel of an object's surface, it is usually performed only on supercomputers or superminicomputers. Phong and Gouraud shading models also support the full range of lighting controls, including multiple, colored point, spot and directional light sources. The special advantage of these schemes is that they fit well with scan line algorithms for filling polygons.

The Phong model yields a surface with a specific normal based solely on the curvature of the surface, which causes a shiny, plastic look. To make this surface appear more realistic, a textured surface must be mapped over the first surface. This technique is called procedural textured mapping and provides a means of defining constant, matte, metal and plastic surfaces.

Ray Casting and Ray Tracing

Ray tracing algorithms simulate the interaction of light with the environment, simply determining such optical effects as reflection, refraction, and shadowing. Ray tracing is a computer graphics technique in which the path of all the individual light rays contributing to the image are traced explicitly. These techniques are direct and somewhat brute force methods for solving the visibility problem. Nevertheless, ray tracing algorithms have produced some of the most spectacular results in graphics images. Many visual and lighting effects such as refraction and reflection, motion blur, depth-of-field, penumbrae, and nonuniform interradiation can be modeled with ray tracing. Despite its simplicity and robustness, ray tracing is seldom used in practical applications because of its high computational requirements.

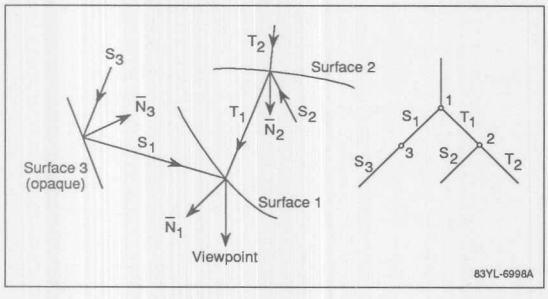
The idea of ray casting is a very simple one: for each pixel, trace a ray from the eye position (in image space) through the pixel and find the intersections with all the objects in the scene. The intersection having the smallest z value determines the color of the pixel. Ray tracing is more complex, because once the first intersection is found, the ray is reflected off the object surface and traced back farther—and so on recursively—until it passes out of the scene or is traced to one of the original light sources. Similarly, if the surface is transparent, then an additional ray is refracted through the surface and traced. In this way, a number of features that are extremely difficult to implement in other methods can be easily introduced into the rendering. Problems with visibility and transparency, as well as with shadows and the reflection of objects on each other, can be easily solved.

The fundamental idea is to trace light rays and to determine which one ends up at the view point. Unfortunately, an infinite number of rays emanate from each

point light source, and most of them never reach the view point. Thus, the tracing starts at the view point and traces rays backward through each pixel to their origin. A ray of light striking the surface of an object breaks into three parts: diffusely reflected light, specularly reflected light, and transmitted light. Similarly, a ray of light leaving the surface of an object is in general the sum of contributions of the three sources. This means that each time a ray leaves an object, up to three new rays should be traced.

Figure 9 shows the tree grown in the process of tracing a particular ray backward. S_1 is the light ray that comes into surface 1 at such an angle that it is specularly reflected and leaves as part of the outgoing ray. Similarly, T_1 is the light ray incident on surface 1 such that it is transmitted and leaves as part of the outgoing ray. Each node of the tree corresponds to a surface. After the tree is completely grown, the intensities at each leaf node are computed and then used to compute the intensity at the parent node, until the root node is reached.

Figure 9. Tree Grown From Tracing a Single Ray to Viewer



An infinite number of rays could be traced backward, but only those rays passing through the view point and the corner of the pixels are actually traced. T_1's permit anti-aliasing to be performed, because the intensities can be averaged to calculate the intensity of the pixel. If the four rays through the corners of a pixel subtend a volume in space that contains a lot of fine detail, the pixel is subdivided and additional rays are traced to help the anti-aliasing process. As ray tracing is developed further, speed increases will undoubtedly come from the application of coherence or other properties of the objects being displayed. Ray tracing also lends itself to parallel processing, because rays can be traced independently of one another. VLSI implementations may therefore be expected.

Surface Detail

The shading algorithms described to this point all produce very smooth and uniform surfaces. In the real world, most surfaces have details of color and texture. Texture mapping is one of the most common techniques used to model surface patterns. The patterns are mapped onto the object surface or modeled on the surface patch itself. Color detail is applied to a smooth surface without appearing to change its geometry, while texture details give the appearance of roughness. Perturbing the surface normal will produce bumpy surfaces, brushed copper, and so forth. A wood grain or marble surface could also be achieved by applying a real-world image to a geometrically defined curved surface.

Although this method works well with smooth surfaces, it does not work well with terrains, coastlines, and jagged mountains, which require a fractal surface method. Hidden surfaces are removed, and an appropriate shading model applied.

Procedural definitions of textures, light sources, volumes, and atmospheres are collectively called "shaders." There are predefined lighting shaders for ambient, distant and point light sources, as well as for spotlights. Atmosphere shaders include depth cue and fog. Volume shaders describe volumes through which light passes and is refracted and attenuated. Atmosphere shaders are based on the principle that light is attenuated over distance, be it through clear or foggy air, and that such attenuation gives the eye a cue to spatial relationships. The syntax of these predefined shaders can be used to define custom shaders of all kinds.

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Introduction

Today's RISC microprocessor architectures offer a promise of high performance systems able to execute an instruction in one system clock cycle, which means the challenge for a system designer is to design a memory system that can support high CPU throughput requirements. Common elements of these VLSI designs include on-chip subsystems such as floating point units and/or cache memory.

Although the size of an on-chip cache is typically small (4 to 8 Kb) to minimize chip size and optimize cost, the system may also require an external, second-level cache that is much larger (256 Kb to 1 Mb) and can interface to a high performance system bus. If the CPU executes an instruction that isn't stored in the cache, the cache must access main memory and fetch an instruction for the processor. Even though a cache is designed to sustain a high hit rate, a percentage of the CPU's read cycles and all writes cycles must access main memory, making it essential that data transfer cycles be executed so that latency of the system bus is minimized. System bus latency may increase dramatically in a multiprocessor system and can be the critical issue in determining system performance.

This application note will discuss quantitative measures of memory performance, as well as a number of design techniques for optimizing performance in today's system environment.

Hierarchical Systems

Bottlenecks in most Von Neumann architectures have traditionally occurred because a processor could only read a single word from memory during each access cycle, and to be able to match processor cycle time, a system would have to use very high-speed devices that in most cases could not be justified in terms of cost. The classical solution has been to configure a hierarchical or multilevel structure containing several types of memory devices with various cost and performance characteristics.

Performance can be affected by such interrelated factors as program behavior with respect to memory references, access times and sizes of each level, granularity of information transfer, memory management policies, and the processor-to-memory interconnection network. One measure of performance is called *effective access time*, which is the sum of average access times at each level of the hierarchy. Another quantitative measure is *bandwidth*, which refers to the number of bits that can be accessed per second. To increase bandwidth, a system designer may choose to reduce cycle time, increase word size by accessing more bits per cycle, or replicate the memory banks and access two or more concurrently.

Properties of Program Locality

The majority of computer systems developed today are based on properties of program locality that reveal a strong tendency for accesses to be clustered in small regions of memory during any short period of time. Program locality has two aspects, temporal and spatial. The first, locality of time, means that information that will be in use in the near future is likely to be in use already. This type of behavior can be expected from program loops in which both the data and instructions are reused. The second property, locality of space, means that portions of the address space which are in use generally consist of a fairly small number of individual contiguous segments of that address space. Locality of space means that the program's loci of reference in the near future are likely to be near the current loci of reference. This theory is based on common patterns of behavior: related data items (e.g., variable arrays) are usually stored together and instructions are mostly executed sequentially.

The characteristics of temporal locality have shown a strong tendency for program references to be grouped in time, and in fact were responsible for the invention of virtual memory and the subsequent design of high-speed caches, both of which exploit the properties of locality by storing a copy of the program in a temporary segment of memory. Virtual memory increases the size of the system by segmenting the program into pages that are individually loaded from magnetic secondary memory into main memory. A cache optimizes CPU throughput by also storing a segment of the program in a buffer that matches the speed of the processor.

Optimizing the Hierarchy

Once program behavior is understood, main memory can be structured to optimize processor performance. As discussed earlier, effective access time is the sum of the average access time in each of the levels of the hierarchy, defined as

$$t_{EFF} = \Sigma\, t_K$$

where t_{EFF} is effective access time from the processor to the *ith* level of the hierarchy, and t_K is the individual average access time at each level, where $K = 1$ *to* i. Generally, t_K includes not only the wait time caused by memory conflicts at level K, but also the delay in the switching network between levels $K - 1$ and K. The degree of conflicts is usually a function of the number of processors, the number of memory modules, and the interconnection network between the processors and modules.

In modeling the performance of a hierarchy, it is often assumed that the probability of finding requested information in the memory of a given level is characterized by a success function or hit ratio h. In general, h depends on the granularity of information transfer, the capacity of memory at that level, the management strategy, and other factors. However, for some class of management policies, it has been found that h is most sensitive to memory size. Because copies of information at the highest hierarchical level are assumed to exist in levels below that level, the probability of finding the data at the higher levels is $f = 1 - h$, where f is the miss ratio. Therefore in a two-level system, effective access time would be equal to

$$t_{EFF} = h\,t_{K1} + (1 - h)\,t_{K2}$$

where $t_{K1} = t_{ACC}$ at level 1 and $t_{K2} = t_{ACC}$ at level 2. If the hierarchy consists of one level of infinite size (an expensive option for most applications), the probability of accessing this data at level one is 100% (hit ratio = 1). Memory size greatly impacts the probability of finding data at a given level, which is why the probabilities at each level are expressed in terms of hit and miss ratios. For example, effective access time for a two-level hierarchy would be expressed as follows:

$$t_{EFF} = h\,t_{K1} + (1 - h)\,t_{K2}$$

If the hit ratio at level one is 0.99, then the probability of finding the data at level two, or the miss ratio at level two, would be $1 - 0.99 = 0.01$. Effective access time then would be

$$t_{EFF} = (0.99)\,t_{K1} + (0.01)\,t_{K2}$$

Hit ratio is crucial to system performance. For example, if the memory at level two is ten times slower than the memory at level one, the hit ratio decreases from 0.99 to 0.98 (roughly 1% fewer hits) and results in an increase in t_{EFF} of roughly 10%. Small changes in hit ratio affect effective cycle time of the overall system, making t_{EFF} very sensitive to hit ratio. A decrease of 10% in hit ratio (from 0.99 to 0.89) almost doubles the effective cycle time and divides net performance in half when the cycle time ratio is 10. If the cycle time ratio is 20, that same 10% decrease increases effective cycle time by almost a factor of 4. Hit ratio should be as high as possible; in many cases, techniques resulting in marginal 1% to 2% improvements may yield substantial performance improvements.

A very large structure in only one level is too expensive for most systems, and a multilevel structure is the only configuration that makes sense in terms of cost and performance objectives. Therefore, the goal is to structure the hierarchy so that the highest performance is available for the least cost. Because hit ratio is a function of the memory size at each level, the implication is that the larger the memory at a given level, the higher the hit rate at that level.

Optimizing the Cache

The other variable in the t_{EFF} equation is average access time (t_K) at each level. The hierarchical level closest to the processor should have access times equal to the processor's cycle time, as well as capacity large enough to maintain a high hit rate. The classical solution has been to design this level as a cache, which is a high-speed buffer typically located between the processor and main memory that provides data to the processor without any wait intervals. Success of the cache is attributed to the properties of program locality and is measured by cache hit ratio, as well as by placement algorithm (degree of associativity), block size, ability to perform during a miss, write cycles, and data consistency in multiprocessor or multicache systems.

A cache operation starts when the processor executes a read cycle and outputs a physical address to the memory system. The physical address is separated into two fields, the address tag field and the set select field. The cache latches the address, and the set field in the physical address selects a set in the cache directory or address tag memory. The address tag from the cache directory is compared to the physical address tag from the CPU. If they're the same, a hit occurs and the data is read from the selected block. If the address tags are not the same, a miss occurs and the data has to be fetched from main memory, which means the CPU must wait until the data is read. New data with a new address tag is stored in the cache.

Cache performance is determined by hit ratio, a function of the design that includes the size of the cache, the degree of associativity used to search the cache directory (placement algorithm), the size of its data block, and the replacement algorithm used in a miss cycle.

Although a larger cache can be effective in sustaining a high hit rate, its benefits are diminished by higher costs.

The same relationship regarding effective access for a two-level hierarchy is valid for a two-level system with a cache in the first level. The cache's hit rate can be optimized not only by increasing the size of the cache, but also by optimizing its placement algorithm, block size, and replacement algorithm. With an optimized architecture, the hit rate should be above 90%.

Effective access time in a two-level hierarchy, with the cache in the first level and main memory in the second level, is calculated as the sum of the hit rate and cache access time in the first level and the miss rate multiplied by the access time of main memory in the second level. For a cache with a read cycle time of 60 ns and a hit ratio of 95%, and a main memory read cycle time of 250 ns and a miss rate of 5%, effective access would be determined as followed:

$t_{EFF} = (h_{CACHE})\ (t_{CACHE}) + (1 - h_{CACHE})\ (t_{MAIN\ MEMORY})$

$t_{EFF} = (0.95)\ (60) + (0.05)\ (250) = 59 + 12.5 = 71.5$ ns

Effective access time must also include the effect of a write cycle on system performance. To determine this effect, the ratio of read and write cycles must be determined by analyzing the program address characteristics. The ratio between read and write cycles is typically 85% to 15% in general-purpose computer environments, but it may change to 50%-50% in scientific and other computation-based environments. The equation would have to be expanded as follows:

$t_{EFF} = R\ [(h_{CACHE})\ (t_{CACHE}) + (1 - h_{CACHE})\ (t_{MAIN\ MEMORY})] + W\ (t_{WCYC})$

where R is the fraction of cycles that are read cycles, W is the fraction of cycles that are write cycles, and t_{WCYC} equals write cycle time. If R = 0.85, W = 0.15, and t_{WCYC} = 250 ns, total effective access time would be equal to

$t_{EFF} = 0.85\ [(0.95)\ (60) + (0.05)\ (250)] + 0.15\ (250) = 96.57$ ns

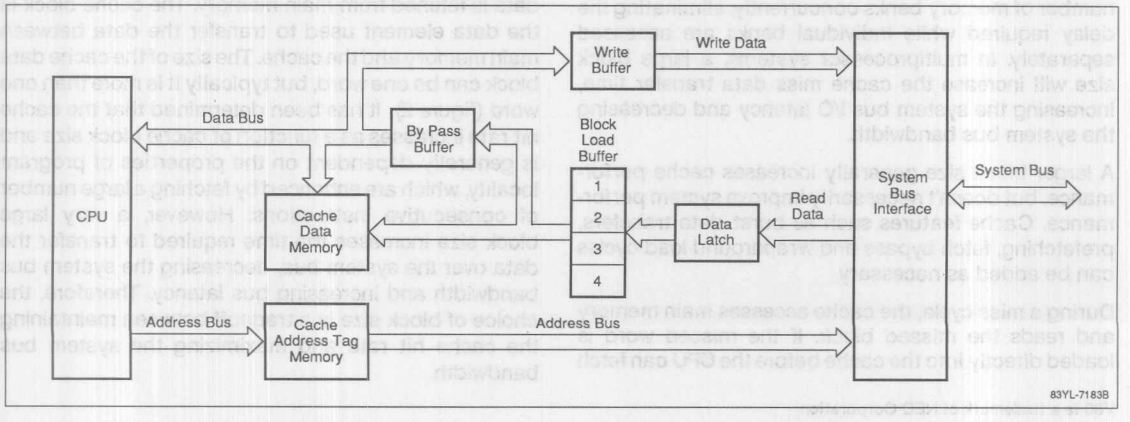
The span of a write cycle does not reflect hit rate. A larger percentage of write cycles will increase t_{EFF}. For example, if R and W were equal at 50%, then t_{EFF} would increase as follows:

$t_{EFF} = 0.50\ [(0.95)\ (60) + (0.05)\ (250)] + 0.50\ (250) = 159.75$ ns

Most program workloads generally have a higher ratio of read cycles to write cycles, allowing the cache to optimize read operation as well as system performance. The main concern with write cycles is that the CPU has to wait for the entire transfer cycle between cache and main memory (> 250 ns) before proceeding to the next instruction. If the cache were able to buffer write data, write cycle time could be reduced to the write access time and the processor wouldn't have to wait for access into main memory and could proceed to the next instruction. Meanwhile the cache could concurrently execute a write cycle into main memory (figure 1). In this case, t_{WCYC} would equal the 60 ns access time of the cache and not the 250 ns access time of main memory. The equation for t_{EFF} in a buffered write cycle is calculated as follows:

$t_{EFF} = 0.85\ [(0.95)\ (60)] + 0.15\ (60) = 57.45$ ns

Figure 1. Write, Fetch Bypass, and Wraparound Load Buffers



The disadvantage of a buffered write cycle is that the circuitry required to control the concurrent CPU and main memory write cycles would have to be more complex.

Optimizing the Miss Cycle

The block size of a cache is the parameter, together with the overall size of the cache itself, that most strongly affects cache performance and also overall system performance. When the data the processor is addressing is not in the cache, the cache executes a miss cycle to access main memory and fetch the missed data to the cache and the CPU. Enlarging block size can decrease the miss ratio and thereby increase the storage delay component of an average instruction, but the longer transfer time required may cause problems in multiprocessor systems because of higher levels of traffic.

A number of design tradeoffs influence block size. For example, architecture of the bus between a cache and main memory plays an important role. A bus protocol that requires an address with each data transfer may force the block size to be one word, because multiple word transfers would be very inefficient. Conversely, if one address can fetch several words of data, then a larger block size would be advantageous. Devices with the ability to transfer bursts of data are becoming popular in a number of microprocessor systems and, together with nibble mode DRAMs, can be implemented to increase memory bus bandwidth. Increasing the width of the bus is another technique that can increase system bandwidth.

In large mainframe systems, block size can reflect the wider bus size and also take advantage of the degree of memory interleaving. Interleaving increases memory bandwidth by enabling data to be accessed from a number of memory banks concurrently, eliminating the delay required while individual banks are accessed separately. In multiprocessor systems, a large block size will increase the cache miss data transfer time, increasing the system bus I/O latency and decreasing the system bus bandwidth.

A larger block size generally increases cache performance, but doesn't necessarily improve system performance. Cache features such as burst data transfers, prefetching, fetch bypass and wraparound load cycles can be added as necessary.

During a miss cycle, the cache accesses main memory and reads the missed block. If the missed word is loaded directly into the cache before the CPU can fetch the data, access time of the miss cycle will equal the sum of the access time from main memory and the delay required for the missed word to be written and read from the cache. The fetch bypass and wraparound load functions minimize this time by initially bypassing the cache and allowing the CPU to directly fetch the missed word from the fetch bypass buffer, which is loaded with the missed word as soon as it is fetched from main memory (figure 1). The CPU can fetch and execute the missed word from the fetch bypass buffer and then proceed to the next address without having to wait for the cache to be updated. The missed data block is concurrently loaded into the wraparound load buffer; after the entire block is fetched from main memory, the cache is updated. If the CPU attempts to fetch the next word in the block before the block is loaded into memory, the CPU may be required to wait for the memory to be updated or, if an additional function exists in the block load buffer, to directly access the next word from the block load buffer.

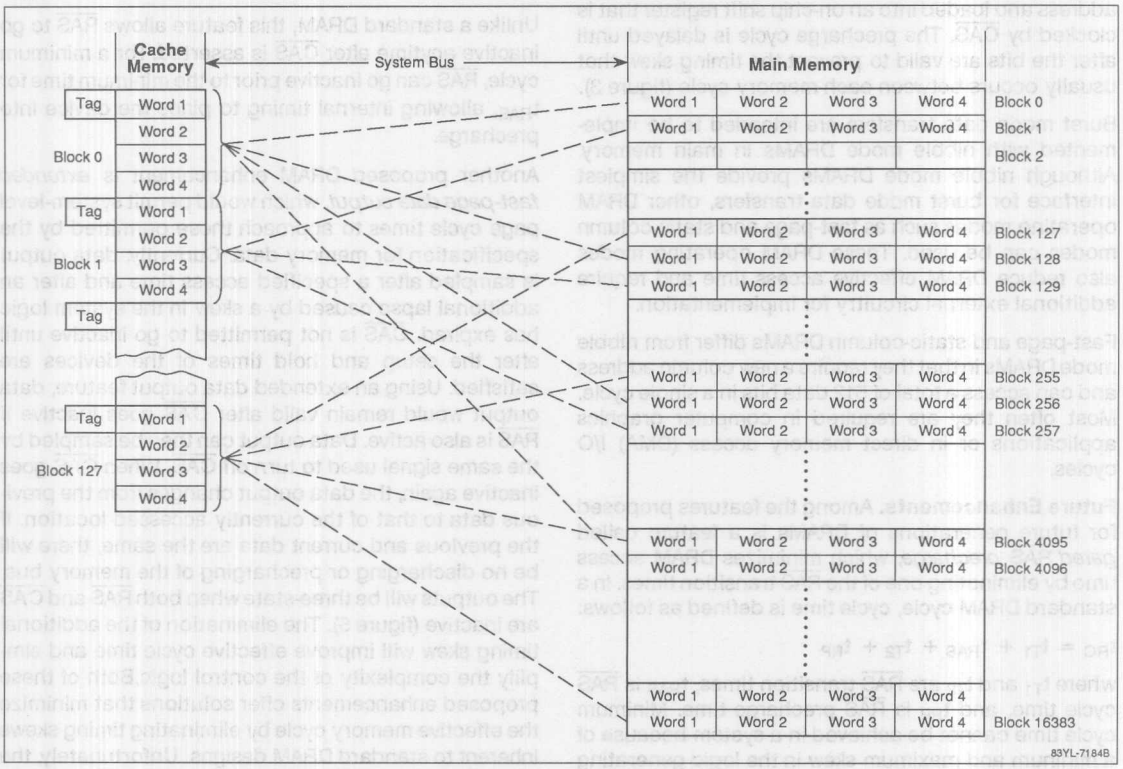
The effective access time of the miss cycle can be minimized by reducing the amount of data required to execute a cache miss cycle. This can be accomplished by employing a data transfer mode, called *burst data transfer*, that requires a single address for each 16 bytes of data rather than separate addresses for each 4 bytes of data. Burst data transfers are implemented in high performance microprocessors such as Intel's 80486, Motorola's 68040, and NEC's V80™. Burst mode allows a 16-byte cache block to be transferred during a cache miss, minimizing the cache miss data transfer time and increasing system bus bandwidth.

Optimizing the Transfer Cycle

As discussed above, during a miss cycle, the missed data is fetched from main memory. The cache block is the data element used to transfer the data between main memory and the cache. The size of the cache data block can be one word, but typically it is more than one word (figure 2). It has been determined that the cache hit rate increases as a function of cache block size and is generally dependent on the properties of program locality, which are enhanced by fetching a large number of consecutive instructions. However, a very large block size increases the time required to transfer the data over the system bus, decreasing the system bus bandwidth and increasing bus latency. Therefore, the choice of block size is a tradeoff between maintaining the cache hit rate and maximizing the system bus bandwidth.

V80 is a trademark of NEC Corporation

Figure 2. Block Transfers for a Direct Mapped Cache



Burst Mode. A 16-byte block size has been implemented in a number of RISC/CISC architectures. This block size is a good compromise between maintaining a high hit rate and minimizing the bus latency during a cache miss cycle. This 16-byte block transfer is called burst mode data transfer and it requires only one address for each 16-byte data transfer. By allowing four consecutive words to be accessed with one address, this feature decreases data transfer time and maximizes system bandwidth.

Although its primary advantage is being able to minimize bus latency and sustain a high hit rate, burst mode would be useless if it could not easily be supported by the interface circuit for main memory. Fortunately, burst mode is designed to be used with DRAMs offering a nibble mode, whereby four consecutive bits can be accessed in a single cycle. In a standard DRAM read cycle, each cycle requires a address that must satisfy the specifications for $\overline{RAS}$ access (t_{RAS}) and precharging (t_{RP}), calculated as follows:

TOTAL CYCLE TIME = $(t_{RAS1} + t_{RP1)} + (t_{RAS2} + t_{RP2})$ + $(t_{RAS3} + t_{RP3})$ + $(t_{RAS4} + t_{RP4})$

The separate address and precharge time represents a significant amount of overhead to complete the memory access.

Nibble mode DRAMs provide additional on-chip circuitry that minimizes total cycle time by eliminating the requirement for precharge between consecutive memory accesses. The nibble mode cycle time is given as follows:

TOTAL NIBBLE MODE CYCLE TIME = $t_{RAS1} + t_{RAS2} + t_{RAS3} + t_{RAS4} + t_{RPN}$

Four consecutive data bits are accessed by a single address and loaded into an on-chip shift register that is clocked by $\overline{CAS}$. The precharge cycle is delayed until after the bits are valid to prevent the timing skew that usually occurs between each memory cycle (figure 3).

Burst mode data transfers are intended to be implemented with nibble mode DRAMs in main memory. Although nibble mode DRAMs provide the simplest interface for burst mode data transfers, other DRAM operating modes such as fast-page and static-column modes can be used. These DRAM operating modes also reduce DRAM effective access time and require additional external circuitry for implementation.

Fast-page and static-column DRAMs differ from nibble mode DRAMs in that they require a new column address and can access a total of 512 data bits in a single cycle. Most often they are required in computer graphics applications or in direct memory access (DMA) I/O cycles.

Future Enhancements. Among the features proposed for future generations of DRAMs is a feature called *gated* $\overline{RAS}$ *precharge*, which minimizes DRAM access time by eliminating one of the $\overline{RAS}$ transition times. In a standard DRAM cycle, cycle time is defined as follows:

$$t_{RC} = t_{T1} + t_{RAS} + t_{T2} + t_{RP}$$

where t_{T1} and t_{T2} are $\overline{RAS}$ transition times, t_{RAS} is $\overline{RAS}$ cycle time, and t_{RP} is $\overline{RAS}$ precharge time. Minimum cycle time cannot be achieved in a system because of a mininum and maximum skew in the logic generating the edges of the $\overline{RAS}$ signal (figure 4). The gated $\overline{RAS}$ precharge feature removes both t_{T2} and the timing skew from the minimum cycle time, as follows:

$$t_{RC} = t_{T1} + t_{RAS} + t_{RP}$$

Unlike a standard DRAM, this feature allows $\overline{RAS}$ to go inactive anytime after $\overline{CAS}$ is asserted. For a minimum cycle, $\overline{RAS}$ can go inactive prior to the minimum time for t_{RAS}, allowing internal timing to place the device into precharge.

Another proposed DRAM enhancement is *extended fast-page data output*, which would permit system-level page cycle times to approach those permitted by the specification for memory data. Currently, data output is sampled after a specified access time and after an additional lapse caused by a skew in the system logic has expired. $\overline{CAS}$ is not permitted to go inactive until after the setup and hold times of the devices are satisfied. Using an extended data output feature, data output would remain valid after $\overline{CAS}$ goes inactive if $\overline{RAS}$ is also active. Data output can then be sampled by the same signal used to turn off $\overline{CAS}$. When $\overline{CAS}$ goes inactive again, the data output changes from the previous data to that of the currently accessed location. If the previous and current data are the same, there will be no discharging or precharging of the memory bus. The outputs will be three-state when both $\overline{RAS}$ and $\overline{CAS}$ are inactive (figure 5). The elimination of the additional timing skew will improve effective cycle time and simplify the complexity of the control logic.Both of these proposed enhancements offer solutions that minimize the effective memory cycle by eliminating timing skews inherent to standard DRAM designs. Unfortunately, the precharge time remains an inherent disadvantage, because consecutive accesses to the memory module will always have a timing skew (t_{RP}).

Figure 3. Types of Data Transfer Cycles

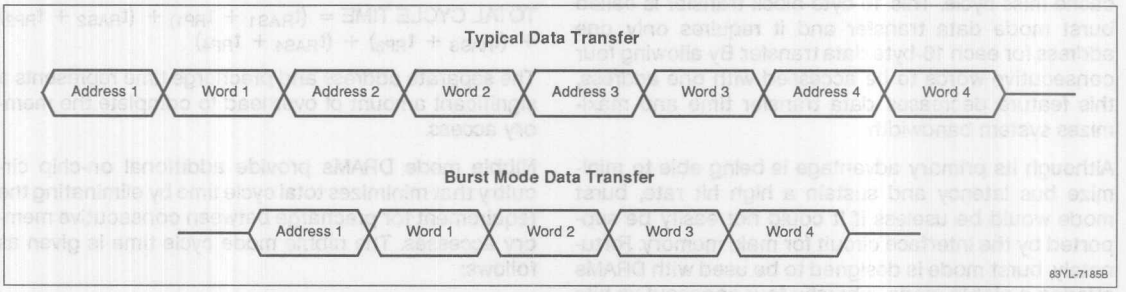
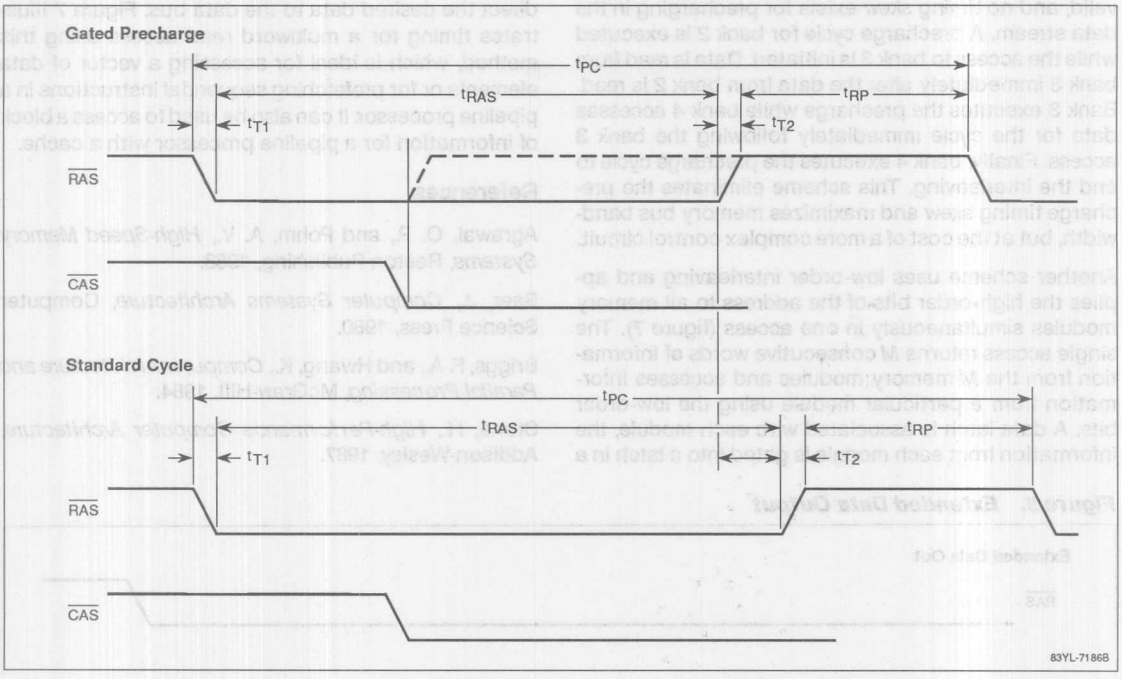


Figure 4. Gated Precharge



Interleaving

In a two-level hierarchy, memory bandwidth in the first level can be optimized by means of a cache that matches the CPU's read cycle time. For cache misses and write cycles, the cache-to-main memory bandwidth can be maximized by means of burst mode data transfers and standard DRAMs with special operating modes.

Interleaving optimizes effective access when more than one row of data needs to be accessed at the same time. Fast-page cycles are a means of reducing access time for bits located in the same row of the memory array, but they are inefficient for handling the consecutive access of data residing in different row addresses. To fetch diagonal elements in the matrix, the system needs to concurrently access row 1 and column 1, row 2 and column 2, etc. Page cycles can't be used in this scheme because a new row must be accessed for each data element.

A memory system organized to distribute the address to several banks simultaneously is said to be interleaved. The interleaving of addresses among *M* modules is called *M*-way interleaving and allows consecutive access to *M* memory banks. In high-order interleaving, the addresses are distributed so that the memory modules contain consecutive addresses. High-order bits are used to select the module while the low-order bits are used to select the address within the module. A second method, called low-order interleaving, distributes the address so that consecutive addresses are located within consecutive modules. The low-order bits of the address select the module, while the remaining bits select the address within the module.

In a low-order interleaved system, the memory is organized into banks with each bank providing data bits equal to the width of the CPU memory bus. An address is latched by the memory circuit and the low-order bits are decoded to determine the number of banks to be accessed (figure 6). If four banks are accessed, they are said to be four-way interleaved.

A memory controller circuit initially generates the control signals for the accessing of bank 1. The data for access 1 will be valid after the specified time for t_{RAS} has elapsed, after which the accessed bank will be precharged. Control signals are simultaneously being generated for bank 2, and they may be skewed by a system clock to accommodate data access for the second fetch from the CPU. Data from bank 2 becomes

valid immediately after the data from bank 1 becomes valid, and no timing skew exists for precharging in the data stream. A precharge cycle for bank 2 is executed while the access to bank 3 is initiated. Data is read from bank 3 immediately after the data from bank 2 is read. Bank 3 executes the precharge while bank 4 accesses data for the cycle immediately following the bank 3 access. Finally, bank 4 executes the precharge cycle to end the interleaving. This scheme eliminates the precharge timing skew and maximizes memory bus bandwidth, but at the cost of a more complex control circuit.

Another scheme uses low-order interleaving and applies the high-order bits of the address to all memory modules simultaneously in one access (figure 7). The single access returns *M* consecutive words of information from the *M* memory modules and accesses information from a particular module using the low-order bits. A data latch is associated with each module, the information from each module is gated into a latch in a fetch cycle, whereupon a multiplexer can be used to direct the desired data to the data bus. Figure 7 illustrates timing for a multiword read access using this method, which is ideal for accessing a vector of data elements or for prefetching sequential instructions in a pipeline processor. It can also be used to access a block of information for a pipeline processor with a cache.

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Figure 5. Extended Data Output

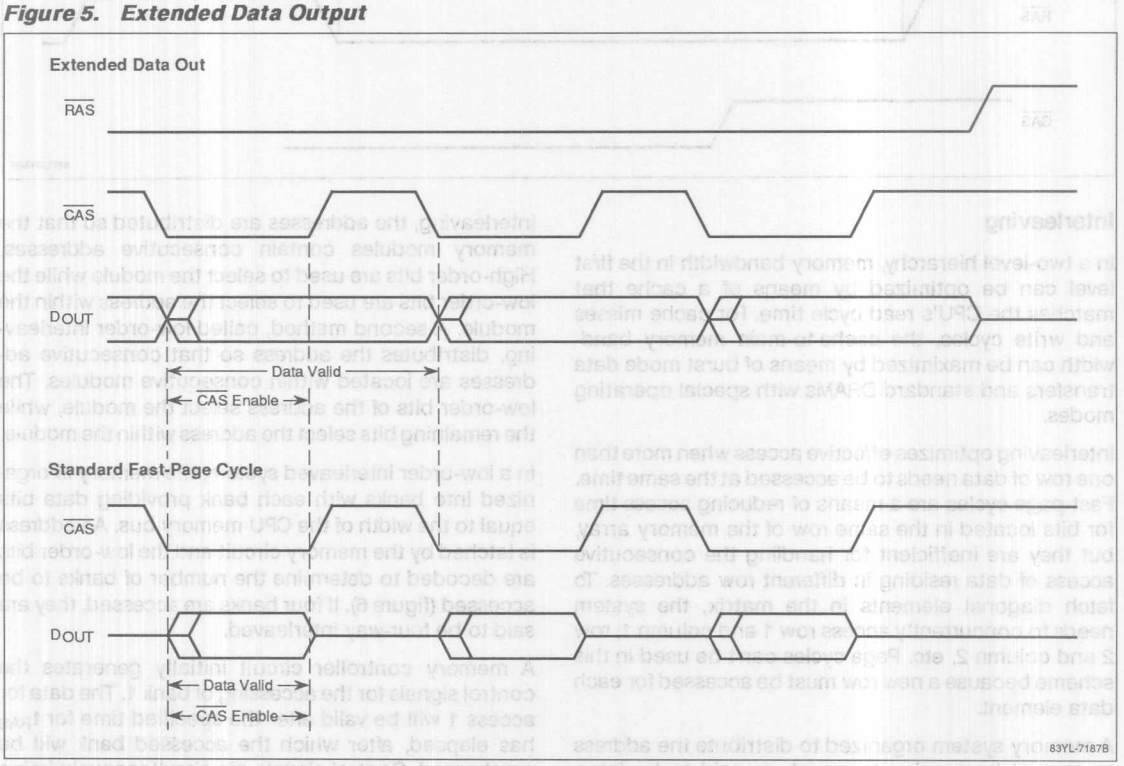


Figure 6. Low-Order Interleaving with Concurrent Access

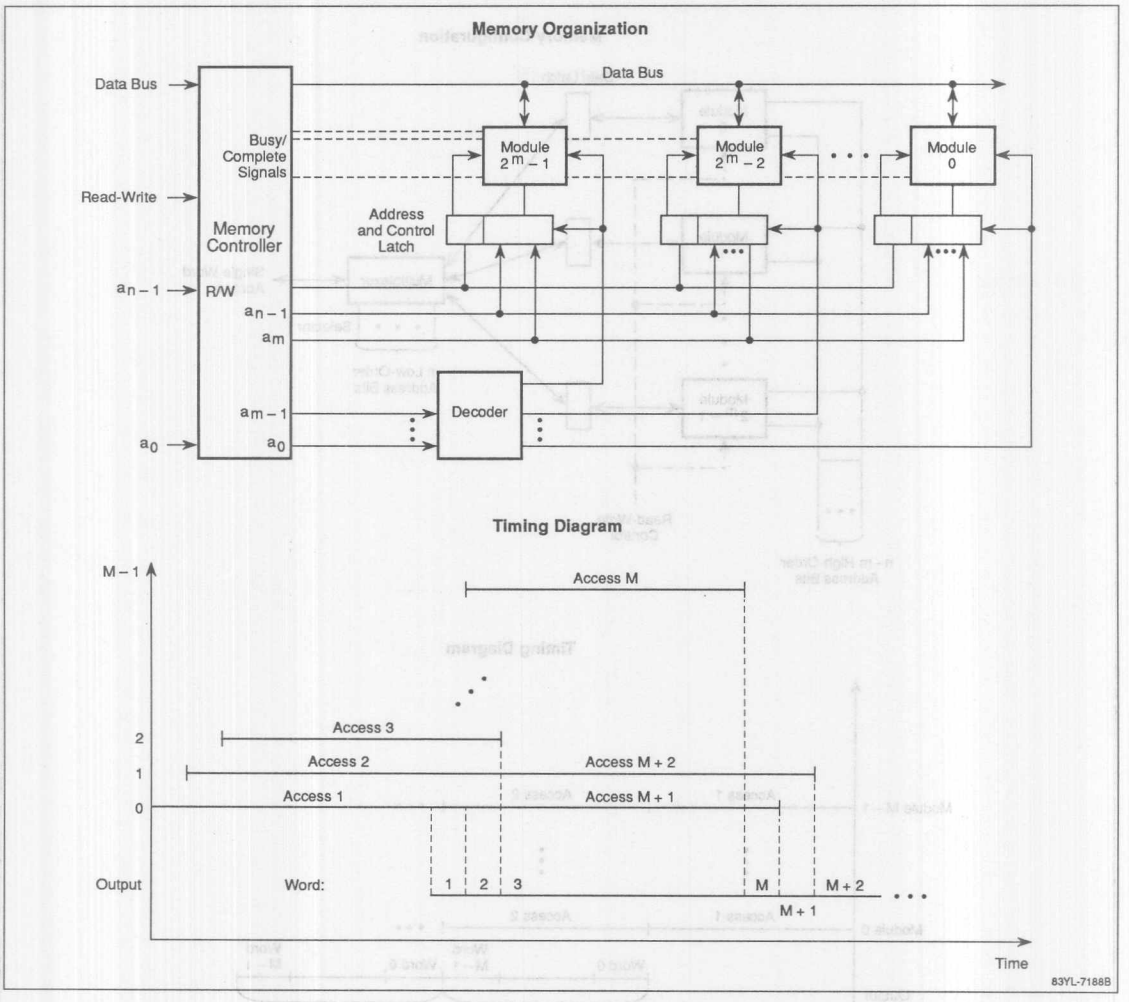
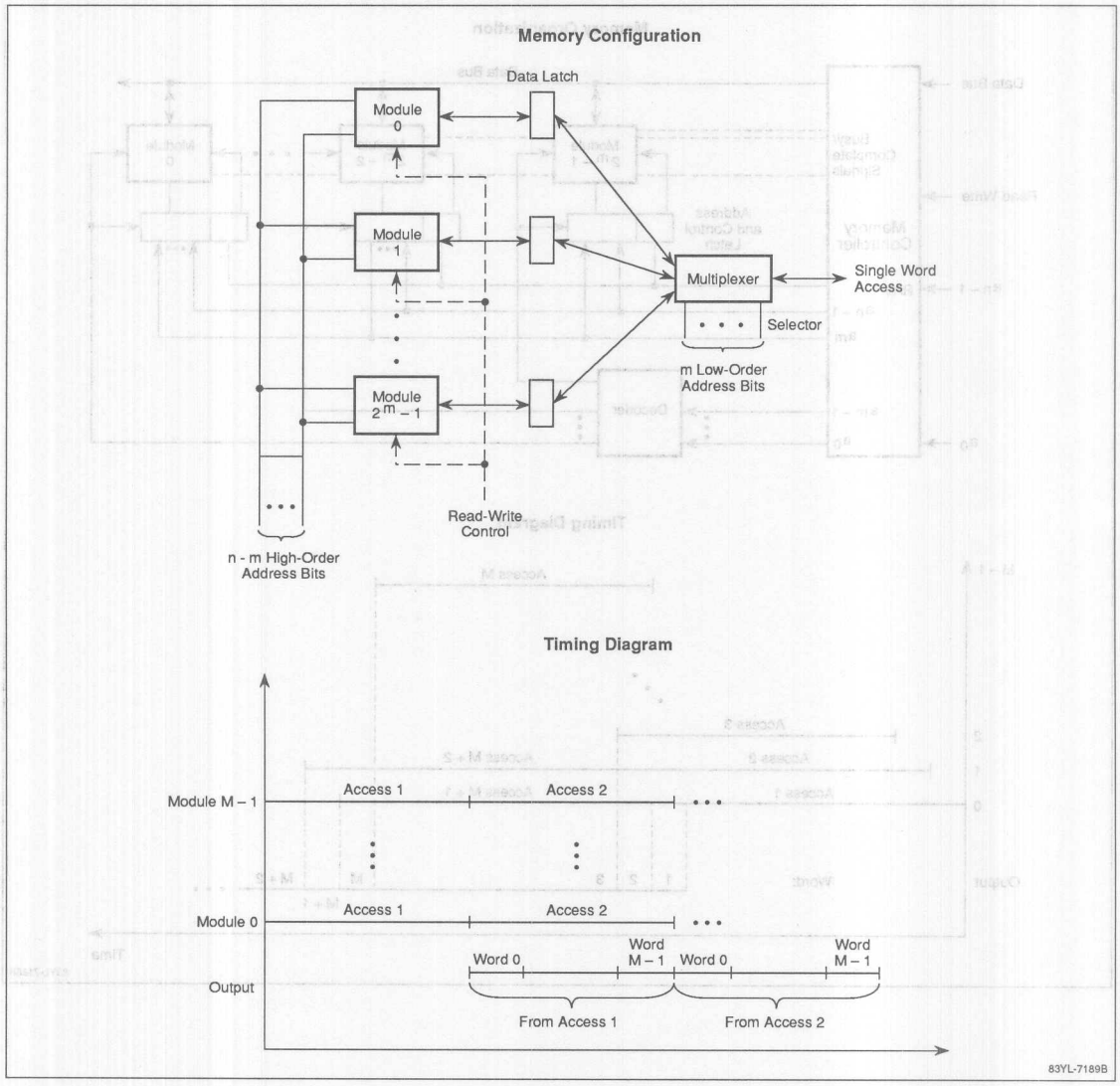


Figure 7. Low-Order Interleaving with Simultaneous Access



Introduction

The objective of a memory system is to match the operating speed of a processor with the rate of information transfer. A CPU is usually about a thousand times faster than the average access time of a memory system, and the high cost of implementing a system with enough speed to accommodate this performance gap would be out of reach. To be able to meet cost and performance goals, a multilevel or hierarchical system encompassing a mix of memory devices must be implemented.

In most of these systems, the top level will have the highest performance and lowest level the slowest. Alternatively, the highest level is usually the most expensive and has the smallest density and the lowest level is the least expensive and has the highest density. Hierarchies are typically structured so that devices at level i are higher than those at level $i + 1$. If C_i, T_i, and S_i, respectively, are the cost per byte, the average access time, and the total memory size at level i, then the following relationships normally would hold between level i and $i + 1$:

$C_i > C_i + 1$, $T_i < T_i + 1$, and $S_i < S_i + 1$ for $i \geq 1$

Memory hierarchy can be classified into primary and secondary devices, depending on access times. In a typical hierarchy, the top level may consist of fast static RAMs with access times of less than 35 ns. These devices have been produced in x1, x4 and x8 organizations, and in some cases need a very low current to retain data during power failures. The next level is classified as main memory and consists of dynamic RAMs with access times between 80 and 120 ns. Secondary memory may consist of several levels of rotating drum or fixed-head magnetic disks with average times taken from the sum of rotational latency and transfer time, most likely a few milliseconds for blocks or sectors of between 1 and 4 Kbytes. Their capacity is in the Mbyte range and reflect a price equaling a few hundredths of a cent per bit. These devices are usually connected to the primary memory on a shared bus. Finally, the lowest level consists of removable magnetic tape for offline storage in a data archive.

A performance gap traditionally has existed between primary and secondary memories. The magnetic bubbles and charge-coupled devices developed to fill this gap did not find wide acceptance in most memory system applications, and contemporary designs are now using low-power, solid-state devices such as NEC's μPD42601 silicon file.

The goal of a system designer is to optimize the memory hierarchy so that system performance approaches that of the highest level of memory and cost approaches the cost of the cheapest memory. Performance depends on a number of interrelated factors, including program behavior with respect to memory references, access time and memory size of each level, granularity of information transfer (size of the data field or block), and management policies. One other important factor is the design of the processor-memory interconnection network.

Hierarchical performance can be measured by *effective access time* from the processor to the lowest level of the hierarchy, i.e., the sum of individual average access times of each of the memory levels. Effective access time generally includes the wait time caused by memory conflicts at a particular level, as well as delays in the switching network between one level and the next. The degree of conflict is usually a function of the number of processors, the number of memory modules, and the interconnection network between the processors and memory modules.

Connections between hierarchical levels are characterized by their transfer rates, or bandwidth, i.e., the number of bits per second that can be accessed. For example, if a memory system has a cycle time of 500 ns and is able to access 32 bits (4 bytes) per cycle, its bandwidth is 64 Mbits (8 Mbytes). To increase bandwidth, a designer might choose to reduce the cycle time, increase word size of the memory, or access the memory modules in parallel. Each would have a different impact on system architecture and cost.

Although the best possible design depends on workload and the available technology, there is no one formula for creating an optimal generic design. When considering a traditional von Neumann architecture, a single memory module of conventional design can access no more than one word during each clock cycle. With this fundamental constraint, the designer must rely on technological advances to be able to improve computer system performance.

HIERARCHICAL CLASSIFICATIONS

High-Speed Static RAMs at Level 1

Although the highest hierarchical level contains memory capable of matching the cycle time of the CPU, capacity of these devices typically will be determined by the cost and performance goals of the system. Static RAM traditionally has been used in this level because of its performance capabilities and ease of use. An SRAM is basically a stable dc flip-flop requiring no clocks or refreshing, which means its storage element retains data as power is applied. Fast access times, a parallel address structure, and the absence of strict timing requirements have made these devices very attractive in cache and small system designs.

SRAMs have been developed with technologies such as Bipolar, CMOS and BiCMOS, resulting in a number of products with different access times and organizations. Some of the most common configurations are 32K x 8, 64K x 4 and 256K x 1, 1M x 1 and 256K x 4, as reflected in NEC's μPD43256A, μPD43254, μPD46251, μPD431001 and μPD431004 devices, respectively. In the small system market, where low cost rather than high performance is the primary objective, byte-wide SRAMs with access times similar to DRAMs or EPROMs are required. Alternatively, cache memory design requires very fast access time, high density, and x1 or x4 organizations with high performance and advanced SRAM technology.

Some SRAMs have the ability to retain data when system power has failed or is shut down. In this case, the SRAM is usually designated as a low-power device (-LL version) whose data retention current can be as low as 10 μA and whose backup power is supplied by a battery backup circuit. This feature is attractive in small laptop systems and in instrumentation applications where low power is a primary concern.

The byte-wide SRAM such as NEC's 32K x 8-bit μPD43256A has access times in the range of 85 to 150 ns, 28-pin DIP packaging (600 mil wide), and access time compatibility with EPROMs (figure 1). However, a 600-mil device requires a substantial amount of board space (figure 1), and thus the part is also offered in a 28-pin plastic miniflat package for higher density, surface-mounted printed circuit board applications (figure 2).

A x1 SRAM is often used for large, high-speed memory circuits where fast access time and high-density chip layouts are required. Having only one data bit per SRAM chip reduces the pin count and allows use of an

Figure 1. 28-Pin Plastic DIP (600 mil)

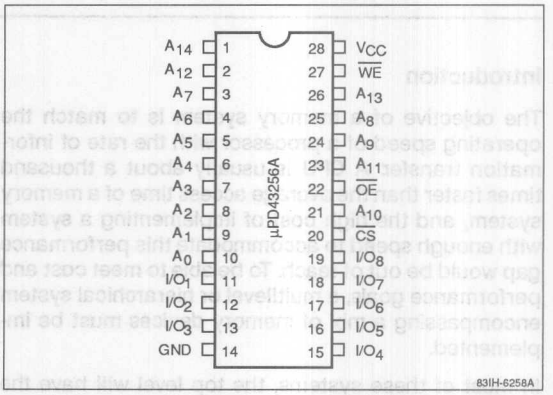
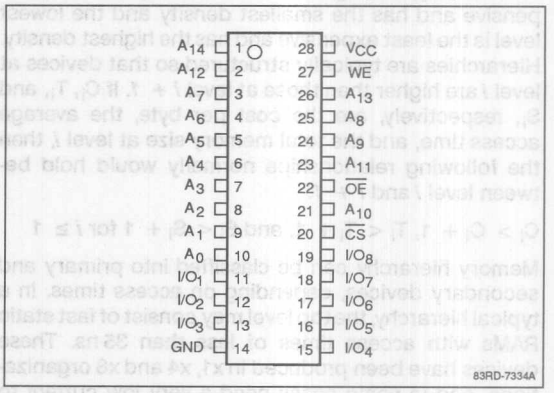


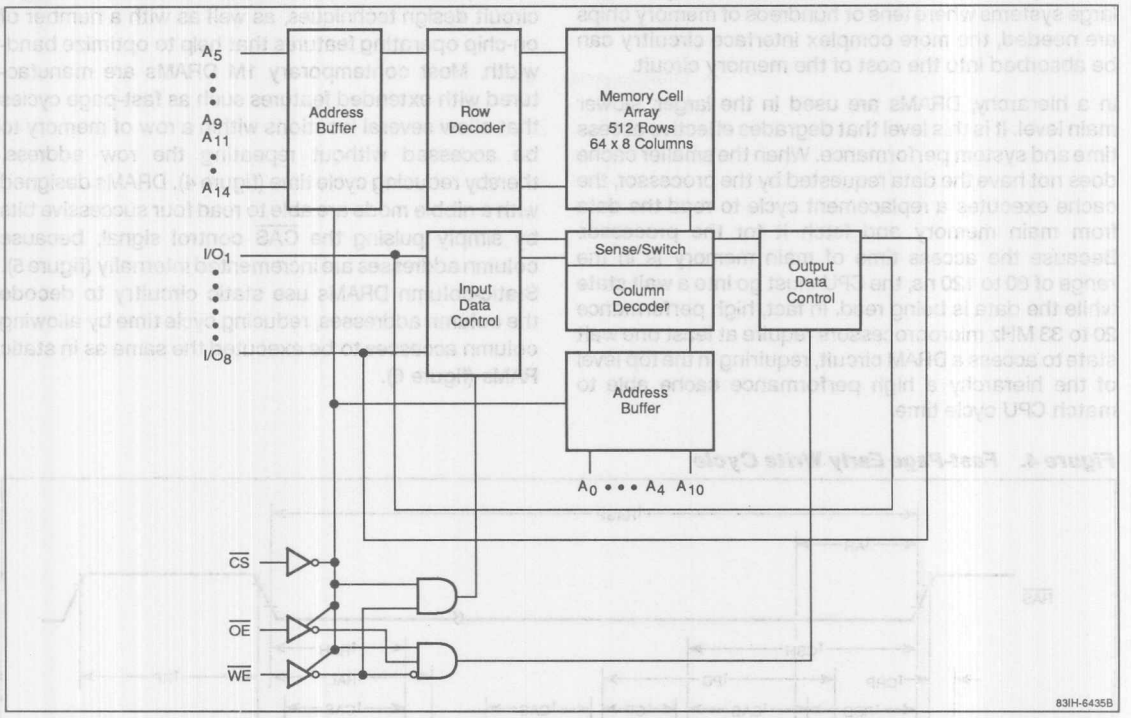
Figure 2. 28-Pin Plastic Miniflat (450 mil)



18- or 22-pin package that significantly reduces board space. High-speed static RAMs are available in x1, x4, and x8 configurations with access times ranging from 15 to 80 ns. A typical application for these devices is as data and address tag memories in cache subsystems whose access times must equal processor access times.

One advantage of using an SRAM is its ability to interface to a memory bus. The μPD43256A, for example, has 15 address lines, 8 common input/output signals, an output enable ($\overline{OE}$) pin, a write enable ($\overline{WE}$) pin, and power and ground pins (figure 3). A chip select ($\overline{CS}$) pin controls operation of the device. When $\overline{CS}$ is high, the device is in standby and power consumption is greatly reduced. A designer can minimize total power supply current by enabling only the accessed devices in standby.

Figure 3. Block Diagram of μPD43256A



The $\overline{OE}$ pin controls the three-state output drivers during a read cycle and can only be active when $\overline{CS}$ is asserted. Write cycles are controlled by $\overline{WE}$. When $\overline{CS}$ and $\overline{WE}$ are asserted low, data on the common I/O pins is written into the memory cells and the output data drivers are disabled to prevent a possible bus fight.

The separation of the chip select function into two components, $\overline{OE}$ and $\overline{CE}$, has several timing implications. The access times from chip select (t_{ACS}) and address valid (t_{AA}) are the same in the μPD43256A, 85 ns, but typically an SRAM design requires that the address be decoded before the chip can be selected. This decoding function requires an additional delay, making the effective address time the sum of the worst case propagation delay of the address decoder (74LS138) and the chip select address access time (t_{ACS}). Alternatively, since the output enable time (t_{OE}) of 40 ns is less than the access time, the effective access time can be optimized by concurrently accessing the SRAM with a valid address and controlling the $\overline{OE}$ pin with a read signal and the output of the address decoder. The disadvantage of this scheme is that the $\overline{CS}$ pin is always asserted, causing the SRAM to always be active. For circuits with only a few SRAM devices, the power considerations are not important. In cases where a lot of SRAMs are being used, power requirements may necessitate that $\overline{CS}$ be asserted to control the active and standby current.

Dynamic RAMs at Level 2

Data in an SRAM cell will remain valid as long as power is applied to the chip, because data is stored as a 1 or 0 in a flip-flop circuit consisting of four or six transistors. This approach allows for simplified operation, although the relatively large memory cell requires a large die. A dynamic RAM, on the other hand, stores data in the charge on a capacitor rather than in a flip-flop, thereby reducing the area required for each cell. And since die size has a direct bearing on the cost of a chip, a denser DRAM circuit will have a lower cost per bit.

Using a capacitor to store memory data means that more complex circuitry is required, as well as sophisticated techniques to sense the charge on the storage capacitor. Because of leakage current, a method of periodically refreshing the charge on the capacitor is

also required. Since DRAMs are traditionally used in large systems where tens or hundreds of memory chips are needed, the more complex interface circuitry can be absorbed into the cost of the memory circuit.

In a hierarchy, DRAMs are used in the larger, slower main level. It is this level that degrades effective access time and system performance. When the smaller cache does not have the data requested by the processor, the cache executes a replacement cycle to read the data from main memory and fetch it for the processor. Because the access time of main memory is in the range of 80 to 120 ns, the CPU must go into a wait state while the data is being read. In fact, high performance 20 to 33 MHz microprocessors require at least one wait state to access a DRAM circuit, requiring in the top level of the hierarchy a high performance cache able to match CPU cycle time.

DRAM performance can be enhanced with a number of circuit design techniques, as well as with a number of on-chip operating features that help to optimize bandwidth. Most contemporary 1M DRAMs are manufactured with extended features such as fast-page cycles that allow several locations within a row of memory to be accessed without repeating the row address, thereby reducing cycle time (figure 4). DRAMs designed with a nibble mode are able to read four successive bits by simply pulsing the $\overline{CAS}$ control signal, because column addresses are incremented internally (figure 5). Static-column DRAMs use static circuitry to decode the column addresses, reducing cycle time by allowing column accesses to be executed the same as in static RAMs (figure 6).

Figure 4. Fast-Page Early Write Cycle

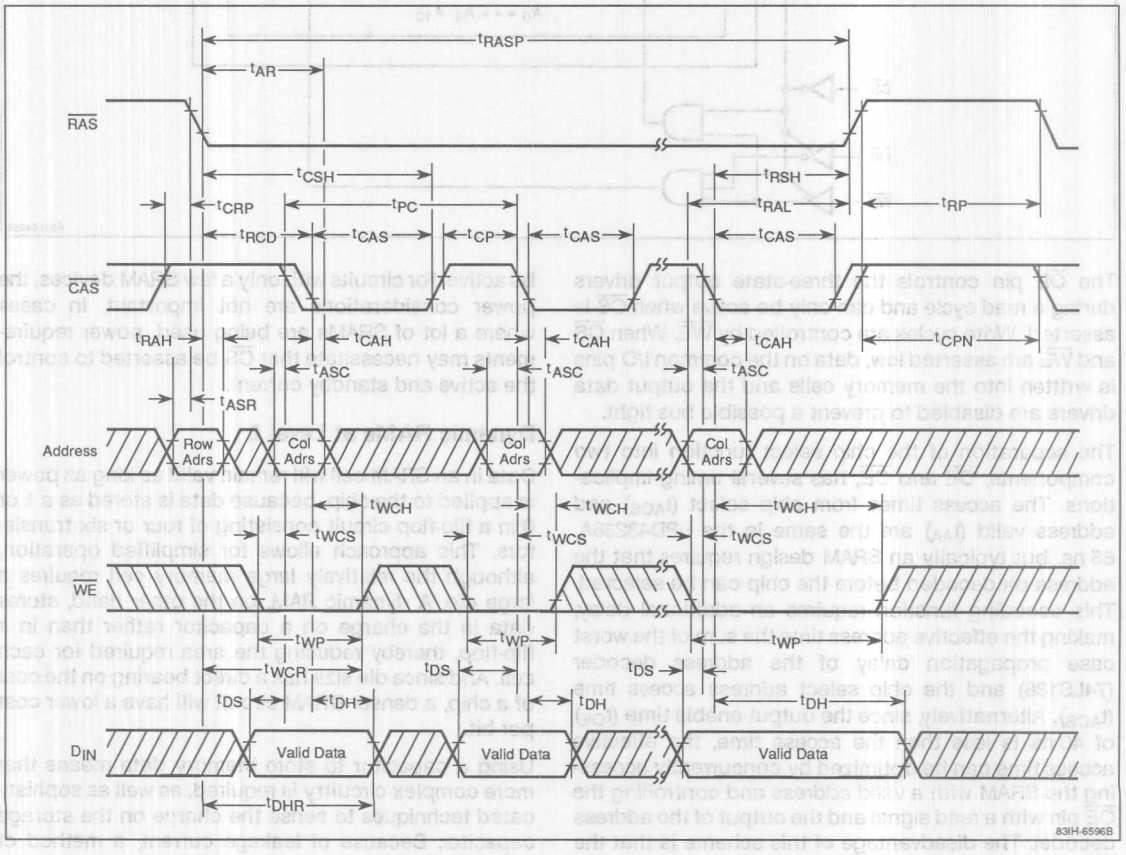


Figure 5. Nibble Mode Read Cycle

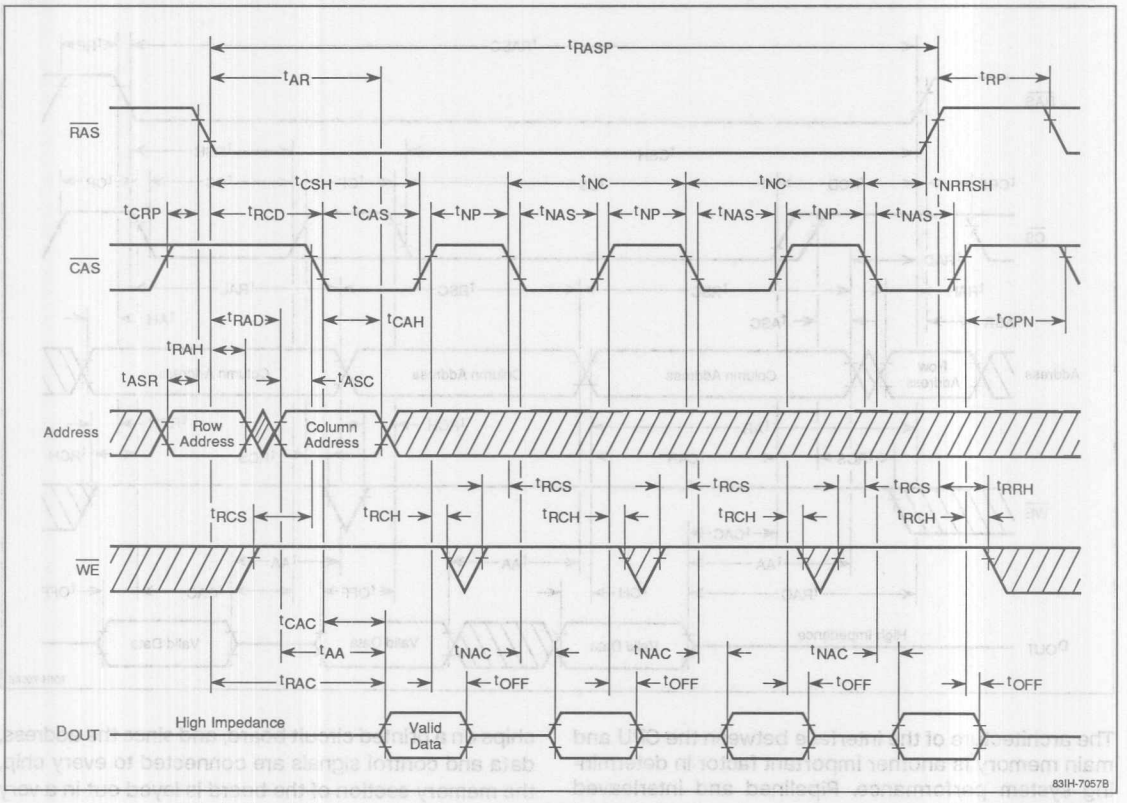
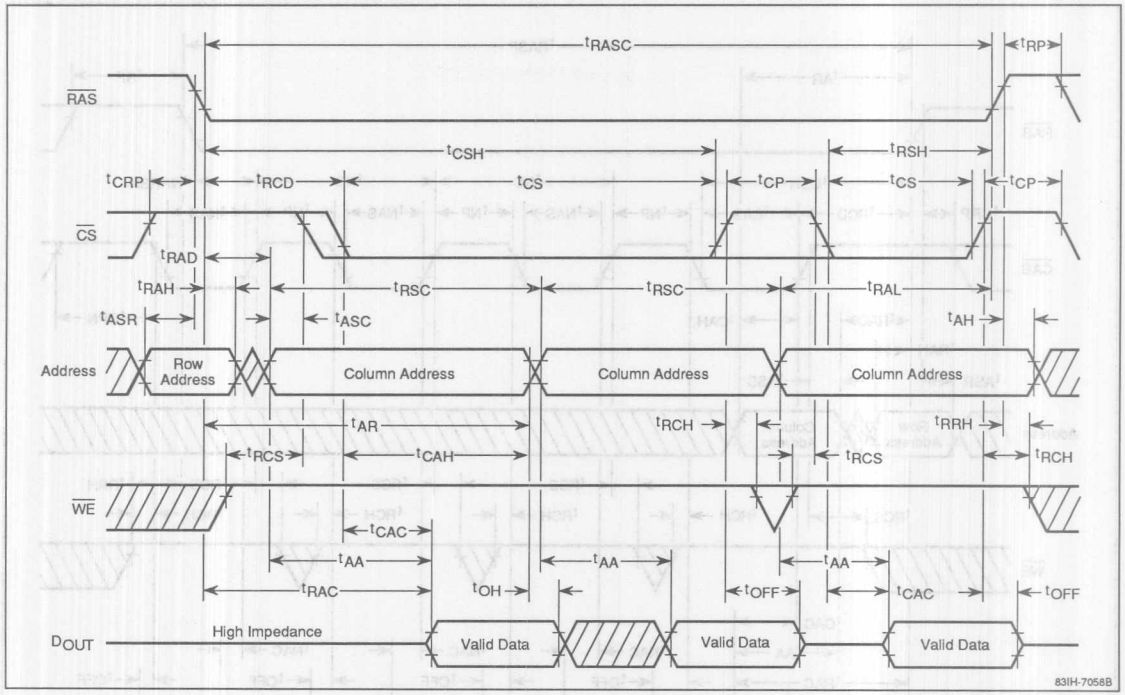


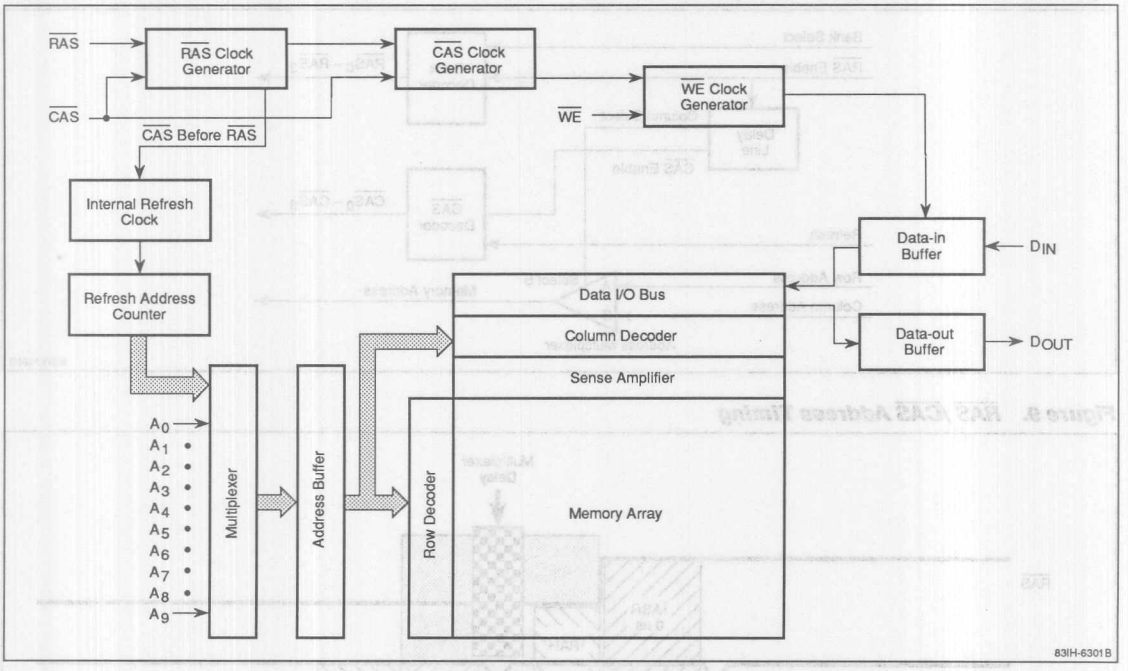
Figure 6. Static-Column Read Cycle



The architecture of the interface between the CPU and main memory is another important factor in determining system performance. Pipelined and interleaved architectures that can access the device in parallel operations can also enhance bandwidth, but require another level of complexity and cost in the CPU-memory interface.

In main memory design, the most efficient DRAM configuration is the x1 DRAM because its organization minimizes the number of pins on the chip (figure 7). Main memory circuits may have hundreds of memory chips on a printed circuit board, and since the address, data and control signals are connected to every chip, the memory section of the board is layed out in a very dense array. In fact, one of the most important parts of the DRAM design is the printed circuit layout. This array requires a memory chip with minimal pins and package size, making the x1 the most efficient. Also, with the high number of memory chips for each circuit, the cost of the circuit is high compared to other system boards and requires a higher system reliability standard.

Figure 7. Block Diagram of 1 Meg DRAM



An error correction and detection technique is typically used to enhance reliability. Most ERCC algorithms can detect two-bit errors and correct single-bit errors, allowing a single memory chip to fail without causing the system to malfunction. If the circuit uses a x4 organization and a single chip failure occurred, the ERCC circuit could not correct the multibit failure, reducing system reliability. Also, a x4 DRAM has more pins, a larger package size, and higher costs, increasing the size and cost of the memory array.

The wider organization does have one advantage for systems that require the number of memory chips to be limited because of layout area or cost. One x4 chip can replace four x1 devices in applications where density is not a factor. A typical application for the x4 organization is in computer graphics where memory size is constrained by screen resolution and the 4:1 increase in bandwidth is required to refresh the screen.

Some disadvantages of using DRAMs involve their complex interface circuitry and dynamic nature. DRAMs are arranged in a rectangular array, in which the cells are connected in a matrix of rows and columns. To be able to reduce the number of address pins, the address field is multiplexed into a row address field and a column address field (figure 8). A row address is first presented to the memory and the row address strobe ($\overline{RAS}$) control signal is asserted, beginning the memory cycle and latching the row address. The row address decoding circuit selects the appropriate row of cells (512 cells in the case of a 1M DRAM) and the column address is multiplexed onto the address pins.

Figure 8. $\overline{RAS}$ /$\overline{CAS}$ Address Multiplexer Circuit

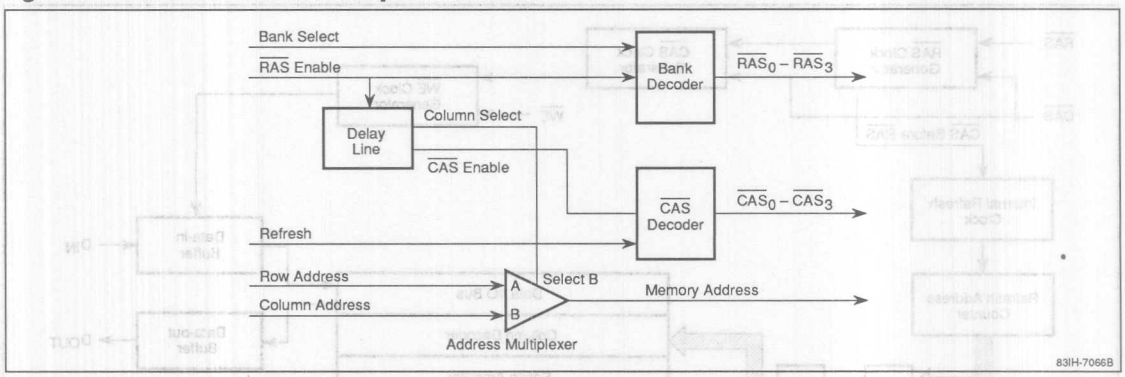
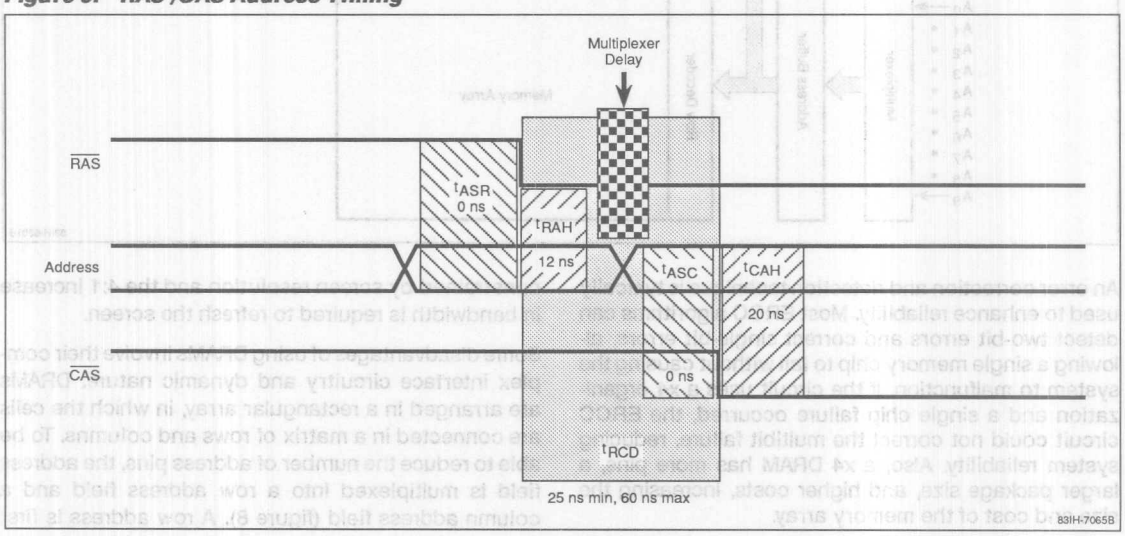


Figure 9. $\overline{RAS}$ /$\overline{CAS}$ Address Timing



The column address strobe ($\overline{CAS}$) is then asserted to latch the column address and enable the output drivers. The column address decoder selects one of the memory cells in the selected row and the data is read and sent to the output circuits. Once the data has been accessed, the $\overline{RAS}$ and $\overline{CAS}$ signals are de-asserted and remain inactive for a specified precharge time so that the circuits can recover from the previous access. Thus, the increase in cycle time over access time equals the precharge time.

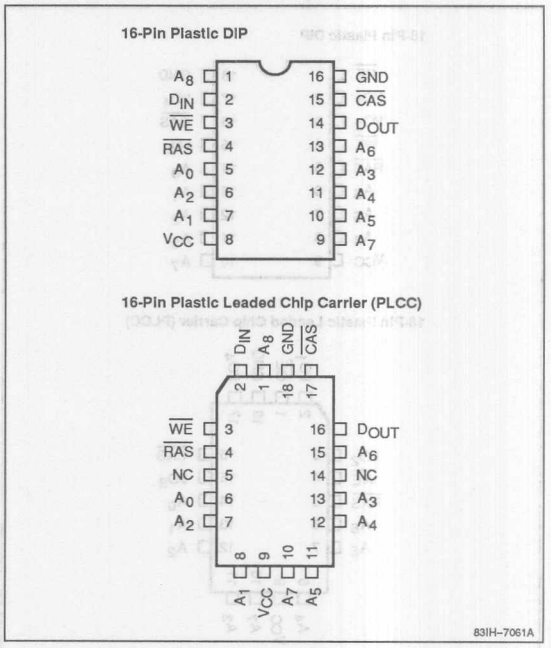
DRAMs with an access time of 80 ns typically have a cycle time of 160 ns. Although multiplexing provides some substantial system benefits in terms of minimizing the number of pins and reducing package size, the address timing is complicated and requires more interface circuitry (figure 9). Row and column addresses are both multiplexed, presenting a rather tight window during which the individual events must occur. Row and column addresses both have setup and hold times with respect to $\overline{RAS}$ and $\overline{CAS}$, and if these specifications aren't met, the read or write cycle could fail. Therefore, the designer must consider the complex requirements very carefully, eliminating any timing skews, control or address line noise, and power supply noise.The dynamic nature of a DRAM means that data is stored in the charge of a capacitor, causing the charge to leak over time and the data to be lost. To prevent data loss, the DRAM must be periodically accessed to guarantee

that the charge will remain in memory. This operation is called a refresh cycle and for a 1M DRAM, all 512 rows have to be refreshed every 8 ms. This requires the DRAM interface circuit to access each row in the memory by means of either a read, write, or refresh cycle every 15.6 μs. Failure to execute a refresh cycle in the specified interval will cause the cell to leak off the charge, resulting in data errors. A refresh cycle consists of using a row address to access the appropriate row and executing a $\overline{RAS}$ cycle to refresh all the cells in that row. No $\overline{CAS}$ or column address is required.

DRAMs specify several refresh cycles: $\overline{RAS}$-only refreshing in which an external counter drives the address on the address pins; $\overline{CAS}$ before $\overline{RAS}$ refreshing in which an internal address counter is used; and hidden refreshing which is executed during a normal refresh cycle. For all refresh cycles, an external timer is required to signal the control circuit to initiate the cycle. Memory control circuitry must also have to arbitrate between an active refresh request and active memory cycle, ensuring that the refresh interval is not exceeded.

An important system design consideration is the standardization of pinouts and package size so that the circuit can be upgraded with the next generation of higher density chips (figures 10, 11, 12, 13). It is also advantageous to design a circuit with options that allow the density of the memory board to be upgraded, saving the expense of developing a new board with each new generation. For example, in the past, a memory board could be designed to easily accommodate both 64K x 1 and 256K x 1 DRAMs, both of which were packaged in a 16-pin plastic DIP. The only difference was that most 64K memory chips had one pin designated as a *no connection*. To accommodate the 256K x 1 device, the extra address line A_8 was added to the circuit to allow operation with both devices.

Figure 10. Typical 256K x 1 DRAM Pin Configuration



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Figure 11. Typical 64K x 4 DRAM Pin Configuration

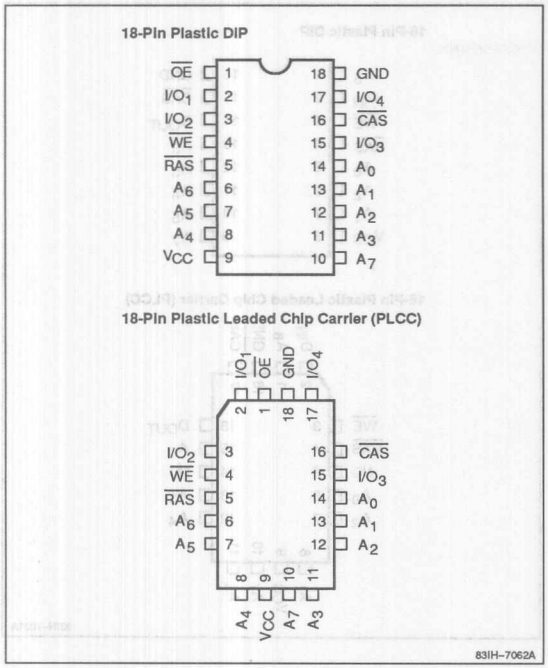


Figure 12. Typical 1 Meg x 1 DRAM Pin Configuration

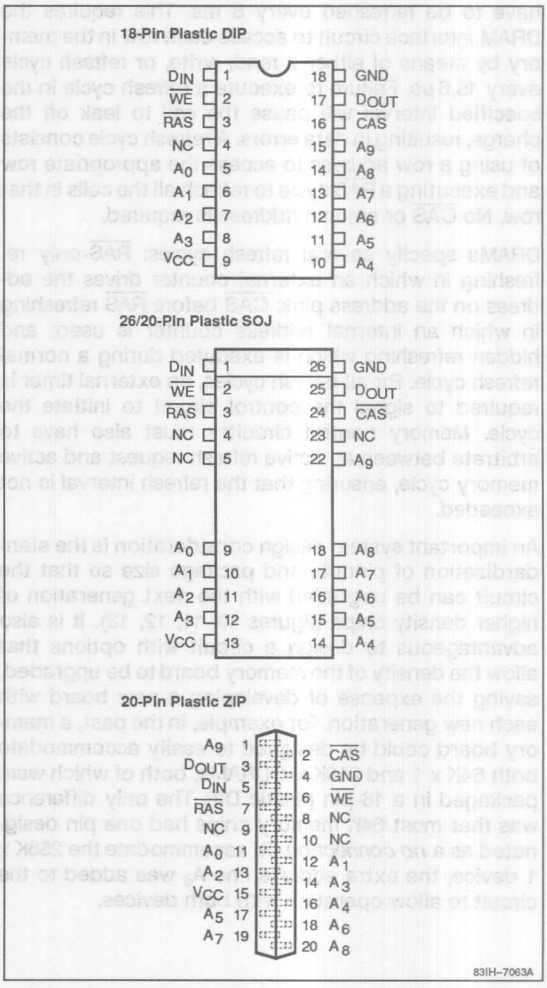
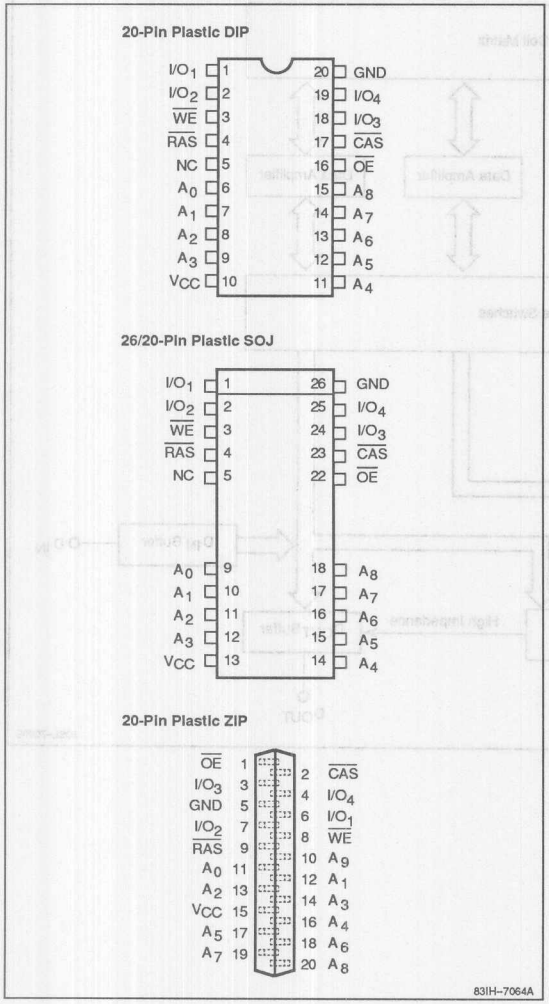


Figure 13. Typical 256K x 4 DRAM Pin Configuration



Designing the system to use either memory size also affects the multiplexing and address decoding logic. Compatibility between 256K and 1M DRAMs is more difficult because the number of pins increases from 16 to 18 pins to accommodate the additional A_9 address. The current 1M and future 4M DRAMs have the same number of pins, with the additional A_{10} address line designated for pin 4 on the DIP package, pin 5 on the SOJ, and pin 10 on the ZIP. The trend in DRAM packaging is evolving from predominantly DIP packages in the 256K era to surface-mounted SOJs and high-density ZIPs in the 1M and 4M eras.

The size of the package is another concern the designer must address when choosing 1M and 4M DRAMs. The transition from 256K to 1M DRAMs saw a change from the 16-pin packages to 18-pin packages. The 1M to 4M evolution represents a crossover generation in SOJ package width—from 300 to 350 mils. NEC's SOJ-packaged 1M μPD421000 has a specified width of 300 mils, but because of the larger die needed to implement the 4M DRAM, a width with an additional 50 mils is required for the initial 4M SOJ package. The 1M and 4M ZIP packages remain the same size, while the 4M DIP is 100 mils larger than the 300-mil DIP for the 1M DRAM. Because the surface-mounted SOJ package is projected to be the dominant package type in the future, some manufacturers may market compatible 300-mil packages for the 1M and 4M devices, but the trend will be toward even larger package sizes. For example, packages for the 16M DRAMs are likely to be 400-mil SOJs and 475-mil ZIPs, while the DIP package eventually will be phased out.

The typical development cycle of a DRAM includes a second generation of 4M DRAMs, scaled in size to optimize access time and die size. This scaled or shrink version will allow the die of a 4M DRAM to be mounted in a 300-mil SOJ package that is compatible with the SOJ package of a 1M DRAM. Also, the shrink version of the 4M DRAM will provide a very fast access time of 60 ns.

The trend in DRAM technology has seen a quadrupling in capacity about every two to four years, a result of fewer features and estimates that the 64M DRAM could use 0.35 μm technology. One major concern with very high density memory chips is test time. The widely used GALPAT standard has a test complexity of $4n^2 + 4n$ for an n-bit RAM and needs about 162 days to test a 4M RAM chip with a cycle time of 200 ns, which is unacceptable in today's manufacturing environment.

To reduce this test time, NEC has built into its μPD421000 1M DRAM a test function that reorganizes the 1M x 1-bit part into a 256K x 4-bit configuration (figure 14). The 1M test mode is enabled by applying a super voltage (V_{CC} + 3 volts) to pin 4 on the 1M DIP package (figure 15). While this super voltage is being applied, the internal configuration is changed to a 4-bit width intended to be used in a testing environment rather than in a circuit environment. Pin 4 should be regarded as a no connection, and as long as standard TTL voltage levels are connected to this pin, the 1M DRAM will remain in its normal operating state.

Figure 14. Internal Test Circuit Block Diagram

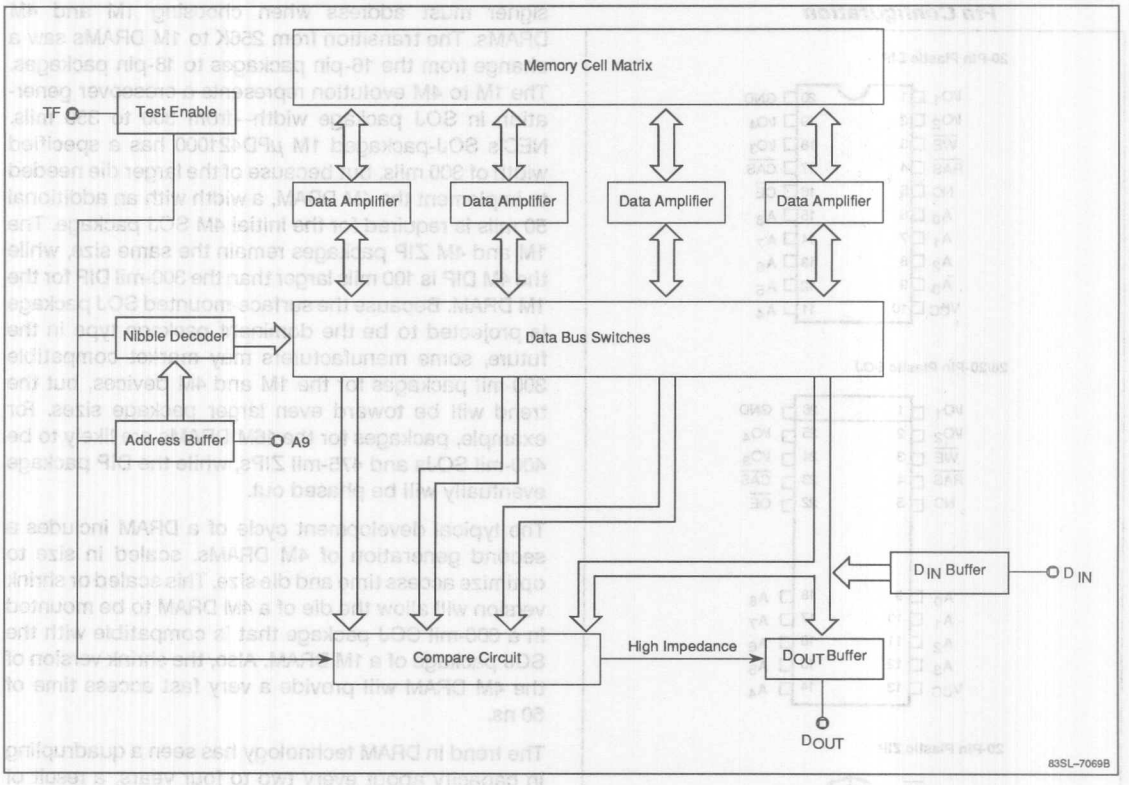
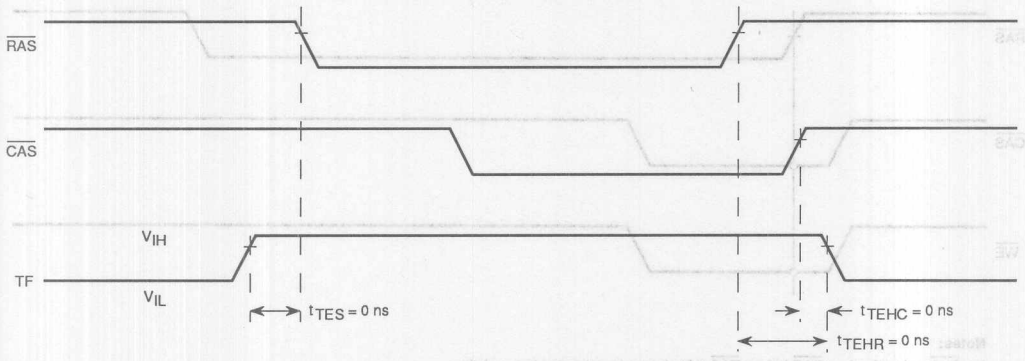


Figure 15. Timing of 1 Meg DRAM Internal Test Circuit



Notes:

[1] $V_{IH} = 9.5\ V + V_{CC}/2$.

[2] $V_{IL} = 1\ V$ min and 7 V max.

[3] Maximum voltage = 12.5 V.

[4] When a test cycle is executed, access times, device power, and the level of V_{CC} are higher than normal. Therefore, a test cycle should only be executed for verifying functional operation of the device.

[5] Data output is high impedance during a write cycle in read-modify-write test operation.

[6] Data output is high impedance after $\overline{RAS}$ goes high in a hidden refresh cycle.

[7] Four bits in a test cycle are treated the same as four bits in nibble mode.

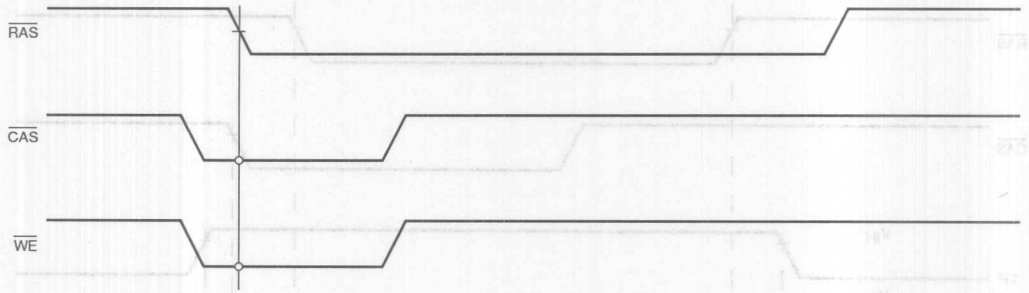
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The same test strategy is implemented for the 4M DRAM, except that pin 4 on the DIP package becomes the new A_{10} address line and the test mode is initialized with logic functions rather than a super voltage. The 4M test mode will be initialized when the $\overline{WE}$ and $\overline{CAS}$ signals are active before the $\overline{RAS}$ signal is asserted, similar to a $\overline{CAS}$ before $\overline{RAS}$ refresh cycle, except that $\overline{WE}$ is asserted at the same time as the $\overline{CAS}$ signal (figure 16). The memory designer must ensure that the memory control logic does not execute $\overline{WE}$ and the $\overline{CAS}$ before $\overline{RAS}$ cycle during normal operation, which would cause the device to be configured into a 4-bit organization and errors to occur. The test issue is a major concern for future DRAM products. The 16M DRAM may have a built-in test circuit that can execute simple test programs and detect on-chip failure, but at this time no standard 16M test procedure has been defined.

Pseudostatic RAMs

The advantage of using a static RAM is its simple interface circuit and its static nature, which means it doesn't have to be periodically refreshed to retain data. Alternatively, a dynamic RAM provides greater density and a lower cost per bit. One approach that tries to provide the best attributes of both devices is the *pseudostatic RAM*, a chip that uses dynamic storage cells but contains all refresh logic on-chip so that it is able to function similarly to a static RAM. NEC's μPD428128 is a 128K x 8-bit pseudostatic RAM that offers a system designer a byte-wide RAM with the density and simple interface of a 1M DRAM (figure 17).

Figure 16. Timing of 4 Meg DRAM Internal Test Circuit



Notes:

[1] $\overline{RAS}$-only refresh or $\overline{CAS}$ before $\overline{RAS}$ refresh may be executed to transistion from a test cycle.

[2] For x 1 parts D_{OUT} is high if all 8 bits are equal, and low if all 8 bits are not equal.

[3] For x 4 parts, all I/O pins are enabled and D_{OUT} is high if all 2 bits are equal, and low if all 2 bits are not equal.

[4] Address compression control bits are defined below.

Data Bus Width (bits)	Control Address Bits (Don't care address)
8	A10R, A10C, A0C (for x 1 bit)
2	A0C (for x 4 bit)

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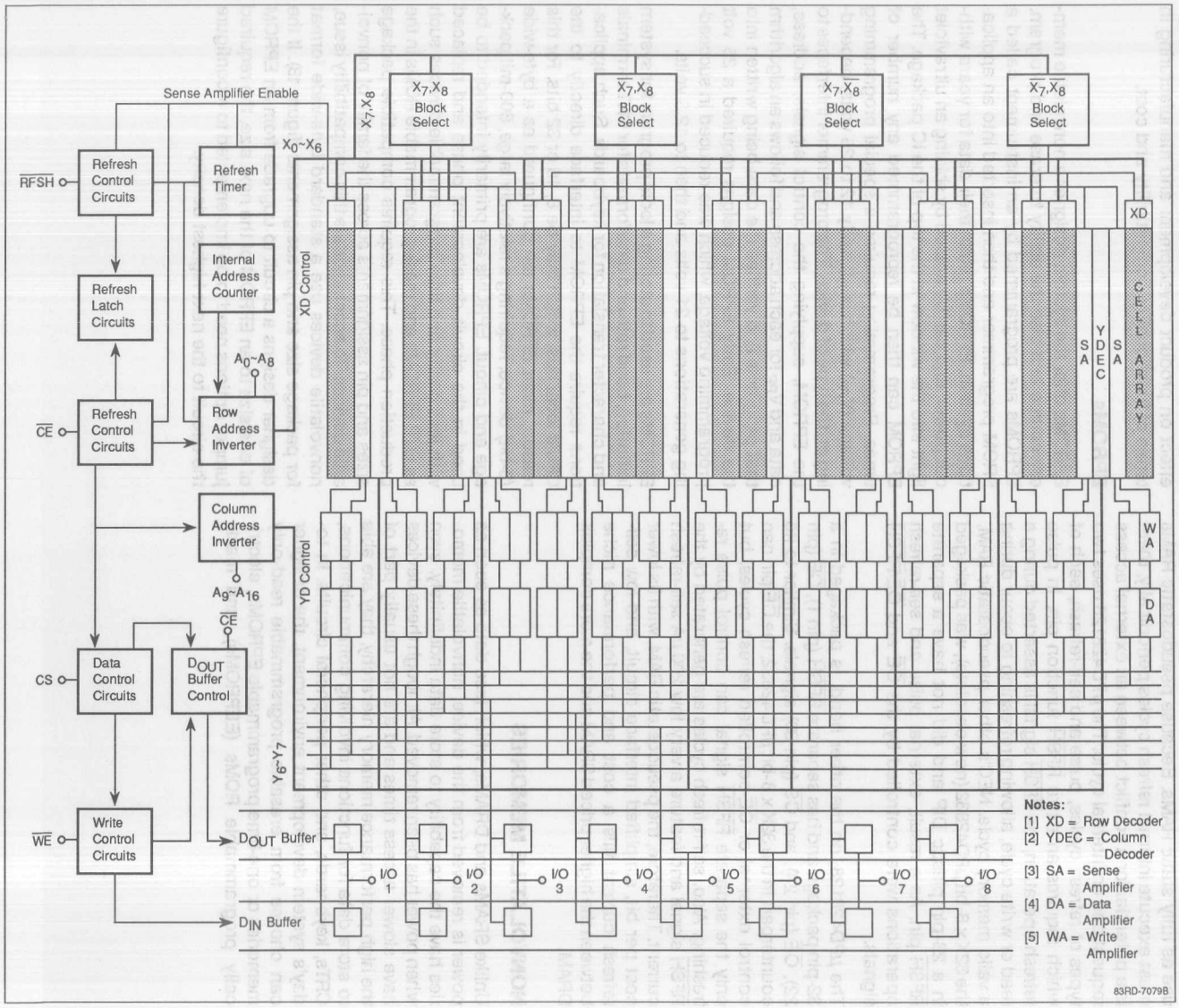


Figure 17. Block Diagram of Pseudostatic RAM

Pseudostatic RAM are nearly, but not quite, as easy to use as fully static RAMs. Because pseudostatic RAMs must execute internal refresh cycles periodically, there is a potential for a conflict between an external access request and an internal cycle. The μPD428128 uses two types of refresh cycles, pulse and self-refresh, each of which requires an extra $\overline{RFSH}$ function pin. In pulse refresh operation, the $\overline{RFSH}$ signal is asserted during a read or write cycle, allowing refreshing to occur during a valid memory cycle. NEC's other pseudostatic RAM, the 32K x 8-bit μPD42832 (now obsolete), was packaged in a 28-pin plastic DIP and did not have a separate $\overline{RFSH}$ pin. As a result, external pulse and self-refresh operations were controlled by the $\overline{CE}$ and $\overline{OE}$/$\overline{RFSH}$ signals.

The μPD428128, on the other hand, is packaged in a 32-pin package and has separate $\overline{RFSH}$ (pin 1), $\overline{CE}$ (pin 22), $\overline{OE}$ (pin 24), and $\overline{CS}$ (pin 30) signals. Similar to its counterpart in the 32K x 8-bit μPD42832, the $\overline{CE}$ pin can control external or $\overline{CE}$-controlled refresh cycles, but only the separate $\overline{RFSH}$ signal can control pulse refreshing. Also, self-refresh cycles are generated by the $\overline{RFSH}$ signal and feature a very low 200 μA self-refresh current. Therefore, the pseudostatic RAM, with its lower cost per bit, simplified interface circuit, and low self-refresh current fills a cost and performance niche between the higher priced SRAM and the more complex DRAM.

NONVOLATILE MEMORIES

Unlike SRAMs and DRAMs, which lose data as soon as power is removed from the device, nonvolatile memories have the capability to store data indefinitely, even when power has been removed. Although these devices have slower access times and are not usually part of the high performance memory hierarchy, they are able to store data for functions involving communications, CRTs, keyboards, and other peripheral circuits. In today's system development environment, the designer can choose from erasable programmable read-only memories or one-time programmable EPROMs, electrically programmable ROMs (EEPROMs), and mask-programmable ROMs, each of which has a different effect on product development and manufacturing in terms of functionality, compatibility and cost.

EPROMs

EPROMs offer the system designer a nonvolatile memory source and also the ability to erase and program. EPROMs are programmed by an instrument called a PROM programmer and then inserted into an applications system. EPROMs retain their data for years without power, and can be erased by shining an ultraviolet light into the window in the top of the IC package. The EPROM can then be reprogrammed any number of times. Programming requires a special programming voltage (V_{PP}) which is typically 12 to 25 volts, depending on the type of device. The programmer interfaces to the EPROM, supplying the control signals, address, data and V_{PP} for each address and follows an algorithm that programs and verifies the data being written into the device. Early EPROM designs required a 25 volt programming voltage, which was reduced in succeeding generations to 21 volts and then to 12.5 volts.

EPROMs are used to storing a local program for system initiation, baud rate and data formats for CRT terminals and character translation for keyboards. Such applications require the EPROM to interface directly to the CPU's local bus, which may be 8, 16 or 32 bits. For this reason, most EPROMs are configured as a byte-wide (8-bit) device, requiring a relatively large, 600-mil package and pinout. EPROMs are primarily intended to be used in the circuit development phase and replaced with less costly one-time programmable devices such as OTP EPROMs and mask-programmable ROMs in the production phase. This requires compatible package sizes and pin assignments across the family of nonvolatile devices. To accommodate this compatibility issue, nonvolatile devices use a standard byte-wide format for package size and pin assignments (figure 18). If the designer designs a circuit to upgrade from an EPROM of one size to an EPROM of the next size, the required jumper options need to be implemented to reconfigure the circuit to the next highest density.

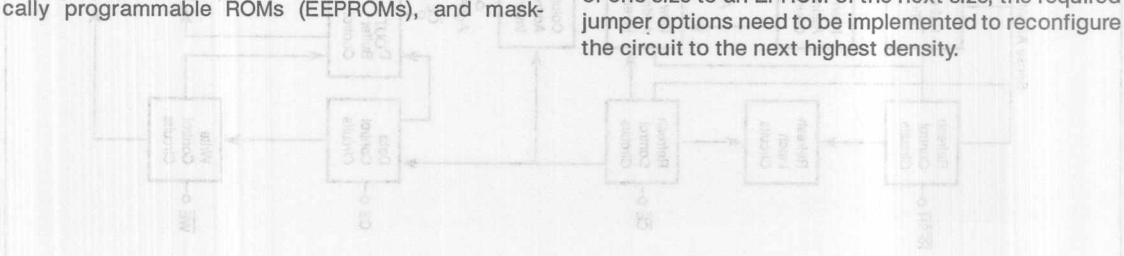
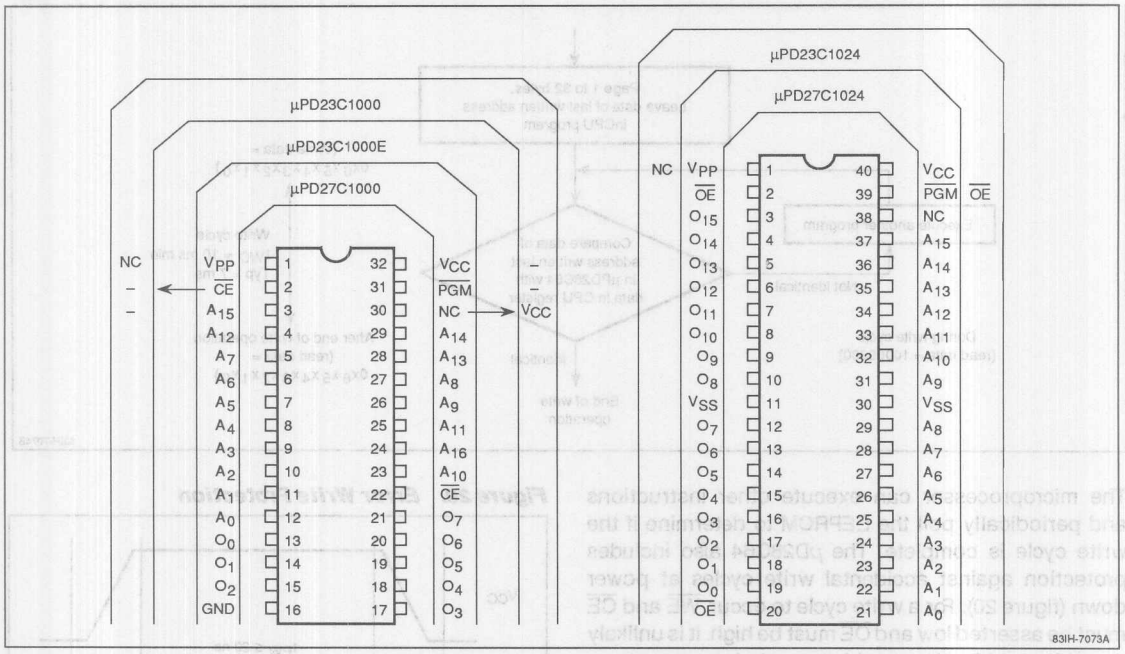


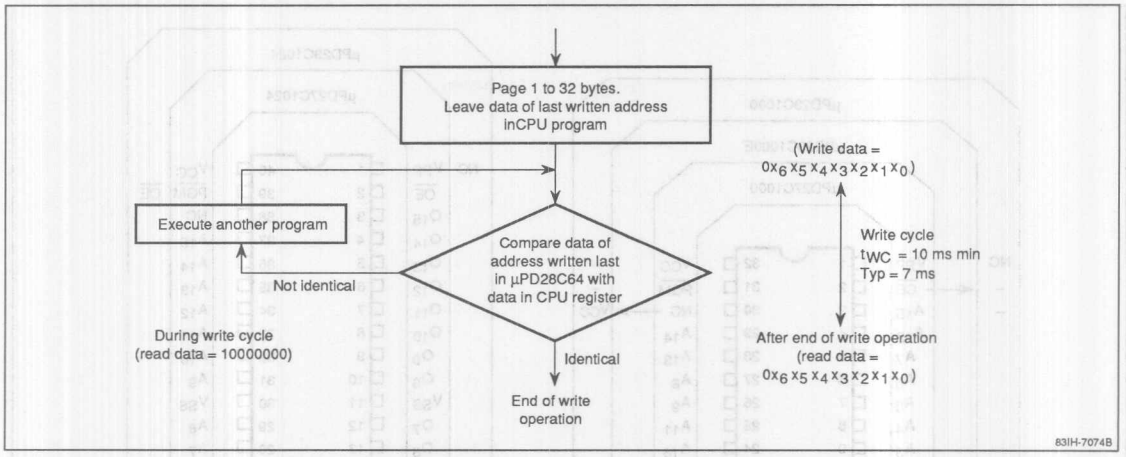
Figure 18. EPROM/ROM Pinout Compatibility



EEPROMs

One disadvantage of the EPROM is that it cannot be programmed while it is in a circuit. The EEPROM solves that problem by providing a write function that can be used while the EEPROM is still in the circuit. The microprocessor can write to the EEPROM just as if it were a RAM and continue with other operations during the long write cycle time. NEC's 8K x 8-bit μPD28C64 EEPROM includes a feature called $\overline{\text{DATA}}$ polling to indicate when a write cycle is complete (figure 19). If the EEPROM is read while an internal write cycle is in progress, the EEPROM returns the complement of the last data written. Thus, the system software can determine when the write cycle is complete by reading the location last written and comparing it to the data being written. The EEPROM can accomplish this because it includes on-chip latches and an automatic "erase before write" function.

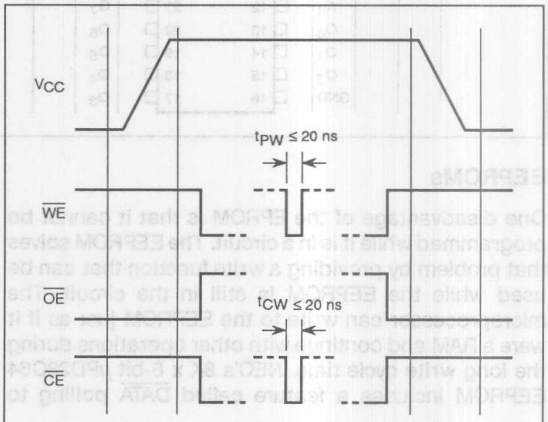
Figure 19. DATA Polling Flow Chart



The microprocessor can execute other instructions and periodically poll the EEPROM to determine if the write cycle is complete. The μD28C64 also includes protection against accidental write cycles at power down (figure 20). For a write cycle to occur, $\overline{WE}$ and $\overline{CE}$ must be asserted low and $\overline{OE}$ must be high. It is unlikely that this combination would occur during power transitions. Additional write protection is provided by a noise immunity filter that inhibits write operation when the $\overline{WE}$ pulse is 20 ns or less, and when the power supply voltage level is detected to be 2.5 volts or less.

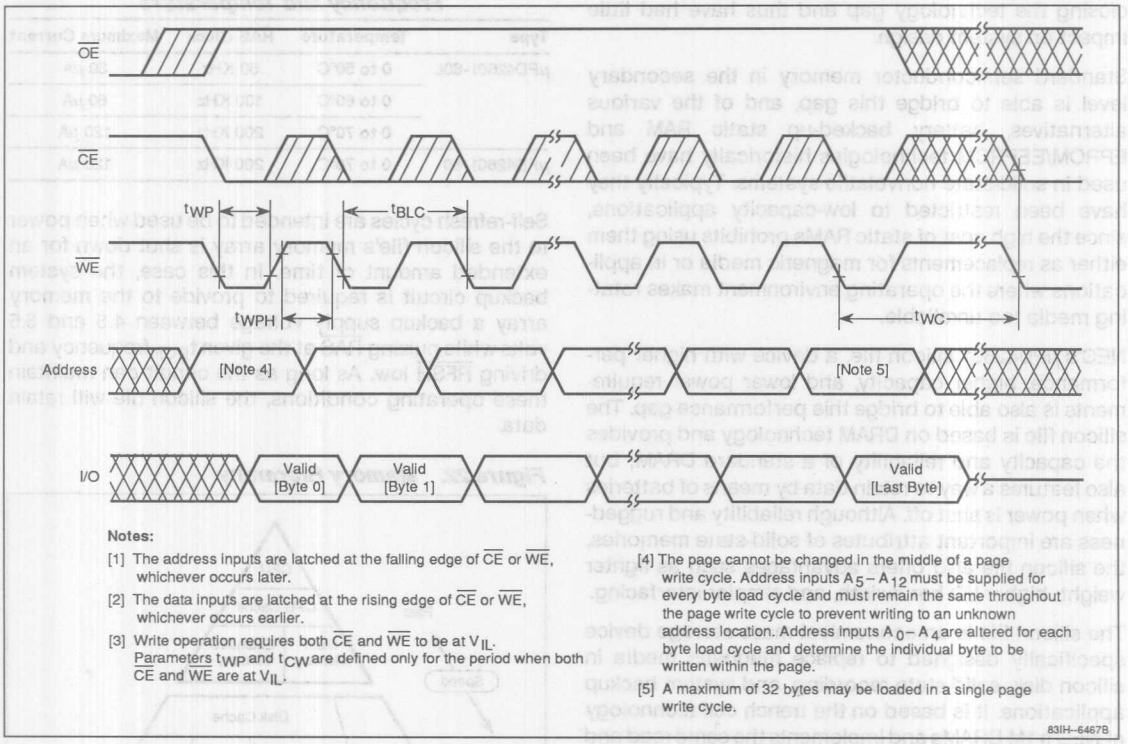
The μPD28C64 optimizes the write cycle with a feature that speeds effective access time when writing a series of 32 bytes simultaneously (figure 20). The 8K x 8-bit device is compatible with the byte-wide pin assignment standard and is pin-compatible with the 8K x 8-bit EPROM and SRAM. While the 8K x 8-bit device is targeted at the larger capacity EEPROM applications, several small devices provide a low-cost solution for low-end systems. The μPD28C04 is such a device and is orgnanized as 256 x 8 bits and provides the same write and protection features as the μPD28C64.

Figure 20. Error Write Protection



Control Terminal			
$\overline{CE}$	$\overline{OE}$	$\overline{WE}$	
V_{IH} or V_{IL}	V_{IH} or V_{IL}	V_{IH}	$\overline{WE}$ Write Inhibit
V_{IH} or V_{IL}	V_{IH} or V_{IL}	≤ 20 ns	
V_{IH} or V_{IL}	V_{IL}	V_{IH} or V_{IL}	$\overline{OE}$ Write Inhibit
V_{IH}	V_{IH} or V_{IL}	V_{IH} or V_{IL}	$\overline{CE}$ Write Inhibit
≤ 20 ns	V_{IH} or V_{IL}	V_{IH} or V_{IL}	

Figure 21. μPD28C64 Page Write Cycle



Notes:

[1] The address inputs are latched at the falling edge of $\overline{CE}$ or $\overline{WE}$, whichever occurs later.

[2] The data inputs are latched at the rising edge of $\overline{CE}$ or $\overline{WE}$, whichever occurs earlier.

[3] Write operation requires both $\overline{CE}$ and $\overline{WE}$ to be at V_{IL}. Parameters t_{WP} and t_{CW} are defined only for the period when both $\overline{CE}$ and $\overline{WE}$ are at V_{IL}.

[4] The page cannot be changed in the middle of a page write cycle. Address inputs $A_5 - A_{12}$ must be supplied for every byte load cycle and must remain the same throughout the page write cycle to prevent writing to an unknown address location. Address inputs $A_0 - A_4$ are altered for each byte load cycle and determine the individual byte to be written within the page.

[5] A maximum of 32 bytes may be loaded in a single page write cycle.

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Mask-Programmable ROMs

The ability to erase an EPROM is an important feature, especially during the product development phase when the EPROM code is frequently changed. When the product enters its manufacturing stage and the program code becomes fixed, the extra cost due to the special package with a transparent lid is difficult to justify. Mask-programmable ROMs, which are programmed during the manufacture of the chip itself, are less expensive. NEC produces mask-programmable ROMs and will also manufacture the custom mask required for the device. There is a charge and lead time required for producing the mask, but for high-volume applications, the mask can be amortized with a cost savings compared to the standard EPROM. Typically, the mask-programmable ROM is compatible with the byte-wide standard used in EPROM devices for feature and package compatibility.

One of the disadvantages of the mask-programmable ROM is that if a bug is found in the code, the mask has to be replaced at a large cost. A one-time programmable (OTP) EPROM fills the gap between the standard EPROM in cost and functionality because this product can be programmed like a standard EPROM, but cannot be erased. Since it doesn't have the special EPROM package with transparent lid, the cost is less than an EPROM but higher than a mask-programmable ROM. The mask charge and lead time is eliminated and the parts can be inventoried in their unprogrammed state and programmed just prior to final assembly. Waste caused by program changes is thus minimized, and only one part type is purchased for any number of different programs.

Silicon File

In the past, there has existed a technology gap between the faster primary and the slower secondary memories (figure 22). Average access time of secondary devices, most often magnetic disks and drums, is 1000 to 10,000 times slower than that of primary devices. Electronic disks such as charge-coupled devices and magnetic

bubble memories have not proved cost-effective in closing the technology gap and thus have had little impact on system design.

Standard semiconductor memory in the secondary level is able to bridge this gap, and of the various alternatives, battery backed-up static RAM and EPROM/EEPROM technologies historically have been used in solid-state nonvolatile systems. Typically they have been restricted to low-capacity applications, since the high cost of static RAMs prohibits using them either as replacements for magnetic media or in applications where the operating environment makes rotating media too unreliable.

NEC's μPD42601 silicon file, a device with higher performance, higher capacity, and lower power requirements is also able to bridge this performance gap. The silicon file is based on DRAM technology and provides the capacity and reliability of a standard DRAM, but also features a way to retain data by means of batteries when power is shut off. Although reliability and ruggedness are important attributes of solid-state memories, the silicon file also offers advantages such as lighter weight, higher I/O bandwidth, and simpler interfacing.

The silicon file is an economical mass storage device specifically designed to replace magnetic media in silicon disk, solid-state recording, and system backup applications. It is based on the trench cell technology of NEC's 1M DRAMs and implements the same read and write cycles (figure 23), but optimizes system bandwidth with a page cycle that repeatedly pulses $\overline{CAS}$ while maintaining $\overline{RAS}$ low (figure 24). The silicon file must also periodically execute standard $\overline{RAS}$-only and $\overline{CAS}$ before $\overline{RAS}$ refresh cycles to refresh its cells within a specified interval of 32 ms, which is four times slower than a 1M DRAM.

An important feature of the silicon file is its ability to retain data while being powered by a backup battery. This is accomplished by means of a self-refresh cycle that can be used in applications requiring a low data retention or self-refresh current. The $\overline{RFSH}$ control signal goes low while the $\overline{RAS}$ signal is clocked at a relatively slow rate (t_{RCF}). Since data loss is caused by leakage, and leakage current is a function of temperature, t_{RCF} is specified at three temperature ratings: 50° C, 60°C, and 70°C. Each rating has a corresponding refresh current (directly proportional to the refresh rate) which is required to maintain data (table 2).

Table 2. Self-Refresh Current Versus Clock Frequency and Temperature

Type	Temperature	$\overline{RAS}$ Clock	Maximum Current
μPD42601-60L	0 to 50°C	50 KHz	30 μA
	0 to 60°C	100 KHz	60 μA
	0 to 70°C	200 KHz	120 μA
μPD42601-60	0 to 70°C	200 KHz	120 μA

Self-refresh cycles are intended to be used when power to the silicon file's memory array is shut down for an extended amount of time. In this case, the system backup circuit is required to provide to the memory array a backup supply voltage between 4.5 and 5.5 volts while pulsing $\overline{RAS}$ at the given t_{RCF} frequency and driving $\overline{RFSH}$ low. As long as the circuit can maintain these operating conditions, the silicon file will retain data.

Figure 22. Memory Hierarchy

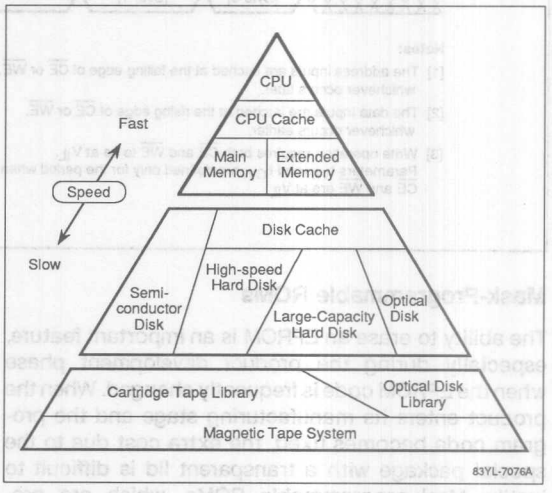


Figure 23. Silicon File Read Cycle

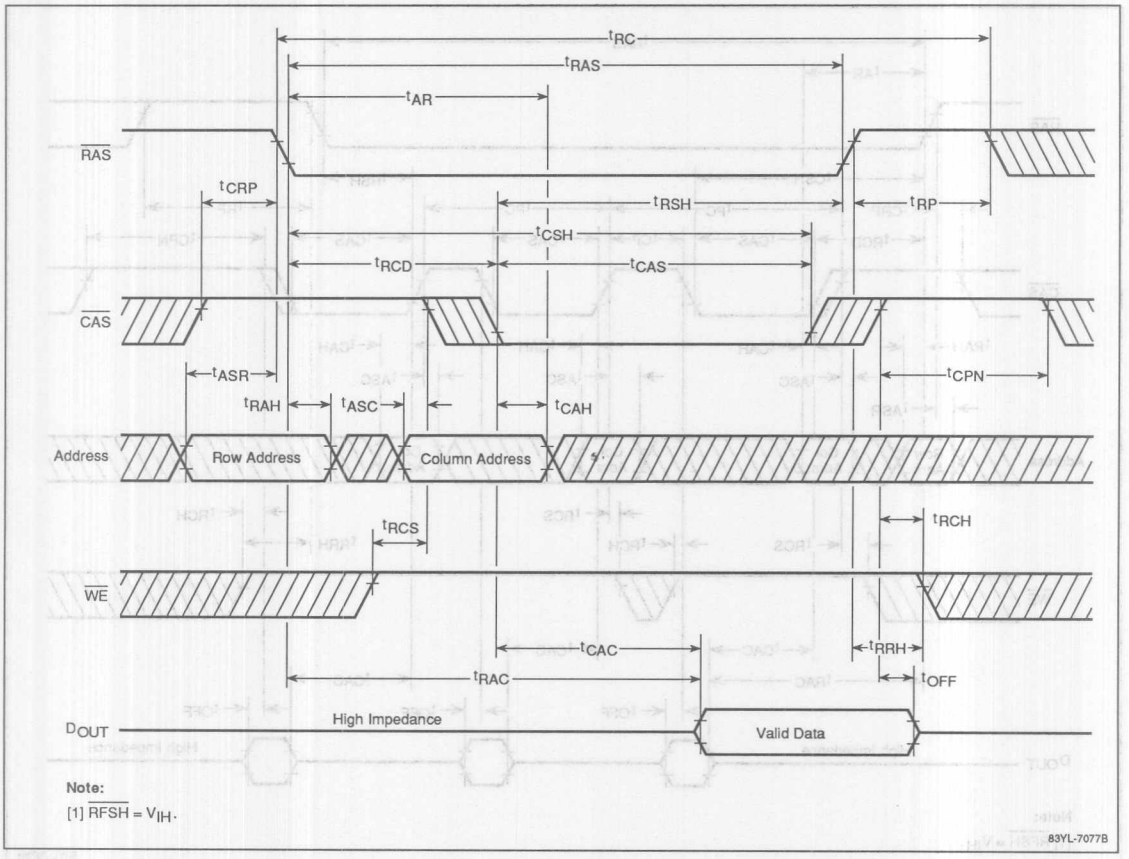
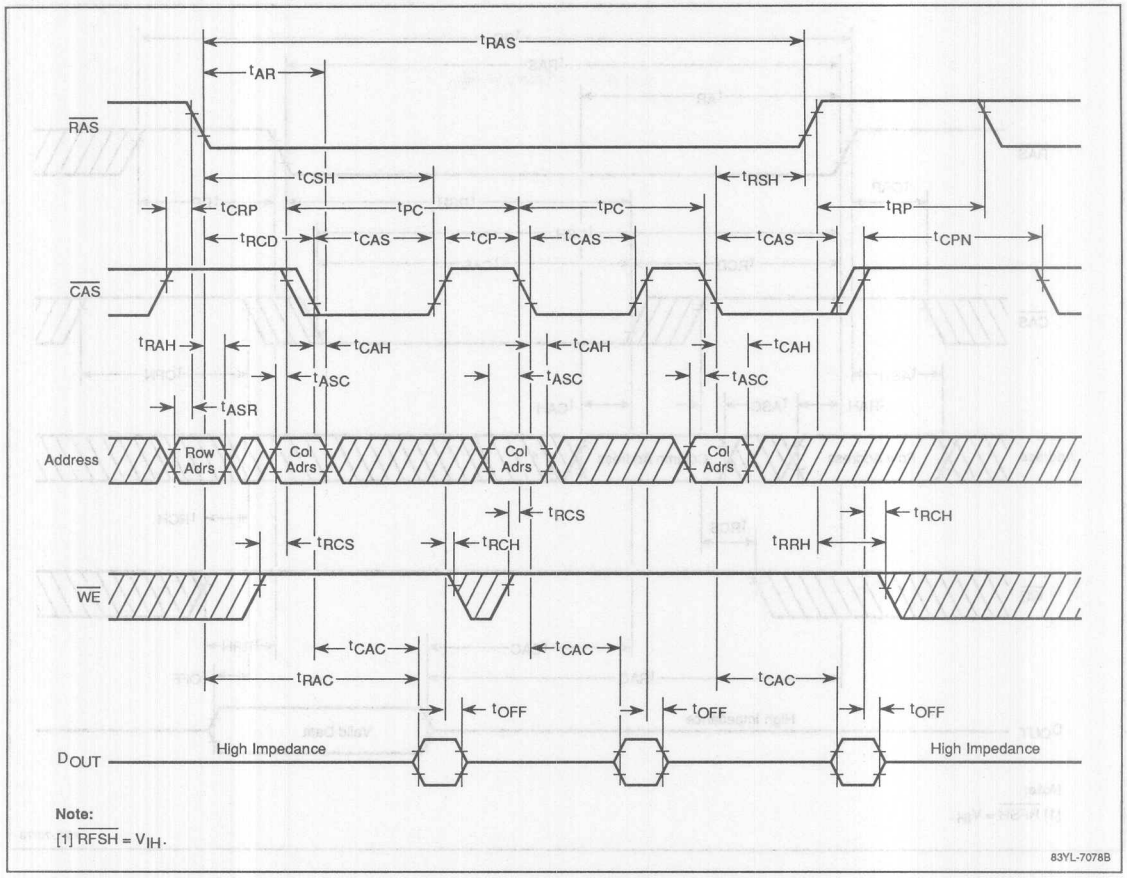


Figure 24. Silicon File Page Read Cycle



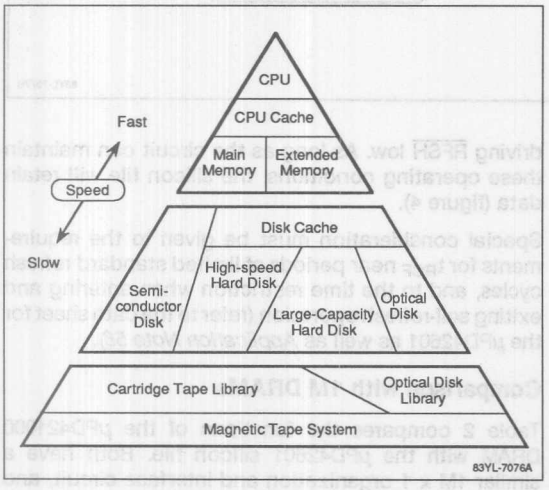
Silicon File System Architecture
Application Note 90-06

Introduction

The objective in designing a hierarchical memory system is to match the processor's speed either with the rate of information transfer or with the bandwidth of the memory at the lowest level, at a reasonable cost. No one type of device meets all criteria, i.e., inexpensive, reliable, fast and nonvolatile. In fact, the hierarchy in most computers is often organized so that the highest level has the fastest speed and the lowest level has the lowest speed, e.g., a cache typically resides in the highest level and contains the fastest and most expensive memory, the next level contains random access devices that are 5 to 10 times slower than the cache, and the lowest level has the slowest and cheapest devices.

In the past, there has existed a technology gap between the faster primary and the slower secondary memories (figure 1). Average access time of secondary devices, most often magnetic disks and drums, is 1000 to 10,000 times slower than that of primary devices. Electronic disks such as charge-coupled devices and magnetic bubble memories have not proved cost-effective in closing the gap and thus have had little impact on system design.

Figure 1. Memory Hierarchy



Standard semiconductor memory in the secondary level is able to bridge this gap, and of the various alternatives, battery backed-up static RAM and EPROM/EEPROM technologies historically have been used in solid-state nonvolatile systems. Typically they have been restricted to low-capacity applications, since the high cost of static RAMs prohibits using them in place of magnetic media or in applications where the operating environment makes rotating media unreliable.

NEC's μPD42601 silicon file, a device with higher performance, higher capacity, and lower power requirements is also able to bridge this performance gap. Based on DRAM technology, the μPD42601 provides the capacity and reliability of a standard DRAM, but also features a way to retain data by means of batteries when power is shut off. It also offers the reliability and ruggedness of solid-state memories, as well as lighter weight, higher I/O bandwidth, and simpler interfacing.

Functional Overview

Standard Operation. The silicon file is specifically designed to replace magnetic media in silicon disk, solid-state recording, and system backup applications. It is based on the trench cell technology of NEC's 1M DRAMs and implements the same read and write cycles (figure 2), but optimizes system bandwidth with a page cycle that repeatedly pulses $\overline{CAS}$ while maintaining $\overline{RAS}$ low (figure 3). The silicon file also periodically executes standard $\overline{RAS}$-only and $\overline{CAS}$ before $\overline{RAS}$ refresh cycles to refresh its cells within a specified interval of 32 ms, which is four times slower than a 1M DRAM.

Low-Power Operation. An important feature of the silicon file is its ability to retain data while being powered by a backup battery. This is accomplished by means of a self-refresh cycle that can be used in applications requiring a low data retention or self-refresh current. The $\overline{RFSH}$ control signal goes low while the $\overline{RAS}$ signal is clocked at a relatively slow rate (t_{RCF}). Since data loss is caused by leakage, and leakage current is a function of temperature, t_{RCF} is specified at three temperature ratings: 50°C, 60°C, and 70°C. Each rating has a corresponding refresh current (directly proportional to the refresh rate) which is required to maintain data (table 1).

Figure 2. Read Cycle

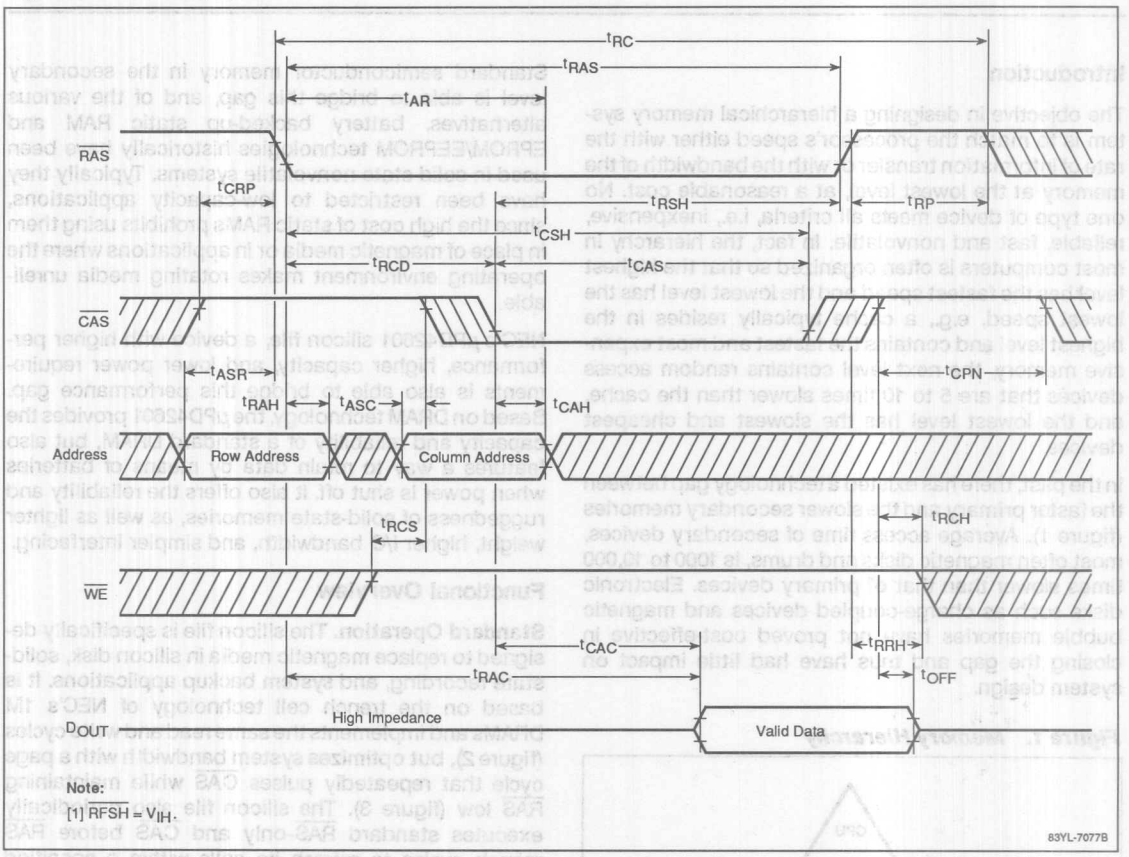


Table 1. Self-Refresh Current Versus Clock Frequency and Temperature

Type	Temperature	RAS Clock	Maximum Current
μPD42601-60L	0 to 50°C	50 KHz	30 μA
	0 to 60°C	100 KHz	60 μA
	0 to 70°C	200 KHz	120 μA
μPD42601-60	0 to 70°C	200 KHz	120 μA

Self-refresh cycles are intended to be used when power to the silicon file's memory array is shut down for an extended amount of time. In this case, the system backup circuit is required to provide to the memory array a backup supply voltage of between 4.5 and 5.5 volts while pulsing RAS at the given t_{RCF} frequency and driving RFSH low. As long as the circuit can maintain these operating conditions, the silicon file will retain data (figure 4).

Special consideration must be given to the requirements for t_{RCF} near periods of limited standard refresh cycles, and to the time restriction when entering and exiting self-refresh operation (refer to the data sheet for the μPD42601 as well as *Application Note 56*).

Comparison with 1M DRAMs

Table 2 compares the functions of the μPD421000 DRAM with the μPD42601 silicon file. Both have a similar 1M x 1 organization and interface circuit, and both are available in the same high-density 26/20-pin plastic SOJ and 20-pin plastic ZIP packages.

Figure 3. Page Read Cycle

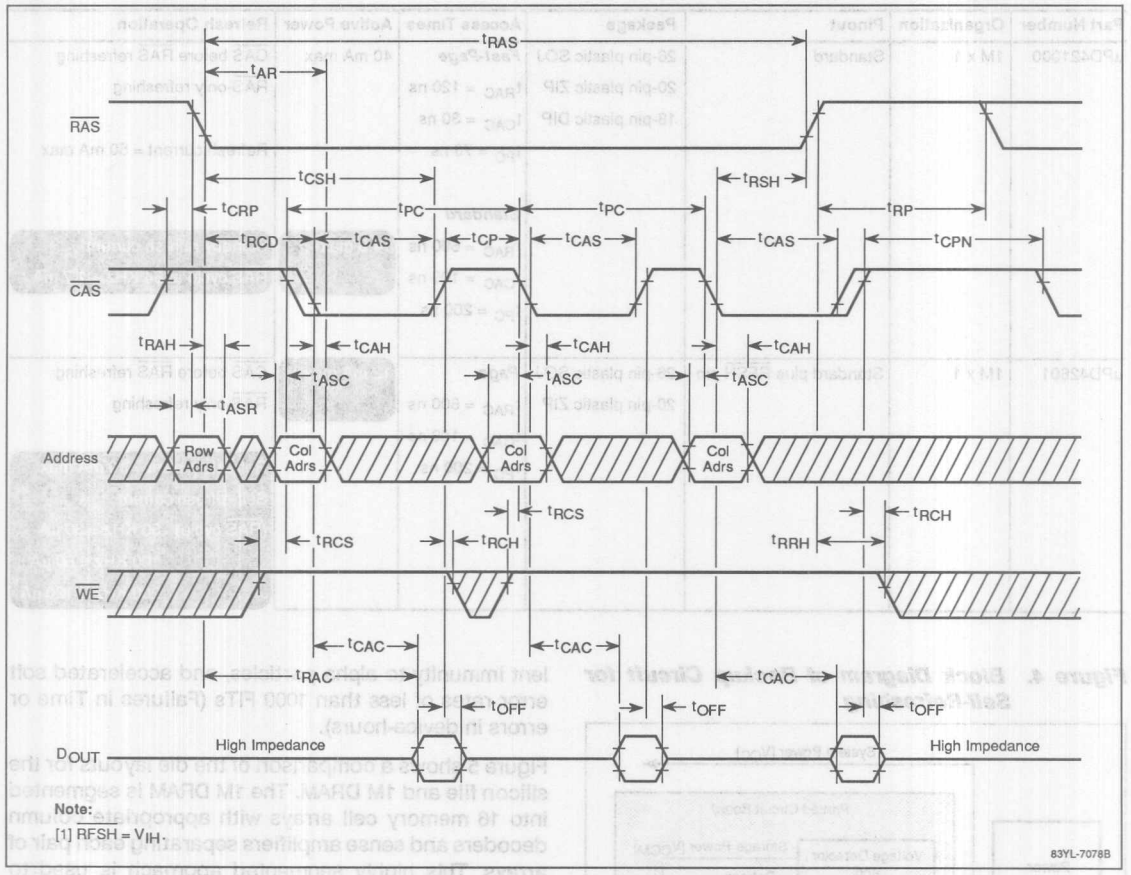
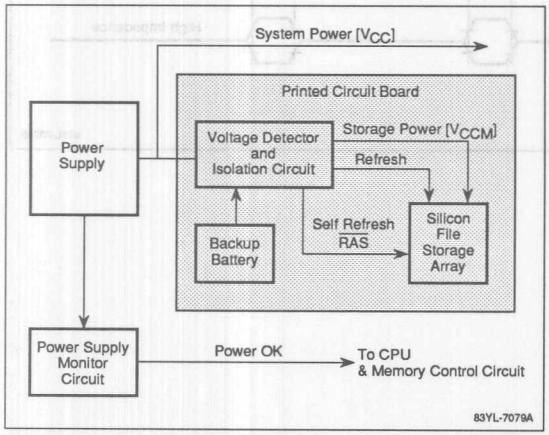


Table 2. Comparison of Silicon File to Standard DRAM

Part Number	Organization	Pinout	Package	Access Times	Active Power	Refresh Operation
μPD421000	1M x 1	Standard	26-pin plastic SOJ 20-pin plastic ZIP 18-pin plastic DIP	***Fast-Page*** t_{RAC} = 120 ns t_{CAC} = 30 ns t_{PC} = 70 ns	40 mA max	$\overline{CAS}$ before $\overline{RAS}$ refreshing $\overline{RAS}$-only refreshing Refresh current = 50 mA max
				Standard t_{RAC} = 600 ns t_{CAC} = 100 ns t_{PC} = 200 ns	14.8 max	Standby refresh current $\overline{RAS}$ cycle at 64 KHz = 1.7 mA
μPD42601	1M x 1	Standard plus $\overline{RFSH}$ pin	26-pin plastic SOJ 20-pin plastic ZIP	***Page*** t_{RAC} = 600 ns t_{CAC} = 100 ns t_{PC} = 200 ns	12 mA max	$\overline{CAS}$ before $\overline{RAS}$ refreshing $\overline{RAS}$-only refreshing Refresh current = 10 mA max Self-refresh current ($\overline{RAS}$ cycle) 50 KHz = 30 μA 100 KHz = 60 μA 200 KHz = 120 μA

Figure 4. Block Diagram of Backup Circuit for Self-Refreshing



Access Time and Power Comparison

The 1M DRAM is designed for high performance at low cost. Its optimized technology, also used in the silicon file and based on NEC's CMOS process and trench memory cell, is proven to provide high reliability, excellent immunity to alpha particles, and accelerated soft error rates of less than 1000 FITs (Failures in Time or errors in device-hours).

Figure 5 shows a comparison of the die layouts for the silicon file and 1M DRAM. The 1M DRAM is segmented into 16 memory cell arrays with appropriate column decoders and sense amplifiers separating each pair of arrays. This highly segmented approach is used to reduce the length of the bit line, which in turn reduces bit line capacitance and results in a faster access time.

Conversely, the eight memory cell segments and eight sense amplifiers in the simplified layout of the silicon file optimize power consumption rather than access time. The silicon file has a slower access time and lower active current, and although active current can be reduced in any DRAM if cycle time is also reduced, active current in the silicon file is still much lower than active current in a DRAM when both are operating at a 1 μs cycle rate.

When a standard DRAM and the silicon file are not being accessed by the system, they operate in standby and dissipate a current much lower than their active current. Standby is used by both devices to reduce system power requirements during normal system operation. The silicon file also has a unique self-refresh

cycle that isn't implemented on a standard DRAM and can operate at very low currents, as low as 30 μA, and still retain data via a battery powered backup system. Furthermore, the silicon file uses an additional $\overline{RFSH}$ pin (pin 4 on the 20/26-pin SOJ and pin 9 on the 20-pin plastic ZIP).

System Design

When considering a system design using the silicon file, the system designer will recognize a number of similarities with the 1M DRAM. Both devices use the same x1 organization, as well as $\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$ and A_0 through A_9, and both are available in the same SOJ and ZIP package types. Typically, a silicon file system design will be functionally similar to a standard DRAM system, making it very easy for the designer to use traditional DRAM system design techniques.

Figure 6 shows an interface between the silicon file and a host interface. It is very similar to a DRAM system, except for the power monitor and backup circuit used to implement self-refreshing. The interface circuit is application-dependent, and can be an interface to a variety of standard I/O or memory interfaces.

3

Figure 5. Die Comparison of 1M DRAM and Silicon File

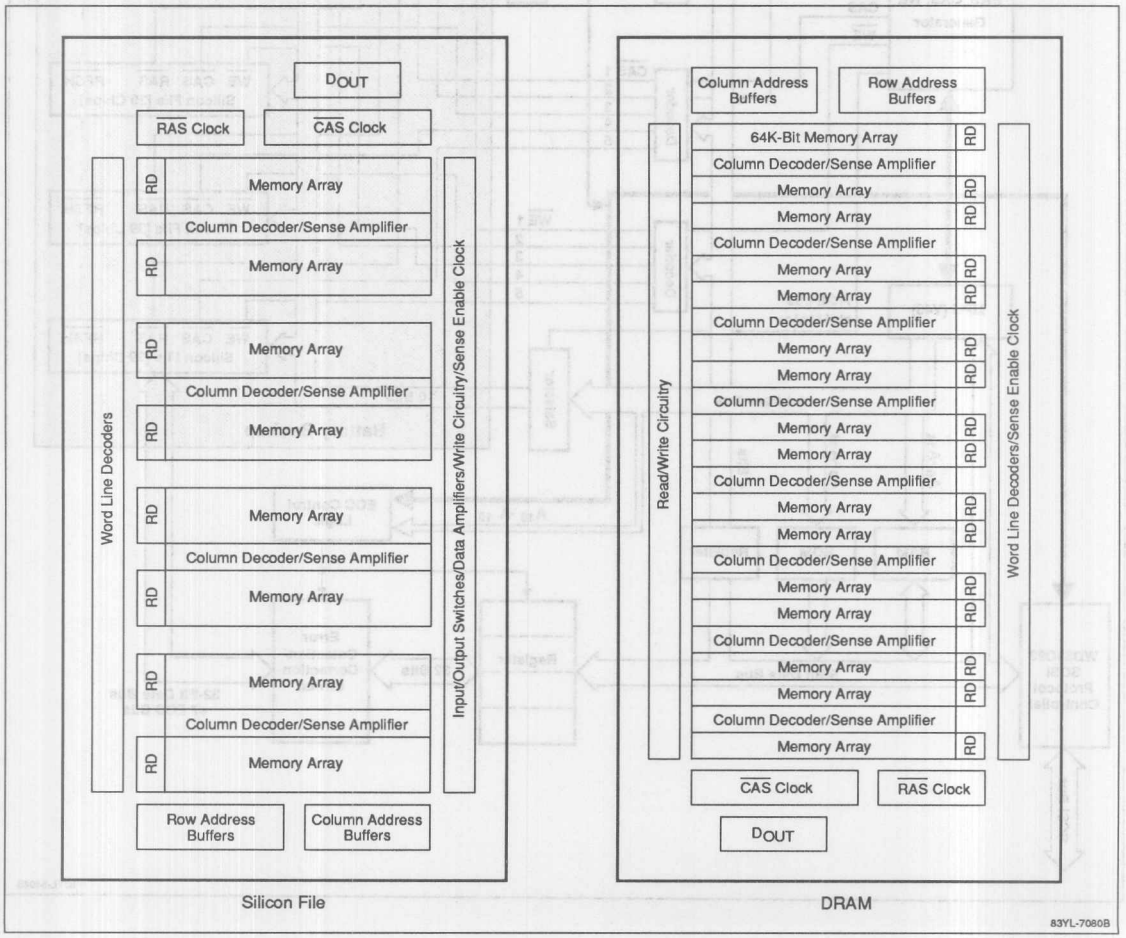
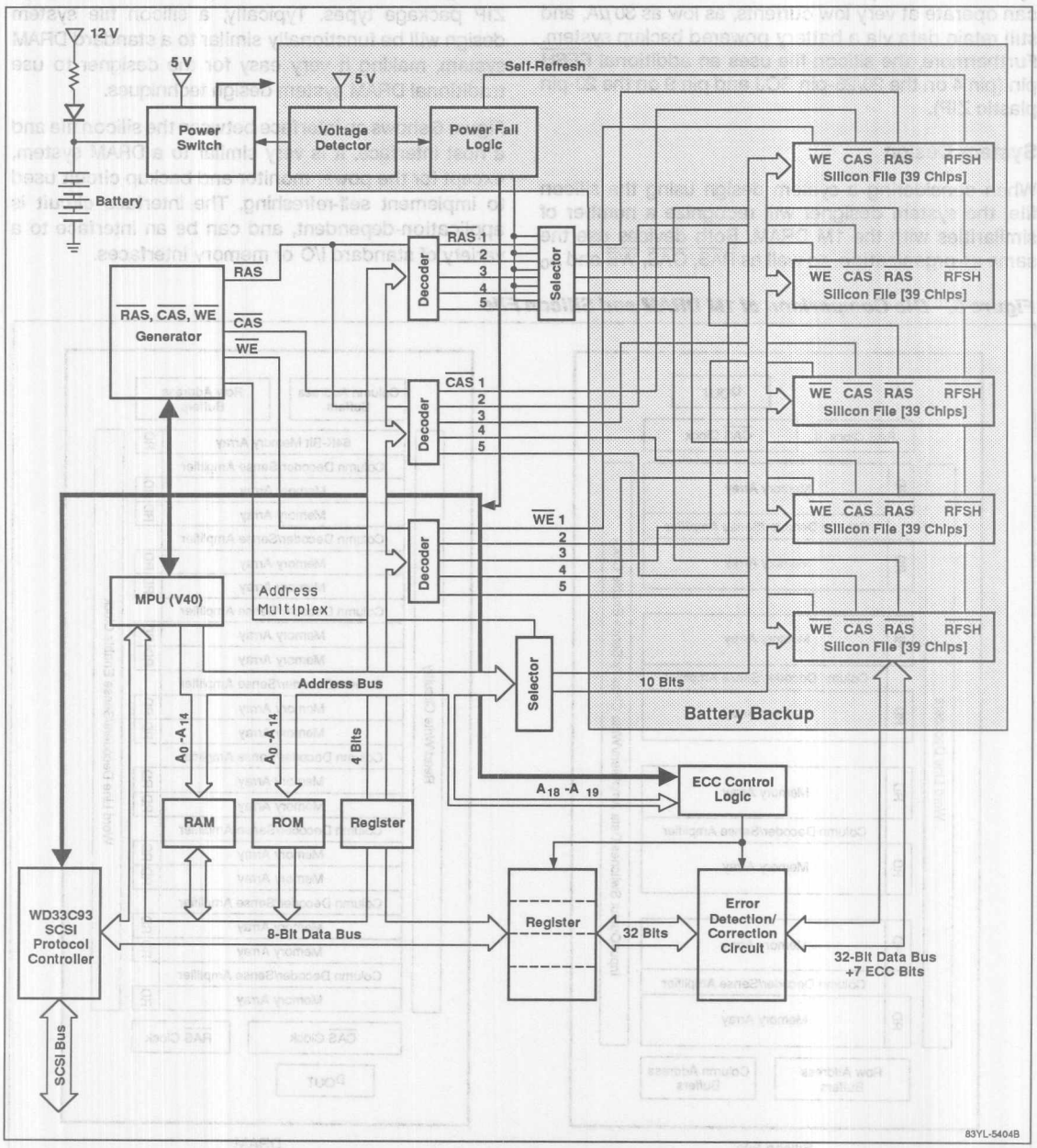


Figure 6. Block Diagram of 20 Mbyte Solid-State Disk System



The control circuit supervises interaction between the host interface and the storage array of the silicon file, translating signals from the host interface into silicon file access cycles and controlling the transfer of data on the host interface bus. The power monitor and backup circuit track power supply voltage for power failures or shutdowns, and maintain memory data by generating control signals for self-refresh cycles and battery backup voltage. To increase system reliability, an error correction and detection circuit, such as a parity bit or ERCC, may be implemented. One common design characteristic is that the silicon file control and memory array circuits will remain application-independent, while the system interface circuit will be application-dependent.

Control Circuitry

This section focuses on the circuitry of a silicon file system, and in particular on the application-independent control circuits and various system interfaces.

The similarity between the silicon file and a 1M DRAM extends to the organization of their memory cells in a matrix of rows and columns, with each individual cell accessed by first addressing a row and then a column (figure 7). The external address is presented to the silicon file in two parts, as shown in the waveform in figure 2. The row address first is driven on the address input pins and $\overline{RAS}$ goes low to clock the row address into an internal row address latch. The row address must be stable for the specified setup time of t_{ASR} before $\overline{RAS}$ is asserted, and also for the specified hold time of t_{RAH} after $\overline{RAS}$ is asserted.

The address inputs are then changed to column addresses and $\overline{CAS}$ is asserted. $\overline{CAS}$ also serves as the output enable signal, in that the three-state driver is enabled whenever $\overline{CAS}$ is asserted. The time when $\overline{CAS}$ can be asserted is determined by the minimum requirements for a $\overline{RAS}$ to $\overline{CAS}$ delay, as specified by t_{RCD}. Additionally, setup and hold times for $\overline{CAS}$ must be met. Presenting the address in two parts has the advantage of reducing by 50% the number of address pins and the package size. The silicon file is typically used in large memory systems where chip size is an important consideration.

Data is available after the access times from both $\overline{RAS}$ (t_{RAC}) and $\overline{CAS}$ (t_{CAC}) have been satisfied. The limit of performance is determined by the access time from $\overline{RAS}$. If the assertion of $\overline{CAS}$ is delayed longer than required, then maximum performance will not be obtained and access time from $\overline{CAS}$ will determine the overall access time.

Another specification of importance is the t_{RP} precharge time for $\overline{RAS}$, which is required for the memory circuit to recover from the previous access. Because a read cycle destroys the data in an addressed memory cell, a precharge cycle must be executed to restore the data and equalize signal levels on the bit lines. Thus, the cycle time for a silicon file is greater than the access time. The difference between access time and cycle time is equal to the precharge time, e.g., a silicon file with an access time of 600 ns will have a cycle time of 1 μs.

Figure 8 shows the timing for an early write cycle. The addressing sequence is the same; the only difference is that $\overline{WE}$ is asserted, and data is supplied by the CPU on the D_{IN} pin. There are two types of write cycles, depending upon the timing relationship between $\overline{WE}$ and $\overline{CAS}$. Figure 8 shows the $\overline{WE}$ signal being asserted before $\overline{CAS}$. In this case, setup and hold times are referenced to the falling edge of $\overline{CAS}$. In a late write cycle, $\overline{WE}$ is asserted after $\overline{CAS}$.

Figure 7. Silicon File Block Diagram

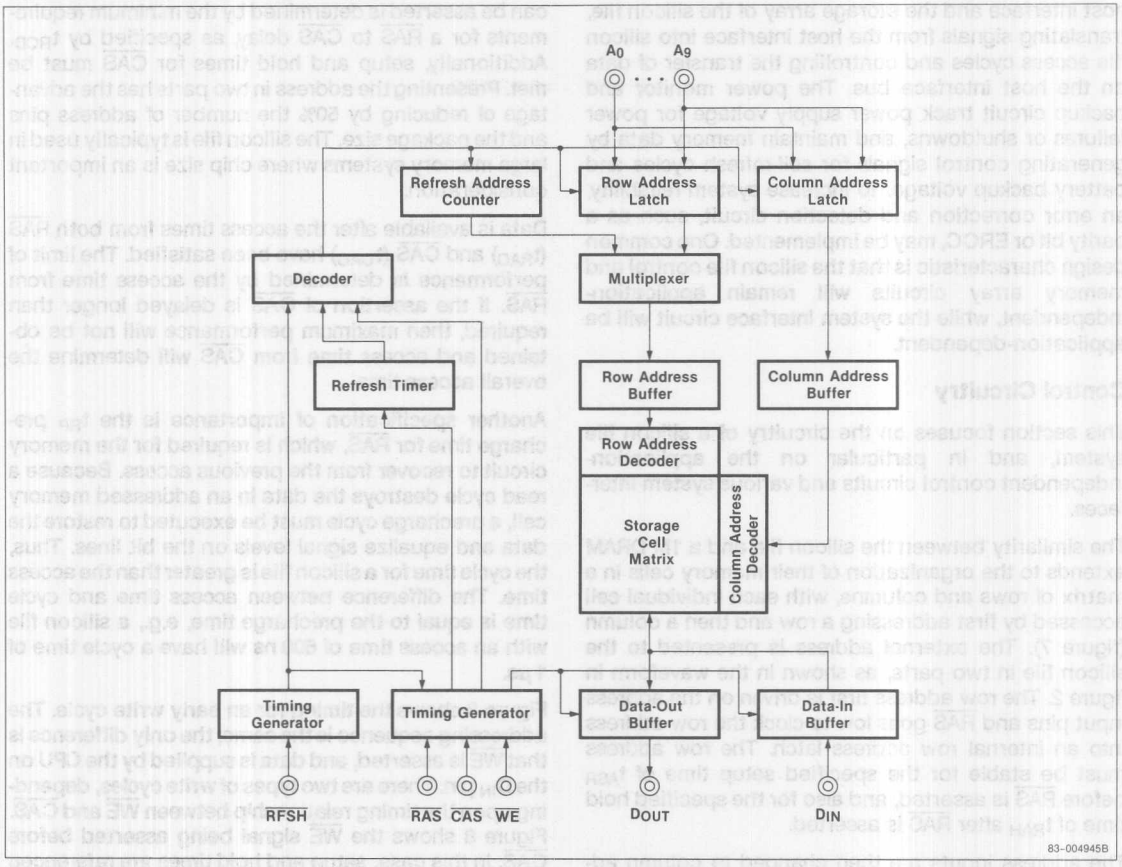
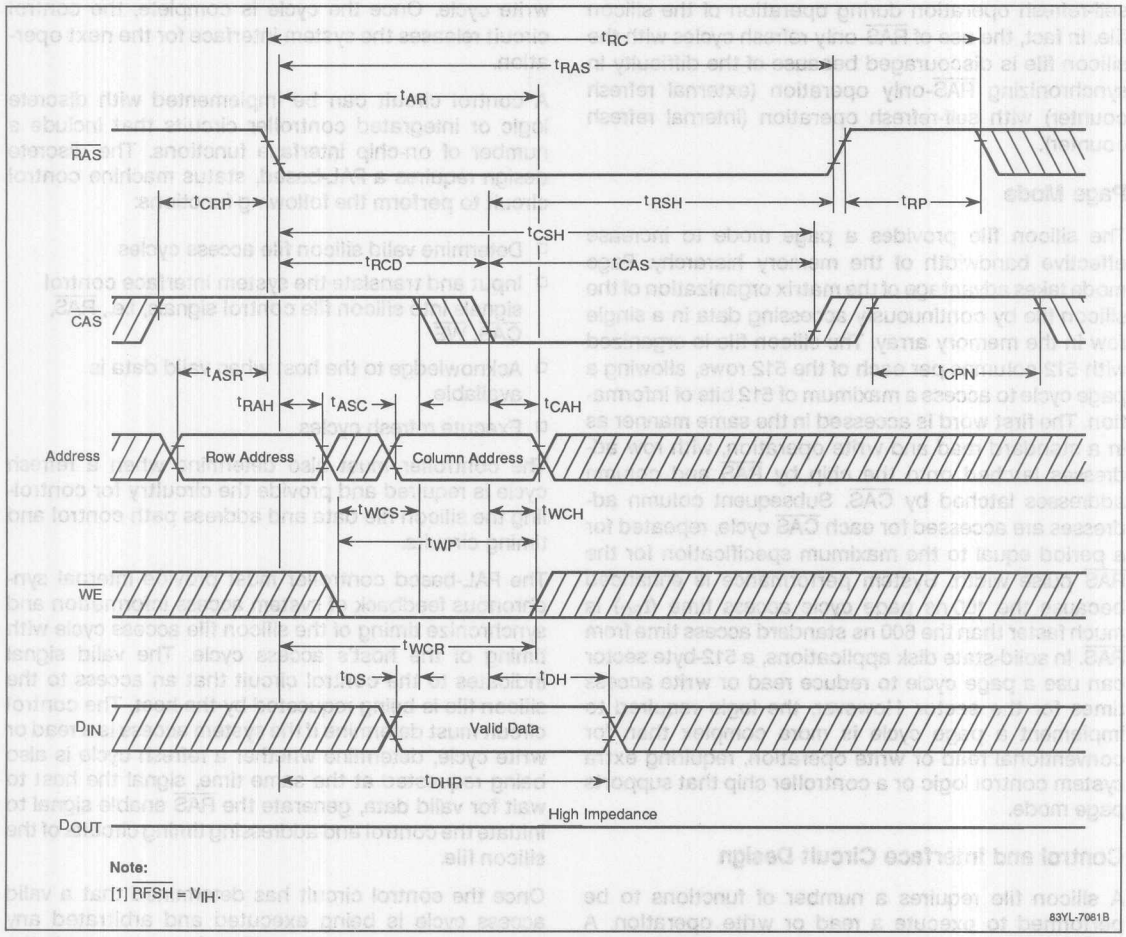


Figure 8. Early Write Cycle



Refreshing of Dynamic Cells

The silicon file, as well as all DRAMs, uses a memory cell structure that stores a dynamic charge on a capacitor, which means that the charge can decrease in time because of leakage. As a result, all devices using DRAM cell technology must be periodically restored or refreshed. Whenever a row is selected in a silicon file, all the cells in that row are accessed and the charge in that cell refreshed. The maximum interval in which a row address must be refreshed is called the refresh period (t_{REF}) and is specified as 32 ms for the silicon file. If each row address is not accessed every 32 ms, data in that row cannot be guaranteed.

Two refresh cycles can be used to refresh a silicon file. $\overline{RAS}$-only refresh cycles are executed when the refresh address is driven onto the address pins by an external circuit when $\overline{RAS}$ is low. $\overline{CAS}$ is left inactive during this cycle since no data is being read or written.

To simplify the circuitry needed to initiate refresh cycles, the silicon file has an on-chip counter that generates every refresh address and is activated by asserting $\overline{CAS}$ before the $\overline{RAS}$ signal. Internal control logic detects this state and uses the address generated by the internal refresh address counter to execute a $\overline{CAS}$ before $\overline{RAS}$ refresh cycle, which is standard in most DRAMs. Its advantage is that no external counter is required and the refresh address sequence is main-

tained when switching between $\overline{CAS}$ before $\overline{RAS}$ and self-refresh operation during operation of the silicon file. In fact, the use of $\overline{RAS}$-only refresh cycles with the silicon file is discouraged because of the difficulty in synchronizing $\overline{RAS}$-only operation (external refresh counter) with self-refresh operation (internal refresh counter).

Page Mode

The silicon file provides a page mode to increase effective bandwidth of the memory hierarchy. Page mode takes advantage of the matrix organization of the silicon file by continuously accessing data in a single row in the memory array. The silicon file is organized with 512 columns per each of the 512 rows, allowing a page cycle to access a maximum of 512 bits of information. The first word is accessed in the same manner as in a standard read and write operation, with row addresses latched onto the chip by $\overline{RAS}$ and column addresses latched by $\overline{CAS}$. Subsequent column addresses are accessed for each $\overline{CAS}$ cycle, repeated for a period equal to the maximum specification for the $\overline{RAS}$ pulse width. System performance is enhanced because the 100 ns page cycle access time (t_{PC}) is much faster than the 600 ns standard access time from $\overline{RAS}$. In solid-state disk applications, a 512-byte sector can use a page cycle to reduce read or write access times for the sector. However, the logic required to implement a page cycle is more complex than for conventional read or write operation, requiring extra system control logic or a controller chip that supports page mode.

Control and Interface Circuit Design

A silicon file requires a number of functions to be performed to execute a read or write operation. A control circuit must determine that a valid silicon file cycle is being executed and translate the read and write control signals from the host CPU into $\overline{RAS}$, $\overline{CAS}$ and $\overline{WE}$ signals compatible with silicon file timing. The address must be latched and multiplexed into the row and column address, conforming to the timing specifications. Finally, the silicon file must be refreshed periodically to guarantee data retention.

The first task requires the control circuit to monitor the system interface and determine if a valid silicon file cycle is being executed by the host. When a valid access cycle is active, the control circuit must interface with the host through asynchronous or asynchronous acknowledgement signals that determine when silicon file data will be valid on the system bus. The control circuit must also generate control and timing signals to the silicon file memory array that executes a read or write cycle. Once the cycle is complete, the control circuit releases the system interface for the next operation.

A control circuit can be implemented with discrete logic or integrated controller circuits that include a number of on-chip interface functions. The discrete design requires a PAL-based, status machine control circuit to perform the following functions:

- Determine valid silicon file access cycles
- Input and translate the system interface control signals into silicon file control signals, i.e., $\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$
- Acknowledge to the host when valid data is available
- Execute refresh cycles

The controller must also determine when a refresh cycle is required and provide the circuitry for controlling the silicon file data and address path control and timing circuits.

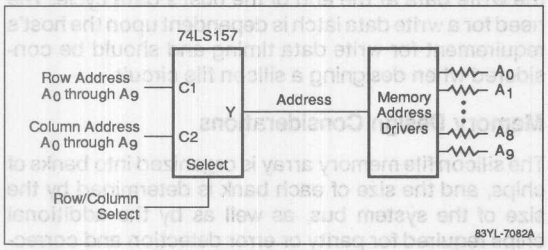
The PAL-based controller must provide internal synchronous feedback of system access information and synchronize timing of the silicon file access cycle with timing of the host's access cycle. The valid signal indicates to the control circuit that an access to the silicon file is being requested by the host. The control circuit must determine if the system access is a read or write cycle, determine whether a refresh cycle is also being requested at the same time, signal the host to wait for valid data, generate the $\overline{RAS}$ enable signal to initiate the control and addressing timing circuits of the silicon file.

Once the control circuit has determined that a valid access cycle is being executed and arbitrated any refresh and access cycle conflicts, it must generate the $\overline{RAS}$ enable signal to initiate the control and address timing circuit. This circuit generates the $\overline{RAS}$ and $\overline{CAS}$ signals and controls the address multiplexer that multiplexes the row and column addresses. Since most silicon file devices are organized into banks of data, the control circuit must also determine what bank is being accessed. The bank decoder circuit decodes the appropriate address bits and selects the $\overline{RAS}$ signal for the selected bank allowing the read or write cycle to start.

The address multiplexer, a two-input device controlled by the select signal *(mux_select)* generated by the control circuit, selects either the lower or upper address bits to generate the row and column address (figure 9). In applications using $\overline{RAS}$-only refresh cy-

cles, the refresh address must also be multiplexed onto the address lines during a refresh cycle. This can be done with an additional multiplexer or by using three-state drivers to drive the address onto one of the multiplexer inputs. Since the silicon file uses the internal $\overline{CAS}$ before $\overline{RAS}$ address counter for self-refresh operation, it is recommended that the $\overline{CAS}$ before $\overline{RAS}$ refresh method be used to eliminate the need for synchronization of the external $\overline{RAS}$-only refresh with the internal self-refresh address. An additional signal from the PAL-based control circuit is required to enable the $\overline{CAS}$ signal before the $\overline{RAS}$ signal.

Figure 9. Address Multiplexer and Driver Circuits

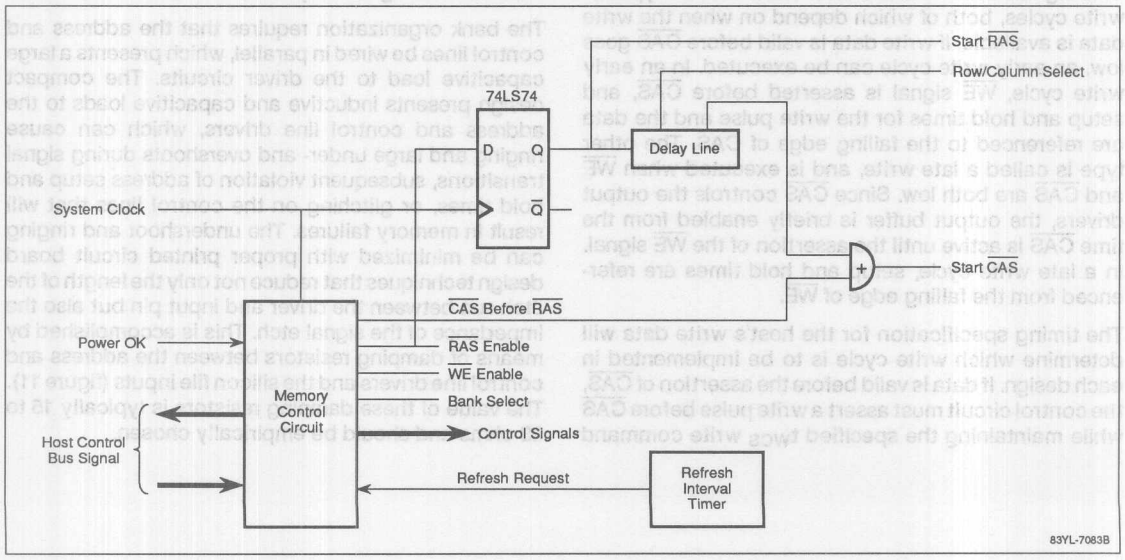


μPD42601 read or write cycles follow this sequence:

- The address multiplexer is selected for the row address bits and the row address is driven onto the address pins for a specified setup time.
- The control circuit generates $\overline{RAS}$, and the bank select decoder selects the $\overline{RAS}$ signal corresponding to the selected bank.
- The row address is maintained for a specified hold time.
- The multiplexer is switched to select a column address.
- The column address is maintained for a specified setup time and for the minimum specification for a $\overline{RAS}$ to $\overline{CAS}$ delay.
- The $\overline{CAS}$ signal is asserted.

The timing for this cycle must be precise to be able to maintain the address setup and hold times and $\overline{RAS}$ to $\overline{CAS}$ delay specifications. This timing is usually implemented in DRAM applications with a delay line of ±1 or 2 ns (figure 10), but since the silicon file's specification are not as critical as a DRAM's, the timing can be derived from a high-speed clock using synchronous flip-flop circuits (although consideration for timing skews between different devices should be considered and minimized by using flip-flops circuits from the same package). A gate array controller could also easily generate the address timing signals for a silicon file application.

Figure 10. Memory Control Circuit and $\overline{RAS}$/$\overline{CAS}$ Timing Circuit



Since the silicon file cannot be read or written while a refresh cycle is executing, the host cannot always have access to memory. The simplest way to override this is to halt the host every 32 ms and execute a burst of 512 refresh cycles, also known as *burst refreshing*. It must be pointed out that burst refresh cycles can degrade the performance of the system. The percentage of time that the microprocessor is halted for refreshing isn't large, but the length of the burst refresh period increases the system's latency time in responding to an asynchronous event.

Another approach is called *distributed refreshing*, in which a single refresh cycle is executed every 62.5 μs. In this method, if a refresh cycle and an access cycle are active at the same time, the silicon file control circuit must arbitrate control between the two cycles, i.e., the control circuit must delay the host until the refresh cycle is completed by causing the host to execute a wait state. The refresh cycle must take precedent over the active access cycle to ensure that the maximum refresh period is not exceeded. Both refresh methods require a refresh interval counter to signal the control circuit when a refresh cycle is to be executed. This circuit consists of synchronous counters, clocked by the system clock and reset after each refresh cycle.

Data Input

Data to be written into a selected cell is latched by an on-chip register with the combination of the $\overline{WE}$ and $\overline{CAS}$ signals while $\overline{RAS}$ is active. There are two types of write cycles, both of which depend on when the write data is available. If write data is valid before $\overline{CAS}$ goes low, an early write cycle can be executed. In an early write cycle, $\overline{WE}$ signal is asserted before $\overline{CAS}$, and setup and hold times for the write pulse and the data are referenced to the falling edge of $\overline{CAS}$. The other type is called a late write, and is executed when $\overline{WE}$ and $\overline{CAS}$ are both low. Since $\overline{CAS}$ controls the output drivers, the output buffer is briefly enabled from the time $\overline{CAS}$ is active until the assertion of the $\overline{WE}$ signal. In a late write cycle, setup and hold times are referenced from the falling edge of $\overline{WE}$.

The timing specification for the host's write data will determine which write cycle is to be implemented in each design. If data is valid before the assertion of $\overline{CAS}$, the control circuit must assert a write pulse before $\overline{CAS}$ while maintaining the specified t_{WCS} write command setup, t_{WCH} hold, and t_{WP} pulse width times. Since the $\overline{WE}$ signal is connected in parallel to all of the silicon file chips, propagation delays caused by capacitive loading should also be taken into account.

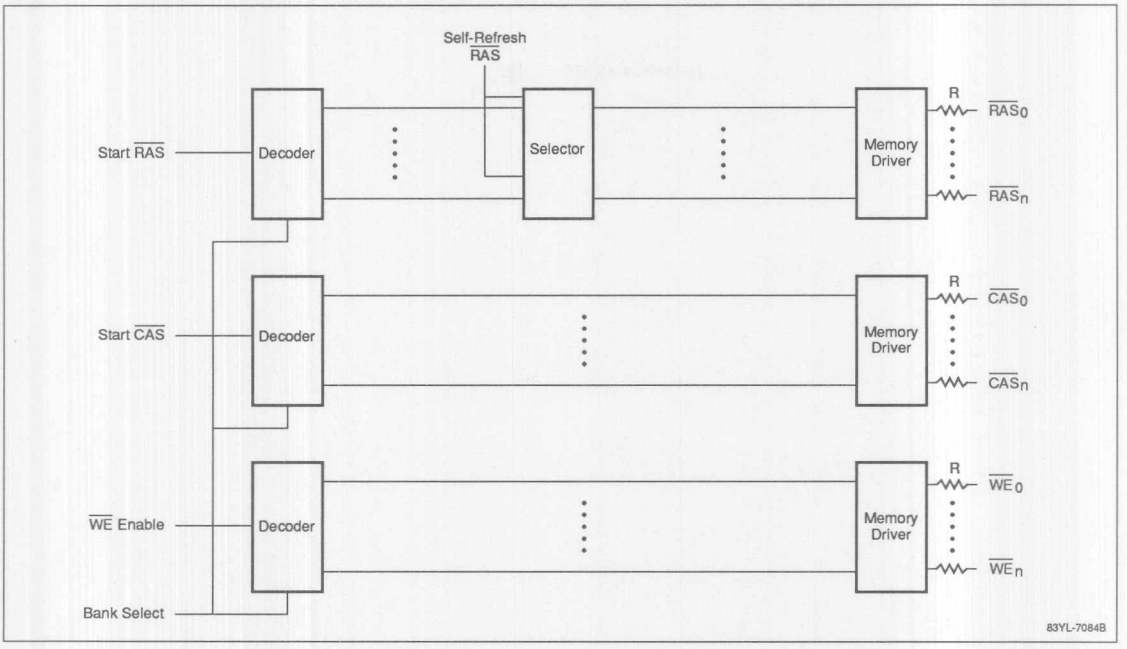
The circuit may also require write data to be latched in a transparent latch if the host isn't capable of maintaining write data long enough to meet the setup and hold times, or if a refresh arbitration cycle has to remain active during a number of wait cycles. A write data latch is controlled by a data strobe from the host that is connected to the latch enable input of the latch. The strobe should be high while write data is valid. The host system bus and the falling edge of the data strobe latch the write data at the end of the host's data cycle. The need for a write data latch is dependent upon the host's requirement for write data timing and should be considered when designing a silicon file circuit.

Memory Design Considerations

The silicon file memory array is organized into banks of chips, and the size of each bank is determined by the size of the system bus, as well as by the additional chips required for parity or error detection and correction (ERCC). For example, a 20 MByte solid-state disk with ERCC will have 5 banks of silicon file chips, each bank consisting of 32 devices to store the memory word and 7 devices to store the ERCC syndrome bits. The bank organization allows active system power to be minimized because only a part of the total array is accessed during each cycle.

The bank organization requires that the address and control lines be wired in parallel, which presents a large capacitive load to the driver circuits. The compact design presents inductive and capacitive loads to the address and control line drivers, which can cause ringing and large under- and overshoots during signal transitions, subsequent violation of address setup and hold times, or glitching on the control lines that will result in memory failures. The undershoot and ringing can be minimized with proper printed circuit board design techniques that reduce not only the length of the etch run between the driver and input pin but also the impedance of the signal etch. This is accomplished by means of damping resistors between the address and control line drivers and the silicon file inputs (figure 11). The value of these damping resistors is typically 15 to 33 ohms and should be empirically chosen.

Figure 11. Bank Decoding and Memory Driver Circuits



Because of the large input capacitance of the memory array, the transitions of address and control signals are slowed by the need to charge and discharge this capacitance. Drivers designed for use with memory arrays can drive large capacitive loads, but the designer must account for the added propagation delay due to the loading effects. If driver circuits are required to drive the address and control lines of each memory bank, the bank must divided into separate groups, and the total capacitance load must not exceed the driver's capabilities. For this purpose, some manufacturers produce memory drivers, but an integrated memory controller will provide such drivers internally.

A typical memory driver can drive a 250 pF capacitive load with the silicon file address and control line inputs specified at 5 pF for address lines and 8 pF for control lines. For a bank of 39 chips, one driver is required to drive each address line (A_0 through A_9) and two drivers to drive each control line ($\overline{RAS}$, $\overline{CAS}$, and $\overline{WE}$). This requires 16 drivers for all address and control lines. Because the driver circuits are quad packages, an additional four packages are required to drive each bank.

Power Distribution and Decoupling

As in all high-speed memory designs, controlling large current transients and protecting high frequency components from fast switching speeds is an important consideration. In order to control these current transients and prevent them from generating voltage spikes that can cause loss of data and *soft errors*, every effort must be made to minimize impedance in the decoupling path of the device.

The decoupling path is the trace distance from a power pin through a decoupling capacitor and to package ground. The impedance of this path is determined by the line inductance and series impedance of the decoupling capacitor. The line inductance can be minimized either by providing a power plane or by girding the power. To increase the effectiveness of the girded power, decoupling capacitors should be placed between the power and ground pins of every chip. The decoupling capacitors used for a typical silicon file design would be a high frequency (100 MHz) 0.2 μF ceramic capacitor. Since most memory designs have some low frequency DC currents, large bulk electrolyte 27 μF capacitors should be located judiciously around the periphery of the printed circuit board.

NEC

Memory Cards 4

Section 4
Memory Cards

MC-174/176 **4-1**
1,048,576-/4,194,304-Bit Memory Cards

PRELIMINARY INFORMATION

Introduction

The MC-174 and MC-176 are static RAM cards designed for use in applications where portability is required. They are packaged in a metal container, approximately the same size as a credit card. However, the thickness is 3.4 mm (0.133 inches), which is the thickness of about three credit cards.

The cards use standard 32,768 x 8-bit μPD43256A static RAM that is able to retain data by means of an internal battery when system power is unavailable. The data bus may be configured as either 8 or 16 bits. Furthermore, the upper or lower memory bytes may be connected for input or output to the upper or lower bytes of the data bus.

The MC-174 is organized as 131,072 bytes and the MC-176 as 524,288 bytes. An external switch prevents accidental changing of write data.

Features

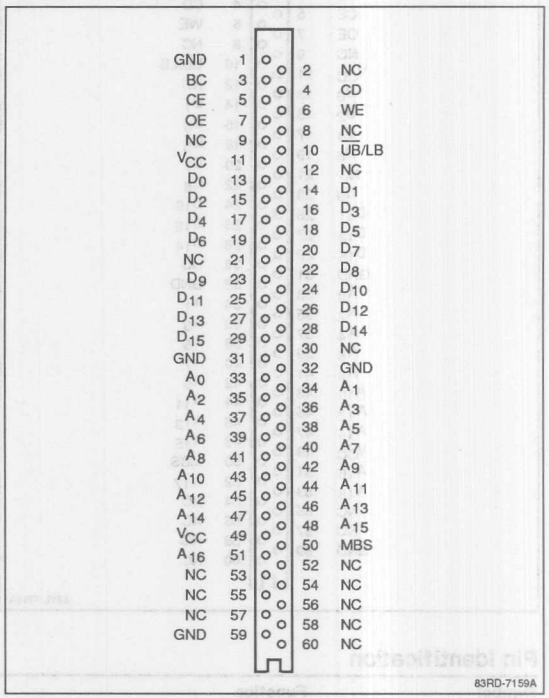
- Credit card size
- Two densities
  - — MC-174 = 131,072 bytes
  - — MC-176 = 524,288 bytes
- Easily accessible write protection switch
- Electronic card identification
- Selectable data-bus width of 8 or 16 bits
- Replaceable battery
- Battery test circuit
- Single + 5-volt power supply

Ordering Information

Part Number	Read Access Cycle (max)	Organization	Package
MC-174	250 ns	131,072 bytes	60-pin IC card
MC-176	250 ns	524,288 bytes	60-pin IC card

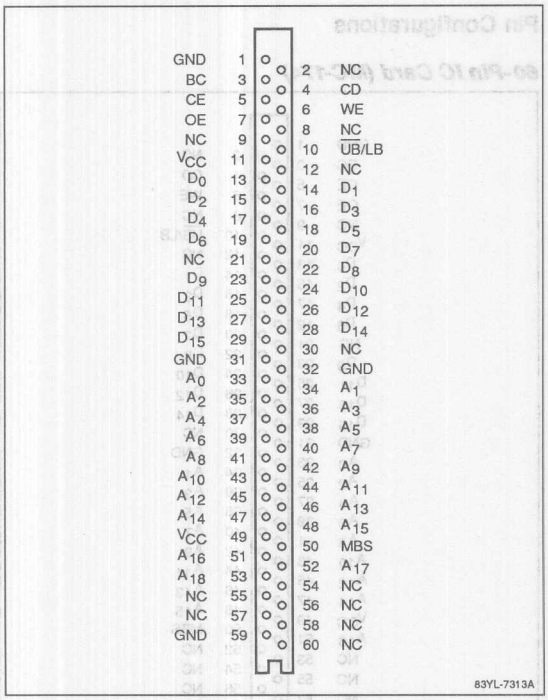
Pin Configurations

60-Pin IC Card (MC-174)



Pin Configurations (cont)

60-Pin IC Card (MC-176)



Pin Identification

Symbol	Function
A_0 - A_{18}	Addresses
BC	Battery check
CD	Card detect
CE	Card enable
D_0 - D_{15}	Data inputs/outputs
MBS	Bus select
OE	Output enable
$\overline{UB}$/LB	Upper byte/lower byte
WE	Write enable
GND	Ground
V_{CC}	+5-volt power supply
NC	No connection

Pin Descriptions

A_0 through A_{18}. These pins serve as addresses for standard read and write cycles.

BC (Battery Check). This pin measures the voltage of the card's internal backup battery.

CD (Card Detect). This pin controls reading of the electronic signature.

CE (Card Enable). This pin is used to select the card for read or write operation. CE high activates the device and CE low puts it in standby.

D_0 through D_{15}. These pins serve as the data bus interface between the MC-174/176 and the system.

MBS (Memory Bus Select). During a write cycle, the signal from this pin selects a byte of the data bus to be written.

OE (Output Enable). The signal from this pin controls the output drivers for D_0 through D_{15}.

$\overline{UB}$/LB (Upper Byte/Lower Byte). The signal from this pin selects the upper or lower byte of the memory card for connection to the upper or lower byte of the data bus.

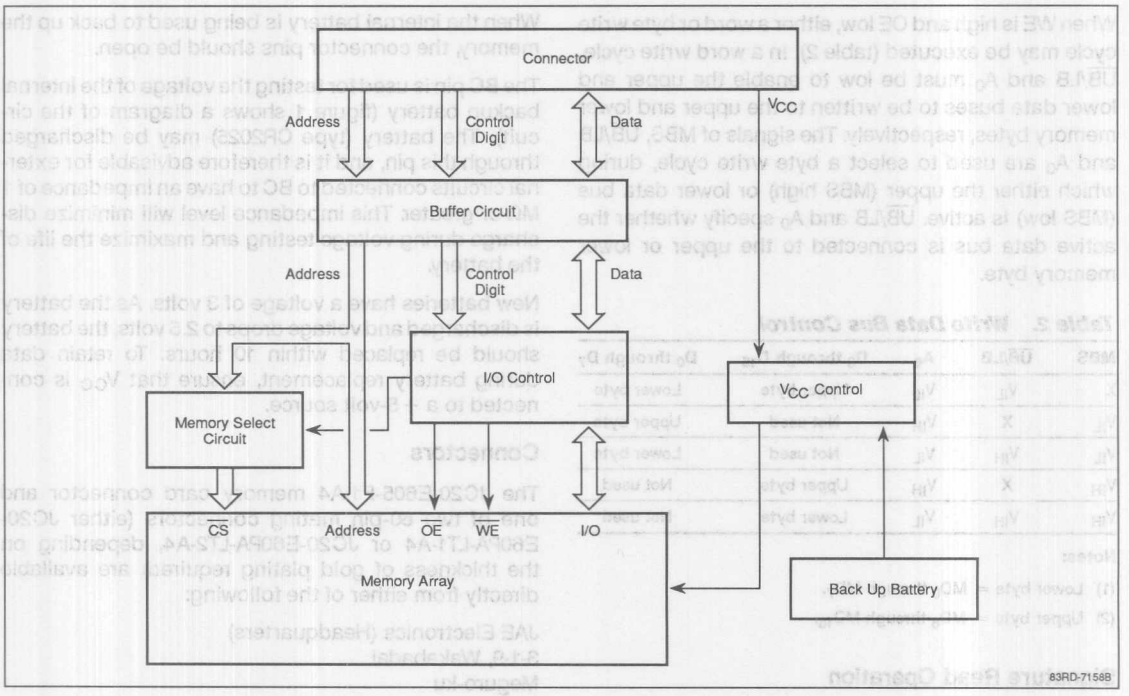
WE (Write Enable). This pin controls read and write operation.

Addressing

Addresses on the MC-174/176 designate bytes to be selected. Since the cards are able to be organized as 8 or 16 bits, the lower memory byte is selected when A_0 is low and the upper memory byte when A_0 is high. A_0 is the least significant bit in byte organization. In word organization, A_0 remains low and A_1 becomes the least significant bit.

The MC-174/176 are internally organized as two 8-bit bytes, a lower byte encompassing locations MD_0 through MD_7 and an upper byte encompassing MD_8 through MD_{15}. The lower and upper memory bytes may be logically connected to the lower or upper data bus, D_0 through D_7 and D_8 through D_{15}, respectively, as specified by a combination of signals from A_0 and $\overline{UB}$/LB.

Block Diagram



A low on $\overline{UB}$/LB while A_0 is toggling connects first the lower and then the upper memory byte to the lower byte of the data bus (D_0 through D_7). A_0 first goes low and then high, respectively. The upper byte of the data bus is connected to the upper memory byte while $\overline{UB}$/LB is low, regardless of whether A_0 is high or low. A high on $\overline{UB}$/LB while A_0 is toggling alternately connects the lower memory byte to both bytes of the data bus when A_0 is low. The upper memory byte is connected to both bytes of the data bus when A_0 is high. See table 1.

If 16-bit data is required, i.e., with the upper memory byte connected to the upper data bus and the lower memory byte to the lower data bus, then A_0 must remain low and A_1 becomes the least significant bit.

Table 1. Read Data Bus Control

$\overline{UB}$/LB	A_0	D_8 through D_{15}	D_0 through D_7
V_{IL}	V_{IL}	Upper byte	Lower byte
X	V_{IH}	Upper byte	Upper byte
V_{IH}	V_{IL}	Lower byte	Lower byte

Notes:

(1) Lower byte = MD_0 through MD_7.

(2) Upper byte = MD_8 through MD_{15}.

Read Operation

Read operation is initiated by applying high logic levels to CE and OE and low levels to CD and WE.

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Write Operation

When WE is high and OE low, either a word or byte write cycle may be executed (table 2). In a word write cycle, $\overline{UB}$/LB and A_0 must be low to enable the upper and lower data buses to be written to the upper and lower memory bytes, respectively. The signals of MBS, $\overline{UB}$/LB and A_0 are used to select a byte write cycle, during which either the upper (MBS high) or lower data bus (MBS low) is active. $\overline{UB}$/LB and A_0 specify whether the active data bus is connected to the upper or lower memory byte.

Table 2. Write Data Bus Control

MBS	$\overline{UB}$/LB	A_0	D_8 through D_{15}	D_0 through D_7
X	V_{IL}	V_{IL}	Upper byte	Lower byte
V_{IL}	X	V_{IH}	Not used	Upper byte
V_{IL}	V_{IH}	V_{IL}	Not used	Lower byte
V_{IH}	X	V_{IH}	Upper byte	Not used
V_{IH}	V_{IH}	V_{IL}	Lower byte	Not used

Notes:

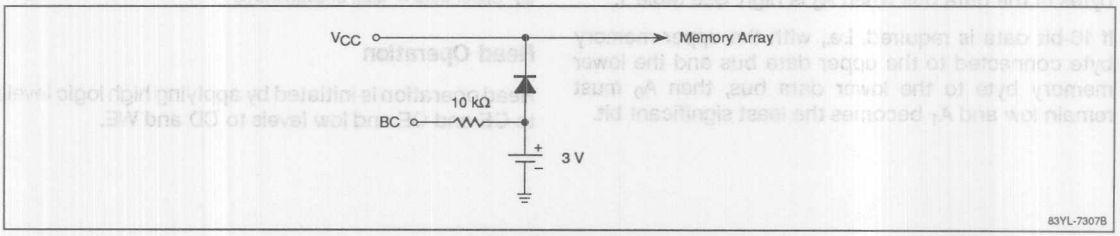
(1) Lower byte = MD_0 through MD_7.

(2) Upper byte = MD_8 through MD_{15}.

Signature Read Operation

The existence and type of memory card installed may be detected by the system using a signature read cycle. The card signature is accessed by applying a high logic level to CD and OE and a low to CE and WE. The signature word will then be accessible on D_0 through D_{15} of the data bus. Table 3 decodes the contents of the signature word.

Figure 1. Battery Test Circuit



Checking the Battery

When the internal battery is being used to back up the memory, the connector pins should be open.

The BC pin is used for testing the voltage of the internal backup battery (figure 1 shows a diagram of the circuit). The battery (type CR2025) may be discharged through this pin, and it is therefore advisable for external circuits connected to BC to have an impedance of 1 MΩ or greater. This impedance level will minimize discharge during voltage testing and maximize the life of the battery.

New batteries have a voltage of 3 volts. As the battery is discharged and voltage drops to 2.5 volts, the battery should be replaced within 10 hours. To retain data during battery replacement, ensure that V_{CC} is connected to a + 5-volt source.

Connectors

The JC20-E605-F1-A4 memory card connector and one of two 60-pin mating connectors (either JC20-E60PA-LT1-A4 or JC20-E60PA-LT2-A4, depending on the thickness of gold plating required) are available directly from either of the following:

JAE Electronics (Headquarters)
3-1-9, Wakabadai
Meguro-ku
Tokyo, Japan 153
Telephone: 011-81-3-780-2889
FAX: 011-81-3-780-2884

JAE Electronics (USA Sales Office)
142 Technology Drive, Suite 100
Irvine, CA 92718
Telephone: (714) 753-2600
FAX: (714) 753-2699

Table 3. Signature Read Operation

Device	D_{15}	D_{14}	D_{13}	D_{12}	D_{11}	D_{10}	D_9	D_8	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
MC-174	V_{IH}	V_{IL}	WP	X	X	V_{IH}	V_{IL}	V_{IL}	V_{IL}	V_{IH}	V_{IL}	V_{IL}	V_{IL}	V_{IH}	V_{IL}	V_{IH}
MC-176	V_{IH}	V_{IL}	WP	X	X	V_{IH}	V_{IL}	V_{IL}	V_{IL}	V_{IH}	V_{IL}	V_{IL}	V_{IL}	V_{IH}	V_{IH}	V_{IH}

Notes:

(1) WP = the status of the write protect switch, where V_{IH} indicates write protection has been enabled and V_{IL} means it is disabled.

(2) X can be either V_{IL} or V_{IH}.

Absolute Maximum Ratings

Supply voltage, V_{CC}	−0.5 to +7.0 V
Input voltage, V_{IN} (Note 1)	−0.5 to V_{CC} + 0.5
Output voltage, V_{OUT}	−0.5 to V_{CC} + 0.5
Storage temperature, t_{STG}	−20 to +60°C
Operating temperature, t_{OPR}	0 to +50°C
Battery backup operating temperature, t_{BU}	0 to +50°C

Notes:

(1) −3.0 V minimum for 50 ns maximum pulse width.

Capacitance

T_A = 25°C; f = 1 MHz; V_{CC} = 0 V; V_{IN} and $V_{I/O}$ = 0 V

Parameter	Symbol	Max	Unit	Pins Under Test
Input capacitance	C_{IN}	10	pF	Addresses, CD, CE, MBS, OE, $\overline{UB}$/LB, WE
Input/output capacitance	$C_{I/O}$	35	pF	D_0 through D_{15}

Notes:

(1) X can be either V_{IL} or V_{IH}.

Recommended Operating Conditions

Parameter	Symbol	Min	Typ	Max	Unit
Supply voltage	V_{CC}	4.75	5.0	5.25	V
Input voltage, low	V_{IL}	0		0.7	V
Input voltage, high	V_{IH}	2.3		V_{CC}	V
Ambient temperature	T_A	0		50	°C

Truth Table

Function	D_0 - D_{15}	CE	CD	WE	OE
Standby	High-Z	V_{IL}	V_{IL}	X	X
Read cycle	Data out	V_{IH}	V_{IL}	V_{IL}	V_{IH}
	High-Z	V_{IH}	V_{IL}	V_{IL}	V_{IL}
Write cycle	Data-in	V_{IH}	V_{IL}	V_{IH}	V_{IL}
Signature read	Data out	V_{IL}	V_{IH}	V_{IL}	V_{IH}
	High-Z	V_{IL}	V_{IH}	V_{IL}	V_{IL}
Invalid	High-Z	V_{IL}	V_{IH}	V_{IH}	V_{IL}
Prohibited	High-Z	V_{IH}	V_{IH}	X	X

Notes:

(1) X can be either V_{IH} or V_{IL}.

Data Bus Control

$\overline{UB}$/LB	A_0	MBS	WE	OE	D_{15} through D_8	D_7 through D_0
V_{IL}	V_{IL}	X	V_{IL}	V_{IH}	Upper byte	Lower byte
X	V_{IH}	X	V_{IL}	V_{IH}	Upper byte	Upper byte
V_{IH}	V_{IL}	X	V_{IL}	V_{IH}	Lower byte	Lower byte
V_{IL}	V_{IL}	V_{IL}	V_{IH}	V_{IL}	Upper byte	Lower byte
X	V_{IH}	V_{IL}	V_{IH}	V_{IL}	Not used	Upper byte
V_{IH}	V_{IL}	V_{IL}	V_{IH}	V_{IL}	Not used	Lower byte
V_{IL}	V_{IL}	V_{IH}	V_{IH}	V_{IL}	Upper byte	Lower byte
X	V_{IH}	V_{IH}	V_{IH}	V_{IL}	Upper byte	Not used
V_{IH}	V_{IL}	V_{IH}	V_{IH}	V_{IL}	Lower byte	Not used

Notes:

(1) X can be either V_{IL} or V_{IH}.

(2) Lower = MD_0 through MD_7.

(3) Upper = MD_8 through MD_{15}.

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DC Characteristics

T_A = 0 to 50°C; V_{CC} = +5.0 V ±5%

Parameter	Symbol	Min	Max	Unit	Test Conditions
I/O leakage current, high	I_{OH}		260	μA	(Notes 1, 2)
I/O leakage current, low	I_{OL}	−10		μA	(Notes 1, 2)
Operating supply current	I_{CCA}		140	mA	
Standby supply current	I_{SB}		2	mA	(Note 3)
Output voltage, high	V_{OH1}	V_{CC} − 0.6		V	I_{OH} = −0.1 mA
	V_{OH2}	V_{CC} − 1.0		V	I_{OH} = −4.0 mA
Output voltage, low	V_{OL}		0.4	V	I_{OL} = 4.0 mA

Notes:

(1) This parameter is periodically sampled and not 100% tested.

(2) V_{IN} = V_{CC} or GND.

(3) CE ≤ 2.0 V and CD ≤ 0.2 V. All other pins ≤ 0.2 V or ≥ V_{CC} − 0.2 V or high impedance.

AC Characteristics

T_A = 0 to 50°C; V_{CC} = +5.0 V ±5%

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions
Read Operation						
Address access time	t_{AA}			250	ns	
CE access time	t_{ACE}			250	ns	
CE to output in high-Z	t_{HZ}			100	ns	
CE to output in low-Z	t_{LZ}	5			ns	
Output enable to output valid	t_{OE}			120	ns	
Output hold from address change	t_{OH}	10			ns	
OE to output in high-Z	t_{OHZ}			80	ns	
OE to output in low-Z	t_{OLZ}	5			ns	
Read cycle time	t_{RC}	250			ns	
Write Operation						
Address setup time	t_{AS}	20			ns	
Address valid to end of write	t_{AW}	200			ns	
CE to end of write	t_{CW}	200			ns	
Data hold time	t_{DH}	10			ns	
Data valid to end of write	t_{DW}	100			ns	
Write cycle time	t_{WC}	250			ns	
Write pulse width	t_{WP}	150			ns	
Write recovery time	t_{WR}	10			ns	

AC Characteristics (cont)

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions
Signature Read Operation						
Address access time	t_{AD1}			200	ns	
Card signature access time	t_{CD1}			100	ns	
Card signature to output in high-Z	t_{CD2}			90	ns	
OE access time	t_{OD1}			150	ns	
OE to output in high-Z	t_{OD2}			60	ns	
Cycle time	t_{OP}	180			ns	

Notes:

(1) Input pulse levels = 0.7 to 2.5 V; input pulse rise and fall times = 5 ns; timing reference levels = 1.5 V. See figures 1 and 2 for output load.

Figure 2. Output Load

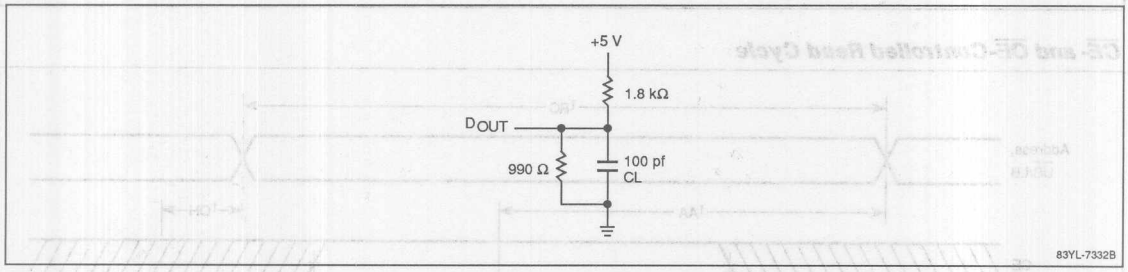
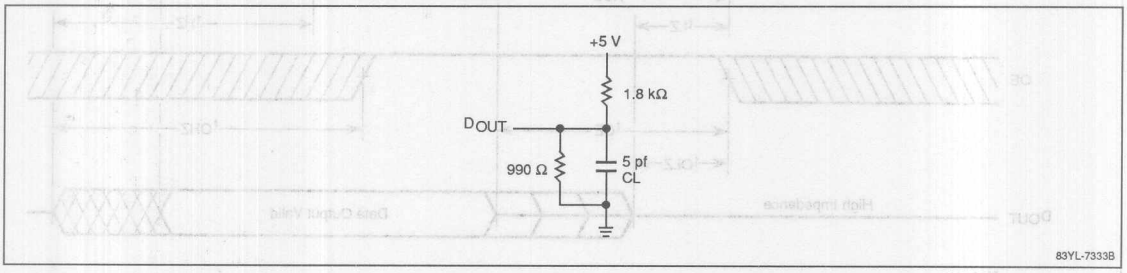


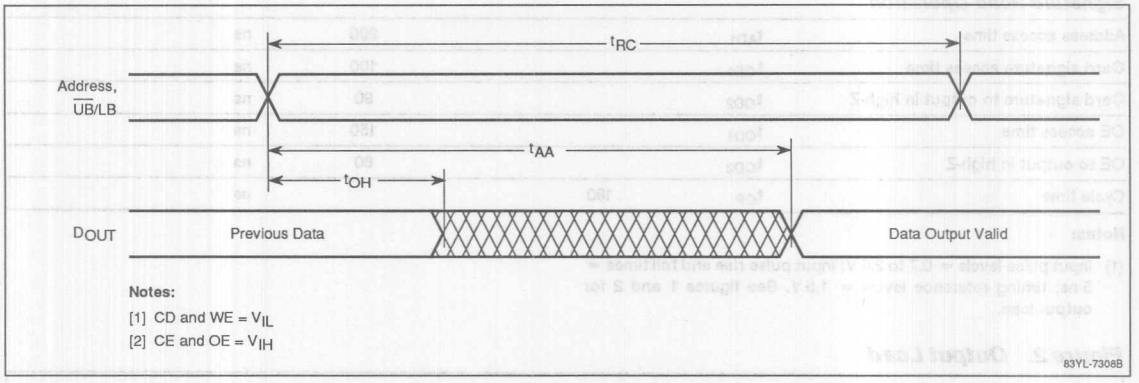
Figure 3. Output Load for t_{HZ}, t_{OHZ} and t_{OLZ}



4

Timing Waveforms

Read Cycle



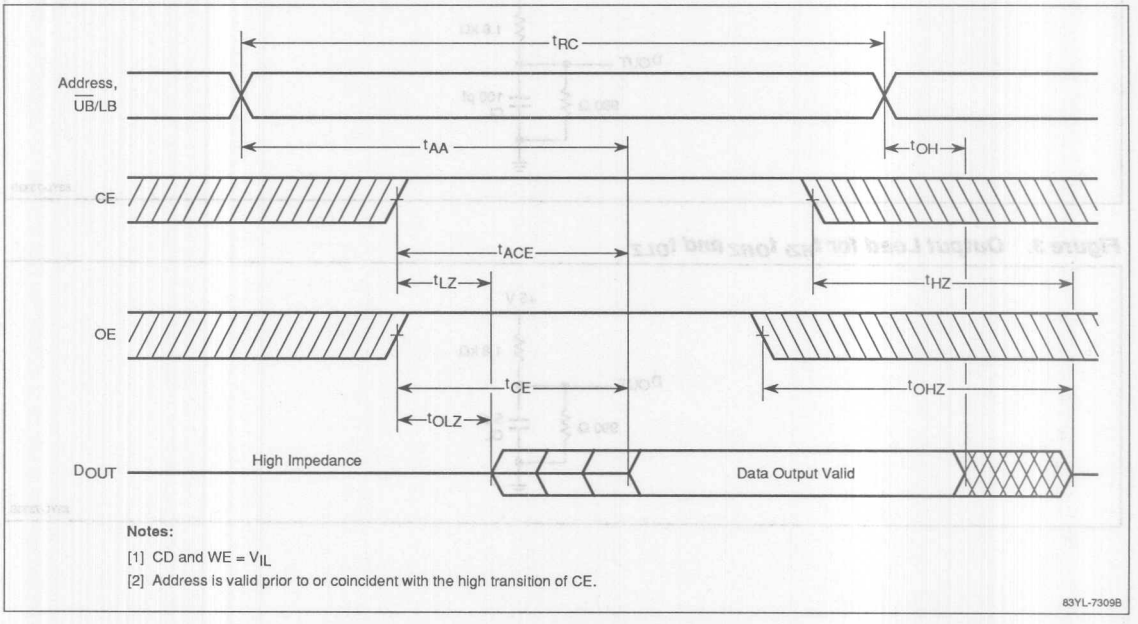
Notes:

[1] CD and WE = V_{IL}

[2] CE and OE = V_{IH}

83YL-7308B

$\overline{CE}$- and $\overline{OE}$-Controlled Read Cycle



Notes:

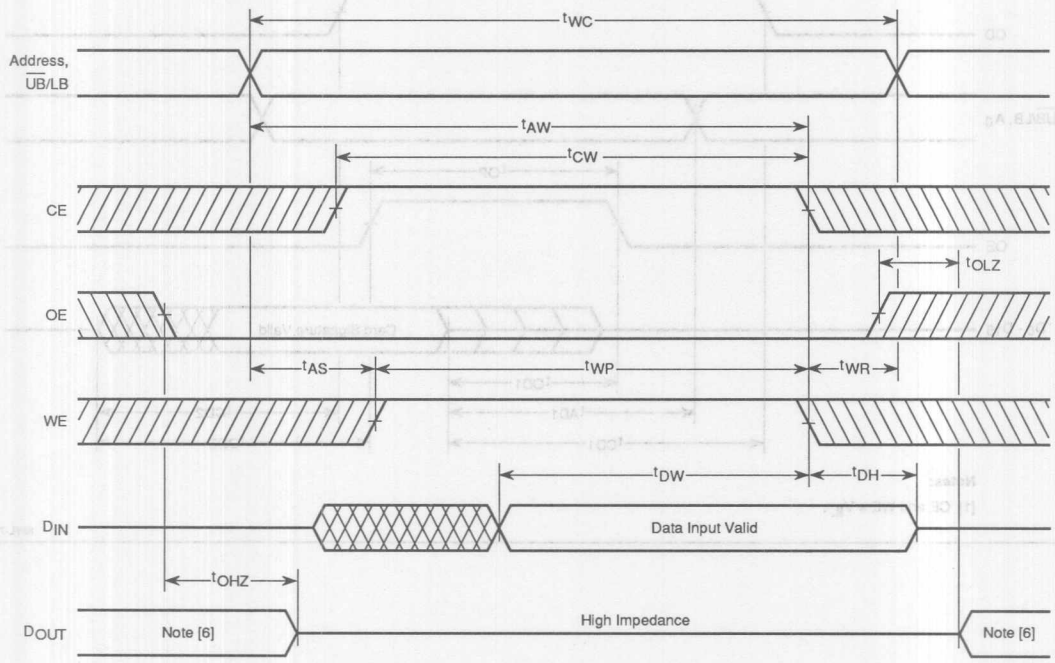
[1] CD and WE = V_{IL}

[2] Address is valid prior to or coincident with the high transition of CE.

83YL-7309B

Timing Waveforms (cont)

Write Cycle



Notes:

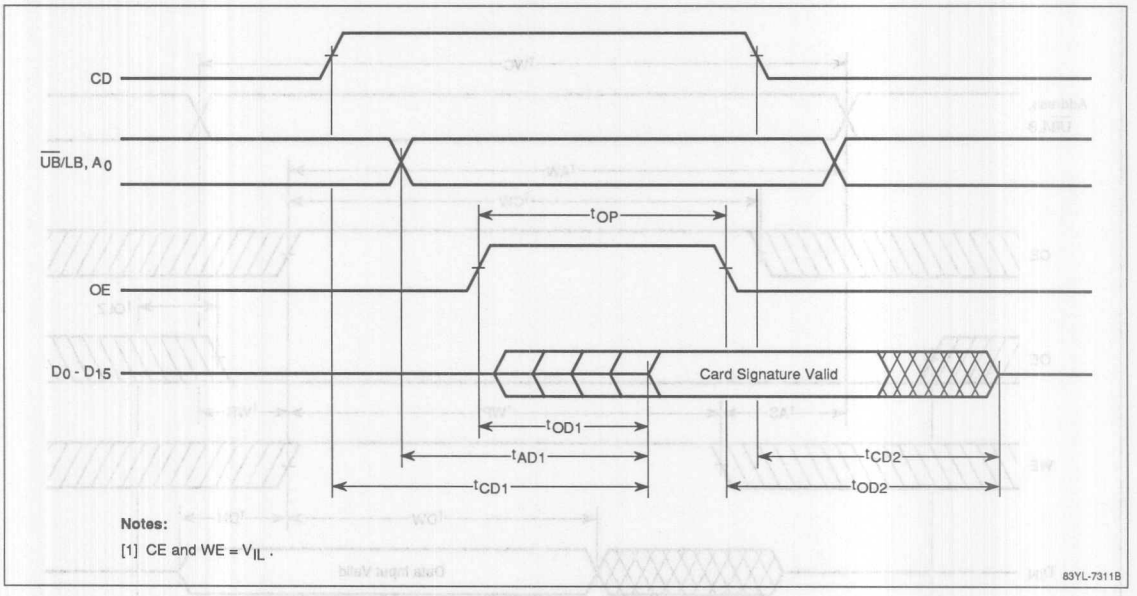
[1] A write cycle occurs during the overlap of a high CE, a high WE, and a low OE.
[2] CE or WE must be low during address transition.
[3] If OE is low, the I/O pins remain in high impedance.
[4] During a write cycle, OE must be low prior to the high-to-low transition of WE.
[5] During a write cycle, MBS must be stable at either a high or low level.
[6] During this period, the I/O pins may be in the output state; therefore, input signals of opposite phase to outputs must not be applied.

83YL-7310B

4

Timing Waveforms (cont)

Signature Read Cycle



Notes:

[1] CE and WE = V_{IL} .

83YL-7311B

NEC

Dynamic RAM Modules

5

Section 5
Dynamic RAM Modules

MC-157 5-1
262,144 x 8-Bit Dynamic CMOS RAM Module

MC-41256A8 5-13
262,144 x 8-Bit Dynamic NMOS RAM Module

MC-421000A8 5-25
1,048,576 x 8-Bit Dynamic CMOS RAM Module

MC-424100A8 5-39
4,194,304 x 8-Bit Dynamic CMOS RAM Module

MC-41256A9 5-51
262,144 x 9-Bit Dynamic NMOS RAM Module

MC-421000A9 5-65
1,048,576 x 9-Bit Dynamic CMOS RAM Module

MC-424100A9 5-81
4,194,304 x 9-Bit Dynamic CMOS RAM Module

MC-424256A36 5-97
262,144 x 36-Bit Dynamic RAM Module

MC-424256A36BH/FH 5-109
262,144 x 36-Bit Dynamic CMOS RAM Module

MC-424512A36 5-123
524,288 x 36-Bit Dynamic RAM Module

MC-424512A36BH/FH 5-135
524,288 x 36-Bit Dynamic CMOS RAM Module

MC-421000A36 5-147
1,048,576 x 36-Bit
Dynamic CMOS RAM Module

MC-422000A36 5-159
2,097,152 x 36-Bit
Dynamic CMOS RAM Module

Additional New Product Information

Device Number	Description	Comments
Dynamic RAM Modules		
MC-42256AE9	256K x 9-bit fast-page SIMM	Three-piece solution, with speeds to 70 ns
MC-424256AE36	256K x 36-bit fast-page SIMM	One-inch height, with speeds to 70 ns
MC-424512AE36	512K x 36-bit fast-page SIMM	One-inch height, with speeds to 70 ns
MC-421000A36xD	1M x 36-bit fast-page SIMM	One-inch height, with speeds to 70 ns
MC-424512AA40	512K x 40-bit fast-page SIMM	Speeds to 60 ns
MC-421000AA40	1M x 40-bit fast-page SIMM	Speeds to 70 ns
MC-422000AA40	2M x 40-bit fast-page SIMM	Speeds to 70 ns

MC-157
262,144 x 8-Bit
Dynamic CMOS RAM Module

Description

The MC-157 is a CMOS-fabricated RAM module organized as 262,144 words by 8 bits and designed to operate from a single +5-volt power supply. Good system operating margins are provided by advanced dynamic circuitry, including a single-transistor storage cell, multiplexed address buffers and flexible refresh controls.

The MC-157 is packaged in a Single Inline Memory Module (SIMM™) and contains two 1-Mbit μPD424256 DRAMs in plastic SOJs and two power supply decoupling capacitors to enhance reliability and reduce the size, weight, and cost of a system. Refreshing is accomplished by means of $\overline{RAS}$-only refresh cycles, hidden refresh cycles, $\overline{CAS}$ before $\overline{RAS}$ refresh cycles, or by normal read or write cycles on the 512 address combinations of A_0 - A_8 during an 8-ms period.

Features

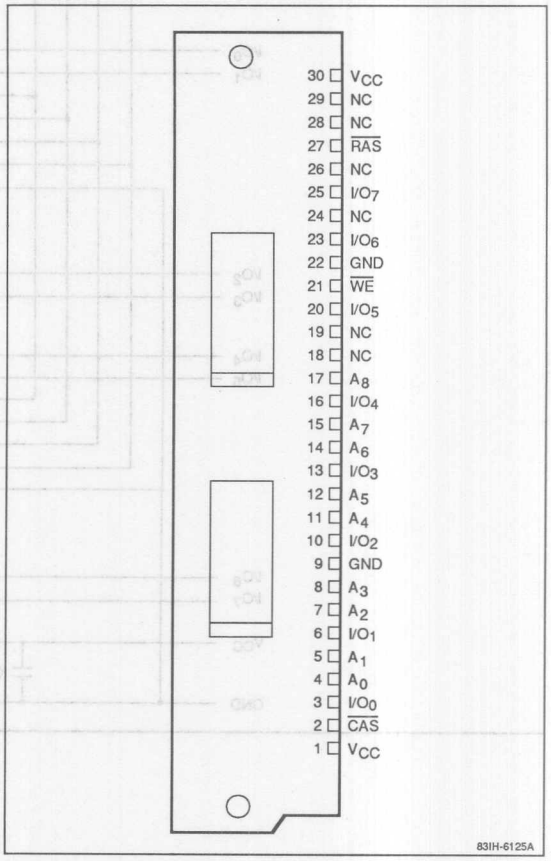
- 262,144-word x 8-bit organization
- Single +5-volt ± 10% power supply
- Standard 30-pin SIMM packaging
- Two standard 1-Mbit DRAMs incorporated in high-density SOJs
- Two power supply decoupling capacitors
- Low power dissipation: 11 mW max (standby)
- TTL-compatible inputs and outputs

Ordering Information

Part Number	Access Time (max)	Fast-Page Cycle Time (min)	Package
MC-157-10	100 ns	60 ns	30-pin socket mountable SIMM

Pin Configuration

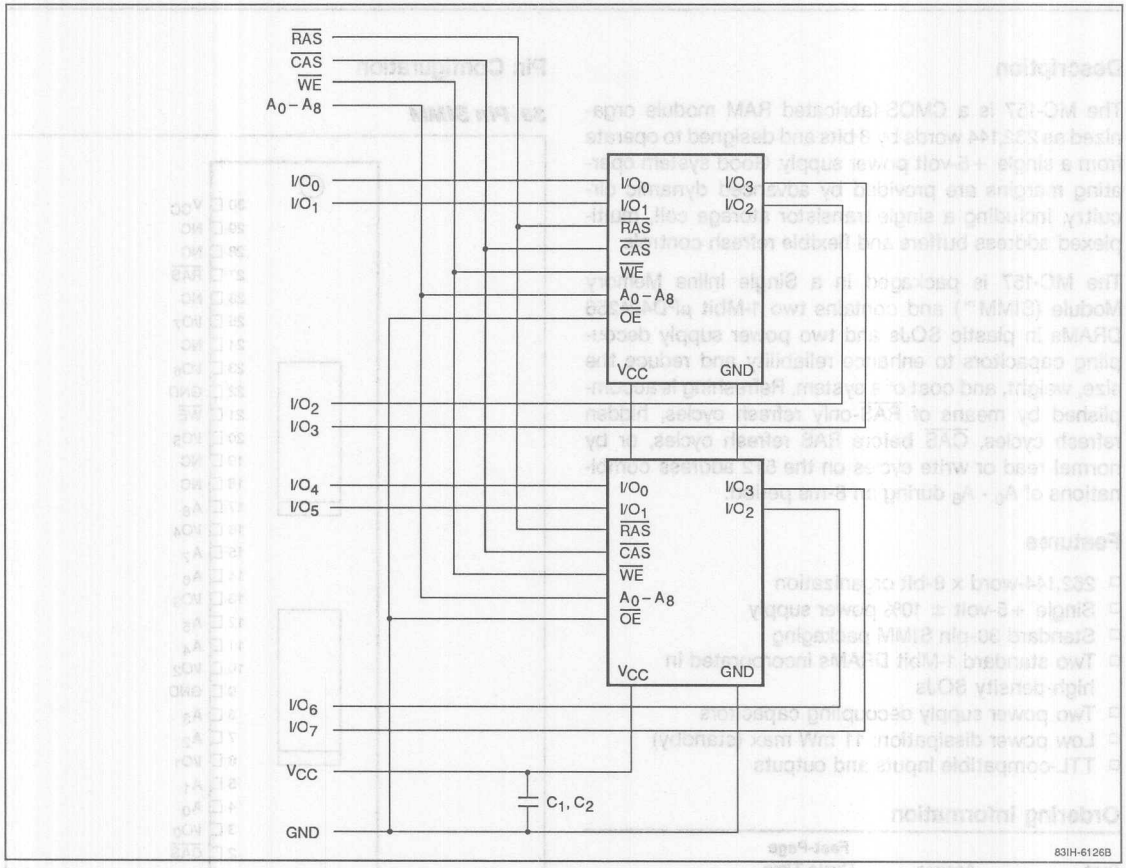
30-Pin SIMM



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SIMM is a trademark of Wang Laboratories.

Block Diagram



Pin Identification

Symbol	Function
A_0 - A_8	Address inputs
I/O_0 - I/O_7	Common data inputs and outputs
$\overline{CAS}$	Column address strobe
$\overline{RAS}$	Row address strobe
$\overline{WE}$	Write enable
GND	Ground
V_{CC}	+5-volt power supply
NC	No connection

Capacitance

T_A = 25°C; f = 1 MHz

Parameter	Symbol	Max	Unit	Pins Under Test
Input capacitance	C_{IA}	12	pF	A_0 - A_8
	C_{IR}	16	pF	$\overline{RAS}$, $\overline{WE}$
	C_{IC}	16	pF	$\overline{CAS}$
Input/output capacitance	C_{DQ}	8	pF	For I/O_0 - I/O_7: $\overline{CAS}$ = V_{IH} to disable D_{OUT}

Absolute Maximum Ratings

Voltage on any pin relative to GND	−1.0 to +7.0 V
Operating temperature, T_{OPR}, ambient	0 to 70°C
Storage temperature, T_{STG}	−55 to +125°C
Short-circuit output current, I_{OS}	50 mA
Power dissipation, P_D	2.0 W

Exposure to Absolute Maximum Ratings for extended periods may affect device reliability; exceeding the ratings could cause permanent damage. The device should be operated within the limits specified under DC and AC Characteristics.

Recommended Operating Conditions

Parameter	Symbol	Min	Typ	Max	Unit
Supply voltage	V_{CC}	4.5	5.0	5.5	V
Input voltage, high	V_{IH}	2.4		V_{CC} + 1.0	V
Input voltage, low	V_{IL}	−1.0		0.8	V
Ambient temperature	T_A	0		70	°C

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DC Characteristics

T_A = 0 to 70°C; V_{CC} = +5.0 V ±10%; GND = 0 V

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions
Operating current, average	I_{CC1}			120	mA	$\overline{RAS}$, $\overline{CAS}$ cycling; t_{RC} = t_{RC} min (Note 5)
Standby current	I_{CC2}			4.0	mA	$\overline{RAS}$ = $\overline{CAS}$ = V_{IH}
				2.0	mA	$\overline{RAS}$ = $\overline{CAS}$ = V_{CC} − 0.2 V
Refresh operating current, average	I_{CC3}			120	mA	$\overline{RAS}$ cycling; $\overline{CAS}$ = V_{IH}; t_{RC} = t_{RC} min (Note 5)
Fast-page operating current, average	I_{CC4}			100	mA	$\overline{RAS}$ = V_{IH}; $\overline{CAS}$ cycling; t_{PC} = t_{PC} min (Note 5)
$\overline{CAS}$ before $\overline{RAS}$ refresh operating current, average	I_{CC5}			120	mA	$\overline{RAS}$ cycling; $\overline{CAS}$ = V_{IL}; t_{RC} = t_{RC} min (Note 5)
Input leakage current	I_{IL}	−20		20	μA	V_{IN} = 0 to V_{CC}; other pins = 0 V
Output leakage current	I_{OL}	−10		10	μA	D_{OUT} disabled; V_{OUT} = 0 to V_{CC}
Output voltage, low	V_{OL}	0		0.4	V	I_{OUT} = 4.2 mA
Output voltage, high	V_{OH}	2.4		V_{CC}	V	I_{OUT} = −5 mA

AC Characteristics

T_A = 0 to 70°C; V_{CC} = +5.0 V ±10%

Parameter	Symbol	Min	Max	Unit	Test Conditions
Random read or write cycle time	t_{RC}	190		ns	(Note 6)
Fast-page cycle time	t_{PC}	60		ns	(Note 6)
Refresh period	t_{REF}		8	ms	Addresses A_0 - A_8
Access time from $\overline{RAS}$	t_{RAC}		100	ns	(Notes 7, 8, 11)
Access time from $\overline{CAS}$	t_{CAC}		25	ns	(Notes 7, 9, 10, 11, 13)
Access time from column address	t_{AA}		50	ns	(Notes 7, 10, 13)
Access time from $\overline{CAS}$ precharge (rising edge)	t_{ACP}		55	ns	(Notes 7, 13)
Output buffer turnoff delay	t_{OFF}	0	25	ns	(Note 17)
Rise and fall transition time	t_T	3	50	ns	(Note 4)
$\overline{RAS}$ precharge time	t_{RP}	80		ns	
$\overline{RAS}$ pulse width	t_{RAS}	100	10000	ns	
$\overline{RAS}$ hold time	t_{RSH}	25		ns	
$\overline{CAS}$ pulse width	t_{CAS}	25	10000	ns	
$\overline{CAS}$ hold time	t_{CSH}	100		ns	
$\overline{RAS}$ to $\overline{CAS}$ delay time	t_{RCD}	25	75	ns	(Note 11)
$\overline{RAS}$ to column address read time	t_{RAD}	17	50	ns	(Note 10)
$\overline{CAS}$ to $\overline{RAS}$ precharge time	t_{CRP}	10		ns	(Note 12)
$\overline{CAS}$ precharge time (non-page cycle)	t_{CPN}	10		ns	
$\overline{CAS}$ precharge time (fast-page cycle)	t_{CP}	10	25	ns	(Note 13)
$\overline{RAS}$ precharge $\overline{CAS}$ hold time	t_{RPC}	0		ns	
Row address setup time	t_{ASR}	0		ns	
Row address hold time	t_{RAH}	12		ns	
Column address setup time	t_{ASC}	0	20	ns	
Column address hold time	t_{CAH}	20		ns	
Column address hold time referenced to $\overline{RAS}$	t_{AR}	70		ns	
Column address lead time referenced to $\overline{RAS}$ (rising edge)	t_{RAL}	50		ns	
Read command setup time referenced to $\overline{RAS}$	t_{RRH}	10		ns	(Note 14)
Read command hold time referenced to $\overline{CAS}$	t_{RCH}	0		ns	(Note 14)
Write command hold time	t_{WCH}	20		ns	
Write command hold time referenced to $\overline{RAS}$	t_{WCR}	70		ns	
Write command pulse width	t_{WP}	20		ns	
Write command to $\overline{RAS}$ lead time	t_{RWL}	30		ns	

AC Characteristics (cont)

Parameter	Symbol	Min	Max	Unit	Test Conditions
Read command setup time referenced to $\overline{CAS}$	t_{RCS}	0		ns	
Write command to $\overline{CAS}$ lead time	t_{CWL}	20		ns	
Data-in setup time	t_{DS}	0		ns	(Note 16)
Data-in hold time	t_{DH}	20		ns	(Note 16)
Data-in hold time referenced to $\overline{RAS}$	t_{DHR}	70		ns	
Write command setup time	t_{WCS}	0		ns	
$\overline{CAS}$ setup time for $\overline{CAS}$ before $\overline{RAS}$ refreshing	t_{CSR}	10		ns	
$\overline{CAS}$ hold time for $\overline{CAS}$ before $\overline{RAS}$ refreshing	t_{CHR}	20		ns	

Notes:

(1) All voltages are referenced to GND.

(2) An initial pause of 100 μs is required after power-up, followed by any eight $\overline{RAS}$ cycles before proper device operation is achieved.

(3) Ac measurements assume t_T = 5 ns.

(4) V_{IH} (min) and V_{IL} (max) are reference levels for measuring timing of input signals. Transition times are measured between V_{IH} and V_{IL}.

(5) I_{CC1}, I_{CC3}, I_{CC4}, and I_{CC5} depend on output loading and cycle rates. Specified values are obtained with the output open. I_{CC3} is measured assuming that all column address inputs are held at either a high level or a low level during $\overline{RAS}$-only refresh cycles. I_{CC4} is measured assuming that all column address inputs are switched only once each fast-page cycle.

(6) The minimum specifications are used only to indicate the cycle time at which proper operation over the full temperature range (T_A = 0 to +70 °C) is assured.

(7) Load = 2 TTL (–1 mA, +4 mA) loads and 100 pF (V_{OH} = 2.0 V, V_{OL} = 0.8 V).

(8) Assumes that $t_{RCD} \leq t_{RCD}$ (max) and $t_{RAD} \leq t_{RAD}$ (max). If t_{RCD} or t_{RAD} is greater than the maximum recommended value in this table, t_{RAC} increases by the amount that t_{RCD} or t_{RAD} exceeds the value shown.

(9) Assumes that $t_{RCD} \geq t_{RCD}$ (max) and $t_{RAD} \leq t_{RAD}$ (max).

(10) If $t_{RAD} \geq t_{RAD}$ (max), then the access time is defined by t_{AA}.

(11) Operation within the t_{RCD} (max) limit assures that t_{RAC} (max) can be met. t_{RCD} (max) is specified as a reference point only; if t_{RCD} is greater than t_{RCD} (max), access time is controlled exclusively by t_{CAC}.

(12) The t_{CRP} requirement should be applicable for $\overline{RAS}$/$\overline{CAS}$ cycles preceded by any cycle.

(13) For fast-page read operation, access time is as follows.

$\overline{CAS}$ and Column Address Input Conditions	Access Time Definition
$t_{CP} \leq t_{CP}$ (max), $t_{ASC} \geq t_{CP}$	t_{ACP}
$t_{CP} \leq t_{CP}$ (max), $t_{ASC} \leq t_{CP}$	t_{AA}
$t_{CP} \geq t_{CP}$ (max), $t_{ASC} \leq t_{ASC}$ (max)	t_{AA}
$t_{CP} \geq t_{CP}$ (max), $t_{ASC} \geq t_{ASC}$ (max)	t_{CAC}

(14) Either t_{RRH} or t_{RCH} must be satisfied for a read cycle.

(15) Parameter t_{WP} is applicable for a delayed write cycle such as a read-write/read-modify-write cycle. For early write operation, both t_{WCS} and t_{WCH} must be met.

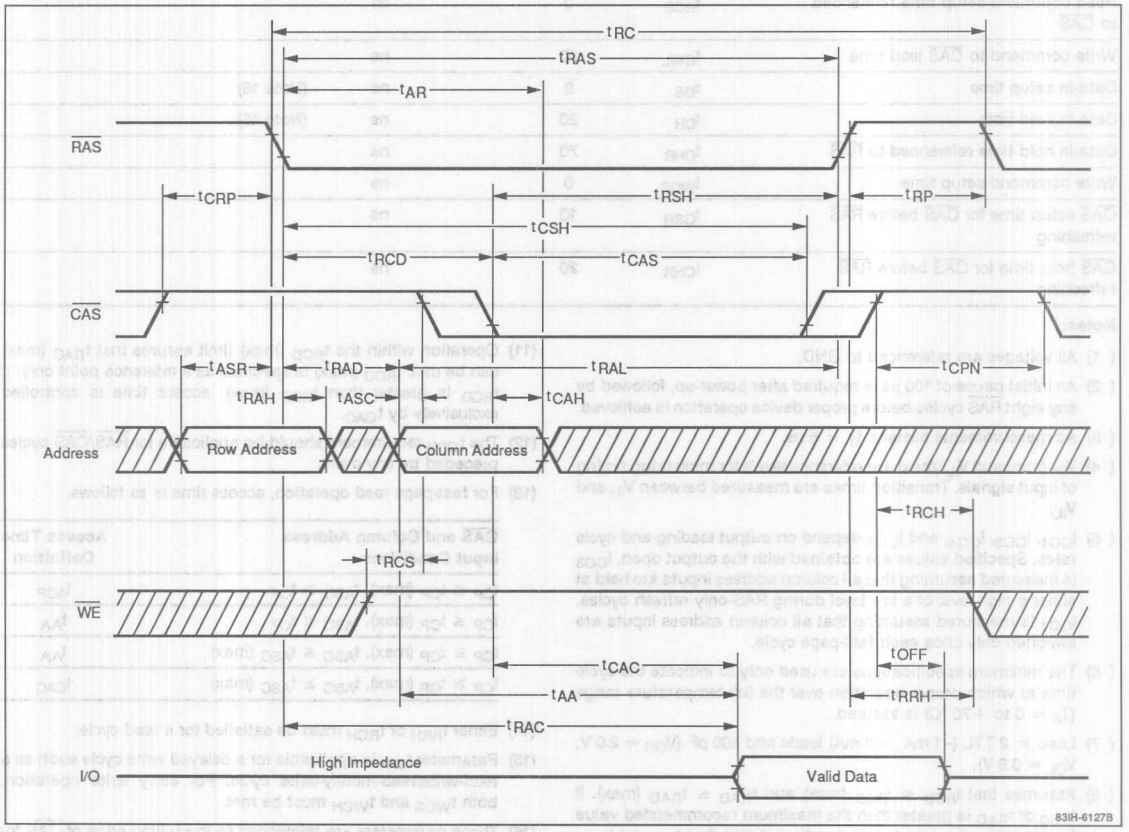
(16) These parameters are referenced to the falling edge of $\overline{CAS}$ for early write cycles and to the falling edge of $\overline{WE}$ for delayed write or read-modify-write cycles.

(17) t_{OFF} (max) defines the time at which the output achieves the open-circuit condition and is not referenced to V_{OH} and V_{OL}.

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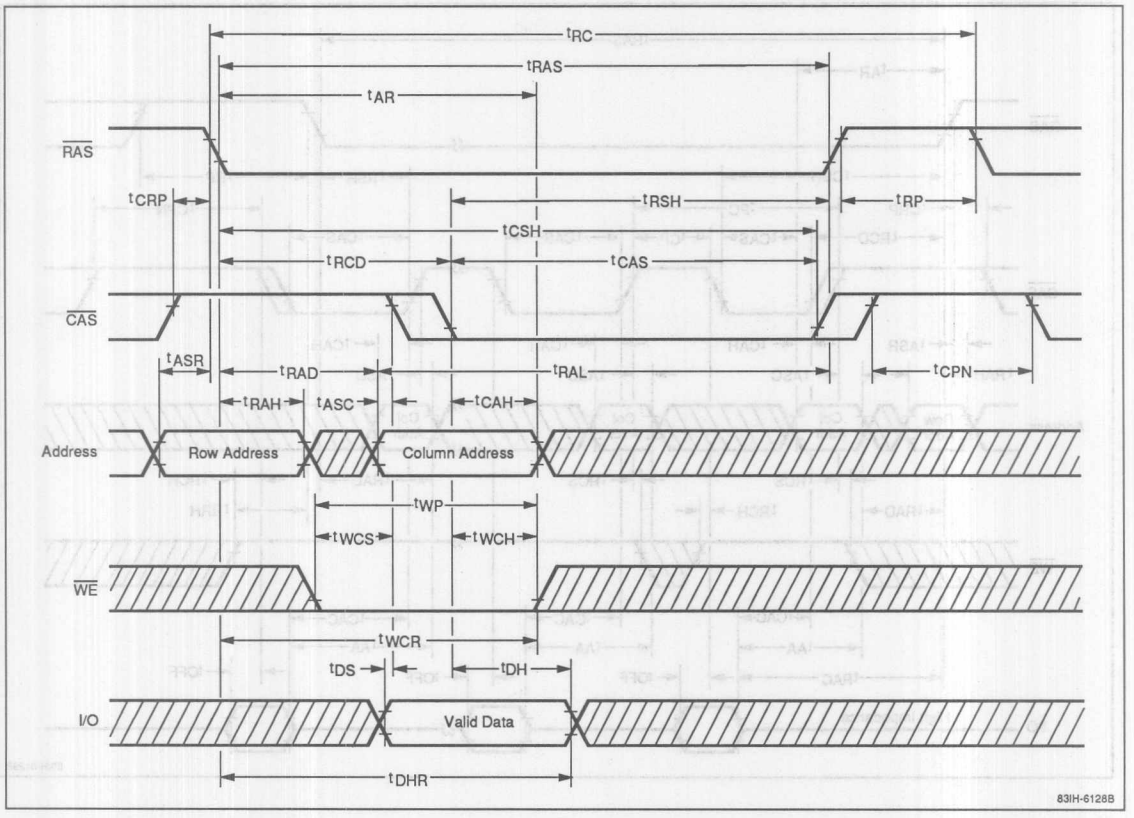
Timing Waveforms

Read Cycle



Timing Waveforms (cont)

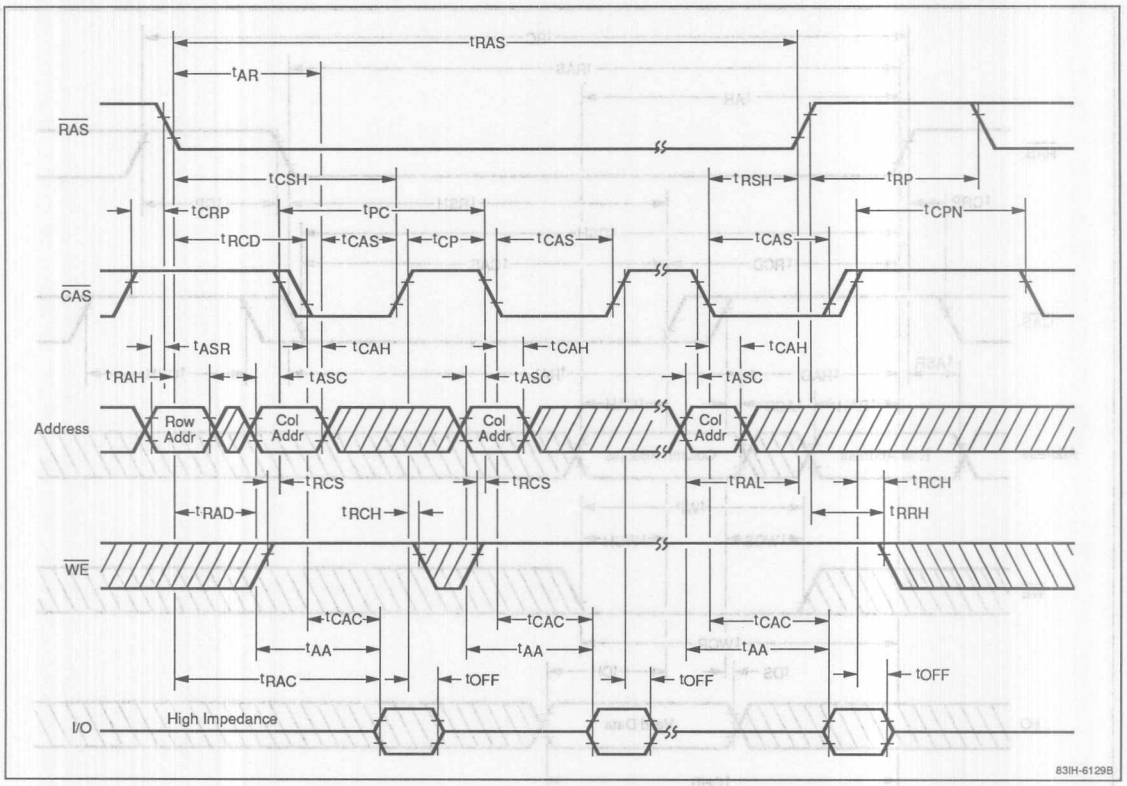
Write Cycle (Early Write)



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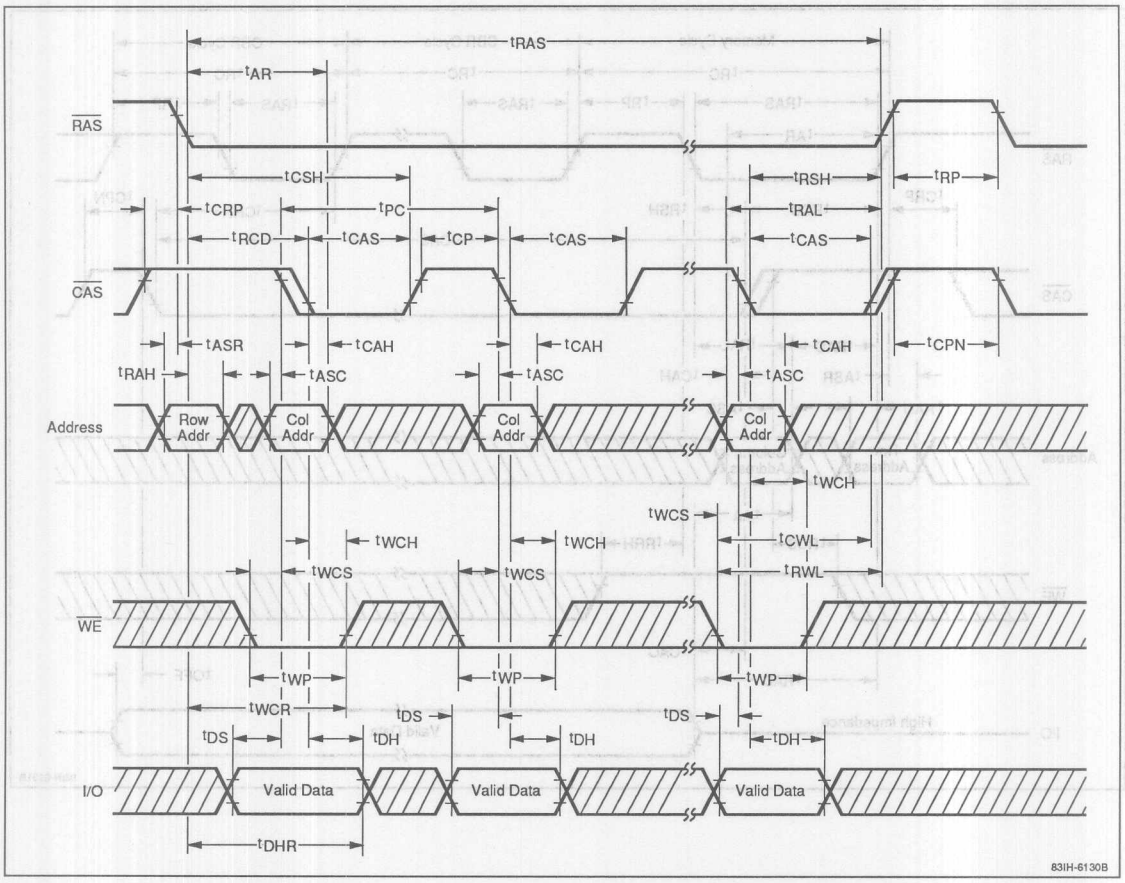
Timing Waveforms (cont)

Fast-Page Read Cycle



Timing Waveforms (cont)

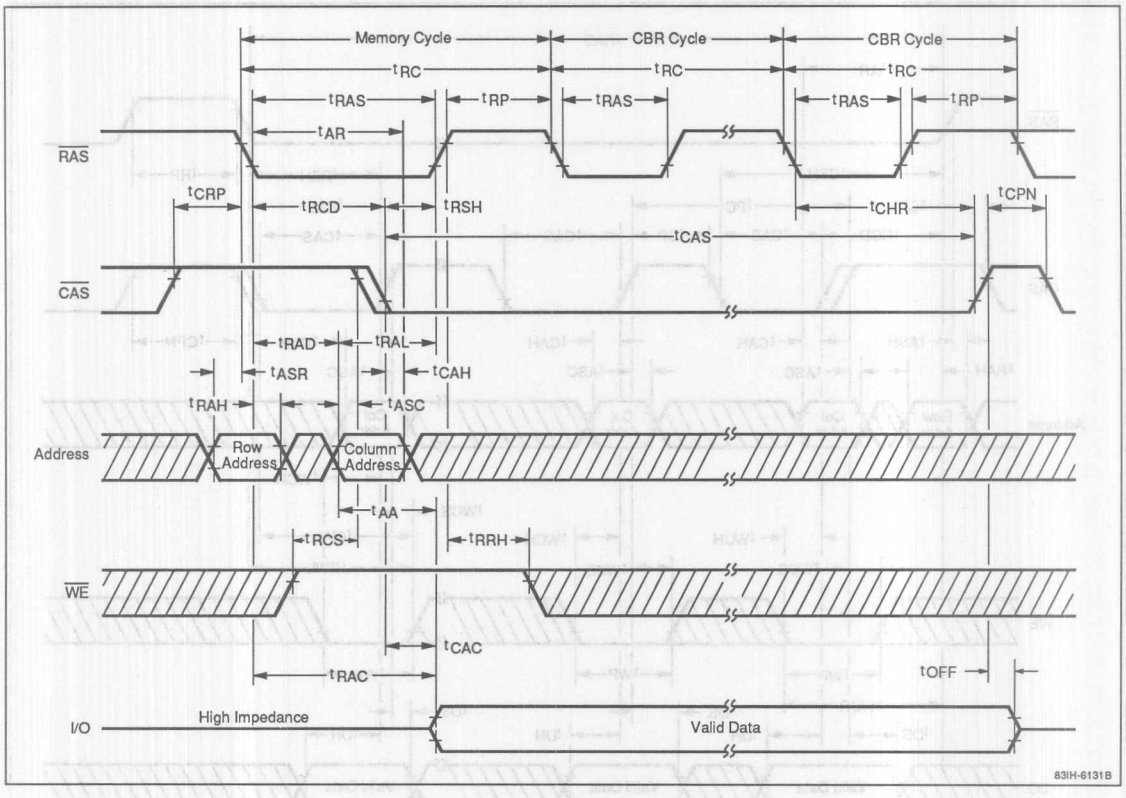
Fast-Page Write Cycle (Early Write)



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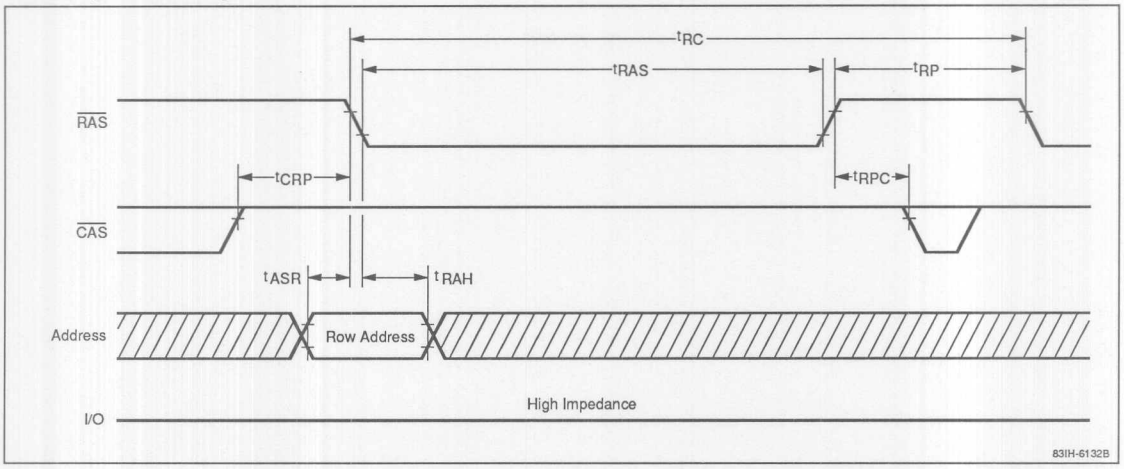
Timing Waveforms (cont)

Hidden Refresh Cycle

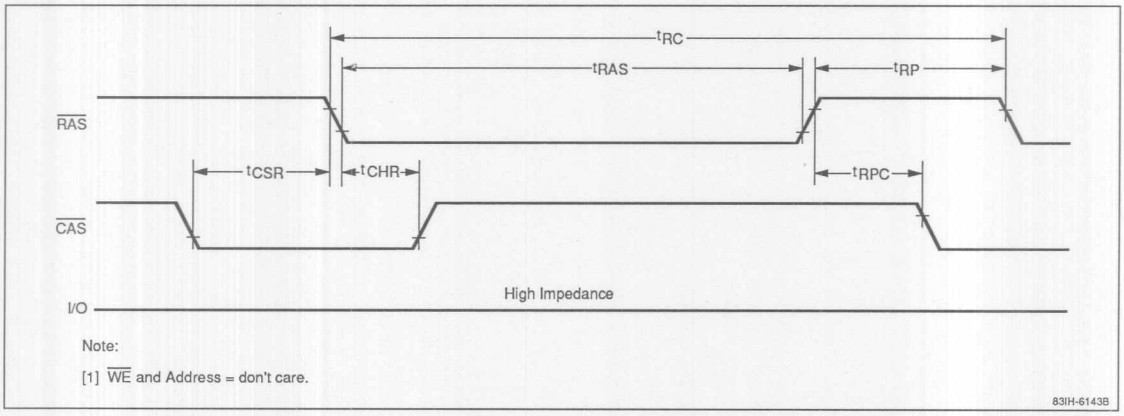


Timing Waveforms (cont)

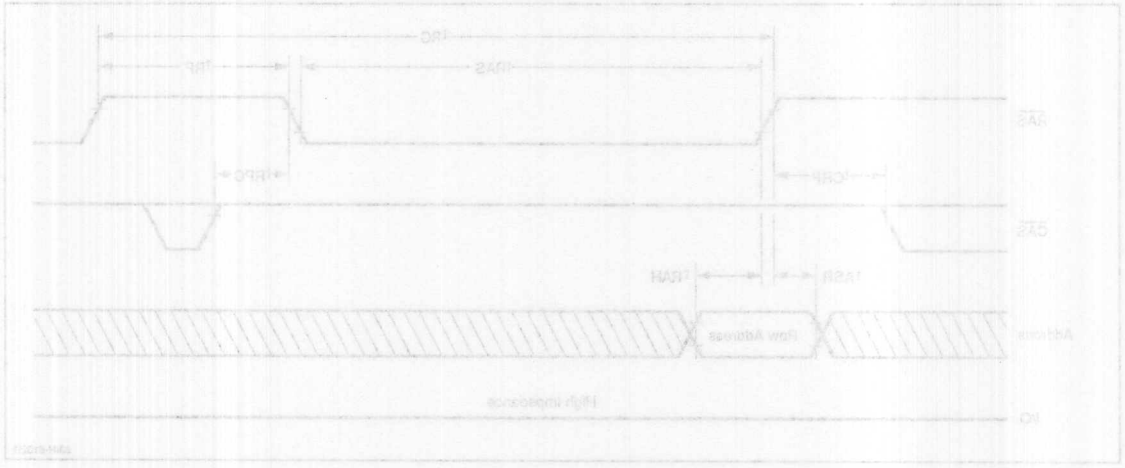
$\overline{RAS}$-Only Refresh Cycle



$\overline{CAS}$ Before $\overline{RAS}$ Refresh Cycle



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MC-41256A8
262,144 x 8-Bit
Dynamic NMOS RAM Module

Description

The MC-41256A8 is a 262,144-word by 8-bit NMOS RAM module designed to operate from a single +5-volt power supply. Advanced dynamic circuitry, including a single-transistor storage cell, 1024 sense amplifiers per data output, multiplexed address buffers and flexible refresh controls, provides good system operating margins.

The MC-41256A8 is functionally equivalent to eight μPD41256 standard 256K DRAMs. Refreshing is accomplished by means of $\overline{RAS}$-only refresh cycles, hidden refresh cycles, $\overline{CAS}$ before $\overline{RAS}$ refresh cycles, or by normal read or write cycles on the 256 address combinations of A_0 through A_7 during a 4-ms period.

Single Inline Memory Module (SIMM™) packaging enhances reliability and reduces the size, weight and cost of a system. The MC-41256A8 includes eight μPD41256s in PLCC packages and eight power supply decoupling capacitors.

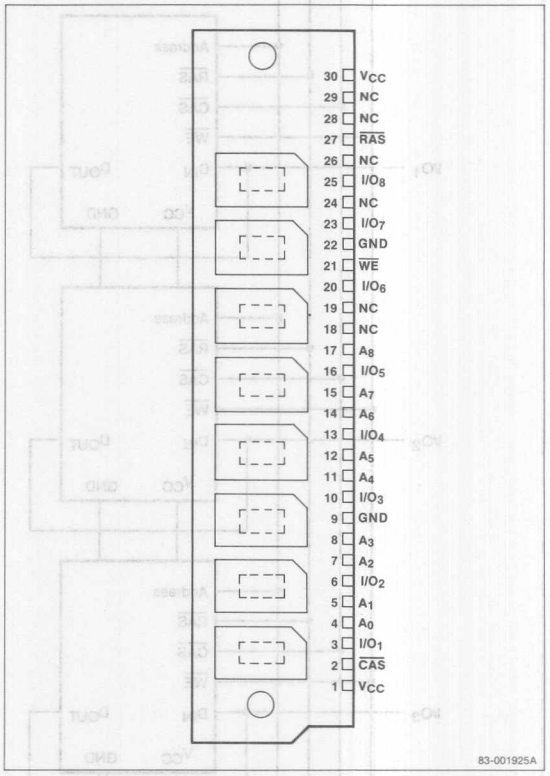
SIMM is a trademark of Wang Laboratories.

Features

- 262,144-word by 8-bit organization
- Single + 5-volt power supply
- Standard 30-pin SIMM packaging
- Eight 256K DRAMs in high-density PLCC packaging
- Eight power supply decoupling capacitors
- Low power dissipation of 220 mW max (standby)
- TTL-compatible inputs and outputs
- 256 refresh cycles every 4 ms
- Page mode

Pin Configuration

30-Pin SIMM

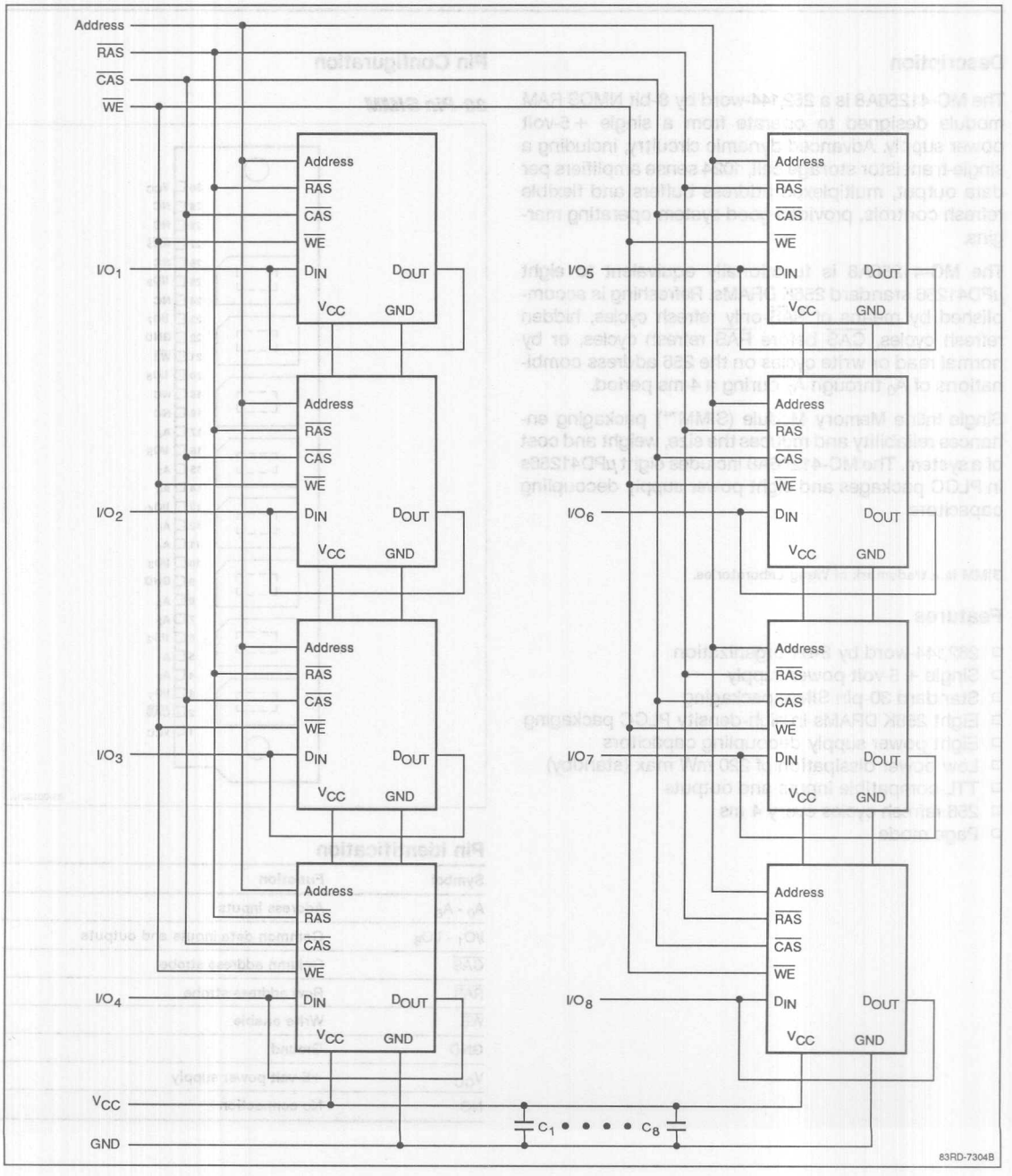


Pin Identification

Symbol	Function
A_0 - A_8	Address inputs
I/O_1 - I/O_8	Common data inputs and outputs
$\overline{CAS}$	Column address strobe
$\overline{RAS}$	Row address strobe
$\overline{WE}$	Write enable
GND	Ground
V_{CC}	+5-volt power supply
NC	No connection

5

Block Diagram



Absolute Maximum Ratings

Voltage on any pin relative to GND, V_T	−1.0 to +7.0 V
Operating temperature, T_{OPR}, ambient	0 to +70°C
Storage temperature, T_{STG}	−55 to +125°C
Short-circuit output current, I_{OS}	50 mA
Power dissipation, P_D	8.0 W

Exposure to Absolute Maximum Ratings for extended periods may affect device reliability; exceeding the ratings could cause permanent damage. The device should be operated within the limits specified under DC and AC Characteristics.

Capacitance

T_A = 25°C; f = 1 MHz

Parameter	Symbol	Max	Unit	Pins Under Test
Input capacitance	C_{IA}	55	pF	A_0 - A_8
	C_{IR}	70	pF	$\overline{RAS}$, $\overline{WE}$
	C_{IC}	70	pF	$\overline{CAS}$
Input/output capacitance	C_{DQ}	17	pF	For I/O_1 - I/O_8: $\overline{CAS}$ = V_{IH} to disable D_{OUT}

Recommended Operating Conditions

Parameter	Symbol	Min	Typ	Max	Unit
Input voltage, high	V_{IH}	2.4		V_{CC} + 1.0	V
Input voltage, low	V_{IL}	−1.0		0.8	V
Supply voltage	V_{CC}	4.5	5.0	5.5	V
Ambient temperature	T_A	0		70	°C

Notes:

(1) V_{CC} = +5.0 V ±5% for the −80 version.

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Ordering Information

Part Number	Access Time (max)	Read/Write Cycle Time (min)	Page Cycle Time (min)	Package
MC-41256A8B-80	80 ns	160 ns	70 ns	30-pin socket-mountable SIMM
B-10	100 ns	200 ns	100 ns	

DC Characteristics

T_A = 0 to +70°C; V_{CC} = +5.0 V ±10%; GND = 0 V

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions
Standby current	I_{CC2}			40.0	mA	$\overline{RAS}$ = V_{IH}; D_{OUT} = high-Z
Input leakage current	I_{IL}	−80		80	μA	V_{IN} = 0 V to V_{CC}; other pins = 0 V
Output leakage current	I_{OL}	−10		10	μA	D_{OUT} disabled; V_{OUT} = 0 V to V_{CC}
Output voltage, low	V_{OL}	0		0.4	V	I_{OUT} = 4.2 mA
Output voltage, high	V_{OH}	2.4		V_{CC}	V	I_{OUT} = −5 mA

Notes:

(1) V_{CC} = +5.0 V ±5% for the −80 version.

AC Characteristics

T_A = 0 to +70°C; V_{CC} = +5.0 V ±10%

		MC-41256A8-80		MC-41256A8-10			
Parameter	Symbol	Min	Max	Min	Max	Unit	Test Conditions
Supply voltage	V_{CC}	4.75	5.25	4.5	5.5	V	
Operating supply current, average	I_{CC1}		720		640	mA	$\overline{RAS}$, $\overline{CAS}$ cycling; t_{RC} = t_{RC} (min); I_O = 0 mA (Note 5)
Operating supply current, $\overline{RAS}$-only refresh cycle, average	I_{CC3}		640		520	mA	$\overline{RAS}$ cycling; $\overline{CAS}$ ≥ V_{IH}; t_{RC} = t_{RC} (min); I_O = 0 mA (Note 5)

AC Characteristics (cont)

Parameter	Symbol	MC-41256A8-80 Min	MC-41256A8-80 Max	MC-41256A8-10 Min	MC-41256A8-10 Max	Unit	Test Conditions
Operating supply current, page cycle, average	I_{CC4}		560		480	mA	$\overline{RAS} \le V_{IL}$; $\overline{CAS}$ cycling; $t_{PC} = t_{PC}$ (min); $I_O = 0$ mA (Note 5)
Operating current, $\overline{CAS}$ before $\overline{RAS}$ refresh cycle, average	I_{CC5}		640		520	mA	$\overline{CAS} \le V_{IL}$; $\overline{RAS}$ cycling; $t_{RC} = t_{RC}$ (min); I/O = 0 mA (Note 5)
Random read or write cycle time	t_{RC}	180		200		ns	(Note 6)
Page cycle time	t_{PC}	70		100		ns	(Note 6)
Access time from $\overline{RAS}$	t_{RAC}		80		100	ns	(Notes 7, 8)
Access time from $\overline{CAS}$	t_{CAC}		40		50	ns	(Notes 7, 9)
Output buffer turnoff delay	t_{OFF}	0	20	0	25	ns	(Note 10)
Rise and fall transition time	t_T	3	50	3	50	ns	(Note 4)
$\overline{RAS}$ precharge time	t_{RP}	70		90		ns	
$\overline{RAS}$ pulse width	t_{RAS}	80	16,000	100	10,000	ns	
$\overline{RAS}$ hold time	t_{RSH}	40		50		ns	
$\overline{CAS}$ pulse width	t_{CAS}	40	10,000	50	10,000	ns	
$\overline{CAS}$ hold time	t_{CSH}	80		100		ns	
$\overline{RAS}$ to $\overline{CAS}$ delay time	t_{RCD}	20	40	20	50	ns	(Note 11)
$\overline{CAS}$ to $\overline{RAS}$ precharge time	t_{CRP}	10		10		ns	(Note 12)
$\overline{CAS}$ precharge time, nonpage cycle	t_{CPN}	25		25		ns	
$\overline{CAS}$ precharge time, page cycle	t_{CP}	20		40		ns	
$\overline{RAS}$ precharge $\overline{CAS}$ hold time	t_{RPC}	0		0		ns	
Row address setup time	t_{ASR}	0		0		ns	
Row address hold time	t_{RAH}	10		10		ns	
Column address setup time	t_{ASC}	0		0		ns	
Column address hold time	t_{CAH}	15		15		ns	
Column address hold time referenced to $\overline{RAS}$	t_{AR}	55		65		ns	
Read command setup time	t_{RCS}	0		0		ns	
Read command hold time referenced to $\overline{RAS}$	t_{RRH}	10		10		ns	(Note 13)
Read command hold time referenced to $\overline{CAS}$	t_{RCH}	0		0		ns	(Note 13)
Write command hold time	t_{WCH}	20		25		ns	
Write command hold time referenced to $\overline{RAS}$	t_{WCR}	60		75		ns	
Write command pulse width	t_{WP}	20		15		ns	
Write command to $\overline{RAS}$ lead time	t_{RWL}	20		35		ns	
Write command to $\overline{CAS}$ lead time	t_{CWL}	20		35		ns	
Data-in setup time	t_{DS}	0		0		ns	(Note 14)
Data-in hold time	t_{DH}	20		25		ns	(Note 14)
Data-in hold time referenced to $\overline{RAS}$	t_{DHR}	60		75		ns	

AC Characteristics (cont)

Parameter	Symbol	MC-41256A8-80 Min	MC-41256A8-80 Max	MC-41256A8-10 Min	MC-41256A8-10 Max	Unit	Test Conditions
Refresh period	t_{REF}		4		4	ms	Addresses A_0 - A_7
$\overline{WE}$ command setup time	t_{WCS}	0		0		ns	
$\overline{CAS}$ setup time for $\overline{CAS}$ before $\overline{RAS}$ refresh cycle	t_{CSR}	10		10		ns	
$\overline{CAS}$ hold time for $\overline{CAS}$ before $\overline{RAS}$ refresh cycle	t_{CHR}	20		20		ns	

Notes:

(1) All voltages are referenced to GND.

(2) An initial pause of 100 μs is required after power-up, followed by any eight $\overline{RAS}$ cycles, before proper device operation is achieved.

(3) AC measurements assume t_T = 5 ns.

(4) V_{IH} (min) and V_{IL} (max) are reference levels for measuring the timing of input signals. Transition times are measured between V_{IH} and V_{IL}.

(5) I_{CC1}, I_{CC3}, I_{CC4}, and I_{CC5} depend on output loading and cycle rates. Specified values are obtained with the output open.

(6) The minimum specifications are used only to indicate the cycle time at which proper operation over the full temperature range (T_A = 0 to +70°C) is assured.

(7) Output load = 2 TTL loads and 100 pF.

(8) Assumes that $t_{RCD} \leq t_{RCD}$ (max). If t_{RCD} is greater than the maximum recommended value shown in this table, t_{RAC} will increase by the amount that t_{RCD} exceeds the value shown.

(9) Assumes that $t_{RCD} \geq t_{RCD}$ (max).

(10) t_{OFF} (max) defines the time at which the output achieves the open-circuit condition and is not referenced to V_{OH} or V_{OL}.

(11) Operation within the t_{RCD} (max) limit assures that t_{RAC} (max) can be met. t_{RCD} (max) is specified as a reference point only. If t_{RCD} is greater than the specified t_{RCD} (max) limit, then access time is controlled exclusively by t_{CAC}.

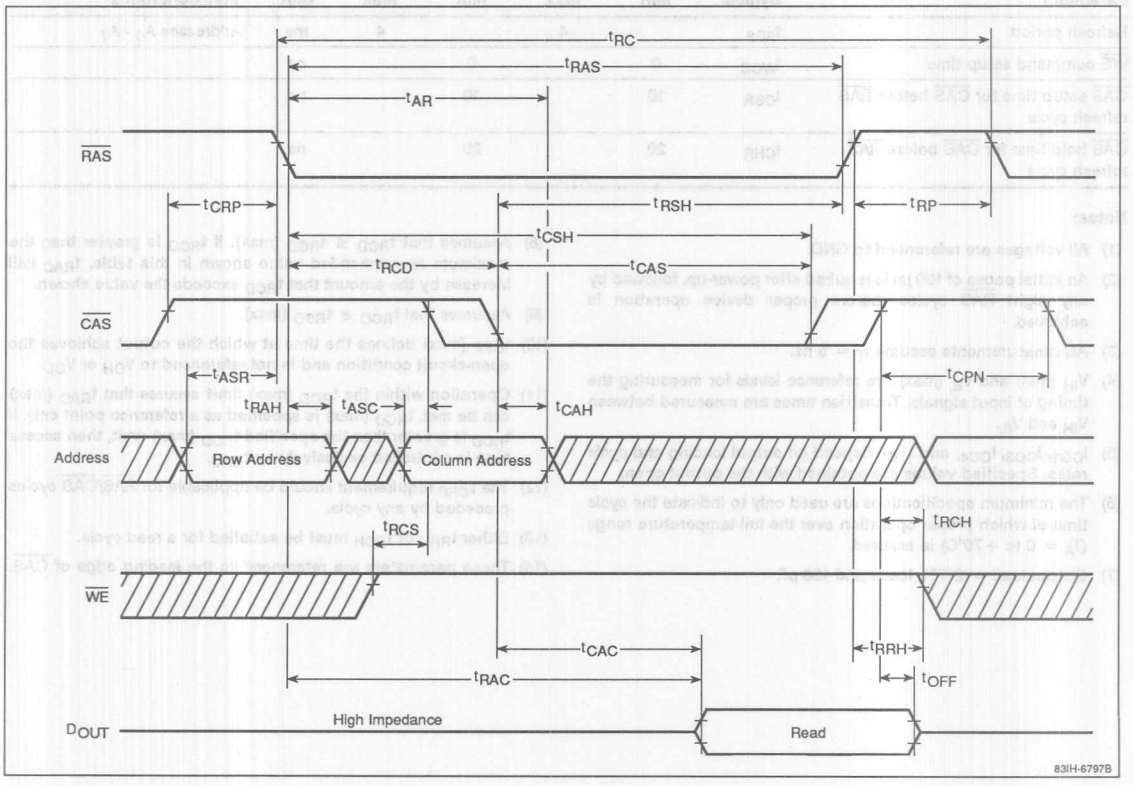
(12) The t_{CRP} requirement should be applicable for $\overline{RAS}$/$\overline{CAS}$ cycles preceded by any cycle.

(13) Either t_{RRH} or t_{RCH} must be satisfied for a read cycle.

(14) These parameters are referenced to the leading edge of $\overline{CAS}$.

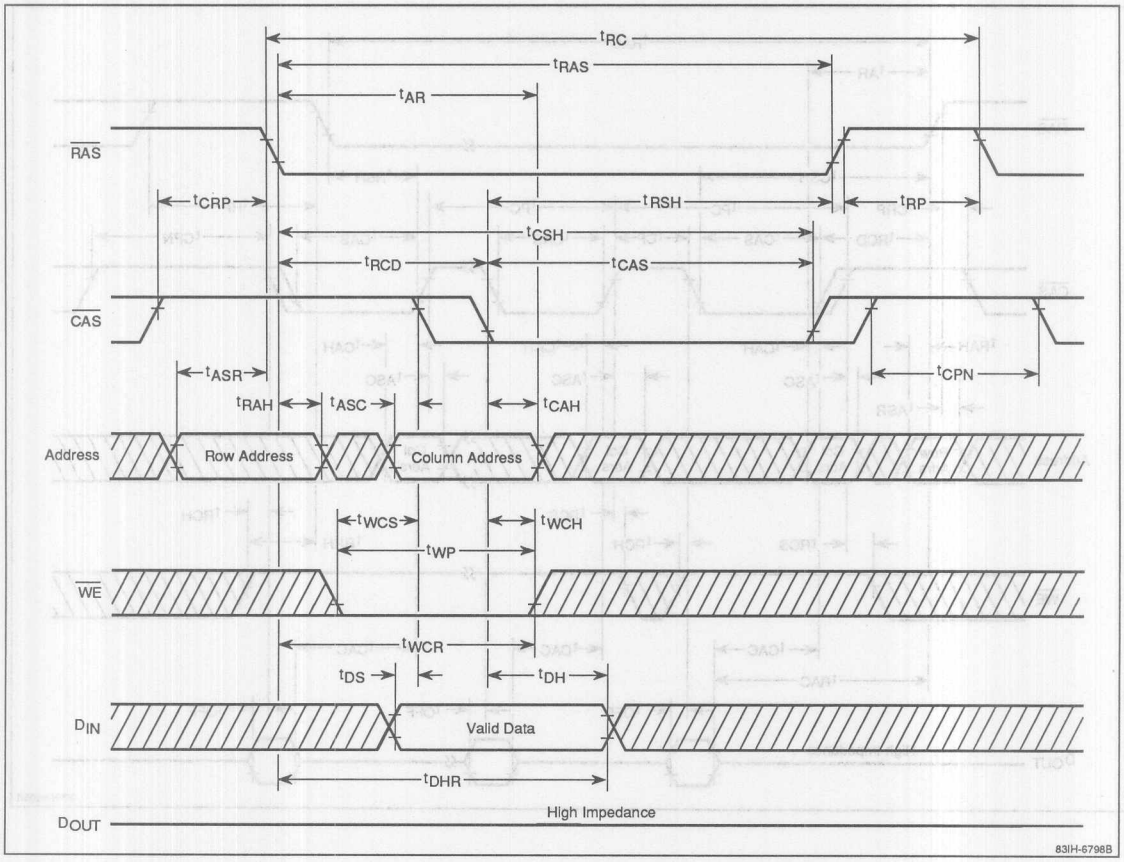
Timing Waveforms

Read Cycle



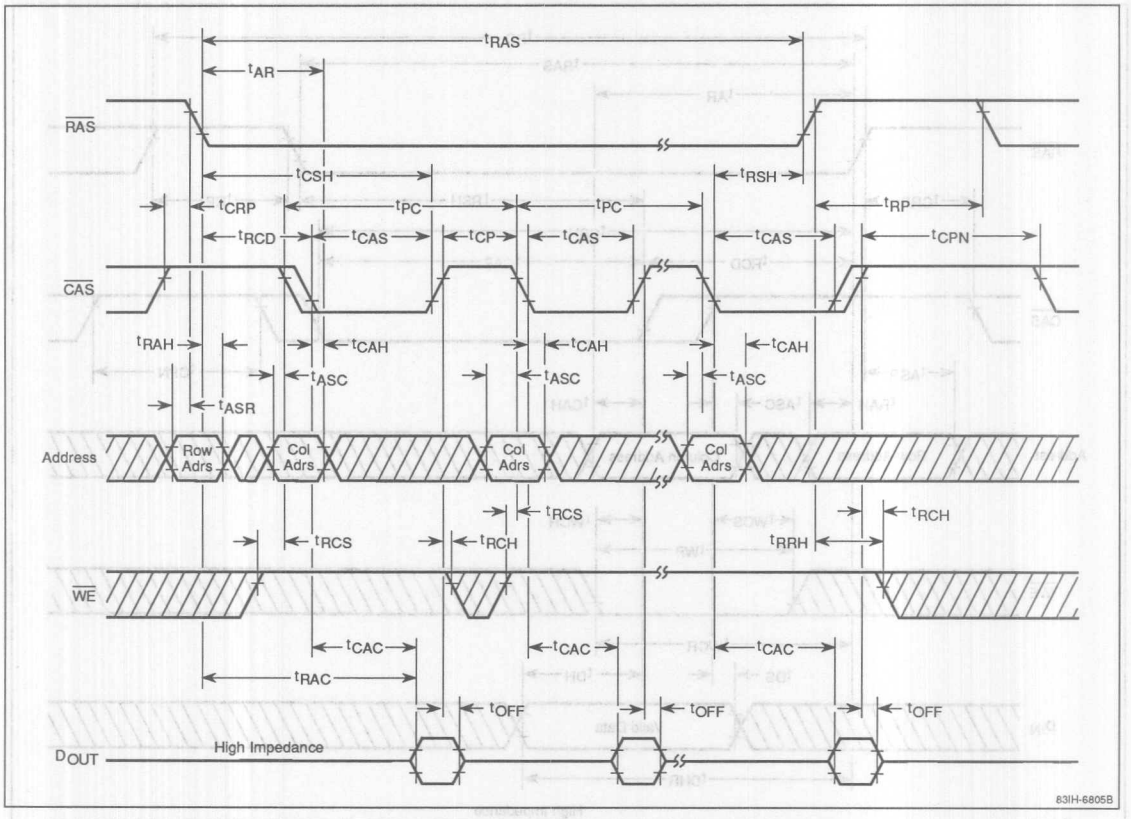
Timing Waveforms (cont)

Early Write Cycle



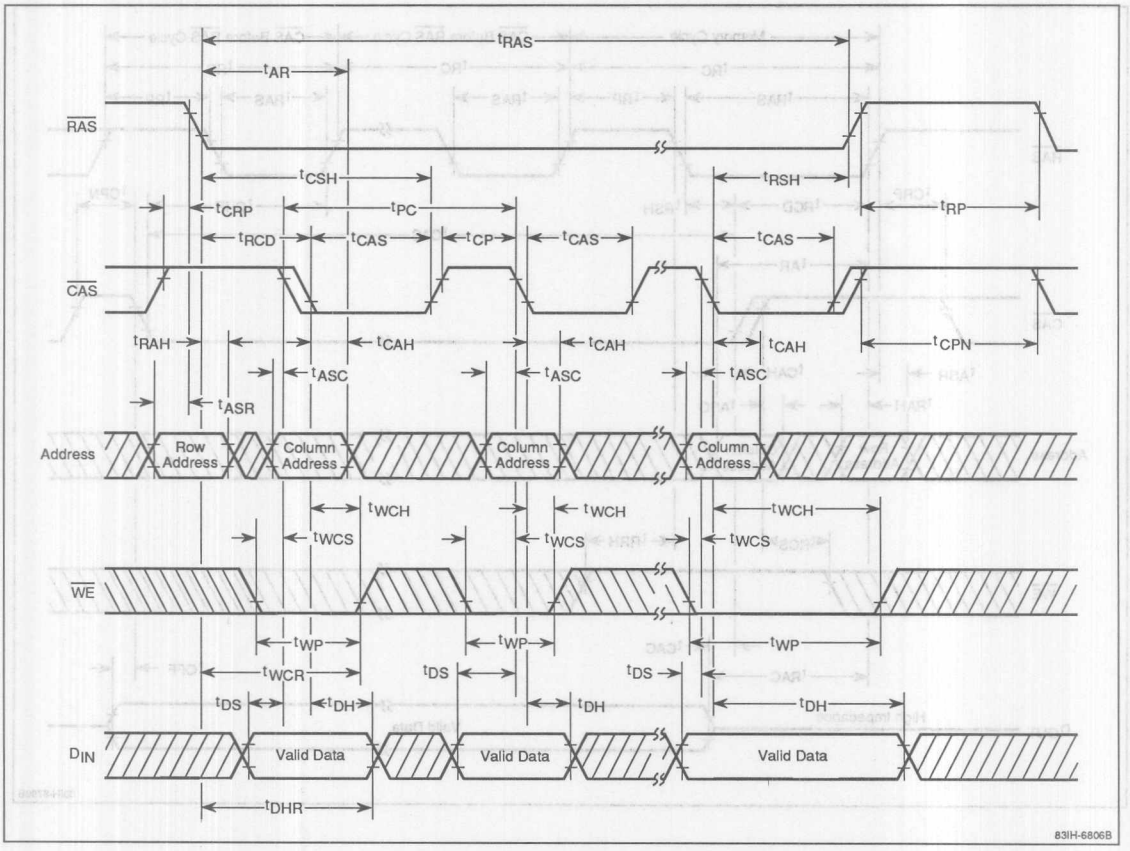
Timing Waveforms (cont)

Page Read Cycle



Timing Waveforms (cont)

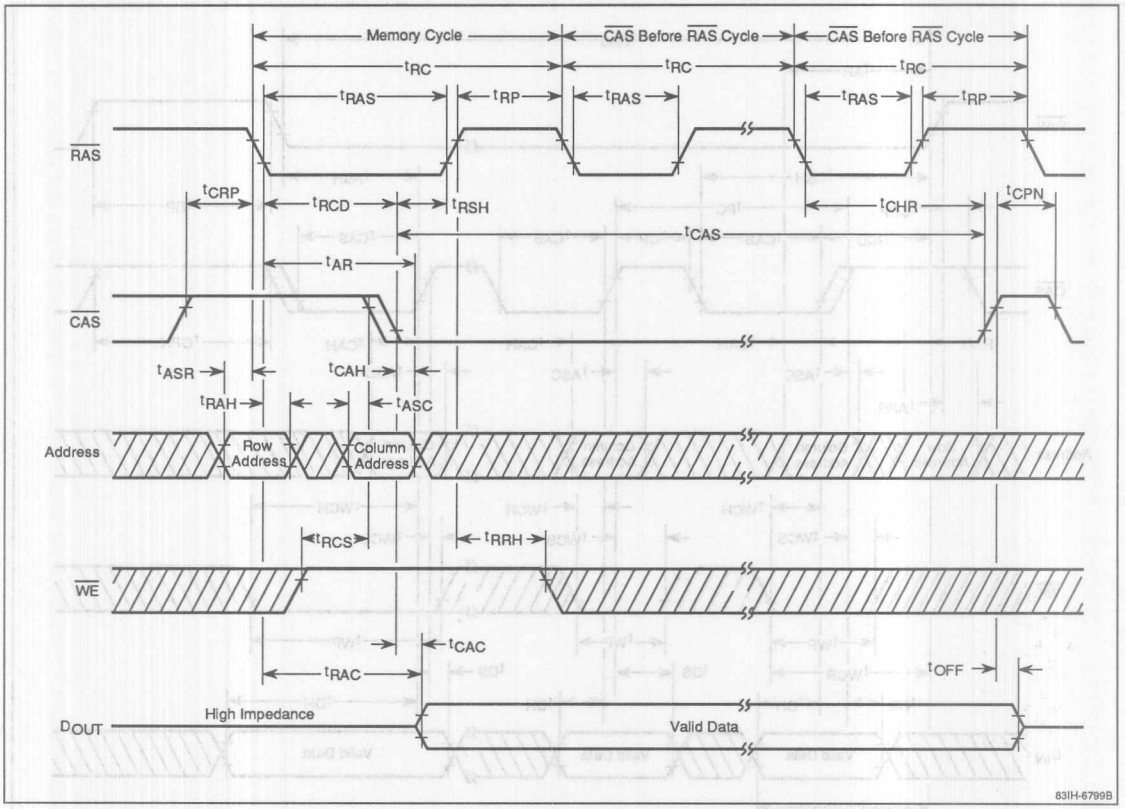
Page Early Write Cycle



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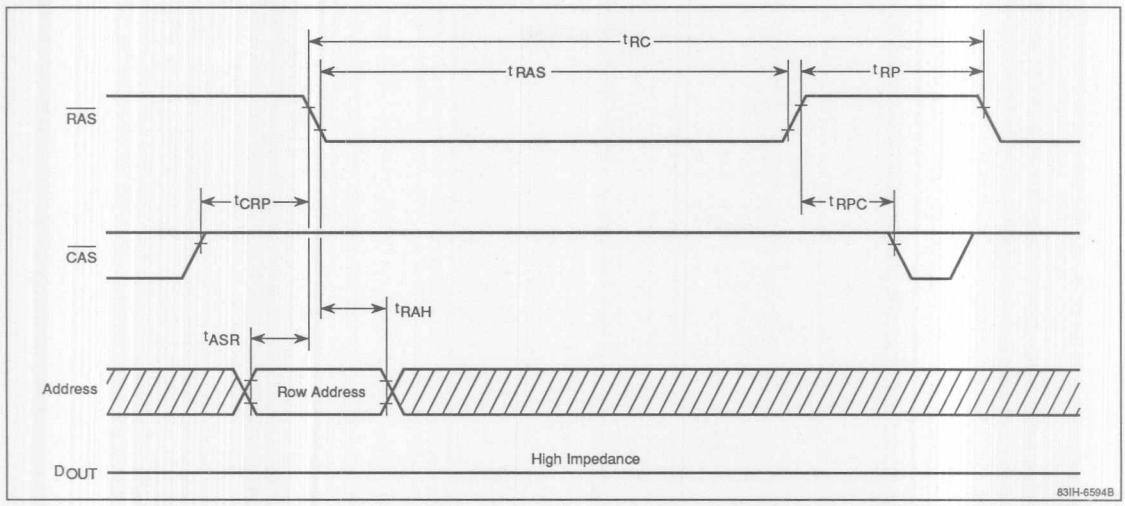
Timing Waveforms (cont)

Hidden Refresh Cycle

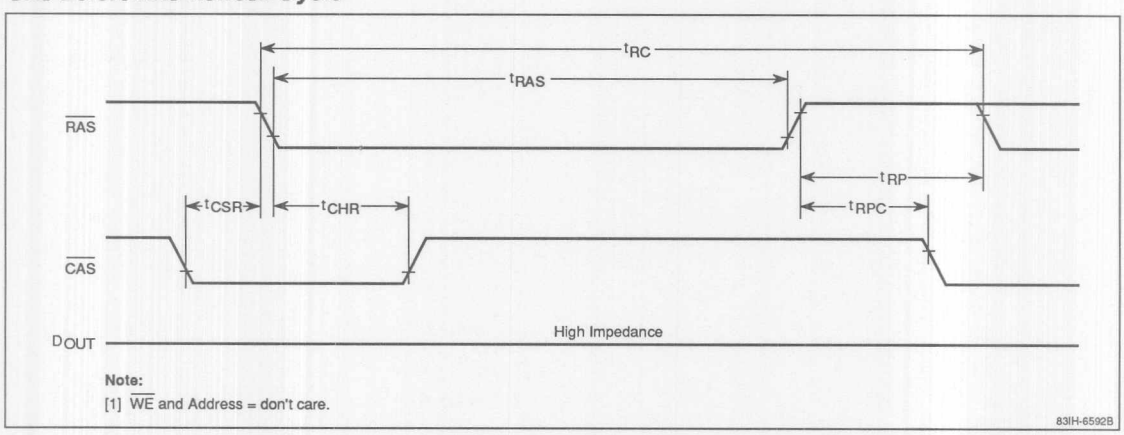


Timing Waveforms (cont)

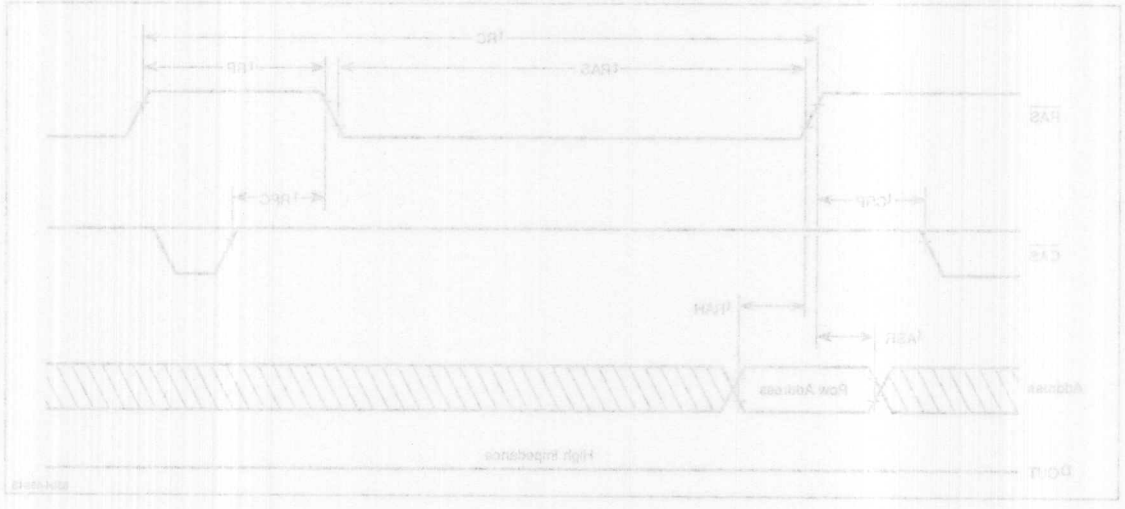
$\overline{RAS}$-Only Refresh Cycle

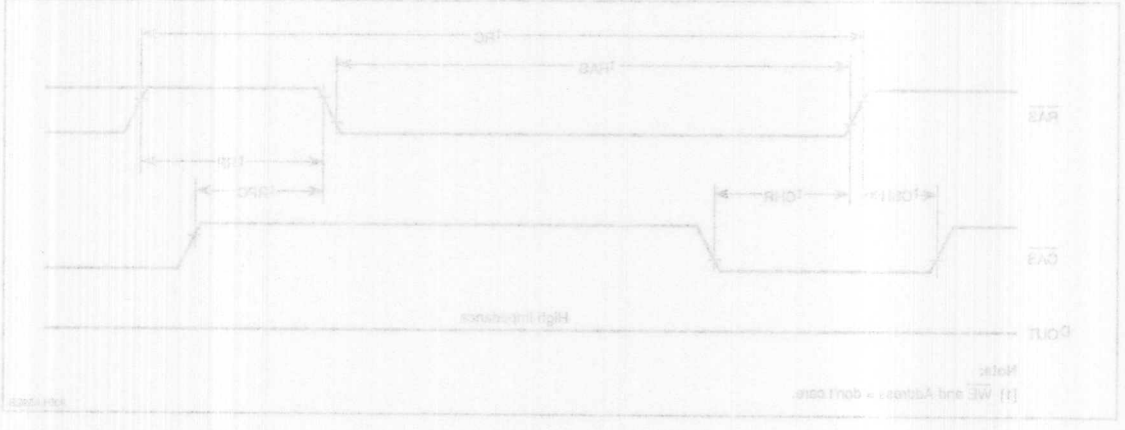


$\overline{CAS}$ Before $\overline{RAS}$ Refresh Cycle



5





NEC Electronics Inc.

MC-421000A8
1,048,576 x 8-Bit
CMOS Dynamic RAM Module

Description

The MC-421000A8 is a fast-page 1,048,576-word by 8-bit CMOS dynamic RAM module designed to operate from a single +5-volt power supply. Advanced CMOS circuitry, including a single-transistor storage cell, 2048 sense amplifiers per data output, multiplexed address buffers and flexible refresh controls, provides good system operating margins.

The MC-421000A8 is functionally equivalent to eight μPD421000 standard 1M DRAMs. Refreshing is accomplished by means of $\overline{RAS}$-only refresh cycles, hidden refresh cycles, $\overline{CAS}$ before $\overline{RAS}$ refresh cycles, or normal read or write cycles on the 512 address combinations of A_0-A_8 during an 8-ms period.

Packaged in a Single Inline Memory Module (SIMM™) to enhance reliability and reduce the size, weight and cost of a system, the MC-421000A8 includes eight μPD421000s in SOJ packages and eight power supply decoupling capacitors.

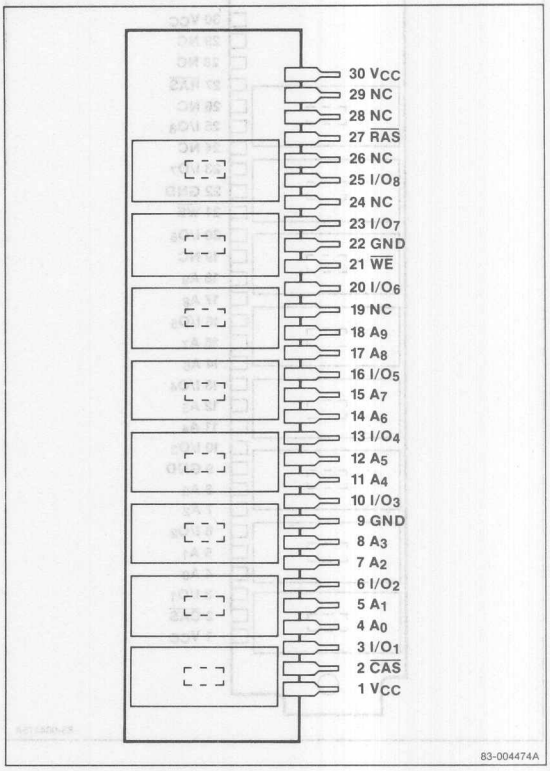
SIMM is a trademark of Wang Laboratories.

Features

- ☐ 1,048,576-word by 8-bit organization
- ☐ Single +5-volt ± 10% power supply
- ☐ Standard 30-pin Single Inline Memory Module (SIMM) packaging
- ☐ Eight 1M dynamic RAMs incorporated in high-density SOJ packaging (μPD421000LA)
- ☐ Eight power supply decoupling capacitors
- ☐ Low power dissipation: 44 mW standby (max)
- ☐ TTL-compatible inputs and outputs
- ☐ 512 refresh cycles (A_0-A_8 are refresh address pins)
- ☐ Fast-page capability

Pin Configurations

30-Pin SIMM, MC-421000A8A



Ordering Information

Part Number	Column Access Time (max)	Row Access Time (max)	Fast-Page Cycle Time (min)	Package
MC-421000A8A-70	70 ns	20 ns	45 ns	30-pin leaded SIMM
A-80	80 ns	20 ns	50 ns	
A-10	100 ns	25 ns	60 ns	
A-12	120 ns	30 ns	70 ns	
MC-421000A8B-70	70 ns	20 ns	45 ns	30-pin socketable SIMM
B-80	80 ns	20 ns	50 ns	
B-10	100 ns	25 ns	60 ns	
B-12	120 ns	30 ns	70 ns	

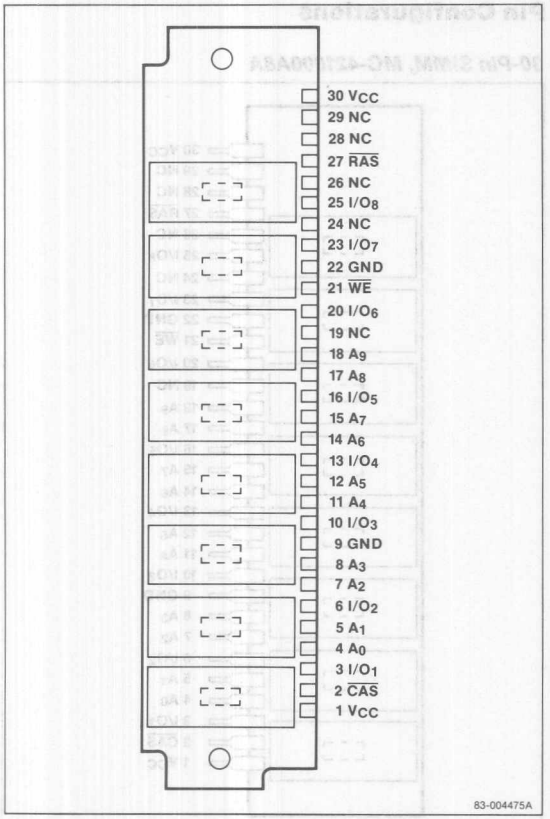
Notes:

(1) Contact your NEC sales representative for a copy of the MC-421000A8A-70 and MC-421000A9B-70 data sheets.

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Pin Configurations (cont)

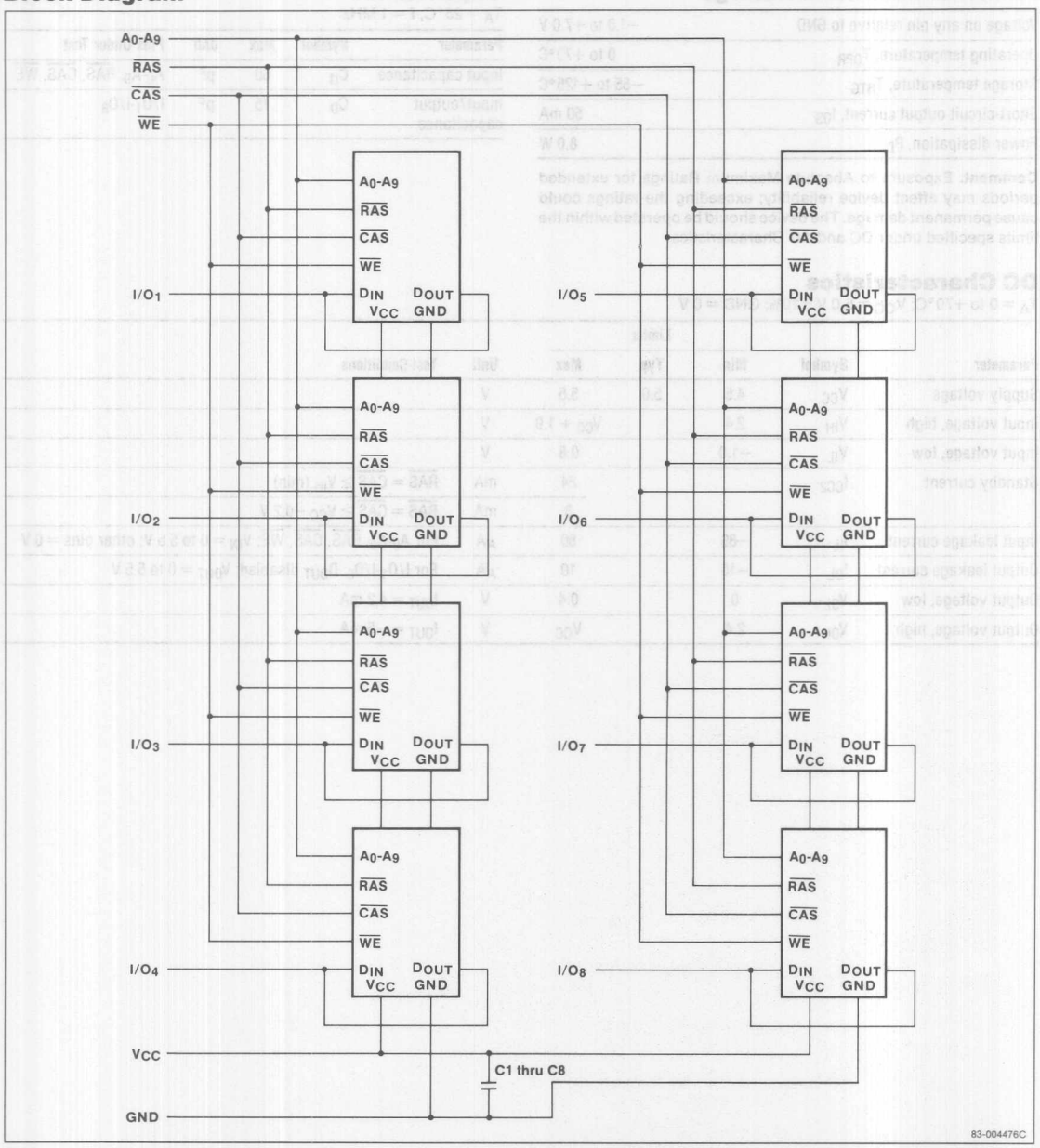
30-Pin SIMM, MC-421000A8B



Pin Identification

Symbol	Function
A_0-A_9	Address inputs
I/O_1-I/O_8	Common data inputs/outputs
$\overline{RAS}$	Row address strobe
$\overline{CAS}$	Column address strobe
$\overline{WE}$	Write enable
GND	Ground
V_{CC}	+5-volt power supply
NC	No connection

Block Diagram



Absolute Maximum Ratings

Voltage on any pin relative to GND	−1.0 to +7.0 V
Operating temperature, T_{OPR}	0 to +70 °C
Storage temperature, T_{STG}	−55 to +125 °C
Short-circuit output current, I_{OS}	50 mA
Power dissipation, P_D	8.0 W

Comment: Exposure to Absolute Maximum Ratings for extended periods may affect device reliability; exceeding the ratings could cause permanent damage. The device should be operated within the limits specified under DC and AC Characteristics.

Capacitance

$T_A = 25$ °C; f = 1 MHz

Parameter	Symbol	Max	Unit	Pins Under Test
Input capacitance	C_{I1}	60	pF	A_0-A_9, $\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$
Input/output capacitance	C_D	15	pF	I/O_1-I/O_8

DC Characteristics

$T_A = 0$ to +70 °C; $V_{CC} = 5.0$ V ±10%; GND = 0 V

		Limits				
Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions
Supply voltage	V_{CC}	4.5	5.0	5.5	V	
Input voltage, high	V_{IH}	2.4		V_{CC} + 1.0	V	
Input voltage, low	V_{IL}	−1.0		0.8	V	
Standby current	I_{CC2}			24	mA	$\overline{RAS} = \overline{CAS} \geq V_{IH}$ (min)
				8	mA	$\overline{RAS} = \overline{CAS} \geq V_{CC}$ −0.2 V
Input leakage current	I_{IL}	−80		80	μA	For A_0-A_9, $\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$: V_{IN} = 0 to 5.5 V; other pins = 0 V
Output leakage current	I_{OL}	−10		10	μA	For I/O_1-I/O_8: D_{OUT} disabled; V_{OUT} = 0 to 5.5 V
Output voltage, low	V_{OL}	0		0.4	V	I_{OUT} = 4.2 mA
Output voltage, high	V_{OH}	2.4		V_{CC}	V	I_{OUT} = −5 mA

AC Characteristics

$T_A = 0$ to $+70°C$; $V_{CC} = 5.0\ V \pm 10\%$

		Limits							
		MC-421000A8-80		MC-421000A8-10		MC-421000A8-12			
Parameter	Symbol	Min	Max	Min	Max	Min	Max	Unit	Test Conditions
Operating current, average	I_{CC1}		560		480		400	mA	$\overline{RAS}$, $\overline{CAS}$ cycling; $t_{RC} = t_{RC}$ min (Note 5)
Refresh operating current, average	I_{CC3}		560		480		400	mA	$\overline{RAS}$ cycling; $\overline{CAS} \geq V_{IH}$; $t_{RC} = t_{RC}$ min; $I_O = 0$ mA (Note 5)
Fast-page operating current, average	I_{CC4}		480		400		320	mA	$\overline{RAS} \leq V_{IL}$; $\overline{CAS}$ cycling; $t_{PC} = t_{PC}$ min; $I_O = 0$ mA (Note 5)
Operating current, $\overline{CAS}$ before $\overline{RAS}$ refreshing, average	I_{CC5}		560		480		400	mA	$t_{RC} = t_{RC}$ min; $I_O = 0$ mA (Note 5)
Random read or write cycle time	t_{RC}	160		190		220		ns	(Note 6)
Fast-page cycle time	t_{PC}	50		60		70		ns	(Note 6)
Refresh period	t_{REF}		8		8		8	ms	
Access time from $\overline{RAS}$	t_{RAC}		80		100		120	ns	(Notes 7, 8)
Access time from $\overline{CAS}$ (falling edge)	t_{CAC}		20		25		30	ns	(Notes 7, 9, 10, 11)
Access time from column address	t_{AA}		45		50		60	ns	(Notes 7, 10, 11)
Access time from $\overline{CAS}$ precharge (rising edge)	t_{ACP}		45		55		65	ns	(Notes 7, 11)
Output buffer turnoff delay	t_{OFF}	0	20	0	25	0	30	ns	(Note 12)
Transition time (rise and fall)	t_T	3	50	3	50	3	50	ns	(Note 4)
$\overline{RAS}$ precharge time	t_{RP}	70		80		90		ns	
$\overline{RAS}$ pulse width	t_{RAS}	80	10000	100	10000	120	10000	ns	
Fast-page $\overline{RAS}$ pulse width	t_{RASP}	80	100000	100	100000	120	100000	ns	
$\overline{RAS}$ hold time	t_{RSH}	20		25		30		ns	
$\overline{CAS}$ pulse width	t_{CAS}	20	10000	25	10000	30	10000	ns	
$\overline{CAS}$ hold time	t_{CSH}	80		100		120		ns	
$\overline{RAS}$ to $\overline{CAS}$ delay time	t_{RCD}	25	60	25	75	25	90	ns	(Note 13)
$\overline{CAS}$ to $\overline{RAS}$ precharge time	t_{CRP}	10		10		10		ns	(Note 14)
$\overline{CAS}$ precharge time (non-page cycle)	t_{CPN}	10		10		15		ns	
Fast-page $\overline{CAS}$ precharge time	t_{CP}	10	20	10	25	15	30	ns	(Note 11)
$\overline{RAS}$ precharge $\overline{CAS}$ hold time	t_{RPC}	0		0		0		ns	
Row address setup time	t_{ASR}	0		0		0		ns	
Row address hold time	t_{RAH}	12		12		15		ns	
$\overline{RAS}$ to column address delay time	t_{RAD}	17	35	17	50	20	60	ns	(Note 10)
Column address setup time	t_{ASC}	0	20	0	20	0	25	ns	(Note 11)
Column address hold time	t_{CAH}	20		20		25		ns	
Column address hold time referenced to $\overline{RAS}$	t_{AR}	60		70		85		ns	

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AC Characteristics (cont)

T_A = 0 to +70°C; V_{CC} = 5.0 V ±10%

		Limits							
		MC-421000A8-80		MC-421000A8-10		MC-421000A8-12			
Parameter	Symbol	Min	Max	Min	Max	Min	Max	Unit	Test Conditions
Column address lead time referenced to $\overline{RAS}$ (rising edge)	t_{RAL}	45		55		65		ns	
Read command setup time	t_{RCS}	0		0		0		ns	
Read command hold time referenced to $\overline{RAS}$	t_{RRH}	10		10		10		ns	(Note 15)
Read command hold time referenced to $\overline{CAS}$	t_{RCH}	0		0		0		ns	(Note 15)
Write command hold time	t_{WCH}	15		20		25		ns	
Write command hold time referenced to $\overline{RAS}$	t_{WCR}	55		70		85		ns	
Write command pulse width	t_{WP}	15		20		25		ns	(Note 16)
Write command to $\overline{RAS}$ lead time	t_{RWL}	25		30		35		ns	
Write command to $\overline{CAS}$ lead time	t_{CWL}	15		20		25		ns	
Data-in setup time	t_{DS}	0		0		0		ns	(Note 17)
Data-in hold time	t_{DH}	20		20		25		ns	(Note 17)
Data-in hold time referenced to $\overline{RAS}$	t_{DHR}	60		70		85		ns	
Write command setup time	t_{WCS}	0		0		0		ns	
$\overline{CAS}$ setup time for $\overline{CAS}$ before $\overline{RAS}$ refreshing	t_{CSR}	10		10		10		ns	(Note 18)
$\overline{CAS}$ hold time for $\overline{CAS}$ before $\overline{RAS}$ refreshing	t_{CHR}	15		20		25		ns	(Note 18)

Notes:

(1) All voltages are referenced to GND.

(2) An initial pause of 100 μs is required after power-up, followed by any eight $\overline{RAS}$ cycles before proper device operation is achieved.

(3) Ac measurements assume t_T = 5 ns.

(4) V_{IH} (min) and V_{IL} (max) are reference levels for measuring timing of input signals. Transition times are measured between V_{IH} and V_{IL}.

(5) I_{CC1}, I_{CC3}, I_{CC4}, and I_{CC5} depend on output loading and cycle rates. Specified values are obtained with the output open. I_{CC3} is measured assuming that all column address inputs are held at either a high level or a low level during $\overline{RAS}$-only refresh cycles. I_{CC4} is measured assuming that all column address inputs are switched only once each fast-page cycle.

(6) The minimum specifications are used only to indicate the cycle time at which proper operation over the full temperature range (T_A = 0 to +70°C) is assured.

(7) Load = 2 TTL (−1 mA, +4 mA) loads and 100 pF (V_{OH} = 2.0 V, V_{OL} = 0.8 V).

(8) Assumes that $t_{RCD} \leq t_{RCD}$ (max) and $t_{RAD} \leq t_{RAD}$ (max). If t_{RCD} or t_{RAD} is greater than the maximum recommended value in this table, t_{RAC} increases by the amount that t_{RCD} or t_{RAD} exceeds the value shown.

(9) Assumes that $t_{RCD} \geq t_{RCD}$ (max) and $t_{RAD} \leq t_{RAD}$ (max).

Notes [cont]:

(10) If $t_{RAD} \geq t_{RAD}$ (max), then the access time is defined by t_{AA}.

(11) For fast-page read operation, the definition of access time is as follows.

$\overline{CAS}$ and Column Address Input Conditions	Access Time Definition
$t_{CP} \leq t_{CP}$ (max), $t_{ASC} \geq t_{CP}$	t_{ACP}
$t_{CP} \leq t_{CP}$ (max), $t_{ASC} \leq t_{CP}$	t_{AA}
$t_{CP} \geq t_{CP}$ (max), $t_{ASC} \leq t_{ASC}$ (max)	t_{AA}
$t_{CP} \geq t_{CP}$ (max), $t_{ASC} \geq t_{ASC}$ (max)	t_{CAC}

(12) t_{OFF} (max) defines the time at which the output achieves the open-circuit condition and is not referenced to V_{OH} or V_{OL}.

(13) Operation within the t_{RCD} (max) limit assures that t_{RAC} (max) can be met. t_{RCD} (max) is specified as a reference point only; if t_{RCD} is greater than t_{RCD} (max), access time is controlled exclusively by t_{CAC}.

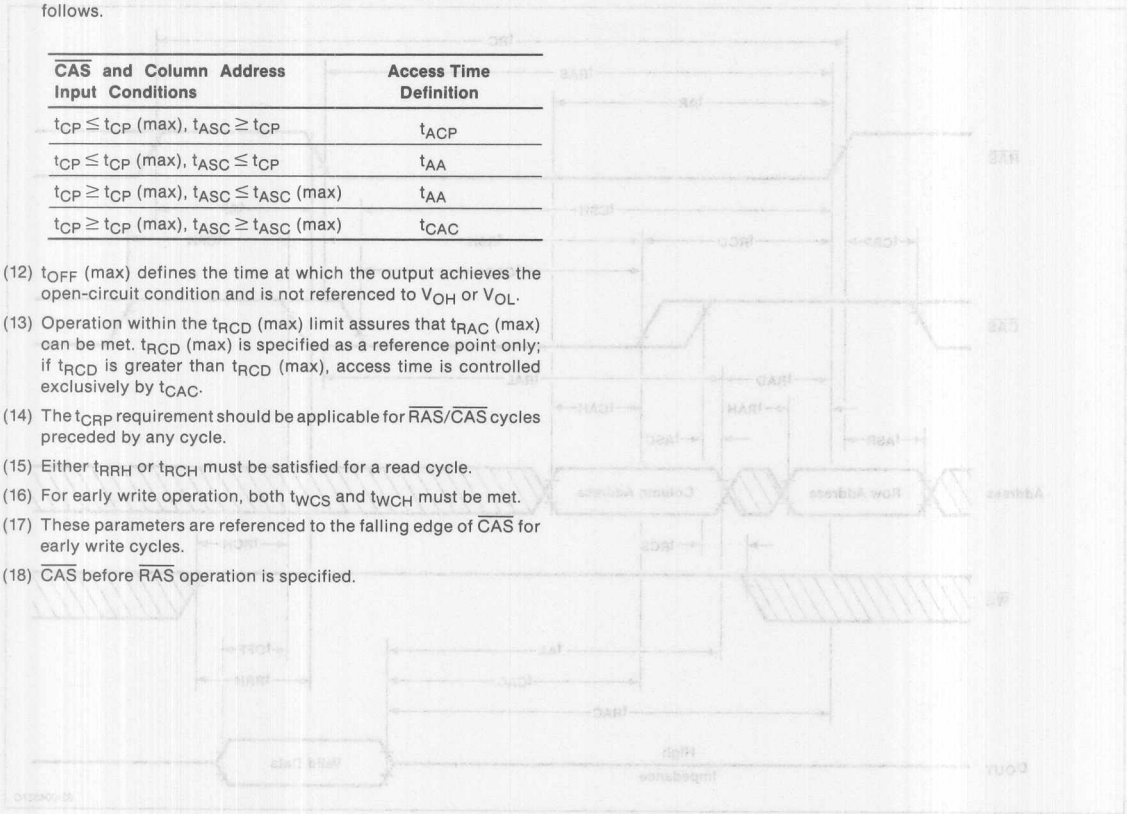
(14) The t_{CRP} requirement should be applicable for $\overline{RAS}$/$\overline{CAS}$ cycles preceded by any cycle.

(15) Either t_{RRH} or t_{RCH} must be satisfied for a read cycle.

(16) For early write operation, both t_{WCS} and t_{WCH} must be met.

(17) These parameters are referenced to the falling edge of $\overline{CAS}$ for early write cycles.

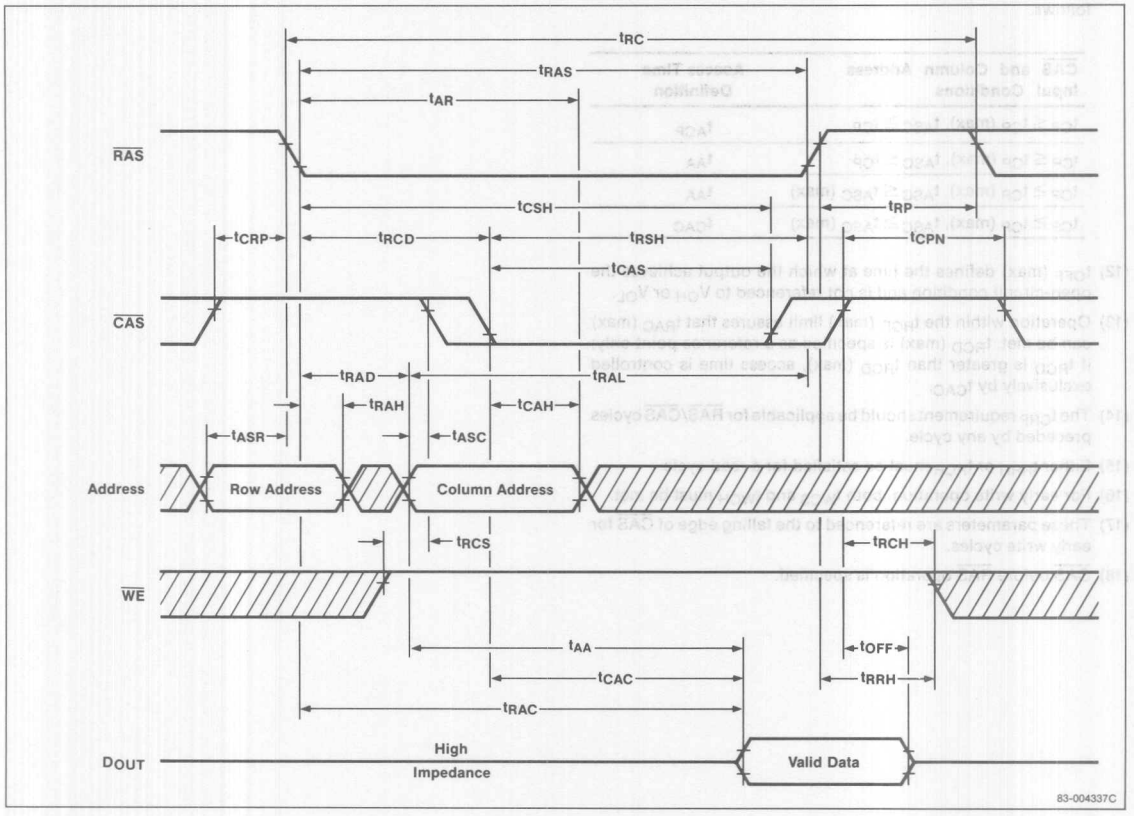
(18) $\overline{CAS}$ before $\overline{RAS}$ operation is specified.



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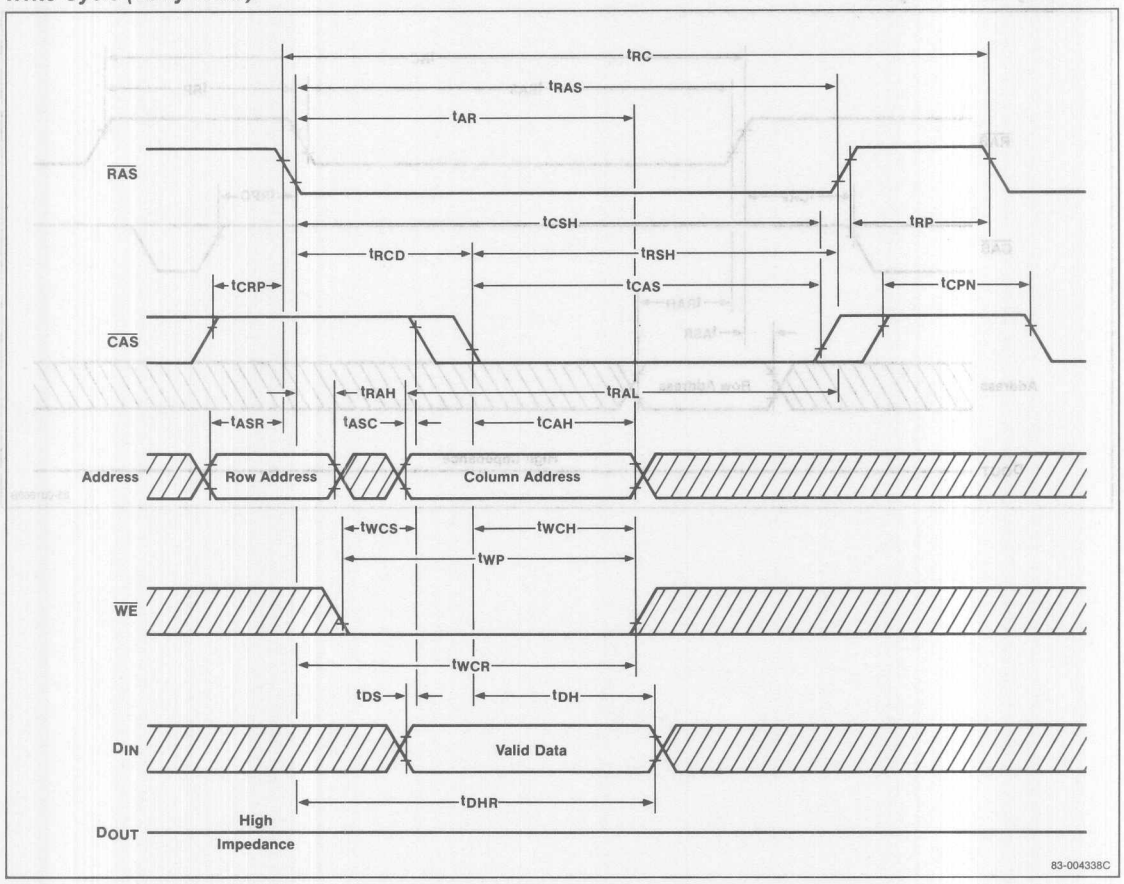
Timing Waveforms

Read Cycle



Timing Waveforms (cont)

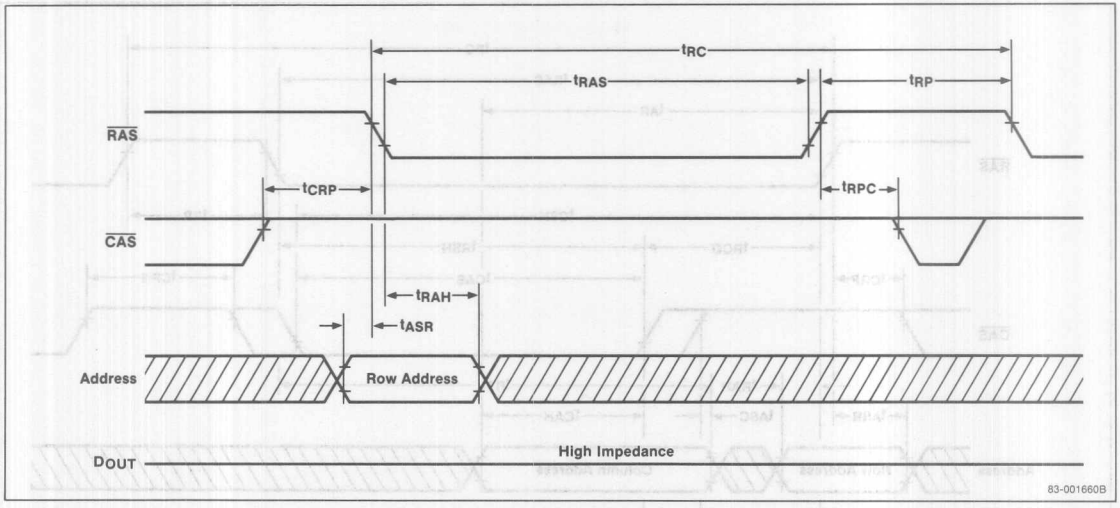
Write Cycle (Early Write)



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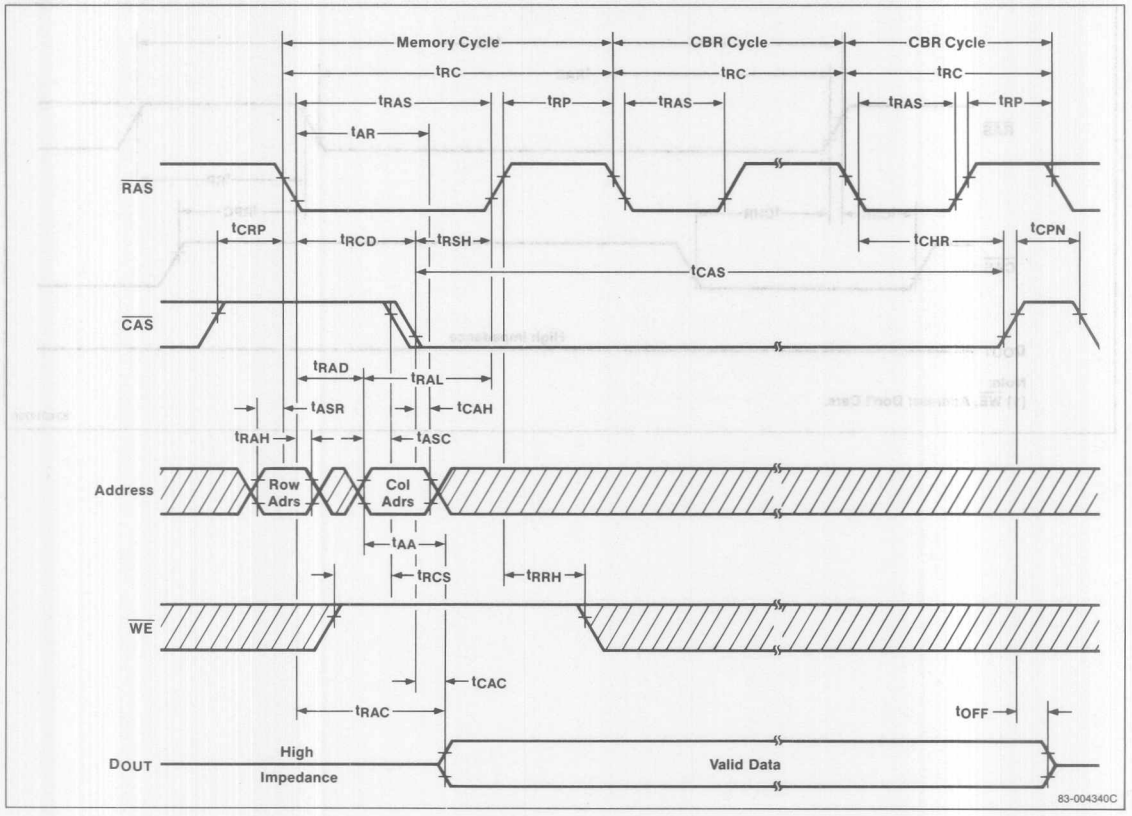
Timing Waveforms (cont)

$\overline{RAS}$-Only Refresh Cycle



Timing Waveforms (cont)

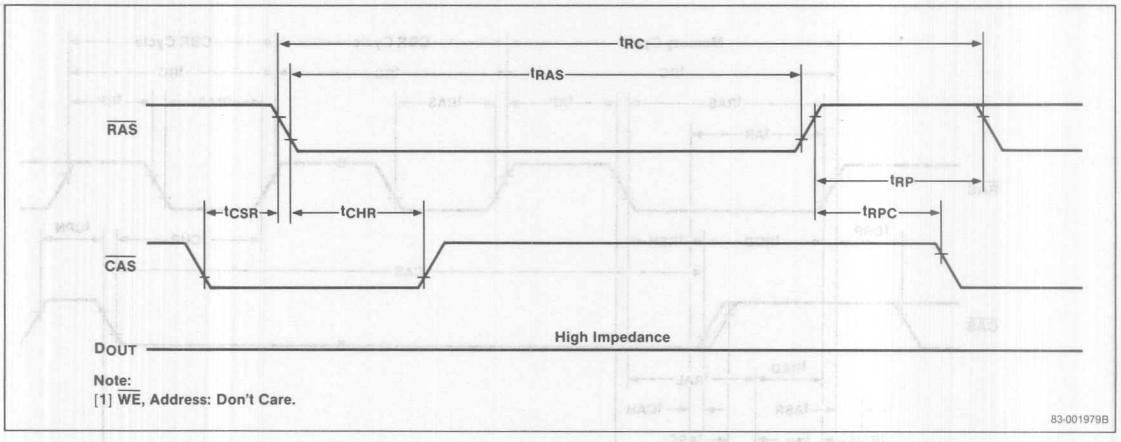
Hidden Refresh Cycle



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Timing Waveforms (cont)

$\overline{CAS}$ Before $\overline{RAS}$ Refresh Cycle

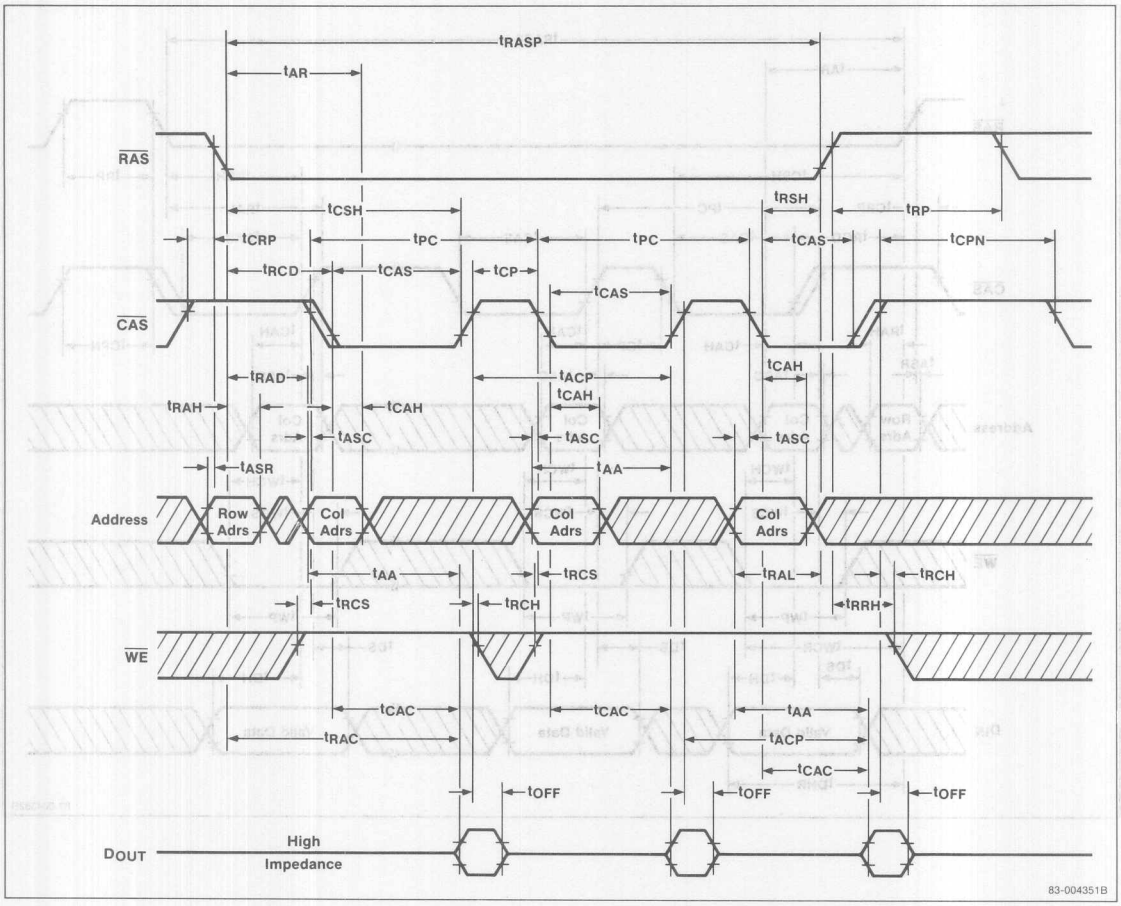


Note:
[1] $\overline{WE}$, Address: Don't Care.

83-001979B

Timing Waveforms (cont)

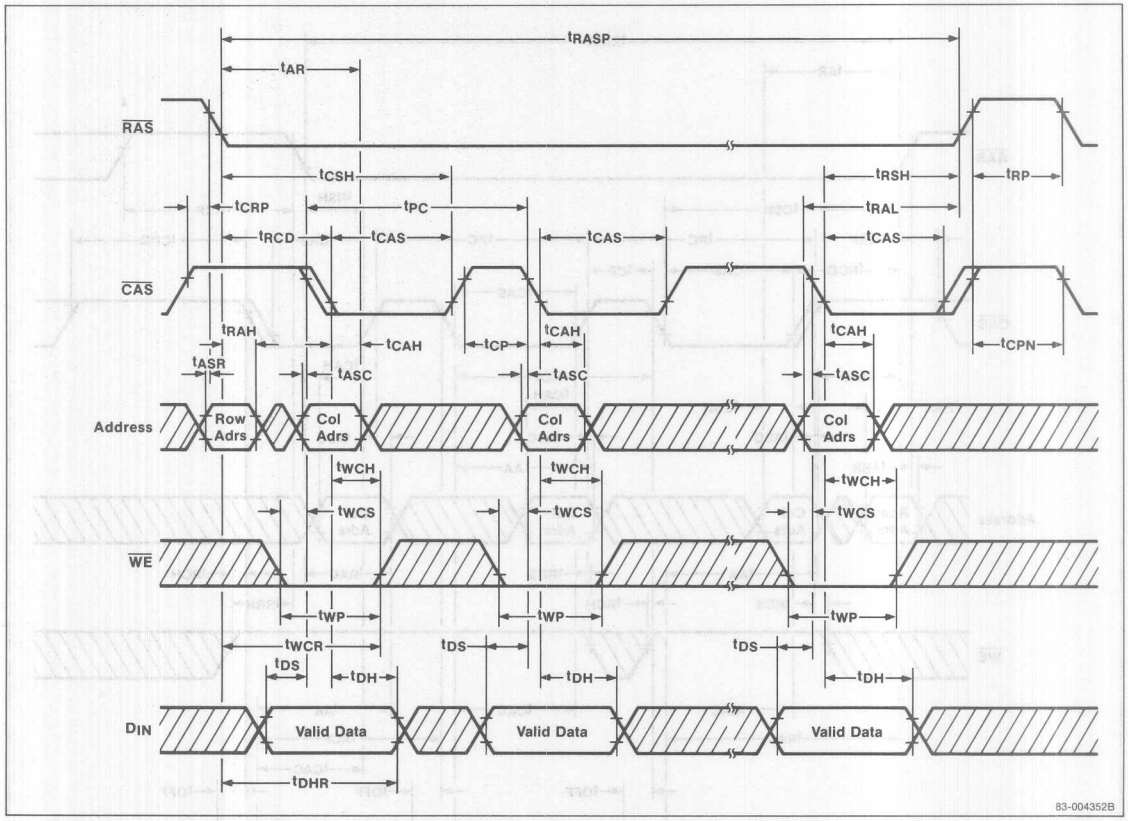
Fast-Page Read Cycle



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Timing Waveforms (cont)

Fast-Page Write Cycle (Early Write)



MC-424100A8
4,194,304 x 8-Bit
Dynamic CMOS RAM Module

Description

The MC-424100A8 is a fast-page 4,194,304-word by 8-bit dynamic RAM module designed to operate from a single +5-volt power supply. Advanced CMOS circuitry, including a single-transistor storage cell, multiplexed address buffers and flexible refresh controls, provides good system operating margins.

The MC-424100A8 is functionally equivalent to eight μPD424100 standard 4M DRAMs. Refreshing is accomplished by means of $\overline{RAS}$-only refresh cycles, hidden refresh cycles, $\overline{CAS}$ before $\overline{RAS}$ refresh cycles, or by normal read or write cycles on the 1024 address combinations of A_0 through A_9 during a 16-ms period.

Single Inline Memory Module (SIMM™) packaging enhances reliability and reduces the size, weight and cost of a system. The SIMM includes eight μPD424100s in SOJ packages and eight power supply decoupling capacitors.

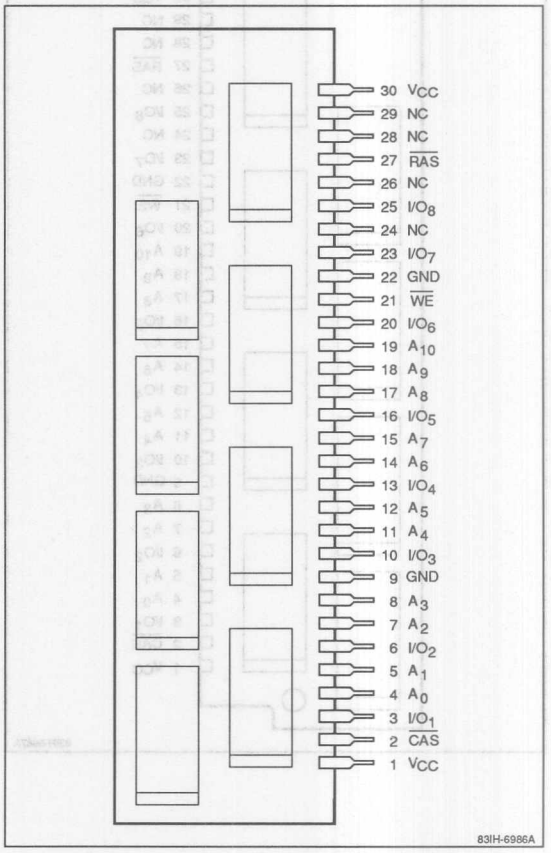
SIMM is a trademark of Wang Laboratories.

Features

- 4,194,304-word by 8-bit organization
- Single +5-volt ±10% power supply
- Standard 30-pin Single Inline Memory Module (SIMM) packaging
- Eight 4M dynamic RAMs incorporated in high-density SOJ packaging (μPD424100LA)
- Eight power supply decoupling capacitors
- Low power dissipation: 44 mW standby (max)
- TTL-compatible inputs and outputs
- 1024 refresh cycles every 16 ms
- Fast-page capability

Pin Configurations

30-Pin Leaded SIMM

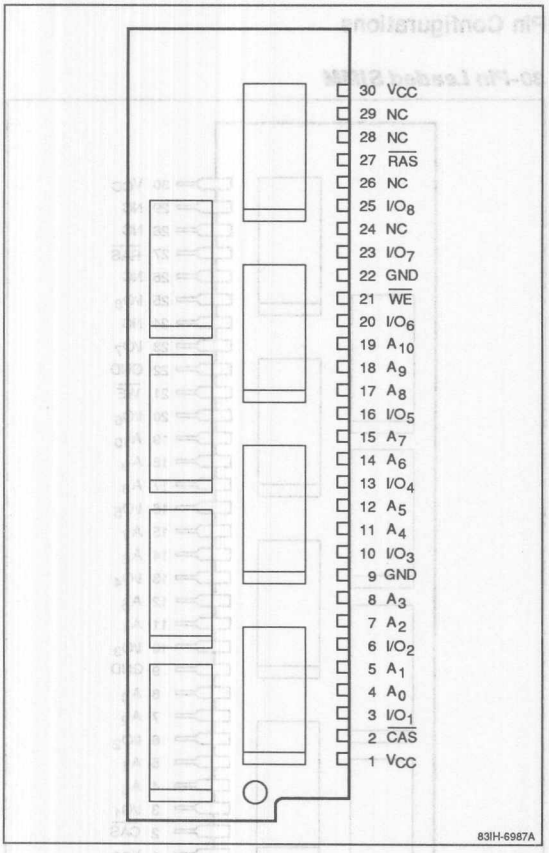


Ordering Information

Part Number	Column Access Time (max)	Row Access Time (max)	Fast-Page Cycle Time (min)	Package
MC-424100A8A-80	80 ns	20 ns	50 ns	30-pin leaded SIMM
A-10	100 s	25 ns	60 ns	
MC-424100A8B-80	80 ns	20 ns	50 ns	30-pin socket-mountable SIMM
B-10	100 ns	25 ns	60 ns	

Pin Configurations (cont)

30-Pin Socket-Mountable SIMM



Pin Identification

Name	Function
A_0 - A_{10}	Address inputs
$\overline{CAS}$	Column address strobe
I/O_1 - I/O_8	Common data inputs and outputs
$\overline{RAS}$	Row address strobe
$\overline{WE}$	Write enable
GND	Ground
V_{CC}	+5-volt power supply
NC	No connection

Absolute Maximum Ratings

Voltage on any pin relative to GND	−1.0 to +7.0 V
Operating temperature, T_{OPR}	0 to +70°C
Storage temperature, T_{STG}	−55 to +125°C
Short-circuit output current, I_{OS}	50 mA
Power dissipation, P_D	8.0 W

Exposure to Absolute Maximum Ratings for extended periods may affect device reliability; exceeding the ratings could cause permanent damage. The device should be operated within the limits specified under DC and AC Characteristics.

Recommended Operating Conditions

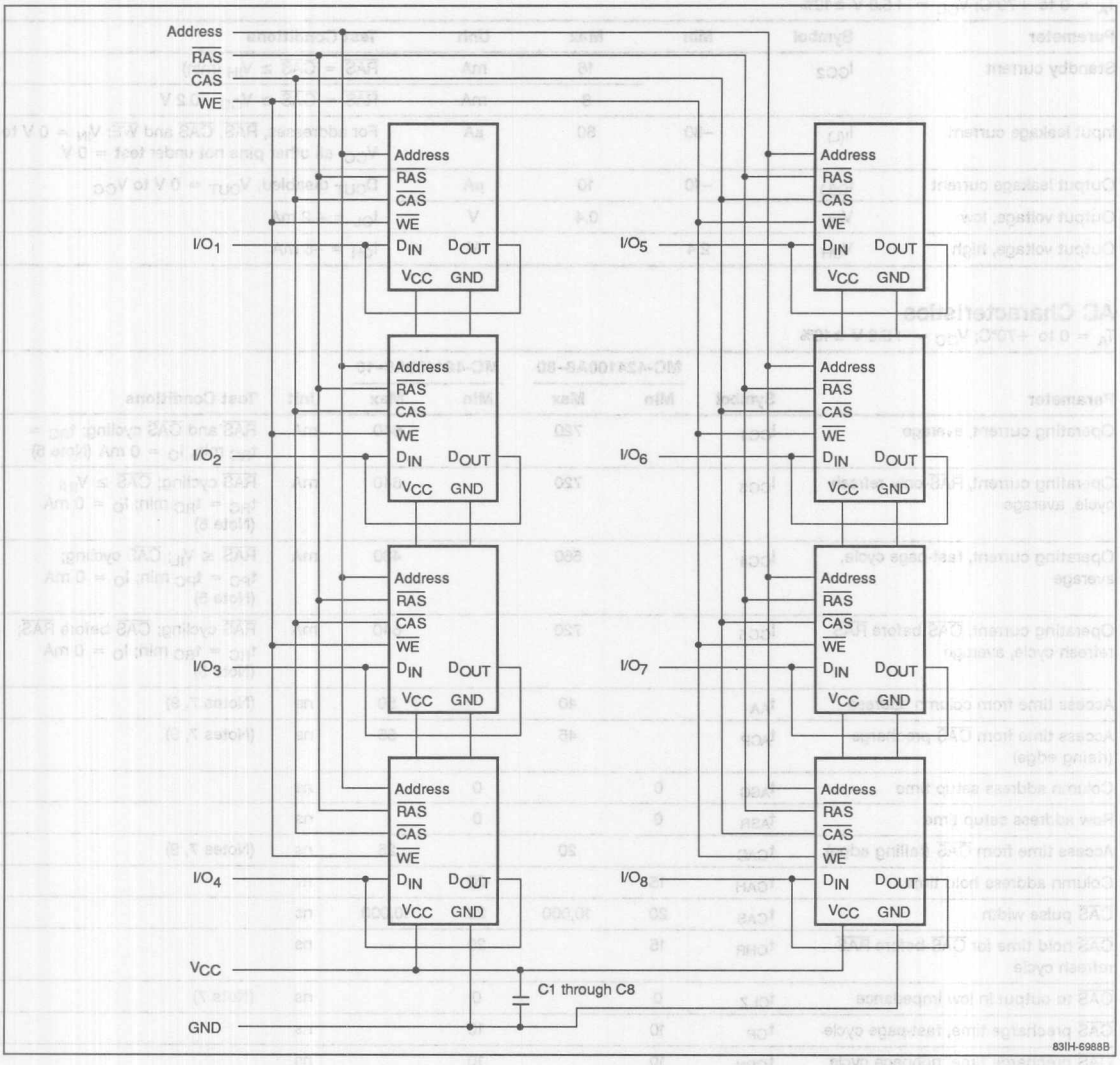
Parameter	Symbol	Min	Typ	Max	Unit
Input voltage, high	V_{IH}	2.4		V_{CC} + 1.0	V
Input voltage, low	V_{IL}	−1.0		0.8	V
Supply voltage	V_{CC}	4.5	5.0	5.5	V
Ambient temperature	T_A	0		70	°C

Capacitance

T_A = 25°C; f = 1 MHz

Parameter	Symbol	Max	Unit	Pins Under Test
Input capacitance	C_{I1}	60	pF	Address, $\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$
Input/output capacitance	C_{IO}	15	pF	I/O_1 through I/O_8

Block Diagram



DC Characteristics

T_A = 0 to +70°C; V_{CC} = +5.0 V ±10%

Parameter	Symbol	Min	Max	Unit	Test Conditions
Standby current	I_{CC2}		16	mA	$\overline{RAS}$ = $\overline{CAS}$ ≥ V_{IH} (min)
			8	mA	$\overline{RAS}$ = $\overline{CAS}$ ≥ V_{CC} – 0.2 V
Input leakage current	$I_{I(L)}$	–80	80	µA	For addresses, $\overline{RAS}$, $\overline{CAS}$ and $\overline{WE}$: V_{IN} = 0 V to V_{CC}; all other pins not under test = 0 V
Output leakage current	$I_{O(L)}$	–10	10	µA	D_{OUT} disabled; V_{OUT} = 0 V to V_{CC}
Output voltage, low	V_{OL}		0.4	V	I_{OL} = 4.2 mA
Output voltage, high	V_{OH}	2.4		V	I_{OH} = –5 mA

AC Characteristics

T_A = 0 to +70°C; V_{CC} = +5.0 V ±10%

		MC-424100A8–80		MC-424100A8–10			
Parameter	Symbol	Min	Max	Min	Max	Unit	Test Conditions
Operating current, average	I_{CC1}		720		640	mA	$\overline{RAS}$ and $\overline{CAS}$ cycling; t_{RC} = t_{RC} min; I_O = 0 mA (Note 5)
Operating current, $\overline{RAS}$-only refresh cycle, average	I_{CC3}		720		640	mA	$\overline{RAS}$ cycling; $\overline{CAS}$ ≥ V_{IH}; t_{RC} = t_{RC} min; I_O = 0 mA (Note 5)
Operating current, fast-page cycle, average	I_{CC4}		560		480	mA	$\overline{RAS}$ ≤ V_{IL}; $\overline{CAS}$ cycling; t_{PC} = t_{PC} min; I_O = 0 mA (Note 5)
Operating current, $\overline{CAS}$ before $\overline{RAS}$ refresh cycle, average	I_{CC5}		720		640	mA	$\overline{RAS}$ cycling; $\overline{CAS}$ before $\overline{RAS}$; t_{RC} = t_{RC} min; I_O = 0 mA (Note 5)
Access time from column address	t_{AA}		40		50	ns	(Notes 7, 9)
Access time from $\overline{CAS}$ precharge (rising edge)	t_{ACP}		45		55	ns	(Notes 7, 9)
Column address setup time	t_{ASC}	0		0		ns	
Row address setup time	t_{ASR}	0		0		ns	
Access time from $\overline{CAS}$ (falling edge)	t_{CAC}		20		25	ns	(Notes 7, 9)
Column address hold time	t_{CAH}	15		20		ns	
$\overline{CAS}$ pulse width	t_{CAS}	20	10,000	25	10,000	ns	
$\overline{CAS}$ hold time for $\overline{CAS}$ before $\overline{RAS}$ refresh cycle	t_{CHR}	15		20		ns	
$\overline{CAS}$ to output in low impedance	t_{CLZ}	0		0		ns	(Note 7)
$\overline{CAS}$ precharge time, fast-page cycle	t_{CP}	10		10		ns	
$\overline{CAS}$ precharge time, nonpage cycle	t_{CPN}	10		10		ns	
$\overline{CAS}$ to $\overline{RAS}$ precharge time	t_{CRP}	10		10		ns	(Note 12)
$\overline{CAS}$ hold time	t_{CSH}	80		100		ns	
$\overline{CAS}$ setup time for $\overline{CAS}$ before $\overline{RAS}$ refresh cycle	t_{CSR}	10		10		ns	
Data-in hold time	t_{DH}	15		20		ns	(Note 15)
Data-in setup time	t_{DS}	0		0		ns	(Note 15)
Output buffer turnoff delay	t_{OFF}	0	20	0	25	ns	(Note 10)
Fast-page cycle time	t_{PC}	50		60		ns	(Note 6)

AC Characteristics (cont)

Parameter	Symbol	MC-424100A8–80		MC-424100A8–10		Unit	Test Conditions
		Min	Max	Min	Max		
Access time from $\overline{RAS}$	t_{RAC}		80		100	ns	(Notes 7, 8)
$\overline{RAS}$ to column address delay time	t_{RAD}	17	40	17	50	ns	(Note 9)
Row address hold time	t_{RAH}	12		12		ns	
Column address lead time referenced to $\overline{RAS}$ (rising edge)	t_{RAL}	40		50		ns	
$\overline{RAS}$ pulse width	t_{RAS}	80	10,000	100	10,000	ns	
$\overline{RAS}$ pulse width, fast-page cycle	t_{RASP}	80	125,000	100	125,000	ns	
Random read or write cycle time	t_{RC}	160		190		ns	(Note 6)
$\overline{RAS}$ to $\overline{CAS}$ delay time	t_{RCD}	25	60	25	75	ns	(Note 11)
Read command hold time referenced to $\overline{CAS}$	t_{RCH}	0		0		ns	(Note 13)
Read command setup time	t_{RCS}	0		0		ns	
Refresh period	t_{REF}		16		16	ms	Addresses A_0 through A_9
$\overline{RAS}$ precharge time	t_{RP}	70		80		ns	
$\overline{RAS}$ precharge $\overline{CAS}$ hold time	t_{RPC}	10		10		ns	
Read command hold time referenced to $\overline{RAS}$	t_{RRH}	10		10		ns	(Note 13)
$\overline{RAS}$ hold time	t_{RSH}	20		25		ns	
Rise and fall transition time	t_T	3	50	3	50	ns	(Note 3)
Write command hold time	t_{WCH}	15		20		ns	
Write command setup time	t_{WCS}	0		0		ns	(Note 16)
$\overline{WE}$ hold time	t_{WHR}	15		20		ns	
Write command pulse width	t_{WP}	15		20		ns	(Note 14)
$\overline{WE}$ setup time	t_{WSR}	10		10		ns	

Notes:

(1) All voltages are referenced to GND.

(2) An initial pause of 100 μs is required after power-up, followed by any eight $\overline{RAS}$ cycles, before proper device operation is achieved. At the end of the initial power-up sequence, it is recommended that either a $\overline{RAS}$-only refresh or a $\overline{CAS}$ before $\overline{RAS}$ refresh cycle be executed while $\overline{WE} \geq V_{IH}$ to ensure normal operation.

(3) AC measurements assume $t_T = 5$ ns.

(4) V_{IH} (min) and V_{IL} (max) are reference levels for measuring the timing of input signals. Transition times are measured between V_{IH} and V_{IL}.

(5) I_{CC1}, I_{CC3}, I_{CC4}, and I_{CC5} depend on output loading and cycle rates. Specified values are obtained with the output open. I_{CC3} is measured assuming that all column address inputs are held at either a high level or a low level during $\overline{RAS}$-only refresh cycles. I_{CC4} is measured assuming that all column address inputs are switched only once during each fast-page cycle.

(6) The minimum specifications are used only to indicate the cycle time at which proper operation over the full temperature range (T_A = 0 to +70°C) is assured.

(7) Load = 2 TTL (–1 mA, +4 mA) loads and 100 pF (V_{OH} = 2.0 V, V_{OL} = 0.8 V).

(8) Assumes that $t_{RCD} \leq t_{RCD}$ (max) and $t_{RAD} \leq t_{RAD}$ (max). If t_{RCD} or t_{RAD} is greater than the maximum recommended value in this table, t_{RAC} increases by the amount that t_{RCD} or t_{RAD} exceeds the value shown.

(9) If $t_{RAD} \geq t_{RAD}$ (max), then the access time is defined by t_{AA}.

(10) t_{OFF} (max) defines the time at which the output achieves the open-circuit condition and is not referenced to V_{OH} or V_{OL}.

(11) Operation within the t_{RCD} (max) limit assures that t_{RAC} (max) can be met. t_{RCD} (max) is specified as a reference point only; if t_{RCD} is greater than t_{RCD} (max), then access time is controlled exclusively by t_{CAC}.

(12) The t_{CRP} requirement should be applicable for $\overline{RAS}/\overline{CAS}$ cycles preceded by any cycle.

(13) Either t_{RRH} or t_{RCH} must be satisfied for a read cycle.

(14) Parameter t_{WP} is applicable for a delayed write cycle such as a read-write/read-modify-write cycle. For early write operation, both t_{WCS} and t_{WCH} must be met.

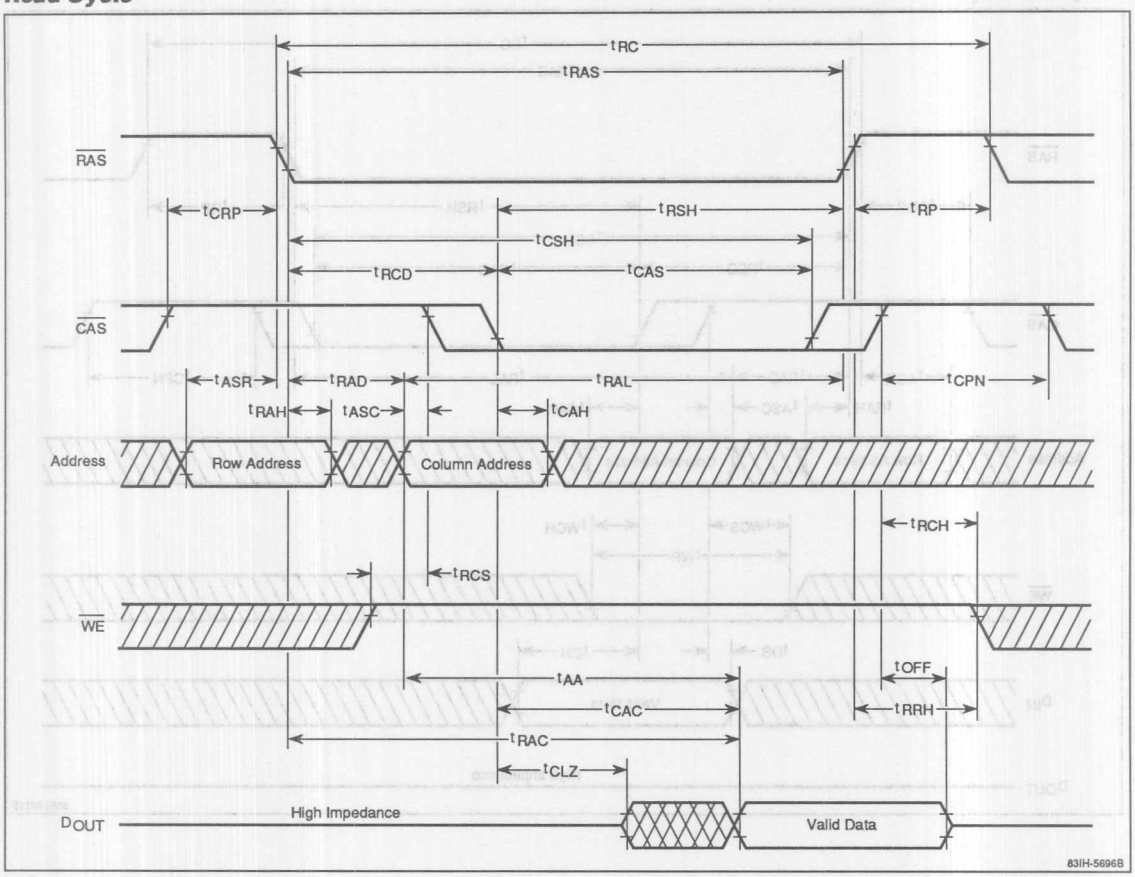
(15) These parameters are referenced to the falling edge of $\overline{CAS}$ for early write cycles and to the falling edge of $\overline{WE}$ for delayed write or read-modify-write cycles.

(16) t_{WCS}, t_{RWD}, t_{CWD}, and t_{AWD} are restrictive operating parameters in read-write/read-modify-write cycles only. If $t_{WCS} \geq t_{WCS}$ (min), the cycle is an early write cycle and the data output will remain open-circuit throughout the entire cycle. If $t_{CWD} \geq t_{CWD}$ (min), $t_{RWD} \geq t_{RWD}$ (min), and $t_{AWD} \geq t_{AWD}$ (min), the cycle is a read-write cycle and the data output will contain data read from the selected cell. If neither of the above conditions is met, the condition of the data output pin (at access time and until $\overline{CAS}$ returns to V_{IH}) is indeterminate.

(17) A test mode may be initiated by executing a $\overline{CAS}$ before $\overline{RAS}$ refresh cycle with $\overline{WE}$ held at V_{IL}. This mode also may inadvertently be initiated during power-up because external control of the signal lines is very difficult during this period. It is therefore recommended that while $\overline{WE}$ is held at V_{IH}, either a $\overline{RAS}$-only or $\overline{CAS}$ before $\overline{RAS}$ refresh cycle should be executed at any time after the end of the initial power-up sequence to ensure normal device operation.

Timing Waveforms

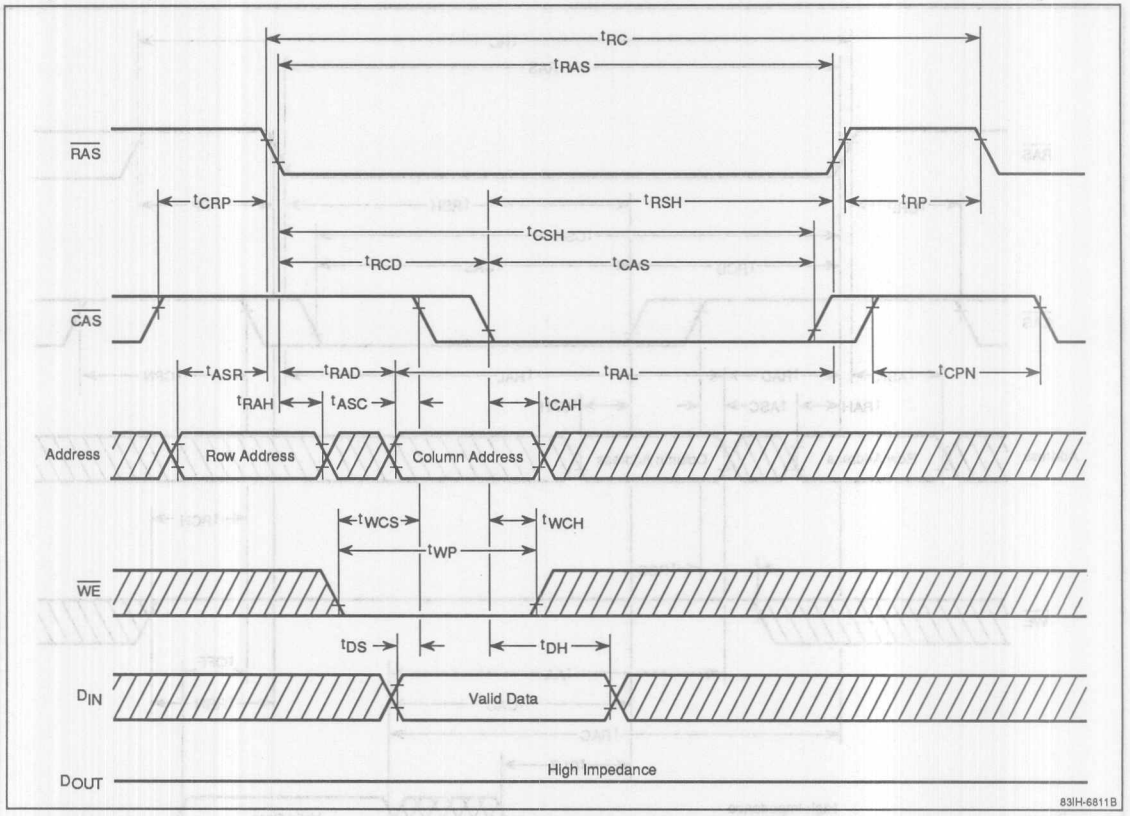
Read Cycle



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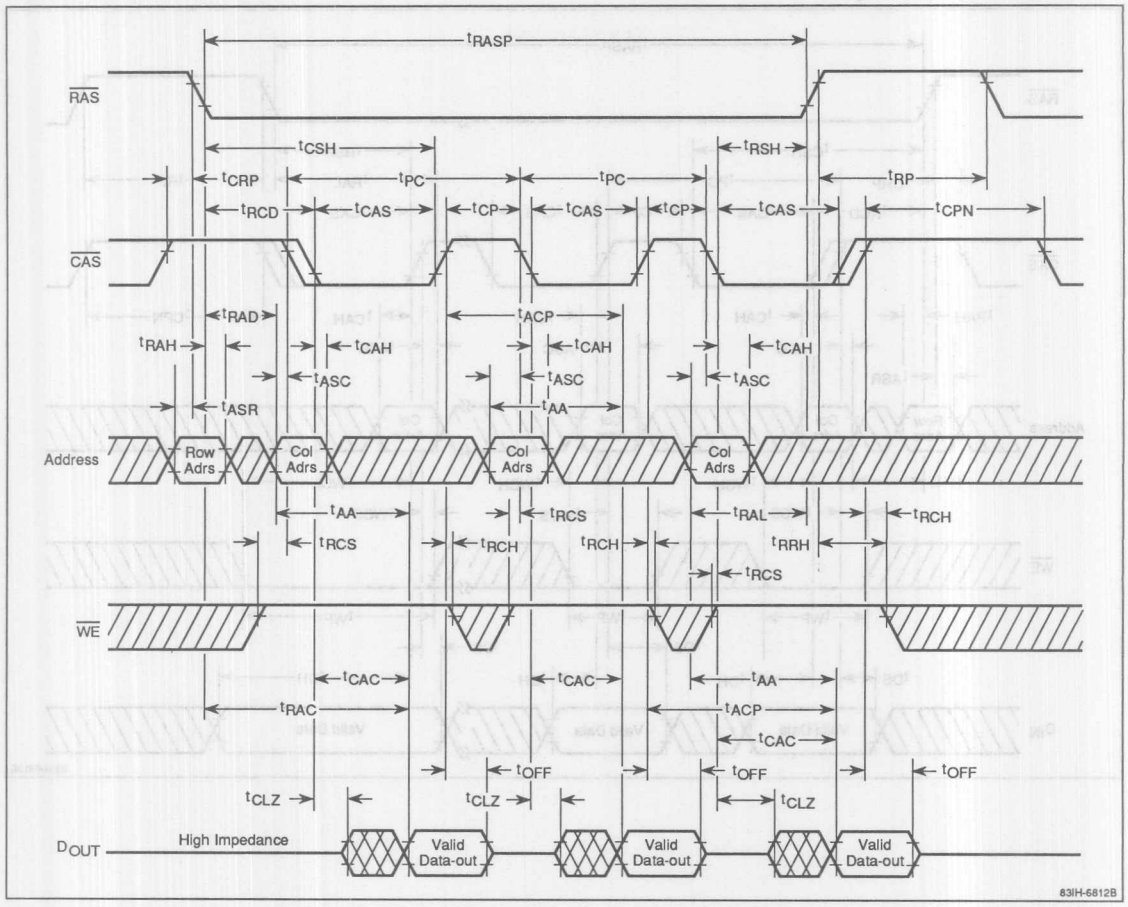
Timing Waveforms (cont)

Early Write Cycle



Timing Waveforms (cont)

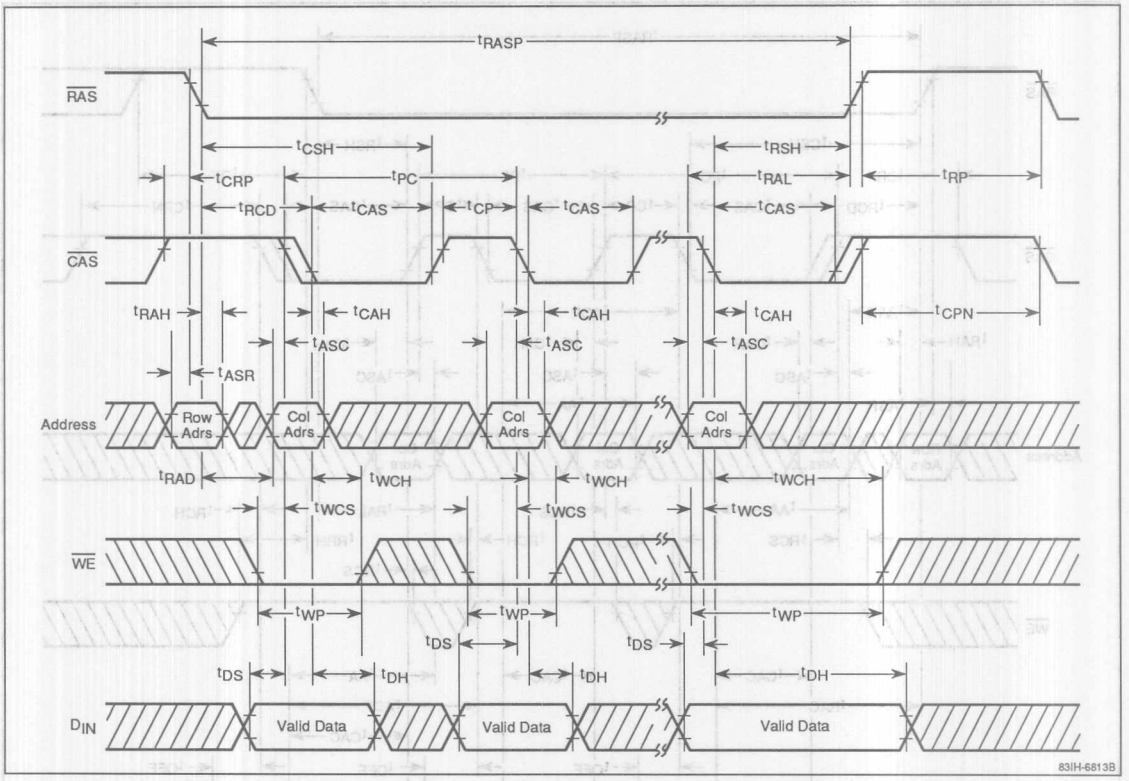
Fast-Page Read Cycle



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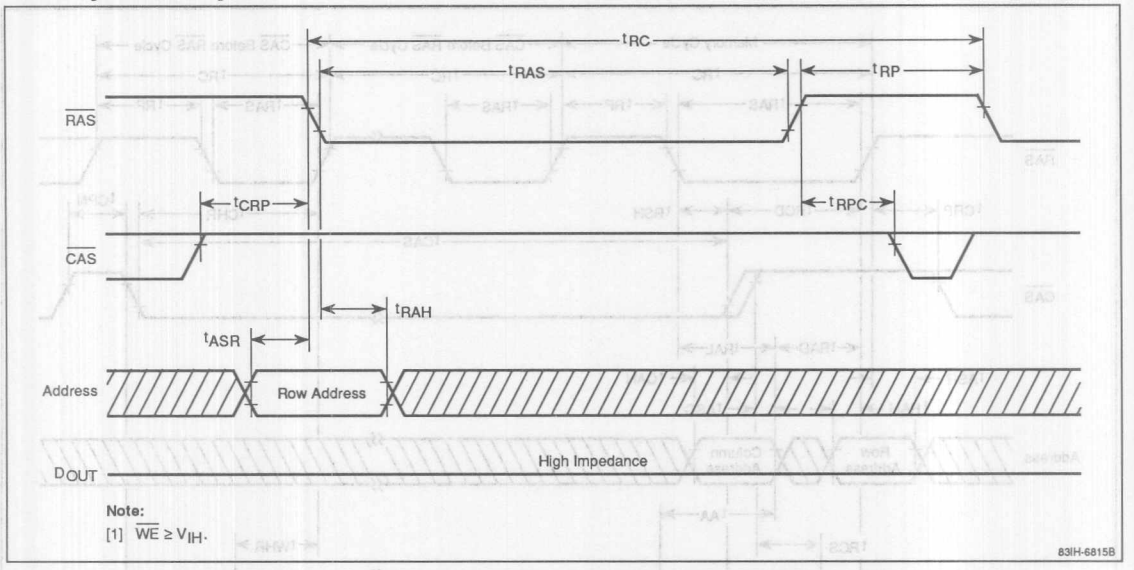
Timing Waveforms (cont)

Fast-Page Early Write Cycle



Timing Waveforms (cont)

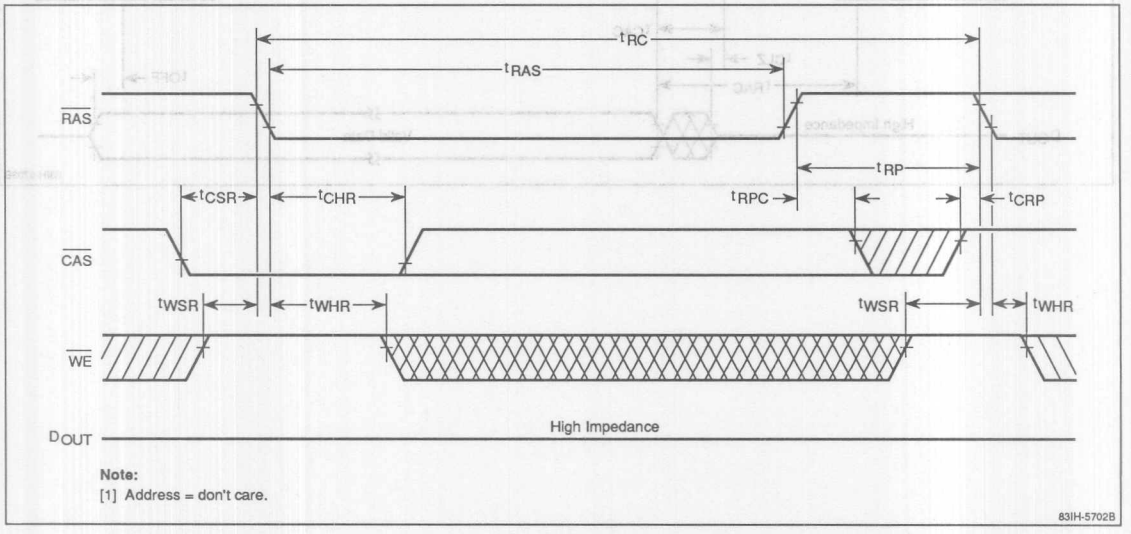
$\overline{RAS}$-Only Refresh Cycle



Note:
[1] $\overline{WE} \geq V_{IH}$.

83IH-6815B

$\overline{CAS}$ Before $\overline{RAS}$ Refresh Cycle



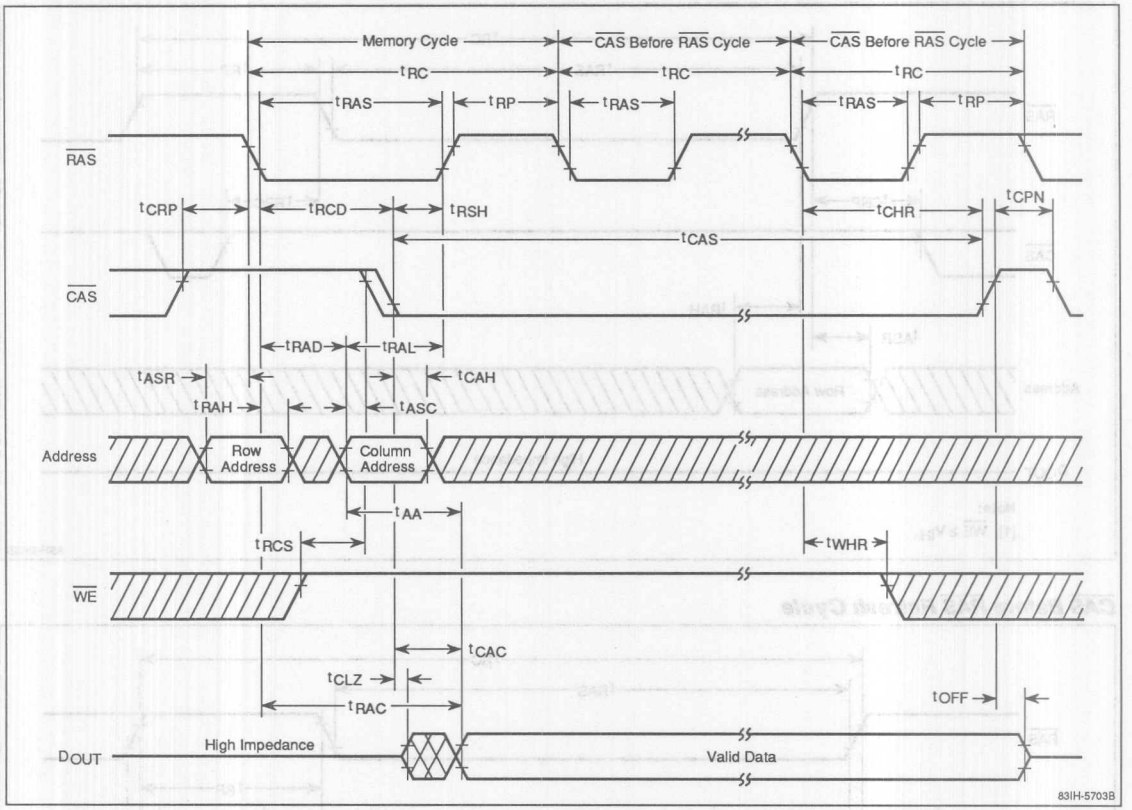
Note:
[1] Address = don't care.

83IH-5702B

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Timing Waveforms (cont)

Hidden Refresh Cycle



MC-41256A9
262,144 x 9-Bit
Dynamic NMOS RAM Module

Description

The MC-41256A9 is a 262,144-word by 9-bit DRAM module designed to operate from a single +5-volt power supply. Advanced dynamic NMOS circuitry, including a single-transistor storage cell, 1024 sense amplifiers per data output, multiplexed address buffers and flexible refresh controls, provides good system operating margins.

The MC-41256A9 is functionally equivalent to eight μPD41256 standard 256K DRAMs with a parity bit. Refreshing is accomplished by means of $\overline{RAS}$-only refresh cycles, hidden refresh cycles, $\overline{CAS}$ before $\overline{RAS}$ refresh cycles, or by normal read or write cycles on the 256 address combinations of A_0 through A_7 during a 4-ms period.

Single Inline Memory Module (SIMM™) packaging enhances reliability and reduces the size, weight and cost of a system. The MC-41256A9 includes nine μPD41256s in PLCC packages and nine power supply decoupling capacitors.

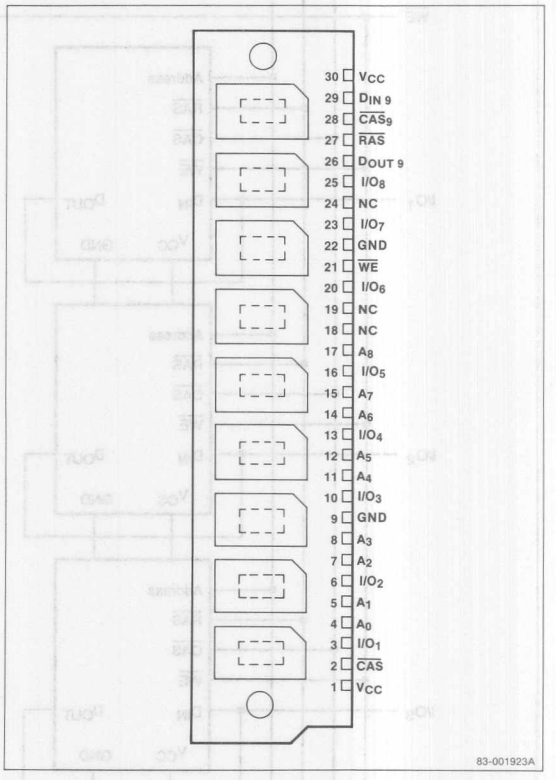
SIMM is a trademark of Wang Laboratories.

Features

- 262,144-word by 9-bit organization
- Single +5-volt power supply
- Standard 30-pin SIMM packaging
- Nine 256K DRAMs in high-density PLCC packaging
- Nine power supply decoupling capacitors
- Low power dissipation of 248 mW max (standby)
- TTL-compatible inputs and outputs
- 256 refresh cycles every 4 ms
- Page-mode capability

Pin Configuration

30-Pin SIMM

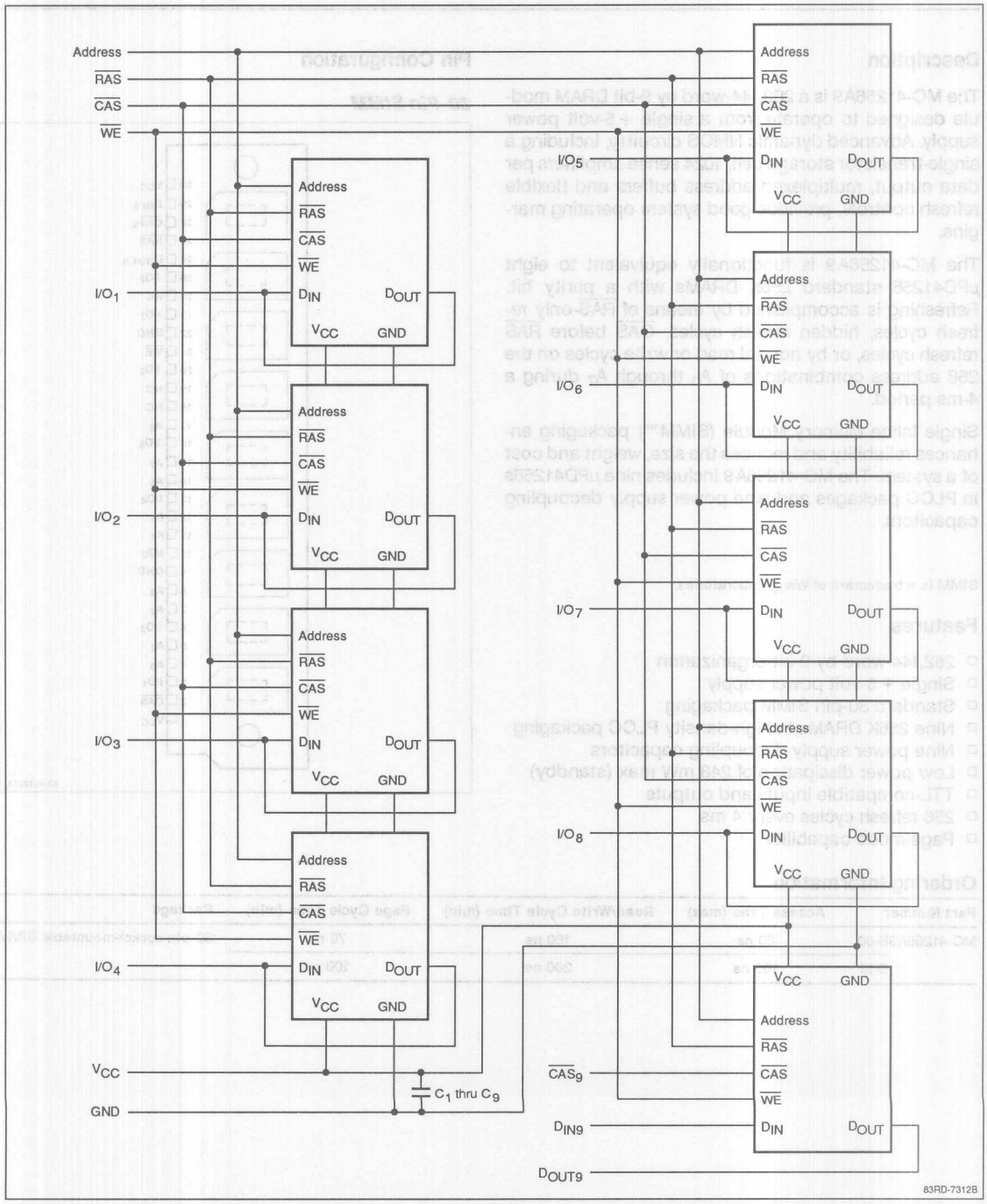


Ordering Information

Part Number	Access Time (max)	Read/Write Cycle Time (min)	Page Cycle Time (min)	Package
MC-41256A9B-80	80 ns	160 ns	70 ns	30-pin socket-mountable SIMM
B-10	100 ns	200 ns	100 ns	

New speed of 70 ns will be available in 1991.

Block Diagram



Pin Identification

Symbol	Function
A_0 - A_8	Address inputs
I/O_1 - I/O_8	Common data inputs/outputs
D_{IN9}	Data input 9
D_{OUT9}	Data output 9
$\overline{CAS}$	Column address strobe
$\overline{CAS_9}$	Column address strobe for data output 9
$\overline{RAS}$	Row address strobe
$\overline{WE}$	Write enable
GND	Ground
V_{CC}	+5-volt power supply
NC	No connection

Recommended Operating Conditions

Parameter	Symbol	Min	Typ	Max	Unit
Input voltage, high	V_{IH}	2.4		V_{CC} + 1.0	V
Input voltage, low	V_{IL}	−1.0		0.8	V
Supply voltage	V_{CC}	4.5	5.0	5.5	V
Ambient temperature	T_A	0		70	°C

Notes:

(1) V_{CC} = +5.0 V ±5% for the −80 version.

Absolute Maximum Ratings

Voltage on any pin relative to GND, V_T	−1.0 to +7.0 V
Operating temperature, T_{OPR}	0 to +70°C
Storage temperature, T_{STG}	−55 to +125°C
Short-circuit output current, I_{OS}	50 mA
Power dissipation, P_D	9.0 W

Exposure to Absolute Maximum Ratings for extended periods may affect device reliability; exceeding the ratings could cause permanent damage. The device should be operated within the limits specified under DC and AC Characteristics.

Capacitance

T_A = 0 to +70°C; f = 1 MHz

Parameter	Symbol	Max	Unit	Pins Under Test
Input capacitance	C_{IA}	60	pF	A_0 - A_8
	C_{IR}	75	pF	$\overline{RAS}$, $\overline{WE}$
	C_{IC}	70	pF	$\overline{CAS}$
	C_{IC9}	13	pF	$\overline{CAS_9}$
	C_{IN9}	10	pF	D_{IN9}
Input/output capacitance	$C_{I/O}$	17	pF	For I/O_1 - I/O_8: $\overline{CAS}$ = V_{IH} to disable D_{OUT}
Capacitance				
Output capacitance	C_{OUT9}	12	pF	For D_{OUT9}: $\overline{CAS_9}$ = V_{IH} to disable D_{OUT9}

DC Characteristics

T_A = 0 to +70°C; GND = 0 V

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions
Standby current	I_{CC2}			45	mA	$\overline{RAS}$ = V_{IH}; D_{OUT} = high-Z
Input leakage current	I_{IL}	−90		90	μA	For A_0 - A_8, $\overline{RAS}$, $\overline{CAS}$ and $\overline{WE}$: V_{IN} = 0 V to V_{CC}; all other pins = 0 V
	I_{IL9}	−10		10	μA	For $\overline{CAS_9}$ and D_{IN9}: V_{IN} = 0 V to V_{CC}; other pins = 0 V
Output leakage current	I_{OL}	−10		10	μA	For I/O_1 - I/O_8: D_{OUT} disabled; V_{OUT} = 0 V to V_{CC}
	I_{OL9}	−10		10	μA	For D_{OUT9}: D_{OUT9} disabled; V_{OUT} = 0 V to V_{CC}
Output voltage, low	V_{OL}			0.4	V	I_{OUT} = 4.2 mA
Output voltage, high	V_{OH}	2.4			V	I_{OUT} = −5 mA

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AC Characteristics

T_A = 0 to +70°C

Parameter	Symbol	MC-41256A9-80 Min	MC-41256A9-80 Max	MC-41256A9-10 Min	MC-41256A9-10 Max	Unit	Test Conditions
Supply voltage	V_{CC}	4.75	5.25	4.5	5.5	V	
Operating supply current, average	I_{CC1}		810		720	mA	$\overline{RAS}$, $\overline{CAS}$ cycling; $t_{RC} = t_{RC}$ (min); I_O = 0 mA (Note 5)
Operating supply current, $\overline{RAS}$-only refresh cycle, average	I_{CC3}		720		585	mA	$\overline{RAS}$ cycling; $\overline{CAS} \geq V_{IH}$; $t_{RC} = t_{RC}$ (min); I_O = 0 mA (Note 5)
Operating supply current, page cycle, average	I_{CC4}		630		540	mA	$\overline{RAS} \leq V_{IL}$; $\overline{CAS}$ cycling; $t_{PC} = t_{PC}$ (min); I_O = 0 mA (Note 5)
Operating current, $\overline{CAS}$ before $\overline{RAS}$ refresh cycle, average	I_{CC5}		720		585	mA	$\overline{CAS} \leq V_{IL}$; $\overline{RAS}$ cycling; $t_{RC} = t_{RC}$ (min); I/O = 0 mA (Note 5)
Random read or write cycle time	t_{RC}	180		200		ns	(Note 6)
Read-write cycle time	t_{RWC}	185		240		ns	(Notes 6, 16)
Page cycle time	t_{PC}	70		100		ns	(Note 6)
Access time from $\overline{RAS}$	t_{RAC}		80		100	ns	(Notes 7, 8)
Access time from $\overline{CAS}$	t_{CAC}		40		50	ns	(Notes 7, 9)
Output buffer turnoff delay	t_{OFF}	0	20	0	25	ns	(Note 10)
Rise and fall transition time	t_T	3	50	3	50	ns	(Note 4)
$\overline{RAS}$ precharge time	t_{RP}	70		90		ns	
$\overline{RAS}$ pulse width	t_{RAS}	80	16,000	100	10,000	ns	
$\overline{RAS}$ hold time	t_{RSH}	40		50		ns	
$\overline{CAS}$ pulse width	t_{CAS}	40	10,000	50	10,000	ns	
$\overline{CAS}$ hold time	t_{CSH}	80		100		ns	
$\overline{RAS}$ to $\overline{CAS}$ delay time	t_{RCD}	20	40	20	50	ns	(Note 11)
$\overline{CAS}$ to $\overline{RAS}$ precharge time	t_{CRP}	10		10		ns	(Note 12)
$\overline{CAS}$ precharge time, nonpage cycle	t_{CPN}	25		25		ns	
$\overline{CAS}$ precharge time, page cycle	t_{CP}	20		40		ns	
$\overline{RAS}$ precharge $\overline{CAS}$ hold time	t_{RPC}	0		0		ns	
Row address setup time	t_{ASR}	0		0		ns	
Row address hold time	t_{RAH}	10		10		ns	
Column address setup time	t_{ASC}	0		0		ns	
Column address hold time	t_{CAH}	15		15		ns	
Column address hold time referenced to $\overline{RAS}$	t_{AR}	55		65		ns	
Read command setup time	t_{RCS}	0		0		ns	
Read command hold time referenced to $\overline{RAS}$	t_{RRH}	10		10		ns	(Note 13)
Read command hold time referenced to $\overline{CAS}$	t_{RCH}	0		0		ns	(Note 13)
Write command hold time	t_{WCH}	20		25		ns	

AC Characteristics (cont)

Parameter	Symbol	MC-41256A9-80 Min	MC-41256A9-80 Max	MC-41256A9-10 Min	MC-41256A9-10 Max	Unit	Test Conditions
Write command hold time referenced to $\overline{RAS}$	t_{WCR}	60		75		ns	
Write command pulse width	t_{WP}	20		15		ns	
Write command to $\overline{RAS}$ lead time	t_{RWL}	20		35		ns	
Write command to $\overline{CAS}$ lead time	t_{CWL}	20		35		ns	
Data-in setup time	t_{DS}	0		0		ns	(Note 14)
Data-in hold time	t_{DH}	20		25		ns	(Note 14)
Data-in hold time referenced to $\overline{RAS}$	t_{DHR}	60		75		ns	
Refresh period	t_{REF}		4		4	ms	Addresses A_0 - A_7
$\overline{WE}$ command setup time	t_{WCS}	0		0		ns	(Notes 15, 16)
$\overline{CAS}$ to $\overline{WE}$ delay	t_{CWD}	40		50		ns	(Notes 15, 16)
$\overline{RAS}$ to $\overline{WE}$ delay	t_{RWD}	80		100		ns	(Notes 15, 16)
$\overline{CAS}$ setup time for $\overline{CAS}$ before $\overline{RAS}$ refresh cycle	t_{CSR}	10		10		ns	
$\overline{CAS}$ hold time for $\overline{CAS}$ before $\overline{RAS}$ refresh cycle	t_{CHR}	20		20		ns	

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Notes:

(1) All voltages are referenced to GND.

(2) An initial pause of 100 μs is required after power-up, followed by any eight $\overline{RAS}$ cycles, before proper device operation is achieved.

(3) AC measurements assume t_T = 5 ns.

(4) V_{IH} (min) and V_{IL} (max) are reference levels for measuring the timing of input signals. Transition times are measured between V_{IH} and V_{IL}.

(5) I_{CC1}, I_{CC3}, I_{CC4}, and I_{CC5} depend on output loading and cycle rates. Specified values are obtained with the output open.

(6) The minimum specifications are used only to indicate the cycle time at which proper operation over the full temperature range (T_A = 0 to +70°C) is assured.

(7) Output load = 2 TTL loads and 100 pF

(8) Assumes that $t_{RCD} \leq t_{RCD}$ (max). If t_{RCD} is greater than the maximum recommended value shown in this table, t_{RAC} will increase by the amount that t_{RCD} exceeds the value shown.

(9) Assumes that $t_{RCD} \geq t_{RCD}$ (max)

(10) t_{OFF} (max) defines the time at which the output achieves the open-circuit condition and is not referenced to V_{OH} or V_{OL}.

(11) Operation within the t_{RCD} (max) limit assures that t_{RAC} (max) can be met. t_{RCD} (max) is specified as a reference point only. If t_{RCD} is greater than the specified t_{RCD} (max) limit, then access time is controlled exclusively by t_{CAC}.

(12) The t_{CRP} requirement should be applicable for $\overline{RAS}$/$\overline{CAS}$ cycles preceded by any cycle.

(13) Either t_{RRH} or t_{RCH} must be satisfied for a read cycle.

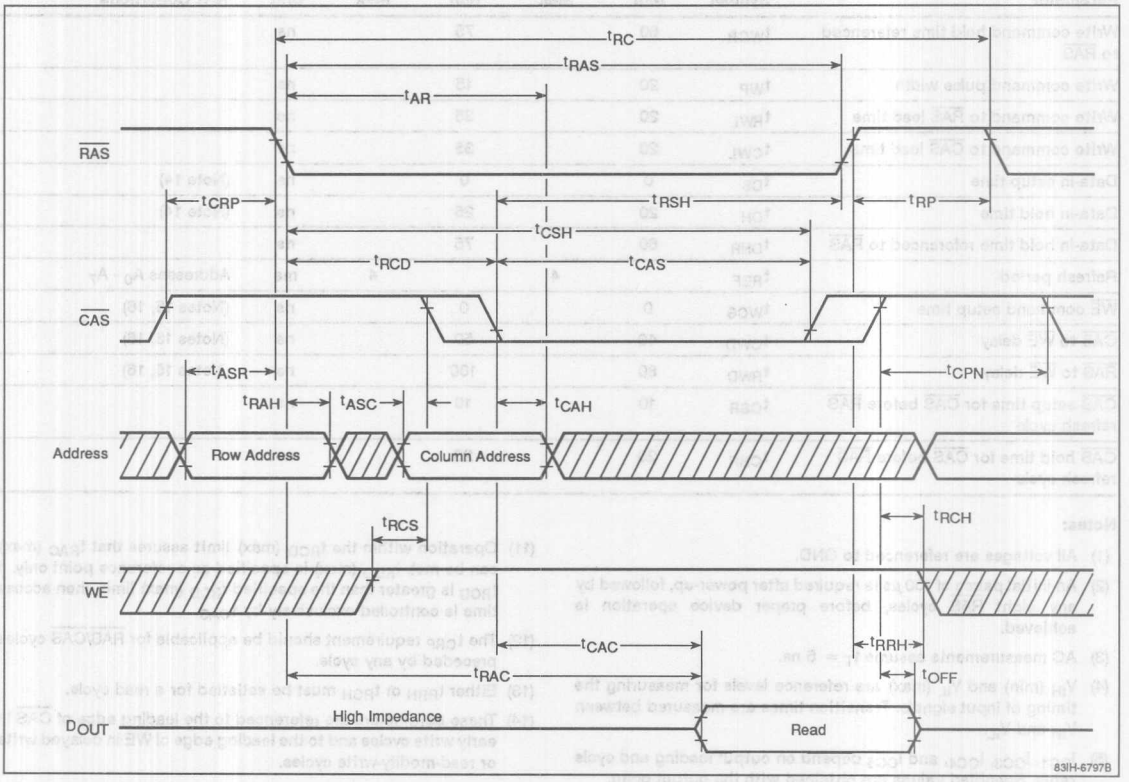
(14) These parameters are referenced to the leading edge of $\overline{CAS}$ in early write cycles and to the leading edge of $\overline{WE}$ in delayed write or read-modify-write cycles.

(15) For D_{OUT9}, t_{WCS}, t_{CWD}, and t_{RWD} are restrictive operating parameters in read-write and read-modify-write cycles only. If $t_{WCS} \geq t_{WCS}$ (min), the cycle is an early write cycle and the data output will remain open-circuit throughout the entire cycle. If $t_{CWD} \geq t_{CWD}$ (min) and $t_{RWD} \geq t_{RWD}$ (min), the cycle is a read-write cycle and the data output will contain data read from the selected cell. If neither of the above conditions is met, the condition of $D_{OUT\,9}$ (at access time and until $\overline{CAS}_9$ goes back to V_{IH}) is indeterminate.

(16) The execution of read-write/read-modify-write cycles is controlled by $\overline{CAS}_9$ because of its separate data input and output pins. Therefore, only one device (of the nine packaged on the SIMM) can execute read-write/read-modify-write cycles.

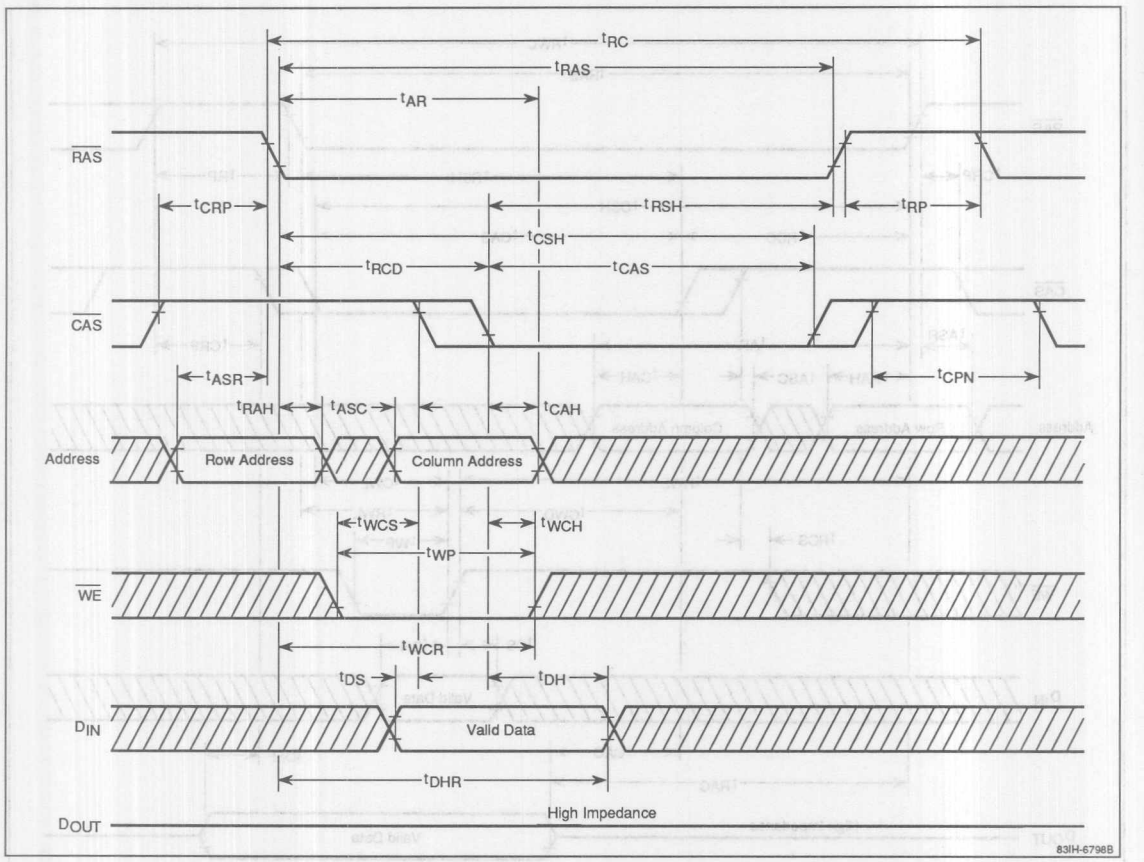
Timing Waveforms

Read Cycle



Timing Waveforms (cont)

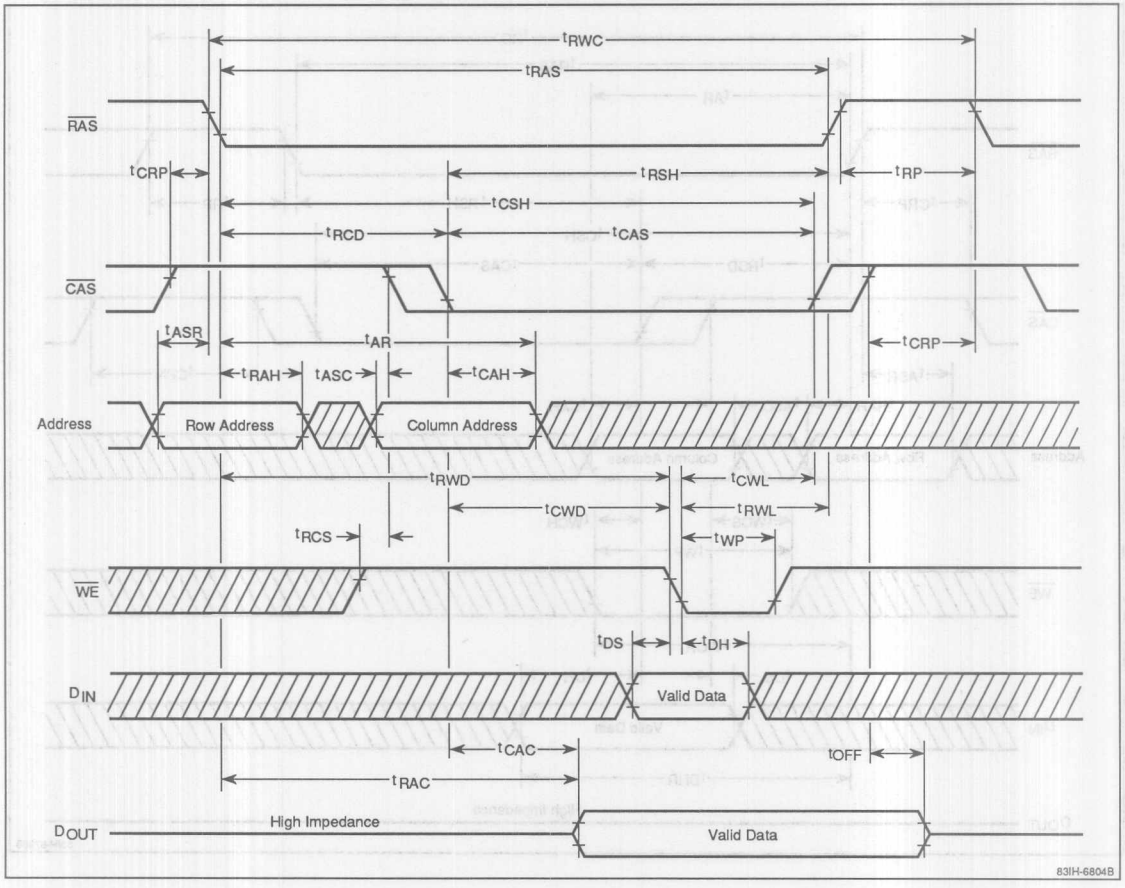
Early Write Cycle



5

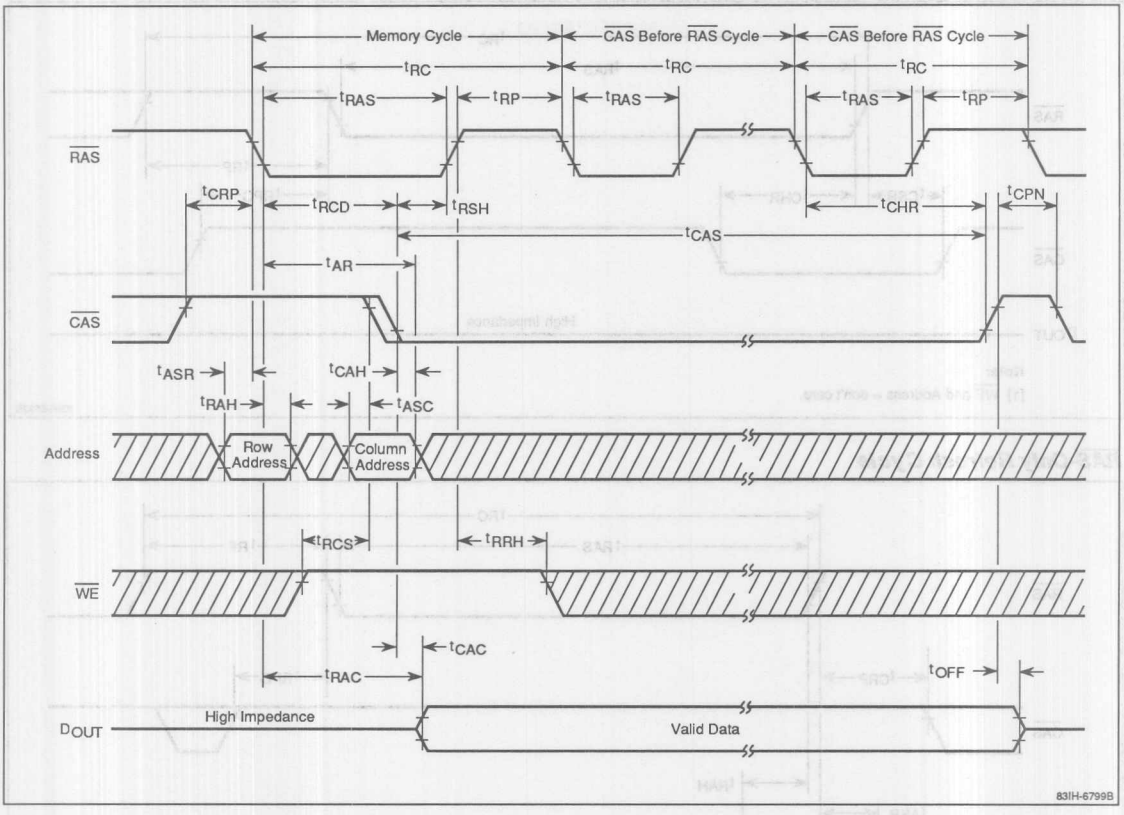
Timing Waveforms (cont)

Read-Write/Read-Modify-Write Cycle (D_{OUT} only)



Timing Waveforms (cont)

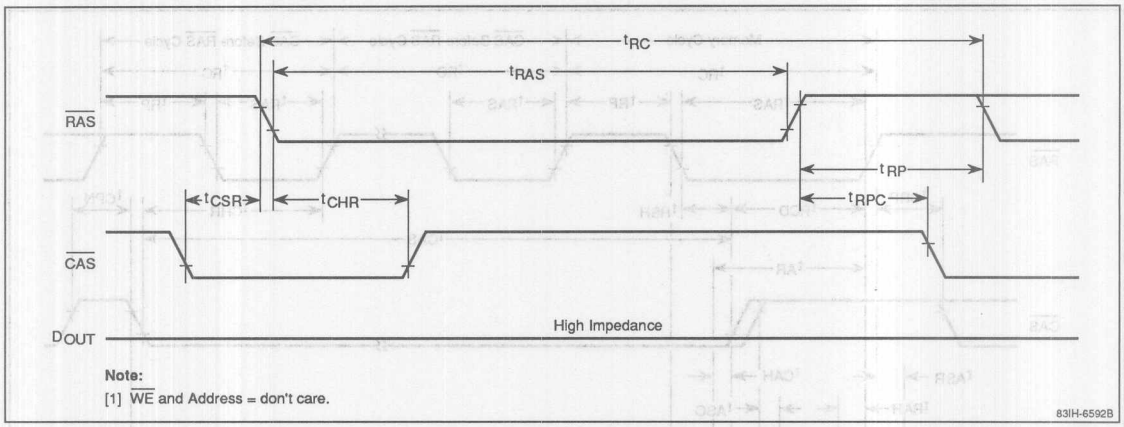
Hidden Refresh Cycle



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Timing Waveforms (cont)

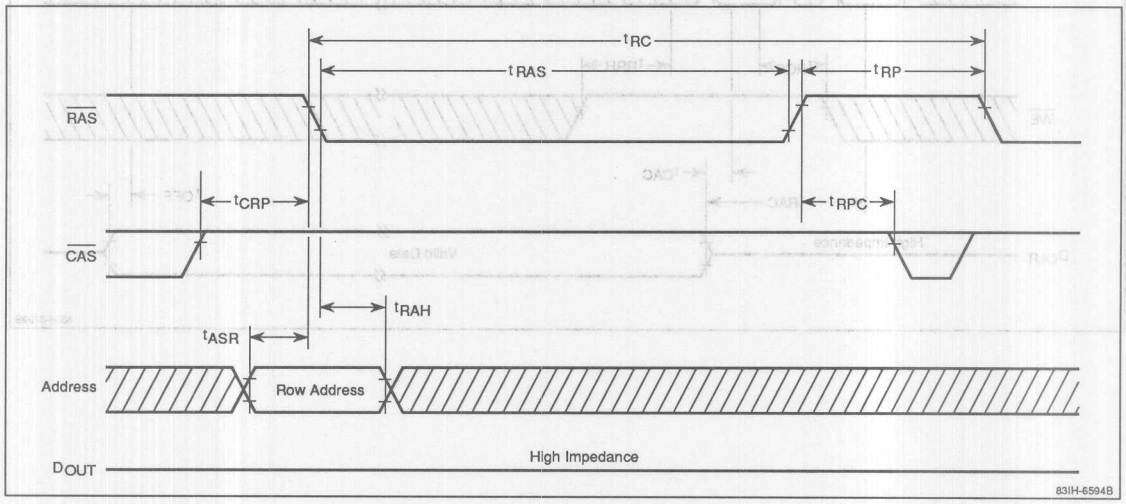
$\overline{CAS}$ Before $\overline{RAS}$ Refresh Cycle



Note:
[1] $\overline{WE}$ and Address = don't care.

83IH-6592B

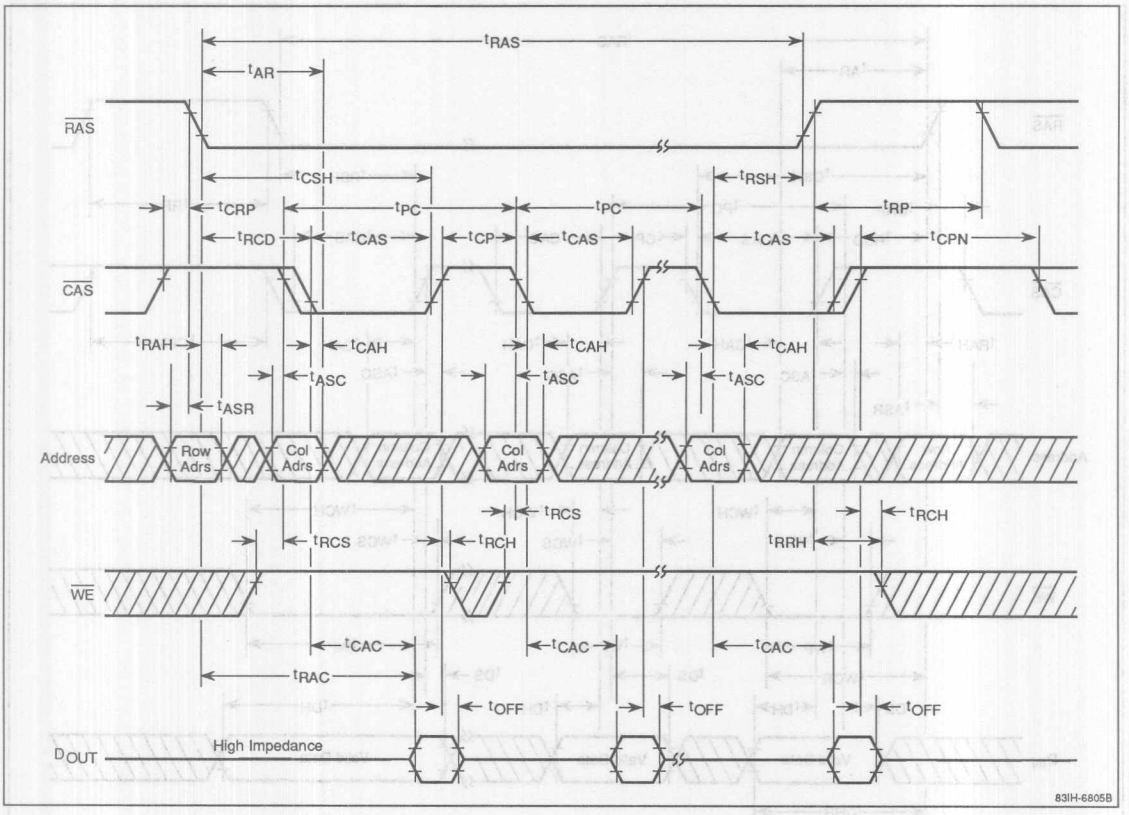
$\overline{RAS}$-Only Refresh Cycle



83IH-6594B

Timing Waveforms (cont)

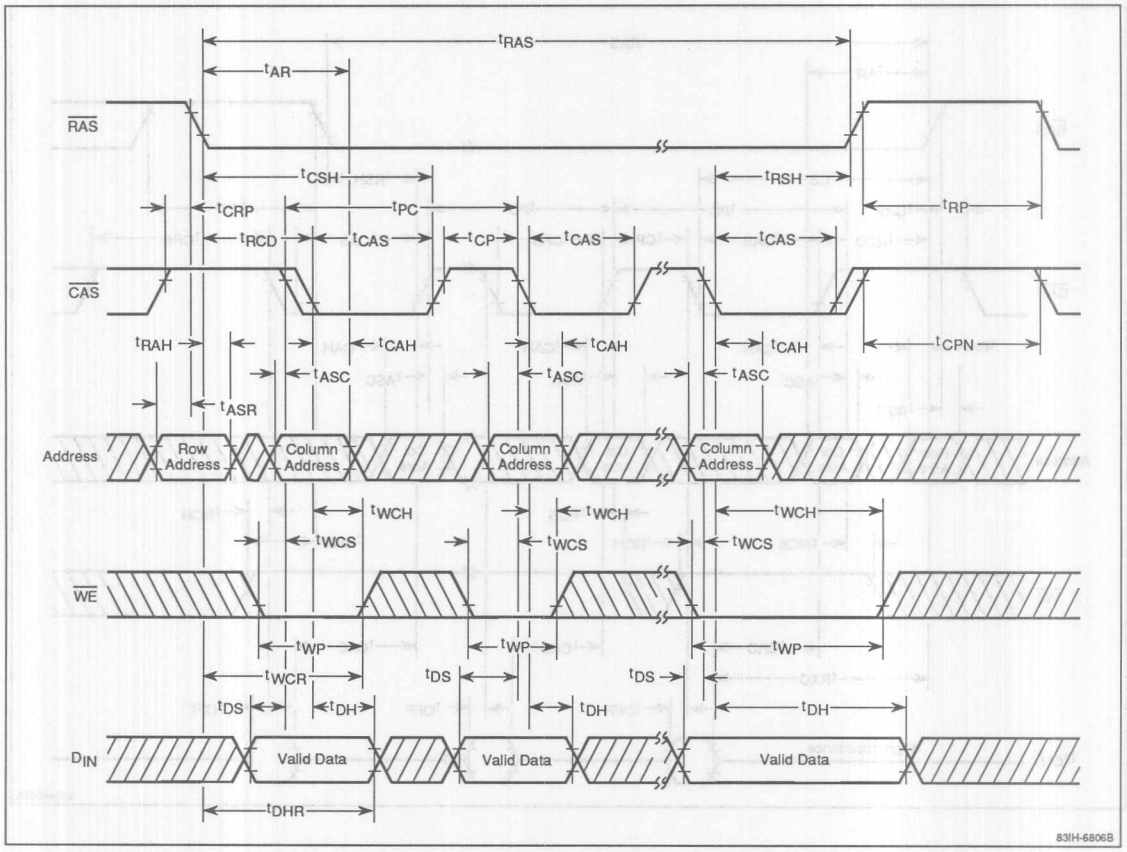
Page Read Cycle



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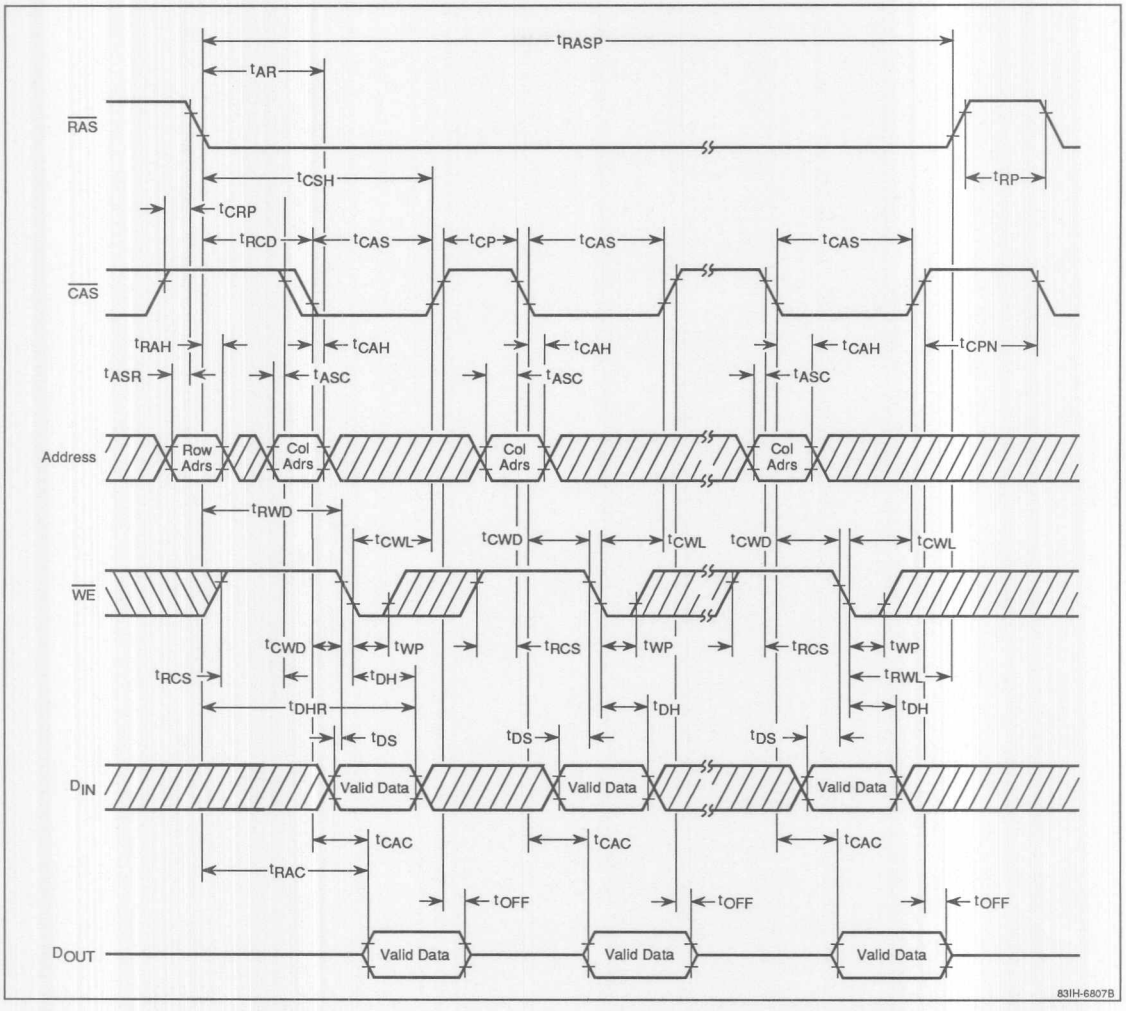
Timing Waveforms (cont)

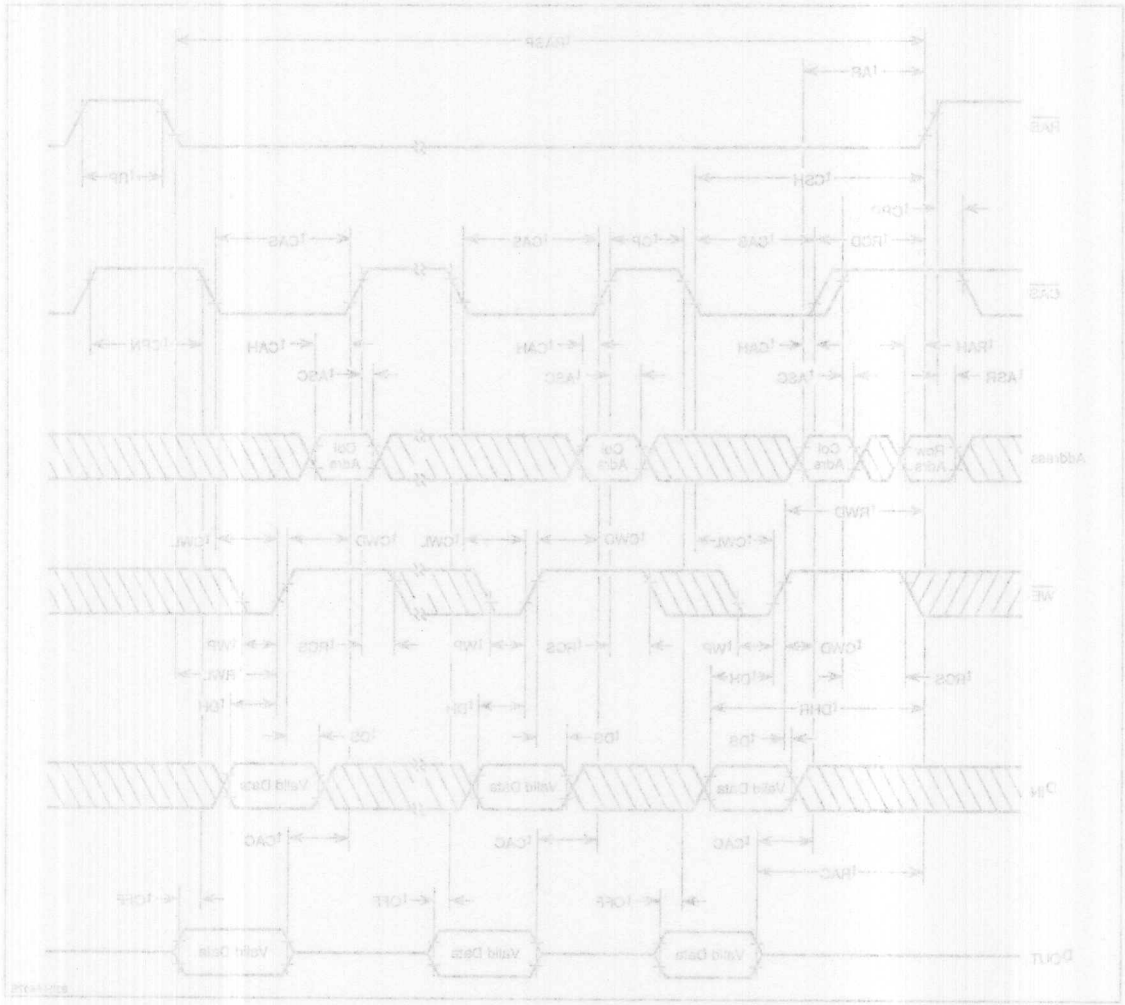
Page Early Write Cycle



Timing Waveforms (cont)

Page Read-Write/Read-Modify-Write Cycle (D_{OUT} only)





NEC Electronics Inc.

MC-421000A9
1,048,576 x 9-Bit
CMOS Dynamic RAM Module

Description

The MC-421000A9 is a fast-page, 1,048,576-word by 9-bit CMOS dynamic RAM module, designed to operate from a single +5 volt power supply. Advanced CMOS circuitry, including a single-transistor storage cell, 2048 sense amplifiers per data output, multiplexed address buffers and flexible refresh controls, provides good system operating margins.

The MC-421000A9 is functionally equivalent to eight μPD421000 standard 1M DRAMs plus a parity bit. Refreshing is accomplished by performing $\overline{RAS}$-only refresh cycles, hidden refresh cycles, $\overline{CAS}$ before $\overline{RAS}$ refresh cycles, or normal read or write cycles on the 512 address combinations of A_0-A_8 during an 8-ms period.

The Single Inline Memory Module (SIMM™) package reduces system cost, enhances reliability, and reduces the size and weight of a system. The SIMM includes nine μPD421000s in SOJ packages and nine power supply decoupling capacitors.

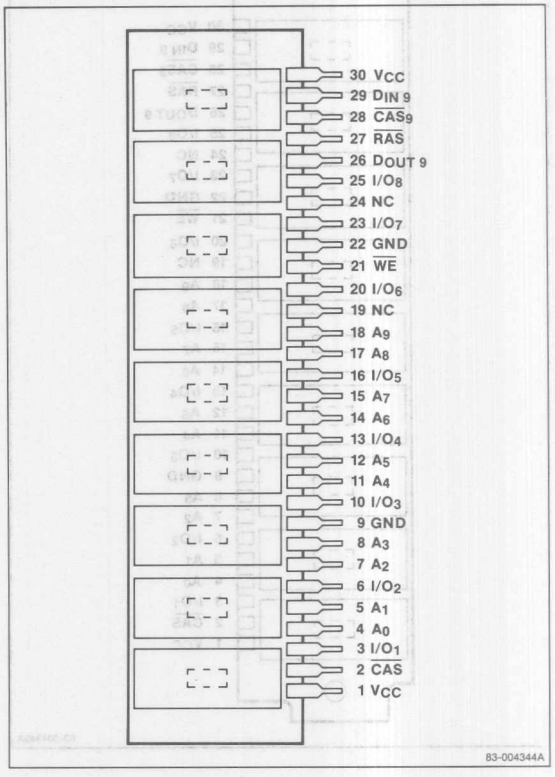
SIMM is a trademark of Wang Laboratories.

Features

- ☐ 1,048,576-word by 9-bit organization
- ☐ Single +5 V ± 10% power supply
- ☐ Standard 30-pin Single Inline Memory Module (SIMM) packaging
- ☐ Incorporates nine 1M dynamic RAMs in high-density SOJ packaging (μPD421000LA)
- ☐ Includes power supply decoupling capacitors
- ☐ Low power dissipation: 49.5 mW standby (max)
- ☐ TTL-compatible I/O
- ☐ 512 refresh cycles (A_0-A_8 are refresh address pins)
- ☐ Fast-page capability

Pin Configurations

30-Pin SIMM, MC-421000A9A



Ordering Information

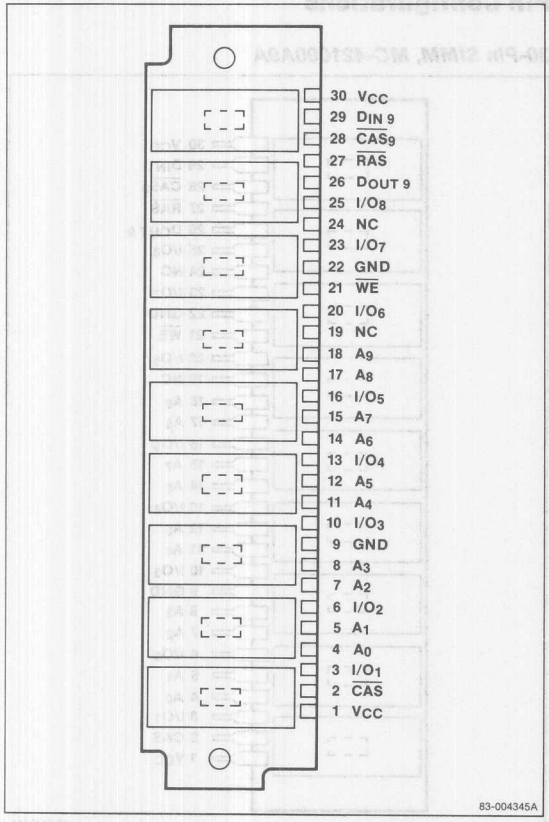
Part Number	Row Access Time (max)	Column Access Time (max)	Fast-Page Cycle Time (min)	Package
MC-421000A9A-70	70 ns	20 ns	45 ns	30-pin leaded SIMM
A-80	80 ns	20 ns	50 ns	
A-10	100 ns	25 ns	60 ns	
A-12	120 ns	30 ns	70 ns	
MC-421000A9B-70	70 ns	20 ns	45 ns	30-pin socketable SIMM
B-80	80 ns	20 ns	50 ns	
B-10	100 ns	25 ns	60 ns	
B-12	120 ns	70 ns	65 ns	

Notes:

(1) Contact your NEC sales representative for a copy of the MC-421000A9A-70 and MC-421000A9B-70 data sheets.

Pin Configurations (cont)

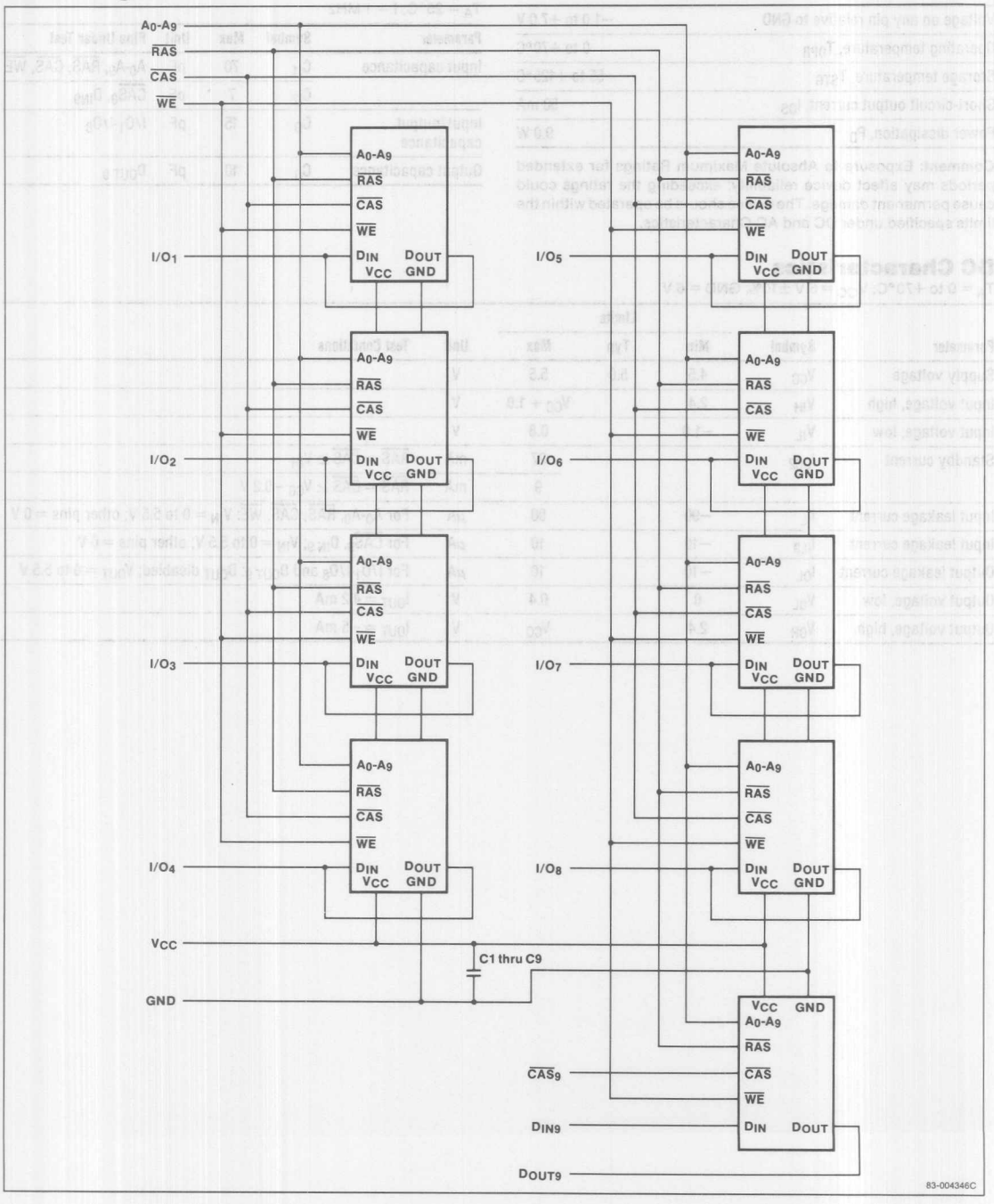
30-Pin SIMM, MC-421000A9B



Pin Identification

Symbol	Function
A_0-A_9	Address inputs
I/O_1-I/O_8	Common data inputs/outputs
$D_{IN\ 9}$	Data input 9
$D_{OUT\ 9}$	Data output 9
$\overline{RAS}$	Row address strobe
$\overline{CAS}$	Column address strobe
$\overline{CAS_9}$	Column address strobe for data output 9
$\overline{WE}$	Write enable
GND	Ground
V_{CC}	+5-volt power supply
NC	No connection

Block Diagram



Absolute Maximum Ratings

Voltage on any pin relative to GND	−1.0 to +7.0 V
Operating temperature, T_{OPR}	0 to +70°C
Storage temperature, T_{STG}	−55 to +125°C
Short-circuit output current, I_{OS}	50 mA
Power dissipation, P_D	9.0 W

Comment: Exposure to Absolute Maximum Ratings for extended periods may affect device reliability; exceeding the ratings could cause permanent damage. The device should be operated within the limits specified under DC and AC Characteristics.

Capacitance

$T_A = 25°C$; f = 1 MHz

Parameter	Symbol	Max	Unit	Pins Under Test
Input capacitance	C_{I1}	70	pF	A_0-A_9, $\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$
	C_{I2}	7	pF	$\overline{CAS}_9$, D_{IN9}
Input/output capacitance	C_D	15	pF	I/O_1-I/O_8
Output capacitance	C_O	10	pF	$D_{OUT\,9}$

DC Characteristics

$T_A = 0$ to +70°C; $V_{CC} = 5\ V \pm 10\%$; GND = 0 V

		Limits				
Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions
Supply voltage	V_{CC}	4.5	5.0	5.5	V	
Input voltage, high	V_{IH}	2.4		$V_{CC} + 1.0$	V	
Input voltage, low	V_{IL}	−1.0		0.8	V	
Standby current	I_{CC2}			27	mA	$\overline{RAS} = \overline{CAS} \geq V_{IH}$
				9	mA	$\overline{RAS} = \overline{CAS} \geq V_{CC} - 0.2\ V$
Input leakage current	I_{IL}	−90		90	μA	For A_0-A_9, $\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$: V_{IN} = 0 to 5.5 V; other pins = 0 V
Input leakage current	I_{IL9}	−10		10	μA	For $\overline{CAS}_9$, $D_{IN\,9}$; V_{IN} = 0 to 5.5 V; other pins = 0 V
Output leakage current	I_{OL}	−10		10	μA	For I/O_1-I/O_8 and $D_{OUT\,9}$: D_{OUT} disabled; V_{OUT} = 0 to 5.5 V
Output voltage, low	V_{OL}	0		0.4	V	$I_{OUT} = 4.2$ mA
Output voltage, high	V_{OH}	2.4		V_{CC}	V	$I_{OUT} = -5$ mA

AC Characteristics

$T_A = 0$ to $+70°C$; $V_{CC} = 5.0\ V \pm 10\%$

		Limits							
		MC-421000A9-80		MC-421000A9-10		MC-421000A9-12			
Parameter	Symbol	Min	Max	Min	Max	Min	Max	Unit	Test Conditions
Operating current, average	I_{CC1}		630		540		450	mA	$\overline{RAS}$, $\overline{CAS}$ cycling; $t_{RC} = t_{RC}$ min (Note 5)
Operating current, refresh cycle, average	I_{CC3}		630		540		450	mA	$\overline{RAS}$ cycling; $\overline{CAS} \geq V_{IH}$, $t_{RC} = t_{RC}$ min; $I_O = 0$ mA (Note 5)
Fast-page operating current, average	I_{CC4}		540		450		360	mA	$\overline{RAS} \leq V_{IL}$; $\overline{CAS}$ cycling; $t_{PC} = t_{PC}$ min; $I_O = 0$ mA (Note 5)
Operating current, $\overline{CAS}$ before $\overline{RAS}$ refreshing, average	I_{CC5}		630		540		450	mA	$t_{RC} = t_{RC}$ min; $I_O = 0$ mA (Note 5)
Random read or write cycle time	t_{RC}	160		190		220		ns	(Note 6)
Read-write cycle time	t_{RWC}	190		225		260		ns	(Notes 6, 20)
Fast-page cycle time	t_{PC}	50		60		70		ns	(Note 6)
Refresh period	t_{REF}		8		8		8	ms	
Access time from $\overline{RAS}$	t_{RAC}		80		100		120	ns	(Notes 7, 8)
Access time from $\overline{CAS}$ (falling edge)	t_{CAC}		20		25		30	ns	(Notes 7, 9, 10, 11)
Access time from column address	t_{AA}		45		50		60	ns	(Notes 7, 10, 11)
Access time from $\overline{CAS}$ precharge (rising edge)	t_{ACP}		45		55		65	ns	(Notes 7, 11)
Output buffer turnoff delay	t_{OFF}	0	20	0	25	0	30	ns	(Note 12)
Transition time (rise and fall)	t_T	3	50	3	50	3	50	ns	(Note 4)
$\overline{RAS}$ precharge time	t_{RP}	70		80		90		ns	
$\overline{RAS}$ pulse width	t_{RAS}	80	10000	100	10000	120	10000	ns	
Fast-page $\overline{RAS}$ pulse width	t_{RASP}	80	100000	100	100000	120	100000	ns	
$\overline{RAS}$ hold time	t_{RSH}	20		25		30		ns	
$\overline{CAS}$ pulse width	t_{CAS}	20	10000	25	10000	30	10000	ns	
$\overline{CAS}$ hold time	t_{CSH}	80		100		120		ns	
$\overline{RAS}$ to $\overline{CAS}$ delay time	t_{RCD}	25	60	25	75	25	90	ns	(Note 13)
$\overline{CAS}$ to $\overline{RAS}$ precharge time	t_{CRP}	10		10		10		ns	(Note 14)
$\overline{CAS}$ precharge time (non-page mode)	t_{CPN}	10		10		15		ns	
Fast-page $\overline{CAS}$ precharge time	t_{CP}	10	20	10	25	15	30	ns	(Note 11)
$\overline{RAS}$ precharge $\overline{CAS}$ hold time	t_{RPC}	0		0		0		ns	
Row address setup time	t_{ASR}	0		0		0		ns	
Row address hold time	t_{RAH}	12		12		15		ns	
$\overline{RAS}$ to column address delay time	t_{RAD}	17	35	17	50	20	60	ns	(Note 10)
Column address setup time	t_{ASC}	0	20	0	20	0	25	ns	(Note 11)
Column address hold time	t_{CAH}	20		20		25		ns	
Column address hold time referenced to $\overline{RAS}$	t_{AR}	60		70		85		ns	

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AC Characteristics (cont)

T_A = 0 to +70°C; V_{CC} = 5.0 V ±10%

Parameter	Symbol	Limits MC-421000A9-80 Min	MC-421000A9-80 Max	MC-421000A9-10 Min	MC-421000A9-10 Max	MC-421000A9-12 Min	MC-421000A9-12 Max	Unit	Test Conditions
Column address lead time referenced to $\overline{RAS}$ (rising edge)	t_{RAL}	45		55		65		ns	
Read command setup time	t_{RCS}	0		0		0		ns	
Read command hold time referenced to $\overline{RAS}$	t_{RRH}	10		10		10		ns	(Note 15)
Read command hold time referenced to $\overline{CAS}$	t_{RCH}	0		0		0		ns	(Note 15)
Write command hold time	t_{WCH}	15		20		25		ns	
Write command hold time referenced to $\overline{RAS}$	t_{WCR}	55		70		85		ns	
Write command pulse width	t_{WP}	15		20		25		ns	(Note 16)
Write command to $\overline{RAS}$ lead time	t_{RWL}	25		30		35		ns	
Write command to $\overline{CAS}$ lead time	t_{CWL}	15		20		25		ns	
Data-in setup time	t_{DS}	0		0		0		ns	(Note 17)
Data-in hold time	t_{DH}	20		20		25		ns	(Note 17)
Data-in hold time referenced to $\overline{RAS}$	t_{DHR}	60		70		85		ns	
Write command setup time	t_{WCS}	0		0		0		ns	(Note 18)
$\overline{CAS}$ to $\overline{WE}$ delay time	t_{CWD}	20		25		30		ns	(Notes 18, 20)
$\overline{RAS}$ to $\overline{WE}$ delay time	t_{RWD}	80		100		120		ns	(Notes 18, 20)
Column address to $\overline{WE}$ delay time	t_{AWD}	45		55		65		ns	(Notes 18, 20)
$\overline{CAS}$ setup time for $\overline{CAS}$ before $\overline{RAS}$ refreshing	t_{CSR}	10		10		10		ns	(Note 19)
$\overline{CAS}$ hold time for $\overline{CAS}$ before $\overline{RAS}$ refreshing	t_{CHR}	15		20		25		ns	(Note 19)

Notes:

(1) All voltages are referenced to GND.

(2) An initial pause of 100 μs is required after power-up, followed by any eight $\overline{RAS}$ cycles before proper device operation is achieved.

(3) Ac measurements assume t_T = 5 ns.

(4) V_{IH} (min) and V_{IL} (max) are reference levels for measuring timing of input signals. Transition times are measured between V_{IH} and V_{IL}.

(5) I_{CC1}, I_{CC3}, I_{CC4}, and I_{CC5} depend on output loading and cycle rates. Specified values are obtained with the output open. I_{CC3} is measured assuming that all column address inputs are held at either a high level or a low level during $\overline{RAS}$-only refresh cycles. I_{CC4} is measured assuming that all column address inputs are switched only once each fast-page cycle.

(6) The minimum specifications are used only to indicate the cycle time at which proper operation over the full temperature range (T_A = 0 to +70°C) is assured.

(7) Load = 2 TTL (−1 mA, +4 mA) loads and 100 pF (V_{OH} = 2.0 V, V_{OL} = 0.8 V).

(8) Assumes that $t_{RCD} \leq t_{RCD}$ (max) and $t_{RAD} \leq t_{RAD}$ (max). If t_{RCD} or t_{RAD} is greater than the maximum recommended value in this table, t_{RAC} increases by the amount that t_{RCD} or t_{RAD} exceeds the value shown.

(9) Assumes that $t_{RCD} \geq t_{RCD}$ (max) and $t_{RAD} \leq t_{RAD}$ (max).

(10) If $t_{RAD} \geq t_{RAD}$ (max), then the access time is defined by t_{AA}.

(11) For fast-page read operation, the definition of access time is as follows.

$\overline{CAS}$ and Column Address Input Conditions	Access Time Definition
$t_{CP} \leq t_{CP}$ (max), $t_{ASC} \geq t_{CP}$	t_{ACP}
$t_{CP} \leq t_{CP}$ (max), $t_{ASC} \leq t_{CP}$	t_{AA}
$t_{CP} \geq t_{CP}$ (max), $t_{ASC} \leq t_{ASC}$ (max)	t_{AA}
$t_{CP} \geq t_{CP}$ (max), $t_{ASC} \geq t_{CP}$	t_{CAC}

Notes [cont]:

(12) t_{OFF} (max) defines the time at which the output achieves the open-circuit condition and is not referenced to V_{OH} or V_{OL}.

(13) Operation within the t_{RCD} (max) limit assures that t_{RAC} (max) can be met. t_{RCD} (max) is specified as a reference point only; if t_{RCD} is greater than t_{RCD} (max), access time is controlled exclusively by t_{CAC}.

(14) The t_{CRP} requirement should be applicable for $\overline{RAS}$/$\overline{CAS}$ cycles preceded by any cycle.

(15) Either t_{RRH} or t_{RCH} must be satisfied for a read cycle.

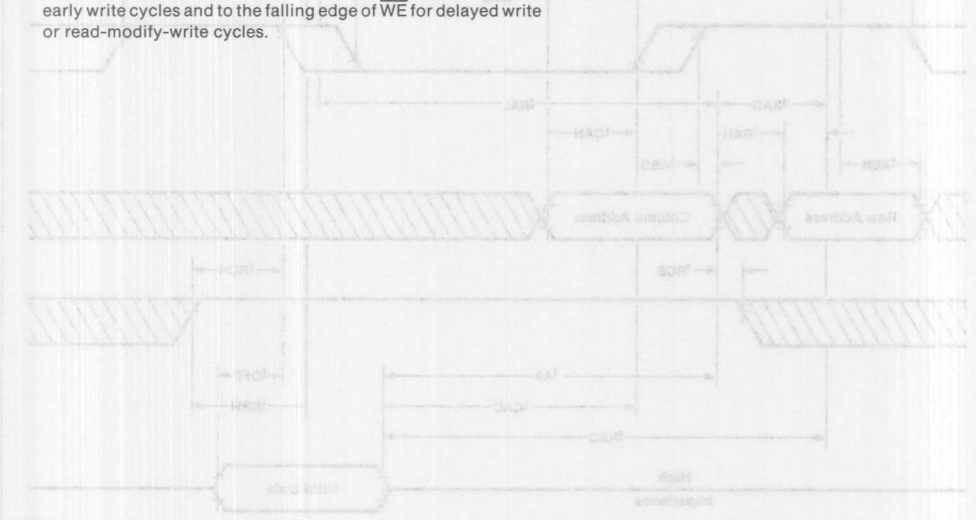
(16) Parameter t_{WP} is applicable for a delayed write cycle such as a read-write/read-modify-write cycle. For early write operation, both t_{WCS} and t_{WCH} must be met.

(17) These parameters are referenced to the falling edge of $\overline{CAS}$ for early write cycles and to the falling edge of $\overline{WE}$ for delayed write or read-modify-write cycles.

(18) For $D_{OUT\ 9}$, parameters t_{WCS}, t_{CWD}, t_{RWD}, and t_{AWD} are restrictive operating parameters in read-write/read-modify-write cycles only. If $t_{WCS} \geq t_{WCS}$ (min), the cycle is an early write cycle and the data output will remain open-circuit throughout the entire cycle. If $t_{CWD} \geq t_{CWD}$ (min), $t_{RWD} \geq t_{RWD}$ (min), and $t_{AWD} \geq t_{AWD}$ (min), the cycle is a read-write cycle and the data output will contain data read from the selected cell. If neither of the above conditions is met, the condition of $D_{OUT\ 9}$ (at access time and until $\overline{CAS}_9$ returns to V_{IH}) is indeterminate.

(19) $\overline{CAS}$ before $\overline{RAS}$ operation is specified.

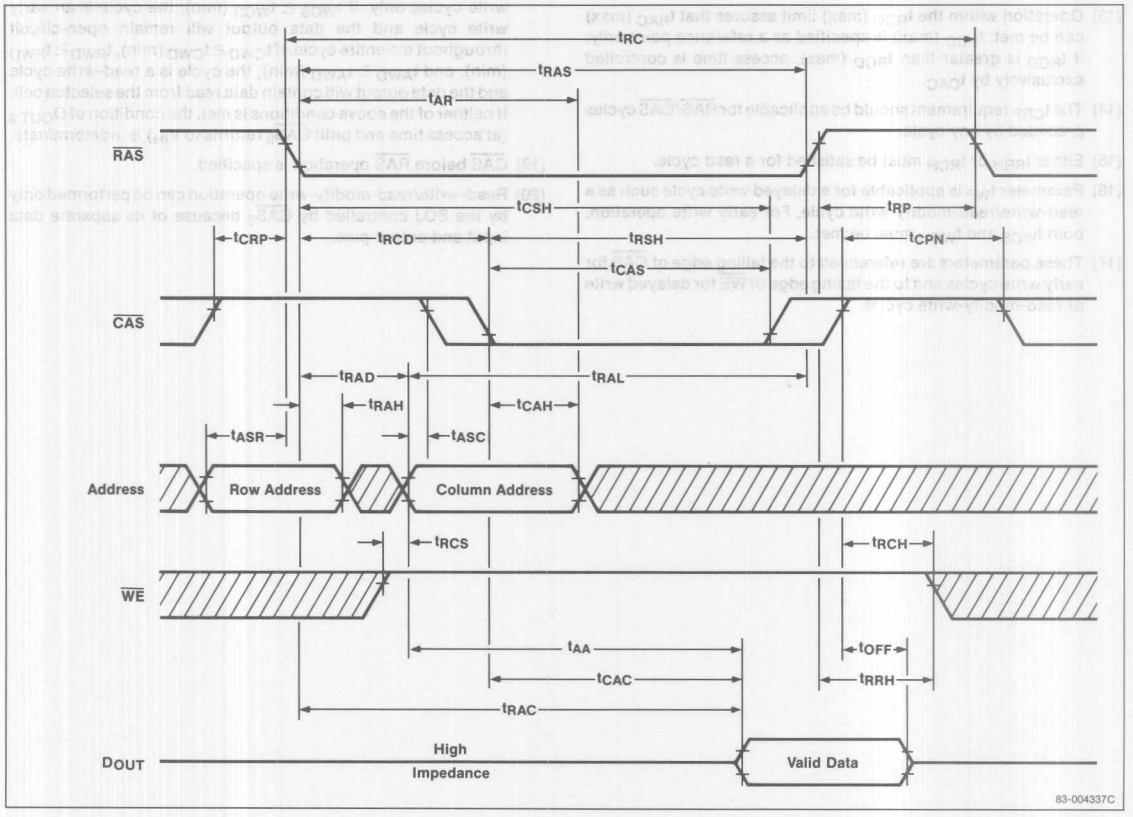
(20) Read-write/read-modify-write operation can be performed only by the SOJ controlled by $\overline{CAS}_9$ because of its separate data input and output pins.



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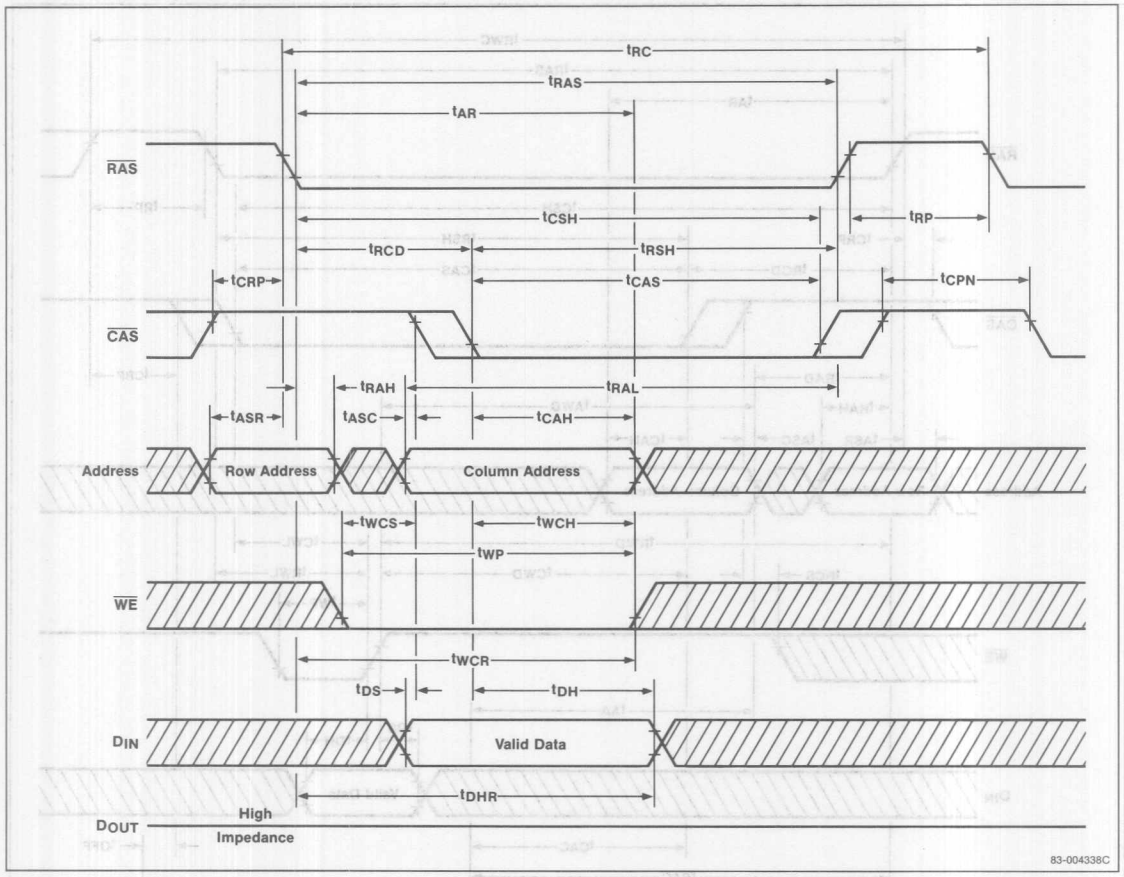
Timing Waveforms

Read Cycle



Timing Waveforms (cont)

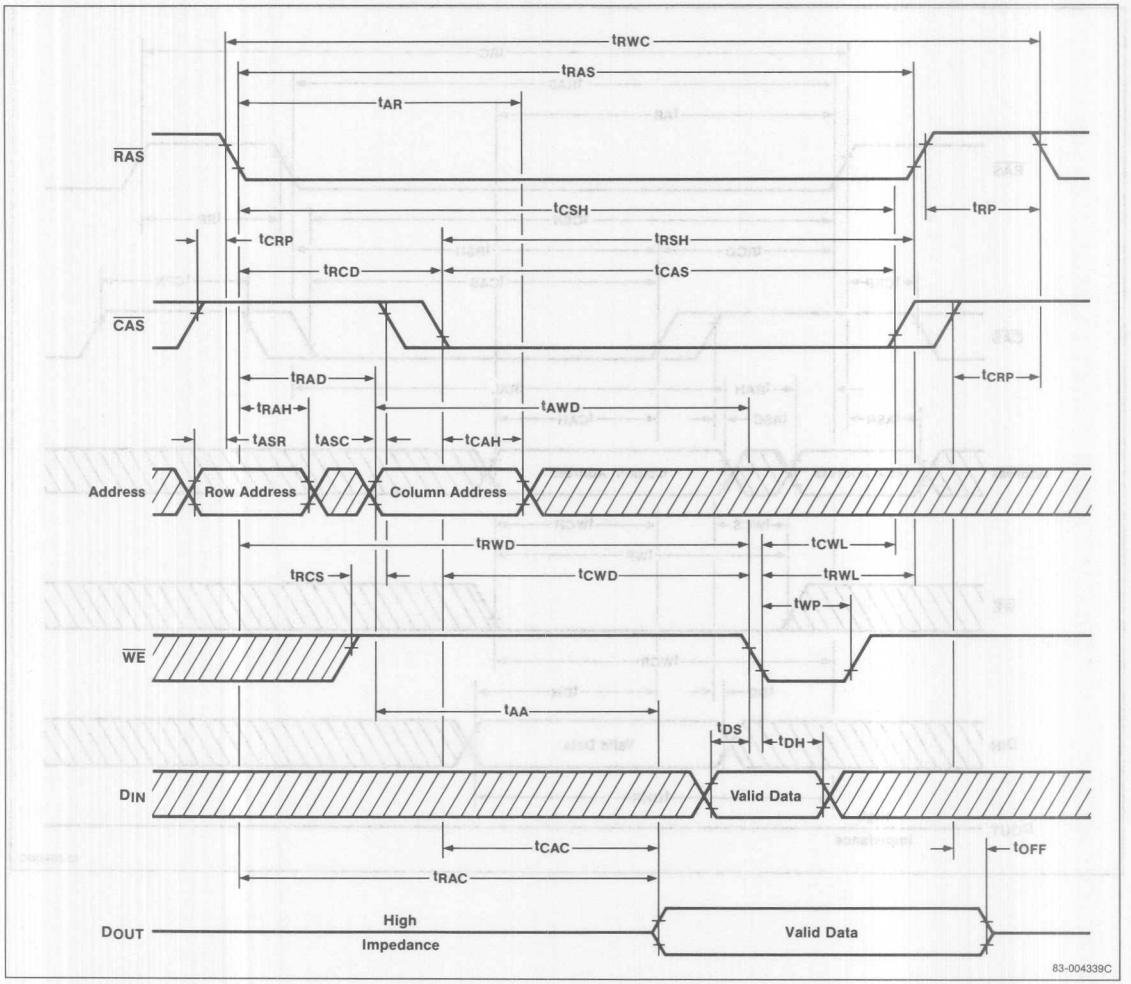
Write Cycle (Early Write)



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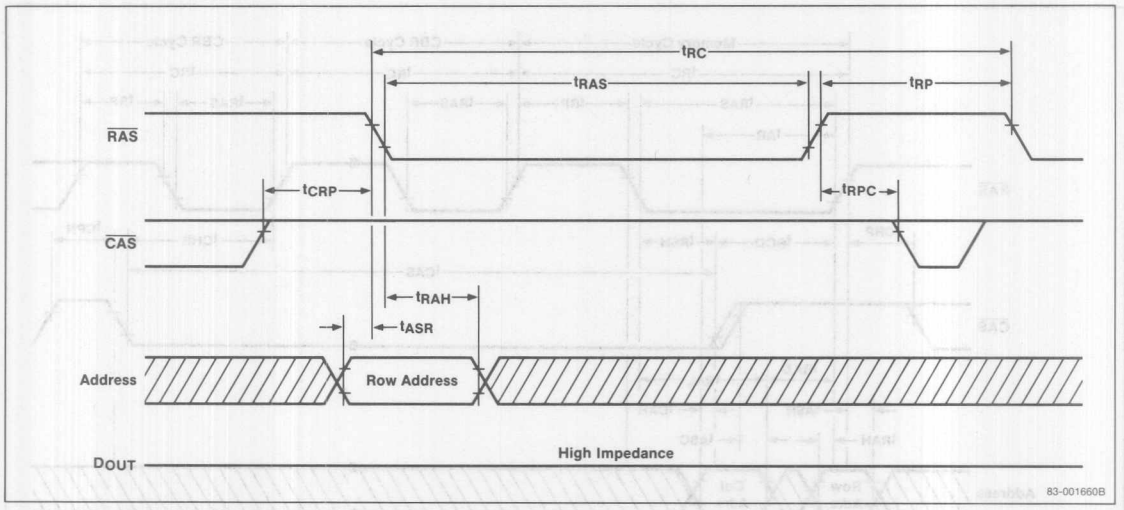
Timing Waveforms (cont)

Read-Write/Read-Modify-Write Cycle ($D_{OUT\ 9}$ only)



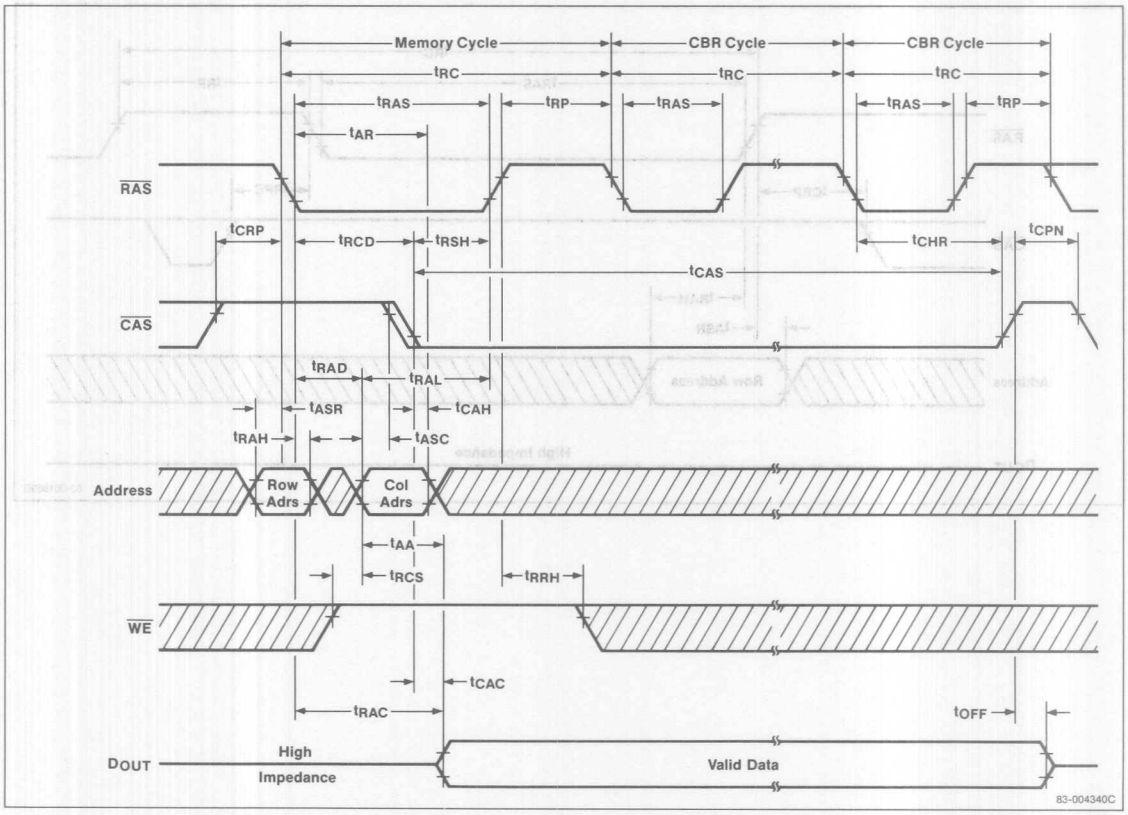
Timing Waveforms (cont)

$\overline{RAS}$-Only Refresh Cycle



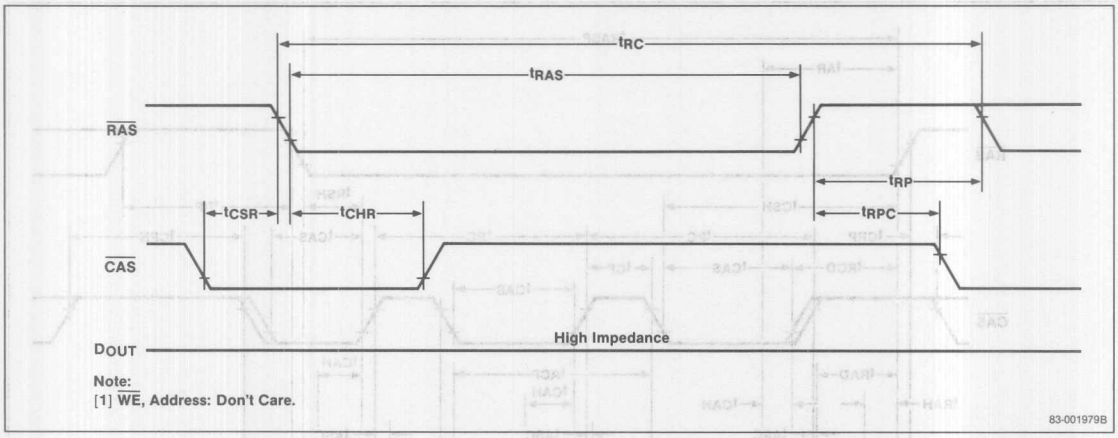
Timing Waveforms (cont)

Hidden Refresh Cycle



Timing Waveforms (cont)

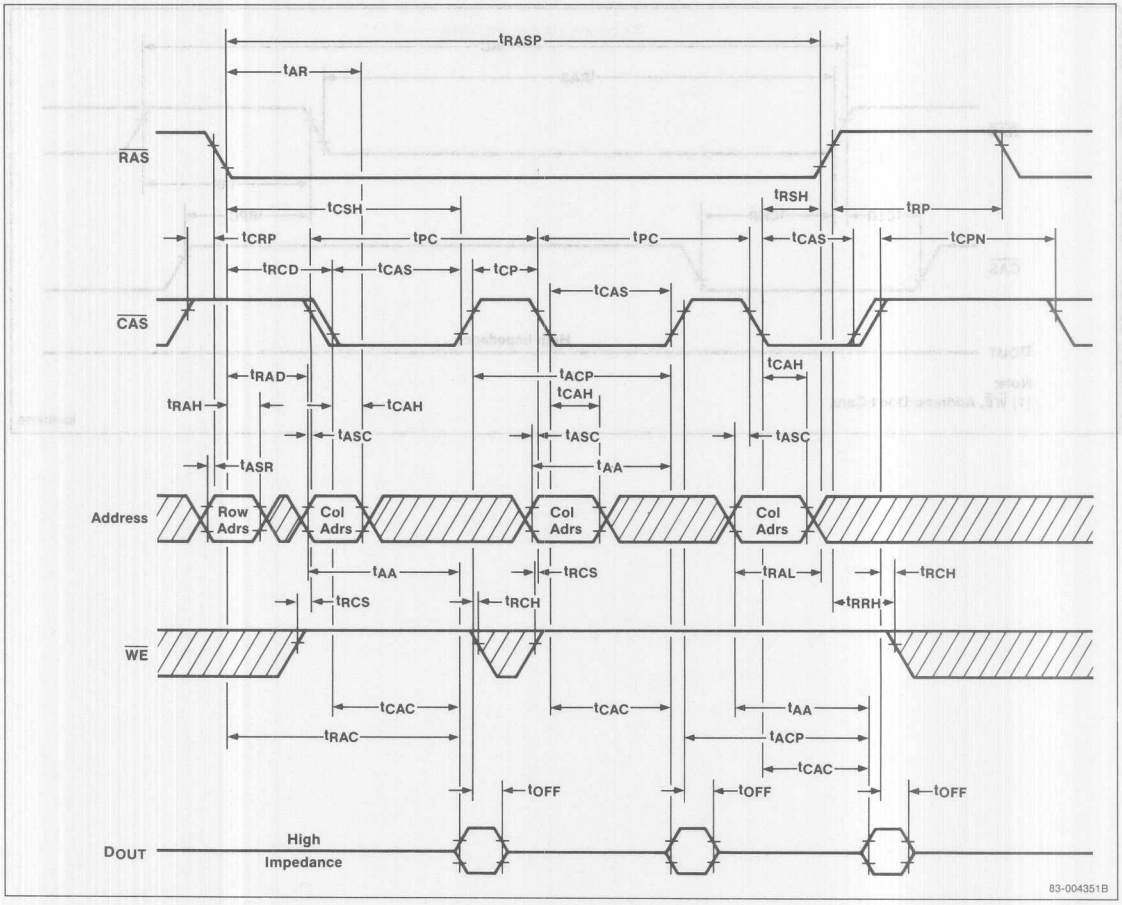
$\overline{CAS}$ Before $\overline{RAS}$ Refresh Cycle



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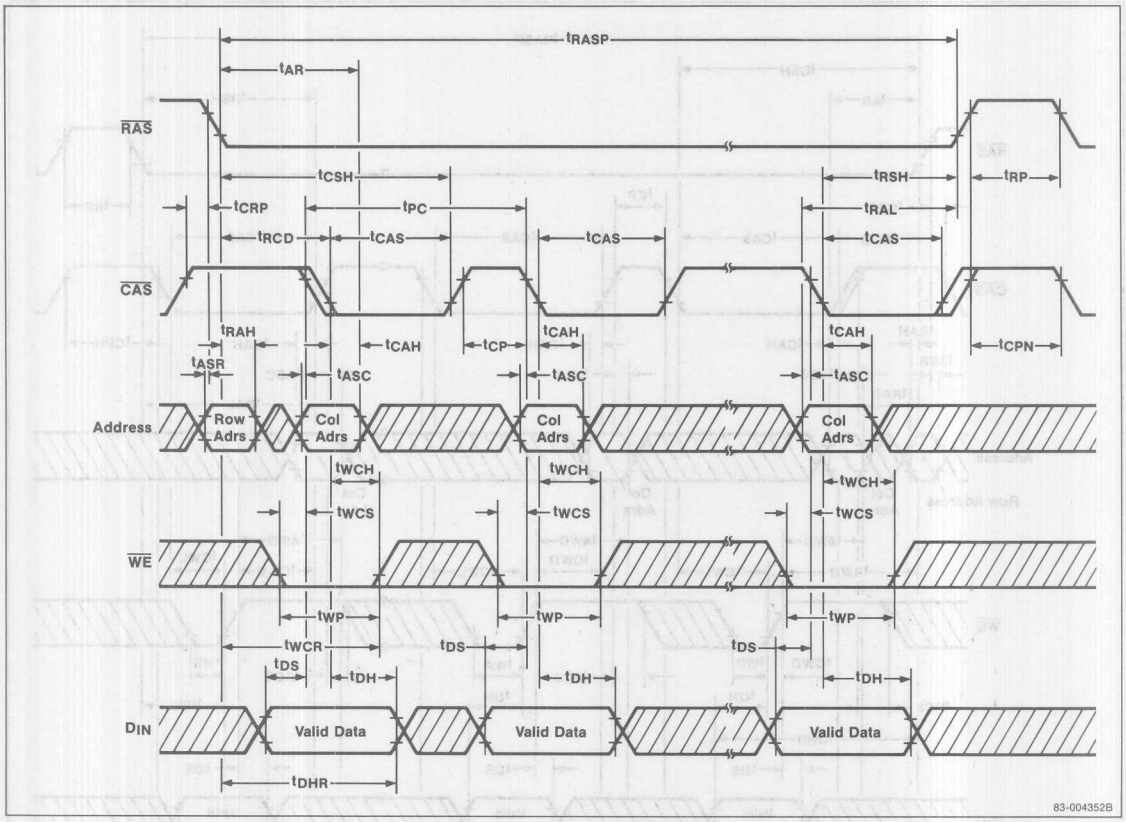
Timing Waveforms (cont)

Fast-Page Read Cycle



Timing Waveforms (cont)

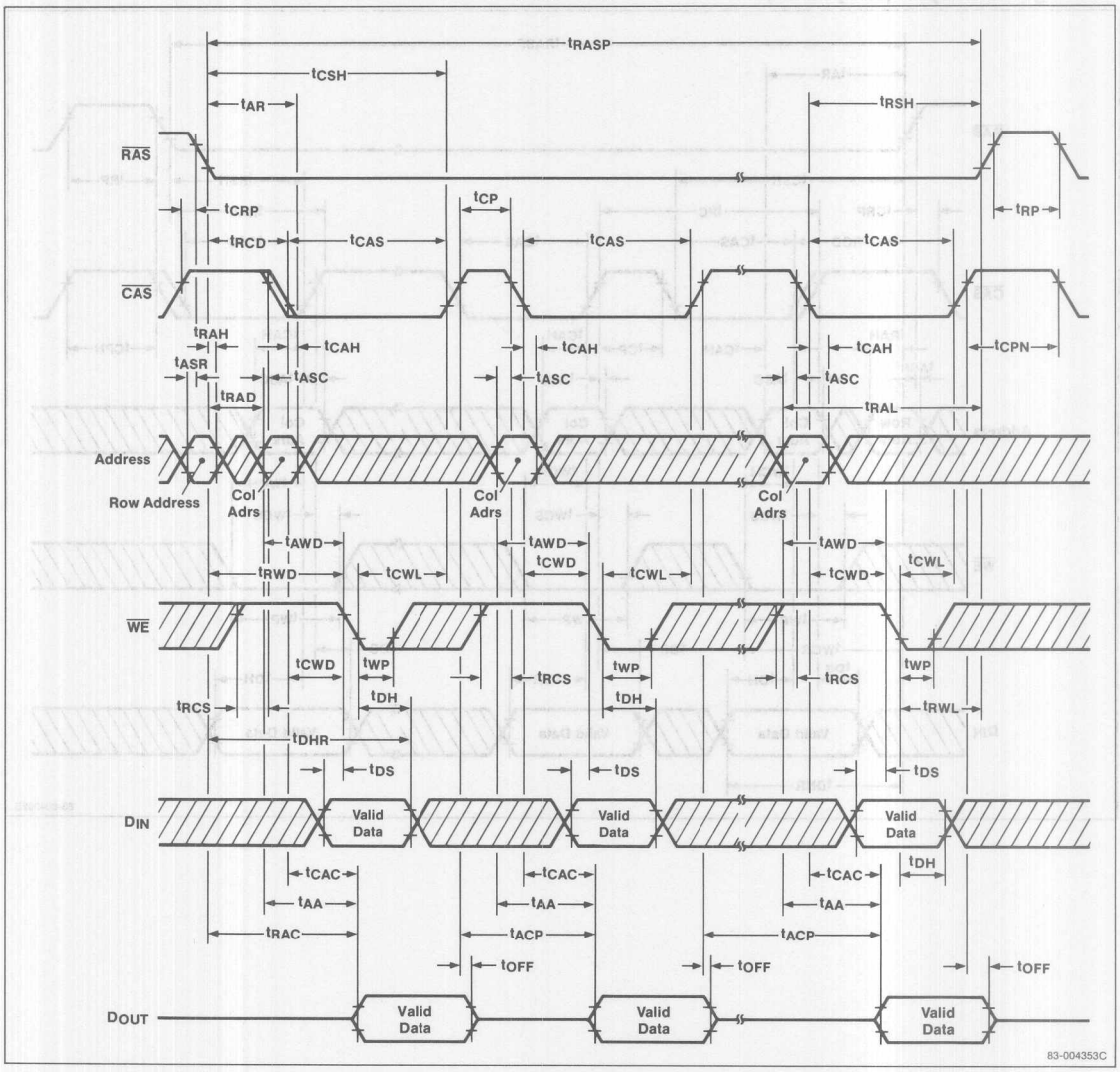
Fast-Page Write Cycle (Early Write)



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Timing Waveforms (cont)

Fast-Page Read-Write/Read-Modify-Write Cycle (D_{OUT} only)



NEC Electronics Inc.

MC-424100A9
4,194,304 x 9-Bit
Dynamic CMOS RAM Module

Description

The MC-424100A9 is a fast-page 4,194,304-word by 9-bit dynamic RAM module designed to operate from a single +5-volt power supply. Advanced CMOS circuitry, including a single-transistor storage cell, multiplexed address buffers and flexible refresh controls, provides good system operating margins.

The MC-424100A9 is functionally equivalent to eight μPD424100 standard 4M DRAMs plus a parity bit. Refreshing is accomplished by means of $\overline{RAS}$-only refresh cycles, hidden refresh cycles, $\overline{CAS}$ before $\overline{RAS}$ refresh cycles, or by normal read or write cycles on the 1024 address combinations of A_0 through A_9 during a 16-ms period.

Single Inline Memory Module (SIMM™) packaging enhances reliability and reduces the size, weight and cost of a system. The SIMM includes nine μPD424100s in SOJ packages and nine power supply decoupling capacitors.

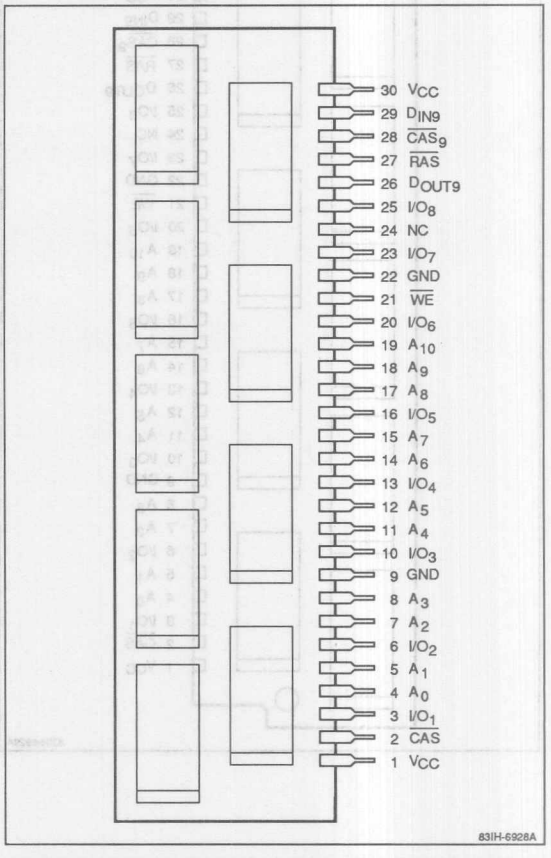
SIMM is a trademark of Wang Laboratories.

Features

- 4,194,304-word by 9-bit organization
- Single +5 V ± 10% power supply
- Standard 30-pin SIMM packaging
- Nine 4M dynamic RAMs incorporated in high-density SOJ packaging (μPD424100LA)
- Nine power supply decoupling capacitors
- Low power dissipation of 49.5 mW standby (max)
- TTL-compatible inputs and outputs
- 1024 refresh cycles every 16 ms
- Fast-page capability

Pin Configurations

30-Pin Leaded SIMM



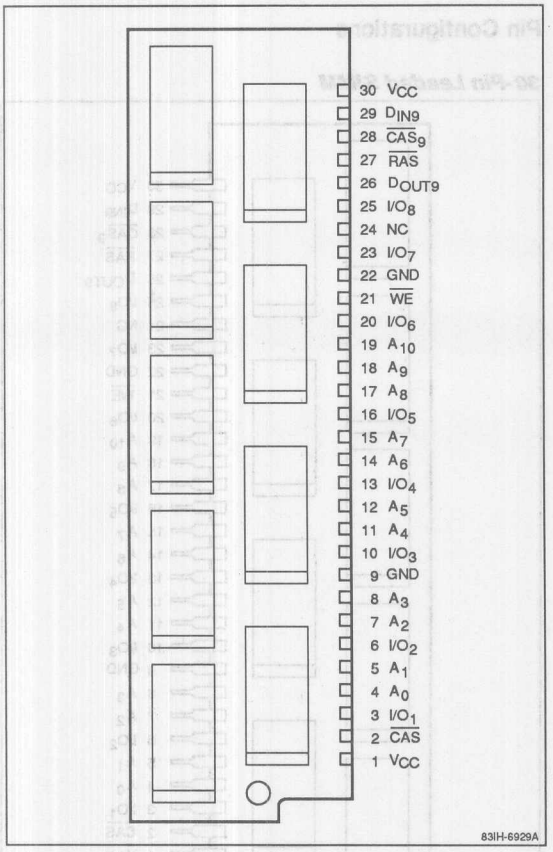
Ordering Information

Part Number	Column Access Time (max)	Row Access Time (max)	Fast Page Cycle Time (min)	Package
MC-424100A9A-80	80 ns	20 ns	50 ns	30-pin leaded SIMM
A-10	100 ns	25 ns	60 ns	
MC-424100A9B-80	80 ns	20 ns	50 ns	30-pin socket-mountable SIMM
B-10	100 ns	25 ns	60 ns	

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Pin Configurations (cont)

30-Pin Socket-Mountable SIMM



Pin Identification

Symbol	Function
A_0 - A_{10}	Address inputs
I/O_1 - I/O_8	Common data inputs/outputs
D_{IN9}	Data input 9
D_{OUT9}	Data output 9
$\overline{CAS}$	Column address strobe
$\overline{CAS}_9$	Column address strobe for data output 9
$\overline{RAS}$	Row address strobe
$\overline{WE}$	Write enable
GND	Ground
V_{CC}	+5-volt power supply
NC	No connection

Absolute Maximum Ratings

Voltage on any pin relative to GND	−1.0 to +7.0 V
Operating temperature, T_{OPR}	0 to +70°C
Storage temperature, T_{STG}	−55 to +125°C
Short-circuit output current, I_{OS}	50 mA
Power dissipation, P_D	9.0 W

Exposure to Absolute Maximum Ratings for extended periods may affect device reliability; exceeding the ratings could cause permanent damage. The device should be operated within the limits specified under DC and AC Characteristics.

Recommended Operating Conditions

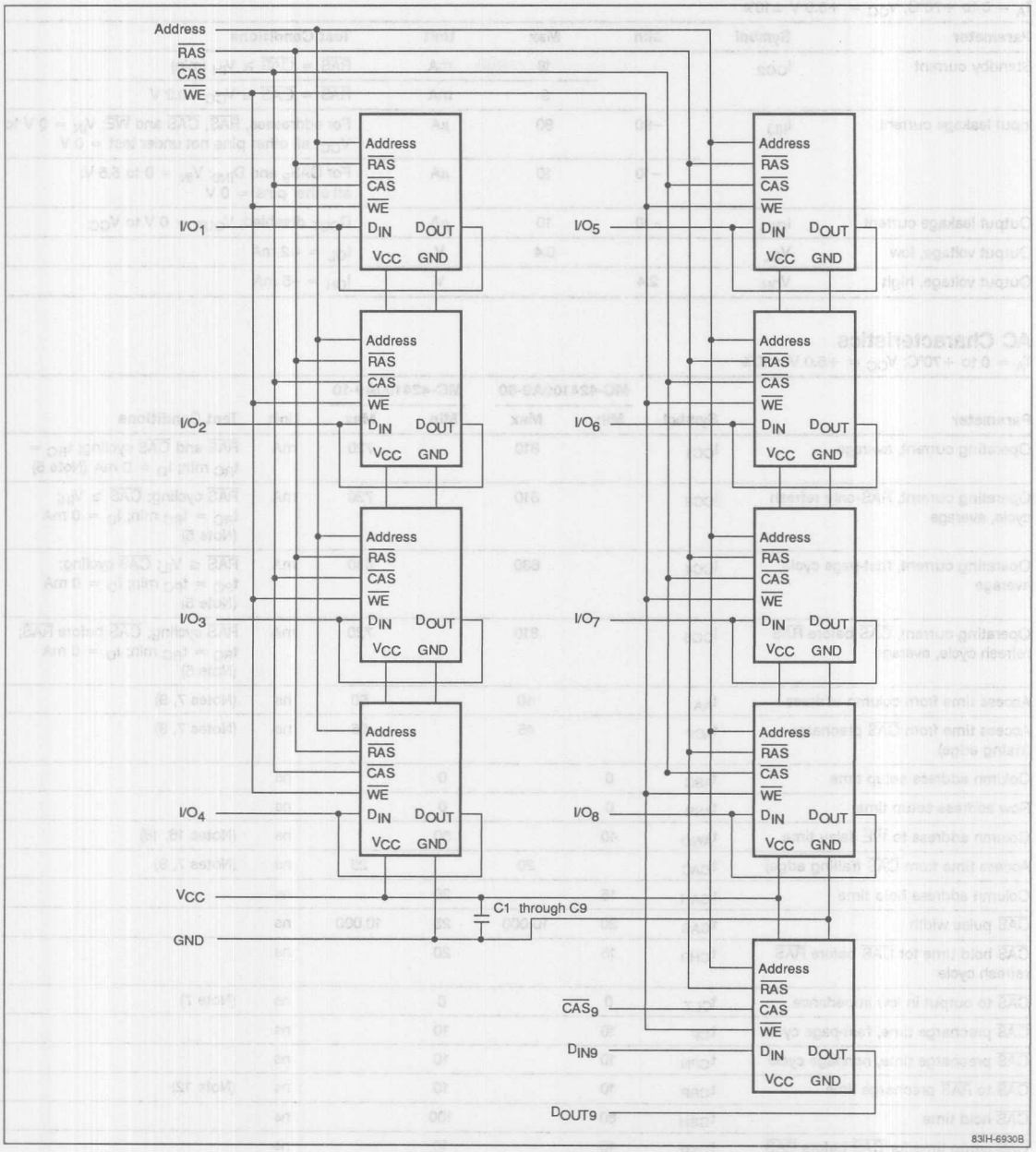
Parameter	Symbol	Min	Typ	Max	Unit
Input voltage, high	V_{IH}	2.4		V_{CC} + 1.0	V
Input voltage, low	V_{IL}	−1.0		0.8	V
Supply voltage	V_{CC}	4.5	5.0	5.5	V
Ambient temperature	T_A	0		70	°C

Capacitance

T_A = 25°C; f = 1 MHz

Parameter	Symbol	Max	Unit	Pins Under Test
Input capacitance	C_{I1}	70	pF	Address, D_{IN}
	C_{I2}	7	pf	$\overline{CAS}_9$, D_{IN9}
Input/output capacitance	C_D	10	pF	D_{OUT9}
	C_{IO}	15	pF	I/O_1 through I/O_8

Block Diagram



DC Characteristics

T_A = 0 to +70°C; V_{CC} = +5.0 V ±10%

Parameter	Symbol	Min	Max	Unit	Test Conditions
Standby current	I_{CC2}		18	mA	$\overline{RAS}$ = $\overline{CAS}$ ≥ V_{IH} (min)
			9	mA	$\overline{RAS}$ = $\overline{CAS}$ ≥ V_{CC} – 0.2 V
Input leakage current	$I_{I(L)}$	–90	90	μA	For addresses, $\overline{RAS}$, $\overline{CAS}$ and $\overline{WE}$: V_{IN} = 0 V to V_{CC}; all other pins not under test = 0 V
		–10	10	μA	For $\overline{CAS}_9$ and D_{IN9}: V_{IN} = 0 to 5.5 V; all other pins = 0 V
Output leakage current	$I_{O(L)}$	–10	10	μA	D_{OUT} disabled; V_{OUT} = 0 V to V_{CC}
Output voltage, low	V_{OL}		0.4	V	I_{OL} = 4.2 mA
Output voltage, high	V_{OH}	2.4		V	I_{OH} = –5 mA

AC Characteristics

T_A = 0 to +70°C; V_{CC} = +5.0 V ±10%

		MC-424100A9-80		MC-424100A9-10			
Parameter	Symbol	Min	Max	Min	Max	Unit	Test Conditions
Operating current, average	I_{CC1}		810		720	mA	$\overline{RAS}$ and $\overline{CAS}$ cycling; t_{RC} = t_{RC} min; I_O = 0 mA (Note 5)
Operating current, $\overline{RAS}$-only refresh cycle, average	I_{CC3}		810		720	mA	$\overline{RAS}$ cycling; $\overline{CAS}$ ≥ V_{IH}; t_{RC} = t_{RC} min; I_O = 0 mA (Note 5)
Operating current, fast-page cycle, average	I_{CC4}		630		540	mA	$\overline{RAS}$ ≤ V_{IL}; $\overline{CAS}$ cycling; t_{PC} = t_{PC} min; I_O = 0 mA (Note 5)
Operating current, $\overline{CAS}$ before $\overline{RAS}$ refresh cycle, average	I_{CC5}		810		720	mA	$\overline{RAS}$ cycling; $\overline{CAS}$ before $\overline{RAS}$; t_{RC} = t_{RC} min; I_O = 0 mA (Note 5)
Access time from column address	t_{AA}		40		50	ns	(Notes 7, 9)
Access time from $\overline{CAS}$ precharge (rising edge)	t_{ACP}		45		55	ns	(Notes 7, 9)
Column address setup time	t_{ASC}	0		0		ns	
Row address setup time	t_{ASR}	0		0		ns	
Column address to $\overline{WE}$ delay time	t_{AWD}	40		50		ns	(Notes 16, 18)
Access time from $\overline{CAS}$ (falling edge)	t_{CAC}		20		25	ns	(Notes 7, 9)
Column address hold time	t_{CAH}	15		20		ns	
$\overline{CAS}$ pulse width	t_{CAS}	20	10,000	25	10,000	ns	
$\overline{CAS}$ hold time for $\overline{CAS}$ before $\overline{RAS}$ refresh cycle	t_{CHR}	15		20		ns	
$\overline{CAS}$ to output in low impedance	t_{CLZ}	0		0		ns	(Note 7)
$\overline{CAS}$ precharge time, fast-page cycle	t_{CP}	10		10		ns	
$\overline{CAS}$ precharge time, nonpage cycle	t_{CPN}	10		10		ns	
$\overline{CAS}$ to $\overline{RAS}$ precharge time	t_{CRP}	10		10		ns	(Note 12)
$\overline{CAS}$ hold time	t_{CSH}	80		100		ns	
$\overline{CAS}$ setup time for $\overline{CAS}$ before $\overline{RAS}$ refresh cycle	t_{CSR}	10		10		ns	
$\overline{CAS}$ to $\overline{WE}$ delay	t_{CWD}	20		25		ns	(Notes 16, 18)

AC Characteristics (cont)

Parameter	Symbol	MC-424100A9-80 Min	MC-424100A9-80 Max	MC-424100A9-10 Min	MC-424100A9-10 Max	Unit	Test Conditions
Write command to $\overline{CAS}$ lead time	t_{CWL}	15		20		ns	(Note 18)
Data-in hold time	t_{DH}	15		20		ns	(Note 15)
Data-in setup time	t_{DS}	0		0		ns	(Note 15)
Output buffer turnoff delay	t_{OFF}	0	20	0	25	ns	(Note 10)
Fast-page cycle time	t_{PC}	50		60		ns	(Note 6)
Fast-page read-modify-write cycle time	t_{PRWC}	80		95		ns	(Note 6, 18)
Access time from $\overline{RAS}$	t_{RAC}		80		100	ns	(Notes 7, 8)
$\overline{RAS}$ to column address delay time	t_{RAD}	17	40	17	50	ns	(Note 9)
Row address hold time	t_{RAH}	12		12		ns	
Column address lead time referenced to $\overline{RAS}$ (rising edge)	t_{RAL}	40		50		ns	
$\overline{RAS}$ pulse width	t_{RAS}	80	10,000	100	10,000	ns	
$\overline{RAS}$ pulse width, fast-page cycle	t_{RASP}	80	125,000	100	125,000	ns	
Random read or write cycle time	t_{RC}	160		190		ns	(Note 6)
$\overline{RAS}$ to $\overline{CAS}$ delay time	t_{RCD}	25	60	25	75	ns	(Note 11)
Read command hold time referenced to $\overline{CAS}$	t_{RCH}	0		0		ns	(Note 13)
Read command setup time	t_{RCS}	0		0		ns	
Refresh period	t_{REF}		16		16	ms	Addresses A_0 through A_9
$\overline{RAS}$ precharge time	t_{RP}	70		80		ns	
$\overline{RAS}$ precharge $\overline{CAS}$ hold time	t_{RPC}	10		10		ns	
Read command hold time referenced to $\overline{RAS}$	t_{RRH}	10		10		ns	(Note 13)
$\overline{RAS}$ hold time	t_{RSH}	20		25		ns	
Read-write cycle time	t_{RWC}	185		220		ns	(Notes 6, 18)
$\overline{RAS}$ to $\overline{WE}$ delay	t_{RWD}	80		100		ns	(Notes 16, 18)
Write command to $\overline{RAS}$ lead time	t_{RWL}	20		25		ns	
Rise and fall transition time	t_T	3	50	3	50	ns	(Note 3)
Write command hold time	t_{WCH}	15		20		ns	
Write command setup time	t_{WCS}	0		0		ns	(Note 16)
$\overline{WE}$ hold time	t_{WHR}	15		20		ns	
Write command pulse width	t_{WP}	15		20		ns	(Note 14)
$\overline{WE}$ setup time	t_{WSR}	10		10		ns	

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Notes:

(1) All voltages are referenced to GND.

(2) An initial pause of 100 μs is required after power-up, followed by any eight $\overline{RAS}$ cycles, before proper device operation is achieved. At the end of the initial power-up sequence, it is recommended that either a $\overline{RAS}$-only refresh or a $\overline{CAS}$ before $\overline{RAS}$ refresh cycle be executed while $\overline{WE} \geq V_{IH}$ to ensure normal operation.

(3) AC measurements assume $t_T = 5$ ns.

(4) V_{IH} (min) and V_{IL} (max) are reference levels for measuring the timing of input signals. Transition times are measured between V_{IH} and V_{IL}.

(5) I_{CC1}, I_{CC3}, I_{CC4}, and I_{CC5} depend on output loading and cycle rates. Specified values are obtained with the output open. I_{CC3} is measured assuming that all column address inputs are held at either a high level or a low level during $\overline{RAS}$-only refresh cycles. I_{CC4} is measured assuming that all column address inputs are switched only once during each fast-page cycle.

(6) The minimum specifications are used only to indicate the cycle time at which proper operation over the full temperature range (T_A = 0 to +70°C) is assured.

(7) Load = 2 TTL (–1 mA, +4 mA) loads and 100 pF (V_{OH} = 2.0 V, V_{OL} = 0.8 V).

(8) Assumes that $t_{RCD} \leq t_{RCD}$ (max) and $t_{RAD} \leq t_{RAD}$ (max). If t_{RCD} or t_{RAD} is greater than the maximum recommended value in this table, t_{RAC} increases by the amount that t_{RCD} or t_{RAD} exceeds the value shown.

(9) If $t_{RAD} \geq t_{RAD}$ (max), then the access time is defined by t_{AA}.

(10) t_{OFF} (max) defines the time at which the output achieves the open-circuit condition and is not referenced to V_{OH} or V_{OL}.

(11) Operation within the t_{RCD} (max) limit assures that t_{RAC} (max) can be met. t_{RCD} (max) is specified as a reference point only; if t_{RCD} is greater than t_{RCD} (max), then access time is controlled exclusively by t_{CAC}.

(12) The t_{CRP} requirement should be applicable for $\overline{RAS}/\overline{CAS}$ cycles preceded by any cycle.

(13) Either t_{RRH} or t_{RCH} must be satisfied for a read cycle.

(14) Parameter t_{WP} is applicable for a delayed write cycle such as a read-write/read-modify-write cycle. For early write operation, both t_{WCS} and t_{WCH} must be met.

(15) These parameters are referenced to the falling edge of $\overline{CAS}$ for early write cycles and to the falling edge of $\overline{WE}$ for delayed write or read-modify-write cycles.

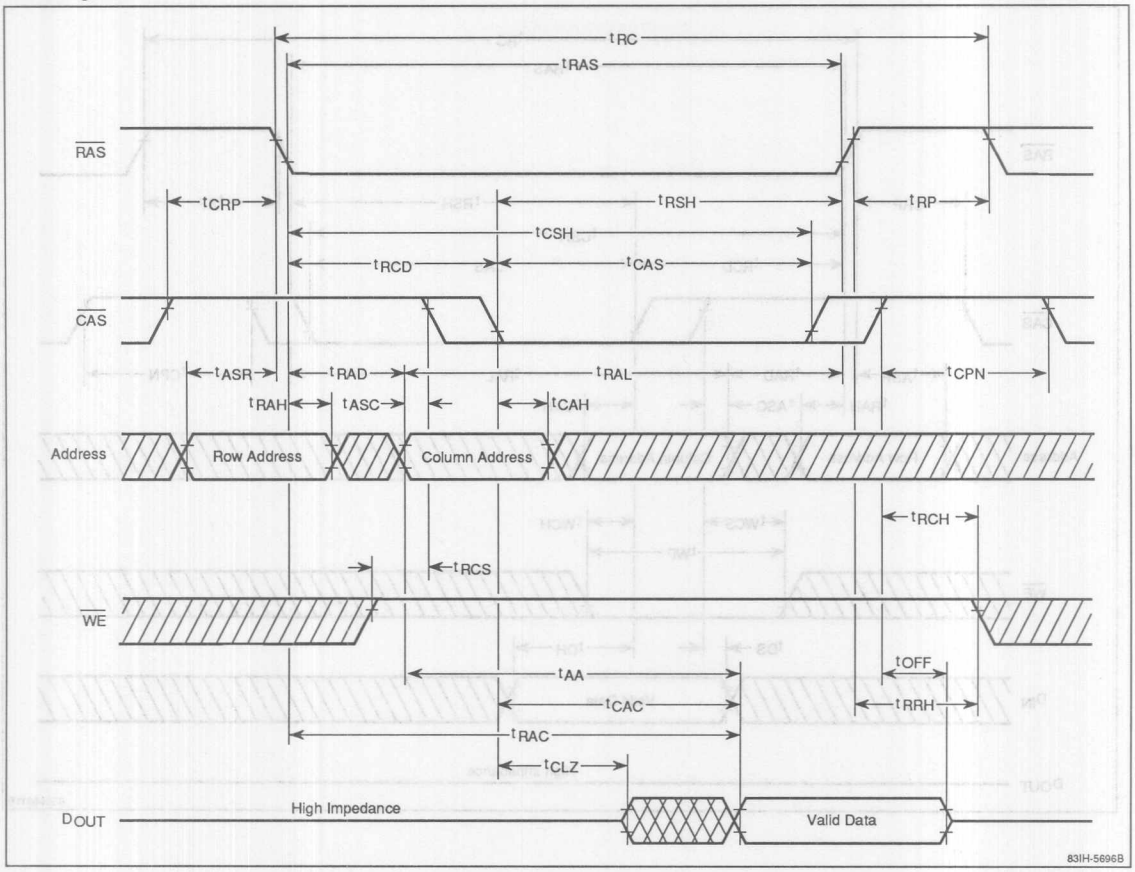
(16) t_{WCS}, t_{RWD}, t_{CWD}, and t_{AWD} are restrictive operating parameters in read-write/read-modify-write cycles only. If $t_{WCS} \geq t_{WCS}$ (min), the cycle is an early write cycle and the data output will remain open-circuit throughout the entire cycle. If $t_{CWD} \geq t_{CWD}$ (min), $t_{RWD} \geq t_{RWD}$ (min), and $t_{AWD} \geq t_{AWD}$ (min), the cycle is a read-write cycle and the data output will contain data read from the selected cell. If neither of the above conditions is met, the condition of the data output pin (at access time and until $\overline{CAS}$ returns to V_{IH}) is indeterminate.

(17) A test mode may be initiated by executing a $\overline{CAS}$ before $\overline{RAS}$ refresh cycle with $\overline{WE}$ held at V_{IL}. This mode also may inadvertently be initiated during power-up because external control of the signal lines is very difficult during this period. It is therefore recommended that while $\overline{WE}$ is held at V_{IH}, either a $\overline{RAS}$-only or $\overline{CAS}$ before $\overline{RAS}$ refresh cycle should be executed at any time after the end of the initial power-up sequence to ensure normal device operation.

(18) Read-write/read-modify-write cycles can be executed only by $\overline{CAS}_9$, D_{IN9} and D_{OUT9} because of the separate data input and output pins. See block diagram.

Timing Waveforms

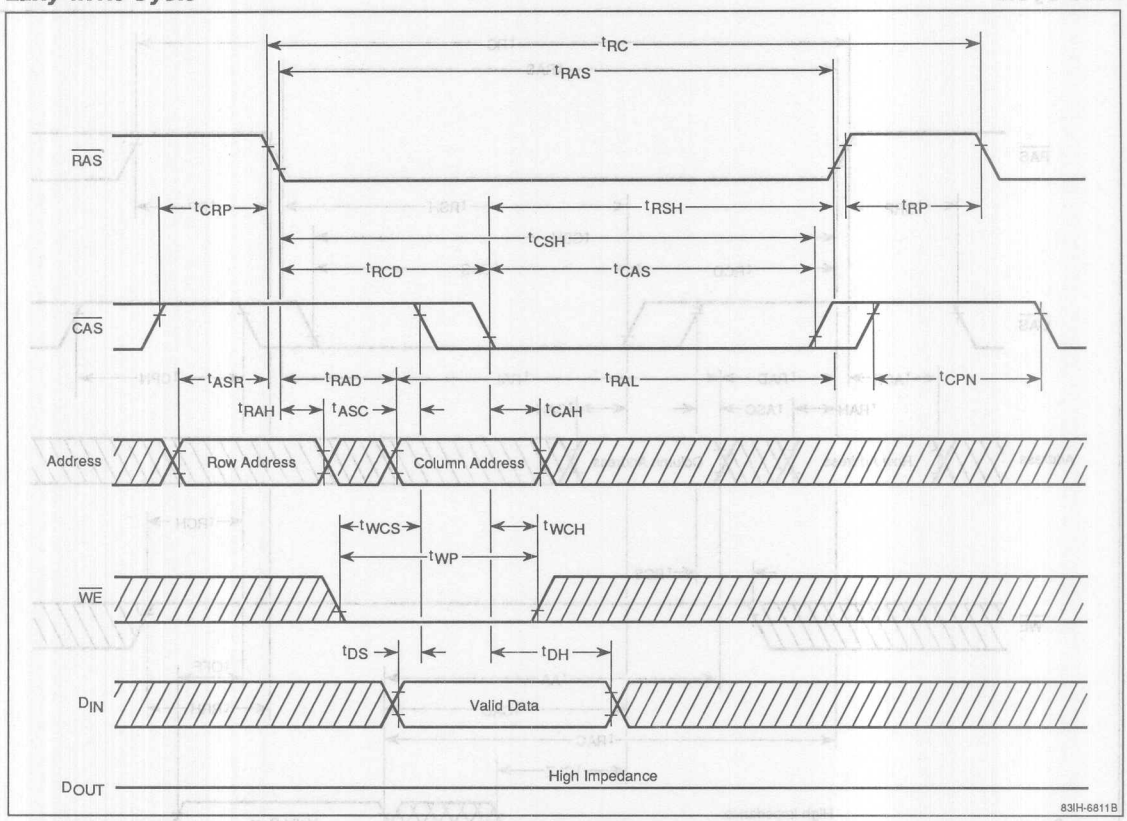
Read Cycle



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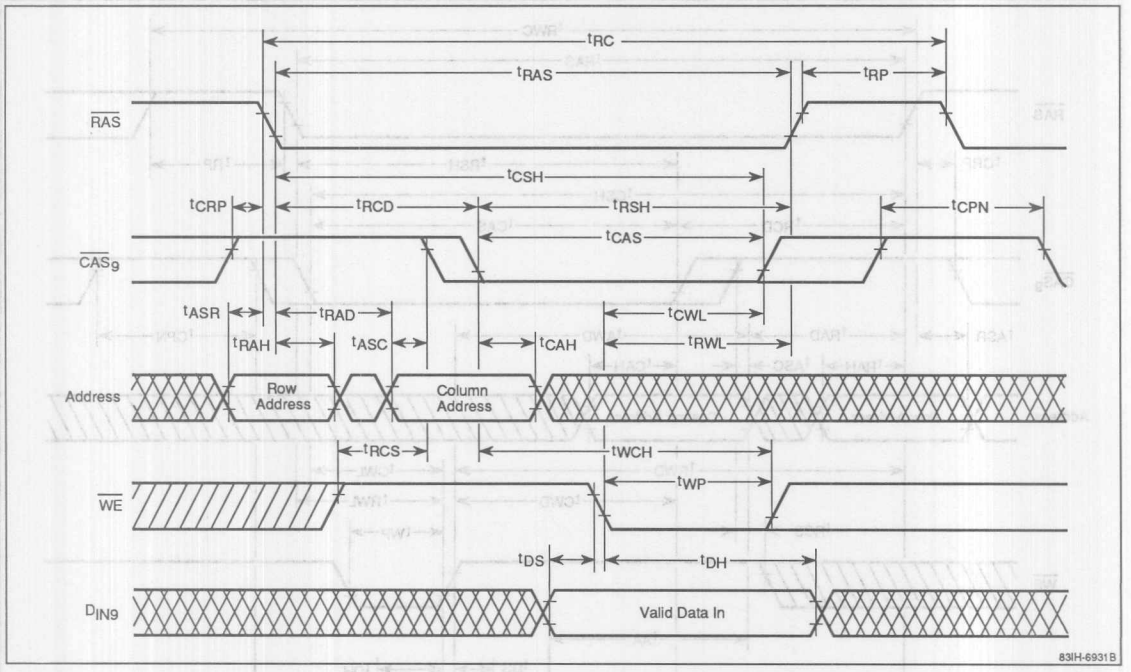
Timing Waveforms (cont)

Early Write Cycle



Timing Waveforms (cont)

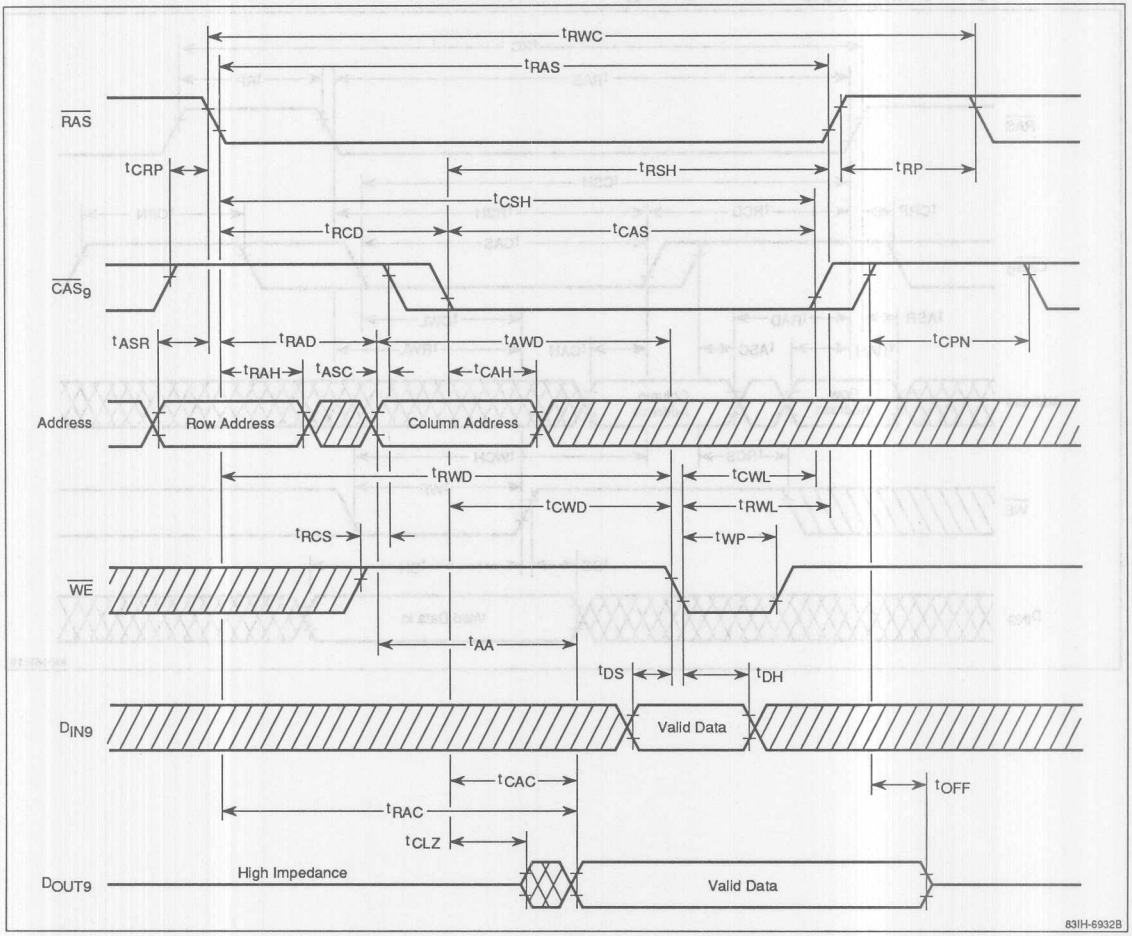
Late Write Cycle (D_{IN9}, D_{OUT9}, and $\overline{CAS_9}$ Only)



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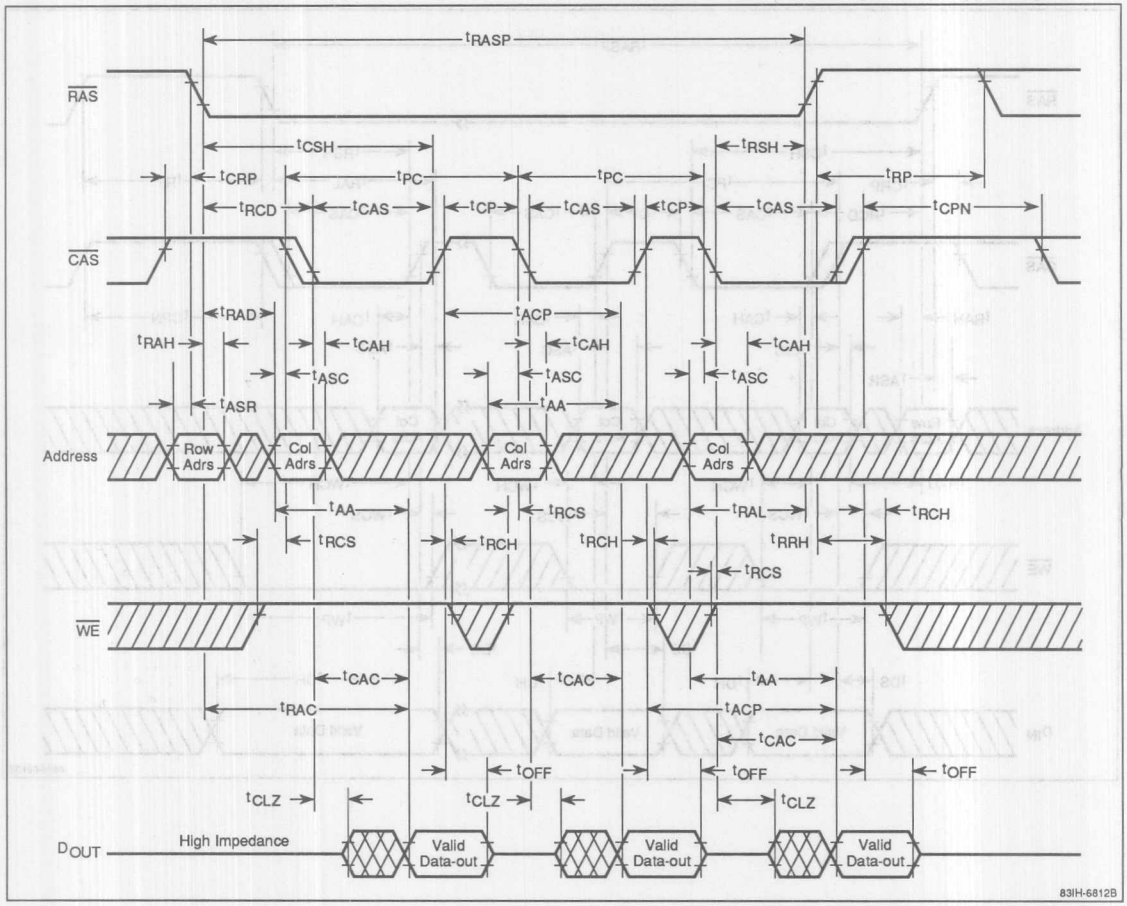
Timing Waveforms (cont)

Read-Write/Read-Modify-Write Cycle (D_{IN9}, D_{OUT9}, and $\overline{CAS_9}$ Only)



Timing Waveforms (cont)

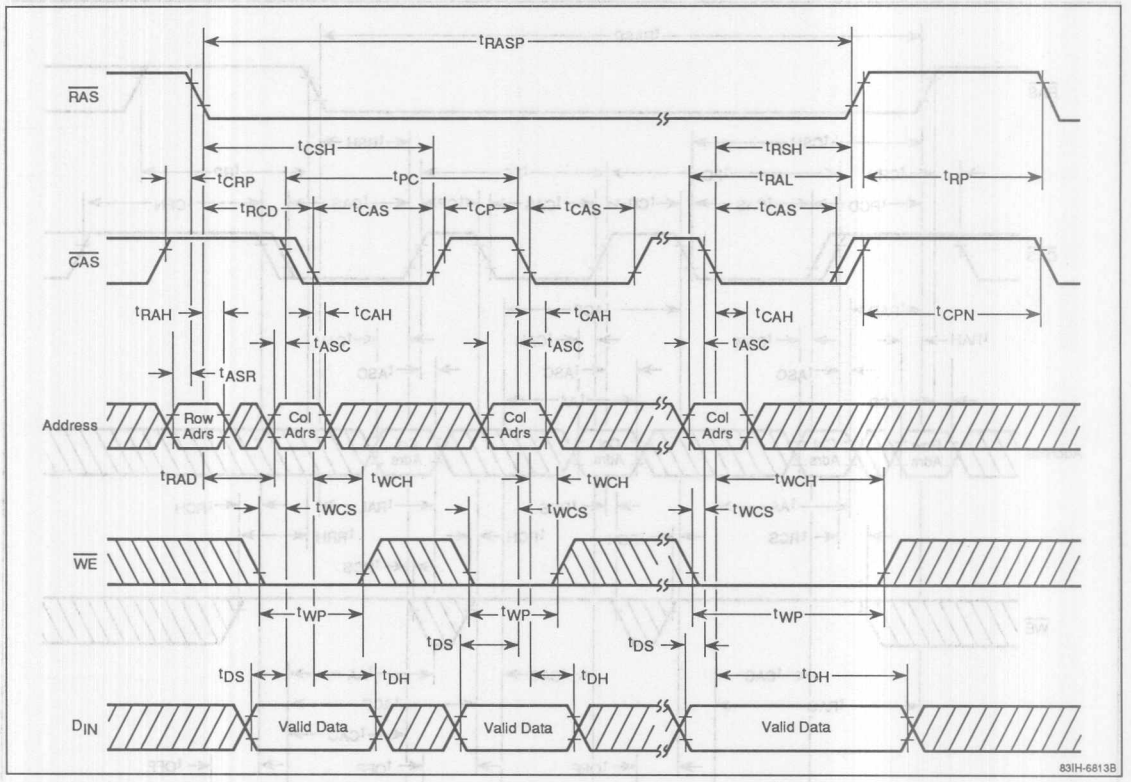
Fast-Page Read Cycle



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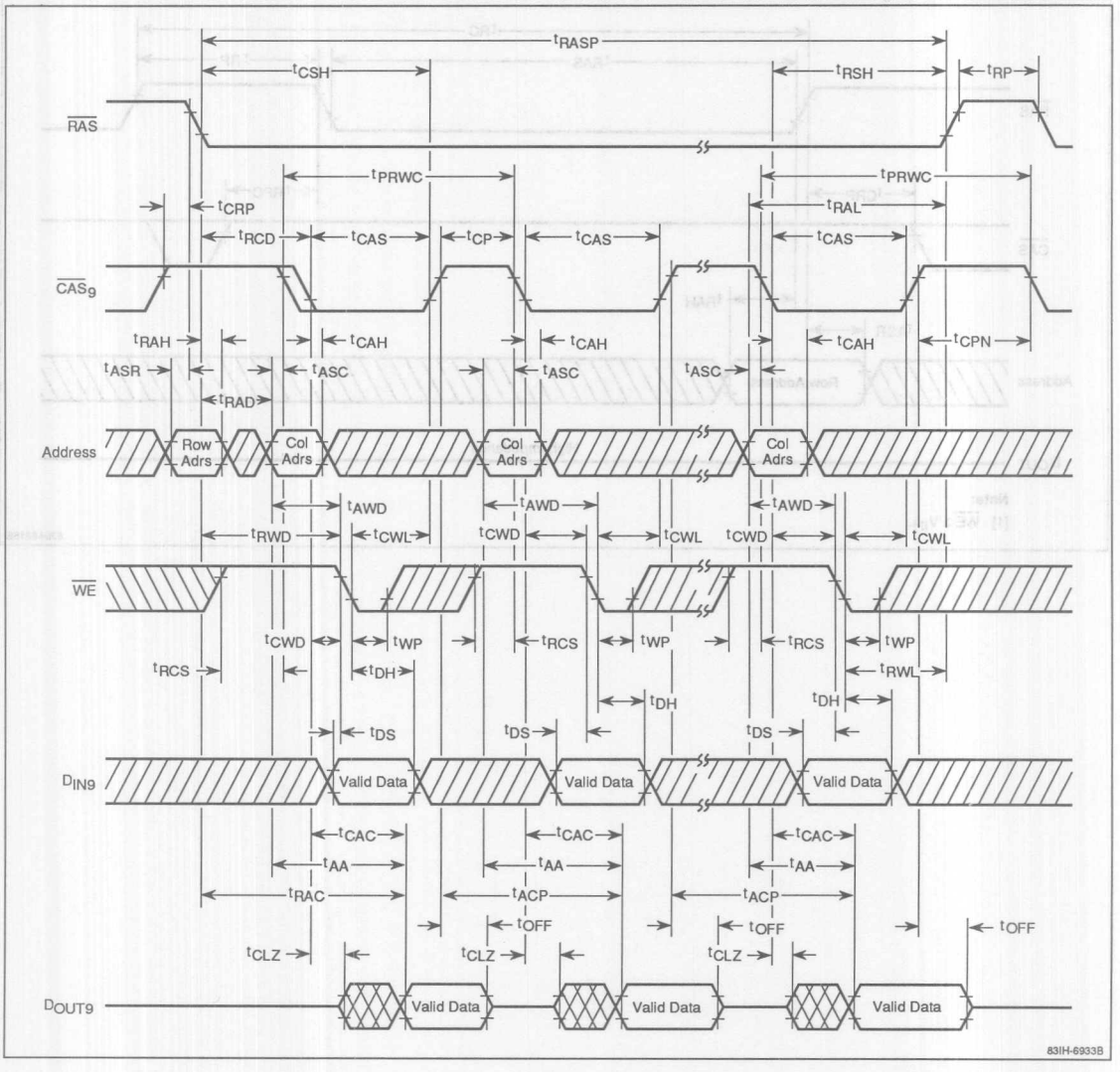
Timing Waveforms (cont)

Fast-Page Early Write Cycle



Timing Waveforms (cont)

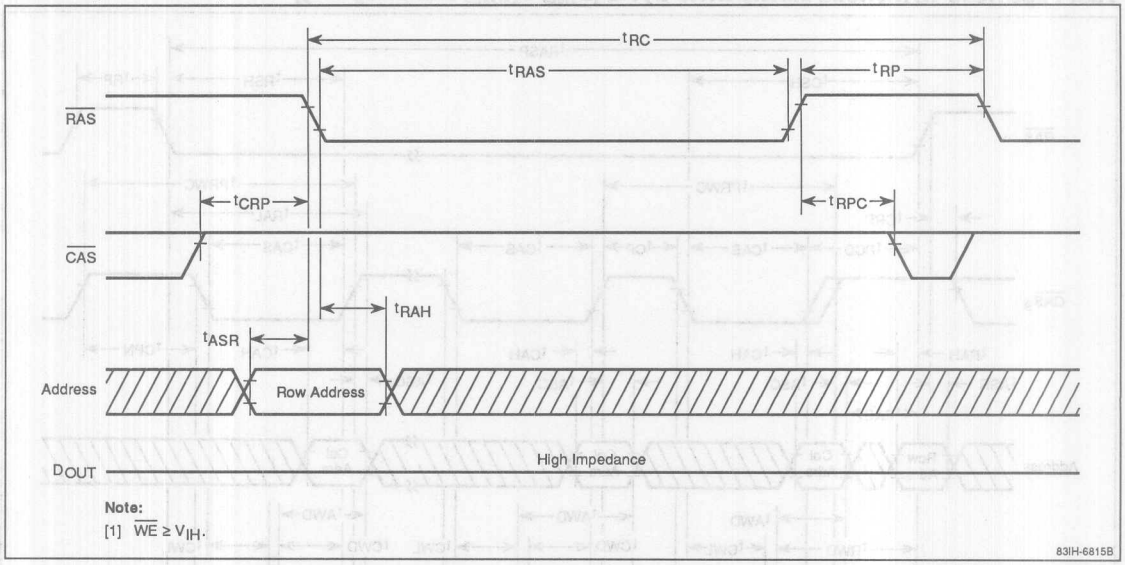
Fast-Page Read-Write/Read-Modify-Write Cycle (D_{IN9}, D_{OUT9}, and $\overline{CAS}_9$ Only)



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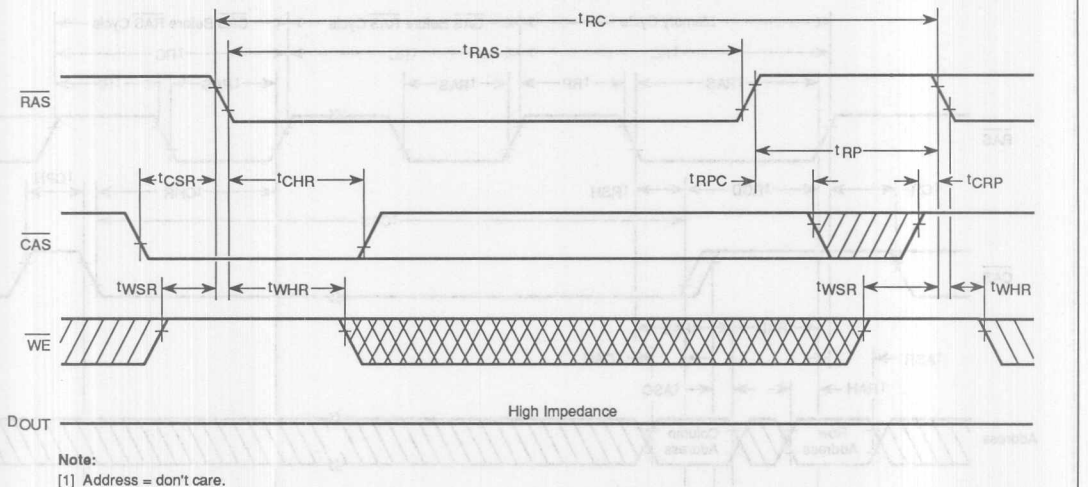
Timing Waveforms (cont)

$\overline{RAS}$-Only Refresh Cycle



Timing Waveforms (cont)

$\overline{CAS}$ Before $\overline{RAS}$ Refresh Cycle



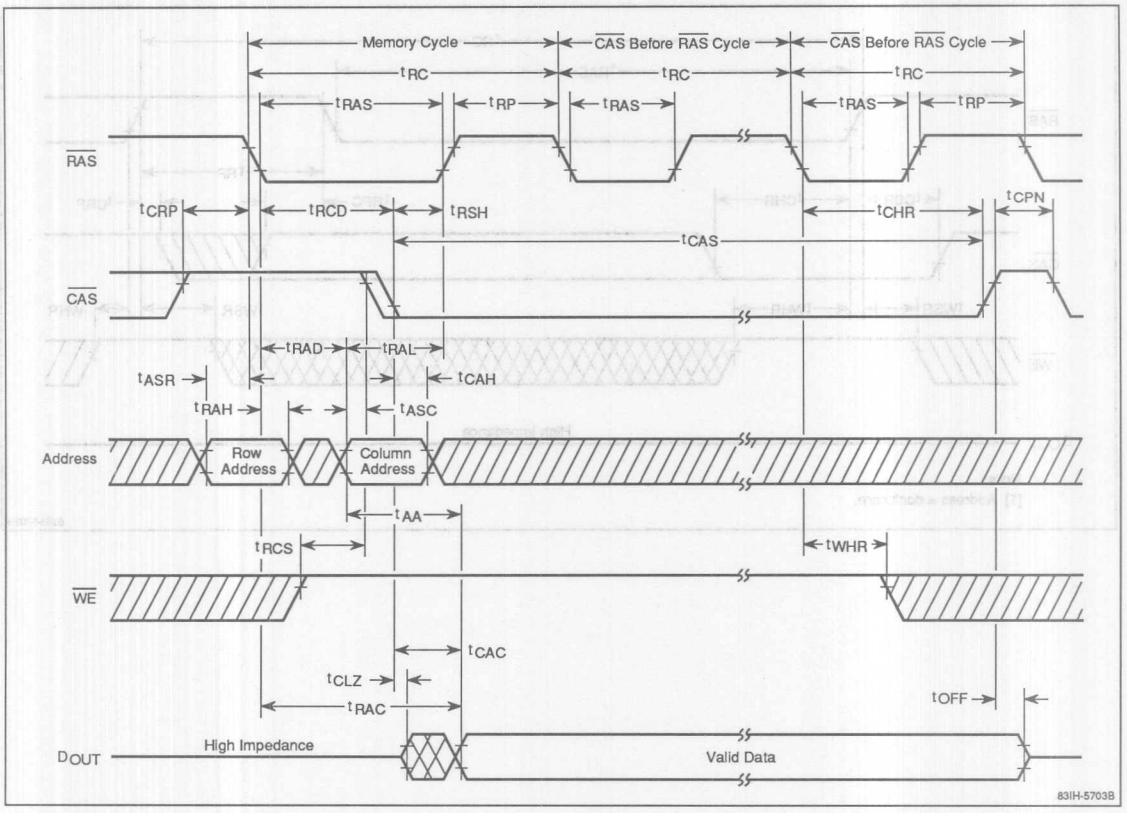
Note:
[1] Address = don't care.

83IH-5702B

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Timing Waveforms (cont)

Hidden Refresh Cycle



MC-424256A36
262,144 x 36-Bit
Dynamic RAM Module

Description

The MC-424256A36 is a page mode dynamic RAM module organized as 262,144 words by 36 bits and designed to operate from a single + 5-volt power supply. Advanced circuitry ensures minimum power dissipation and excellent operating margins.

The three-state output is controlled by $\overline{CAS}$ independent of $\overline{RAS}$. After a valid read or read-modify-write cycle, data is held on the output by holding $\overline{CAS}$ low. Data output is returned to high impedance by returning $\overline{CAS}$ high. Refreshing is accomplished by means of $\overline{RAS}$-only refresh cycles, $\overline{CAS}$ before $\overline{RAS}$ refresh cycles, hidden refresh cycles, or by the 512 address combinations of A_0 through A_8 during an 8-ms period.

Single Inline Memory Module (SIMM™) packaging enhances reliability and reduces the size, weight and cost of a system. Each SIMM contains eight 262,144 x 4-bit μPD424256s in SOJ packages, four 262,144 x 1-bit μPD41256s in PLCC packages, and twelve power supply decoupling capacitors for noise reduction. DQ_0 through DQ_{35} are common input/output pins.

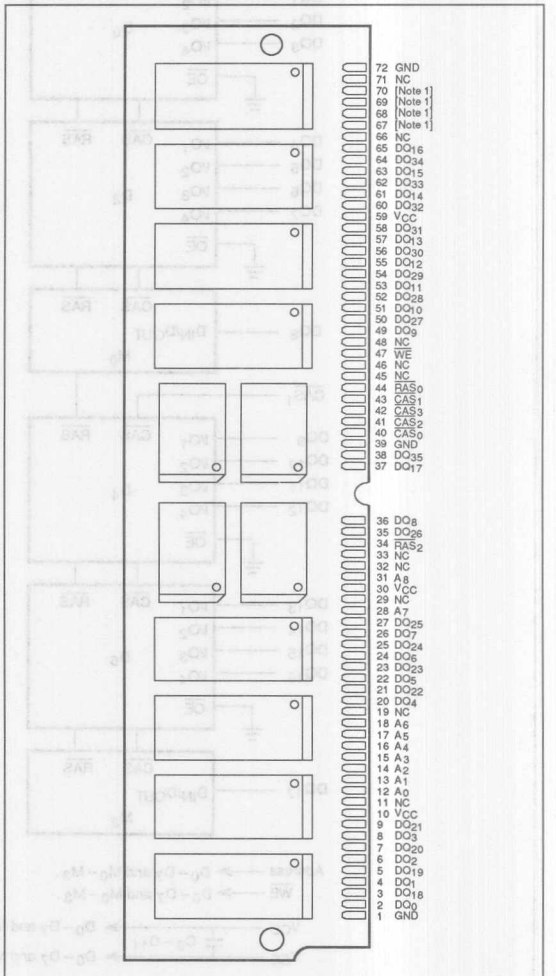
Features

- 262,144-word by 36-bit organization
- Single + 5-volt power supply
- Page mode operation
- Low power dissipation
- $\overline{RAS}$-only refresh cycles
- $\overline{CAS}$ before $\overline{RAS}$ refresh cycles
- Hidden refresh cycles
- 512 refresh cycles every 8 ms
- TTL-compatible inputs and outputs
- 72-pin SIMM packaging

SIMM is a trademark of Wang Laboratories.

Pin Configuration

72-Pin SIMM



Notes:

[1] Pins 67 through 70 are defined by access time:

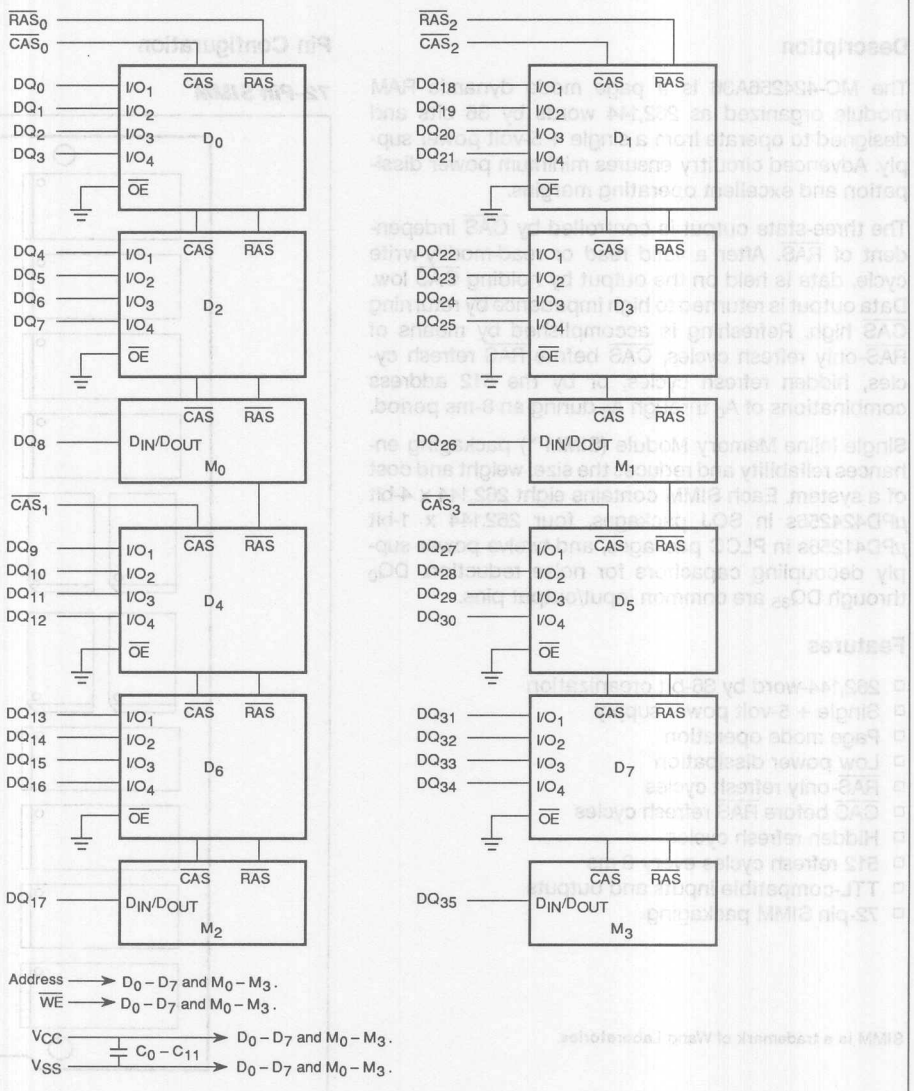
Pins	80 ns	85 ns	100 ns
67	GND	GND	GND
68	NC	NC	NC
69	NC	NC	GND
70	GND	GND	GND

83YL-7320A

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New 70 ns speed and 1-inch height will be available in 1991.

Block Diagram



Notes:

[1] D_0 through D_7 pertain to the μPD424256 and M_0 through M_3 to the μPD41256.

83YL-7249B

Pin Identification

Name	Function
A_0 - A_8	Address inputs
$\overline{CAS}_0$ - $\overline{CAS}_3$	Column address strobe
DQ_0 - DQ_{35}	Common data inputs/outputs
$\overline{RAS}_0$, $\overline{RAS}_2$	Row address strobe
$\overline{WE}$	Write enable
GND	Ground
V_{CC}	+5-volt power supply
NC	No connection

Absolute Maximum Ratings

Voltage on any pin relative to GND	−1.0 to +7.0 V
Operating temperature, T_{OPR}	0 to +70°C
Storage temperature, T_{STG}	−55 to +125°C
Short-circuit output current, I_{OS}	50 mA
Power dissipation, P_D	12 W

Exposure to Absolute Maximum Ratings for extended periods may affect device reliability; exceeding the ratings could cause permanent damage. The device should be operated within the limits specified under DC and AC Characteristics.

Recommended Operating Conditions

Parameter	Symbol	Min	Typ	Max	Unit
Input voltage, high	V_{IH}	2.4		V_{CC} + 1.0	V
Input voltage, low	V_{IL}	−1.0		0.8	V
Supply voltage	V_{CC}	4.75	5.0	5.25	V
Ambient temperature	T_A	0		70	°C

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Capacitance

T_A = 25°C; f = 1 MHz

Parameter	Symbol	Max	Unit	Pins Under Test
Input capacitance	C_{I1}	88	pF	A_0 - A_8
	C_{I2}	104	pF	$\overline{WE}$
	C_{I3}	57	pF	$\overline{RAS}$
	C_{I4}	36	pF	$\overline{CAS}$
Input/output capacitance	C_{I1}/C_{O1}	17	pF	DQ_0 - DQ_7, DQ_9 - DQ_{16}, DQ_{18} - DQ_{25}, DQ_{27} - DQ_{34}
	C_{I2}/C_{O2}	22	pF	DQ_8, DQ_{17}, DQ_{26}, DQ_{35}

Ordering Information

Part Number	Row Access Time (max)	R/W Cycle Time (min)	Fast-Page Cycle (min)	Package
MC424256A36B-80	80 ns	160 ns	70 ns	72-pin socket-mountable SIMM (solder plating)
B-85	85 ns	165 ns	70 ns	
B-10	100 ns	200 ns	100 ns	
MC424256A36F-80	80 ns	160 ns	70 ns	72-pin socket-mountable SIMM (gold plating)
F-85	85 ns	165 ns	70 ns	
F-10	100 ns	200 ns	100 ns	

DC Characteristics

T_A = 0 to +70°C; V_{CC} = +5.0 V ±5%

Parameter	Symbol	Min	Max	Unit	Test Conditions
Standby current	I_{CC2}		36	mA	$\overline{RAS}$ = $\overline{CAS}$ ≥ V_{IH} (min)
			8	mA	$\overline{RAS}$ = $\overline{CAS}$ ≥ V_{CC} – 0.2 V
Input leakage current	$I_{I(L)}$	–120	120	μA	V_{IN} = 0 V to V_{CC}; all other pins not under test = 0 V
Output leakage current	$I_{O(L)}$	–10	10	μA	DQ_0 to DQ_{35} disabled; V_{OUT} = 0 V to V_{CC}
Output voltage, low	V_{OL}		0.4	V	I_{OL} = 4.2 mA
Output voltage, high	V_{OH}	2.4		V	I_{OH} = –5 mA

AC Characteristics

T_A = 0 to +70°C; V_{CC} = +5.0 V ±5%

		-80		-85		-10			
Parameter	Symbol	Min	Max	Min	Max	Min	Max	Unit	Test Conditions
Operating current, average	I_{CC1}		960		808		680	mA	$\overline{RAS}$ and $\overline{CAS}$ cycling; t_{RC} = t_{RC} min; I_O = 0 mA (Note 5)
Operating current, $\overline{RAS}$-only refresh cycle, average	I_{CC3}		960		808		680	mA	$\overline{RAS}$ cycling; $\overline{CAS}$ ≥ V_{IH}; t_{RC} = t_{RC} min; I_O = 0 mA (Note 5)
Operating current, page mode cycle, average	I_{CC4}		916		764		660	mA	$\overline{RAS}$ ≤ V_{IL}; $\overline{CAS}$ cycling; t_{PC} = t_{PC} min; I_O = 0 mA (Note 5)
Operating current, $\overline{CAS}$ before $\overline{RAS}$ refresh cycle, average	I_{CC5}		960		808		680	mA	$\overline{RAS}$ cycling; $\overline{CAS}$ before $\overline{RAS}$; t_{RC} = t_{RC} min; I_O = 0 mA (Note 5)
Column address hold time referenced to $\overline{RAS}$	t_{AR}	55		55		65		ns	
Column address setup time	t_{ASC}	0		0		0		ns	
Row address setup time	t_{ASR}	0		0		0		ns	
Access time from $\overline{CAS}$ (falling edge)	t_{CAC}		40		40		50	ns	(Notes 7, 9)
Column address hold time	t_{CAH}	20		20		20		ns	
$\overline{CAS}$ pulse width	t_{CAS}	40	10,000	40	10,000	50	10,000	ns	
$\overline{CAS}$ hold time for $\overline{CAS}$ before $\overline{RAS}$ refresh cycle	t_{CHR}	15		15		20		ns	

AC Characteristics (cont)

Parameter	Symbol	-80 Min	-80 Max	-85 Min	-85 Max	-10 Min	-10 Max	Unit	Test Conditions
$\overline{CAS}$ precharge time, page mode cycle	t_{CP}	20		20		40		ns	
$\overline{CAS}$ precharge time, nonpage cycle	t_{CPN}	25		25		25		ns	
$\overline{CAS}$ to $\overline{RAS}$ precharge time	t_{CRP}	10		10		10		ns	(Note 12)
$\overline{CAS}$ hold time	t_{CSH}	80		85		100		ns	
$\overline{CAS}$ setup time for $\overline{CAS}$ before $\overline{RAS}$ refresh cycle	t_{CSR}	10		10		10		ns	
Data-in hold time	t_{DH}	20		20		25		ns	(Note 15)
Data-in hold time referenced to $\overline{RAS}$	t_{DHR}	60		65		75		ns	
Data-in setup time	t_{DS}	0		0		0		ns	(Note 15)
Output buffer turnoff delay	t_{OFF}	0	20	0	20	0	25	ns	(Note 10)
Page cycle time	t_{PC}	70		70		100		ns	(Note 6)
Access time from $\overline{RAS}$	t_{RAC}		80		85		100	ns	(Notes 7, 8)
Row address hold time	t_{RAH}	12		12		12		ns	
$\overline{RAS}$ pulse width	t_{RAS}	80	10,000	85	10,000	100	10,000	ns	
Random read or write cycle time	t_{RC}	160		165		200		ns	(Note 6)
$\overline{RAS}$ to $\overline{CAS}$ delay time	t_{RCD}	20	40	25	45	25	50	ns	(Note 11)
Read command hold time referenced to $\overline{CAS}$	t_{RCH}	0		0		0		ns	(Note 13)
Read command setup time	t_{RCS}	0		0		0		ns	
Refresh period	t_{REF}		8		8		8	ms	Addresses A_0 - A_8
$\overline{RAS}$ precharge time	t_{RP}	70		70		90		ns	
$\overline{RAS}$ precharge $\overline{CAS}$ hold time	t_{RPC}	0		0		0		ns	
Read command hold time referenced to $\overline{RAS}$	t_{RRH}	10		10		10		ns	(Note 13)
$\overline{RAS}$ hold time	t_{RSH}	40		40		50		ns	
Rise and fall transition time	t_T	3	50	3	50	3	50	ns	(Note 3)

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AC Characteristics (cont)

Parameter	Symbol	-80 Min	-80 Max	-85 Min	-85 Max	-10 Min	-10 Max	Unit	Test Conditions
Write command hold time	t_{WCH}	20		20		25		ns	
Write command hold time referenced to $\overline{RAS}$	t_{WCR}	60		65		75		ns	
Write command setup time	t_{WCS}	0		0		0		ns	(Note 16)
Write command pulse width	t_{WP}	15		15		15		ns	(Note 14)

Notes:

(1) All voltages are referenced to GND.

(2) An initial pause of 100 μs is required after power-up, followed by any eight $\overline{RAS}$ cycles, before proper device operation is achieved.

(3) AC measurements assume $t_T = 5$ ns.

(4) V_{IH} (min) and V_{IL} (max) are reference levels for measuring the timing of input signals. Transition times are measured between V_{IH} and V_{IL}.

(5) I_{CC1}, I_{CC3}, I_{CC4}, and I_{CC5} depend on output loading and cycle rates. Specified values are obtained with the output open. I_{CC3} is measured assuming that all column address inputs are held at either a high level or a low level during $\overline{RAS}$-only refresh cycles. I_{CC4} is measured assuming that all column address inputs are switched only once during each fast-page cycle.

(6) The minimum specifications are used only to indicate the cycle time at which proper operation over the full temperature range (T_A = 0 to +70°C) is assured.

(7) Load = 2 TTL (–1 mA, +4 mA) loads and 100 pF (V_{OH} = 2.0 V, V_{OL} = 0.8 V).

(8) Assumes that $t_{RCD} \leq t_{RCD}$ (max) and $t_{RAD} \leq t_{RAD}$ (max). If t_{RCD} or t_{RAD} is greater than the maximum recommended value in this table, t_{RAC} increases by the amount that t_{RCD} or t_{RAD} exceeds the value shown.

(9) If $t_{RAD} \geq t_{RAD}$ (max), then the access time is defined by t_{AA}.

(10) t_{OFF} (max) defines the time at which the output achieves the open-circuit condition an is not referenced to V_{OH} or V_{OL}.

(11) Operation within the t_{RCD} (max) limit assures that t_{RAC} (max) can be met. t_{RCD} (max) is specified as a reference point only; if t_{RCD} is greater than t_{RCD} (max), then access time is controlled exclusively by t_{CAC}.

(12) The t_{CRP} requirement should be applicable for $\overline{RAS}$/$\overline{CAS}$ cycles preceded by any cycle.

(13) Either t_{RRH} or t_{RCH} must be satisfied for a read cycle.

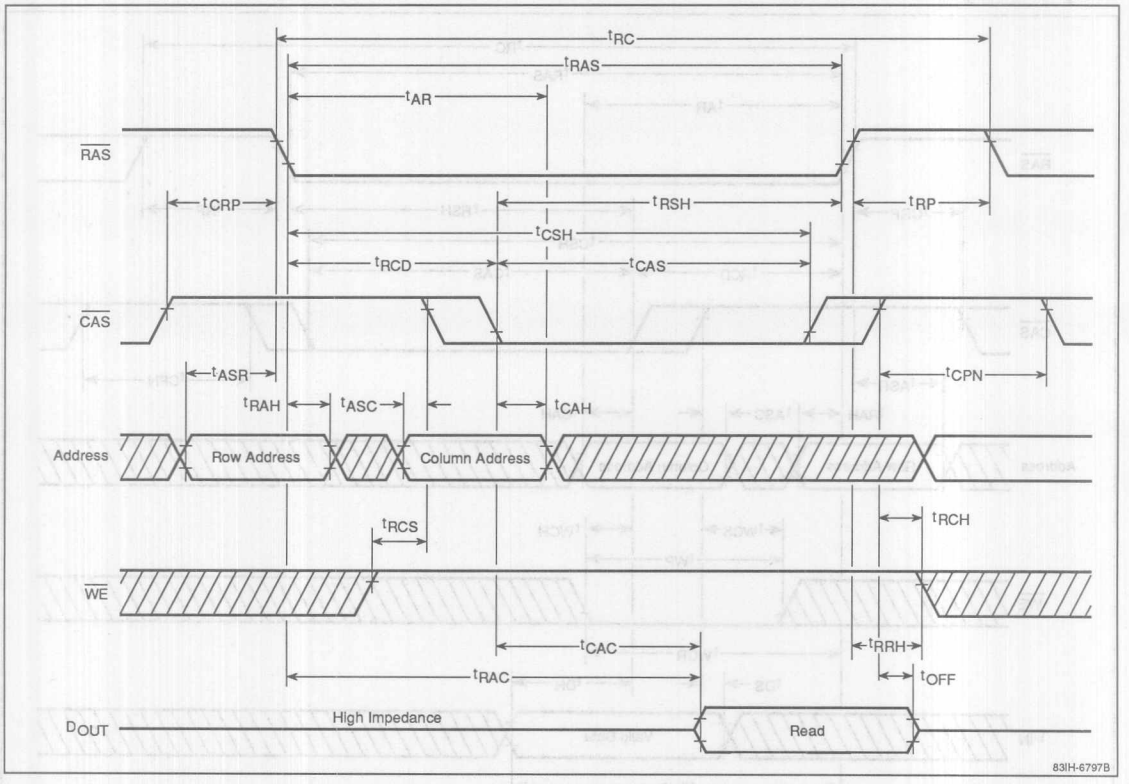
(14) Parameter t_{WP} is applicable for a delayed write cycle such as a read-write/read-modify-write cycle. For early write operation, both t_{WCS} and t_{WCH} must be met.

(15) These parameters are referenced to the falling edge of $\overline{CAS}$ for early write cycles and to the falling edge of $\overline{WE}$ for delayed write or read-modify-write cycles.

(16) t_{WCS}, t_{RWD}, t_{CWD}, and t_{AWD} are restrictive operating parameters in read-write/read-modify-write cycles only. If $t_{WCS} \geq t_{WCS}$ (min), the cycle is an early write cycle and the data output will remain open-circuit throughout the entire cycle. If $t_{CWD} \geq t_{CWD}$ (min), $t_{RWD} \geq t_{RWD}$ (min), and $t_{AWD} \geq t_{AWD}$ (min), the cycle is a read-write cycle and the data output will contain data read from the selected cell. If neither of the above conditions is met, the condition of the data output pin (at access time and until $\overline{CAS}$ returns to V_{IH}) is indeterminate.

Timing Waveforms

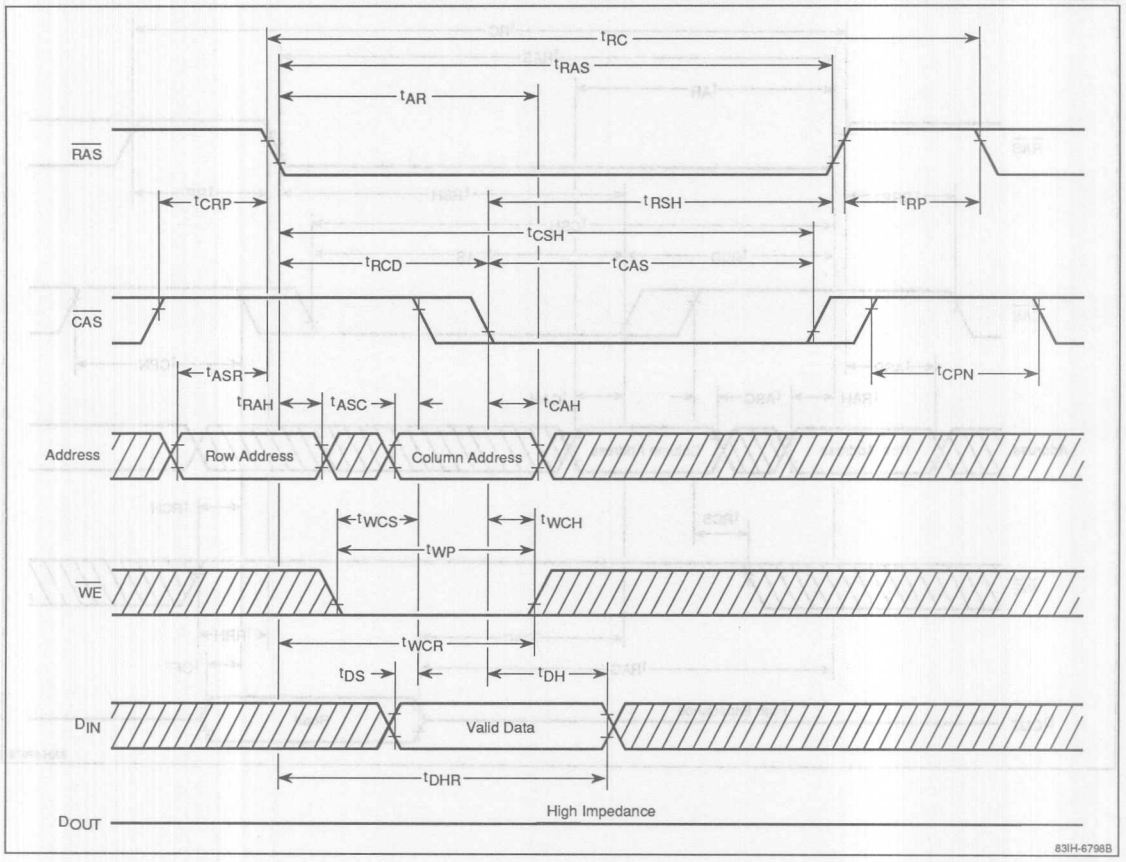
Read Cycle



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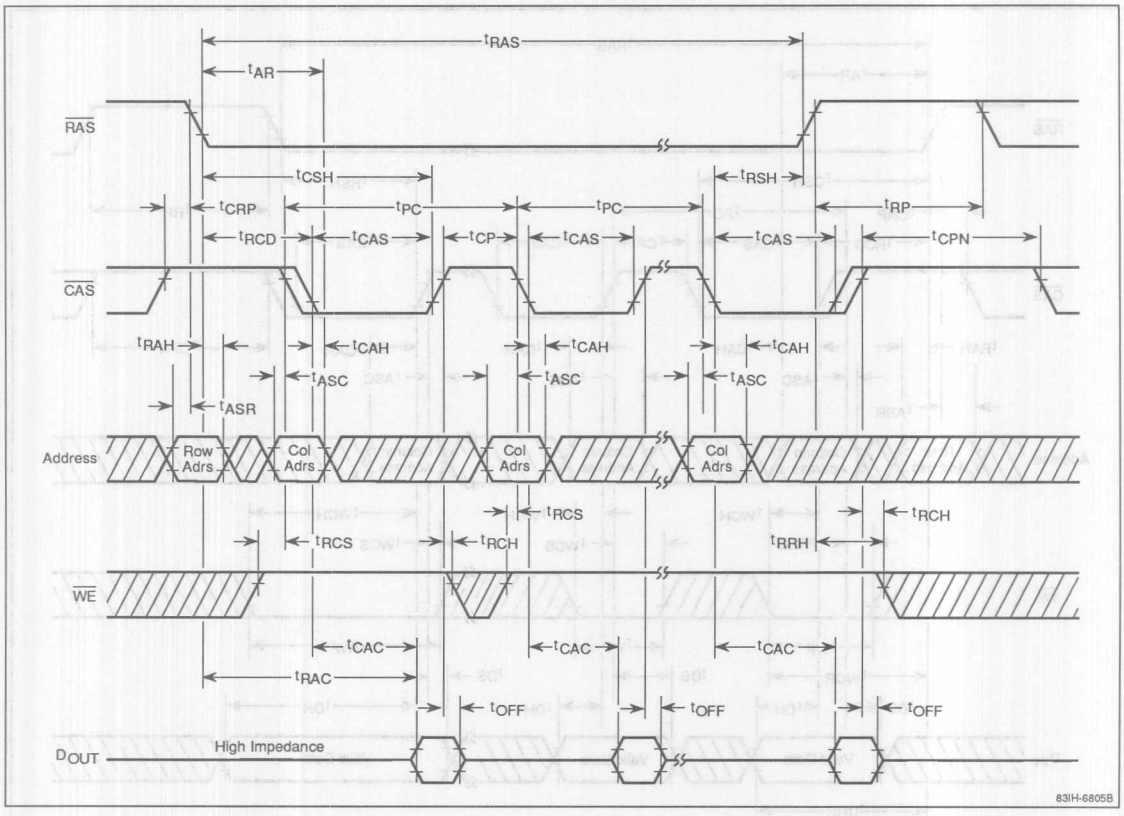
Timing Waveforms (cont)

Early Write Cycle



Timing Waveforms (cont)

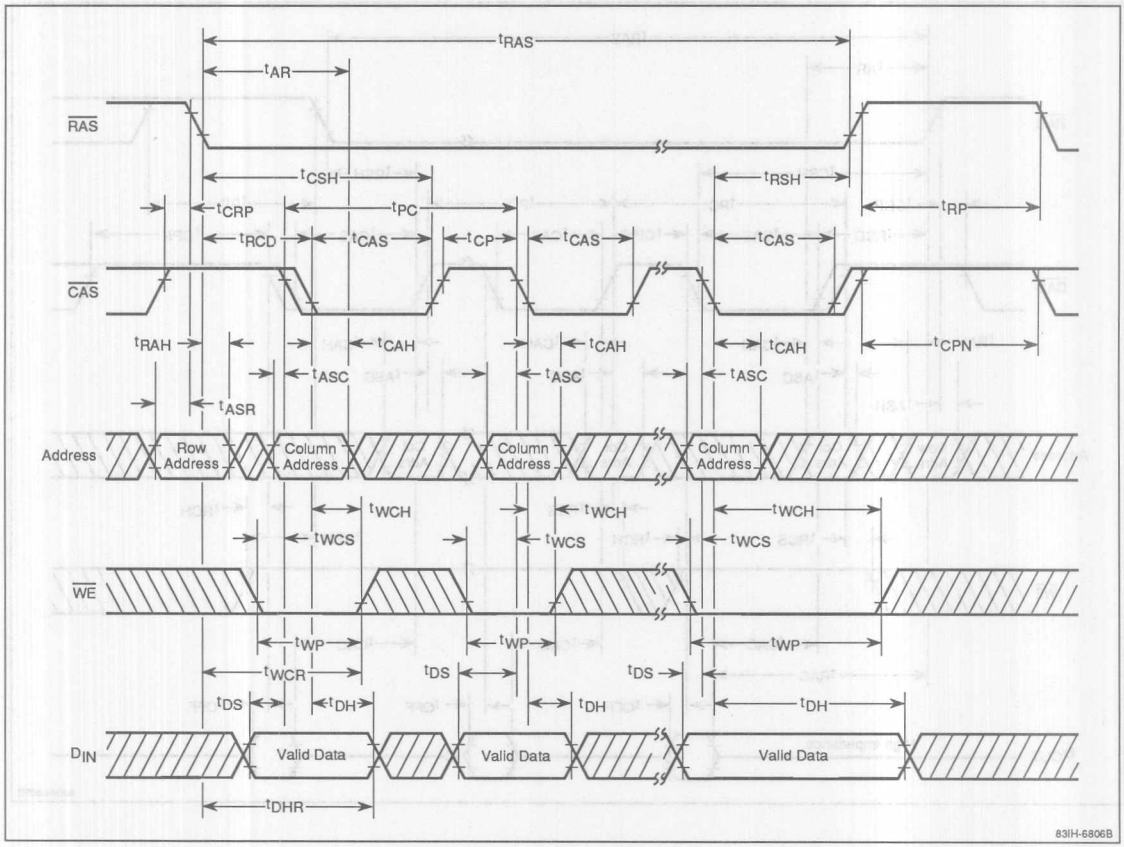
Page Mode Read Cycle



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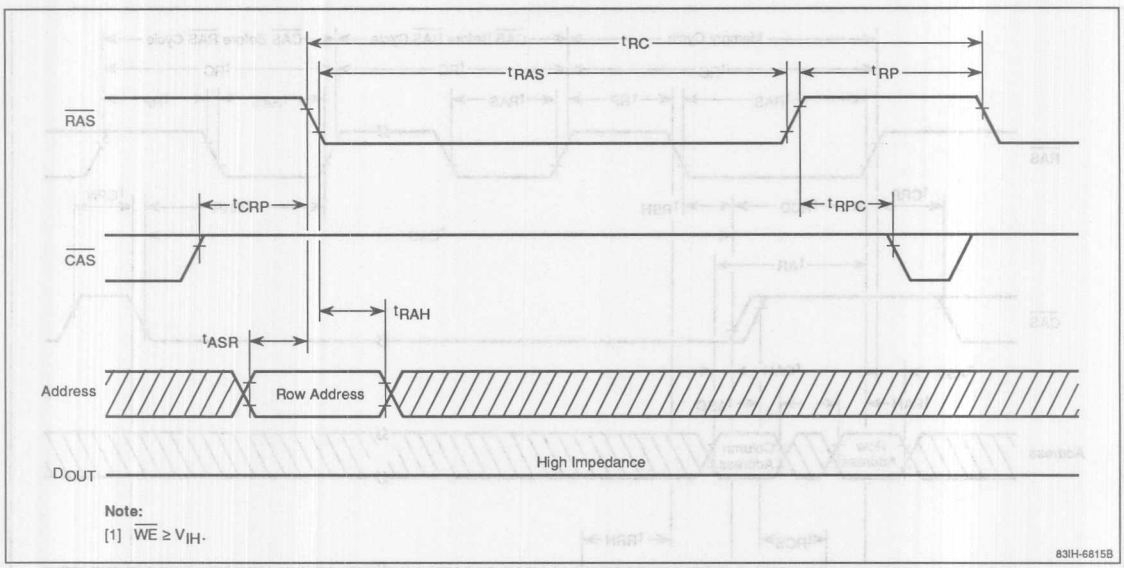
Timing Waveforms (cont)

Page Early Write Cycle



Timing Waveforms (cont)

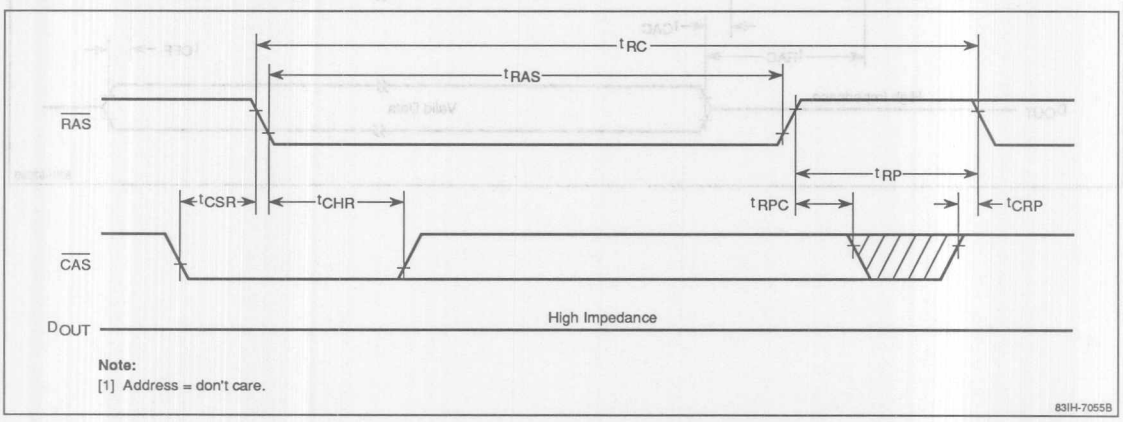
$\overline{RAS}$-Only Refresh Cycle



Note:
[1] $\overline{WE} \geq V_{IH}$.

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$\overline{CAS}$ Before $\overline{RAS}$ Refresh Cycle



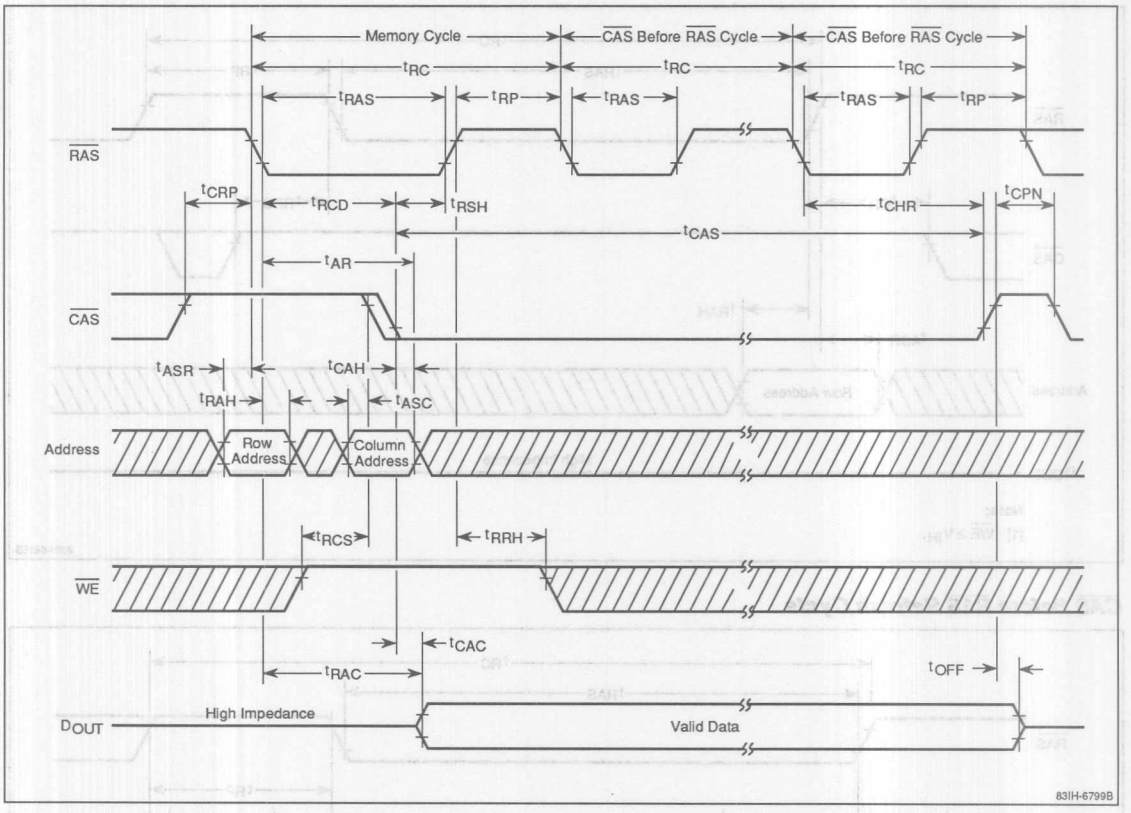
Note:
[1] Address = don't care.

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Timing Waveforms (cont)

Hidden Refresh Cycle



NEC Electronics Inc.

MC-424256A36BH/FH
262,144 x 36-Bit
Dynamic CMOS RAM Module

Description

The MC-424256A36BH/FH is a fast-page dynamic RAM module organized as 262,144 words by 36 bits and designed to operate from a single + 5-volt power supply. Advanced CMOS circuitry ensures minimum power dissipation and excellent operating margins.

The three-state output is controlled by $\overline{CAS}$ independent of $\overline{RAS}$. After a valid read or read-modify-write cycle, data is held on the output by holding $\overline{CAS}$ low. Data output is returned to high impedance by returning $\overline{CAS}$ high. Fast-page read and write cycles can be executed by cycling $\overline{CAS}$. Refreshing is accomplished by means of $\overline{RAS}$-only refresh cycles, $\overline{CAS}$ before $\overline{RAS}$ refresh cycles, hidden refresh cycles, or by the 1024 address combinations of A_0 through A_8 during a 16-ms period.

Single Inline Memory Module (SIMM™) packaging enhances reliability and reduces the size, weight and cost of a system. Each SIMM contains eight 262,144 x 4-bit μPD424256s in SOJ packages, four 1,048,576 x 1-bit μPD421000s in SOJ packages, and twelve power supply decoupling capacitors for noise reduction. DQ_0 through DQ_{35} are common input/output pins.

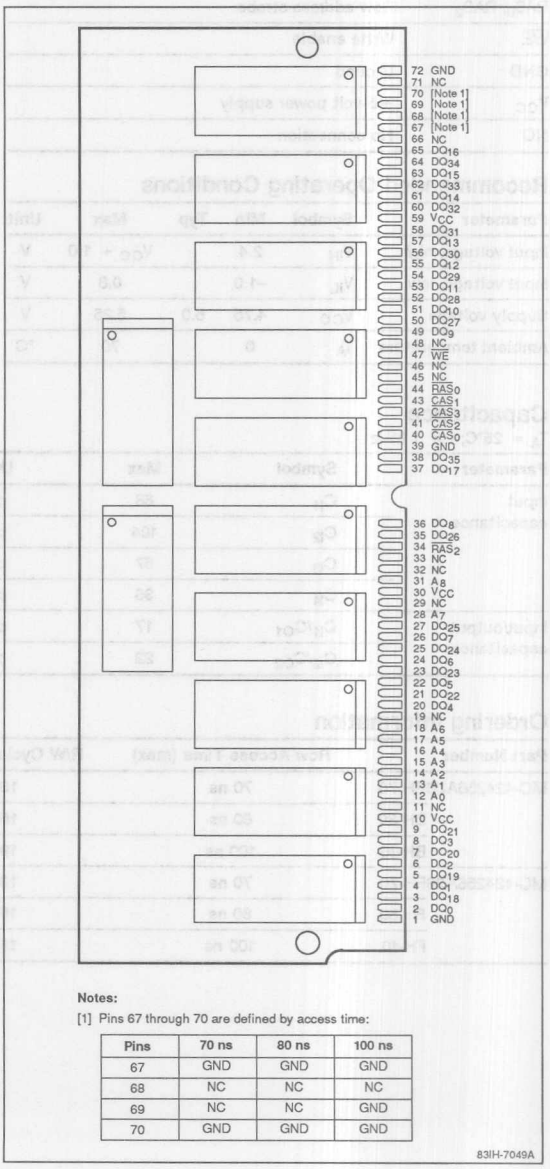
SIMM is a trademark of Wang Laboratories.

Features

- 262,144-word by 36-bit organization
- Single + 5-volt power supply
- Fast-page cycles
- Low power dissipation (126 mW max in standby)
- $\overline{RAS}$-only refresh cycles
- $\overline{CAS}$ before $\overline{RAS}$ refresh cycles
- Hidden refresh cycles
- 1024 refresh cycles every 16 ms
- TTL-compatible inputs and outputs
- 72-pin SIMM packaging

Pin Configuration

72-Pin SIMM



Notes:

[1] Pins 67 through 70 are defined by access time:

Pins	70 ns	80 ns	100 ns
67	GND	GND	GND
68	NC	NC	NC
69	NC	NC	GND
70	GND	GND	GND

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Pin Identification

Name	Function
A_0 - A_8	Address inputs
$\overline{CAS}_0$ - $\overline{CAS}_3$	Column address strobe
DQ_0 - DQ_{35}	Common data inputs/outputs
$\overline{RAS}_0$, $\overline{RAS}_2$	Row address strobe
$\overline{WE}$	Write enable
GND	Ground
V_{CC}	+5-volt power supply
NC	No connection

Absolute Maximum Ratings

Voltage on any pin relative to GND	−1.0 to +7.0 V
Operating temperature, T_{OPR}	0 to +70°C
Storage temperature, T_{STG}	−55 to +125°C
Short-circuit output current, I_{OS}	50 mA
Power dissipation, P_D	12 W

Exposure to Absolute Maximum Ratings for extended periods may affect device reliability; exceeding the ratings could cause permanent damage. The device should be operated within the limits specified under DC and AC Characteristics.

Recommended Operating Conditions

Parameter	Symbol	Min	Typ	Max	Unit
Input voltage, high	V_{IH}	2.4		V_{CC} + 1.0	V
Input voltage, low	V_{IL}	−1.0		0.8	V
Supply voltage	V_{CC}	4.75	5.0	5.25	V
Ambient temperature	T_A	0		70	°C

Capacitance

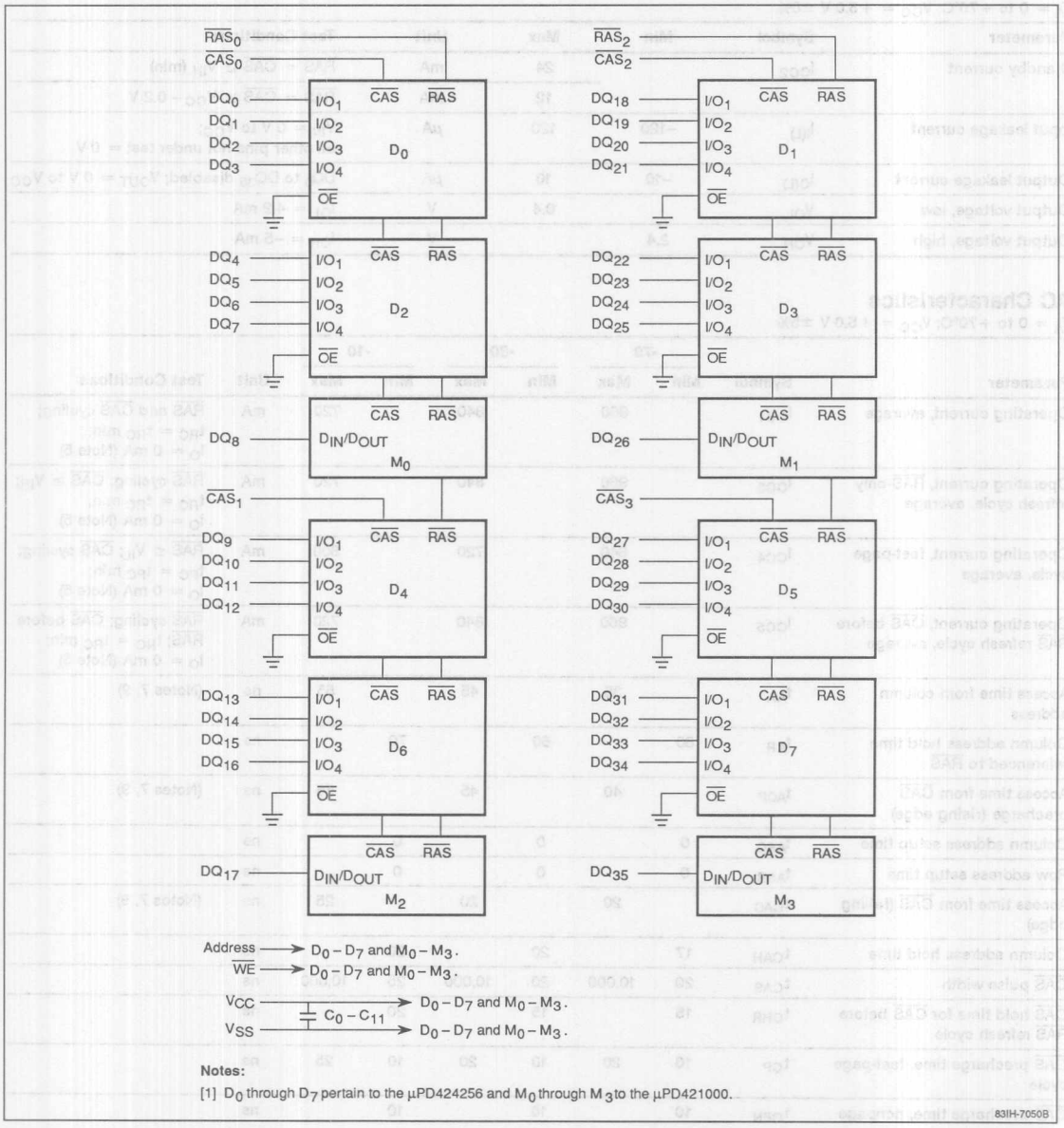
T_A = 25°C; f = 1 MHz

Parameter	Symbol	Max	Unit	Pins Under Test
Input capacitance	C_{I1}	88	pF	A_0 - A_8
	C_{I2}	104	pF	$\overline{WE}$
	C_{I3}	57	pF	$\overline{RAS}$
	C_{I4}	36	pF	$\overline{CAS}$
Input/output capacitance	C_{I1}/C_{O1}	17	pF	DQ_0 - DQ_7, DQ_9 - DQ_{16}, DQ_{18} - DQ_{25}, DQ_{27} - DQ_{34}
	C_{I2}/C_{O2}	22	pF	DQ_8, DQ_{17}, DQ_{26}, DQ_{35}

Ordering Information

Part Number	Row Access Time (max)	R/W Cycle Time (min)	Fast-Page Cycle (min)	Package
MC-424256A36BH-70	70 ns	130 ns	45 ns	72-pin socket-mountable (solder plating)
BH-80	80 ns	160 ns	50 ns	
BH-10	100 ns	190 ns	60 ns	
MC-424256A36FH-70	70 ns	130 ns	45 ns	72-pin socket-mountable (gold plating)
FH-80	80 ns	160 ns	50 ns	
FH-10	100 ns	190 ns	60 ns	

Block Diagram



Notes:

[1] D_0 through D_7 pertain to the μPD424256 and M_0 through M_3 to the μPD421000.

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DC Characteristics

T_A = 0 to +70°C; V_{CC} = +5.0 V ±5%

Parameter	Symbol	Min	Max	Unit	Test Conditions
Standby current	I_{CC2}		24	mA	$\overline{RAS}$ = $\overline{CAS}$ ≥ V_{IH} (min)
			12	mA	$\overline{RAS}$ = $\overline{CAS}$ ≥ V_{CC} – 0.2 V
Input leakage current	$I_{I(L)}$	–120	120	μA	V_{IN} = 0 V to V_{CC}; all other pins not under test = 0 V
Output leakage current	$I_{O(L)}$	–10	10	μA	DQ_0 to DQ_{35} disabled; V_{OUT} = 0 V to V_{CC}
Output voltage, low	V_{OL}		0.4	V	I_{OL} = 4.2 mA
Output voltage, high	V_{OH}	2.4		V	I_{OH} = –5 mA

AC Characteristics

T_A = 0 to +70°C; V_{CC} = +5.0 V ±5%

		-70		-80		-10			
Parameter	Symbol	Min	Max	Min	Max	Min	Max	Unit	Test Conditions
Operating current, average	I_{CC1}		960		840		720	mA	$\overline{RAS}$ and $\overline{CAS}$ cycling; t_{RC} = t_{RC} min; I_O = 0 mA (Note 5)
Operating current, $\overline{RAS}$-only refresh cycle, average	I_{CC3}		960		840		720	mA	$\overline{RAS}$ cycling; $\overline{CAS}$ ≥ V_{IH}; t_{RC} = t_{RC} min; I_O = 0 mA (Note 5)
Operating current, fast-page cycle, average	I_{CC4}		840		720		600	mA	$\overline{RAS}$ ≤ V_{IL}; $\overline{CAS}$ cycling; t_{PC} = t_{PC} min; I_O = 0 mA (Note 5)
Operating current, $\overline{CAS}$ before $\overline{RAS}$ refresh cycle, average	I_{CC5}		960		840		720	mA	$\overline{RAS}$ cycling; $\overline{CAS}$ before $\overline{RAS}$; t_{RC} = t_{RC} min; I_O = 0 mA (Note 5)
Access time from column address	t_{AA}		35		45		55	ns	(Notes 7, 9)
Column address hold time referenced to $\overline{RAS}$	t_{AR}	60		60		70		ns	
Access time from $\overline{CAS}$ precharge (rising edge)	t_{ACP}		40		45		55	ns	(Notes 7, 9)
Column address setup time	t_{ASC}	0		0		0		ns	
Row address setup time	t_{ASR}	0		0		0		ns	
Access time from $\overline{CAS}$ (falling edge)	t_{CAC}		20		20		25	ns	(Notes 7, 9)
Column address hold time	t_{CAH}	17		20		20		ns	
$\overline{CAS}$ pulse width	t_{CAS}	20	10,000	20	10,000	25	10,000	ns	
$\overline{CAS}$ hold time for $\overline{CAS}$ before $\overline{RAS}$ refresh cycle	t_{CHR}	15		15		20		ns	
$\overline{CAS}$ precharge time, fast-page cycle	t_{CP}	10	20	10	20	10	25	ns	
$\overline{CAS}$ precharge time, nonpage cycle	t_{CPN}	10		10		10		ns	
$\overline{CAS}$ to $\overline{RAS}$ precharge time	t_{CRP}	10		10		10		ns	(Note 12)
$\overline{CAS}$ hold time	t_{CSH}	70		80		100		ns	
$\overline{CAS}$ setup time for $\overline{CAS}$ before $\overline{RAS}$ refresh cycle	t_{CSR}	10		10		10		ns	

AC Characteristics (cont)

Parameter	Symbol	-70 Min	-70 Max	-80 Min	-80 Max	-10 Min	-10 Max	Unit	Test Conditions
Data-in hold time	t_{DH}	15		20		20		ns	(Note 15)
Data-in hold time referenced to $\overline{RAS}$	t_{DHR}	60		60		70		ns	
Data-in setup time	t_{DS}	0		0		0		ns	(Note 15)
Output buffer turnoff delay	t_{OFF}	0	15	0	20	0	25	ns	(Note 10)
Fast-page cycle time	t_{PC}	45		50		60		ns	(Note 6)
Access time from $\overline{RAS}$	t_{RAC}		70		80		100	ns	(Notes 7, 8)
$\overline{RAS}$ to column address delay time	t_{RAD}	15	35	17	35	17	45	ns	(Note 9)
Row address hold time	t_{RAH}	10		12		12		ns	
Column address lead time referenced to $\overline{RAS}$ (rising edge)	t_{RAL}	35		45		55		ns	
$\overline{RAS}$ pulse width	t_{RAS}	70	10,000	80	10,000	100	10,000	ns	
$\overline{RAS}$ pulse width, fast-page cycle	t_{RASP}	70	100,000	80	100,000	100	100,000	ns	
Random read or write cycle time	t_{RC}	130		160		190		ns	(Note 6)
$\overline{RAS}$ to $\overline{CAS}$ delay time	t_{RCD}	20	60	25	60	25	75	ns	(Note 11)
Read command hold time referenced to $\overline{CAS}$	t_{RCH}	0		0		0		ns	(Note 13)
Read command setup time	t_{RCS}	0		0		0		ns	
Refresh period	t_{REF}		8		8		8	ms	Addresses A_0 - A_8
$\overline{RAS}$ precharge time	t_{RP}	60		70		80		ns	
$\overline{RAS}$ precharge $\overline{CAS}$ hold time	t_{RPC}	10		10		10		ns	
Read command hold time referenced to $\overline{RAS}$	t_{RRH}	10		10		10		ns	(Note 13)
$\overline{RAS}$ hold time	t_{RSH}	20		20		25		ns	
Rise and fall transition time	t_T	3	50	3	50	3	50	ns	(Note 3)
Write command hold time	t_{WCH}	15		15		20		ns	
Write command hold time referenced to $\overline{RAS}$	t_{WCR}	55		55		70		ns	
Write command setup time	t_{WCS}	0		0		0		ns	(Note 16)
$\overline{WE}$ hold time	t_{WHR}	15		15		20		ns	
Write command pulse width	t_{WP}	15		15		20		ns	(Note 14)

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Notes:

(1) All voltages are referenced to GND.

(2) An initial pause of 100 μs is required after power-up, followed by any eight $\overline{RAS}$ cycles, before proper device operation is achieved.

(3) AC measurements assume t_T = 5 ns.

(4) V_{IH} (min) and V_{IL} (max) are reference levels for measuring the timing of input signals. Transition times are measured between V_{IH} and V_{IL}.

(5) I_{CC1}, I_{CC3}, I_{CC4}, and I_{CC5} depend on output loading and cycle rates. Specified values are obtained with the output open. I_{CC3} is measured assuming that all column address inputs are held at either a high level or a low level during $\overline{RAS}$-only refresh cycles. I_{CC4} is measured assuming that all column address inputs are switched only once during each fast-page cycle.

(6) The minimum specifications are used only to indicate the cycle time at which proper operation over the full temperature range (T_A = 0 to +70°C) is assured.

(7) Load = 2 TTL (–1 mA, +4 mA) loads and 100 pF (V_{OH} = 2.0 V, V_{OL} = 0.8 V).

(8) Assumes that $t_{RCD} \leq t_{RCD}$ (max) and $t_{RAD} \leq t_{RAD}$ (max). If t_{RCD} or t_{RAD} is greater than the maximum recommended value in this table, t_{RAC} increases by the amount that t_{RCD} or t_{RAD} exceeds the value shown.

(9) If $t_{RAD} \geq t_{RAD}$ (max), then the access time is defined by t_{AA}.

(10) t_{OFF} (max) defines the time at which the output achieves the open-circuit condition an is not referenced to V_{OH} or V_{OL}.

(11) Operation within the t_{RCD} (max) limit assures that t_{RAC} (max) can be met. t_{RCD} (max) is specified as a reference point only; if t_{RCD} is greater than t_{RCD} (max), then access time is controlled exclusively by t_{CAC}.

(12) The t_{CRP} requirement should be applicable for $\overline{RAS}$/$\overline{CAS}$ cycles preceded by any cycle.

(13) Either t_{RRH} or t_{RCH} must be satisfied for a read cycle.

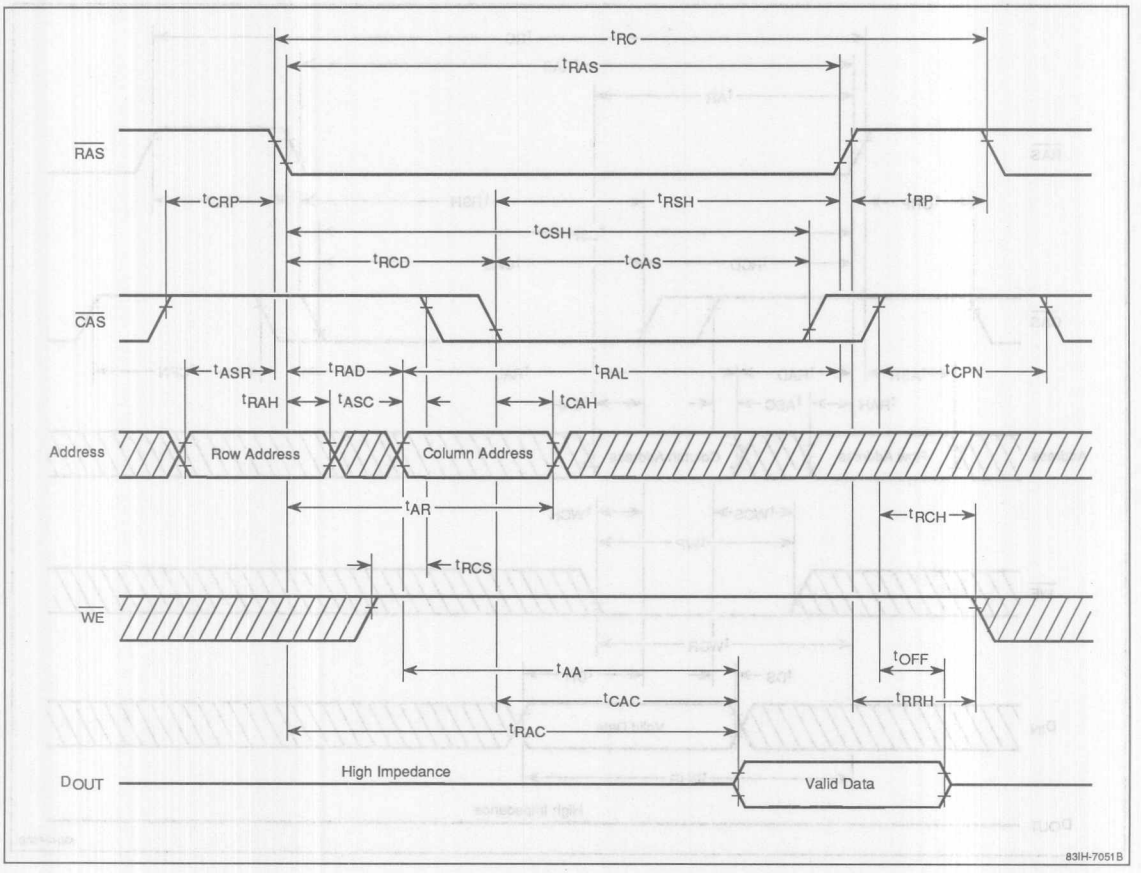
(14) Parameter t_{WP} is applicable for a delayed write cycle such as a read-write/read-modify-write cycle. For early write operation, both t_{WCS} and t_{WCH} must be met.

(15) These parameters are referenced to the falling edge of $\overline{CAS}$ for early write cycles and to the falling edge of $\overline{WE}$ for delayed write or read-modify-write cycles.

(16) t_{WCS}, t_{RWD}, t_{CWD}, and t_{AWD} are restrictive operating parameters in read-write/read-modify-write cycles only. If $t_{WCS} \geq t_{WCS}$ (min), the cycle is an early write cycle and the data output will remain open-circuit throughout the entire cycle. If $t_{CWD} \geq t_{CWD}$ (min), $t_{RWD} \geq t_{RWD}$ (min), and $t_{AWD} \geq t_{AWD}$ (min), the cycle is a read-write cycle and the data output will contain data read from the selected cell. If neither of the above conditions is met, the condition of the data output pin (at access time and until $\overline{CAS}$ returns to V_{IH}) is indeterminate.

Timing Waveforms

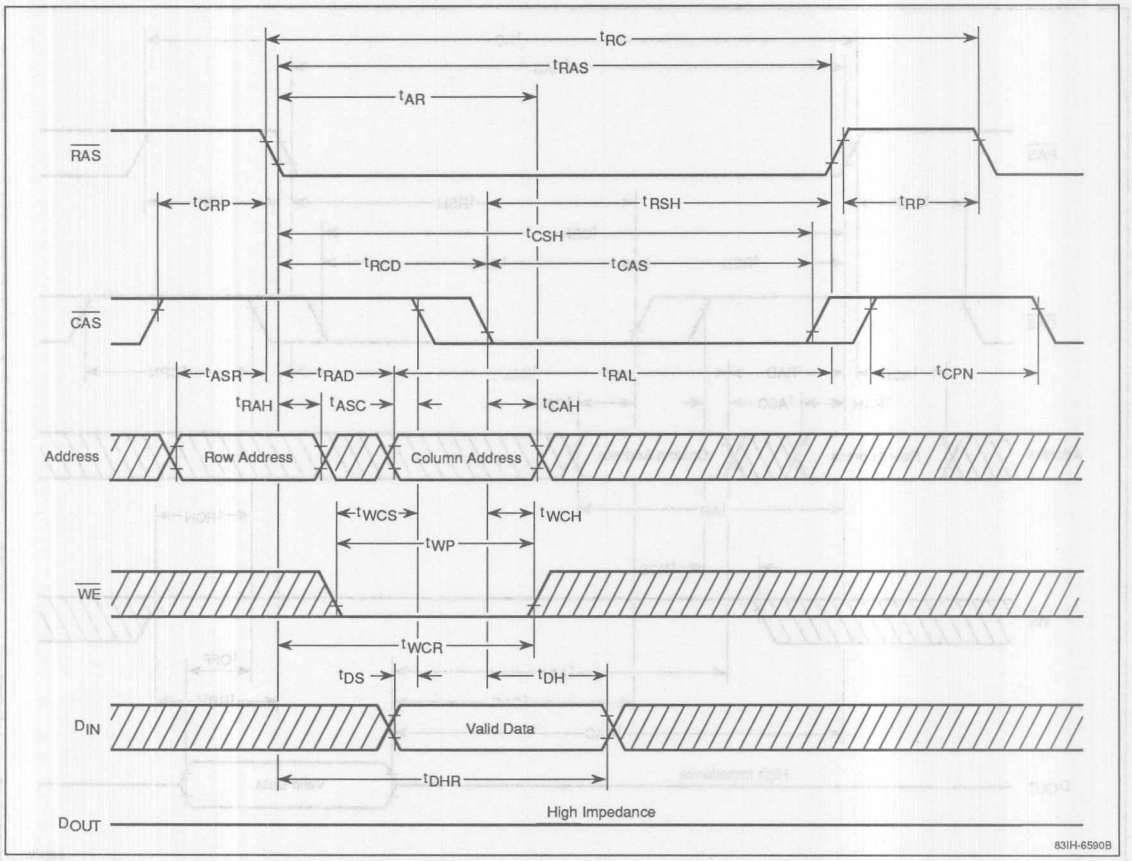
Read Cycle



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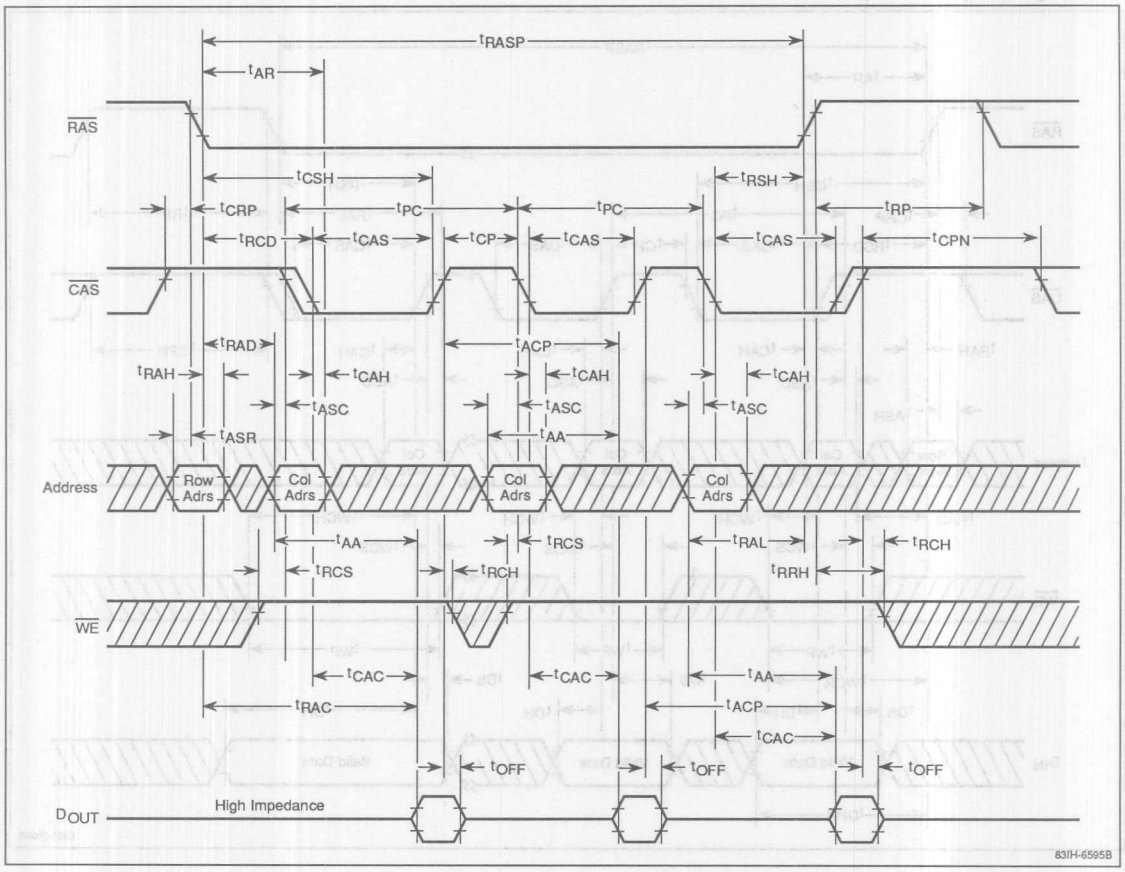
Timing Waveforms (cont)

Early Write Cycle



Timing Waveforms (cont)

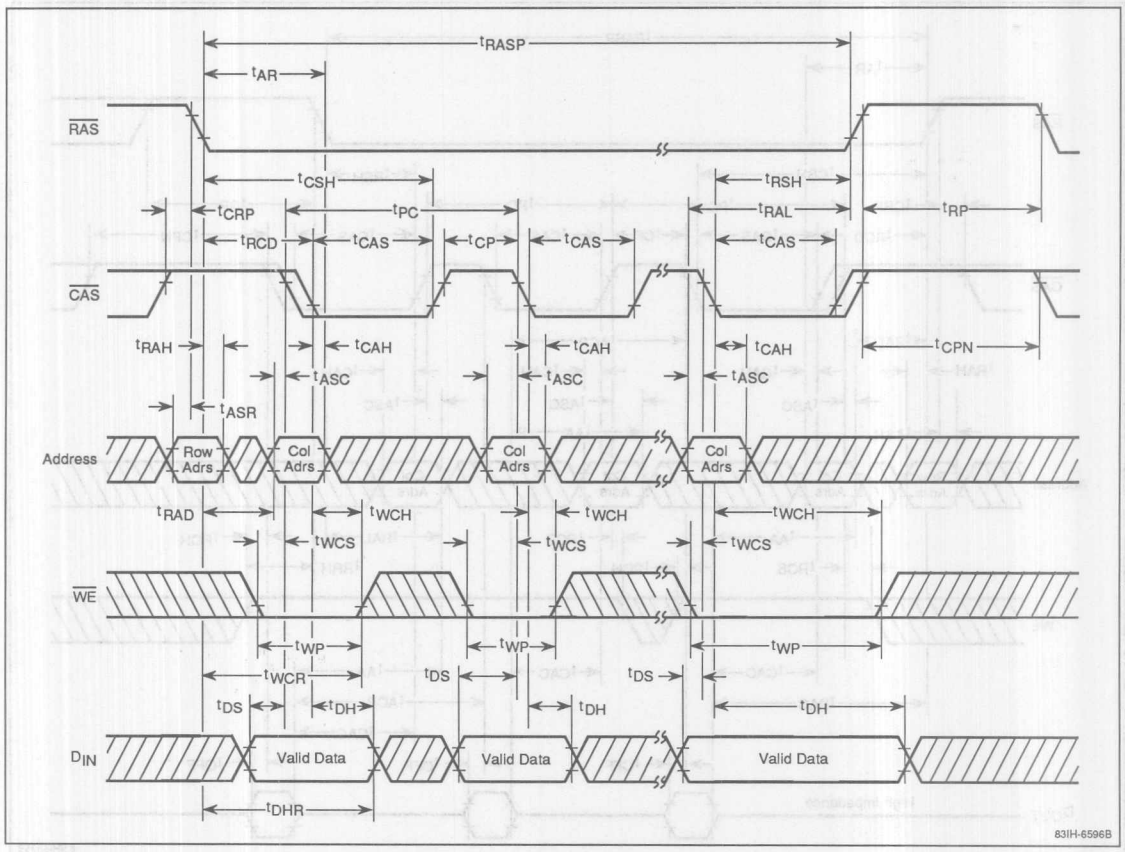
Fast-Page Read Cycle



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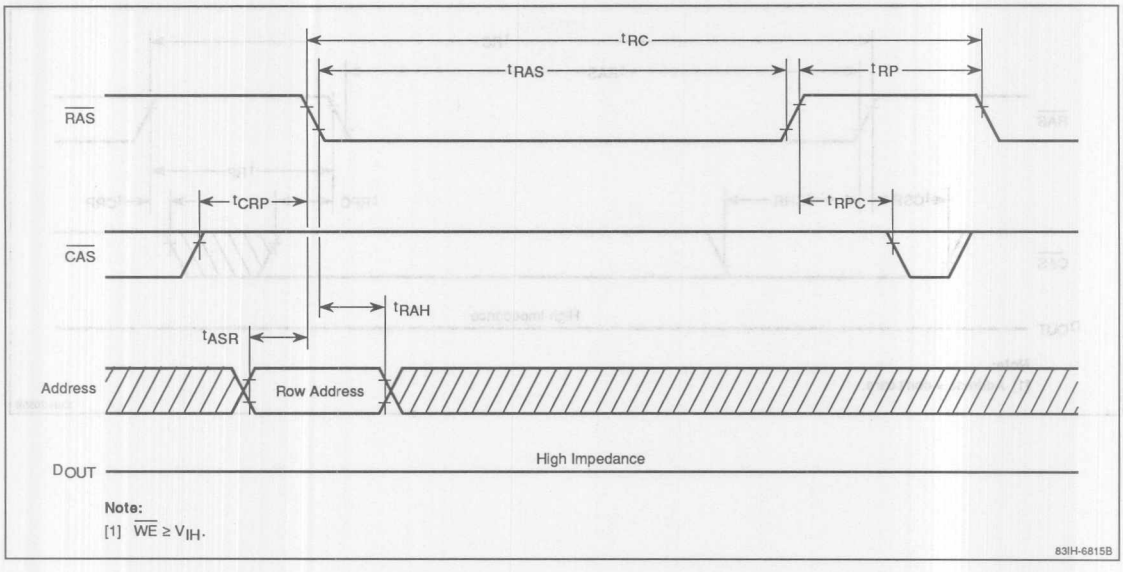
Timing Waveforms (cont)

Fast-Page Early Write Cycle



Timing Waveforms (cont)

$\overline{RAS}$-Only Refresh Cycle

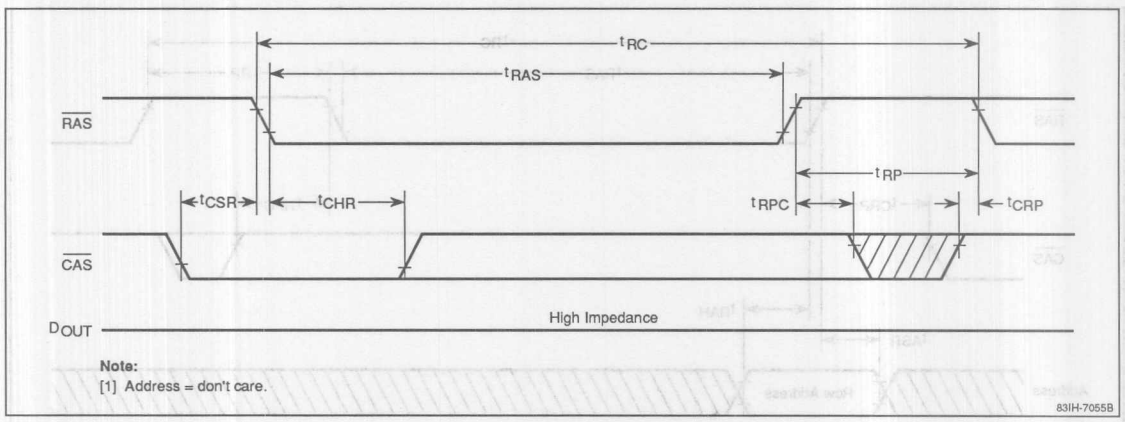


Note:

[1] $\overline{WE} \geq V_{IH}$.

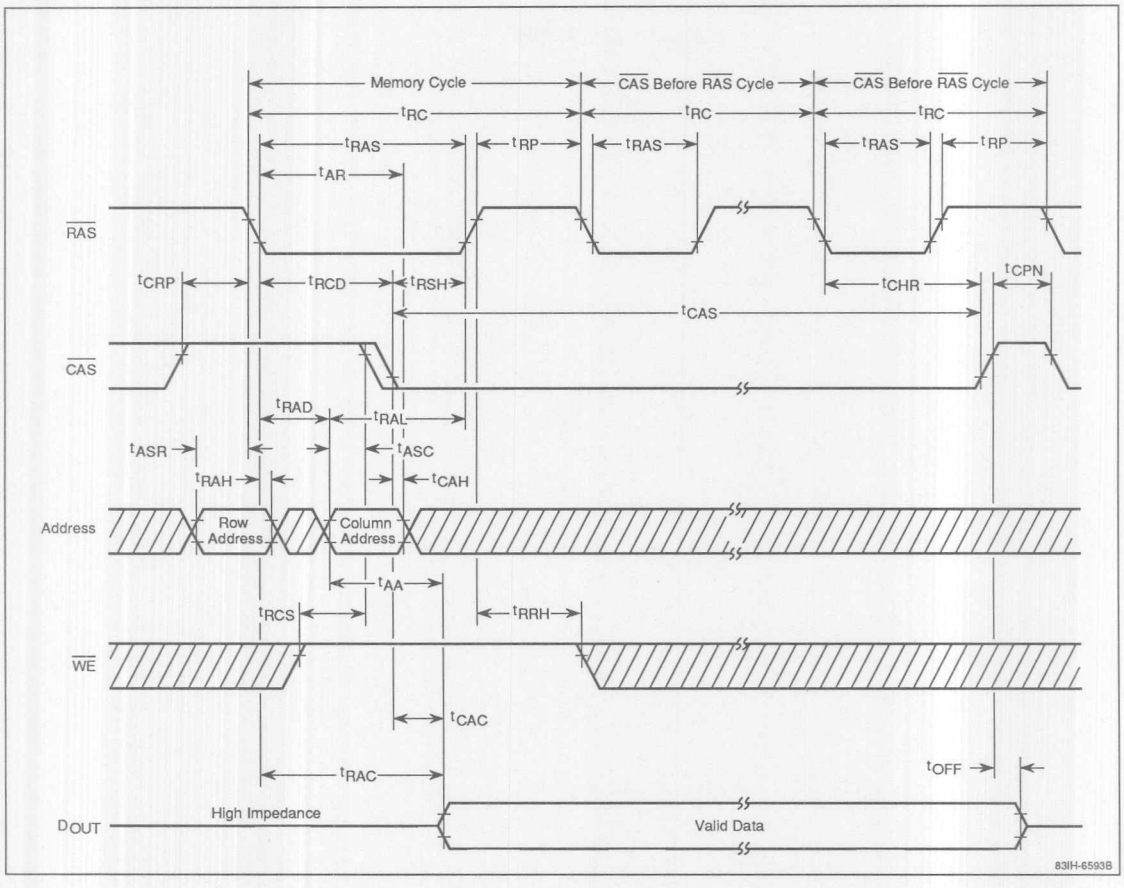
Timing Waveforms (cont)

$\overline{CAS}$ Before $\overline{RAS}$ Refresh Cycle



Timing Waveforms (cont)

Hidden Refresh Cycle



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MC-424512A36
524,288 x 36-Bit
Dynamic RAM Module

Description

The MC-424512A36 is a page mode dynamic RAM module organized as 524,288 words by 36 bits and designed to operate from a single + 5-volt power supply. Advanced circuitry ensures minimum power dissipation and excellent operating margins.

The three-state output is controlled by $\overline{CAS}$ independent of $\overline{RAS}$. After a valid read or read-modify-write cycle, data is held on the output by holding $\overline{CAS}$ low. Data output is returned to high impedance by returning $\overline{CAS}$ high. Refreshing is accomplished by means of $\overline{RAS}$-only refresh cycles, $\overline{CAS}$ before $\overline{RAS}$ refresh cycles, hidden refresh cycles, or by the 512 address combinations of A_0 through A_8 during an 8-ms period.

Single Inline Memory Module (SIMM™) packaging enhances reliability and reduces the size, weight and cost of a system. Each SIMM contains sixteen 262,144 x 4-bit μPD424256s in SOJ packages, eight 262,144 x 1-bit μPD41256s in PLCC packages, and 24 power supply decoupling capacitors for noise reduction. DQ_0 through DQ_{35} are common input/output pins.

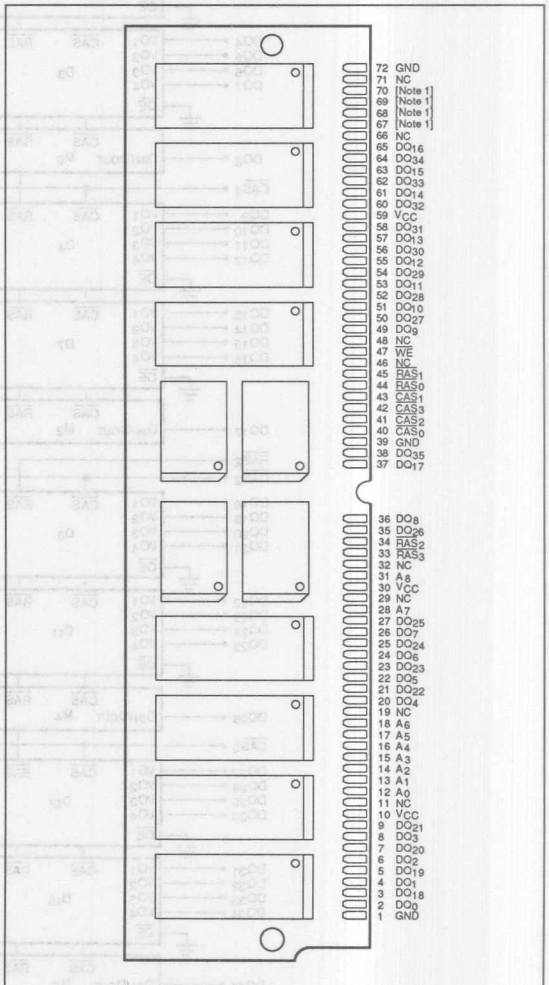
Features

- 524,288-word by 36-bit organization
- Single + 5-volt power supply
- Page mode operation
- Low power dissipation (126 mW max in standby)
- $\overline{RAS}$-only refresh cycles
- $\overline{CAS}$ before $\overline{RAS}$ refresh cycles
- Hidden refresh cycles
- 512 refresh cycles every 8 ms
- TTL-compatible inputs and outputs
- 72-pin SIMM packaging

SIMM is a trademark of Wang Laboratories.

Pin Configuration

72-Pin SIMM



Notes:

[1] Pins 67 through 70 are defined by access time:

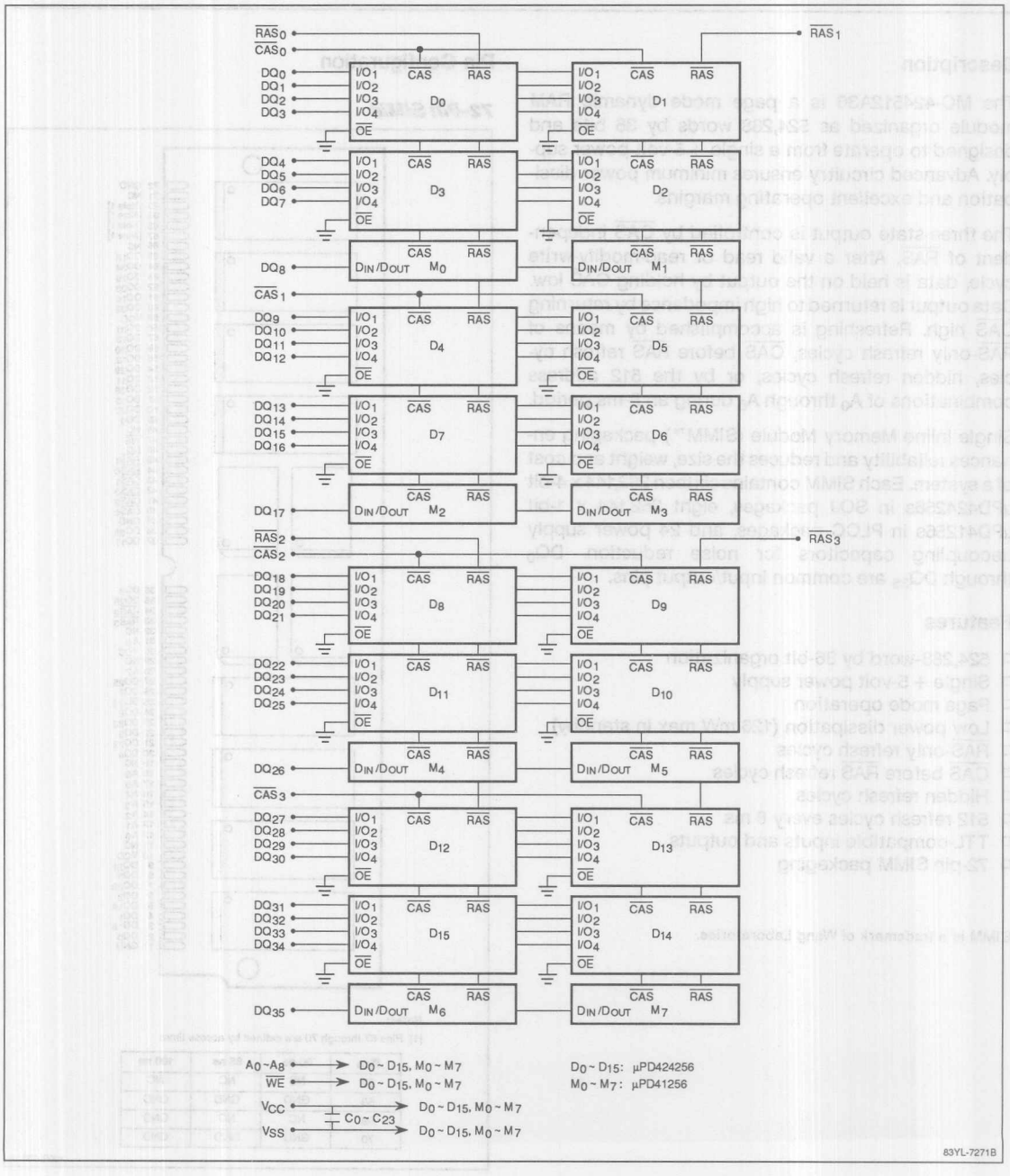
Pins	80 ns	85 ns	100 ns
67	NC	NC	NC
68	GND	GND	GND
69	NC	NC	GND
70	GND	GND	GND

83YL-7319A

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New 70 ns speed and 1-inch height will be available in 1991.

Block Diagram



Pin Identification

Name	Function
A_0 - A_8	Address inputs
$\overline{CAS}_0$ - $\overline{CAS}_3$	Column address strobe
DQ_0 - DQ_{35}	Common data inputs/outputs
$\overline{RAS}_0$ - $\overline{RAS}_3$	Row address strobe
$\overline{WE}$	Write enable
GND	Ground
V_{CC}	+5-volt power supply
NC	No connection

Absolute Maximum Ratings

Voltage on any pin relative to GND	−1.0 to +7.0 V
Operating temperature, T_{OPR}	0 to +70°C
Storage temperature, T_{STG}	−55 to +125°C
Short-circuit output current, I_{OS}	50 mA
Power dissipation, P_D	24 W

Exposure to Absolute Maximum Ratings for extended periods may affect device reliability; exceeding the ratings could cause permanent damage. The device should be operated within the limits specified under DC and AC Characteristics.

Recommended Operating Conditions

Parameter	Symbol	Min	Typ	Max	Unit
Input voltage, high	V_{IH}	2.4		V_{CC} + 1.0	V
Input voltage, low	V_{IL}	−1.0		0.8	V
Supply voltage	V_{CC}	4.75	5.0	5.25	V
Ambient temperature	T_A	0		70	°C

Capacitance

T_A = 25°C; f = 1 MHz

Parameter	Symbol	Max	Unit	Pins Under Test
Input capacitance	C_{I1}	161	pF	A_0 through A_8
	C_{I2}	193	pF	$\overline{WE}$
	C_{I3}	62	pF	$\overline{RAS}$
	C_{I4}	62	pF	$\overline{CAS}$
Input/output capacitance	C_{I1}/C_{O1}	29	pF	DQ_0 - DQ_7, DQ_9 - DQ_{16}, DQ_{18} - DQ_{25}, DQ_{27} - DQ_{34}
	C_{I2}/C_{O2}	39	pF	DQ_8, DQ_{17}, DQ_{26}, DQ_{35}

Ordering Information

Part Number	Row Access Time (max)	R/W Cycle Time (min)	Fast-Page Cycle (min)	Package
MC424512A36B-80	80 ns	160 ns	70 ns	72-pin socket-mountable SIMM (solder plating)
B-85	85 ns	165 ns	70 ns	
B-10	100 ns	200 ns	100 ns	
MC424512A36F-80	80 ns	160 ns	70 ns	72-pin socket-mountable SIMM (gold plating)
F-85	85 ns	165 ns	70 ns	
F-10	100 ns	200 ns	100 ns	

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DC Characteristics

T_A = 0 to +70°C; V_{CC} = +5.0 V ±5%

Parameter	Symbol	Min	Max	Unit	Test Conditions
Standby current	I_{CC2}		72	mA	$\overline{RAS}$ = $\overline{CAS}$ ≥ V_{IH} (min)
			16	mA	$\overline{RAS}$ = $\overline{CAS}$ ≥ V_{CC} – 0.2 V
Input leakage current	$I_{I(L)}$	–240	240	μA	V_{IN} = 0 V to V_{CC}; all other pins not under test = 0 V
Output leakage current	$I_{O(L)}$	–10	10	μA	DQ_0 to DQ_{35} disabled; V_{OUT} = 0 V to V_{CC}
Output voltage, low	V_{OL}		0.4	V	I_{OL} = 4.2 mA
Output voltage, high	V_{OH}	2.4		V	I_{OH} = –5 mA

AC Characteristics

T_A = 0 to +70°C; V_{CC} = +5.0 V ±5%

		-80		-85		-10			
Parameter	Symbol	Min	Max	Min	Max	Min	Max	Unit	Test Conditions
Operating current, average	I_{CC1}		1024		872		744	mA	$\overline{RAS}$ and $\overline{CAS}$ cycling; t_{RC} = t_{RC} min; I_O = 0 mA (Note 5)
Operating current, $\overline{RAS}$-only refresh cycle, average	I_{CC3}		1024		872		744	mA	$\overline{RAS}$ cycling; $\overline{CAS}$ ≥ V_{IH}; t_{RC} = t_{RC} min; I_O = 0 mA (Note 5)
Operating current, page mode cycle, average	I_{CC4}		996		828		724	mA	$\overline{RAS}$ ≤ V_{IL}; $\overline{CAS}$ cycling; t_{PC} = t_{PC} min; I_O = 0 mA (Note 5)
Operating current, $\overline{CAS}$ before $\overline{RAS}$ refresh cycle, average	I_{CC5}		1024		872		744	mA	$\overline{RAS}$ cycling; $\overline{CAS}$ before $\overline{RAS}$; t_{RC} = t_{RC} min; I_O = 0 mA (Note 5)
Column address hold time referenced to $\overline{RAS}$	t_{AR}	55		55		65		ns	
Column address setup time	t_{ASC}	0		0		0		ns	
Row address setup time	t_{ASR}	0		0		0		ns	
Access time from $\overline{CAS}$ (falling edge)	t_{CAC}		40		40		50	ns	(Notes 7, 9)
Column address hold time	t_{CAH}	20		20		20		ns	
$\overline{CAS}$ pulse width	t_{CAS}	40	10,000	40	10,000	50	10,000	ns	
$\overline{CAS}$ hold time for $\overline{CAS}$ before $\overline{RAS}$ refresh cycle	t_{CHR}	15		15		20		ns	
$\overline{CAS}$ precharge time, page cycle	t_{CP}	20		20		40		ns	
$\overline{CAS}$ precharge time, nonpage cycle	t_{CPN}	25		25		25		ns	

AC Characteristics (cont)

Parameter	Symbol	-80 Min	-80 Max	-85 Min	-85 Max	-10 Min	-10 Max	Unit	Test Conditions
$\overline{CAS}$ to $\overline{RAS}$ precharge time	t_{CRP}	10		10		10		ns	(Note 12)
$\overline{CAS}$ hold time	t_{CSH}	80		85		100		ns	
$\overline{CAS}$ setup time for $\overline{CAS}$ before $\overline{RAS}$ refresh cycle	t_{CSR}	10		10		10		ns	
Data-in hold time	t_{DH}	20		20		25		ns	(Note 15)
Data-in hold time referenced to $\overline{RAS}$	t_{DHR}	60		65		75		ns	
Data-in setup time	t_{DS}	0		0		0		ns	(Note 15)
Output buffer turnoff delay	t_{OFF}	0	20	0	20	0	25	ns	(Note 10)
Page cycle time	t_{PC}	70		70		100		ns	(Note 6)
Access time from $\overline{RAS}$	t_{RAC}		80		85		100	ns	(Notes 7, 8)
Row address hold time	t_{RAH}	12		12		12		ns	
$\overline{RAS}$ pulse width	t_{RAS}	80	10,000	85	10,000	100	10,000	ns	
Random read or write cycle time	t_{RC}	160		165		200		ns	(Note 6)
$\overline{RAS}$ to $\overline{CAS}$ delay time	t_{RCD}	20	40	25	45	25	50	ns	(Note 11)
Read command hold time referenced to $\overline{CAS}$	t_{RCH}	0		0		0		ns	(Note 13)
Read command setup time	t_{RCS}	0		0		0		ns	
Refresh period	t_{REF}		8		8		8	ms	Addresses A_0 - A_8
$\overline{RAS}$ precharge time	t_{RP}	70		70		90		ns	
$\overline{RAS}$ precharge $\overline{CAS}$ hold time	t_{RPC}	0		0		0		ns	
Read command hold time referenced to $\overline{RAS}$	t_{RRH}	10		10		10		ns	(Note 13)
$\overline{RAS}$ hold time	t_{RSH}	40		40		50		ns	
Rise and fall transition time	t_T	3	50	3	50	3	50	ns	(Note 3)
Write command hold time	t_{WCH}	20		20		25		ns	

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AC Characteristics (cont)

Parameter	Symbol	-80 Min	-80 Max	-85 Min	-85 Max	-10 Min	-10 Max	Unit	Test Conditions
Write command hold time referenced to $\overline{RAS}$	t_{WCR}	60		65		75		ns	
Write command setup time	t_{WCS}	0		0		0		ns	(Note 16)
Write command pulse width	t_{WP}	15		15		15		ns	(Note 14)

Notes:

(1) All voltages are referenced to GND.

(2) An initial pause of 100 μs is required after power-up, followed by any eight $\overline{RAS}$ cycles, before proper device operation is achieved.

(3) AC measurements assume t_T = 5 ns.

(4) V_{IH} (min) and V_{IL} (max) are reference levels for measuring the timing of input signals. Transition times are measured between V_{IH} and V_{IL}.

(5) I_{CC1}, I_{CC3}, I_{CC4}, and I_{CC5} depend on output loading and cycle rates. Specified values are obtained with the output open. I_{CC3} is measured assuming that all column address inputs are held at either a high level or a low level during $\overline{RAS}$-only refresh cycles. I_{CC4} is measured assuming that all column address inputs are switched only once during each fast-page cycle.

(6) The minimum specifications are used only to indicate the cycle time at which proper operation over the full temperature range (T_A = 0 to +70°C) is assured.

(7) Load = 2 TTL (–1 mA, +4 mA) loads and 100 pF (V_{OH} = 2.0 V, V_{OL} = 0.8 V).

(8) Assumes that $t_{RCD} \leq t_{RCD}$ (max) and $t_{RAD} \leq t_{RAD}$ (max). If t_{RCD} or t_{RAD} is greater than the maximum recommended value in this table, t_{RAC} increases by the amount that t_{RCD} or t_{RAD} exceeds the value shown.

(9) If $t_{RAD} \geq t_{RAD}$ (max), then the access time is defined by t_{AA}.

(10) t_{OFF} (max) defines the time at which the output achieves the open-circuit condition an is not referenced to V_{OH} or V_{OL}.

(11) Operation within the t_{RCD} (max) limit assures that t_{RAC} (max) can be met. t_{RCD} (max) is specified as a reference point only; if t_{RCD} is greater than t_{RCD} (max), then access time is controlled exclusively by t_{CAC}.

(12) The t_{CRP} requirement should be applicable for $\overline{RAS}$/$\overline{CAS}$ cycles preceded by any cycle.

(13) Either t_{RRH} or t_{RCH} must be satisfied for a read cycle.

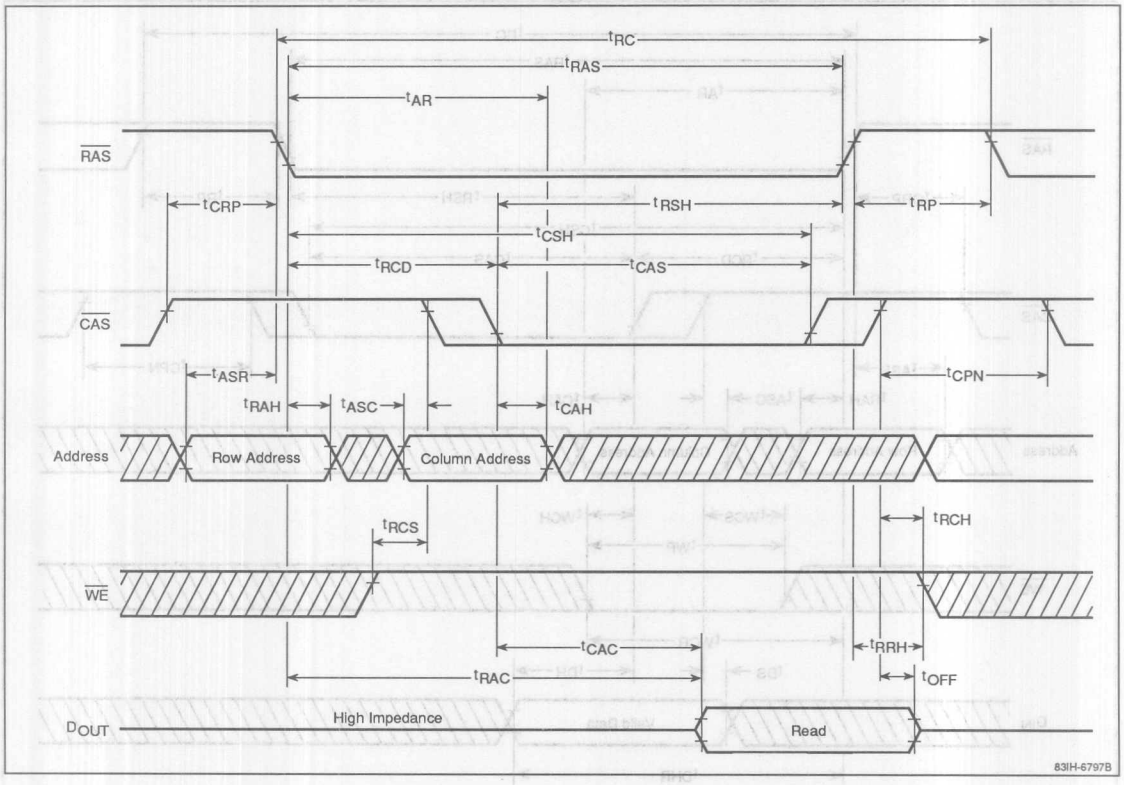
(14) Parameter t_{WP} is applicable for a delayed write cycle such as a read-write/read-modify-write cycle. For early write operation, both t_{WCS} and t_{WCH} must be met.

(15) These parameters are referenced to the falling edge of $\overline{CAS}$ for early write cycles and to the falling edge of $\overline{WE}$ for delayed write or read-modify-write cycles.

(16) t_{WCS}, t_{RWD}, t_{CWD}, and t_{AWD} are restrictive operating parameters in read-write/read-modify-write cycles only. If $t_{WCS} \geq t_{WCS}$ (min), the cycle is an early write cycle and the data output will remain open-circuit throughout the entire cycle. If $t_{CWD} \geq t_{CWD}$ (min), $t_{RWD} \geq t_{RWD}$ (min), and $t_{AWD} \geq t_{AWD}$ (min), the cycle is a read-write cycle and the data output will contain data read from the selected cell. If neither of the above conditions is met, the condition of the data output pin (at access time and until $\overline{CAS}$ returns to V_{IH}) is indeterminate.

Timing Waveforms

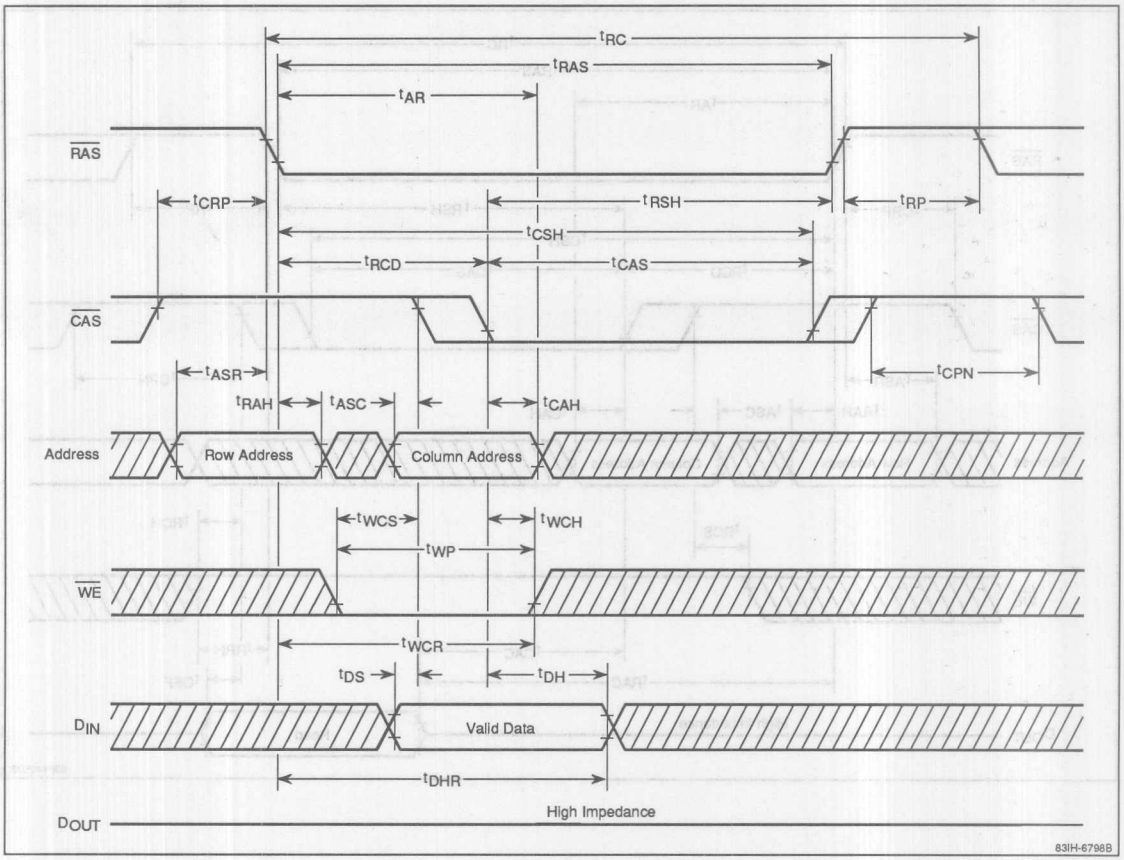
Read Cycle



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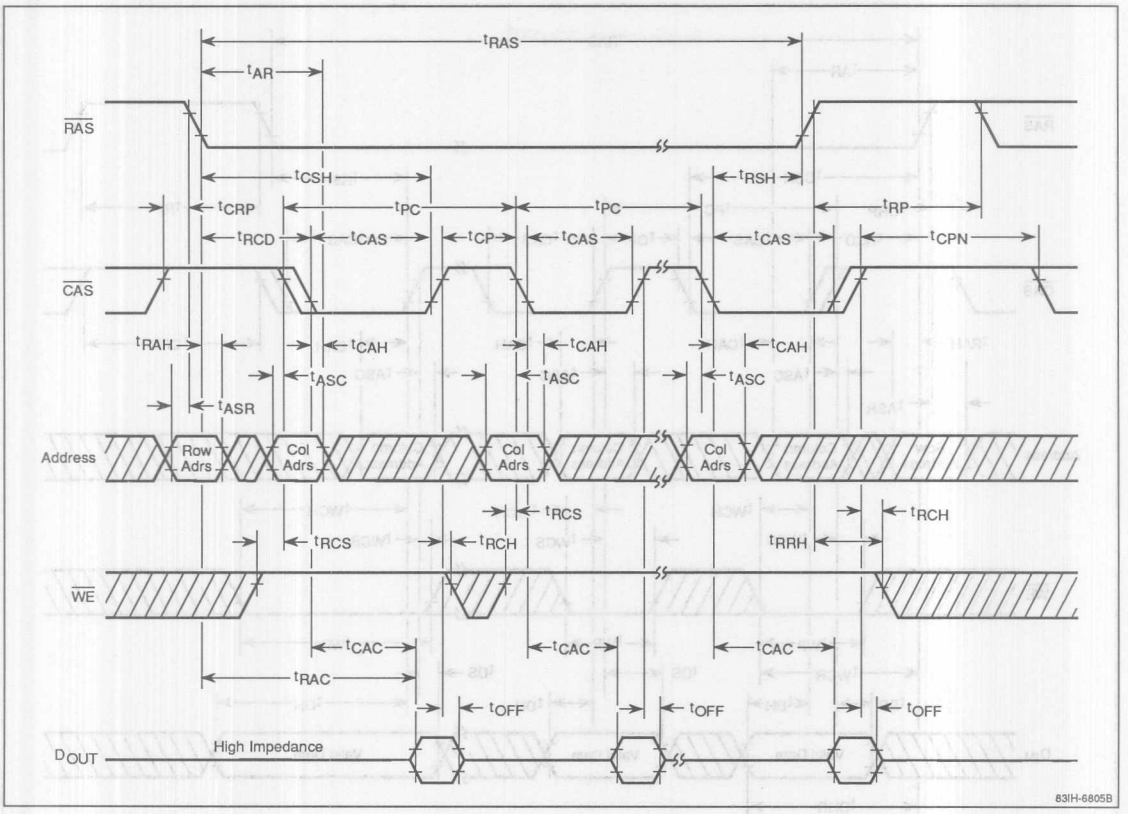
Timing Waveforms (cont)

Early Write Cycle



Timing Waveforms (cont)

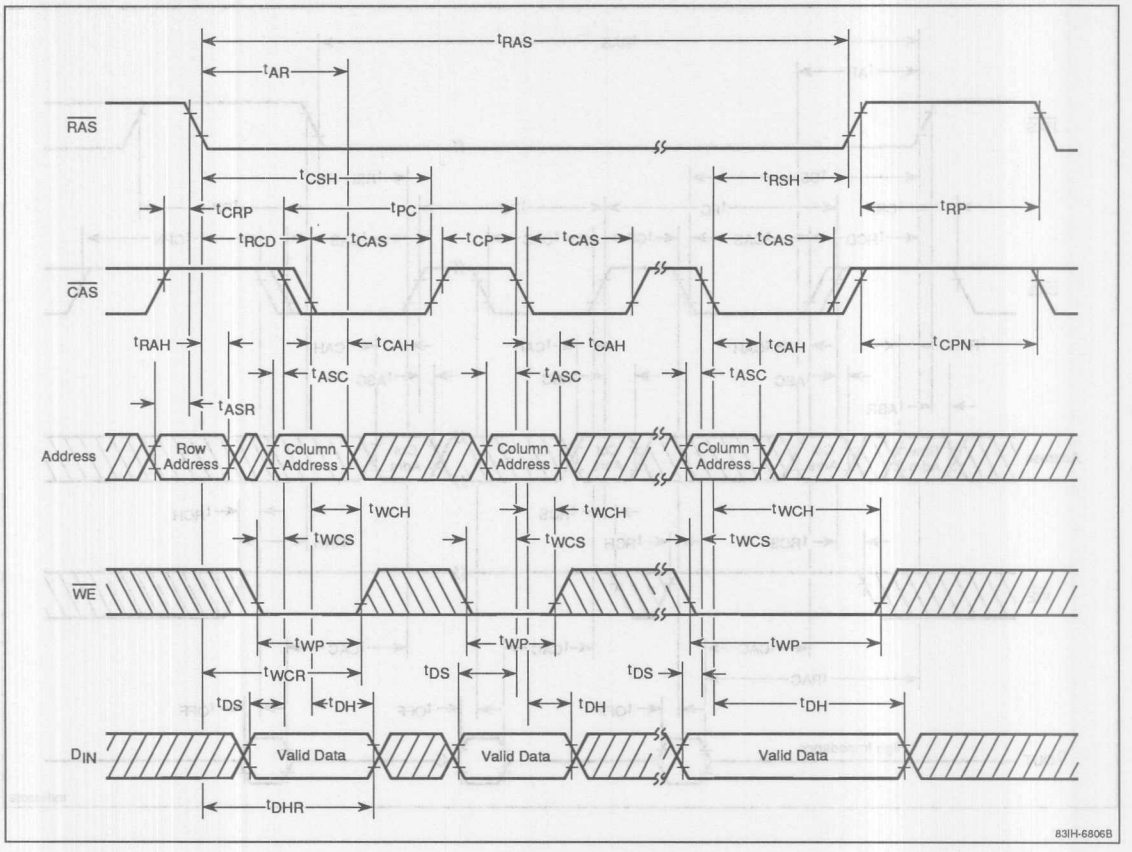
Page Mode Read Cycle



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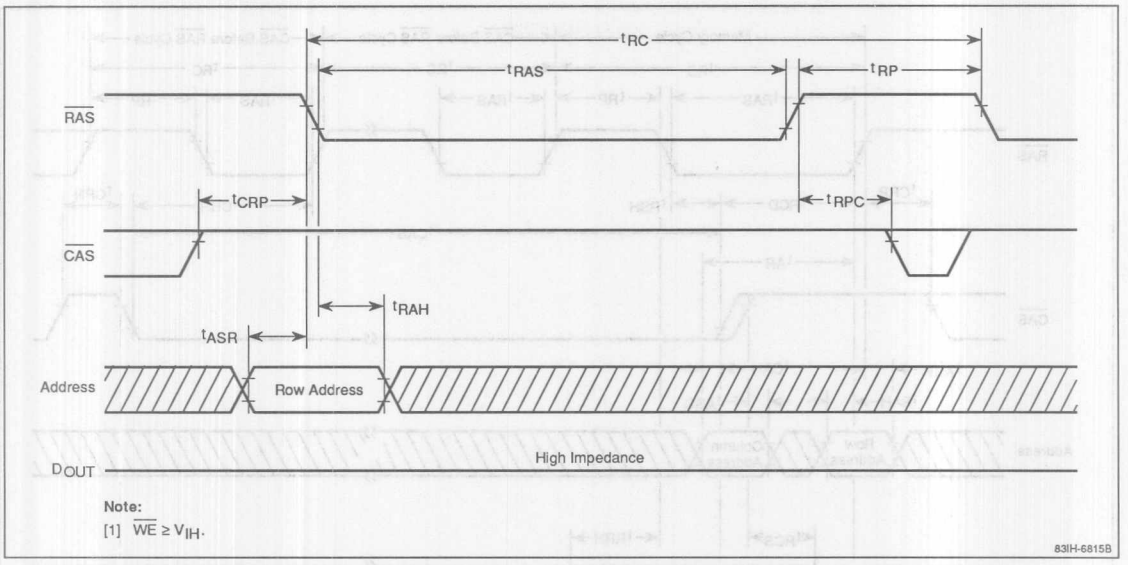
Timing Waveforms (cont)

Page Early Write Cycle



Timing Waveforms (cont)

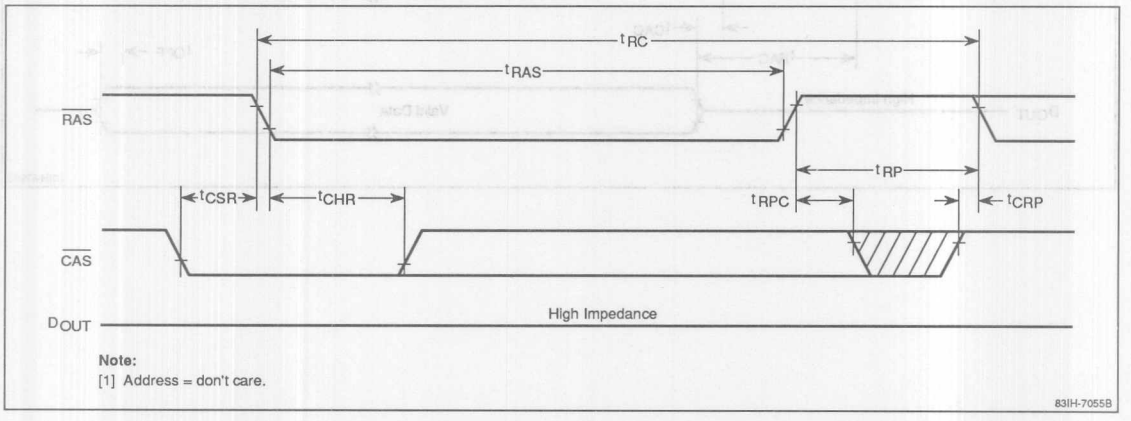
$\overline{RAS}$-Only Refresh Cycle



Note:
[1] $\overline{WE} \geq V_{IH}$.

83IH-6815B

$\overline{CAS}$ Before $\overline{RAS}$ Refresh Cycle



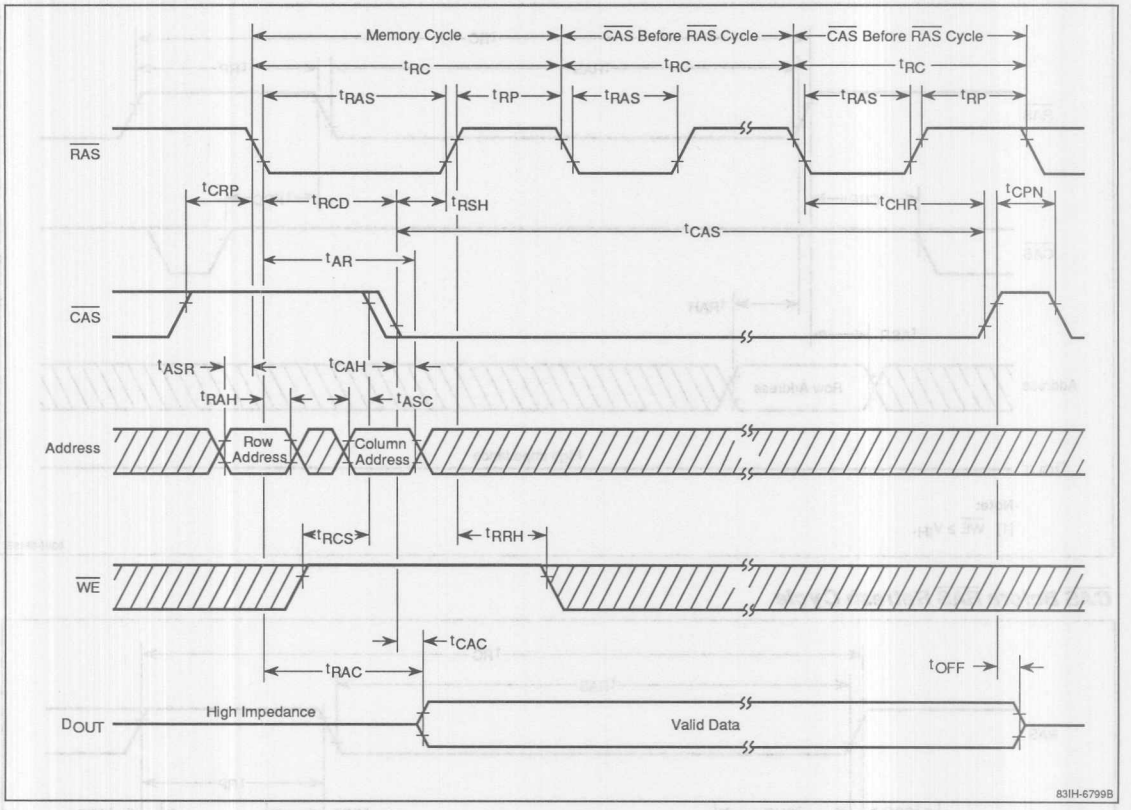
Note:
[1] Address = don't care.

83IH-7055B

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Timing Waveforms (cont)

Hidden Refresh Cycle



NEC Electronics Inc.

MC-424512A36BH/FH
524,288 x 36-Bit
Dynamic CMOS RAM Module

Description

The MC-42512A36BH/FH is a fast-page dynamic RAM module organized as 524,288 words by 36 bits and designed to operate from a single + 5-volt power supply. Advanced CMOS circuitry ensures minimum power dissipation and excellent operating margins.

The three-state output is controlled by $\overline{CAS}$ independent of $\overline{RAS}$. After a valid read or read-modify-write cycle, data is held on the output by holding $\overline{CAS}$ low. Data output is returned to high impedance by returning $\overline{CAS}$ high. Fast-page read and write cycles can be executed by cycling $\overline{CAS}$. Refreshing is accomplished by means of $\overline{RAS}$-only refresh cycles, $\overline{CAS}$ before $\overline{RAS}$ refresh cycles, hidden refresh cycles, or by the 512 address combinations of A_0 through A_8 during a 8-ms period.

Single Inline Memory Module (SIMM™) packaging enhances reliability and reduces the size, weight and cost of a system. Each SIMM contains sixteen 262,144 x 4-bit μPD424256s in SOJ packages, eight 1,048,576 x 1-bit μPD421000s in SOJ packages, and twenty-four power supply decoupling capacitors for noise reduction. DQ_0 through DQ_{35} are common input/output pins.

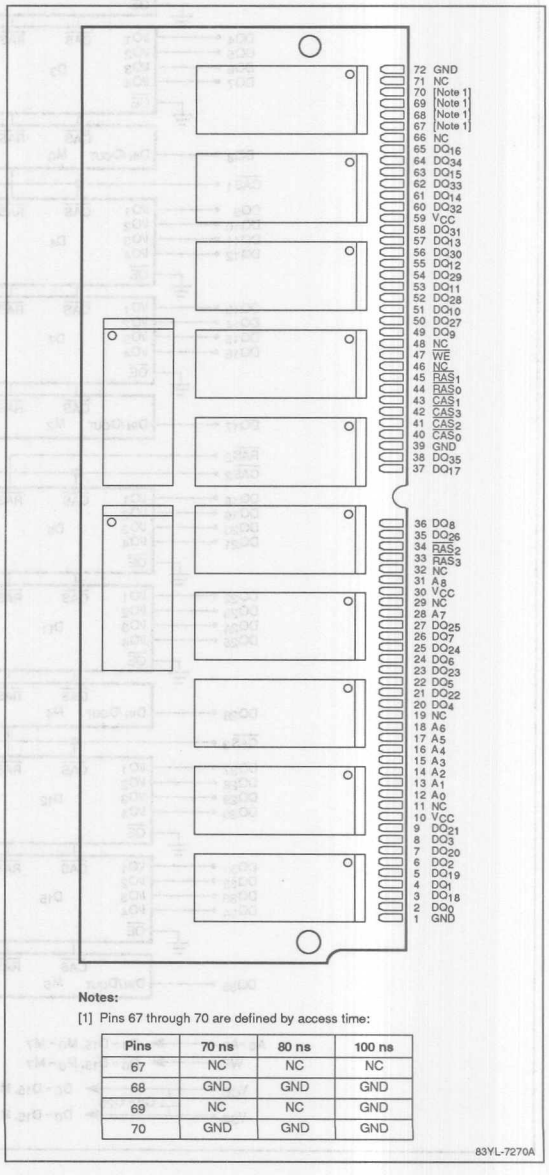
Features

- 524,288-word by 36-bit organization
- Single + 5-volt power supply
- Fast-page cycles
- Low power dissipation (252 mW max in standby)
- $\overline{RAS}$-only refresh cycles
- $\overline{CAS}$ before $\overline{RAS}$ refresh cycles
- Hidden refresh cycles
- 512 refresh cycles every 8 ms
- TTL-compatible inputs and outputs
- 72-pin SIMM packaging

SIMM is a trademark of Wang Laboratories.

Pin Configuration

72-Pin SIMM



Notes:

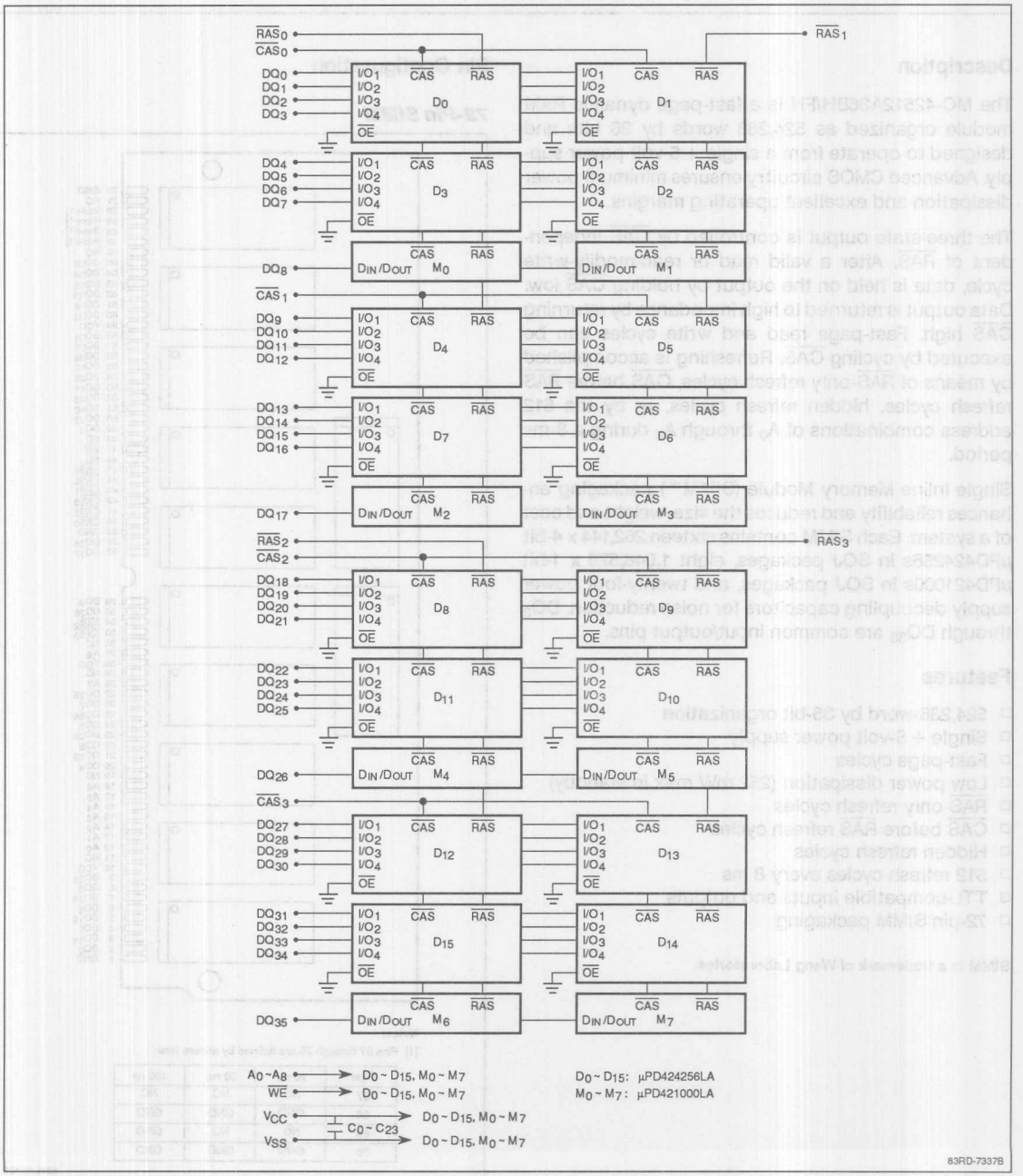
[1] Pins 67 through 70 are defined by access time:

Pins	70 ns	80 ns	100 ns
67	NC	NC	NC
68	GND	GND	GND
69	NC	NC	GND
70	GND	GND	GND

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Block Diagram



Pin Identification

Name	Function
A_0 - A_8	Address inputs
$\overline{CAS}_0$ - $\overline{CAS}_3$	Column address strobe
DQ_0 - DQ_{35}	Common data inputs/outputs
$\overline{RAS}_0$ - $\overline{RAS}_3$	Row address strobe
$\overline{WE}$	Write enable
GND	Ground
V_{CC}	+5-volt power supply
NC	No connection

Absolute Maximum Ratings

Voltage on any pin relative to GND	−1.0 to +7.0 V
Operating temperature, T_{OPR}	0 to +70°C
Storage temperature, T_{STG}	−55 to +125°C
Short-circuit output current, I_{OS}	50 mA
Power dissipation, P_D	24 W

Exposure to Absolute Maximum Ratings for extended periods may affect device reliability; exceeding the ratings could cause permanent damage. The device should be operated within the limits specified under DC and AC Characteristics.

Recommended Operating Conditions

Parameter	Symbol	Min	Typ	Max	Unit
Input voltage, high	V_{IH}	2.4		V_{CC} + 1.0	V
Input voltage, low	V_{IL}	−1.0		0.8	V
Supply voltage	V_{CC}	4.75	5.0	5.25	V
Ambient temperature	T_A	0		70	°C

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Capacitance

T_A = 25°C; f = 1 MHz

Parameter	Symbol	Max	Unit	Pins Under Test
Input capacitance	C_{I1}	161	pF	A_0 - A_9
	C_{I2}	193	pF	$\overline{WE}$
	C_{I3}	62	pF	$\overline{RAS}$
	C_{I4}	62	pF	$\overline{CAS}$
Input/output capacitance	C_{I1}/C_{O1}	29	pF	DQ_0 - DQ_7, DQ_9 - DQ_{16}, DQ_{18} - DQ_{25}, DQ_{27} - DQ_{34}
	C_{I2}/C_{O2}	39	pF	DQ_8, DQ_{17}, DQ_{26}, DQ_{35}

Ordering Information

Part Number	Row Access Time (max)	R/W Cycle Time (min)	Fast-Page Cycle (min)	Package
MC424512A36BH-70	70 ns	130 ns	45 ns	72-pin socket-mountable SIMM (solder plating)
BH-80	80 ns	160 ns	50 ns	
BH-10	100 ns	190 ns	60 ns	
MC424512A36FH-70	70 ns	130 ns	45 ns	72-pin socket-mountable SIMM (gold plating)
FH-80	80 ns	160 ns	50 ns	
FH-10	100 ns	190 ns	60 ns	

DC Characteristics

T_A = 0 to +70°C; V_{CC} = +5.0 V ±5%

Parameter	Symbol	Min	Max	Unit	Test Conditions
Standby current	I_{CC2}		24	mA	$\overline{RAS}$ = $\overline{CAS}$ ≥ V_{IH} (min)
			12	mA	$\overline{RAS}$ = $\overline{CAS}$ ≥ V_{CC} – 0.2 V
Input leakage current	$I_{I(L)}$	–240	240	μA	V_{IN} = 0 V to V_{CC}; all other pins not under test = 0 V
Output leakage current	$I_{O(L)}$	–10	10	μA	DQ_0 to DQ_{35} disabled; V_{OUT} = 0 V to V_{CC}
Output voltage, low	V_{OL}		0.4	V	I_{OL} = 4.2 mA
Output voltage, high	V_{OH}	2.4		V	I_{OH} = –5 mA

AC Characteristics

T_A = 0 to +70°C; V_{CC} = +5.0 V ±5%

		-70		-80		-10			
Parameter	Symbol	Min	Max	Min	Max	Min	Max	Unit	Test Conditions
Operating current, average	I_{CC1}		1040		910		780	mA	$\overline{RAS}$ and $\overline{CAS}$ cycling; t_{RC} = t_{RC} min; I_O = 0 mA (Note 5)
Operating current, $\overline{RAS}$-only refresh cycle, average	I_{CC3}		1040		910		780	mA	$\overline{RAS}$ cycling; $\overline{CAS}$ ≥ V_{IH}; t_{RC} = t_{RC} min; I_O = 0 mA (Note 5)
Operating current, fast-page cycle, average	I_{CC4}		910		780		650	mA	$\overline{RAS}$ ≤ V_{IL}; $\overline{CAS}$ cycling; t_{PC} = t_{PC} min; I_O = 0 mA (Note 5)
Operating current, $\overline{CAS}$ before $\overline{RAS}$ refresh cycle, average	I_{CC5}		1040		910		780	mA	$\overline{RAS}$ cycling; $\overline{CAS}$ before $\overline{RAS}$; t_{RC} = t_{RC} min; I_O = 0 mA (Note 5)
Access time from column address	t_{AA}		35		45		55	ns	(Notes 7, 9)
Column address hold time referenced to $\overline{RAS}$	t_{AR}	60		60		70		ns	
Access time from $\overline{CAS}$ precharge (rising edge)	t_{ACP}		40		45		55	ns	(Notes 7, 9)
Column address setup time	t_{ASC}	0		0		0		ns	
Row address setup time	t_{ASR}	0		0		0		ns	
Access time from $\overline{CAS}$ (falling edge)	t_{CAC}		20		20		25	ns	(Notes 7, 9)
Column address hold time	t_{CAH}	17		20		20		ns	
$\overline{CAS}$ pulse width	t_{CAS}	20	10,000	20	10,000	25	10,000	ns	
$\overline{CAS}$ hold time for $\overline{CAS}$ before $\overline{RAS}$ refresh cycle	t_{CHR}	15		15		20		ns	
$\overline{CAS}$ precharge time, fast-page cycle	t_{CP}	10	20	10	20	10	25	ns	

AC Characteristics (cont)

Parameter	Symbol	-70 Min	-70 Max	-80 Min	-80 Max	-10 Min	-10 Max	Unit	Test Conditions
$\overline{CAS}$ precharge time, nonpage cycle	t_{CPN}	10		10		10		ns	
$\overline{CAS}$ to $\overline{RAS}$ precharge time	t_{CRP}	10		10		10		ns	(Note 12)
$\overline{CAS}$ hold time	t_{CSH}	70		80		100		ns	
$\overline{CAS}$ setup time for $\overline{CAS}$ before $\overline{RAS}$ refresh cycle	t_{CSR}	10		10		10		ns	
Data-in hold time	t_{DH}	15		20		20		ns	(Note 15)
Data-in hold time referenced to $\overline{RAS}$	t_{DHR}	60		60		70		ns	
Data-in setup time	t_{DS}	0		0		0		ns	(Note 15)
Output buffer turnoff delay	t_{OFF}	0	15	0	20	0	25	ns	(Note 10)
Fast-page cycle time	t_{PC}	45		50		60		ns	(Note 6)
Access time from $\overline{RAS}$	t_{RAC}		70		80		100	ns	(Notes 7, 8)
$\overline{RAS}$ to column address delay time	t_{RAD}	15	35	17	35	17	45	ns	(Note 9)
Row address hold time	t_{RAH}	10		12		12		ns	
Column address lead time referenced to $\overline{RAS}$ (rising edge)	t_{RAL}	35		45		55		ns	
$\overline{RAS}$ pulse width	t_{RAS}	70	10,000	80	10,000	100	10,000	ns	
$\overline{RAS}$ pulse width, fast-page cycle	t_{RASP}	70	100,000	80	100,000	100	100,000	ns	
Random read or write cycle time	t_{RC}	130		160		190		ns	(Note 6)
$\overline{RAS}$ to $\overline{CAS}$ delay time	t_{RCD}	20	60	25	60	25	75	ns	(Note 11)
Read command hold time referenced to $\overline{CAS}$	t_{RCH}	0		0		0		ns	(Note 13)
Read command setup time	t_{RCS}	0		0		0		ns	
Refresh period	t_{REF}		8		8		8	ms	Addresses A_0 - A_8
$\overline{RAS}$ precharge time	t_{RP}	60		70		80		ns	
$\overline{RAS}$ precharge $\overline{CAS}$ hold time	t_{RPC}	10		10		10		ns	
Read command hold time referenced to $\overline{RAS}$	t_{RRH}	10		10		10		ns	(Note 13)
$\overline{RAS}$ hold time	t_{RSH}	20		20		25		ns	
Rise and fall transition time	t_T	3	50	3	50	3	50	ns	(Note 3)

AC Characteristics (cont)

Parameter	Symbol	-70 Min	-70 Max	-80 Min	-80 Max	-10 Min	-10 Max	Unit	Test Conditions
Write command hold time	t_{WCH}	15		15		20		ns	
Write command hold time referenced to $\overline{RAS}$	t_{WCR}	55		55		70		ns	
Write command setup time	t_{WCS}	0		0		0		ns	(Note 16)
Write command pulse width	t_{WP}	15		15		20		ns	(Note 14)

Notes:

(1) All voltages are referenced to GND.

(2) An initial pause of 100 μs is required after power-up, followed by any eight $\overline{RAS}$ cycles, before proper device operation is achieved.

(3) AC measurements assume t_T = 5 ns.

(4) V_{IH} (min) and V_{IL} (max) are reference levels for measuring the timing of input signals. Transition times are measured between V_{IH} and V_{IL}.

(5) I_{CC1}, I_{CC3}, I_{CC4}, and I_{CC5} depend on output loading and cycle rates. Specified values are obtained with the output open. I_{CC3} is measured assuming that all column address inputs are held at either a high level or a low level during $\overline{RAS}$-only refresh cycles. I_{CC4} is measured assuming that all column address inputs are switched only once during each fast-page cycle.

(6) The minimum specifications are used only to indicate the cycle time at which proper operation over the full temperature range (T_A = 0 to +70°C) is assured.

(7) Load = 2 TTL (–1 mA, +4 mA) loads and 100 pF (V_{OH} = 2.0 V, V_{OL} = 0.8 V).

(8) Assumes that $t_{RCD} \leq t_{RCD}$ (max) and $t_{RAD} \leq t_{RAD}$ (max). If t_{RCD} or t_{RAD} is greater than the maximum recommended value in this table, t_{RAC} increases by the amount that t_{RCD} or t_{RAD} exceeds the value shown.

(9) If $t_{RAD} \geq t_{RAD}$ (max), then the access time is defined by t_{AA}.

(10) t_{OFF} (max) defines the time at which the output achieves the open-circuit condition an is not referenced to V_{OH} or V_{OL}.

(11) Operation within the t_{RCD} (max) limit assures that t_{RAC} (max) can be met. t_{RCD} (max) is specified as a reference point only; if t_{RCD} is greater than t_{RCD} (max), then access time is controlled exclusively by t_{CAC}.

(12) The t_{CRP} requirement should be applicable for $\overline{RAS}$/$\overline{CAS}$ cycles preceded by any cycle.

(13) Either t_{RRH} or t_{RCH} must be satisfied for a read cycle.

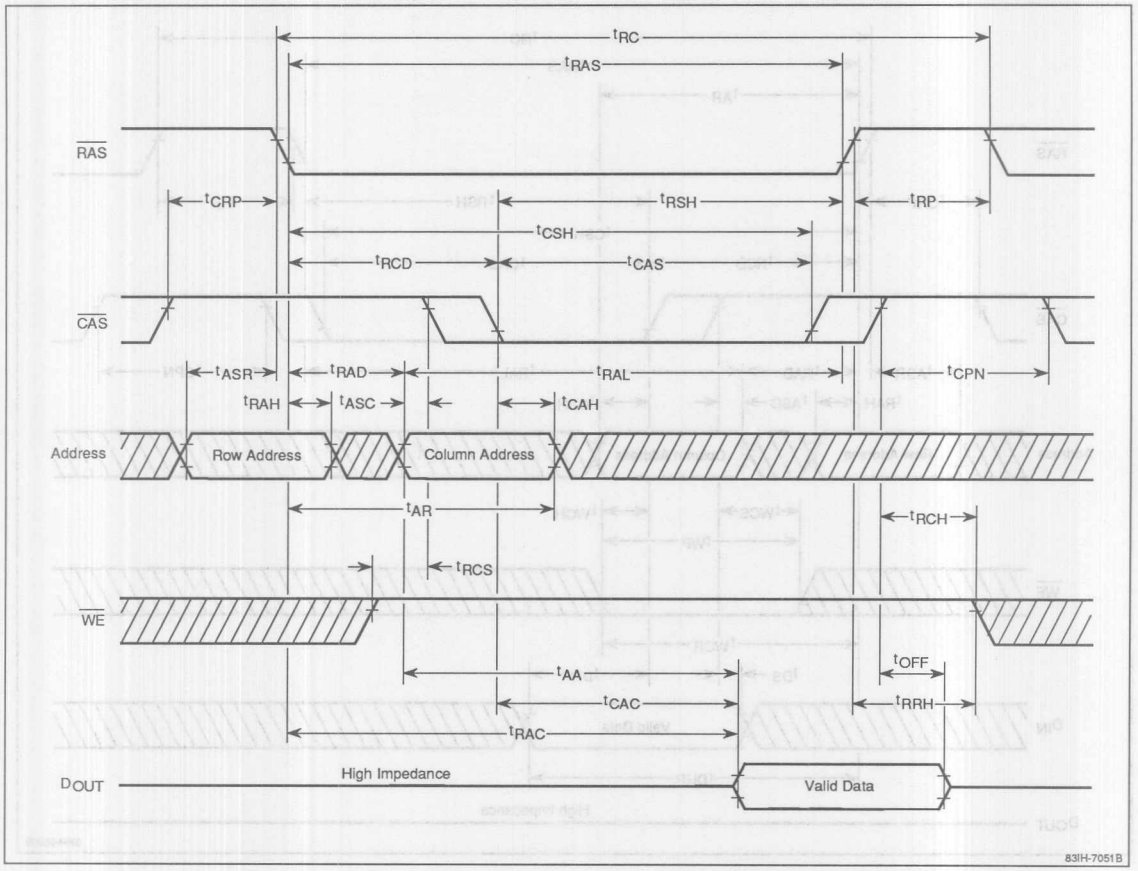
(14) Parameter t_{WP} is applicable for a delayed write cycle such as a read-write/read-modify-write cycle. For early write operation, both t_{WCS} and t_{WCH} must be met.

(15) These parameters are referenced to the falling edge of $\overline{CAS}$ for early write cycles and to the falling edge of $\overline{WE}$ for delayed write or read-modify-write cycles.

(16) t_{WCS}, t_{RWD}, t_{CWD}, and t_{AWD} are restrictive operating parameters in read-write/read-modify-write cycles only. If $t_{WCS} \geq t_{WCS}$ (min), the cycle is an early write cycle and the data output will remain open-circuit throughout the entire cycle. If $t_{CWD} \geq t_{CWD}$ (min), $t_{RWD} \geq t_{RWD}$ (min), and $t_{AWD} \geq t_{AWD}$ (min), the cycle is a read-write cycle and the data output will contain data read from the selected cell. If neither of the above conditions is met, the condition of the data output pin (at access time and until $\overline{CAS}$ returns to V_{IH}) is indeterminate.

Timing Waveforms

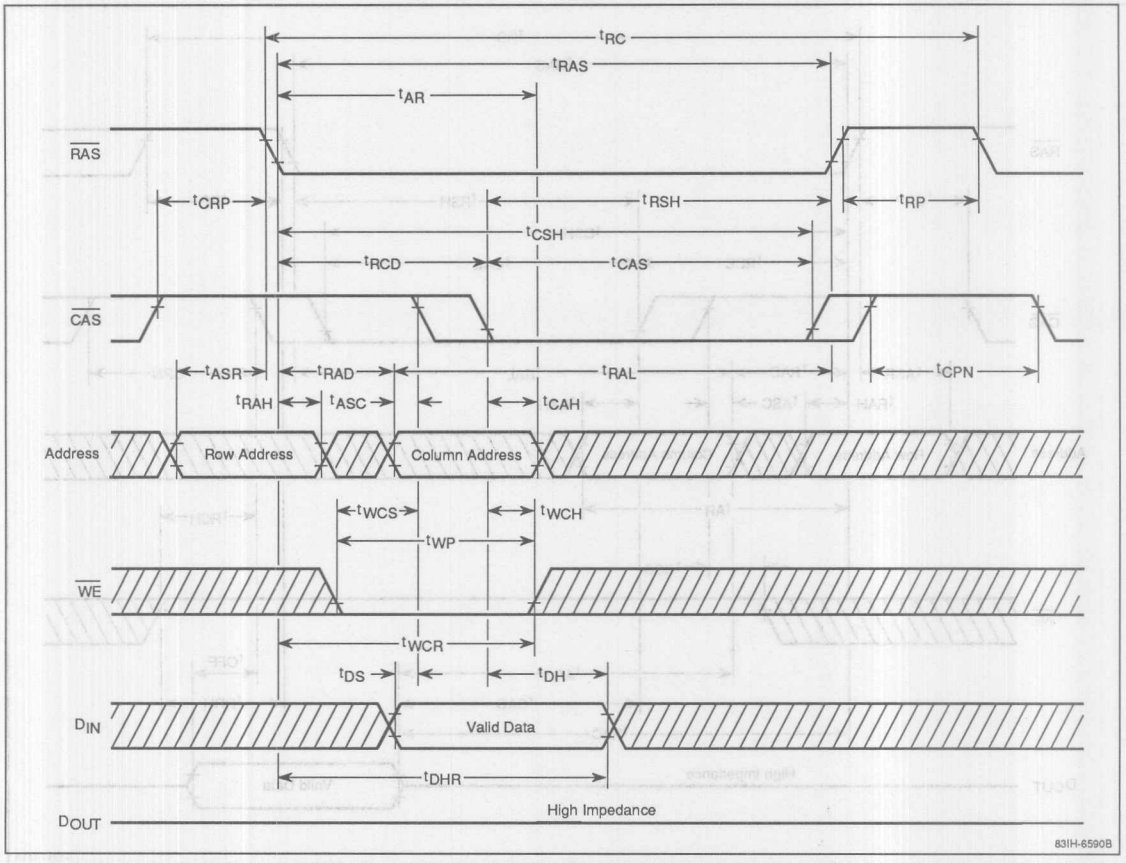
Read Cycle



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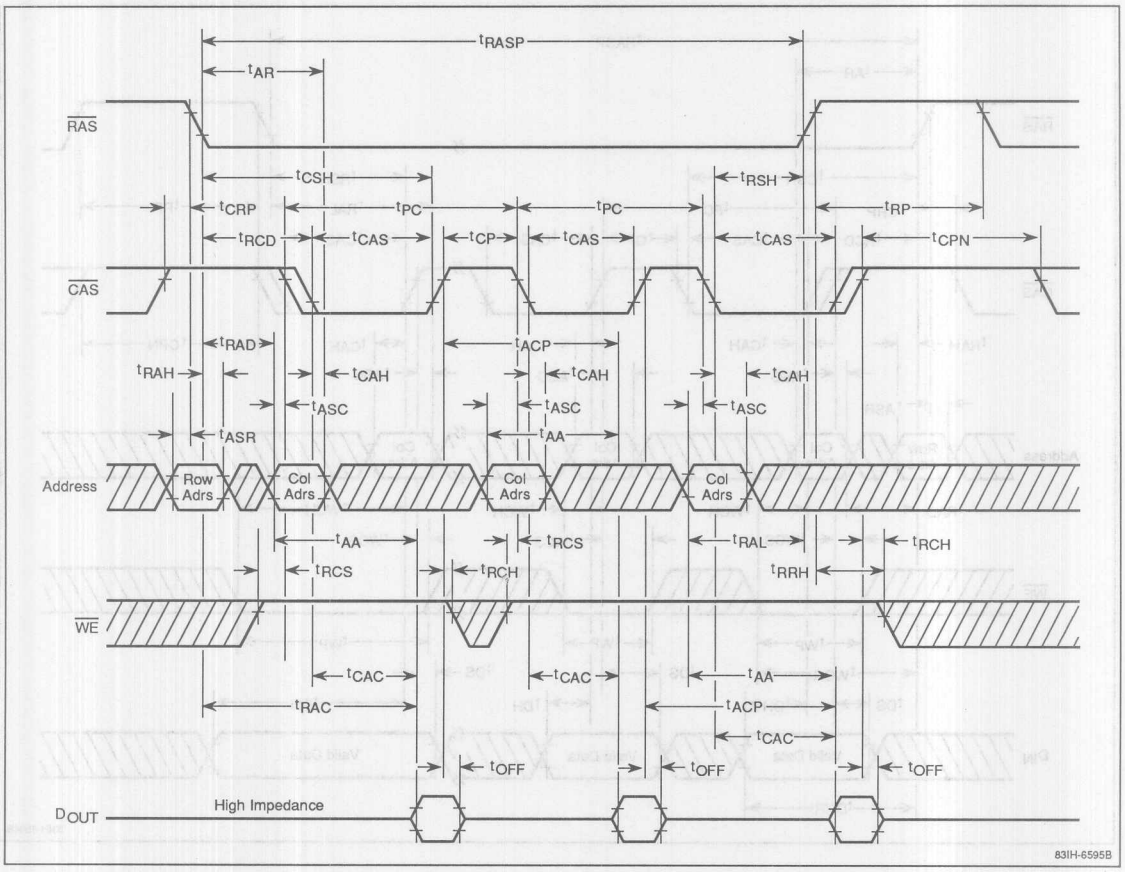
Timing Waveforms (cont)

Early Write Cycle



Timing Waveforms (cont)

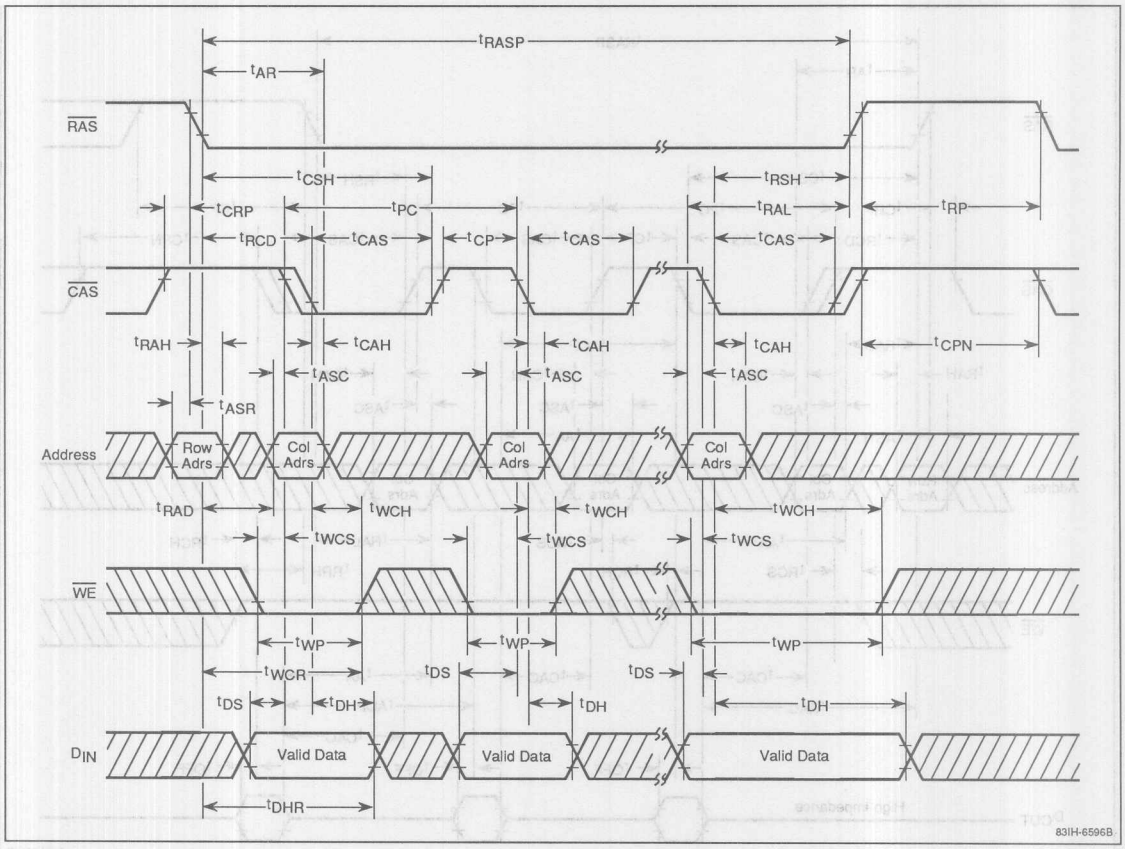
Fast-Page Read Cycle



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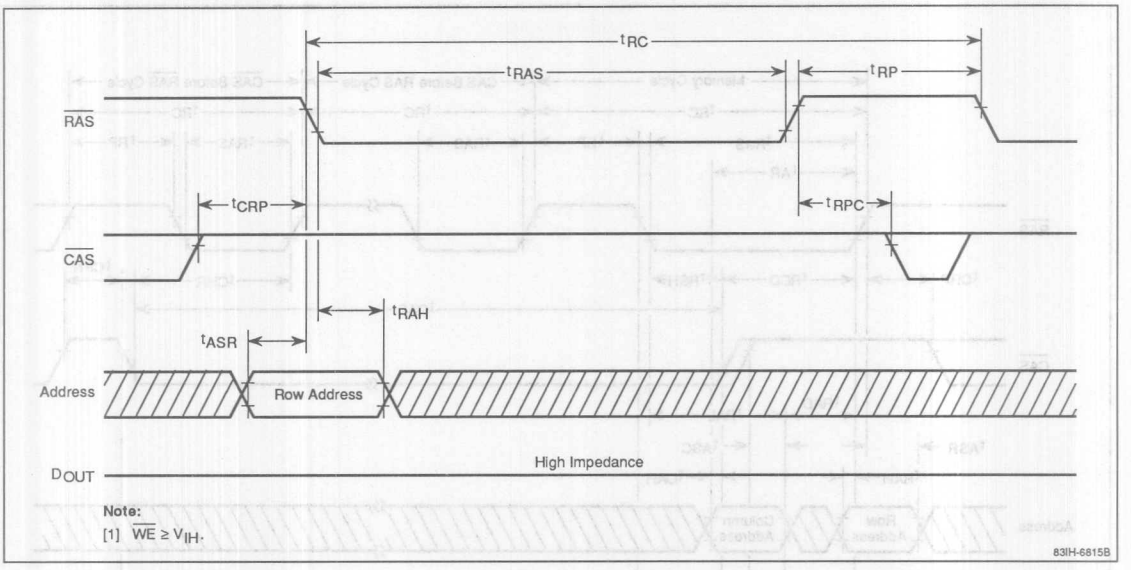
Timing Waveforms (cont)

Fast-Page Early Write Cycle



Timing Waveforms (cont)

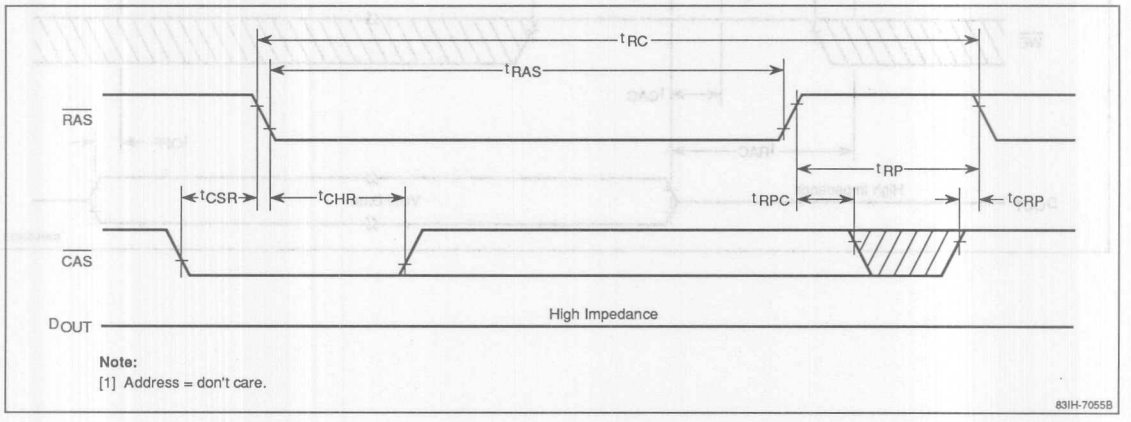
$\overline{RAS}$-Only Refresh Cycle



Note:
[1] $\overline{WE} \geq V_{IH}$.

83IH-6815B

$\overline{CAS}$ Before $\overline{RAS}$ Refresh Cycle



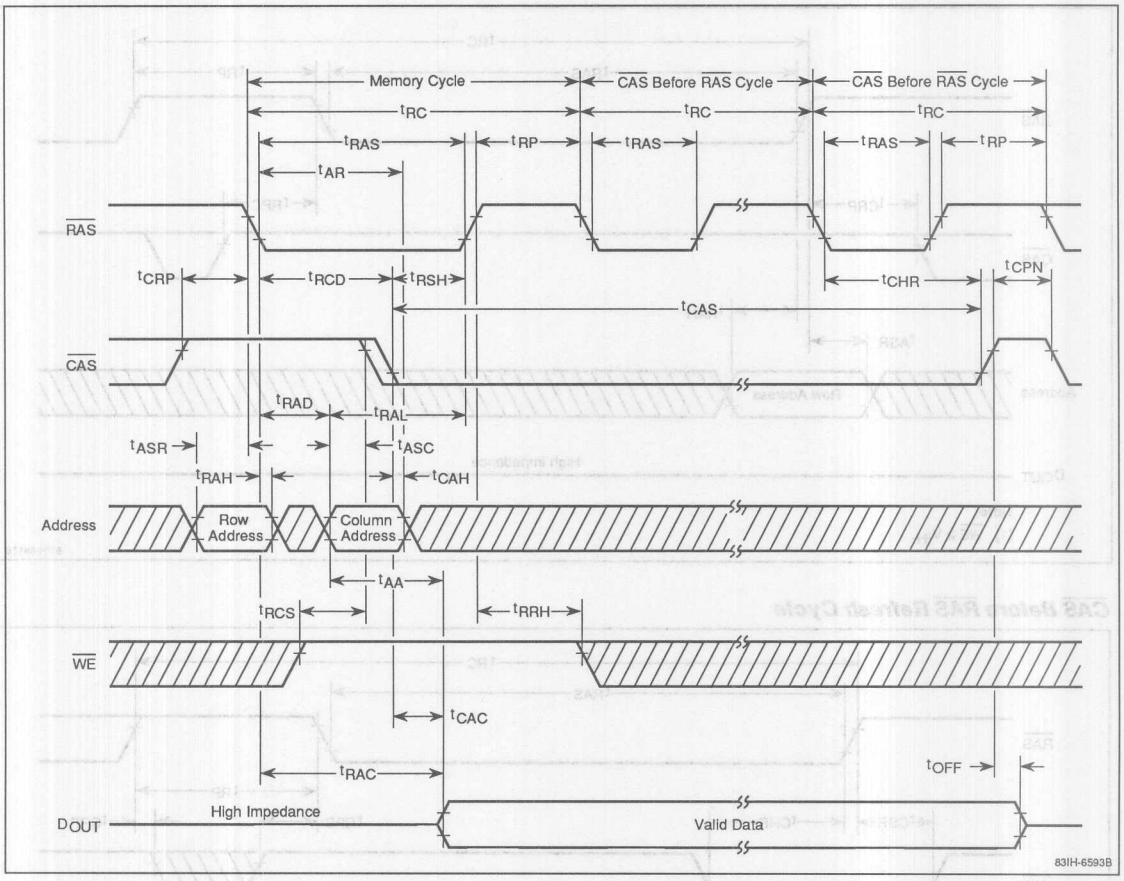
Note:
[1] Address = don't care.

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Timing Waveforms (cont)

Hidden Refresh Cycle



NEC Electronics Inc.

MC-421000A36
1,048,576 x 36-Bit
Dynamic CMOS RAM Module

Description

The MC-421000A36 is a fast-page dynamic RAM module organized as 1,048,576 words by 36 bits and designed to operate from a single +5-volt power supply. Advanced CMOS circuitry ensures minimum power dissipation and excellent operating margins.

The three-state output is controlled by $\overline{CAS}$ independent of $\overline{RAS}$. After a valid read or read-modify-write cycle, data is held on the output by holding $\overline{CAS}$ low. Data output is returned to high impedance by returning $\overline{CAS}$ high. Fast-page read and write cycles can be executed by cycling $\overline{CAS}$. Refreshing is accomplished by means of $\overline{RAS}$-only refresh cycles, $\overline{CAS}$ before $\overline{RAS}$ refresh cycles, hidden refresh cycles, or by the 1024 address combinations of A_0 through A_9 during a 16-ms period.

Single Inline Memory Module (SIMM™) packaging enhances reliability and reduces the size, weight and cost of a system. Each SIMM contains eight 1,048,576 x 4-bit μPD424400s in SOJ packages, four 1,048,576 x 1-bit μPD421000s in SOJ packages, and twelve power supply decoupling capacitors for noise reduction. DQ_0 through DQ_{35} are common input/output pins.

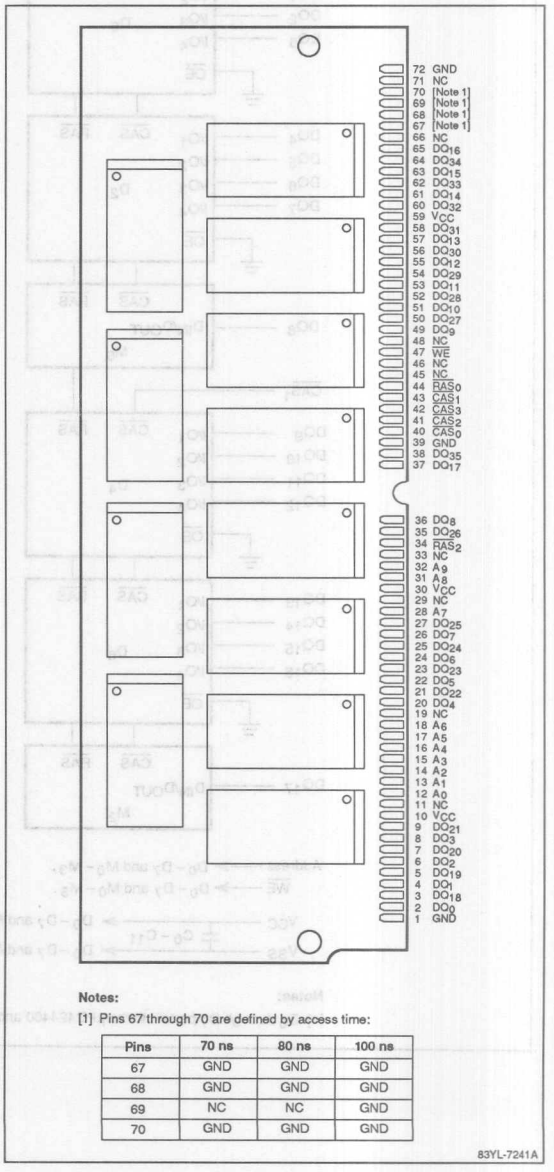
Features

- 1,048,576-word by 36-bit organization
- Single +5 V power supply
- Fast-page option
- Low power dissipation
- $\overline{RAS}$-only refresh cycles
- $\overline{CAS}$ before $\overline{RAS}$ refresh cycles
- Hidden refresh cycles
- 1024 refresh cycles every 16 ms
- TTL-compatible inputs and outputs
- 72-pin SIMM packaging

SIMM is a trademark of Wang Laboratories.

Pin Configuration

72-Pin SIMM



Notes:

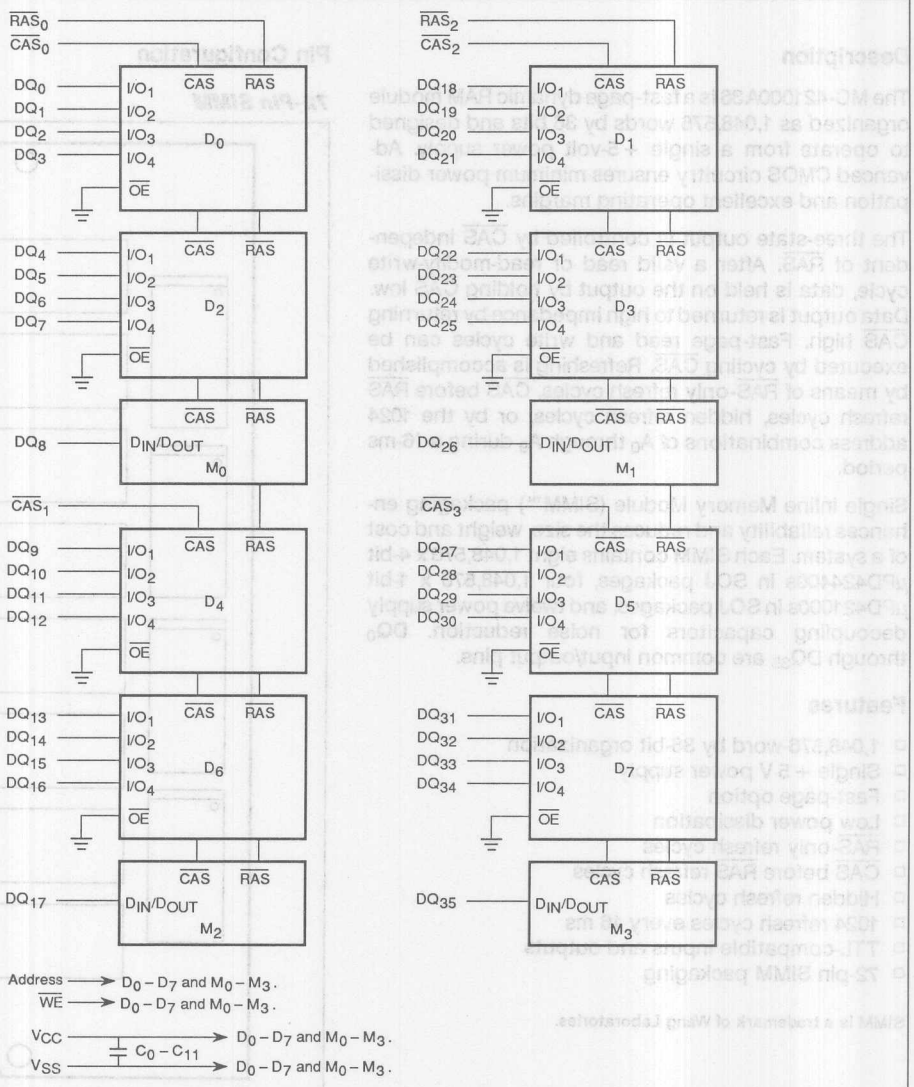
[1] Pins 67 through 70 are defined by access time:

Pins	70 ns	80 ns	100 ns
67	GND	GND	GND
68	GND	GND	GND
69	NC	NC	GND
70	GND	GND	GND

83YL-7241A

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Block Diagram



Notes:

[1] D_0 through D_7 pertain to the μPD424400 and M_0 through M_3 to the μPD421000.

83YL-7242B

Pin Identification

Name	Function
A_0 - A_9	Address inputs
$\overline{CAS}_0$ - $\overline{CAS}_3$	Column address strobe
DQ_0 - DQ_{35}	Common data inputs/outputs
$\overline{RAS}_0$ - $\overline{RAS}_2$	Row address strobe
$\overline{WE}$	Write enable
GND	Ground
V_{CC}	+5-volt power supply
NC	No connection

Absolute Maximum Ratings

Voltage on any pin relative to GND	−1.0 to +7.0 V
Operating temperature, T_{OPR}	0 to +70°C
Storage temperature, T_{STG}	−55 to +125°C
Short-circuit output current, I_{OS}	50 mA
Power dissipation, P_D	12 W

Exposure to Absolute Maximum Ratings for extended periods may affect device reliability; exceeding the ratings could cause permanent damage. The device should be operated within the limits specified under DC and AC Characteristics.

Recommended Operating Conditions

Parameter	Symbol	Min	Typ	Max	Unit
Input voltage, high	V_{IH}	2.4		V_{CC} + 1.0	V
Input voltage, low	V_{IL}	−1.0		0.8	V
Supply voltage	V_{CC}	4.75	5.0	5.25	V
Ambient temperature	T_A	0		70	°C

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Capacitance

T_A = 25°C; f = 1 MHz

Parameter	Symbol	Max	Unit	Pins Under Test
Input capacitance	C_{I1}	88	pF	A_0 - A_9
	C_{I2}	104	pF	$\overline{WE}$
	C_{I3}	57	pF	$\overline{RAS}$
	C_{I4}	36	pF	$\overline{CAS}$
Input/output capacitance	C_{I0}/C_{O0}	17	pF	DQ_0 - DQ_7, DQ_9 - DQ_{16}, DQ_{18} - DQ_{25}, DQ_{27} - DQ_{34}
	C_{I2}/C_{O2}	22	pF	DQ_8, DQ_{17}, DQ_{26}, DQ_{35}

Ordering Information

Part Number	Row Access Time (max)	R/W Cycle Time (min)	Fast-Page Cycle (min)	Package
MC421000A36BH-70	70 ns	140 ns	45 ns	72-pin socket-mountable SIMM (solder plating)
BH-80	80 ns	160 ns	50 ns	
BH-10	100 ns	190 ns	60 ns	
MC421000A36FH-70	70 ns	140 ns	45 ns	72-pin socket-mountable SIMM (gold plating)
FH-80	80 ns	160 ns	50 ns	
FH-10	100 ns	190 ns	60 ns	

DC Characteristics

T_A = 0 to +70°C; V_{CC} = +5.0 V ±5%

Parameter	Symbol	Min	Max	Unit	Test Conditions
Standby current	I_{CC2}		24	mA	$\overline{RAS}$ = $\overline{CAS}$ ≥ V_{IH} (min)
			12	mA	$\overline{RAS}$ = $\overline{CAS}$ ≥ V_{CC} – 0.2 V
Input leakage current	$I_{I(L)}$	–120	120	μA	V_{IN} = 0 V to V_{CC}; all other pins not under test = 0 V
Output leakage current	$I_{O(L)}$	–10	10	μA	DQ_0 to DQ_{35} disabled; V_{OUT} = 0 V to V_{CC}
Output voltage, low	V_{OL}		0.4	V	I_{OL} = 4.2 mA
Output voltage, high	V_{OH}	2.4		V	I_{OH} = –5 mA

AC Characteristics

T_A = 0 to +70°C; V_{CC} = +5.0 V ±5%

		-70		-80		-10			
Parameter	Symbol	Min	Max	Min	Max	Min	Max	Unit	Test Conditions
Operating current, average	I_{CC1}		1120		1000		880	mA	$\overline{RAS}$ and $\overline{CAS}$ cycling; t_{RC} = t_{RC} min; I_O = 0 mA (Note 5)
Operating current, $\overline{RAS}$-only refresh cycle, average	I_{CC3}		1120		1000		880	mA	$\overline{RAS}$ cycling; $\overline{CAS}$ ≥ V_{IH}; t_{RC} = t_{RC} min; I_O = 0 mA (Note 5)
Operating current, fast-page cycle, average	I_{CC4}		920		800		680	mA	$\overline{RAS}$ ≤ V_{IL}; $\overline{CAS}$ cycling; t_{PC} = t_{PC} min; I_O = 0 mA (Note 5)
Operating current, $\overline{CAS}$ before $\overline{RAS}$ refresh cycle, average	I_{CC5}		1120		1000		880	mA	$\overline{RAS}$ cycling; $\overline{CAS}$ before $\overline{RAS}$; t_{RC} = t_{RC} min; I_O = 0 mA (Note 5)
Access time from column address	t_{AA}		35		45		55	ns	(Notes 7, 9)
Access time from $\overline{CAS}$ precharge (rising edge)	t_{ACP}		40		45		55	ns	(Notes 7, 9)
Column address setup time	t_{ASC}	0		0		0		ns	
Row address setup time	t_{ASR}	0		0		0		ns	
Access time from $\overline{CAS}$ (falling edge)	t_{CAC}		20		20		25	ns	(Notes 7, 9)
Column address hold time	t_{CAH}	17		20		20		ns	
$\overline{CAS}$ pulse width	t_{CAS}	20	10,000	20	10,000	25	10,000	ns	
$\overline{CAS}$ hold time for $\overline{CAS}$ before $\overline{RAS}$ refresh cycle	t_{CHR}	15		15		20		ns	
$\overline{CAS}$ to output in low impedance	t_{CLZ}	0		0		0		ns	(Note 7)
$\overline{CAS}$ precharge time, fast-page cycle	t_{CP}	10	20	10	20	10	25	ns	

AC Characteristics (cont)

Parameter	Symbol	-70 Min	-70 Max	-80 Min	-80 Max	-10 Min	-10 Max	Unit	Test Conditions
$\overline{CAS}$ precharge time, nonpage cycle	t_{CPN}	10		10		10		ns	
$\overline{CAS}$ to $\overline{RAS}$ precharge time	t_{CRP}	10		10		10		ns	(Note 12)
$\overline{CAS}$ hold time	t_{CSH}	70		80		100		ns	
$\overline{CAS}$ setup time for $\overline{CAS}$ before $\overline{RAS}$ refresh cycle	t_{CSR}	10		10		10		ns	
Data-in hold time	t_{DH}	15		20		20		ns	(Note 15)
Data-in setup time	t_{DS}	0		0		0		ns	(Note 15)
Output buffer turnoff delay	t_{OFF}	0	15	0	20	0	25	ns	(Note 10)
Fast-page cycle time	t_{PC}	45		50		60		ns	(Note 6)
Access time from $\overline{RAS}$	t_{RAC}		70		80		100	ns	(Notes 7, 8)
$\overline{RAS}$ to column address delay time	t_{RAD}	15	35	17	35	17	45	ns	(Note 9)
Row address hold time	t_{RAH}	10		12		12		ns	
Column address lead time referenced to $\overline{RAS}$ (rising edge)	t_{RAL}	35		45		55		ns	
$\overline{RAS}$ pulse width	t_{RAS}	70	10,000	80	10,000	100	10,000	ns	
$\overline{RAS}$ pulse width, fast-page cycle	t_{RASP}	70	100,000	80	100,000	100	100,000	ns	
Random read or write cycle time	t_{RC}	140		160		190		ns	(Note 6)
$\overline{RAS}$ to $\overline{CAS}$ delay time	t_{RCD}	20	60	25	60	25	75	ns	(Note 11)
Read command hold time referenced to $\overline{CAS}$	t_{RCH}	0		0		0		ns	(Note 13)
Read command setup time	t_{RCS}	0		0		0		ns	
Refresh period	t_{REF}		16		16		16	ms	Addresses A_0 - A_9
$\overline{RAS}$ precharge time	t_{RP}	60		70		80		ns	
$\overline{RAS}$ precharge $\overline{CAS}$ hold time	t_{RPC}	10		10		10		ns	
Read command hold time referenced to $\overline{RAS}$	t_{RRH}	10		10		10		ns	(Note 13)

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AC Characteristics (cont)

Parameter	Symbol	-70 Min	-70 Max	-80 Min	-80 Max	-10 Min	-10 Max	Unit	Test Conditions
$\overline{RAS}$ hold time	t_{RSH}	20		20		25		ns	
Rise and fall transition time	t_T	3	50	3	50	3	50	ns	(Note 3)
Write command hold time	t_{WCH}	15		15		20		ns	
Write command setup time	t_{WCS}	0		0		0		ns	(Note 16)
$\overline{WE}$ hold time	t_{WHR}	15		15		20		ns	
$\overline{WE}$ setup time	t_{WSR}	10		10		10		ns	
Write command pulse width	t_{WP}	15		15		20		ns	(Note 14)

Notes:

(1) All voltages are referenced to GND.

(2) An initial pause of 100 μs is required after power-up, followed by any eight $\overline{RAS}$ cycles, before proper device operation is achieved. At the end of the initial power-up sequence, it is recommended that either a $\overline{RAS}$-only refresh or a $\overline{CAS}$ before $\overline{RAS}$ refresh cycle be executed while $\overline{WE} \geq V_{IH}$ to ensure normal operation.

(3) AC measurements assume $t_T = 5$ ns.

(4) V_{IH} (min) and V_{IL} (max) are reference levels for measuring the timing of input signals. Transition times are measured between V_{IH} and V_{IL}.

(5) I_{CC1}, I_{CC3}, I_{CC4}, and I_{CC5} depend on output loading and cycle rates. Specified values are obtained with the output open. I_{CC3} is measured assuming that all column address inputs are held at either a high level or a low level during $\overline{RAS}$-only refresh cycles. I_{CC4} is measured assuming that all column address inputs are switched only once during each fast-page cycle.

(6) The minimum specifications are used only to indicate the cycle time at which proper operation over the full temperature range (T_A = 0 to +70°C) is assured.

(7) Load = 2 TTL (–1 mA, +4 mA) loads and 100 pF (V_{OH} = 2.0 V, V_{OL} = 0.8 V).

(8) Assumes that $t_{RCD} \leq t_{RCD}$ (max) and $t_{RAD} \leq t_{RAD}$ (max). If t_{RCD} or t_{RAD} is greater than the maximum recommended value in this table, t_{RAC} increases by the amount that t_{RCD} or t_{RAD} exceeds the value shown.

(9) If $t_{RAD} \geq t_{RAD}$ (max), then the access time is defined by t_{AA}.

(10) t_{OFF} (max) defines the time at which the output achieves the open-circuit condition an is not referenced to V_{OH} or V_{OL}.

(11) Operation within the t_{RCD} (max) limit assures that t_{RAC} (max) can be met. t_{RCD} (max) is specified as a reference point only; if t_{RCD} is greater than t_{RCD} (max), then access time is controlled exclusively by t_{CAC}.

(12) The t_{CRP} requirement should be applicable for $\overline{RAS}$/$\overline{CAS}$ cycles preceded by any cycle.

(13) Either t_{RRH} or t_{RCH} must be satisfied for a read cycle.

(14) Parameter t_{WP} is applicable for a delayed write cycle such as a read-write/read-modify-write cycle. For early write operation, both t_{WCS} and t_{WCH} must be met.

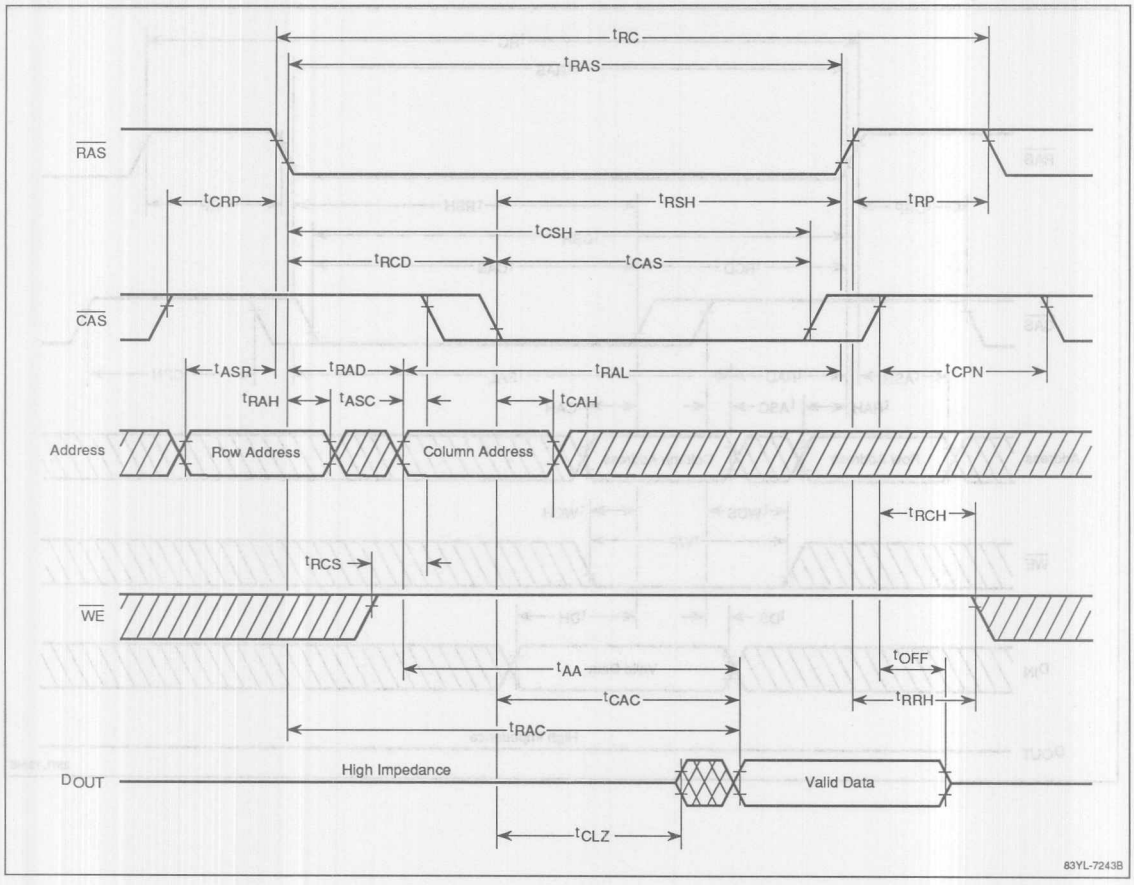
(15) These parameters are referenced to the falling edge of $\overline{CAS}$ for early write cycles and to the falling edge of $\overline{WE}$ for delayed write or read-modify-write cycles.

(16) t_{WCS}, t_{RWD}, t_{CWD}, and t_{AWD} are restrictive operating parameters in read-write/read-modify-write cycles only. If $t_{WCS} \geq t_{WCS}$ (min), the cycle is an early write cycle and the data output will remain open-circuit throughout the entire cycle. If $t_{CWD} \geq t_{CWD}$ (min), $t_{RWD} \geq t_{RWD}$ (min), and $t_{AWD} \geq t_{AWD}$ (min), the cycle is a read-write cycle and the data output will contain data read from the selected cell. If neither of the above conditions is met, the condition of the data output pin (at access time and until $\overline{CAS}$ returns to V_{IH}) is indeterminate.

(17) A test mode may be initiated by executing a $\overline{CAS}$ before $\overline{RAS}$ refresh cycle with $\overline{WE}$ held at V_{IL}. This mode also may inadvertently be initiated during power-up because external control of the signal lines is very difficult during this period. It is therefore recommended that while $\overline{WE}$ is held at V_{IH}, either a $\overline{RAS}$-only or $\overline{CAS}$ before $\overline{RAS}$ refresh cycle should be executed at any time after the end of the initial power-up sequence to ensure normal device operation.

Timing Waveforms

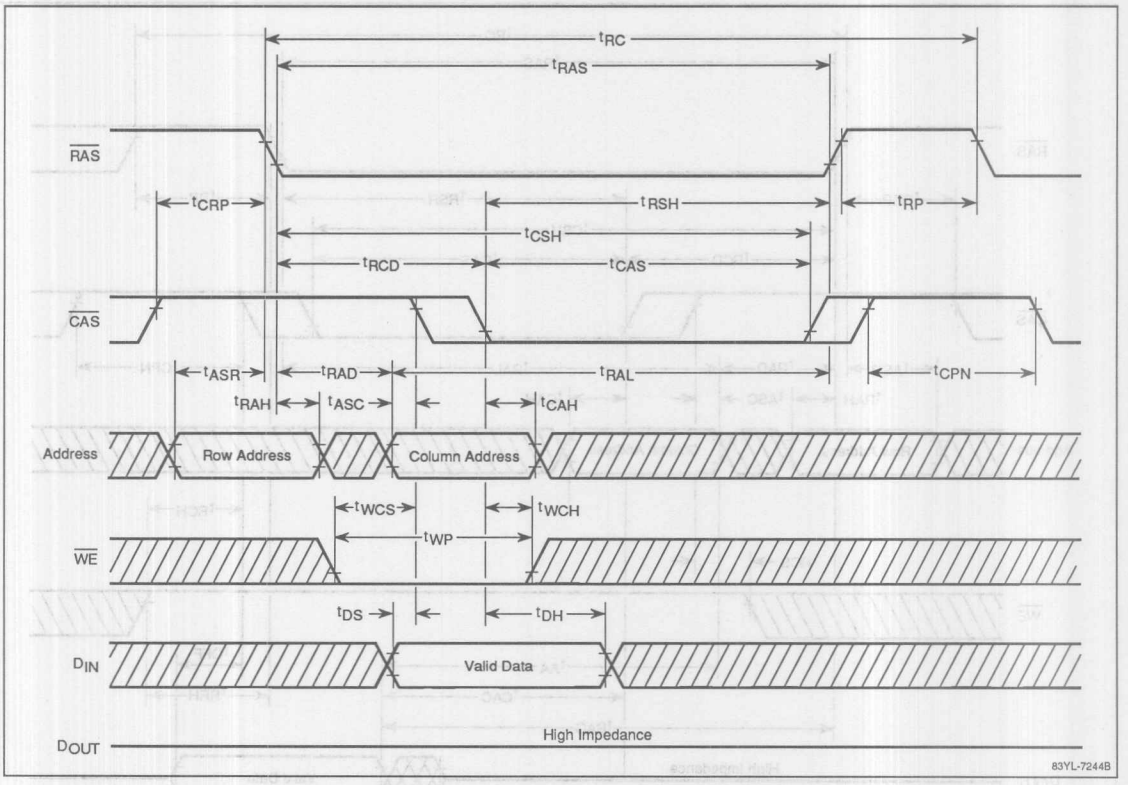
Read Cycle



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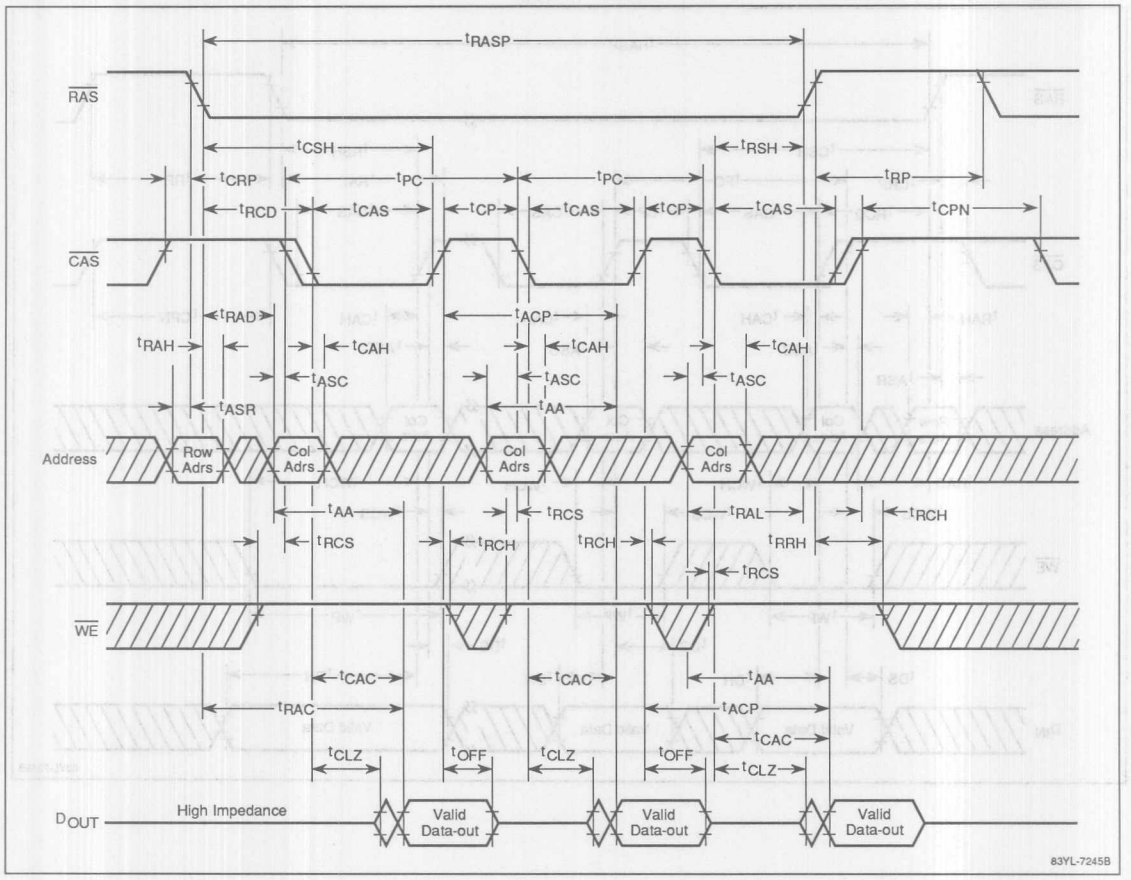
Timing Waveforms (cont)

Early Write Cycle



Timing Waveforms (cont)

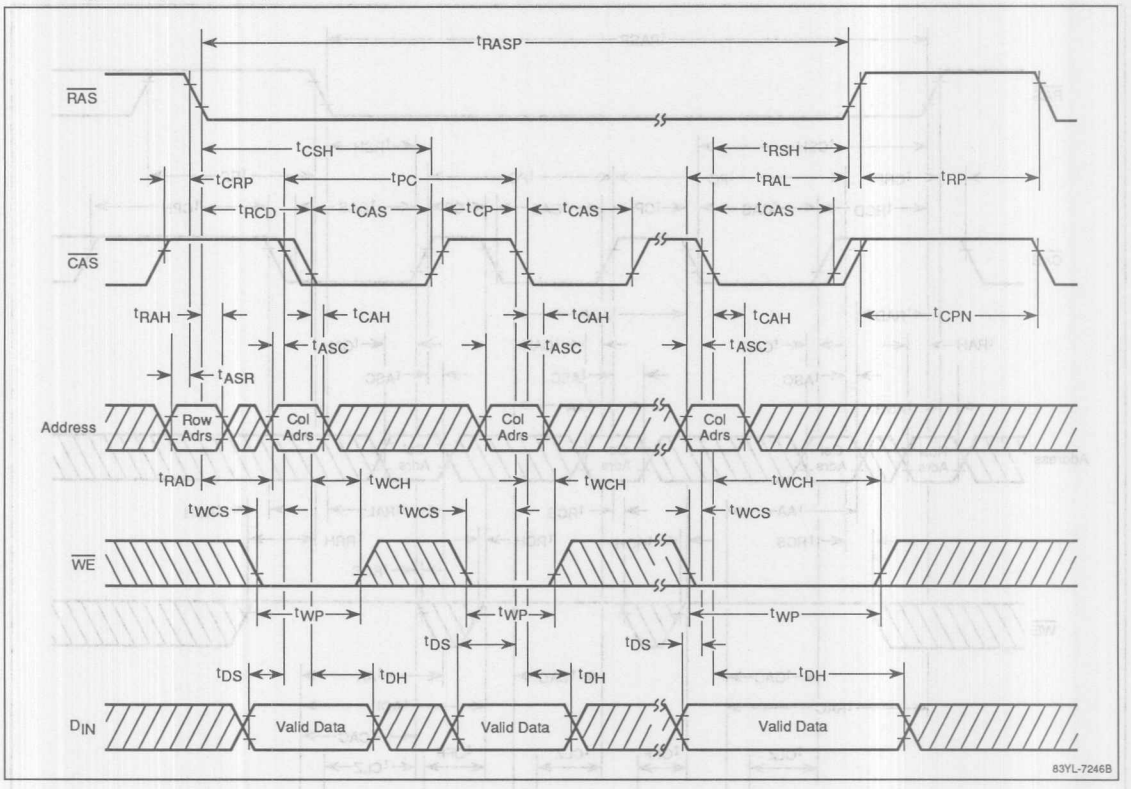
Fast-Page Read Cycle



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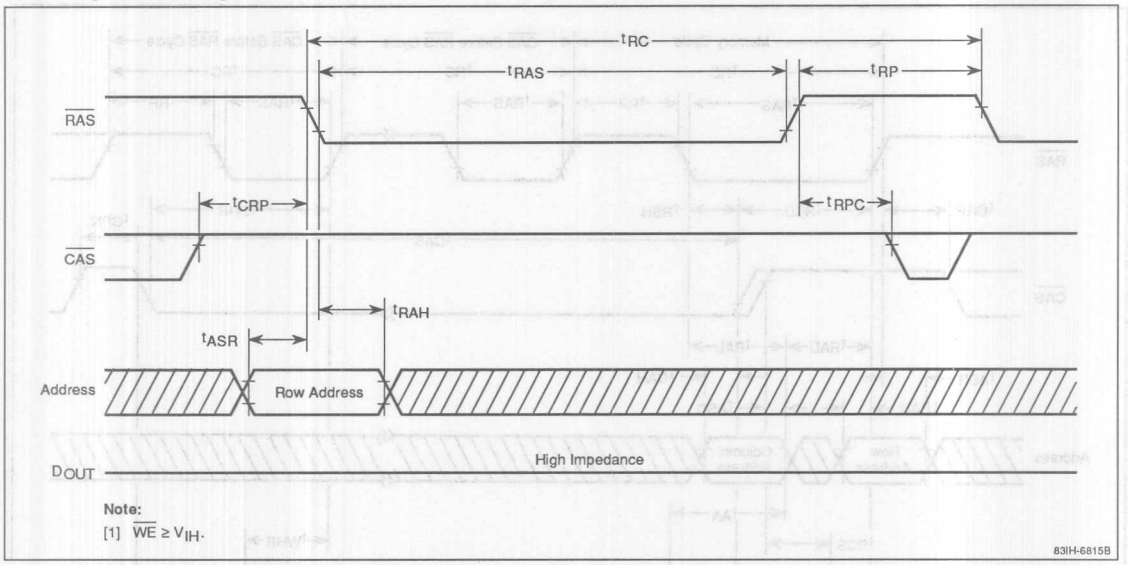
Timing Waveforms (cont)

Fast-Page Early Write Cycle



Timing Waveforms (cont)

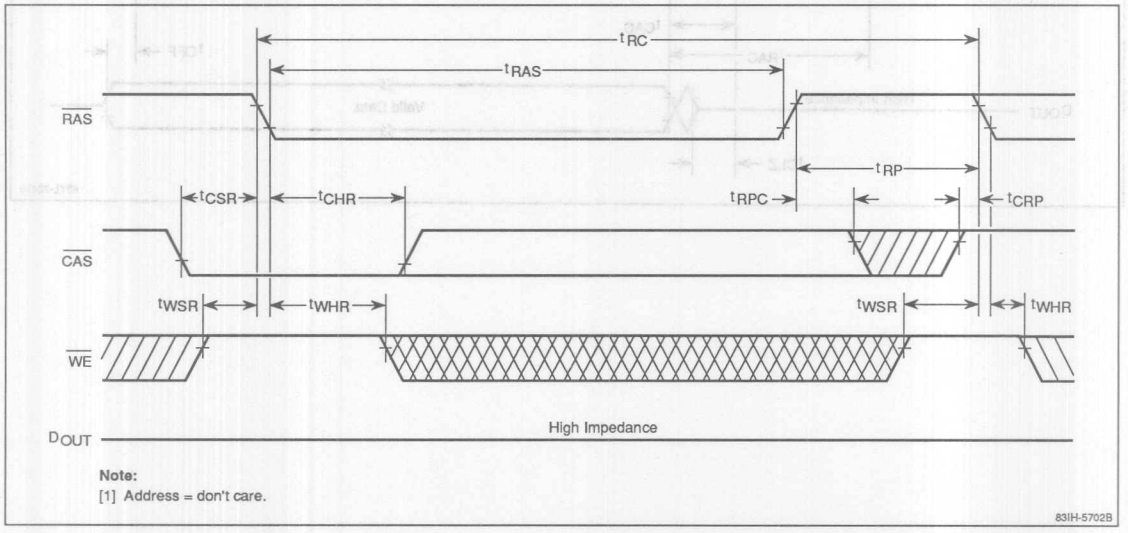
$\overline{RAS}$-Only Refresh Cycle



Note:
[1] $\overline{WE} \geq V_{IH}$.

83IH-6815B

$\overline{CAS}$ Before $\overline{RAS}$ Refresh Cycle



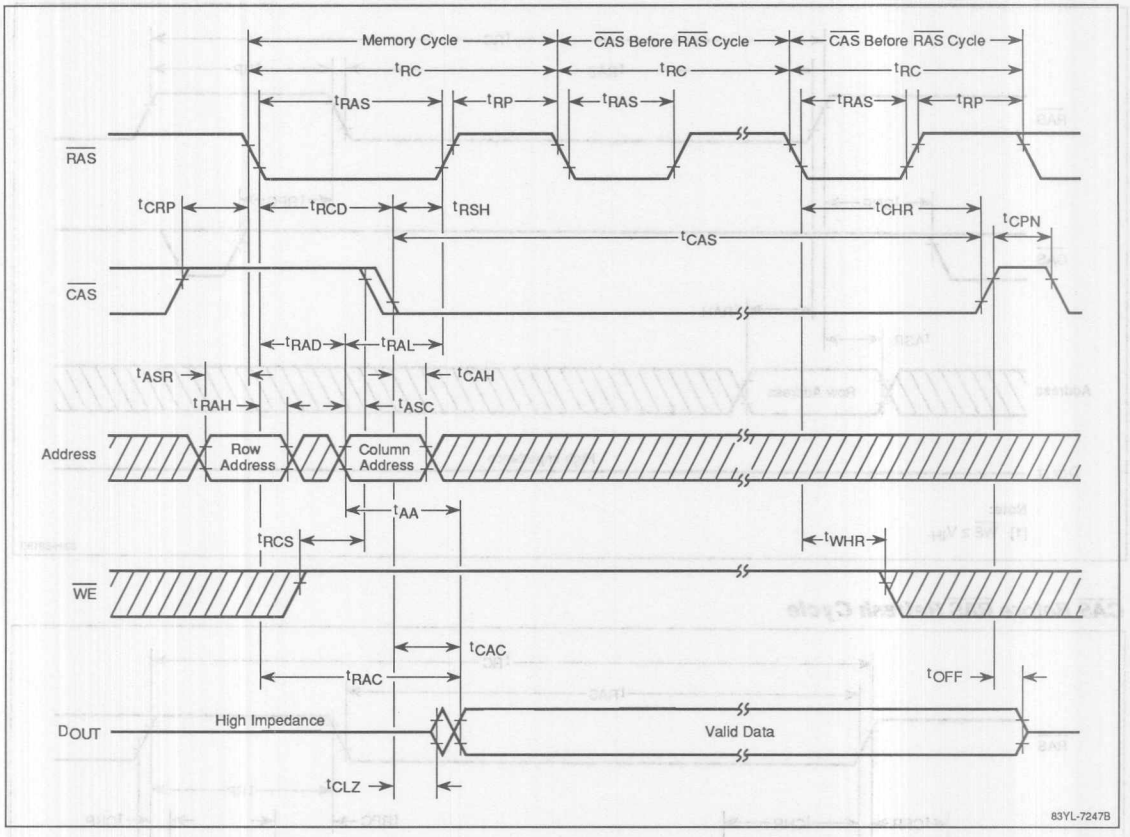
Note:
[1] Address = don't care.

83IH-5702B

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Timing Waveforms (cont)

Hidden Refresh Cycle



NEC Electronics Inc.

MC-422000A36BH/FH
2,097,152 x 36-Bit
Dynamic CMOS RAM Module

Description

The MC-422000A36BH/FH is a fast-page dynamic RAM module organized as 2,097,152 words by 36 bits and designed to operate from a single + 5-volt power supply. Advanced CMOS circuitry ensures minimum power dissipation and excellent operating margins.

The three-state output is controlled by $\overline{CAS}$ independent of $\overline{RAS}$. After a valid read or read-modify-write cycle, data is held on the output by holding $\overline{CAS}$ low. Data output is returned to high impedance by returning $\overline{CAS}$ high. Fast-page read and write cycles can be executed by cycling $\overline{CAS}$. Refreshing is accomplished by means of $\overline{RAS}$-only refresh cycles, $\overline{CAS}$ before $\overline{RAS}$ refresh cycles, hidden refresh cycles, or by the 1024 address combinations of A_0 through A_9 during a 16-ms period.

Single Inline Memory Module (SIMM™) packaging enhances reliability and reduces the size, weight and cost of a system. Each SIMM contains sixteen 1,048,576 x 4-bit μPD424400s in SOJ packages, eight 1,048,576 x 1-bit μPD421000s in SOJ packages, and twenty-four power supply decoupling capacitors for noise reduction. DQ_0 through DQ_{35} are common input/output pins.

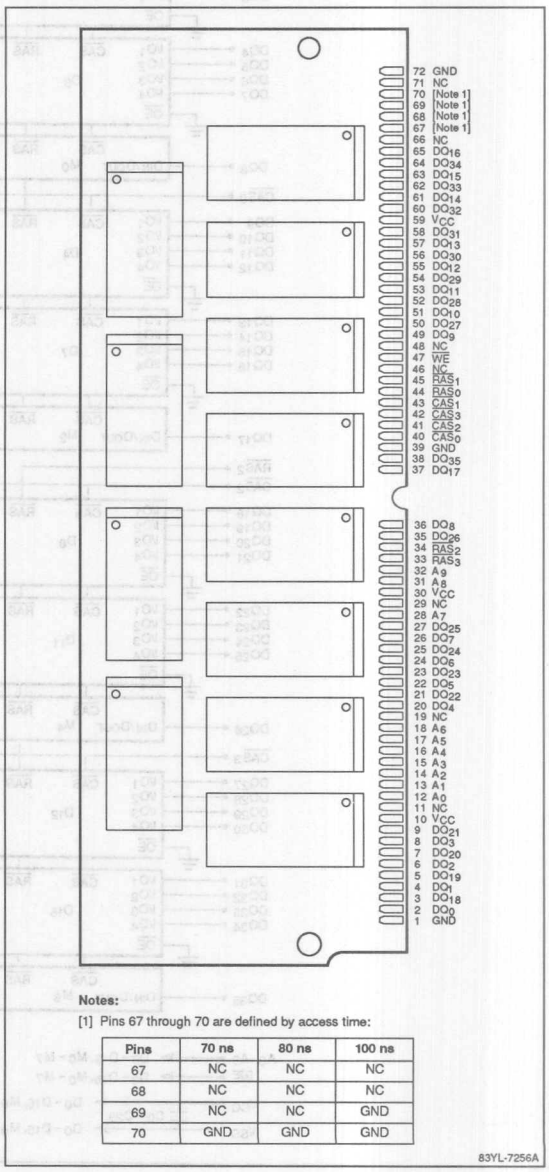
Features

- 2,097,152-word by 36-bit organization
- Single + 5 V ±5% power supply
- Fast-page cycles
- Low power dissipation
- $\overline{RAS}$-only refresh cycles
- $\overline{CAS}$ before $\overline{RAS}$ refresh cycles
- Hidden refresh cycles
- 1024 refresh cycles every 16 ms
- TTL-compatible inputs and outputs
- 72-pin SIMM packaging

SIMM is a trademark of Wang Laboratories.

Pin Configuration

72-Pin SIMM



Notes:

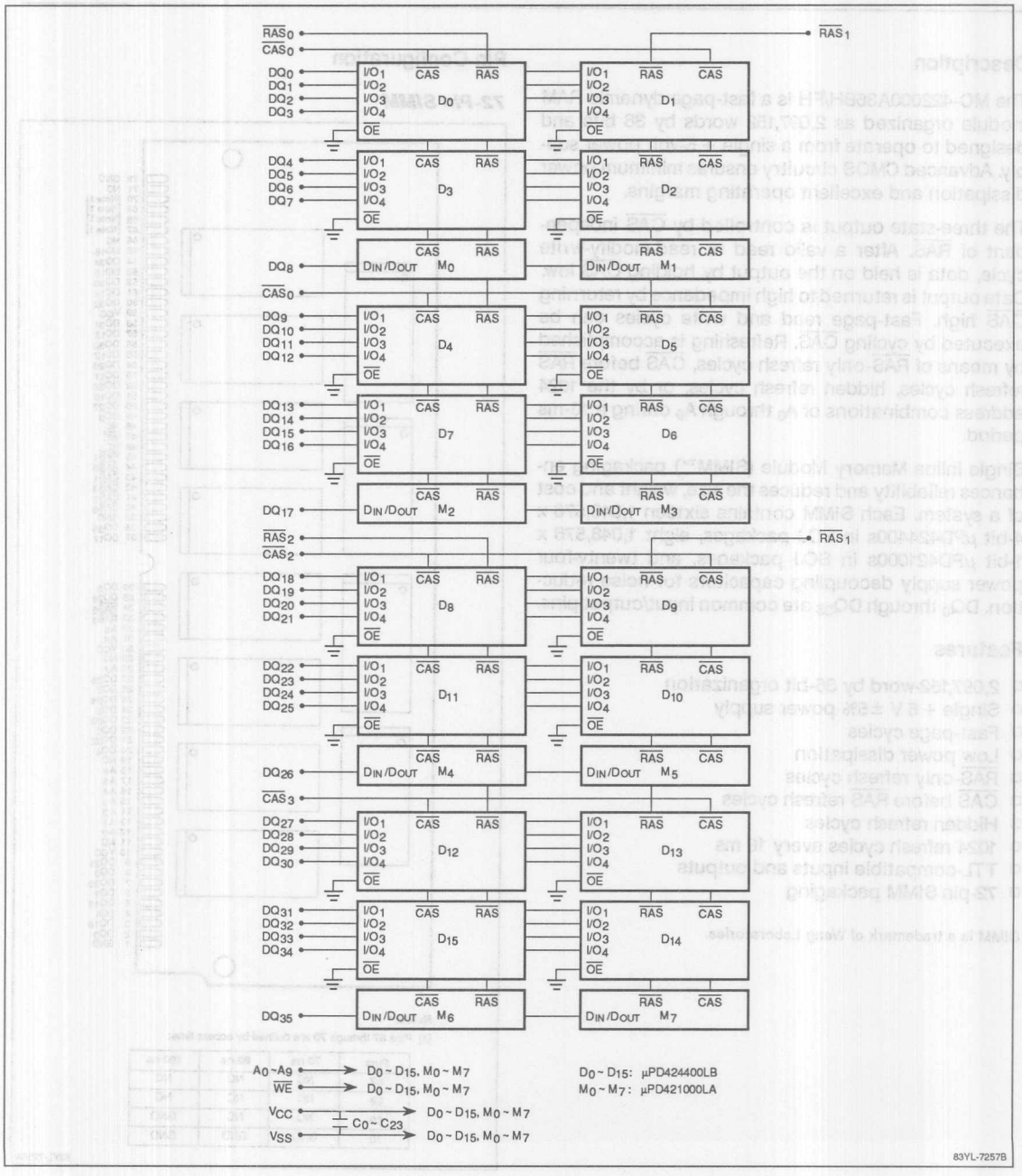
[1] Pins 67 through 70 are defined by access time:

Pins	70 ns	80 ns	100 ns
67	NC	NC	NC
68	NC	NC	NC
69	NC	NC	GND
70	GND	GND	GND

83YL-7256A

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Block Diagram



Pin Identification

Name	Function
A_0 - A_8	Address inputs
$\overline{CAS}_0$ - $\overline{CAS}_3$	Column address strobe
DQ_0 - DQ_{35}	Common data inputs/outputs
$\overline{RAS}_0$ - $\overline{RAS}_2$	Row address strobe
$\overline{WE}$	Write enable
GND	Ground
V_{CC}	+5-volt power supply
NC	No connection

Absolute Maximum Ratings

Voltage on any pin relative to GND	−1.0 to +7.0 V
Operating temperature, T_{OPR}	0 to +70°C
Storage temperature, T_{STG}	−55 to +125°C
Short-circuit output current, I_{OS}	50 mA
Power dissipation, P_D	24 W

Exposure to Absolute Maximum Ratings for extended periods may affect device reliability; exceeding the ratings could cause permanent damage. The device should be operated within the limits specified under DC and AC Characteristics.

Recommended Operating Conditions

Parameter	Symbol	Min	Typ	Max	Unit
Input voltage, high	V_{IH}	2.4		V_{CC} + 1.0	V
Input voltage, low	V_{IL}	−1.0		0.8	V
Supply voltage	V_{CC}	4.75	5.0	5.25	V
Ambient temperature	T_A	0		70	°C

Capacitance

T_A = 25°C; f = 1 MHz

Parameter	Symbol	Max	Unit	Pins Under Test
Input capacitance	C_{I1}	161	pF	A_0 - A_9
	C_{I2}	193	pF	$\overline{WE}$
	C_{I3}	62	pF	$\overline{RAS}$
	C_{I4}	62	pF	$\overline{CAS}$
Input/output capacitance	C_{IO}/C_{OO}	29	pF	DQ_0 - DQ_7, DQ_9 - DQ_{16}, DQ_{18} - DQ_{25}, DQ_{27} - DQ_{34}
	C_{I2}/C_{O2}	39	pF	DQ_8, DQ_{17}, DQ_{26}, DQ_{35}

Ordering Information

Part Number	Row Access Time (max)	R/W Cycle Time (min)	Fast-Page Cycle (min)	Package
MC422000A36BH-70	70 ns	140 ns	45 ns	72-pin socket-mountable SIMM (solder plating)
BH-80	80 ns	160 ns	50 ns	
BH-10	100 ns	190 ns	60 ns	
MC422000A36FH-70	70 ns	140 ns	45 ns	72-pin socket-mountable SIMM (gold plating)
FH-80	80 ns	160 ns	50 ns	
FH-10	100 ns	190 ns	60 ns	

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DC Characteristics

T_A = 0 to +70°C; V_{CC} = +5.0 V ±5%

Parameter	Symbol	Min	Max	Unit	Test Conditions
Standby current	I_{CC2}		48	mA	$\overline{RAS}$ = $\overline{CAS}$ ≥ V_{IH} (min)
			24	mA	$\overline{RAS}$ = $\overline{CAS}$ ≥ V_{CC} – 0.2 V
Input leakage current	$I_{I(L)}$	240	240	μA	V_{IN} = 0 V to V_{CC}; all other pins not under test = 0 V
Output leakage current	$I_{O(L)}$	–10	10	μA	DQ_0 to DQ_{35} disabled; V_{OUT} = 0 V to V_{CC}
Output voltage, low	V_{OL}		0.4	V	I_{OL} = 4.2 mA
Output voltage, high	V_{OH}	2.4		V	I_{OH} = –5 mA

AC Characteristics

T_A = 0 to +70°C; V_{CC} = +5.0 V ±5%

		-70		-80		-10			
Parameter	Symbol	Min	Max	Min	Max	Min	Max	Unit	Test Conditions
Operating current, average	I_{CC1}		1180		1060		940	mA	$\overline{RAS}$ and $\overline{CAS}$ cycling; t_{RC} = t_{RC} min; I_O = 0 mA (Note 5)
Operating current, $\overline{RAS}$-only refresh cycle, average	I_{CC3}		1180		1060		940	mA	$\overline{RAS}$ cycling; $\overline{CAS}$ ≥ V_{IH}; t_{RC} = t_{RC} min; I_O = 0 mA (Note 5)
Operating current, fast-page cycle, average	I_{CC4}		980		860		740	mA	$\overline{RAS}$ ≤ V_{IL}; $\overline{CAS}$ cycling; t_{PC} = t_{PC} min; I_O = 0 mA (Note 5)
Operating current, $\overline{CAS}$ before $\overline{RAS}$ refresh cycle, average	I_{CC5}		1180		1060		940	mA	$\overline{RAS}$ cycling; $\overline{CAS}$ before $\overline{RAS}$; t_{RC} = t_{RC} min; I_O = 0 mA (Note 5)
Access time from column address	t_{AA}		35		45		55	ns	(Notes 7, 9)
Access time from $\overline{CAS}$ precharge (rising edge)	t_{ACP}		40		45		55	ns	(Notes 7, 9)
Column address setup time	t_{ASC}	0		0		0		ns	
Row address setup time	t_{ASR}	0		0		0		ns	
Access time from $\overline{CAS}$ (falling edge)	t_{CAC}		20		20		25	ns	(Notes 7, 9)
Column address hold time	t_{CAH}	17		20		20		ns	
$\overline{CAS}$ pulse width	t_{CAS}	20	10,000	20	10,000	25	10,000	ns	
$\overline{CAS}$ hold time for $\overline{CAS}$ before $\overline{RAS}$ refresh cycle	t_{CHR}	15		15		20		ns	
Data setup time	t_{CLZ}	0		0		0		ns	
$\overline{CAS}$ precharge time, fast-page cycle	t_{CP}	10	20	10	20	10	25	ns	

AC Characteristics (cont)

Parameter	Symbol	-70 Min	-70 Max	-80 Min	-80 Max	-10 Min	-10 Max	Unit	Test Conditions
$\overline{CAS}$ precharge time, nonpage cycle	t_{CPN}	10		10		10		ns	
$\overline{CAS}$ to $\overline{RAS}$ precharge time	t_{CRP}	10		10		10		ns	(Note 12)
$\overline{CAS}$ hold time	t_{CSH}	70		80		100		ns	
$\overline{CAS}$ setup time for $\overline{CAS}$ before $\overline{RAS}$ refresh cycle	t_{CSR}	10		10		10		ns	
Data-in hold time	t_{DH}	15		20		20		ns	(Note 15)
Data-in setup time	t_{DS}	0		0		0		ns	(Note 15)
Output buffer turnoff delay	t_{OFF}	0	15	0	20	0	25	ns	(Note 10)
Fast-page cycle time	t_{PC}	45		50		60		ns	(Note 6)
Access time from $\overline{RAS}$	t_{RAC}		70		80		100	ns	(Notes 7, 8)
$\overline{RAS}$ to column address delay time	t_{RAD}	15	35	17	35	17	45	ns	(Note 9)
Row address hold time	t_{RAH}	10		12		12		ns	
Column address lead time referenced to $\overline{RAS}$ (rising edge)	t_{RAL}	35		45		55		ns	
$\overline{RAS}$ pulse width	t_{RAS}	70	10,000	80	10,000	100	10,000	ns	
$\overline{RAS}$ pulse width, fast-page cycle	t_{RASP}	70	100,000	80	100,000	100	100,000	ns	
Random read or write cycle time	t_{RC}	130		160		190		ns	(Note 6)
$\overline{RAS}$ to $\overline{CAS}$ delay time	t_{RCD}	20	60	25	60	25	75	ns	(Note 11)
Read command hold time referenced to $\overline{CAS}$	t_{RCH}	0		0		0		ns	(Note 13)
Read command setup time	t_{RCS}	0		0		0		ns	
Refresh period	t_{REF}		8		8		8	ms	Addresses A_0 - A_9
$\overline{RAS}$ precharge time	t_{RP}	60		70		80		ns	
$\overline{RAS}$ precharge $\overline{CAS}$ hold time	t_{RPC}	10		10		10		ns	
Read command hold time referenced to $\overline{RAS}$	t_{RRH}	10		10		10		ns	(Note 13)
$\overline{RAS}$ hold time	t_{RSH}	20		20		25		ns	

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AC Characteristics (cont)

Parameter	Symbol	-70 Min	-70 Max	-80 Min	-80 Max	-10 Min	-10 Max	Unit	Test Conditions
Rise and fall transition time	t_T	3	50	3	50	3	50	ns	(Note 3)
Write command hold time	t_{WCH}	15		15		20		ns	
Write command setup time	t_{WCS}	0		0		0		ns	(Note 16)
$\overline{WE}$ hold time	t_{WHR}	15		15		20		ns	
$\overline{WE}$ setup time	t_{WSR}	10		10		10		ns	
Write command pulse width	t_{WP}	15		15		20		ns	(Note 14)

Notes:

(1) All voltages are referenced to GND.

(2) An initial pause of 100 μs is required after power-up, followed by any eight $\overline{RAS}$ cycles, before proper device operation is achieved. At the end of the initial power-up sequence, it is recommended that either a $\overline{RAS}$-only refresh or a $\overline{CAS}$ before $\overline{RAS}$ refresh cycle be executed while $\overline{WE} \geq V_{IH}$ to ensure normal operation.

(3) AC measurements assume $t_T = 5$ ns.

(4) V_{IH} (min) and V_{IL} (max) are reference levels for measuring the timing of input signals. Transition times are measured between V_{IH} and V_{IL}.

(5) I_{CC1}, I_{CC3}, I_{CC4}, and I_{CC5} depend on output loading and cycle rates. Specified values are obtained with the output open. I_{CC3} is measured assuming that all column address inputs are held at either a high level or a low level during $\overline{RAS}$-only refresh cycles. I_{CC4} is measured assuming that all column address inputs are switched only once during each fast-page cycle.

(6) The minimum specifications are used only to indicate the cycle time at which proper operation over the full temperature range (T_A = 0 to +70°C) is assured.

(7) Load = 2 TTL (–1 mA, +4 mA) loads and 100 pF (V_{OH} = 2.0 V, V_{OL} = 0.8 V).

(8) Assumes that $t_{RCD} \leq t_{RCD}$ (max) and $t_{RAD} \leq t_{RAD}$ (max). If t_{RCD} or t_{RAD} is greater than the maximum recommended value in this table, t_{RAC} increases by the amount that t_{RCD} or t_{RAD} exceeds the value shown.

(9) If $t_{RAD} \geq t_{RAD}$ (max), then the access time is defined by t_{AA}.

(10) t_{OFF} (max) defines the time at which the output achieves the open-circuit condition an is not referenced to V_{OH} or V_{OL}.

(11) Operation within the t_{RCD} (max) limit assures that t_{RAC} (max) can be met. t_{RCD} (max) is specified as a reference point only; if t_{RCD} is greater than t_{RCD} (max), then access time is controlled exclusively by t_{CAC}.

(12) The t_{CRP} requirement should be applicable for $\overline{RAS}/\overline{CAS}$ cycles preceded by any cycle.

(13) Either t_{RRH} or t_{RCH} must be satisfied for a read cycle.

(14) Parameter t_{WP} is applicable for a delayed write cycle such as a read-write/read-modify-write cycle. For early write operation, both t_{WCS} and t_{WCH} must be met.

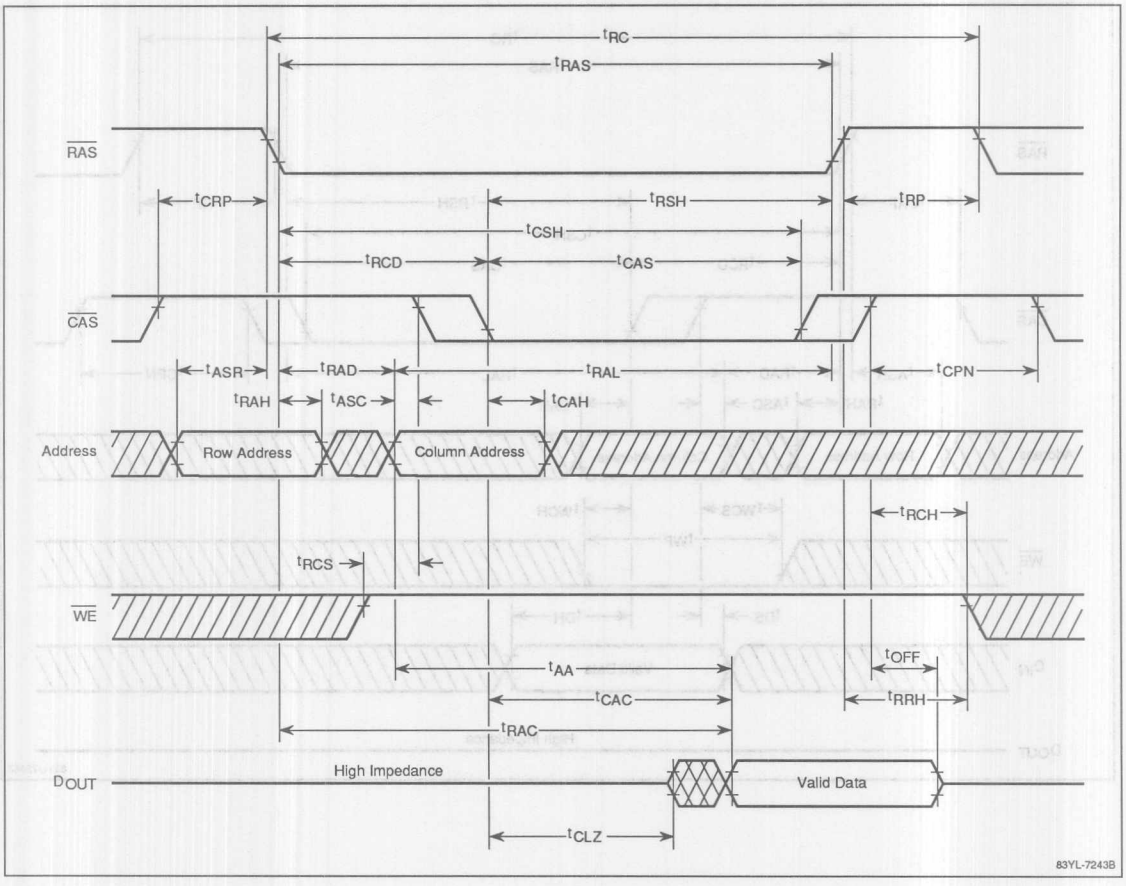
(15) These parameters are referenced to the falling edge of $\overline{CAS}$ for early write cycles and to the falling edge of $\overline{WE}$ for delayed write or read-modify-write cycles.

(16) t_{WCS}, t_{RWD}, t_{CWD}, and t_{AWD} are restrictive operating parameters in read-write/read-modify-write cycles only. If $t_{WCS} \geq t_{WCS}$ (min), the cycle is an early write cycle and the data output will remain open-circuit throughout the entire cycle. If $t_{CWD} \geq t_{CWD}$ (min), $t_{RWD} \geq t_{RWD}$ (min), and $t_{AWD} \geq t_{AWD}$ (min), the cycle is a read-write cycle and the data output will contain data read from the selected cell. If neither of the above conditions is met, the condition of the data output pin (at access time and until $\overline{CAS}$ returns to V_{IH}) is indeterminate.

(17) A test mode may be initiated by executing a $\overline{CAS}$ before $\overline{RAS}$ refresh cycle with $\overline{WE}$ held at V_{IL}. This mode also may inadvertently be initiated during power-up because external control of the signal lines is very difficult during this period. It is therefore recommended that while $\overline{WE}$ is held at V_{IH}, either a $\overline{RAS}$-only or $\overline{CAS}$ before $\overline{RAS}$ refresh cycle should be executed at any time after the end of the initial power-up sequence to ensure normal device operation.

Timing Waveforms

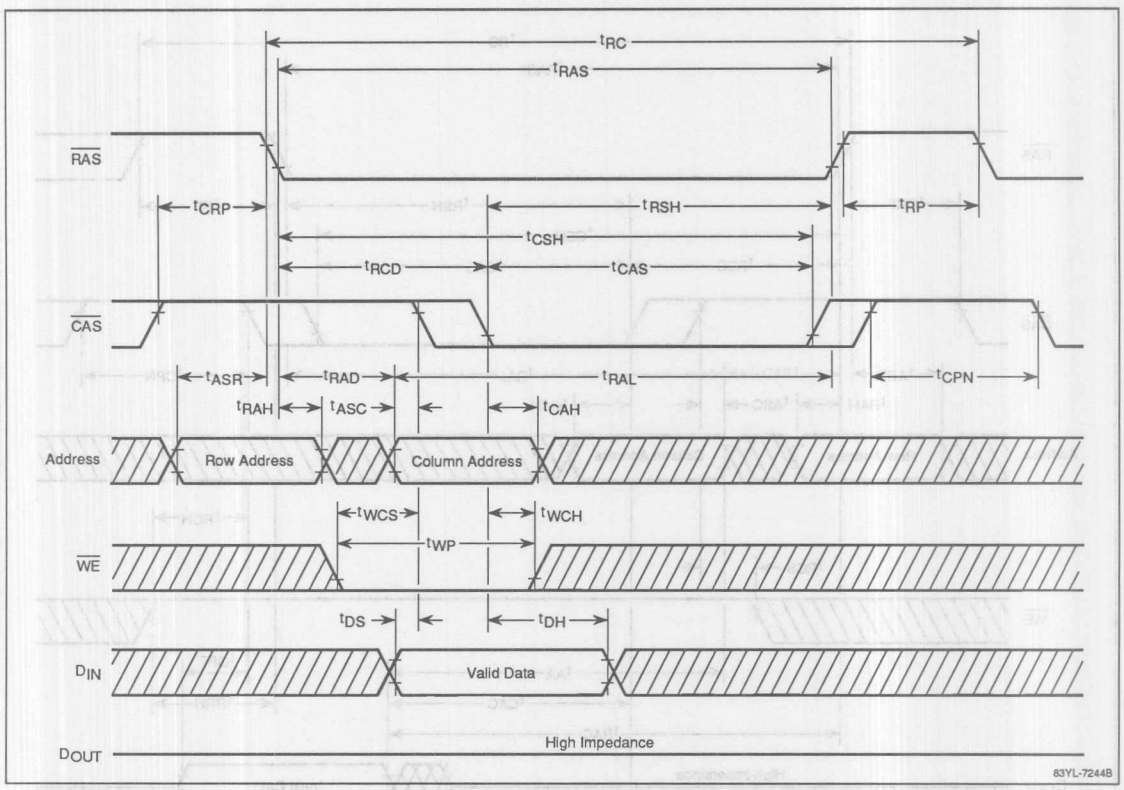
Read Cycle



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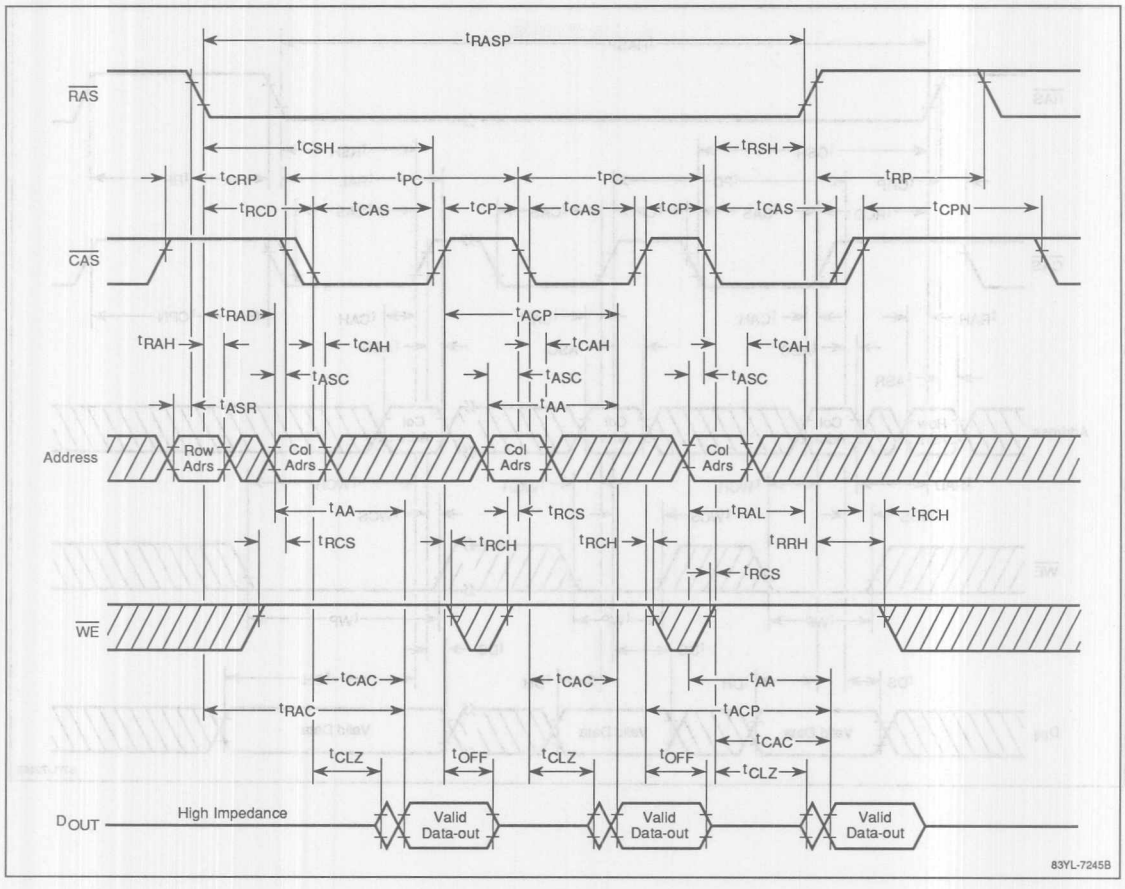
Timing Waveforms (cont)

Early Write Cycle



Timing Waveforms (cont)

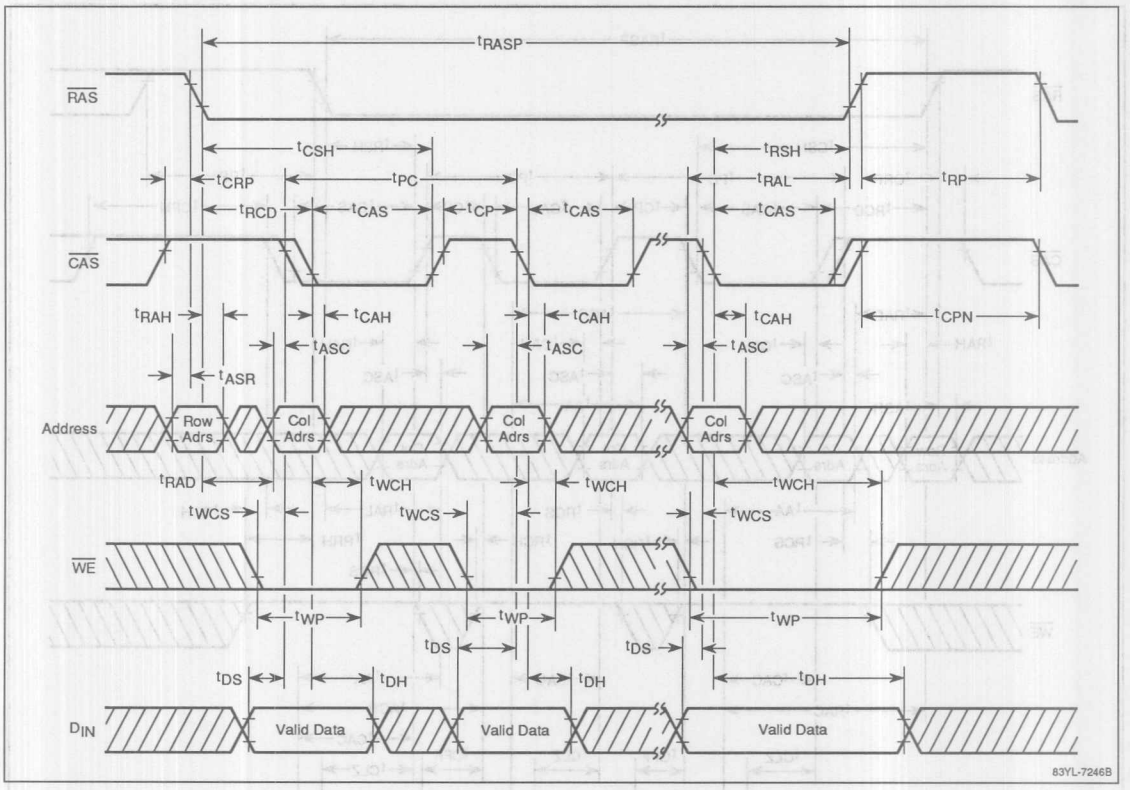
Fast-Page Read Cycle



5

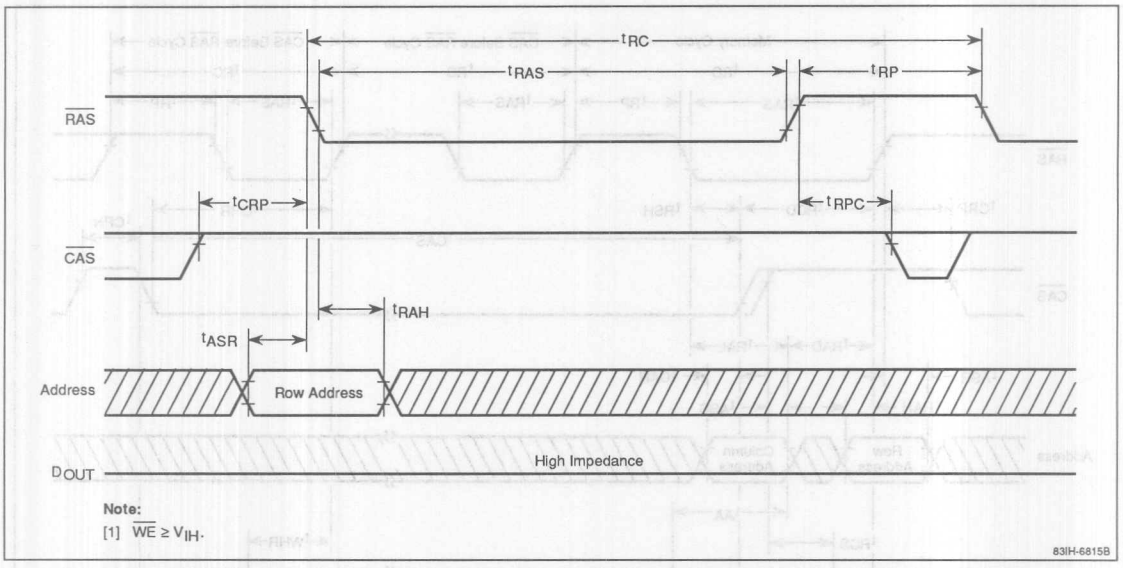
Timing Waveforms (cont)

Fast-Page Early Write Cycle



Timing Waveforms (cont)

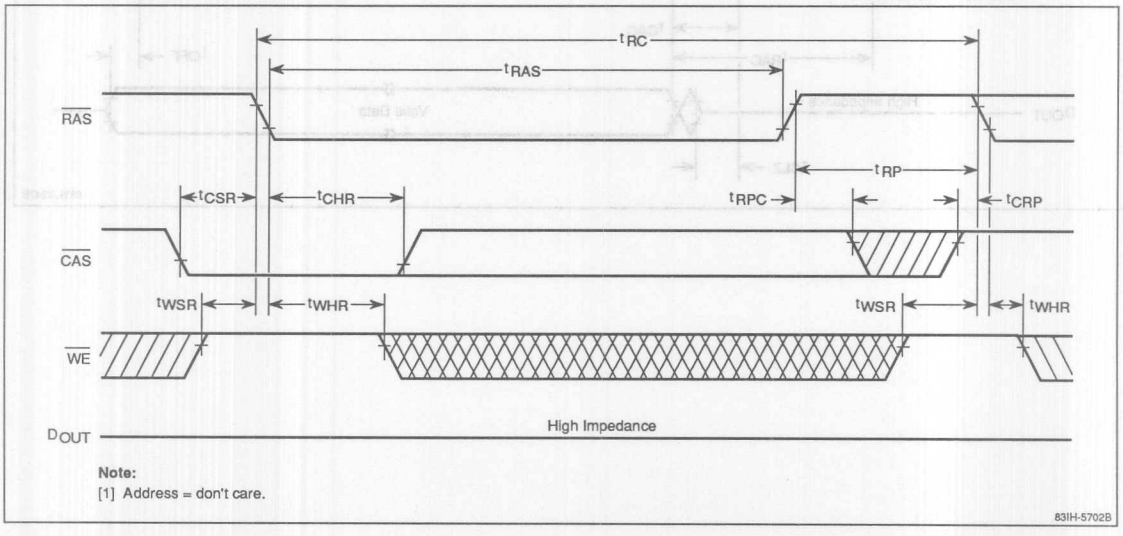
$\overline{RAS}$-Only Refresh Cycle



Note:
[1] $\overline{WE} \geq V_{IH}$.

83IH-6815B

$\overline{CAS}$ Before $\overline{RAS}$ Refresh Cycle



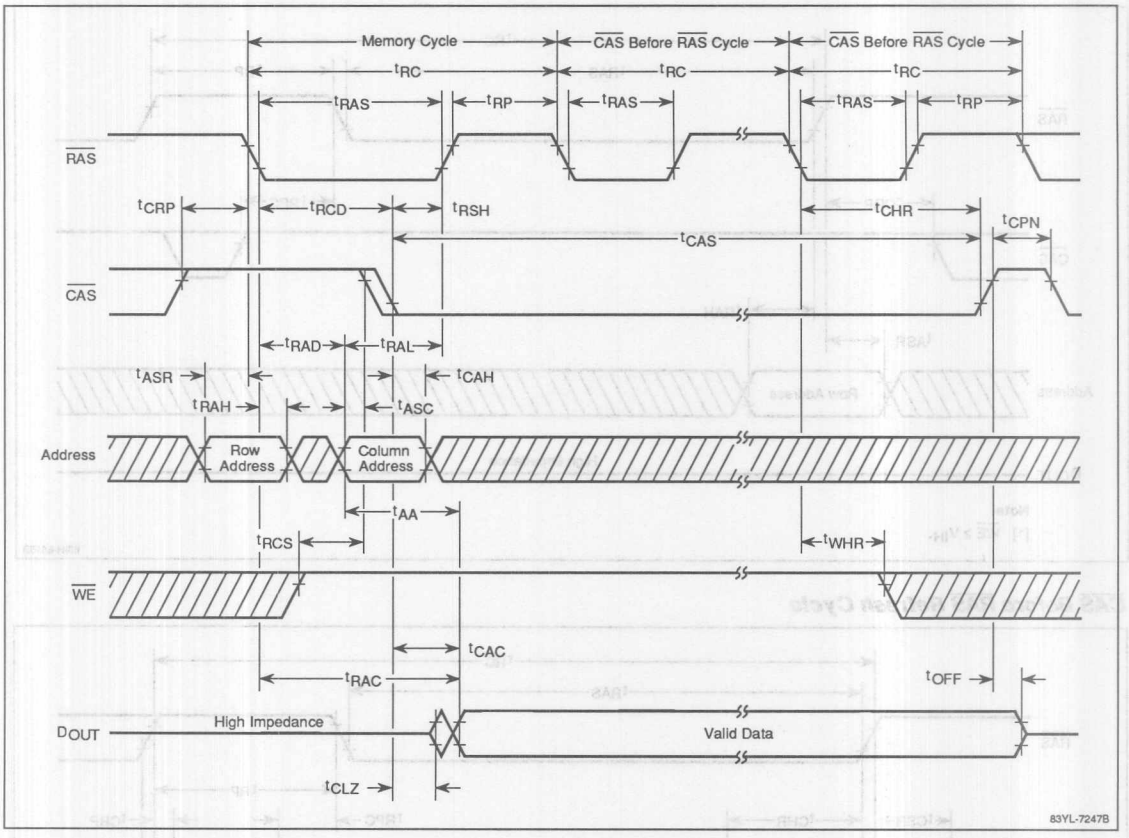
Note:
[1] Address = don't care.

83IH-5702B

5

Timing Waveforms (cont)

Hidden Refresh Cycle



NEC

Dynamic RAMs

6

Section 6
Dynamic RAMs

μPD41256 6-1
262,144 x 1-Bit Dynamic CMOS RAM

μPD41464 6-19
65,536 x 4-Bit Dynamic NMOS RAM

μPD421000 6-39
1,048,576 x 1-Bit Dynamic CMOS RAM

μPD421001 6-55
1,048,576 x 1-Bit Dynamic CMOS RAM

μPD421002 6-69
1,048,576 x 1-Bit Dynamic CMOS RAM

μPD424256 6-83
262,144 x 4-Bit Dynamic CMOS RAM

μPD424258 6-101
262,144 x 4-Bit Dynamic CMOS RAM

μPD424266 6-117
262,144 x 4-Bit Dynamic CMOS RAM

μPD424268 6-135
262,144 x 4-Bit Dynamic CMOS RAM

μPD424100 6-151
4,194,304 x 1-Bit Dynamic CMOS RAM

μPD424101 6-167
4,194,304 x 1-Bit Dynamic CMOS RAM

μPD424102 6-183
4,194,304 x 1-Bit Dynamic CMOS RAM

μPD424400 6-199
1,048,576 x 4-Bit Dynamic CMOS RAM

μPD424402 6-215
1,048,576 x 4-Bit Dynamic CMOS RAM

μPD424410 6-229
1,048,576 x 4-Bit Dynamic CMOS RAM

μPD424412 6-245
1,048,576 x 4-Bit Dynamic CMOS RAM

μPD424800 6-261
524,288 x 8-Bit Dynamic CMOS RAM

Application Note 53 6-277
μPD421000/421001/421002
1-Megabit Dynamic RAMs

Additional New Product Information

Device Number	Description	Comments
Dynamic RAMs		
μPD421000/1/2	1M x 1-bit; TSOP packaging	New package (GX suffix)
μPD424256/258/266/268	256K x 4 bits; TSOP packaging	New package (GX suffix)
μPD424100/1/2	4M x 1-bit DRAM enhancements	New speeds of 60 and 70 ns; new 300-mil SOJ (LA suffix); new TSOP package (Gx suffix)
μPD424400/402/410/412	1M x 4-bit DRAM enhancements	New speeds of 60 and 70 ns; new 300-mil SOJ package (LA suffix); new TSOP package (Gx suffix)
μPD424802	512K x 8-bit static-column DRAM	Speeds to 70 ns; SOJ and ZIP packaging
μPD424810	512K x 8-bit fast-page DRAM with write-per-bit option	Speeds to 70 ns; SOJ and ZIP packaging
μPD424812	512K x 8-bit static-column DRAM with write-per-bit option	Speeds to 70 ns; SOJ and ZIP packaging
μPD42xxxx	Various 256K x 16-bit DRAMs	40-pin SOJ, samples first half 1991

NEC Electronics Inc.

μPD41256
262,144 x 1-Bit
Dynamic NMOS RAM

Description

The μPD41256 is a 262,144-word by 1-bit dynamic RAM designed to operate from a single +5-volt power supply and fabricated with a double polylayer, N-channel, silicon-gate process for high density, high performance, and high reliability. A single-transistor storage cell and advanced dynamic circuitry, including 1024 sense amplifiers, ensure that power dissipation is minimized, while an on-chip circuit generates the negative-voltage substrate bias—automatically and transparently.

The three-state output is controlled by $\overline{CAS}$ independent of $\overline{RAS}$. After a valid read or read-modify-write cycle, data is held on the output by holding $\overline{CAS}$ low. The data output is returned to high impedance by returning $\overline{CAS}$ high. A hidden refresh feature allows $\overline{CAS}$ to be held low to maintain output data while $\overline{RAS}$ is used to execute refresh cycles.

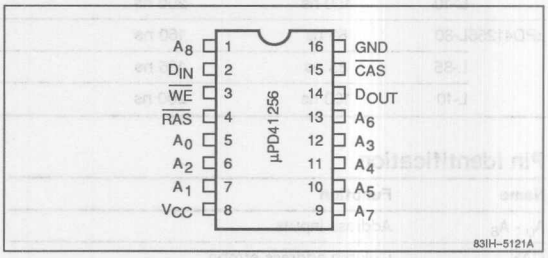
Refreshing may be accomplished by means of $\overline{RAS}$-only refresh cycles, hidden refresh cycles, $\overline{CAS}$ before $\overline{RAS}$ refresh cycles, or by normal read or write cycles on the 256 address combinations of A_0 through A_7 during a 4-ms refresh period.

Features

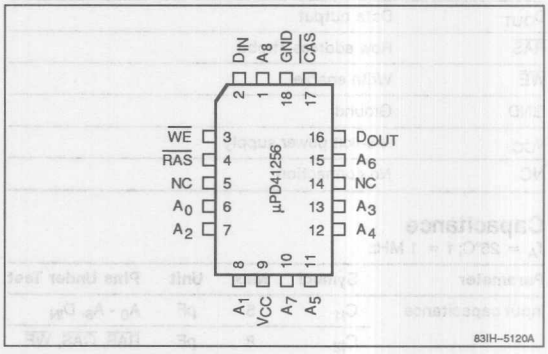
- 262,144-word x 1-bit organization
- High-density plastic DIP and PLCC packaging
- Multiplexed address inputs
- Single +5-volt power supply
- On-chip substrate bias generator
- Low power dissipation of 28 mW max (standby)
- Nonlatched, three-state outputs
- Fully TTL-compatible inputs and outputs
- Low input capacitance
- 256 refresh cycles every 4 ms
- Optional page cycle
- $\overline{RAS}$-only, hidden, and $\overline{CAS}$ before $\overline{RAS}$ refreshing

Pin Configurations

16-Pin Plastic DIP



18-Pin Plastic Leaded Chip Carrier (PLCC)



6

Ordering Information

Part Number	Row Access Time (max)	R/W Cycle (min)	Page Cycle (min)	Power Supply Tolerance	Package
μPD41256C-80	80 ns	160 ns	70 ns	±5%	16-pin plastic DIP
C-85	85 ns	165 ns	70 ns		
C-10	100 ns	200 ns	100 ns	±10%	
μPD41256L-80	80 ns	160 ns	70 ns	±5%	18-pin plastic leaded chip carrier
L-85	85 ns	165 ns	70 ns		
L-10	100 ns	200 ns	100 ns	±10%	

Pin Identification

Name	Function
A_0 - A_8	Address inputs
$\overline{CAS}$	Column address strobe
D_{IN}	Data input
D_{OUT}	Data output
$\overline{RAS}$	Row address strobe
$\overline{WE}$	Write enable
GND	Ground
V_{CC}	+5-volt power supply
NC	No connection

Capacitance

T_A = 25°C; f = 1 MHz

Parameter	Symbol	Max	Unit	Pins Under Test
Input capacitance	C_{I1}	5	pF	A_0 - A_8, D_{IN}
	C_{I2}	8	pF	$\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$
Output capacitance	C_{OUT}	7	pF	D_{OUT}

Absolute Maximum Ratings

Voltage on any pin relative to GND, V_T	−1.0 to +7.0 V
Operating temperature, T_A (ambient)	0 to +70°C
Storage temperature, T_{STG}	−55 to +125°C
Short-circuit output current, I_{OS}	50 mA
Power dissipation, P_D	1.0 W

Exposure to Absolute Maximum Ratings for extended periods may affect device reliability; exceeding the ratings could cause permanent damage. The device should be operated within the limits specified under DC and AC Characteristics.

Recommended Operating Conditions

Parameter	Symbol	Min	Typ	Max	Unit
Supply voltage	V_{CC}	4.5	5.0	5.5	V
Input voltage, high	V_{IH}	2.4		V_{CC} + 1.0	V
Input voltage, low	V_{IL}	−1.0		0.8	V
Ambient temperature	T_A	0		70	°C

Notes:

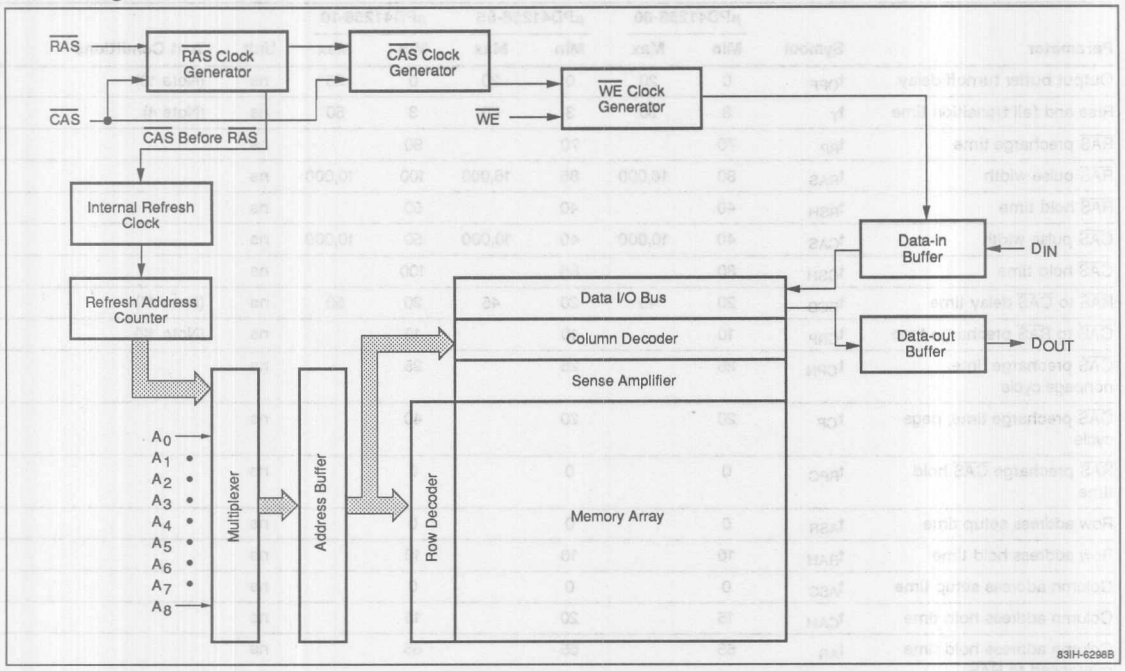
(1) V_{CC} = +5 V ±5% for the −80 and −85 versions.

DC Characteristics

T_A = 0 to +70°C; V_{CC} = +5.0 V ±10%

Parameter	Symbol	Min	Max	Unit	Test Conditions
Standby supply current	I_{CC2}		5.0	mA	$\overline{RAS}$ = V_{IH}; D_{OUT} = high impedance
Input leakage current	$I_{I(L)}$	−10	10	μA	V_{IN} = 0 V to V_{CC}; all other pins not under test = 0 V
Output leakage current	$I_{O(L)}$	−10	10	μA	D_{OUT} disabled; V_{OUT} = 0 V to V_{CC}
Output voltage, low	V_{OL}		0.4	V	I_{OL} = 4.2 mA
Output voltage, high	V_{OH}	2.4		V	I_{OUT} = −5 mA

Block Diagram



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AC Characteristics

T_A = 0 to +70°C

Parameter	Symbol	μPD41256-80 Min	μPD41256-80 Max	μPD41256-85 Min	μPD41256-85 Max	μPD41256-10 Min	μPD41256-10 Max	Unit	Test Conditions
Supply voltage	V_{CC}	4.75	5.25	4.75	5.25	4.5	5.5		
Operating supply current, average	I_{CC1}		90		90		80	mA	$\overline{RAS}$, $\overline{CAS}$ cycling; $t_{RC} = t_{RC}$ (min); I_O = 0 mA (Note 5)
Operating supply current, $\overline{RAS}$-only refresh cycle, average	I_{CC3}		80		80		65	mA	$\overline{RAS}$ cycling; $\overline{CAS} \geq V_{IH}$; $t_{RC} = t_{RC}$ (min); I_O = 0 mA (Note 5)
Operating supply current, page cycle, average	I_{CC4}		70		70		60	mA	$\overline{RAS} \leq V_{IL}$; $\overline{CAS}$ cycling; $t_{PC} = t_{PC}$ (min); I_O = 0 mA (Note 5)
Operating current, $\overline{CAS}$ before $\overline{RAS}$ refresh cycle, average	I_{CC5}		80		80		65	mA	$\overline{CAS} \leq V_{IL}$; $\overline{RAS}$ cycling; $t_{RC} = t_{RC}$ (min); I/O = 0 mA (Note 5)
Random read or write cycle time	t_{RC}	180		165		200		ns	(Note 6)
Read-write cycle time	t_{RWC}	185		195		240		ns	(Note 6)
Page cycle time	t_{PC}	70		70		100		ns	(Note 6)
Access time from $\overline{RAS}$	t_{RAC}		80		85		100	ns	(Notes 7, 8)
Access time from $\overline{CAS}$	t_{CAC}		40		40		50	ns	(Notes 7, 9)

AC Characteristics (cont)

Parameter	Symbol	μPD41256-80		μPD41256-85		μPD41256-10		Unit	Test Conditions
		Min	Max	Min	Max	Min	Max		
Output buffer turnoff delay	t_{OFF}	0	20	0	20	0	25	ns	(Note 10)
Rise and fall transition time	t_T	3	50	3	50	3	50	ns	(Note 4)
$\overline{RAS}$ precharge time	t_{RP}	70		70		90		ns	
$\overline{RAS}$ pulse width	t_{RAS}	80	16,000	85	16,000	100	10,000	ns	
$\overline{RAS}$ hold time	t_{RSH}	40		40		50		ns	
$\overline{CAS}$ pulse width	t_{CAS}	40	10,000	40	10,000	50	10,000	ns	
$\overline{CAS}$ hold time	t_{CSH}	80		85		100		ns	
$\overline{RAS}$ to $\overline{CAS}$ delay time	t_{RCD}	20	40	20	45	20	50	ns	(Note 11)
$\overline{CAS}$ to $\overline{RAS}$ precharge time	t_{CRP}	10		10		10		ns	(Note 12)
$\overline{CAS}$ precharge time, nonpage cycle	t_{CPN}	25		25		25		ns	
$\overline{CAS}$ precharge time, page cycle	t_{CP}	20		20		40		ns	
$\overline{RAS}$ precharge $\overline{CAS}$ hold time	t_{RPC}	0		0		0		ns	
Row address setup time	t_{ASR}	0		0		0		ns	
Row address hold time	t_{RAH}	10		10		10		ns	
Column address setup time	t_{ASC}	0		0		0		ns	
Column address hold time	t_{CAH}	15		20		15		ns	
Column address hold time referenced to $\overline{RAS}$	t_{AR}	55		65		65		ns	
Read command setup time	t_{RCS}	0		0		0		ns	
Read command hold time referenced to $\overline{RAS}$	t_{RRH}	10		10		10		ns	(Note 13)
Read command hold time referenced to $\overline{CAS}$	t_{RCH}	0		0		0		ns	(Note 13)
Write command hold time	t_{WCH}	20		20		25		ns	
Write command hold time referenced to $\overline{RAS}$	t_{WCR}	60		65		75		ns	
Write command pulse width	t_{WP}	20		15		15		ns	(Note 17)
Write command to $\overline{RAS}$ lead time	t_{RWL}	20		30		35		ns	
Write command to $\overline{CAS}$ lead time	t_{CWL}	20		30		35		ns	
Data-in setup time	t_{DS}	0		0		0		ns	(Note 14)
Data-in hold time	t_{DH}	20		20		25		ns	(Note 14)
Data-in hold time referenced to $\overline{RAS}$	t_{DHR}	60		65		75		ns	
Refresh period	t_{REF}		4		4		4	ms	Addresses A_0 - A_7
$\overline{WE}$ command setup time	t_{WCS}	0		0		0		ns	(Note 15)
$\overline{CAS}$ to $\overline{WE}$ delay	t_{CWD}	40		40		50		ns	(Note 15)
$\overline{RAS}$ to $\overline{WE}$ delay	t_{RWD}	80		85		100		ns	(Note 15)
$\overline{CAS}$ setup time for $\overline{CAS}$ before $\overline{RAS}$ refresh cycle	t_{CSR}	10		10		10		ns	(Note 16)

AC Characteristics (cont)

Parameter	Symbol	μPD41256-80 Min	μPD41256-80 Max	μPD41256-85 Min	μPD41256-85 Max	μPD41256-10 Min	μPD41256-10 Max	Unit	Test Conditions
$\overline{CAS}$ hold time for $\overline{CAS}$ before $\overline{RAS}$ refresh cycle	t_{CHR}	20		15		20		ns	(Note 16)
Read-write cycle time (counter test cycle)	t_{TRC}	N/A		N/A		220		ns	(Note 18)
Read-write cycle time (counter test cycle)	t_{TRWC}	N/A		N/A		260		ns	(Note 18)

Notes:

(1) All voltages are referenced to GND.

(2) An initial pause of 100 μs is required after power-up, followed by any eight $\overline{RAS}$ cycles, before proper device operation is achieved.

(3) AC measurements assume t_T = 5 ns.

(4) V_{IH} (min) and V_{IL} (max) are reference levels for measuring the timing of input signals. Transition times are measured between V_{IH} and V_{IL}.

(5) I_{CC1}, I_{CC3}, I_{CC4}, and I_{CC5} depend on output loading and cycle rates. Specified values are obtained with the output open.

(6) The minimum specifications are used only to indicate the cycle time at which proper operation over the full temperature range (T_A = 0 to +70°C) is assured.

(7) Output load = 2 TTL loads and 100 pF

(8) Assumes that $t_{RCD} \leq t_{RCD}$ (max). If t_{RCD} is greater than the maximum recommended value shown in this table, t_{RAC} will increase by the amount that t_{RCD} exceeds the value shown.

(9) Assumes that $t_{RCD} \geq t_{RCD}$ (max)

(10) t_{OFF} (max) defines the time at which the output achieves the open-circuit condition and is not referenced to V_{OH} or V_{OL}.

(11) Operation within the t_{RCD} (max) limit assures that t_{RAC} (max) can be met. t_{RCD} (max) is specified as a reference point only. If t_{RCD} is greater than the specified t_{RCD} (max) limit, then access time is controlled exclusively by t_{CAC}.

(12) The t_{CRP} requirement should be applicable for $\overline{RAS}$/$\overline{CAS}$ cycles preceded by any cycle.

(13) Either t_{RRH} or t_{RCH} must be satisfied for a read cycle.

(14) These parameters are referenced to the leading edge of $\overline{CAS}$ in early write cycles and to the leading edge of $\overline{WE}$ in delayed write or read-modify-write cycles.

(15) t_{WCS}, t_{CWD}, and t_{RWD} are restrictive operating parameters in read-write and read-modify-write cycles only. If $t_{WCS} \geq t_{WCS}$ (min), the cycle is an early write cycle and the data output will remain open-circuit throughout the entire cycle. If $t_{CWD} \geq t_{CWD}$ (min) and $t_{RWD} \geq t_{RWD}$ (min), the cycle is a read-write cycle and the data output will contain data read from the selected cell. If neither of the above conditions is met, the condition of the data output (at access time and until $\overline{CAS}$ goes back to V_{IH}) is indeterminate.

(16) DIP products with process codes E, K, P and X do not have the $\overline{CAS}$ before $\overline{RAS}$ refresh feature. All other package types and process codes do have $\overline{CAS}$ before $\overline{RAS}$ refreshing.

On DIP products with process codes E, K, P and X, the external address inputs are required in hidden refresh cycles and the address timing must satisfy t_{ASR} and t_{RAH}, which are specified with respect to the falling edge of $\overline{RAS}$.

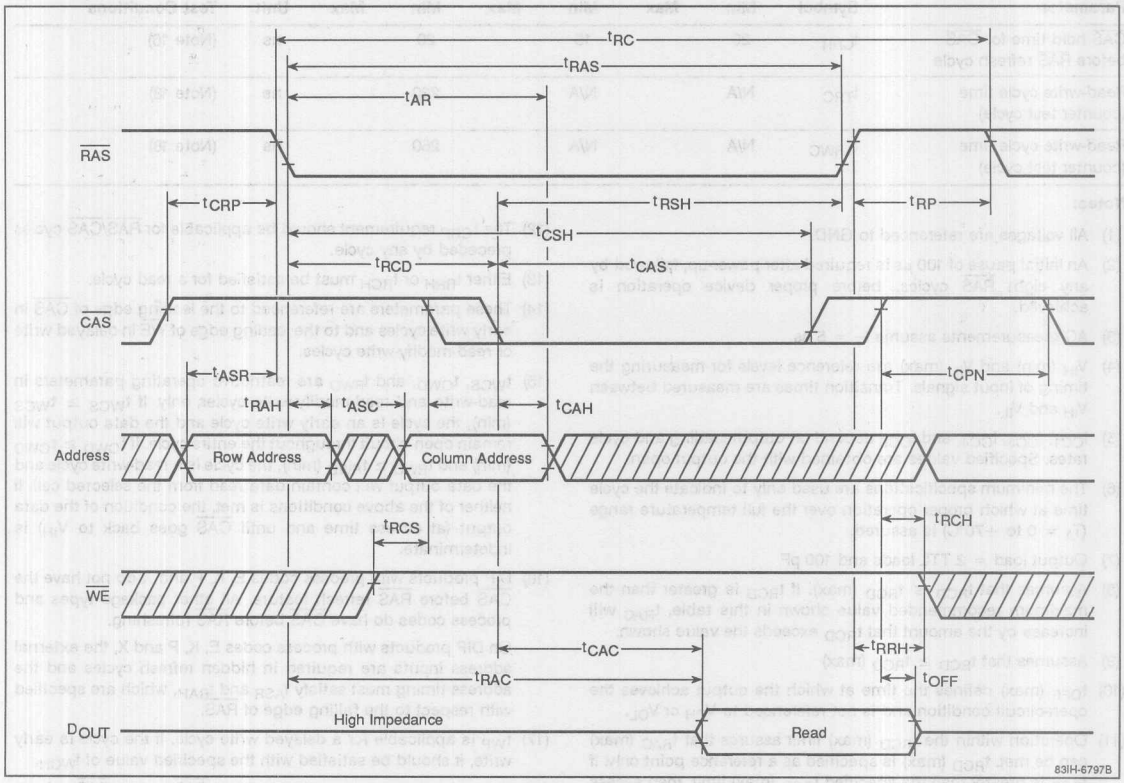
(17) t_{WP} is applicable for a delayed write cycle. If the cycle is early write, it should be satisfied with the specified value of t_{WCH}.

(18) t_{TRC} and t_{TRWL} are applicable for a $\overline{CAS}$ before $\overline{RAS}$ refresh counter test cycle.

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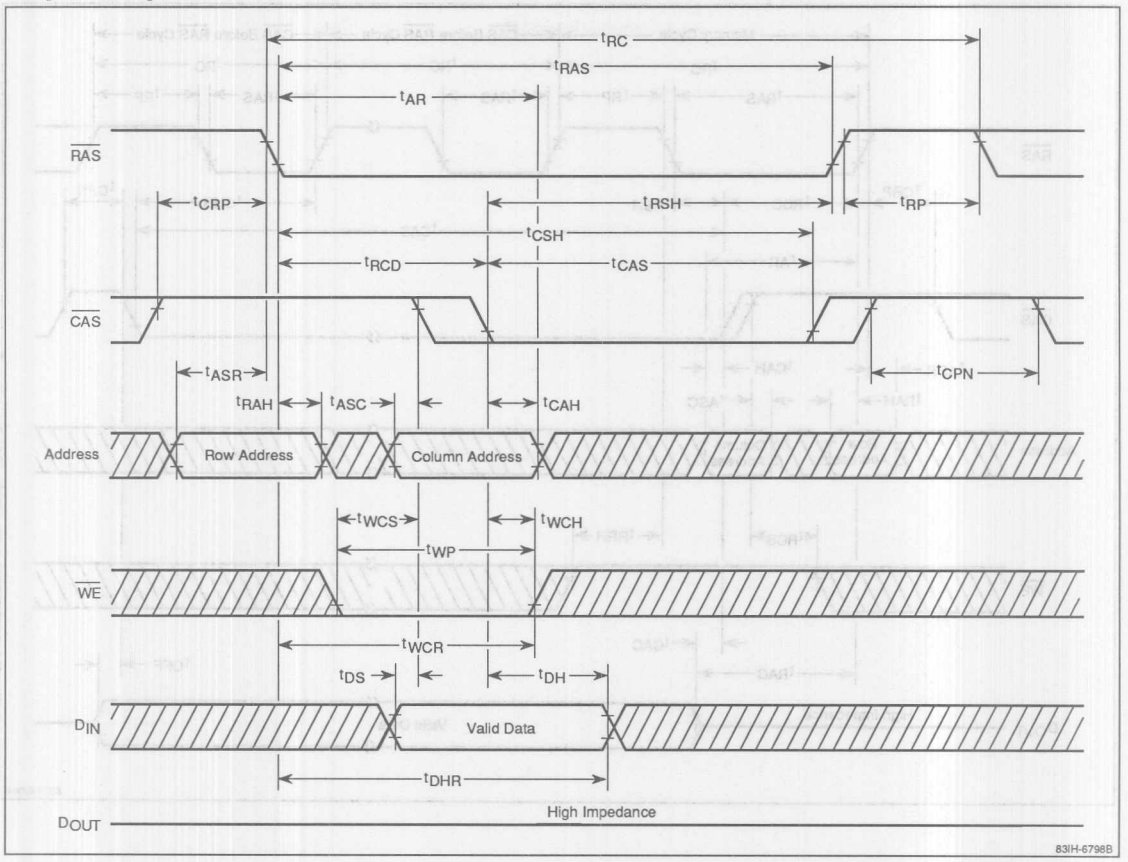
Timing Waveforms

Read Cycle



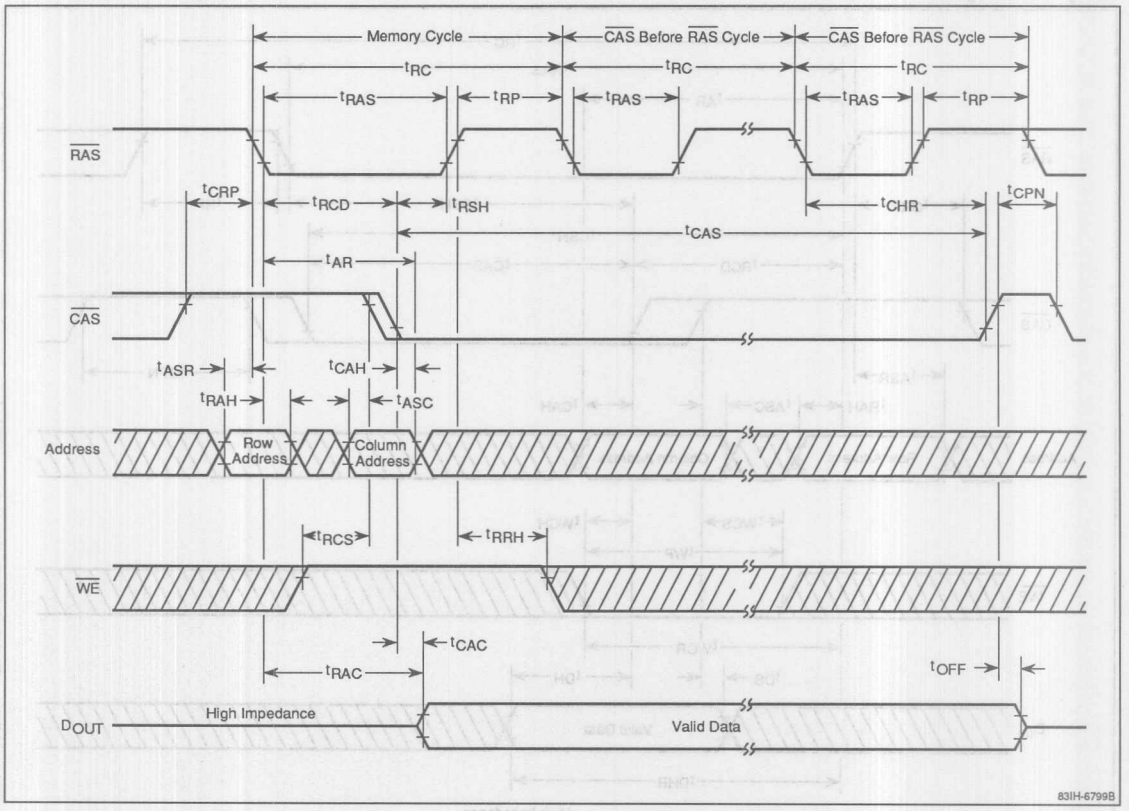
Timing Waveforms (cont)

Early Write Cycle



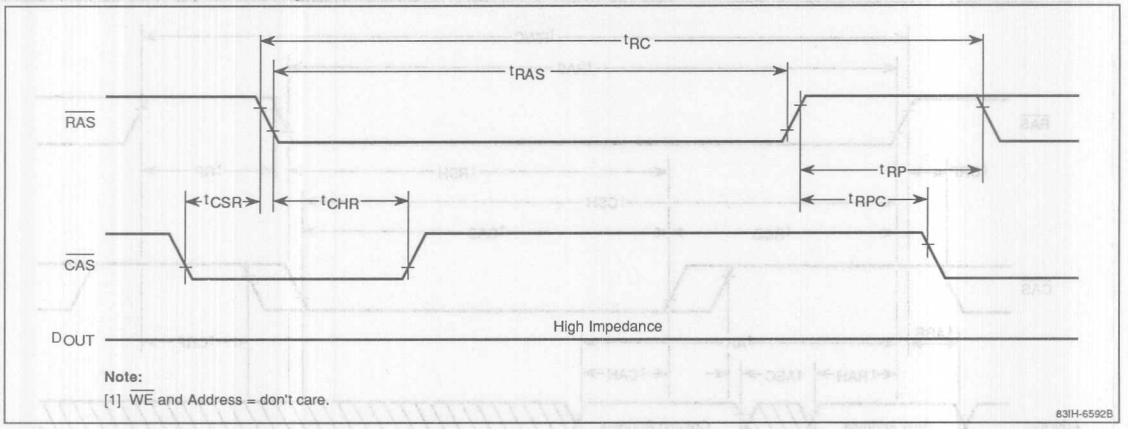
Timing Waveforms (cont)

Hidden Refresh Cycle



Timing Waveforms (cont)

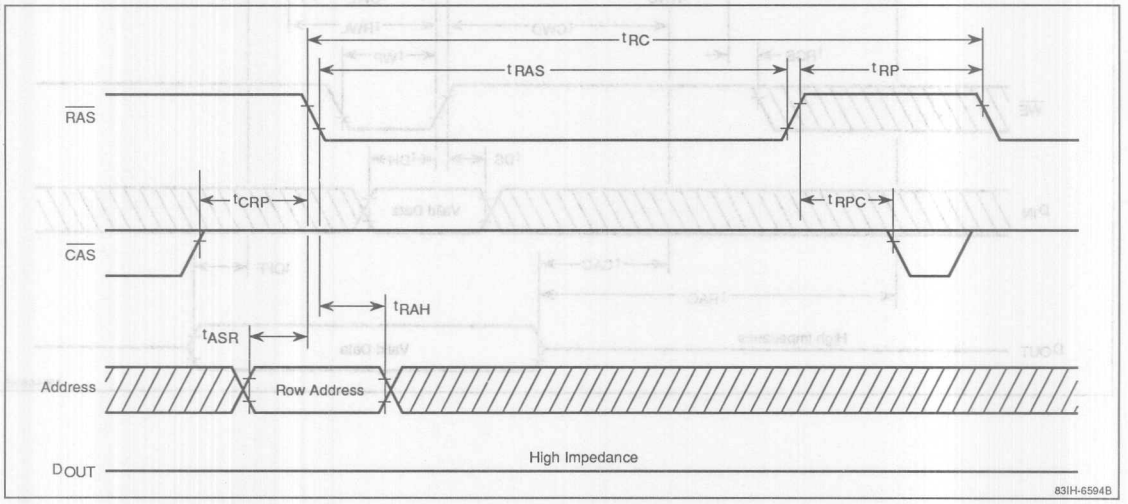
$\overline{CAS}$ Before $\overline{RAS}$ Refresh Cycle



Note:
[1] $\overline{WE}$ and Address = don't care.

83IH-6592B

$\overline{RAS}$-Only Refresh Cycle

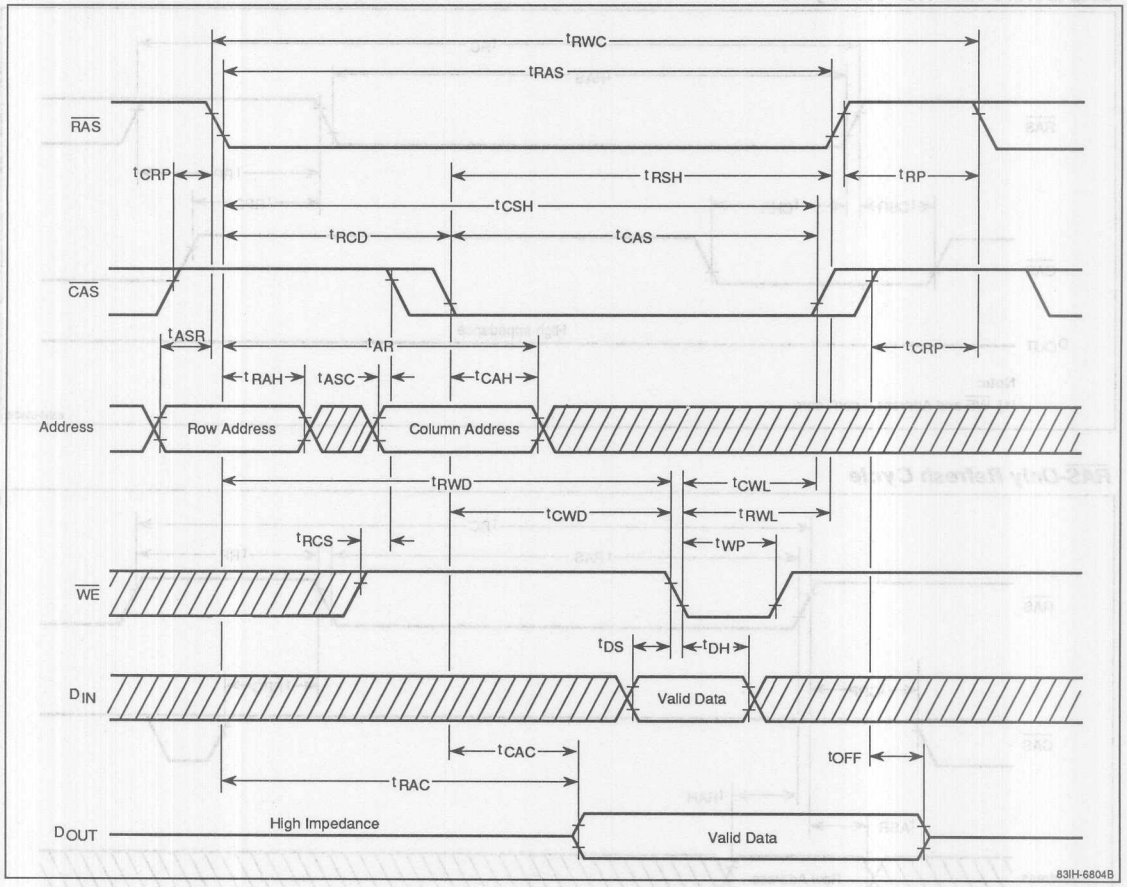


83IH-6594B

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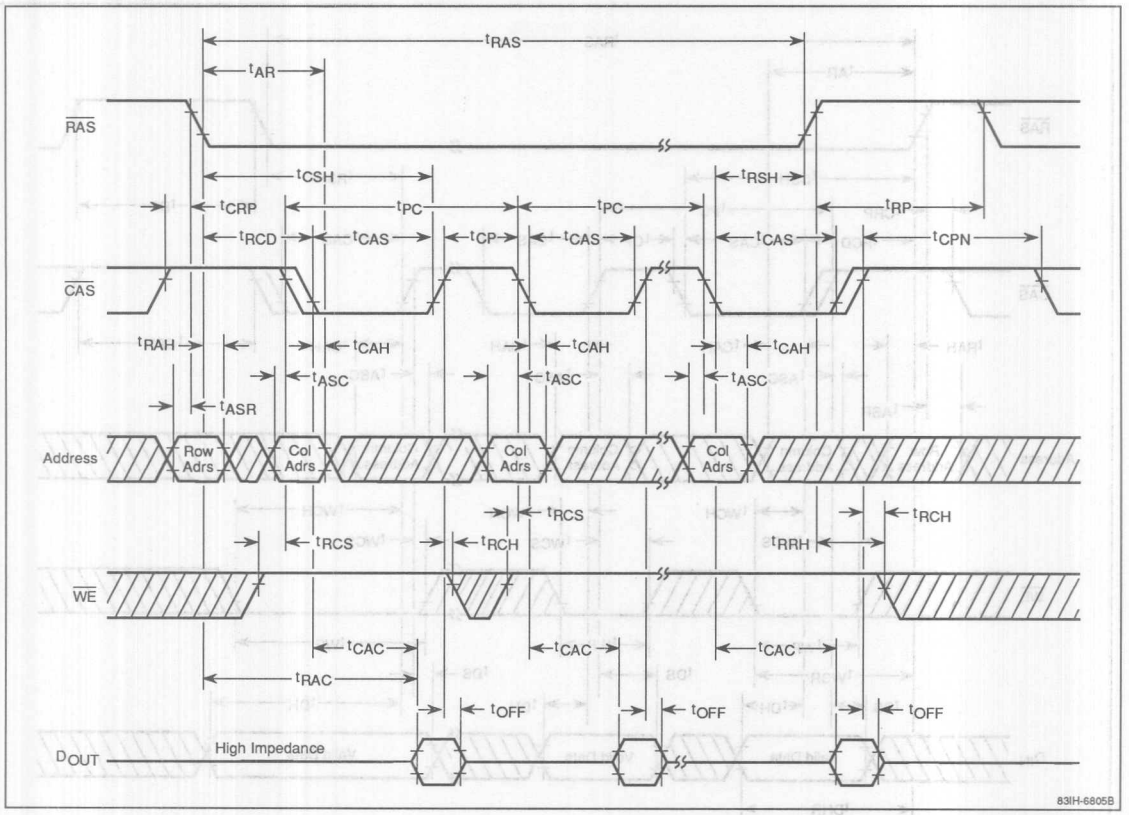
Timing Waveforms (cont)

Read-Write/Read-Modify-Write Cycle



Timing Waveforms (cont)

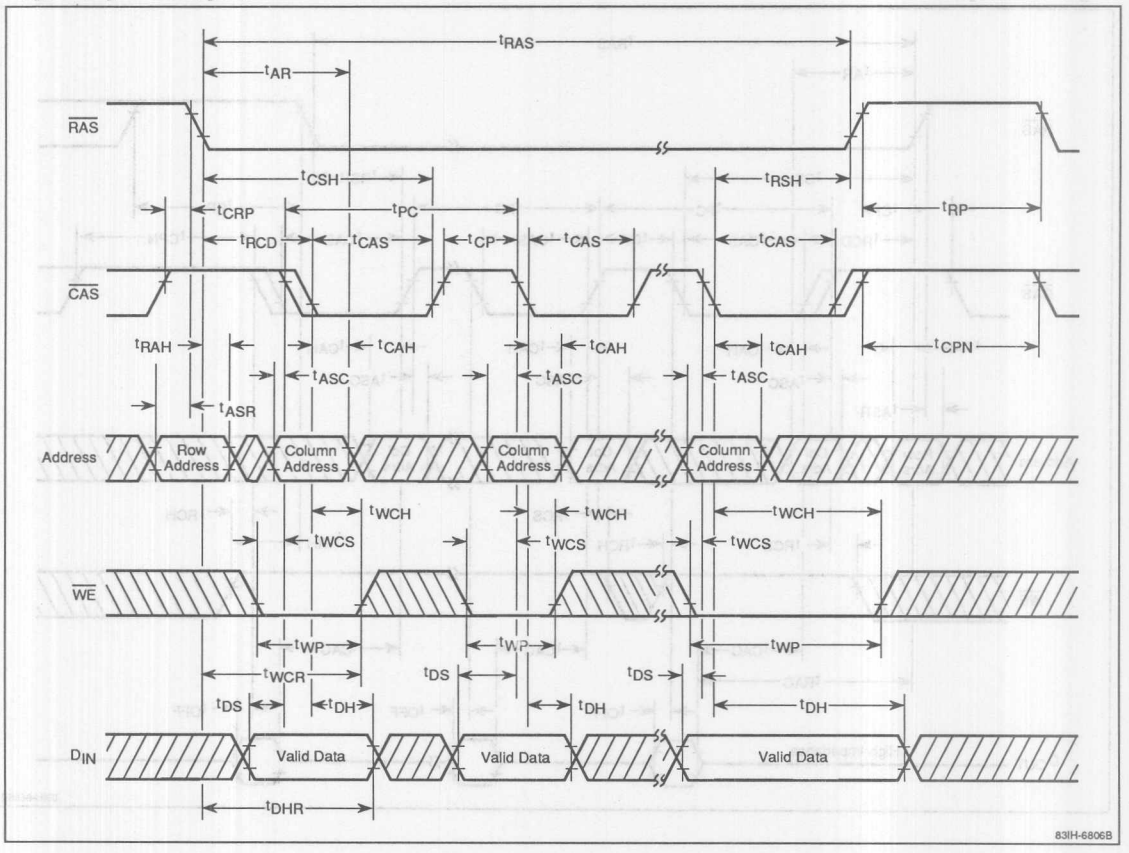
Page Read Cycle



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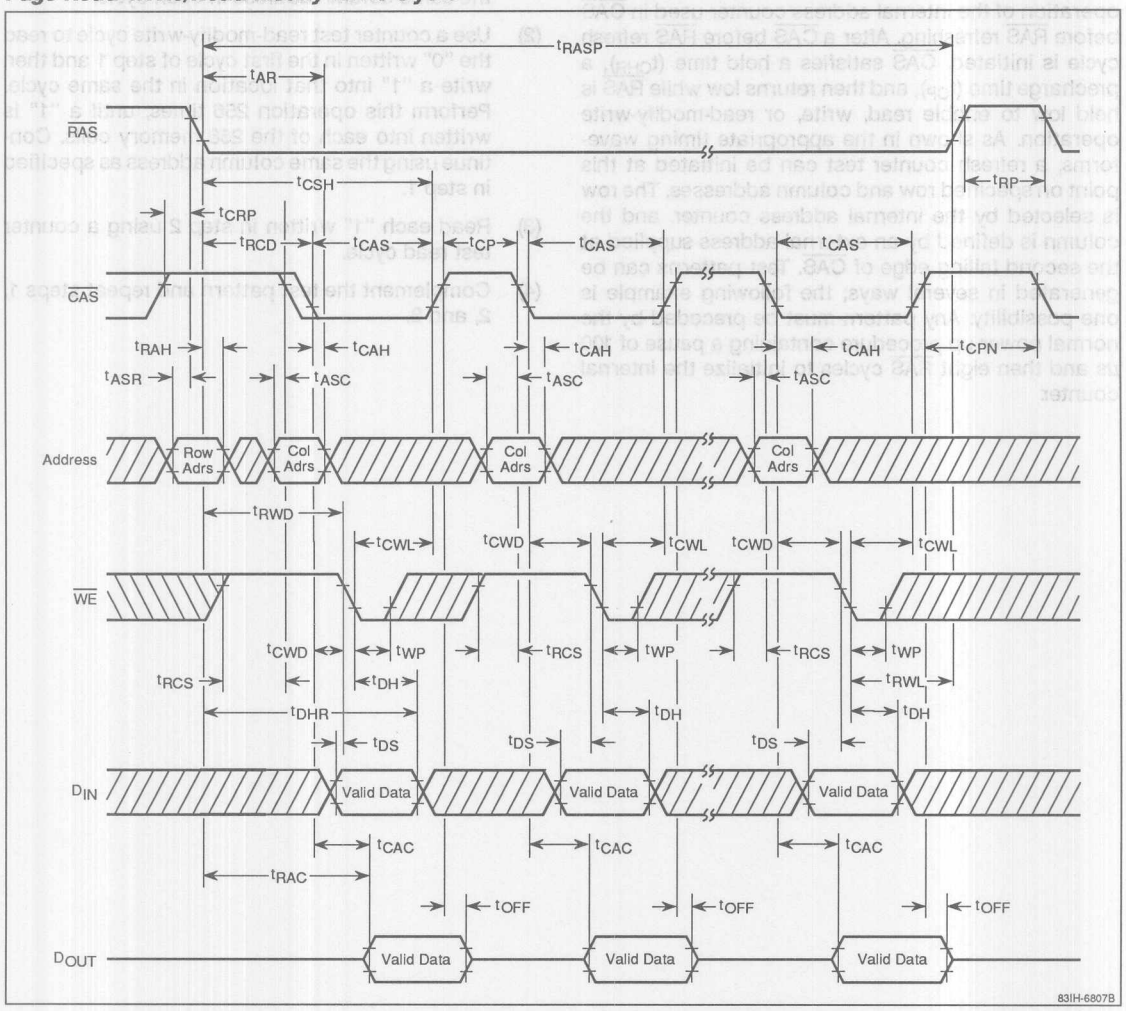
Timing Waveforms (cont)

Page Early Write Cycle



Timing Waveforms (cont)

Page Read-Write/Read-Modify-Write Cycle



6

$\overline{CAS}$ Before $\overline{RAS}$ Refresh Counter Test

The μPD41256 provides a method to verify proper operation of the internal address counter used in $\overline{CAS}$ before $\overline{RAS}$ refreshing. After a $\overline{CAS}$ before $\overline{RAS}$ refresh cycle is initiated, $\overline{CAS}$ satisfies a hold time (t_{CHR}), a precharge time (t_{CP}), and then returns low while $\overline{RAS}$ is held low to enable read, write, or read-modify-write operation. As shown in the appropriate timing waveforms, a refresh counter test can be initiated at this point on specified row and column addresses. The row is selected by the internal address counter, and the column is defined by an external address supplied at the second falling edge of $\overline{CAS}$. Test patterns can be generated in several ways; the following example is one possibility. Any pattern must be preceded by the normal power-up procedure containing a pause of 100 μs and then eight $\overline{RAS}$ cycles to initialize the internal counter.

(1) Write "0" into 256 memory cells with 256 $\overline{CAS}$ before $\overline{RAS}$ refresh counter test write cycles. Use the same column address in each cycle.

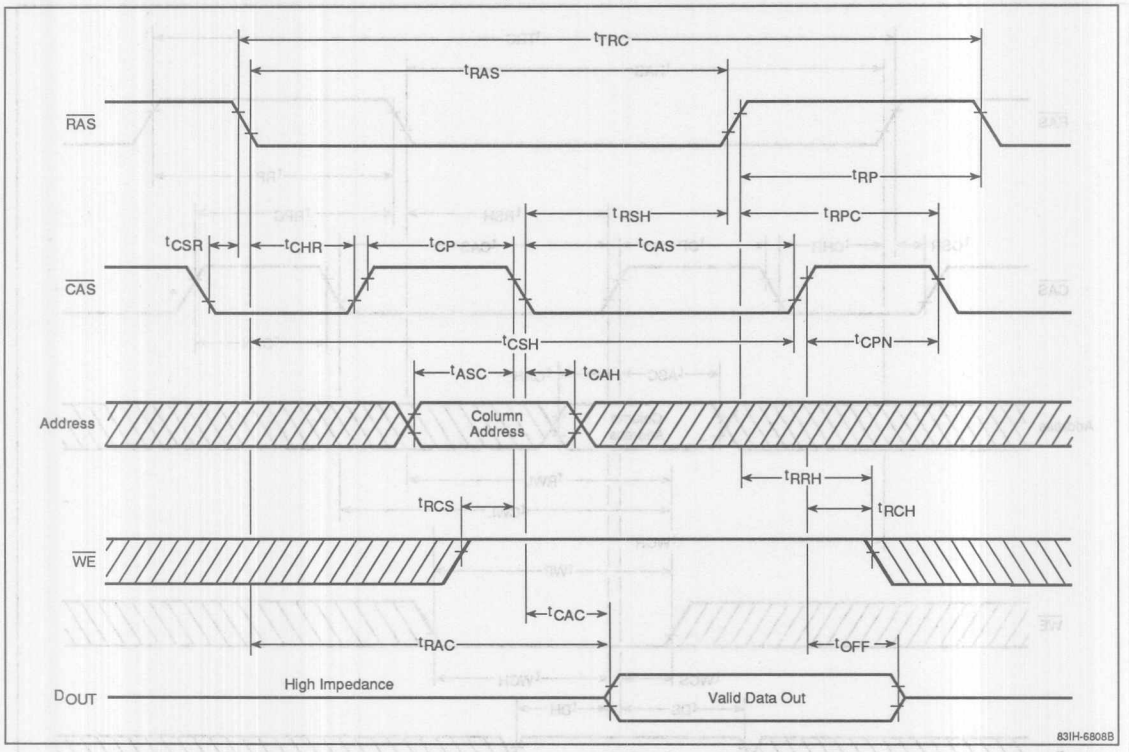
(2) Use a counter test read-modify-write cycle to read the "0" written in the first cycle of step 1 and then write a "1" into that location in the same cycle. Perform this operation 256 times, until a "1" is written into each of the 256 memory cells. Continue using the same column address as specified in step 1.

(3) Read each "1" written in step 2 using a counter test read cycle.

(4) Complement the test pattern and repeat steps 1, 2, and 3.

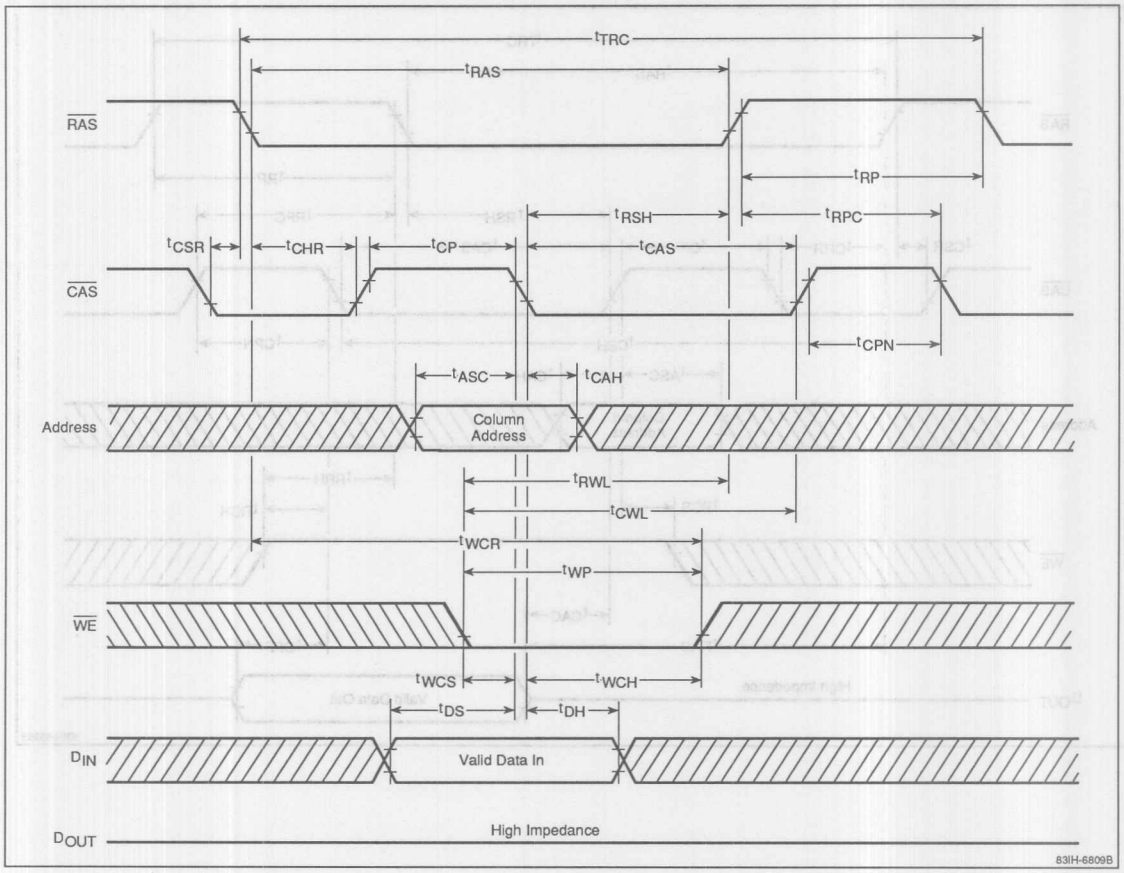
Timing Waveforms (cont)

$\overline{CAS}$ Before $\overline{RAS}$ Refresh Counter Test Read Cycle



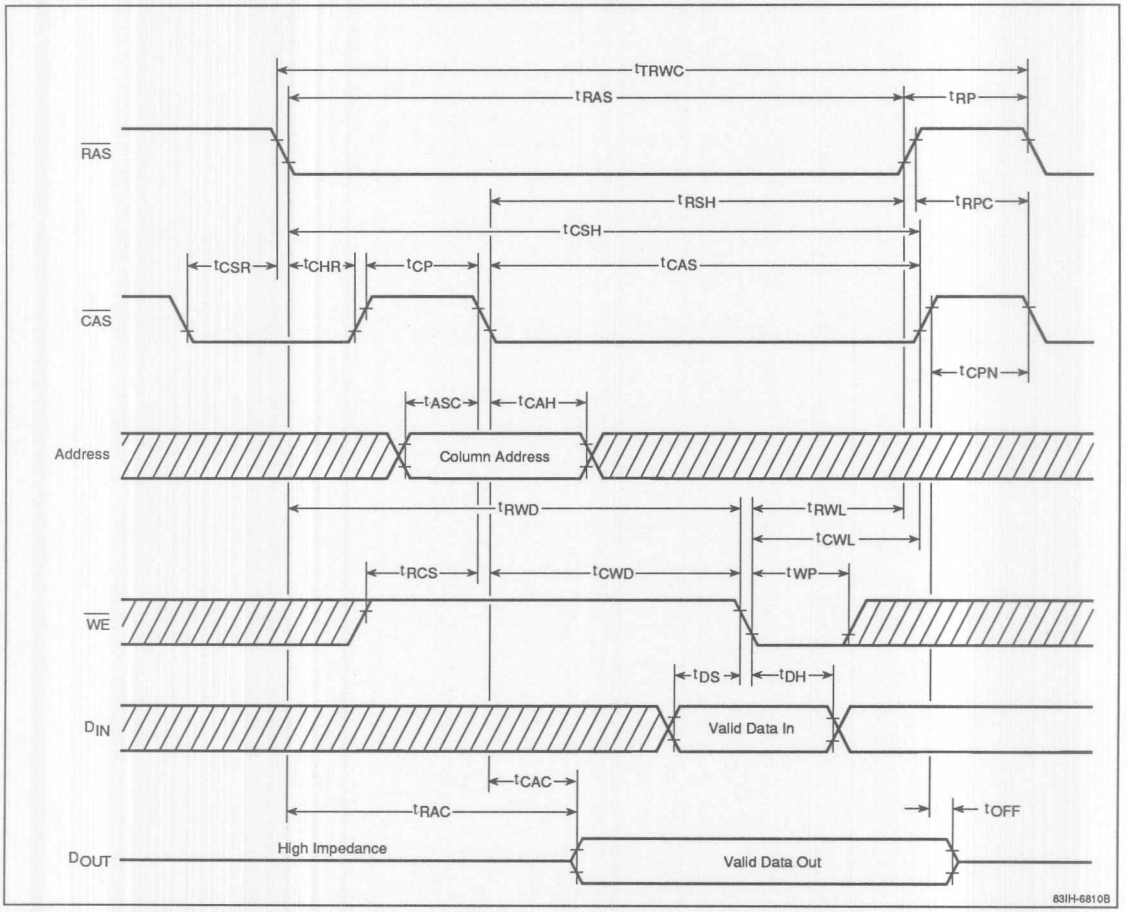
Timing Waveforms (cont)

$\overline{CAS}$ Before $\overline{RAS}$ Refresh Counter Test Write Cycle

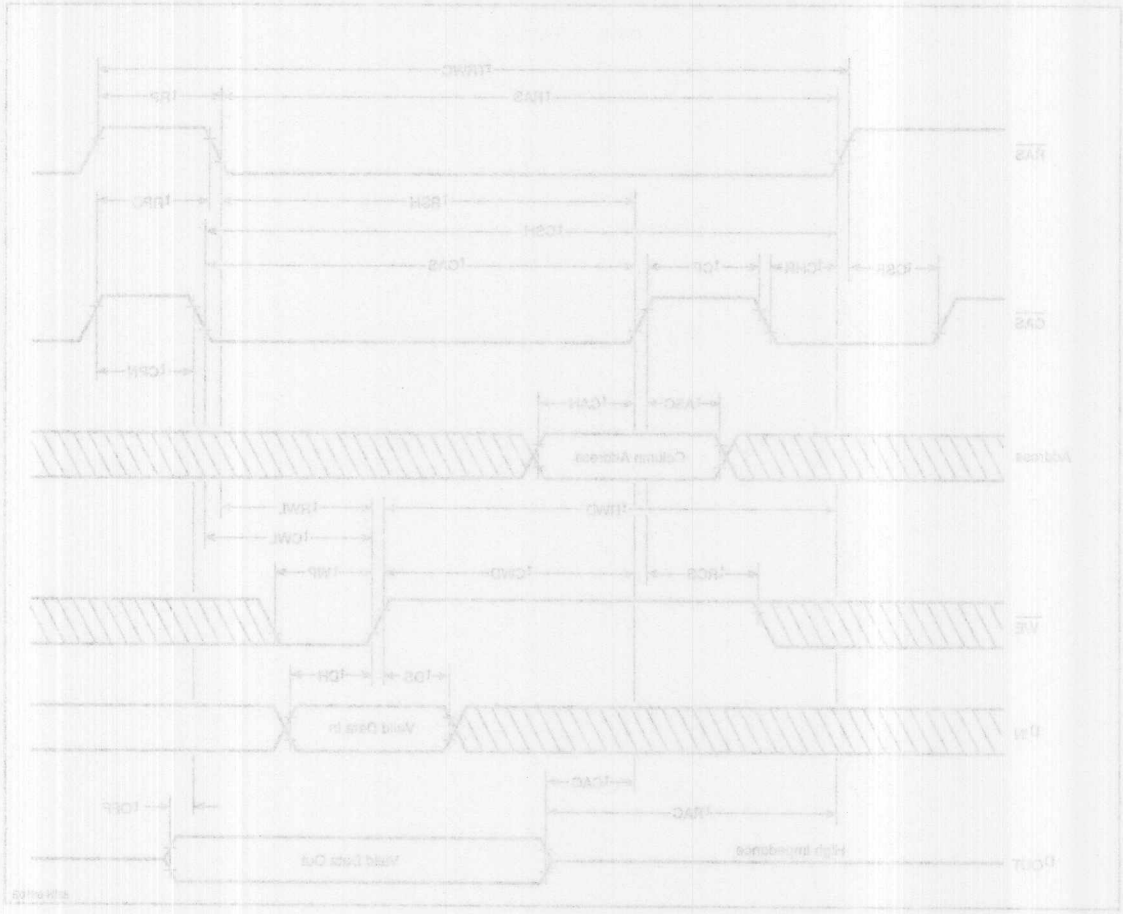


Timing Waveforms (cont)

$\overline{CAS}$ Before $\overline{RAS}$ Refresh Counter Test Read-Modify-Write Cycle



6



μPD41464
65,536 x 4-Bit
Dynamic NMOS RAM

Description

The μPD41464 is a 65,536-word by 4-bit dynamic RAM designed to operate from a single + 5-volt power supply and fabricated with a double polylayer, N-channel silicon-gate process for high density, high performance, and high reliability. A single-transistor storage cell and advanced dynamic circuitry ensure minimum power dissipation, while an on-chip feature internally generates the negative voltage substrate bias—automatically and transparently.

The three-state I/O is controlled by $\overline{CAS}$ independent of $\overline{RAS}$. After a valid read or hidden refresh cycle, data is held by holding $\overline{CAS}$ low. Data input and output is returned to high impedance by returning $\overline{CAS}$ high. Hidden refreshing allows $\overline{CAS}$ to be held low to maintain output data while $\overline{RAS}$ is used to execute $\overline{RAS}$-only refresh cycles.

Refreshing may be accomplished by means of a $\overline{CAS}$ before $\overline{RAS}$ cycle that internally generates the refresh address, by means of $\overline{RAS}$-only refresh cycles, or by normal read or write cycles on the 256 address combinations of A_0 through A_7 during a 4-ms refresh period.

Features

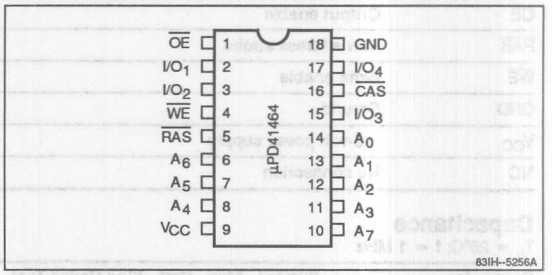
- 65,536-word by 4-bit organization
- Single + 5-volt ±10% power supply
- $\overline{CAS}$ before $\overline{RAS}$ internal refreshing
- Multiplexed address inputs
- On-chip substrate bias generator
- Low power dissipation
  - —28 mA max (standby)
  - —440 mW (active, $t_{RC} = t_{RC}$ min)
- Nonlatched, TTL-compatible inputs and outputs
- Low input capacitance
- 256 refresh cycles every 4 ms
- Standard 18-pin plastic DIP and PLCC packaging

Ordering Information

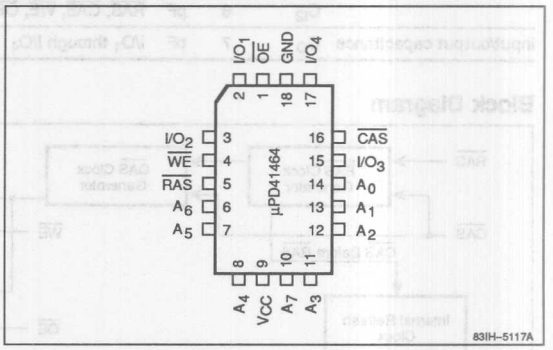
Part Number	Row Access Time (max)	Package
μPD41464C-80	80 ns	18-pin plastic DIP
C-10	100 ns	
C-12	120 ns	
μPD41464L-80	80 ns	18-pin PLCC
L-10	100 ns	
L-12	120 ns	

Pin Configurations

18-Pin Plastic DIP



18-Pin Plastic Leaded Chip Carrier (PLCC)



6

Pin Identification

Name	Function
A_0 - A_7	Address inputs
I/O_1 - I/O_4	Data inputs and outputs
$\overline{CAS}$	Column address strobe
$\overline{OE}$	Output enable
$\overline{RAS}$	Row address strobe
$\overline{WE}$	Write enable
GND	Ground
V_{CC}	+5-volt power supply
NC	No connection

Capacitance

T_A = 25°C; f = 1 MHz

Parameter	Symbol	Max	Unit	Pins Under Test
Input capacitance	C_{I1}	5	pF	A_0 through A_7
	C_{I2}	8	pF	$\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$, $\overline{OE}$
Input/output capacitance	C_O	7	pF	I/O_1 through I/O_4

Absolute Maximum Ratings

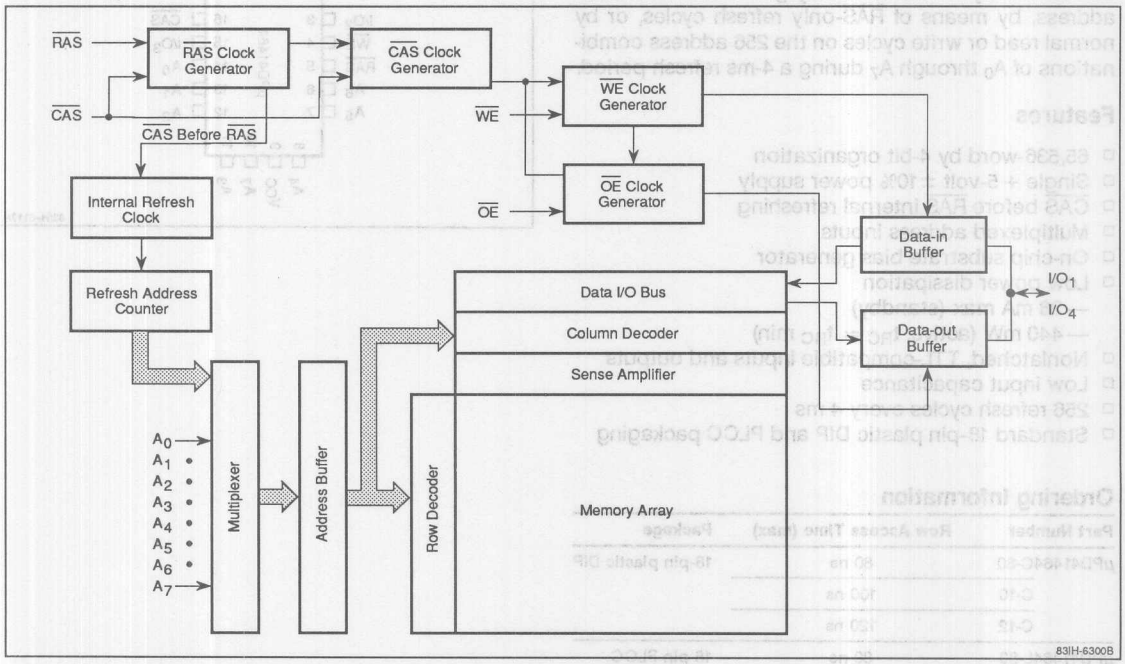
Voltage on any pin relative to GND	−1.0 to +7.0 V
Operating temperature, T_{OPR}	0 to +70°C
Storage temperature, T_{STG}	−55 to +125°C
Short-circuit output current, I_{OS}	50 mA
Power dissipation, P_D	1.0 W

Exposure to Absolute Maximum Ratings for extended periods may affect device reliability; exceeding the ratings could cause permanent damage. The device should be operated within the limits specified under DC and AC Characteristics.

Recommended Operating Conditions

Parameter	Symbol	Min	Typ	Max	Unit
Input voltage, high	V_{IH}	2.4		V_{CC} + 1	V
Input voltage, low	V_{IL}	−1		0.8	V
Supply voltage	V_{CC}	4.5	5.0	5.5	V
Ambient temperature	T_A	0		70	°C

Block Diagram



DC Characteristics

T_A = 0 to +70°C; V_{CC} = +5.0 V ±10%

Parameter	Symbol	Min	Max	Unit	Test Conditions
Standby current	I_{CC2}		5.0	mA	$\overline{RAS}$ = $\overline{CAS}$ = V_{IH}
Input leakage current	$I_{I(L)}$	–10	10	μA	V_{IN} = 0 V to V_{CC}; all other pins not under test = 0 V
Output leakage current	$I_{O(L)}$	–10	10	μA	I/O is high-Z; $V_{I/O}$ = 0 V to V_{CC}
Output voltage, low	V_{OL}	0	0.4	V	I_{OL} = 4.2 mA
Output voltage, high	V_{OH}	2.4	V_{CC}	V	I_{OH} = –5 mA

AC Characteristics

T_A = 0 to +70°C; V_{CC} = +5.0 V ±10%

		μPD41464–80		μPD41464–10		μPD41464–12			
Parameter	Symbol	Min	Max	Min	Max	Min	Max	Unit	Test Conditions
Operating current, average	I_{CC1}		85		80		75	mA	$\overline{RAS}$, $\overline{CAS}$ cycling; t_{RC} = t_{RC} min (Note 5)
Operating current, refresh cycle, average	I_{CC3}		70		65		60	mA	$\overline{RAS}$ cycling; $\overline{CAS}$ = V_{IH}; t_{RC} = t_{RC} min (Note 5)
Operating current, page cycle, average	I_{CC4}		60		55		50	mA	$\overline{RAS}$ = V_{IL}; $\overline{CAS}$ cycling; t_{PC} = t_{PC} min (Note 5)
Operating current, $\overline{CAS}$ before $\overline{RAS}$ refresh cycle, average	I_{CC5}		70		70		65	mA	$\overline{RAS}$ cycling; $\overline{CAS}$ ≥ V_{IH}; t_{RC} = t_{RC} min (Note 5)
Random read or write cycle time	t_{RC}	160		200		220		ns	(Note 6)
Read-write cycle time	t_{RWC}	230		270		300		ns	(Note 6)
Page cycle time	t_{PC}	70		100		120		ns	(Note 6)
Refresh period	t_{REF}		4		4		4	ms	
Access time from $\overline{RAS}$	t_{RAC}		80		100		120	ns	(Notes 7, 8)
Access time from $\overline{CAS}$	t_{CAC}		40		50		60	ns	(Notes 7, 9)
Ouput buffer turnoff delay	t_{OFF}	0	20	0	25	0	30	ns	(Note 10)
Rise and fall transition time	t_T	3	50	3	50	3	50	ns	(Notes 2, 3)
$\overline{RAS}$ precharge time	t_{RP}	70		90		90		ns	
$\overline{RAS}$ pulse width	t_{RAS}	80	10000	100	10000	120	10000	ns	
$\overline{RAS}$ hold time	t_{RSH}	40		50		60		ns	
$\overline{CAS}$ pulse width	t_{CAS}	40	10000	50	10000	60	10000	ns	
$\overline{CAS}$ hold time	t_{CSH}	80		100		120		ns	
$\overline{RAS}$ to $\overline{CAS}$ delay time	t_{RCD}	20	40	20	50	25	60	ns	(Note 11)
$\overline{CAS}$ to $\overline{RAS}$ precharge time	t_{CRP}	10		10		10		ns	(Note 12)
$\overline{CAS}$ precharge time for nonpage cycle	t_{CPN}	25		25		25		ns	
$\overline{CAS}$ precharge time for page cycle	t_{CP}	30		40		50		ns	
$\overline{RAS}$ precharge $\overline{CAS}$ hold time	t_{RPC}	0		0		0		ns	
Row address setup time	t_{ASR}	0		0		0		ns	
Row address hold time	t_{RAH}	10		10		15		ns	
Column address setup time	t_{ASC}	0		0		0		ns	
Column address hold time	t_{CAH}	15		15		20		ns	
Column address hold time referenced to $\overline{RAS}$	t_{AR}	55		65		80		ns	

6

AC Characteristics (cont)

Parameter	Symbol	μPD41464–80 Min	μPD41464–80 Max	μPD41464–10 Min	μPD41464–10 Max	μPD41464–12 Min	μPD41464–12 Max	Unit	Test Conditions
Read command hold time referenced to $\overline{RAS}$	t_{RRH}	10		10		10		ns	(Note 13)
Read command hold time referenced to $\overline{CAS}$	t_{RCH}	0		0		0		ns	(Note 13)
Write command hold time	t_{WCH}	20		25		30		ns	
Write command hold time referenced to $\overline{RAS}$	t_{WCR}	60		75		90		ns	
Write command pulse width	t_{WP}	20		15		20		ns	
Write command to $\overline{RAS}$ lead time	t_{RWL}	30		35		40		ns	
Write command to $\overline{CAS}$ lead time	t_{CWL}	30		35		40		ns	
Data-in setup time	t_{DS}	0		0		0		ns	(Note 14)
Data-in hold time	t_{DH}	20		25		30		ns	(Note 14)
Data-in hold time referenced to $\overline{RAS}$	t_{DHR}	60		75		90		ns	
Write command setup time	t_{WCS}	0		0		0		ns	(Note 15)
$\overline{RAS}$ to $\overline{WE}$ delay	t_{RWD}	105		130		155		ns	(Note 15)
$\overline{CAS}$ to $\overline{WE}$ delay	t_{CWD}	65		80		95		ns	(Note 15)
Access time from $\overline{OE}$	t_{OEA}		20		25		30	ns	
Data delay time	t_{OED}	20		25		30		ns	
$\overline{OE}$ command hold time	t_{OEH}	0		0		0		ns	
Output turnoff delay from $\overline{OE}$	t_{OEZ}	0	20	0	25	0	30	ns	
$\overline{OE}$ to $\overline{RAS}$ inactive setup time	t_{OES}	10		10		10		ns	
Read or write cycle time for counter test cycle	t_{TRC}	185		220		245		ns	(Note 16)
Read or write cycle time for counter test cycle	t_{TRWC}	245		290		325		ns	(Note 16)
$\overline{CAS}$ setup time for $\overline{CAS}$ before $\overline{RAS}$ refresh cycle	t_{CSR}	10		10		10		ns	
$\overline{CAS}$ hold time for$\overline{CAS}$ before $\overline{RAS}$ refresh cycle	t_{CHR}	15		20		25		ns	

Notes:

(1) An initial pause of 100 μs ($\overline{RAS}$ inactive) is required after power-up, followed by any eight $\overline{RAS}$ cycles, before proper device operation is achieved.

(2) AC measurements assume t_T = 5 ns.

(3) V_{IH} (min) and V_{IL} (max) are reference levels for measuring the timing of input signals.

(4) All voltages are referenced to GND.

(5) I_{CC1}, I_{CC3}, I_{CC4}, and I_{CC5} depend on output loading and cycle rates. Specified values are obtained with the output open. For lot code K of the μPD41464-15, t_{RC} (min) must be 270 ns and I_{CC3} = 60 mA.

(6) The minimum specifications are used only to indicate the cycle time at which proper operation over the full temperature range (T_A = 0 to +70°C) is assured. For lot code K of the μPD41464-15, t_{RC} (min) must be 270 ns.

(7) Load = 2 TTL loads and 100 pF

(8) Assumes that $t_{RCD} \leq t_{RCD}$ (max). If t_{RCD} is greater than the maximum recommended value in this table, t_{RAC} increases by the amount that t_{RCD} exceeds the value shown. For a $\overline{CAS}$ before $\overline{RAS}$ refresh counter test cycle, t_{RAC} is specified as $t_{RAC} = t_{CHR} + t_{CP} + t_{CAC} + 2t_T$ and is greater than the maximum specified value shown in this table.

(9) Assumes that $t_{RCD} \geq t_{RCD}$ (max).

(10) t_{OFF} (max) and t_{OEZ} (max) define the time at which the output achieves the open-circuit condition and are not referenced to V_{OH} or V_{OL}.

(11) Operation within the t_{RCD} (max) limit assures that t_{RAC} (max) can be met. t_{RCD} (max) is specified as a reference point only; if t_{RCD} is greater than t_{RCD} (max), access time is controlled exclusively by t_{CAC}.

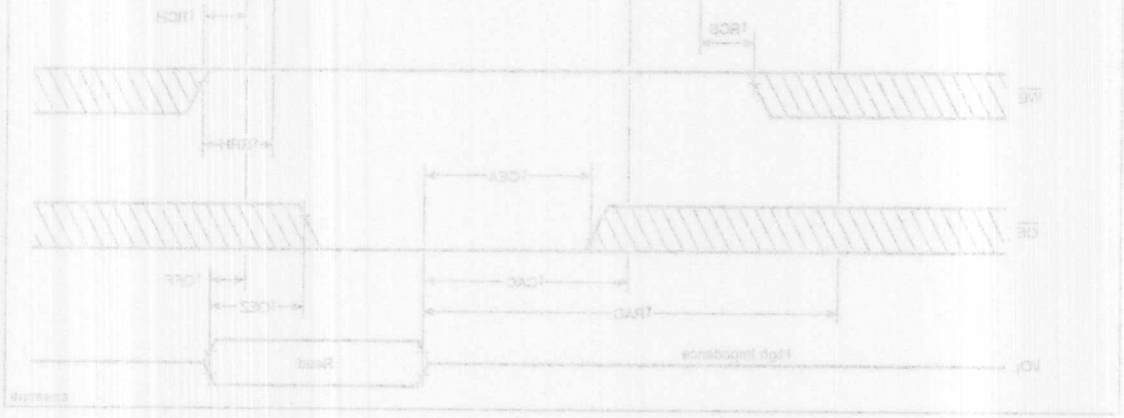
(12) The t_{CRP} requirement should be applicable for $\overline{RAS}$/$\overline{CAS}$ cycles preceded by any cycle.

(13) Either t_{RRH} or t_{RCH} must be satisfied for a read cycle.

(14) These parameters are referenced to the leading edge of $\overline{CAS}$ for early write cycles and to the leading edge of $\overline{WE}$ for delayed write or read-modify-write cycles.

(15) t_{WCS}, t_{CWD}, and t_{RWD} are restrictive operating parameters in read-write/read-modify-write cycles only. If $t_{WCS} \geq t_{WCS}$ (min), the cycle is an early write cycle and the data I/O pins will remain high impedance throughout the entire cycle. If $t_{CWD} \geq t_{CWD}$ (min), $t_{RWD} \geq t_{RWD}$ (min), the cycle is a read-write cycle and the data I/O pins will contain data read from the selected cell. If neither of the above conditions is met, the condition of the data I/O pins (at access time and until $\overline{CAS}$ returns to V_{IH}) is indeterminate.

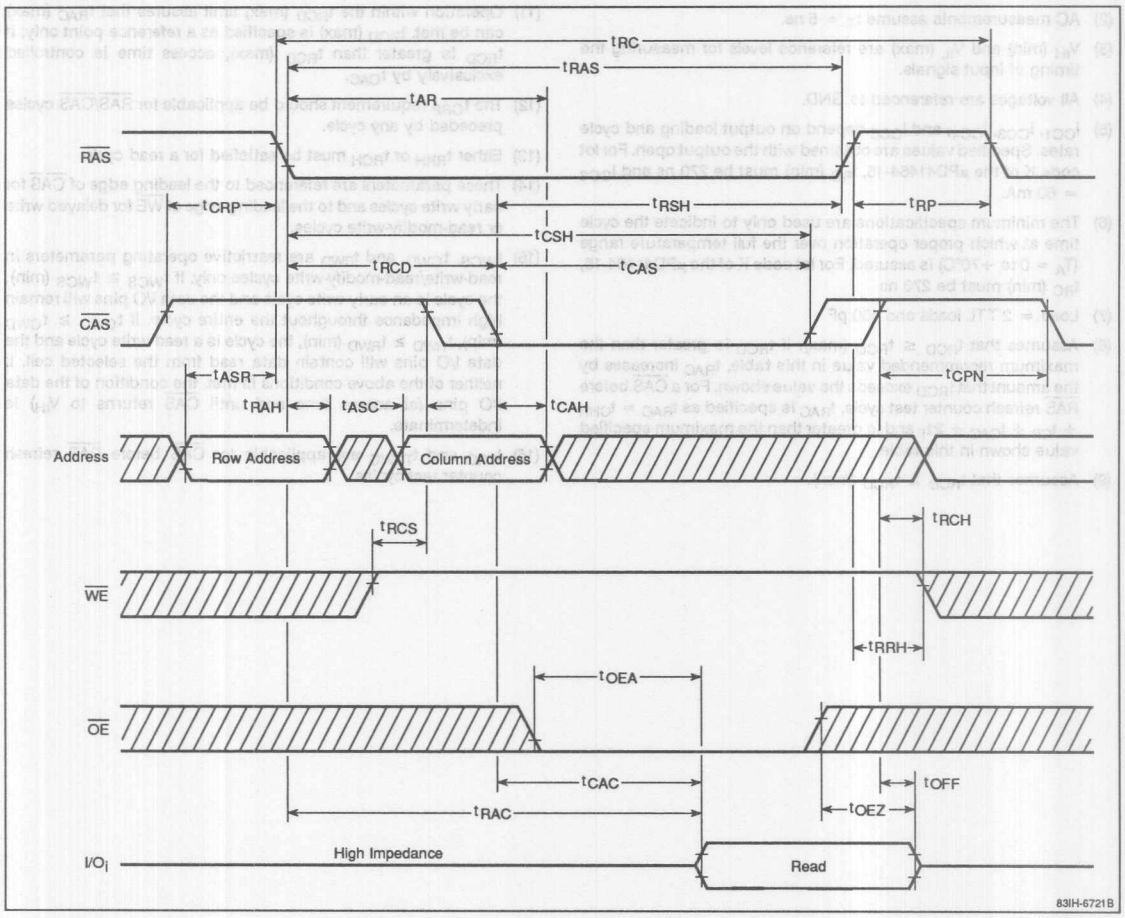
(16) t_{TRC} and t_{TRWC} are applicable for $\overline{CAS}$ before $\overline{RAS}$ refresh counter test cycles.



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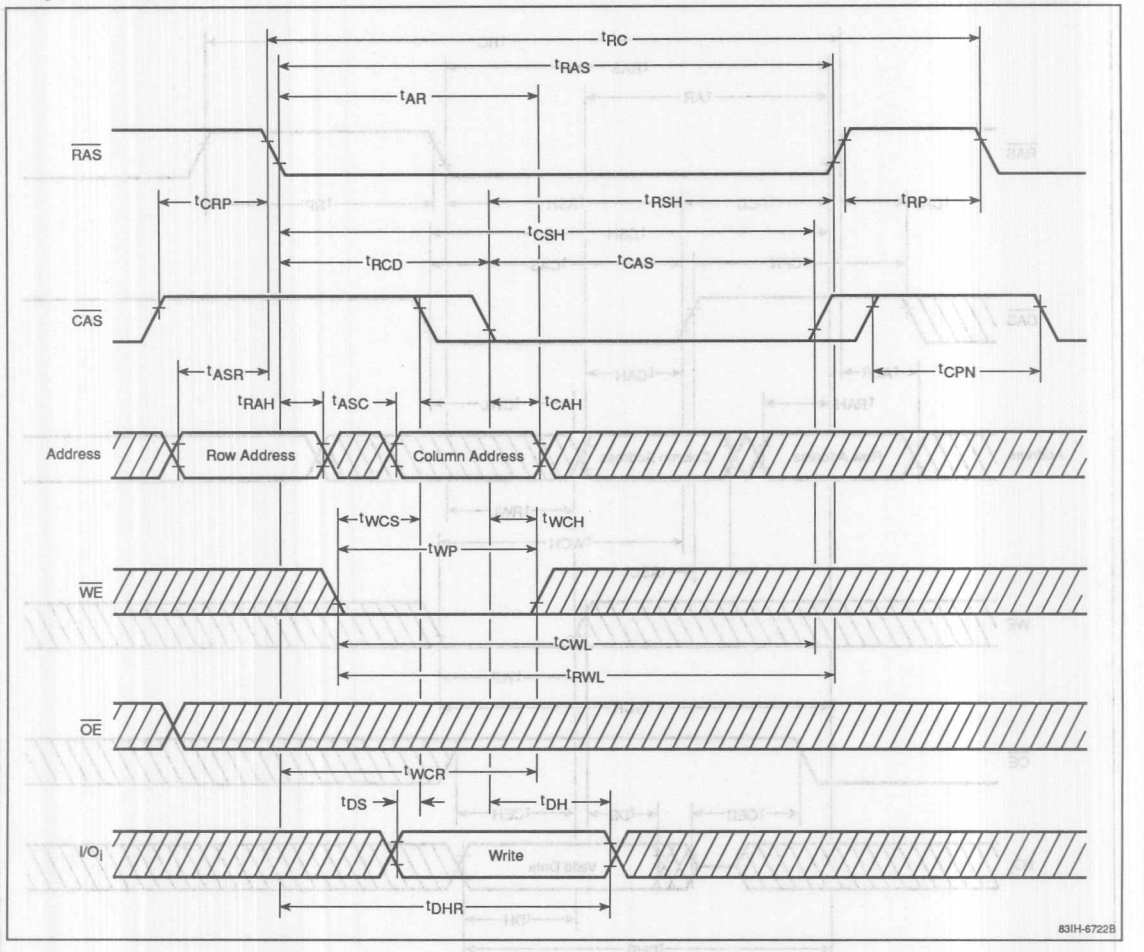
Timing Waveforms

Read Cycle



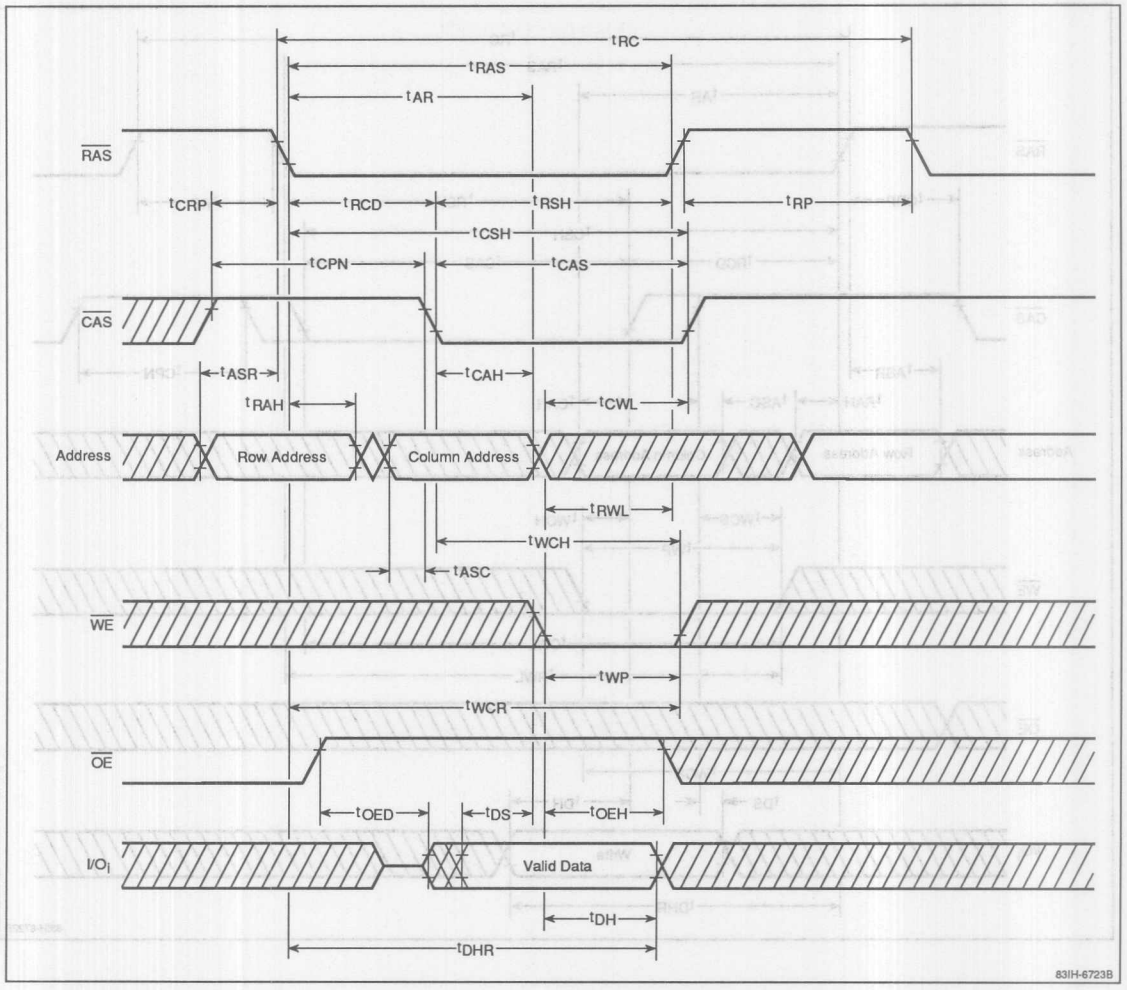
Timing Waveforms (cont)

Early Write Cycle



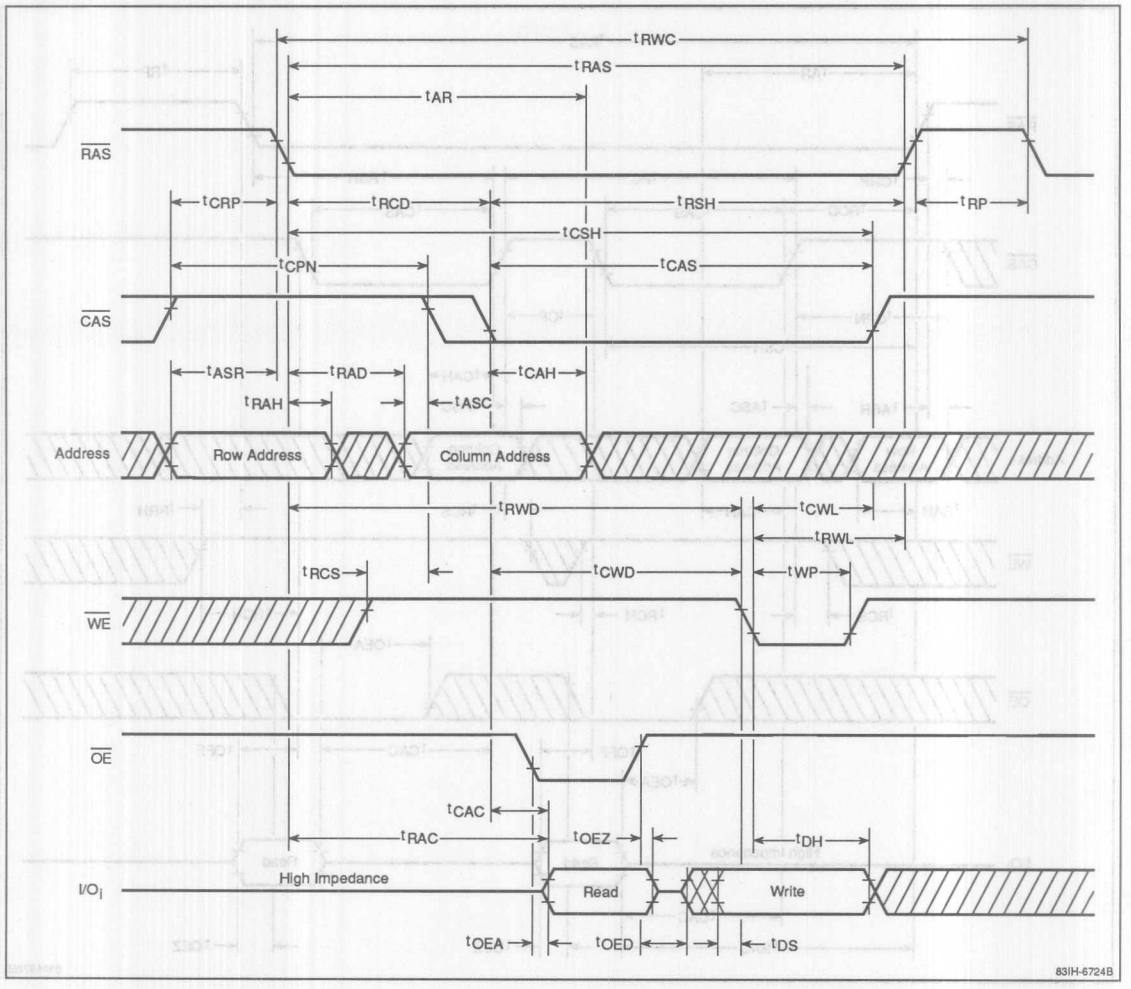
Timing Waveforms (cont)

$\overline{OE}$-Controlled Write Cycle



Timing Waveforms (cont)

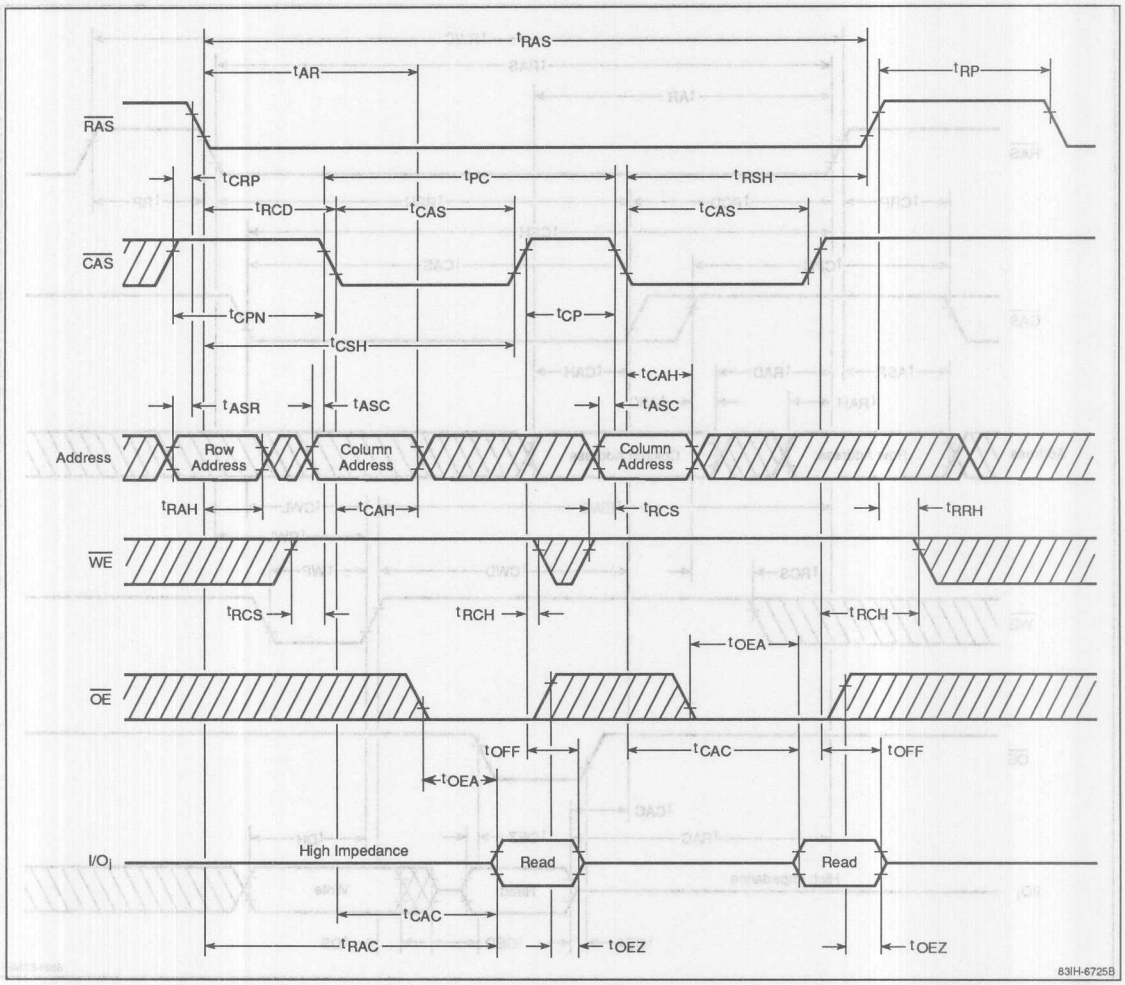
Read-Write/Read-Modify-Write Cycle



6

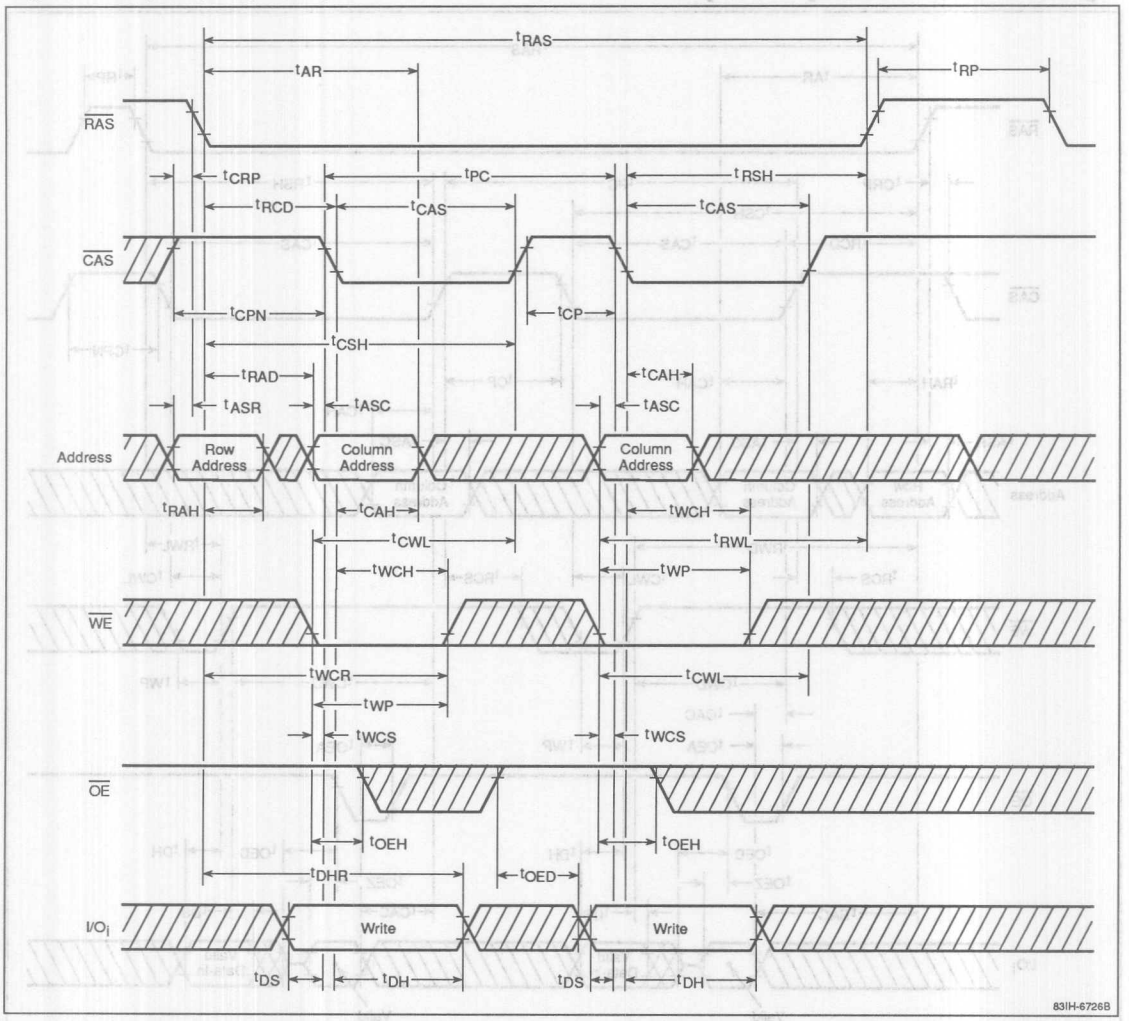
Timing Waveforms (cont)

Page Read Cycle



Timing Waveforms (cont)

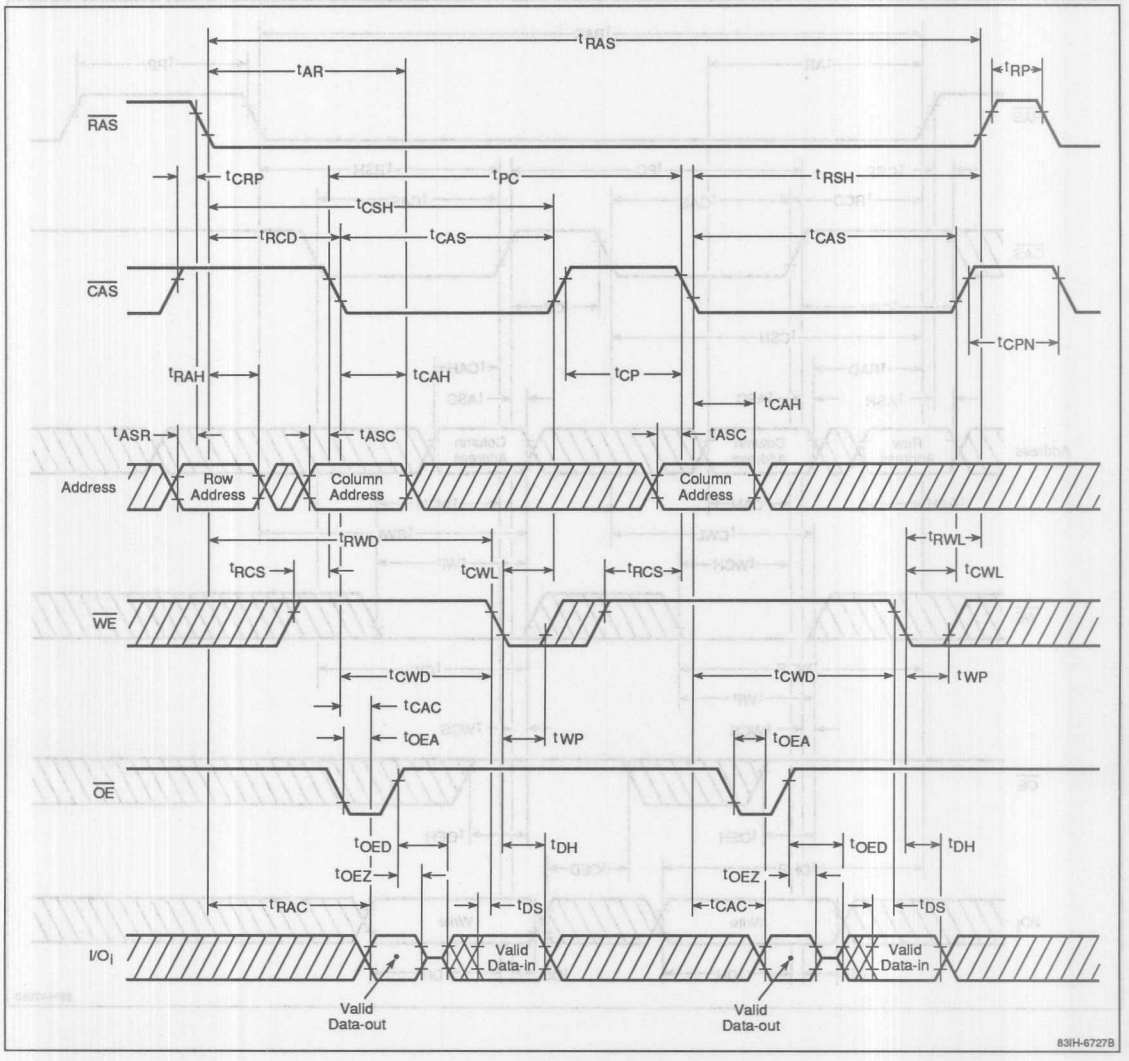
Page Write Cycle (Early Write)



6

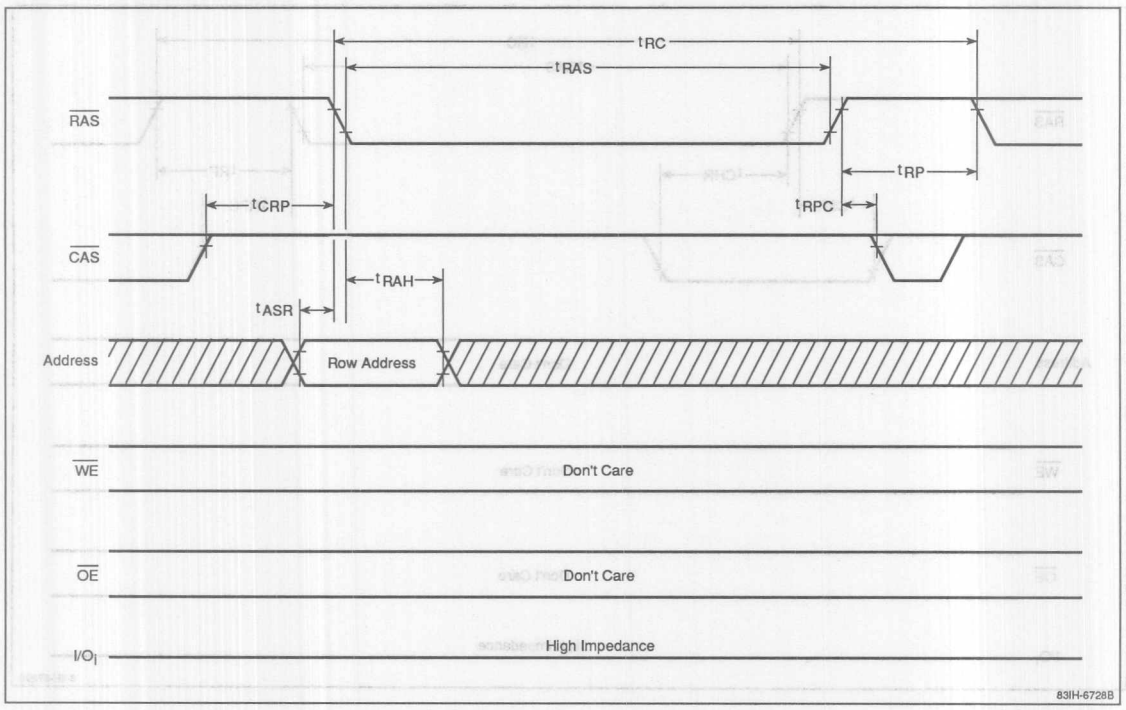
Timing Waveforms (cont)

Page Read-Write/Read-Modify-Write Cycle



Timing Waveforms (cont)

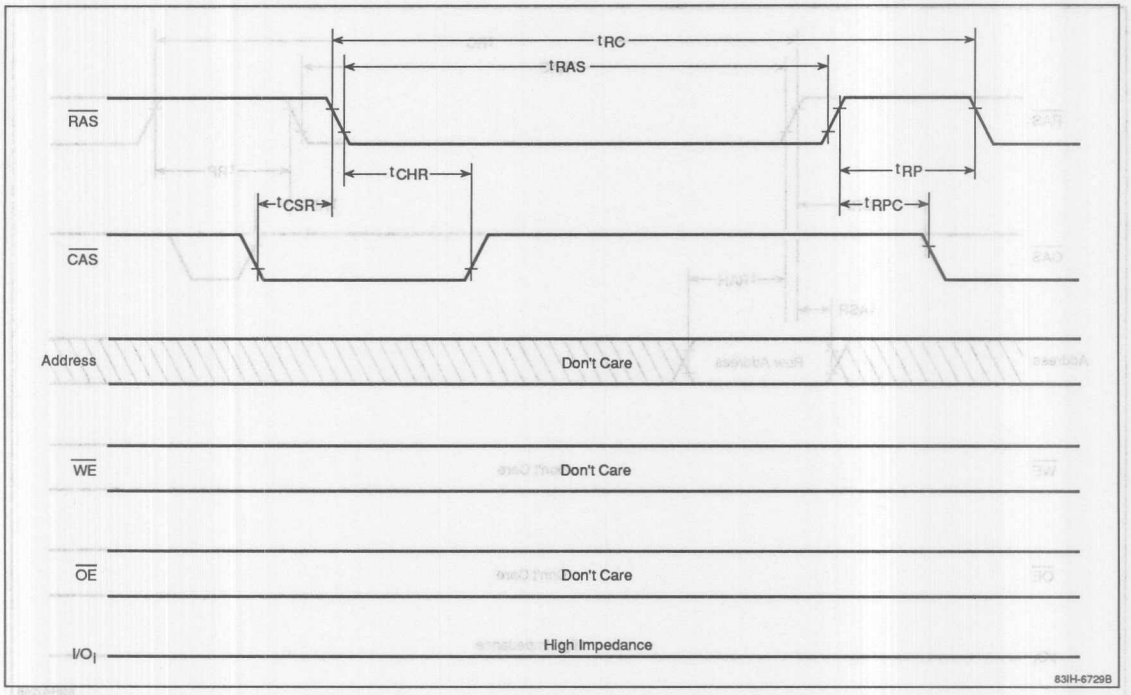
$\overline{RAS}$-Only Refresh Cycle



6

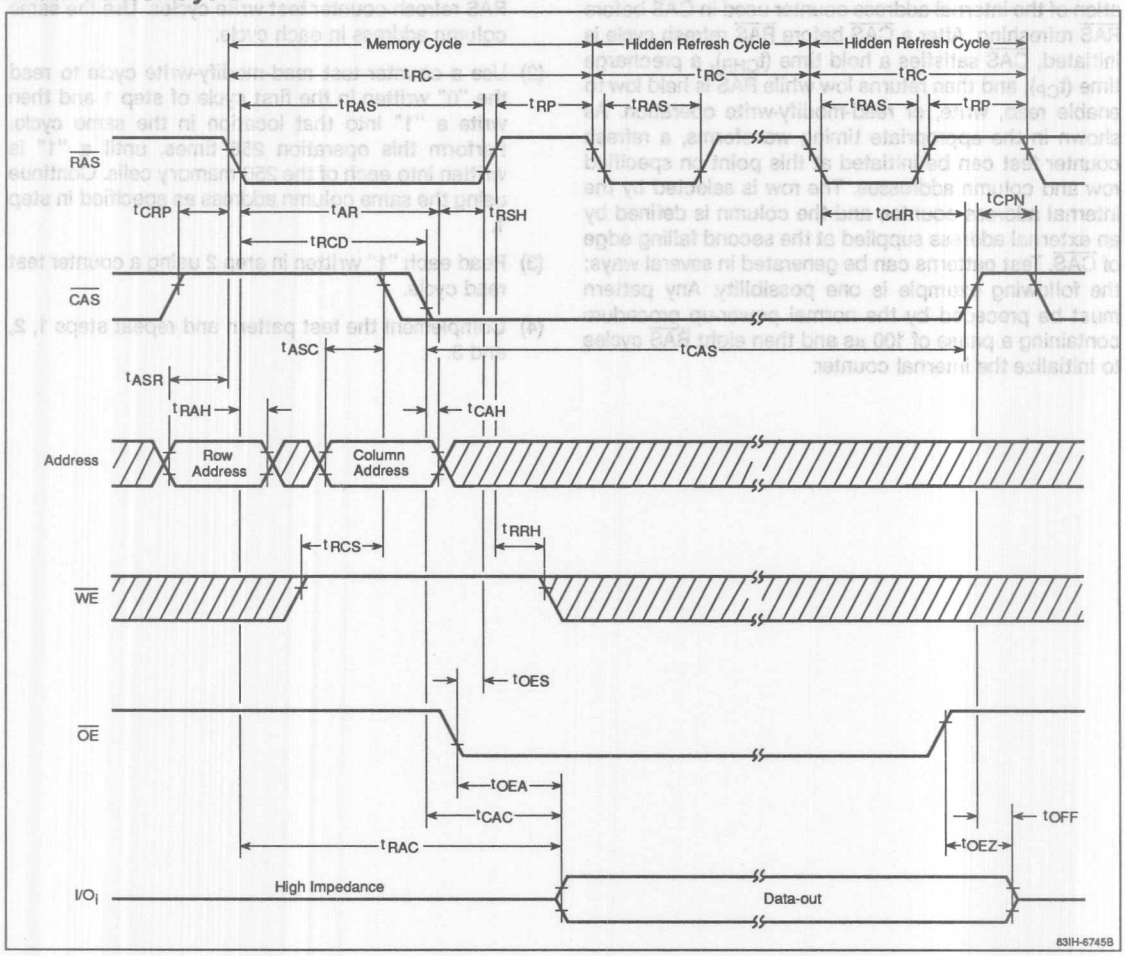
Timing Waveforms (cont)

$\overline{CAS}$ Before $\overline{RAS}$ Refresh Cycle



Timing Waveforms (cont)

Hidden Refresh Cycle



6

$\overline{CAS}$ Before $\overline{RAS}$ Refresh Counter Test

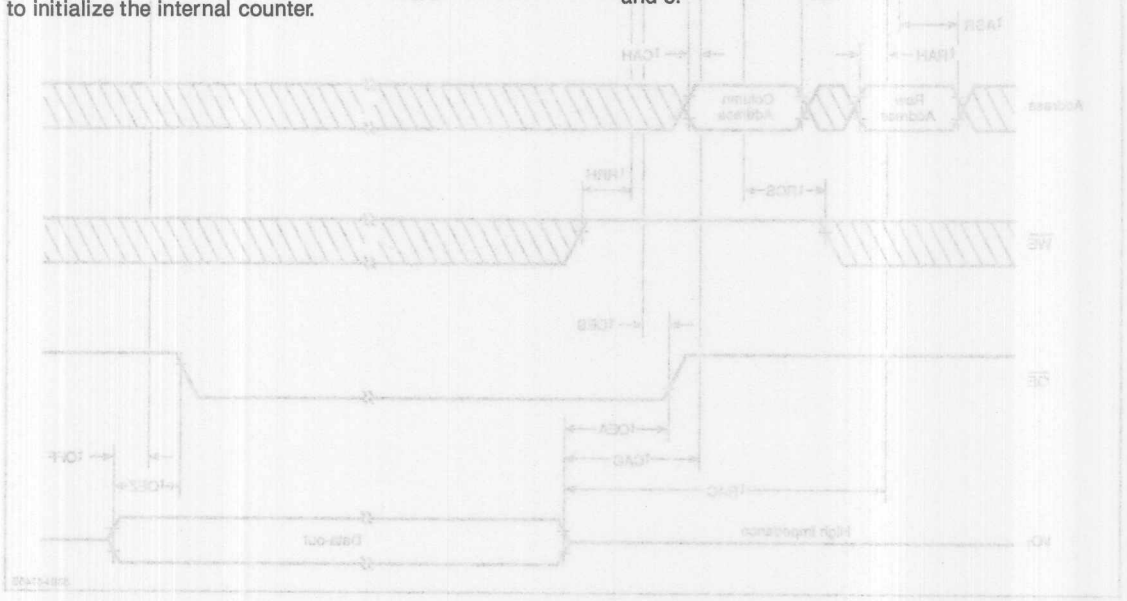
The μPD41464 provides a method to verify proper operation of the internal address counter used in $\overline{CAS}$ before $\overline{RAS}$ refreshing. After a $\overline{CAS}$ before $\overline{RAS}$ refresh cycle is initiated, $\overline{CAS}$ satisfies a hold time (t_{CHR}), a precharge time (t_{CP}), and then returns low while $\overline{RAS}$ is held low to enable read, write, or read-modify-write operation. As shown in the appropriate timing waveforms, a refresh counter test can be initiated at this point on specified row and column addresses. The row is selected by the internal address counter, and the column is defined by an external address supplied at the second falling edge of $\overline{CAS}$. Test patterns can be generated in several ways; the following example is one possibility. Any pattern must be preceded by the normal power-up procedure containing a pause of 100 μs and then eight $\overline{RAS}$ cycles to initialize the internal counter.

(1) Write "0" into 256 memory cells with 256 $\overline{CAS}$ before $\overline{RAS}$ refresh counter test write cycles. Use the same column address in each cycle.

(2) Use a counter test read-modify-write cycle to read the "0" written in the first cycle of step 1 and then write a "1" into that location in the same cycle. Perform this operation 256 times, until a "1" is written into each of the 256 memory cells. Continue using the same column address as specified in step 1.

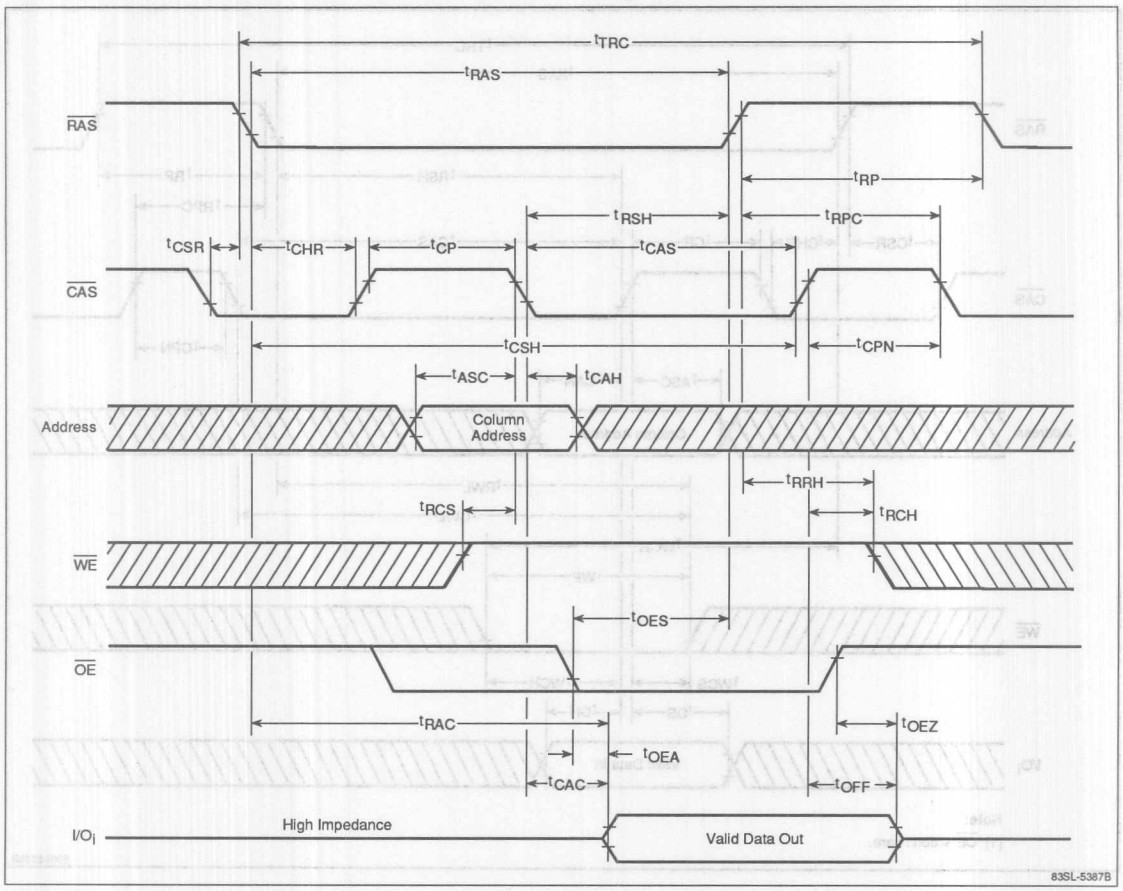
(3) Read each "1" written in step 2 using a counter test read cycle.

(4) Complement the test pattern and repeat steps 1, 2, and 3.



Timing Waveforms (cont)

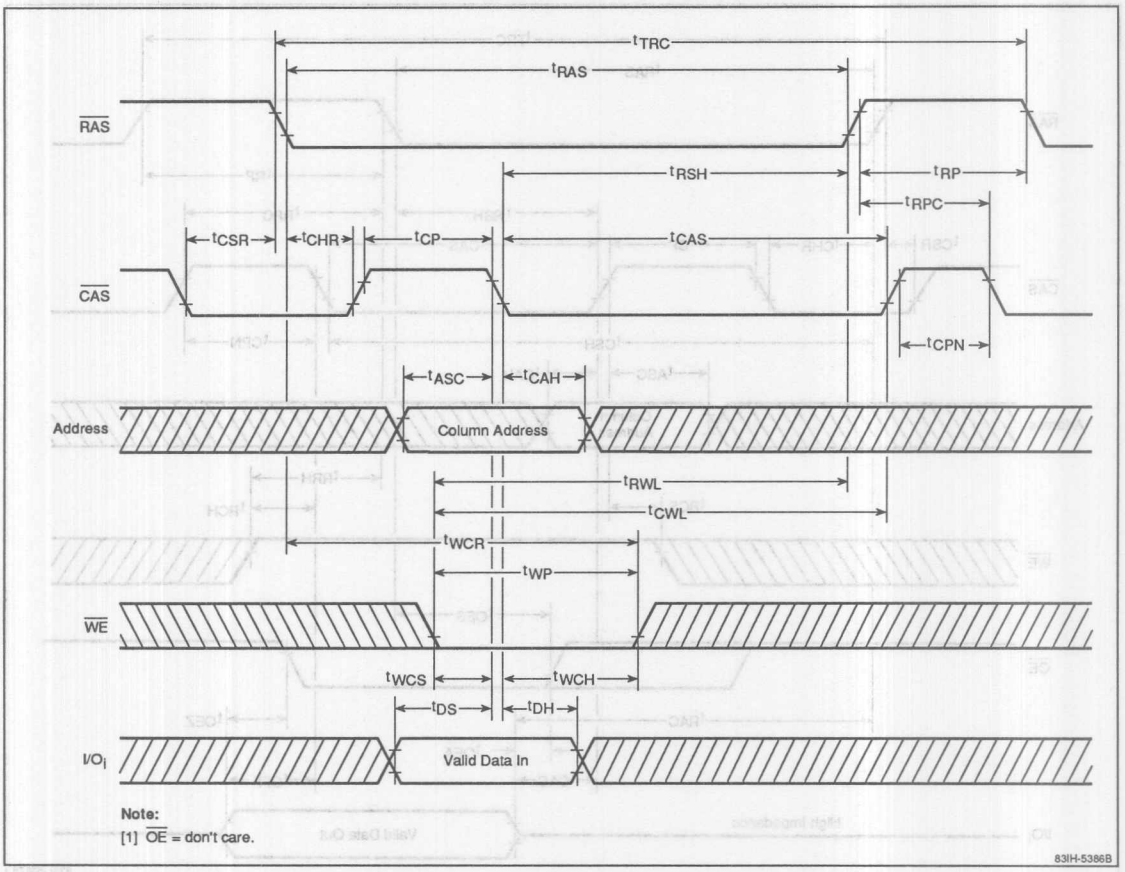
$\overline{CAS}$ Before $\overline{RAS}$ Refresh Counter Test Read Cycle



6

Timing Waveforms (cont)

$\overline{CAS}$ Before $\overline{RAS}$ Refresh Counter Test Write Cycle

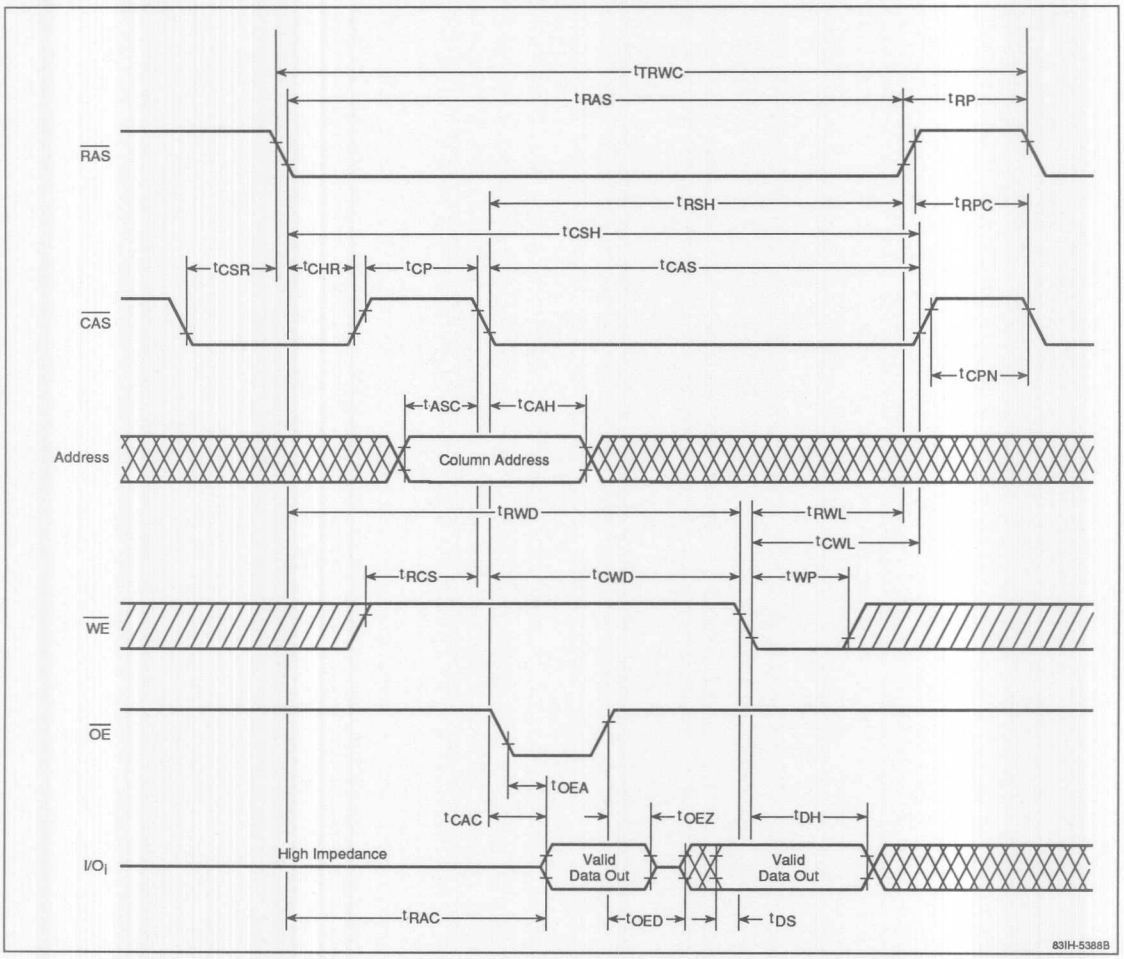


Note:
[1] $\overline{OE}$ = don't care.

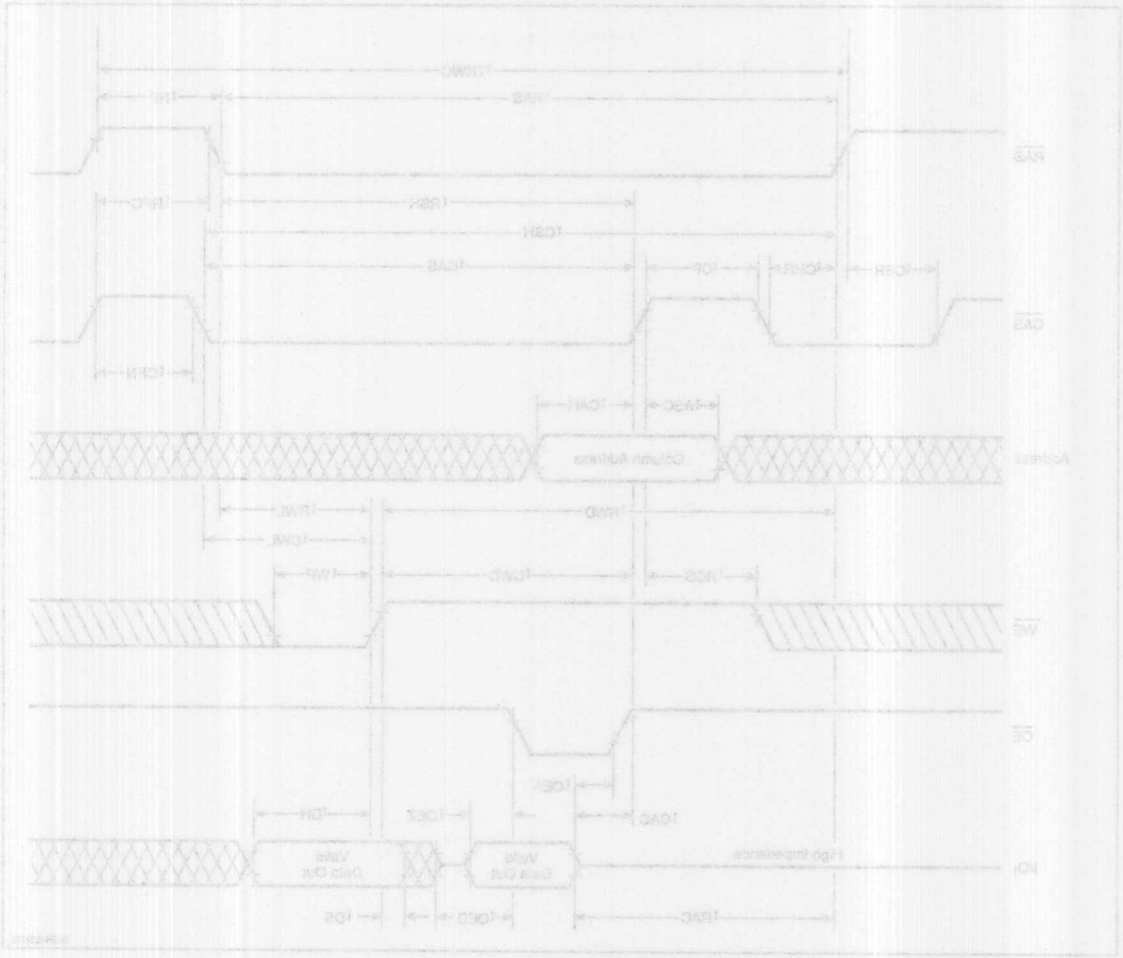
83IH-5386B

Timing Waveforms (cont)

$\overline{CAS}$ Before $\overline{RAS}$ Refresh Counter Test Read-Modify-Write Cycle



6



μPD421000
1,048,576 x 1-bit
Dynamic CMOS RAM

Description

The μPD421000 is a fast-page dynamic RAM organized as 1,048,576 words by 1 bit and designed to operate from a single +5-volt power supply. Advanced polycide technology using trench capacitors minimizes silicon area and provides high storage cell capacity, high performance, and high reliability. A single-transistor dynamic storage cell and advanced CMOS circuitry throughout ensure minimum power dissipation, while an on-chip circuit internally generates the negative-voltage substrate bias—automatically and transparently.

The three-state output is controlled by $\overline{CAS}$ independent of $\overline{RAS}$. After a valid read or read-modify-write cycle, data is held on the output by holding $\overline{CAS}$ low. The data output is returned to high impedance by returning $\overline{CAS}$ high. Fast-page read and write cycles can be executed by cycling $\overline{CAS}$.

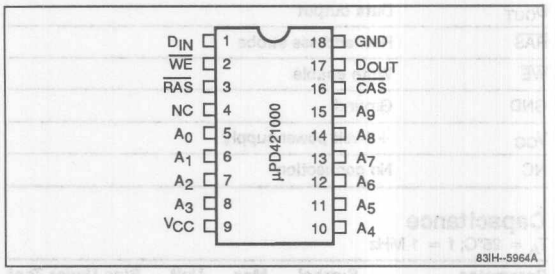
Refreshing may be accomplished by means of a $\overline{CAS}$ before $\overline{RAS}$ cycle that internally generates the refresh address. Refreshing can also be accomplished by means of $\overline{RAS}$-only refresh cycles or by normal read or write cycles on the 512 address combinations of A_0 through A_8 during an 8-ms refresh period.

Features

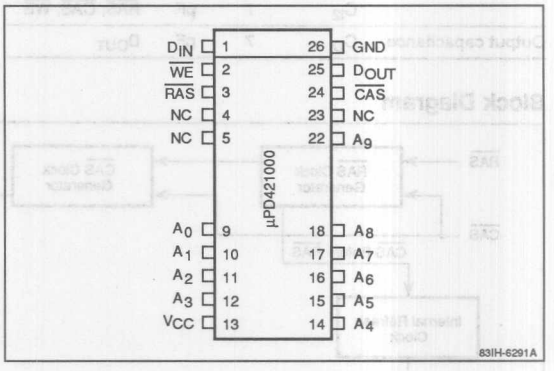
- 1,048,576-word by 1-bit organization
- Single +5-volt ±10% power supply
- Fast-page option
- $\overline{CAS}$ before $\overline{RAS}$ refresh cycles
- Multiplexed address inputs
- On-chip substrate bias generator
- Nonlatched, three-state outputs
- Low input capacitance
- TTL-compatible inputs and outputs
- 512 refresh cycles every 8 ms
- High-density 18-pin plastic DIP, 26/20-pin SOJ, or 20-pin plastic ZIP packaging

Pin Configurations

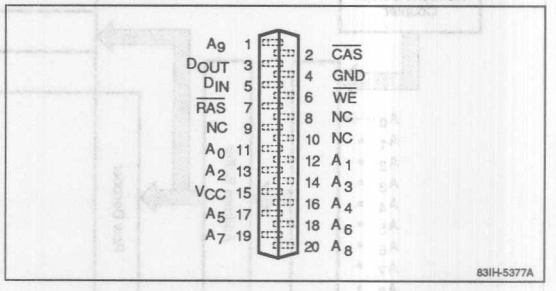
18-Pin Plastic DIP



26/20-Pin Plastic SOJ



20-Pin Plastic ZIP



6

TSOP package will be available in 1991.

Pin Identification

Name	Function
A_0 - A_9	Address inputs
$\overline{CAS}$	Column address strobe
D_{IN}	Data input
D_{OUT}	Data output
$\overline{RAS}$	Row address strobe
$\overline{WE}$	Write enable
GND	Ground
V_{CC}	+5-volt power supply
NC	No connection

Capacitance

T_A = 25°C; f = 1 MHz

Parameter	Symbol	Max	Unit	Pins Under Test
Input capacitance	C_{I1}	5	pF	Address, D_{IN}
	C_{I2}	7	pF	$\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$
Output capacitance	C_O	7	pF	D_{OUT}

Recommended Operating Conditions

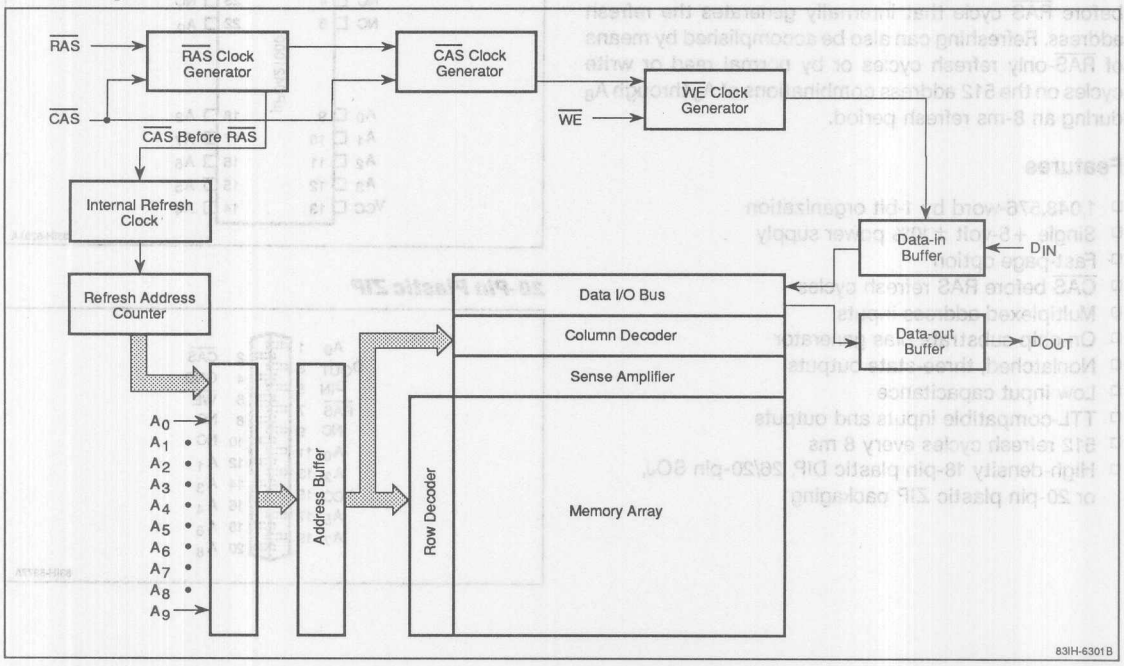
Parameter	Symbol	Min	Typ	Max	Unit
Input voltage, high	V_{IH}	2.4		V_{CC} + 1.0	V
Input voltage, low	V_{IL}	−1		0.8	V
Supply voltage	V_{CC}	4.5	5.0	5.5	V
Ambient temperature	T_A	0		70	°C

Absolute Maximum Ratings

Voltage on any pin relative to GND	−1.0 to +7.0 V
Operating temperature, T_{OPR}	0 to +70°C
Storage temperature, T_{STG}	−55 to +125°C
Short-circuit output current, I_{OS}	50 mA
Power dissipation, P_D	1.0 W

Exposure to Absolute Maximum Ratings for extended periods may affect device reliability; exceeding the ratings could cause permanent damage. The device should be operated within the limits specified under DC and AC Characteristics.

Block Diagram



Ordering Information

Part Number	$\overline{RAS}$ Access Time (max)	R/W Cycle Time (max)	Fast-Page Cycle (max)	Refresh Period	Standby Current (min)	Package
μPD421000C-60	60 ns	120 ns	40 ns	8 ms	1 mA	20-pin plastic DIP
C-70	70 ns	130 ns	45 ns			
C-80	80 ns	160 ns	50 ns			
C-10	100 ns	190 ns	60 ns			
μPD421000C-60L	60 ns	120 ns	40 ns	64 ms	200 μA	
C-70L	70 ns	130 ns	45 ns			
C-80L	80 ns	160 ns	50 ns			
C-10L	100 ns	190 ns	60 ns			
μPD421000LA-60	60 ns	120 ns	40 ns	8 ms	1 mA	26/20-pin plastic SOJ
LA-70	70 ns	130 ns	45 ns			
LA-80	80 ns	160 ns	50 ns			
LA-10	100 ns	190 ns	60 ns			
μPD421000LA-60L	60 ns	120 ns	40 ns	64 ms	200 μA	
LA-70L	70 ns	130 ns	45 ns			
LA-80L	80 ns	160 ns	50 ns			
LA-10L	100 ns	190 ns	60 ns			
μPD421000V-60	60 ns	120 ns	40 ns	8 ms	1 mA	20-pin plastic ZIP
V-70	70 ns	130 ns	45 ns			
V-80	80 ns	160 ns	50 ns			
V-10	100 ns	190 ns	60 ns			
μPD421000V-60L	60 ns	120 ns	40 ns	64 ms	200 μA	
V-70L	70 ns	130 ns	45 ns			
V-80L	80 ns	160 ns	50 ns			
V-10L	100 ns	190 ns	60 ns			

DC Characteristics

T_A = 0 to +70°C; V_{CC} = +5.0 V ±10%

Parameter	Symbol	Min	Max	Unit	Test Conditions
Standby current	I_{CC2}		2.0	mA	$\overline{RAS}$ = $\overline{CAS}$ = V_{IH}
			1.0	mA	$\overline{RAS}$ = $\overline{CAS}$ ≥ V_{CC} – 0.2 V
Input leakage current	$I_{I(L)}$	–10	10	µA	V_{IN} = 0 to 5.5 V; all other pins not under test = 0 V
Output leakage current	$I_{O(L)}$	–10	10	µA	D_{OUT} disabled; V_{OUT} = 0 to 5.5 V
Output voltage, low	V_{OL}	0	0.4	V	I_{OL} = 4.2 mA
Output voltage, high	V_{OH}	2.4	V_{CC}	V	I_{OH} = –5 mA

AC Characteristics

T_A = 0 to +70°C; V_{CC} = +5.0 V ±10%

		–60		–70		–80		–10			
Parameter	Symbol	Min	Max	Min	Max	Min	Max	Min	Max	Unit	Test Conditions
Operating current, average	I_{CC1}		90		80		70		60	mA	$\overline{RAS}$, $\overline{CAS}$ cycling; t_{RC} = t_{RC} min (Note 5)
Operating current, $\overline{RAS}$-only refresh cycle, average	I_{CC3}		90		80		70		60	mA	$\overline{RAS}$ cycling; $\overline{CAS}$ = V_{IH}; t_{RC} = t_{RC} min (Note 5)
Operating current, fast-page cycle, average	I_{CC4}		80		70		60		50	mA	$\overline{RAS}$ = V_{IL}; $\overline{CAS}$ cycling; t_{PC} = t_{PC} min (Note 5)
Operating current, $\overline{CAS}$ before $\overline{RAS}$ refresh cycle, average	I_{CC5}		90		80		70		60	mA	$\overline{RAS}$ cycling; $\overline{CAS}$ before $\overline{RAS}$; t_{RC} = t_{RC} min (Note 5)
Access time from column address	t_{AA}		30		35		45		50	ns	(Notes 7, 10, 13)
Access time from $\overline{CAS}$ precharge (rising edge)	t_{ACP}		35		40		45		55	ns	(Notes 7, 13)
Column address hold time referenced to $\overline{RAS}$	t_{AR}	N/A		N/A		60		70		ns	(Note 19)
Column address setup time	t_{ASC}	0		0		0	20	0	20	ns	(Note 13)
Row address setup time	t_{ASR}	0		0		0		0		ns	
Column address to $\overline{WE}$ delay time	t_{AWD}	30		35		45		50		ns	(Note 18)
Access time from $\overline{CAS}$ (falling edge)	t_{CAC}		20		20		20		25	ns	(Notes 7, 9, 10, 13)
Column address hold time	t_{CAH}	15		17		20		20		ns	
$\overline{CAS}$ pulse width	t_{CAS}	20	10,000	20	10,000	20	10,000	25	10,000	ns	
$\overline{CAS}$ hold time for $\overline{CAS}$ before $\overline{RAS}$ refresh cycle	t_{CHR}	15		15		15		20		ns	
$\overline{CAS}$ precharge time, fast-page cycle	t_{CP}	10		10		10	20	10	25	ns	(Note 13)
$\overline{CAS}$ precharge time, nonpage cycle	t_{CPN}	10		10		10		10		ns	
$\overline{CAS}$ to $\overline{RAS}$ precharge time	t_{CRP}	10		10		10		10		ns	(Note 14)

AC Characteristics (cont)

Parameter	Symbol	-60 Min	-60 Max	-70 Min	-70 Max	-80 Min	-80 Max	-10 Min	-10 Max	Unit	Test Conditions
$\overline{CAS}$ hold time	t_{CSH}	60		70		80		100		ns	
$\overline{CAS}$ setup time for $\overline{CAS}$ before $\overline{RAS}$ refresh cycle	t_{CSR}	10		10		10		10		ns	
$\overline{CAS}$ to $\overline{WE}$ delay	t_{CWD}	20		20		20		25		ns	(Note 18)
Write command to $\overline{CAS}$ lead time	t_{CWL}	15		15		15		20		ns	
Data-in hold time	t_{DH}	15		15		20		20		ns	(Note 17)
Data-in hold time referenced to $\overline{RAS}$	t_{DHR}	N/A		N/A		60		70		ns	(Note 19)
Data-in setup time	t_{DS}	0		0		0		0		ns	(Note 17)
Output buffer turnoff delay	t_{OFF}	0	15	0	15	0	20	0	25	ns	(Note 11)
Fast-page cycle time	t_{PC}	40		45		50		60		ns	(Note 6)
Access time from $\overline{RAS}$	t_{RAC}		60		70		80		100	ns	(Notes 7, 8)
$\overline{RAS}$ to column address delay time	t_{RAD}	15	30	15	35	17	35	17	50	ns	(Note 10)
Row address hold time	t_{RAH}	10		10		12		12		ns	
Column address lead time referenced to $\overline{RAS}$ (rising edge)	t_{RAL}	30		35		45		50		ns	
$\overline{RAS}$ pulse width	t_{RAS}	60	10,000	70	10,000	80	10,000	100	10,000	ns	
$\overline{RAS}$ pulse width, fast-page cycle	t_{RASP}	60	10,000	70	100,000	80	100,000	100	100,000	ns	
Random read or write cycle time	t_{RC}	120		130		160		190		ns	(Note 6)
$\overline{RAS}$ to $\overline{CAS}$ delay time	t_{RCD}	20	40	20	50	25	60	25	75	ns	(Note 12)
Read command hold time referenced to $\overline{CAS}$	t_{RCH}	0		0		0		0		ns	(Note 15)
Read command setup time	t_{RCS}	0		0		0		0		ns	
Refresh period	t_{REF}		8		8		8		8	ms	Addresses A_0 - A_8
$\overline{RAS}$ precharge time	t_{RP}	50		50		70		80		ns	
$\overline{RAS}$ precharge $\overline{CAS}$ hold time	t_{RPC}	10		10		0		0		ns	
Read command hold time referenced to $\overline{RAS}$	t_{RRH}	10		10		10		10		ns	(Note 15)
$\overline{RAS}$ hold time	t_{RSH}	20		20		20		25		ns	
Read-write cycle time	t_{RWC}	145		155		190		225		ns	(Note 6)
$\overline{RAS}$ to $\overline{WE}$ delay	t_{RWD}	60		70		80		100		ns	(Note 18)
Write command to $\overline{RAS}$ lead time	t_{RWL}	20		20		25		30		ns	
Rise and fall transition time	t_T	3	50	3	50	3	50	3	50	ns	(Note 4)
Write command hold time	t_{WCH}	15		15		15		20		ns	

AC Characteristics (cont)

Parameter	Symbol	-60 Min	-60 Max	-70 Min	-70 Max	-80 Min	-80 Max	-10 Min	-10 Max	Unit	Test Conditions
Write command hold time referenced to $\overline{RAS}$	t_{WCR}	N/A		N/A		55		70		ns	(Note 19)
Write command setup time	t_{WCS}	0		0		0		0		ns	(Note 18)
Write command pulse width	t_{WP}	15		15		15		20		ns	(Note 16)

Notes:

(1) All voltages are referenced to GND.

(2) An initial pause of 100 μs is required after power-up, followed by any eight $\overline{RAS}$ cycles, before proper device operation is achieved.

(3) AC measurements assume $t_T = 5$ ns.

(4) V_{IH} (min) and V_{IL} (max) are reference levels for measuring the timing of input signals. Transition times are measured between V_{IH} and V_{IL}.

(5) I_{CC1}, I_{CC3}, I_{CC4}, and I_{CC5} depend on output loading and cycle rates. Specified values are obtained with the output open. I_{CC3} is measured assuming that all column address inputs are held at either a high level or a low level during $\overline{RAS}$-only refresh cycles. I_{CC4} is measured assuming that all column address inputs are switched only once during each fast-page cycle.

(6) The minimum specifications are used only to indicate the cycle time at which proper operation over the full temperature range (T_A = 0 to +70°C) is assured.

(7) Load = 2 TTL (–1 mA, +4 mA) loads and 100 pF (V_{OH} = 2.0 V, V_{OL} = 0.8 V).

(8) Assumes that $t_{RCD} \leq t_{RCD}$ (max) and $t_{RAD} \leq t_{RAD}$ (max). If t_{RCD} or t_{RAD} is greater than the maximum recommended value in this table, t_{RAC} increases by the amount that t_{RCD} or t_{RAD} exceeds the value shown.

(9) Assumes that $t_{RCD} \geq t_{RCD}$ (max) and $t_{RAD} \leq t_{RAD}$ (max).

(10) If $t_{RAD} \geq t_{RAD}$ (max), then the access time is defined by t_{AA}.

(11) t_{OFF} (max) defines the time at which the output achieves the open-circuit condition and is not referenced to V_{OH} or V_{OL}.

(12) Operation within the t_{RCD} (max) limit assures that t_{RAC} (max) can be met. t_{RCD} (max) is specified as a reference point only; if t_{RCD} is greater than t_{RCD} (max), then access time is controlled exclusively by t_{CAC}.

(13) For fast-page read operation, the definition of access time is as follows:

$\overline{CAS}$ and Column Address Input Conditions	Access Time Definition
$t_{CP} \leq t_{CP}$ (max), $t_{ASC} \geq t_{CP}$	t_{ACP}
$t_{CP} \leq t_{CP}$ (max), $t_{ASC} \leq t_{CP}$	t_{AA}
$t_{CP} \geq t_{CP}$ (max), $t_{ASC} \leq t_{ASC}$ (max)	t_{AA}
$t_{CP} \geq t_{CP}$ (max), $t_{ASC} \geq t_{CP}$	t_{CAC}

(14) The t_{CRP} requirement should be applicable for $\overline{RAS}$/$\overline{CAS}$ cycles preceded by any cycle.

(15) Either t_{RRH} or t_{RCH} must be satisfied for a read cycle.

(16) Parameter t_{WP} is applicable for a delayed write cycle such as a read-write/read-modify-write cycle. For early write operation, both t_{WCS} and t_{WCH} must be met.

(17) These parameters are referenced to the falling edge of $\overline{CAS}$ for early write cycles and to the falling edge of $\overline{WE}$ for delayed write or read-modify-write cycles.

(18) t_{WCS}, t_{RWD}, t_{CWD}, and t_{AWD} are restrictive operating parameters in read-write/read-modify-write cycles only. If $t_{WCS} \geq t_{WCS}$ (min), the cycle is an early write cycle and the data output will remain open-circuit throughout the entire cycle. If $t_{CWD} \geq t_{CWD}$ (min), $t_{RWD} \geq t_{RWD}$ (min), and $t_{AWD} \geq t_{AWD}$ (min), the cycle is a read-write cycle and the data output will contain data read from the selected cell. If neither of the above conditions is met, the condition of the data output pin (at access time and until $\overline{CAS}$ returns to V_{IH}) is indeterminate.

(19) This parameter is not needed for the μPD421000-60 and μPD421000-70.

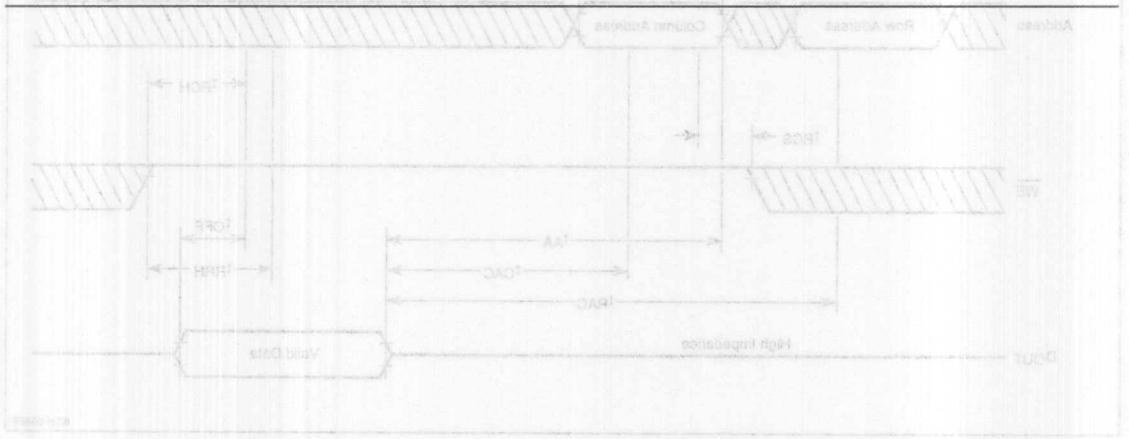
Low Power Battery Backup (-L Versions Only)

The μPD421000-L is capable of low power battery backup during times of reduced system power, when the input buffers and all nonessential internal circuits are turned off. For the input buffers to be turned off and the amount of leakage current flowing through them reduced, the μPD421000-L must be in standby and all control lines within 0.2 V of either V_{CC} or GND, as appropriate. When $\overline{RAS}$ and $\overline{CAS}$ are both within 0.2 V of V_{CC}, the internal circuits are inactive and power requirements reduced even further. Standby current can drop as low as 200 μA.

$\overline{CAS}$ before $\overline{RAS}$ refresh cycles are executed at a minimum rate to ensure that all 512 rows are refreshed only once every 64 ms. The time that $\overline{RAS}$ is low (t_{RAS}) and the μPD421000-L active needs to be as short as possible, typically less than 300 ns, to minimize power usage during refresh operation. The following table shows the conditions under which the lowest average standby current can be obtained.

Battery Backup Current

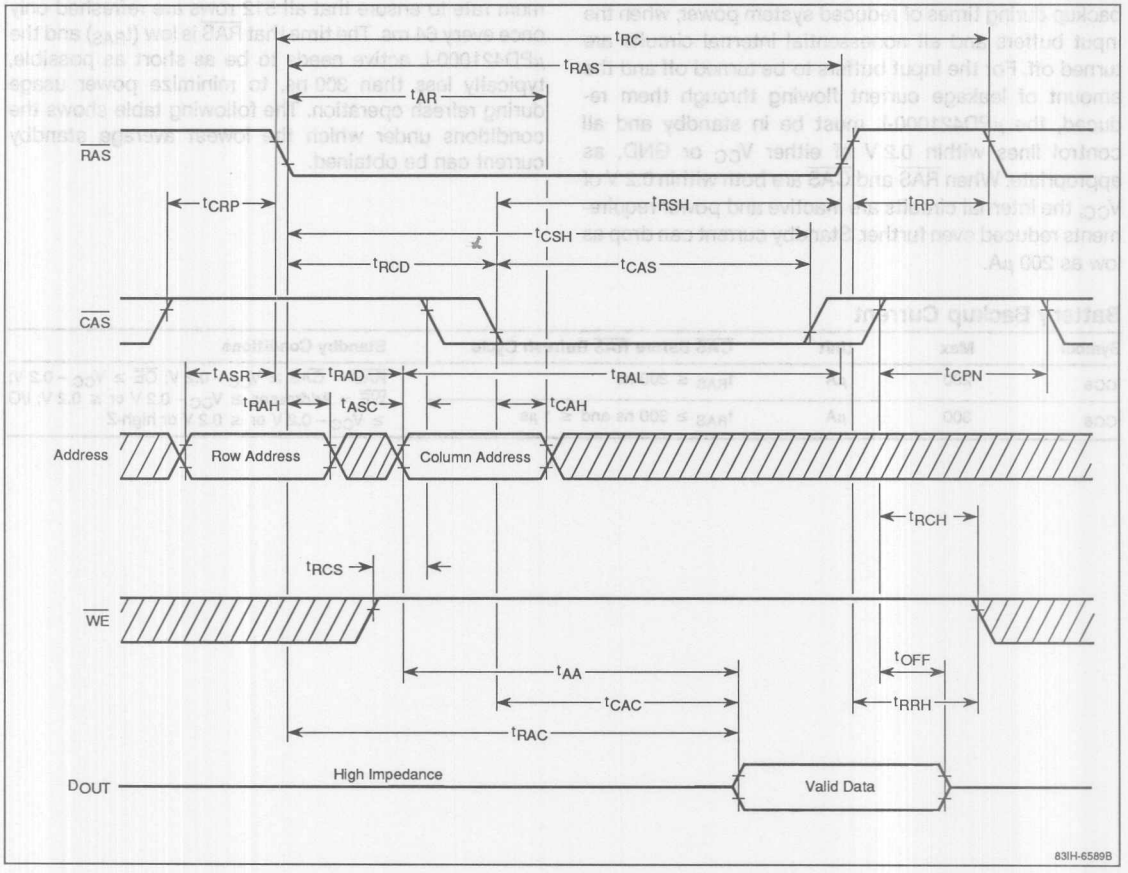
Symbol	Max	Unit	$\overline{CAS}$ Before $\overline{RAS}$ Refresh Cycle	Standby Conditions
I_{CC6}	200	μA	$t_{RAS} \leq 300$ ns	$\overline{RAS} = \overline{CAS} \geq V_{CC} - 0.2$ V; $\overline{OE} \geq V_{CC} - 0.2$ V; $\overline{WE}$ = Addresses $\geq V_{CC} - 0.2$ V or ≤ 0.2 V; I/O $\geq V_{CC} - 0.2$ V or ≤ 0.2 V or high-Z
I_{CC6}	300	μA	$t_{RAS} \geq 300$ ns and ≤ 1 μs	



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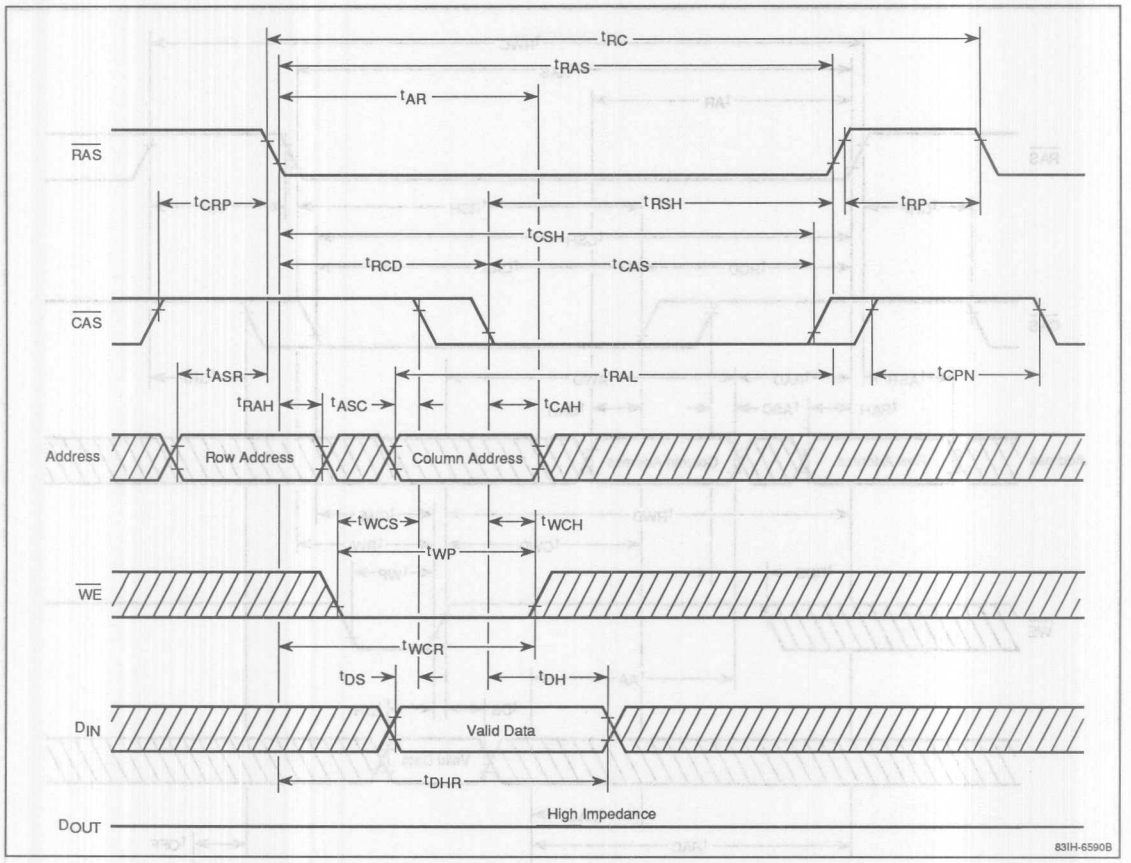
Timing Waveforms

Read Cycle



Timing Waveforms (cont)

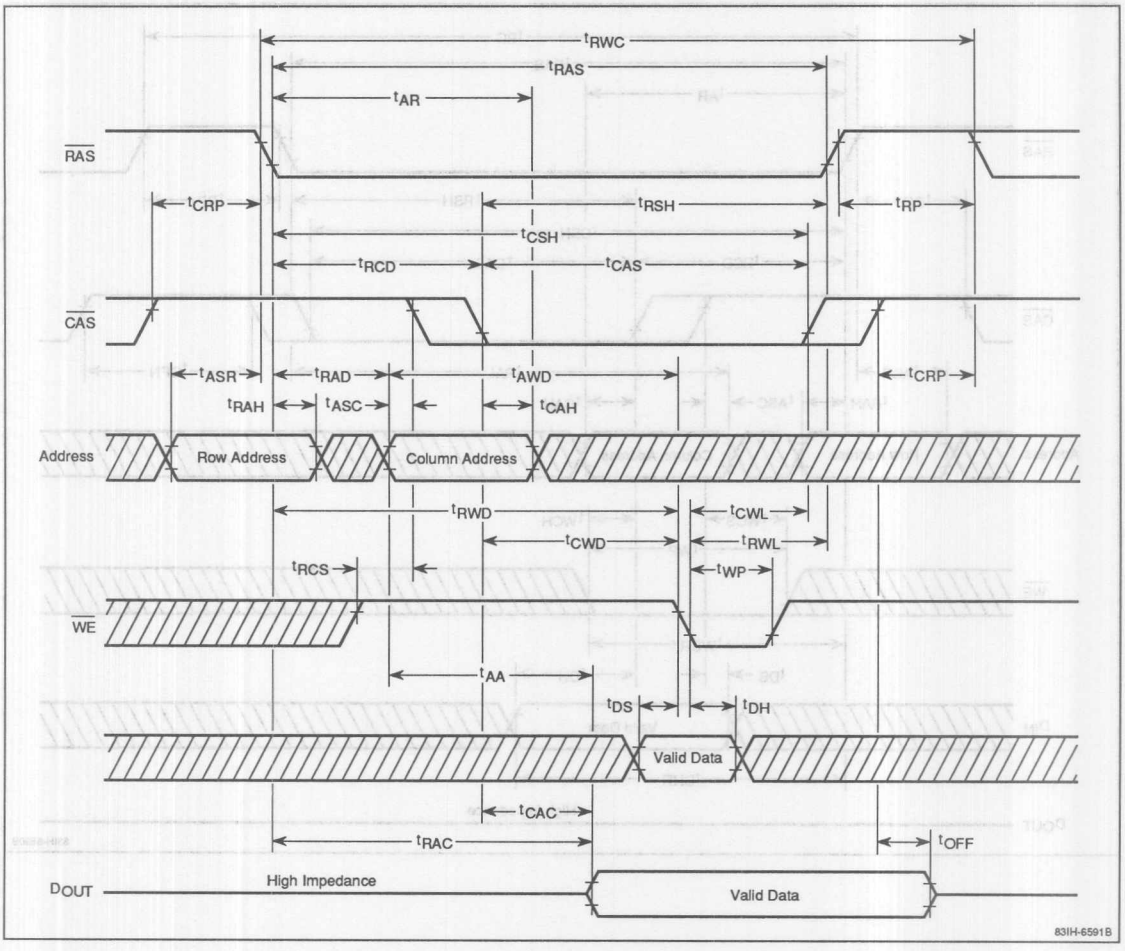
Early Write Cycle



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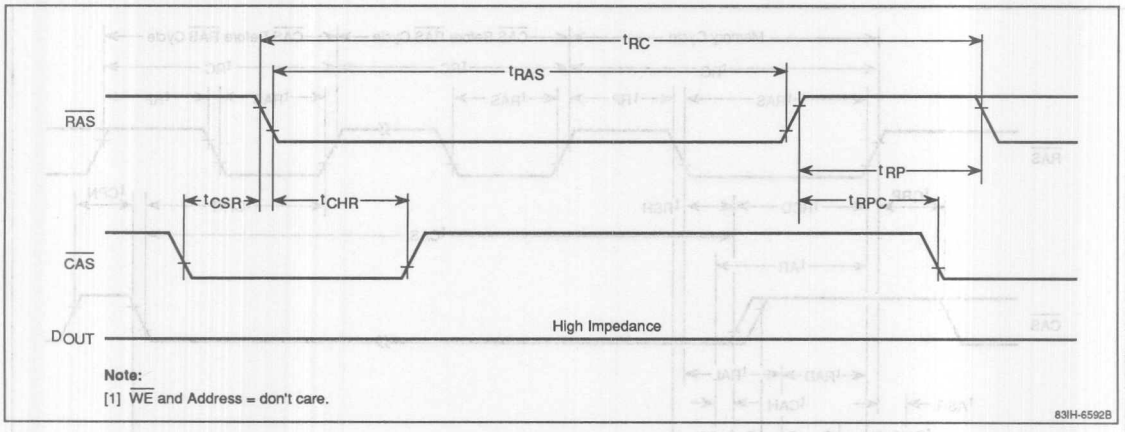
Timing Waveforms (cont)

Read-Write/Read-Modify-Write Cycle



Timing Waveforms (cont)

$\overline{CAS}$ Before $\overline{RAS}$ Refresh Cycle

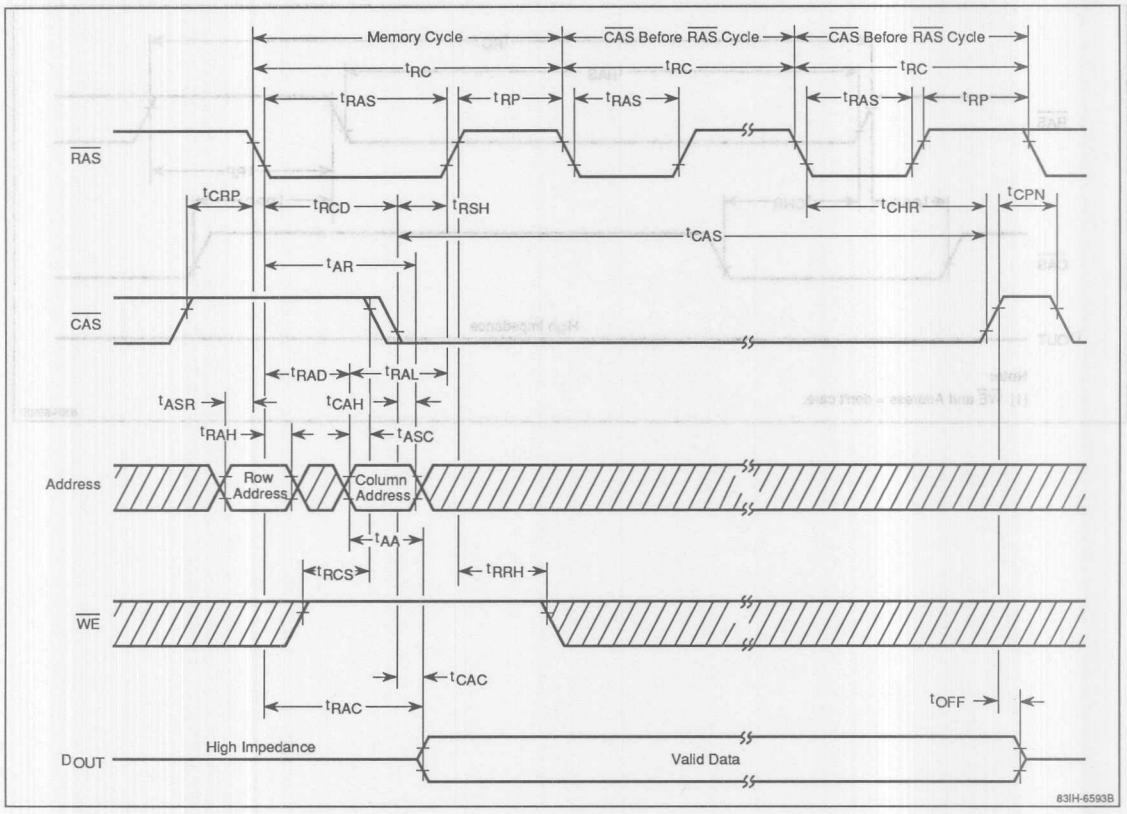


Note:
[1] $\overline{WE}$ and Address = don't care.

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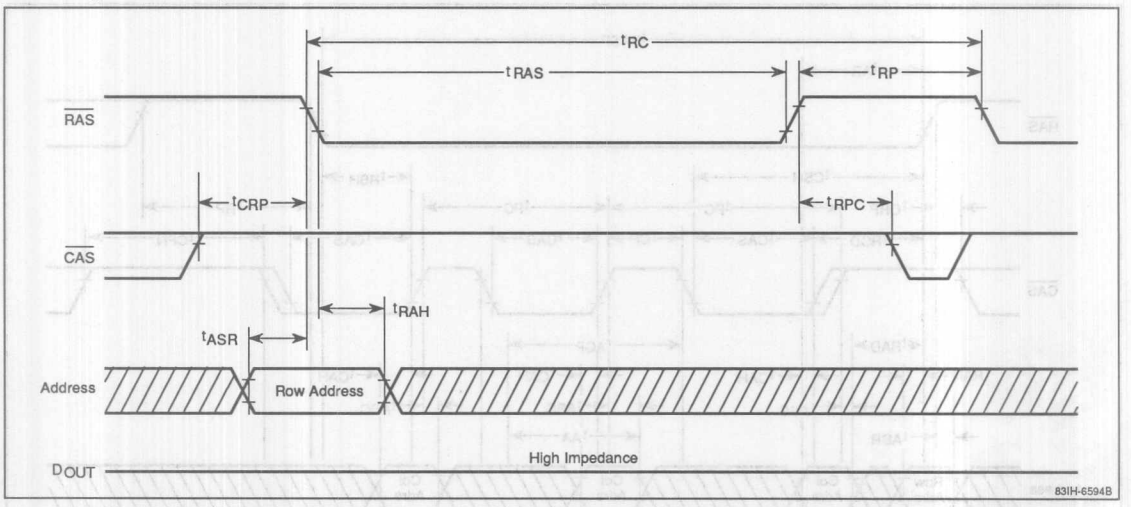
Timing Waveforms (cont)

Hidden Refresh Cycle



Timing Waveforms (cont)

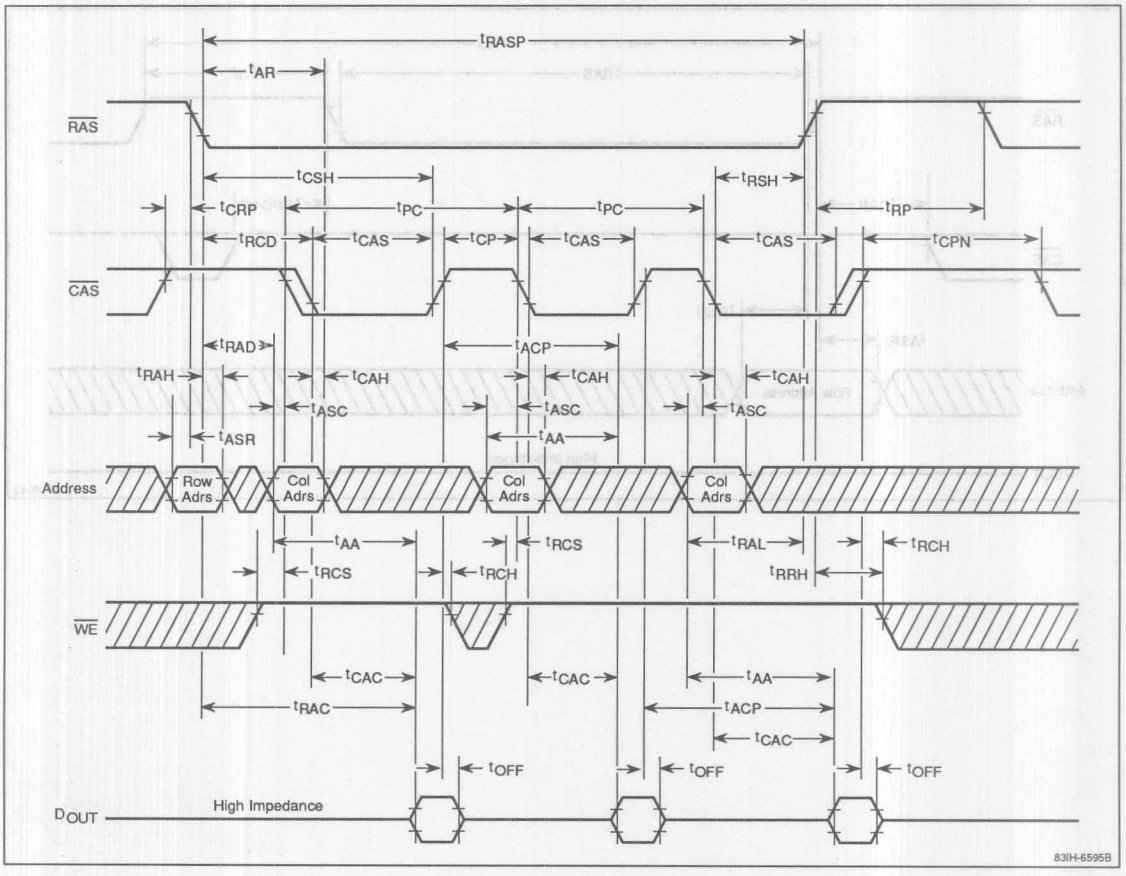
$\overline{RAS}$-Only Refresh Cycle



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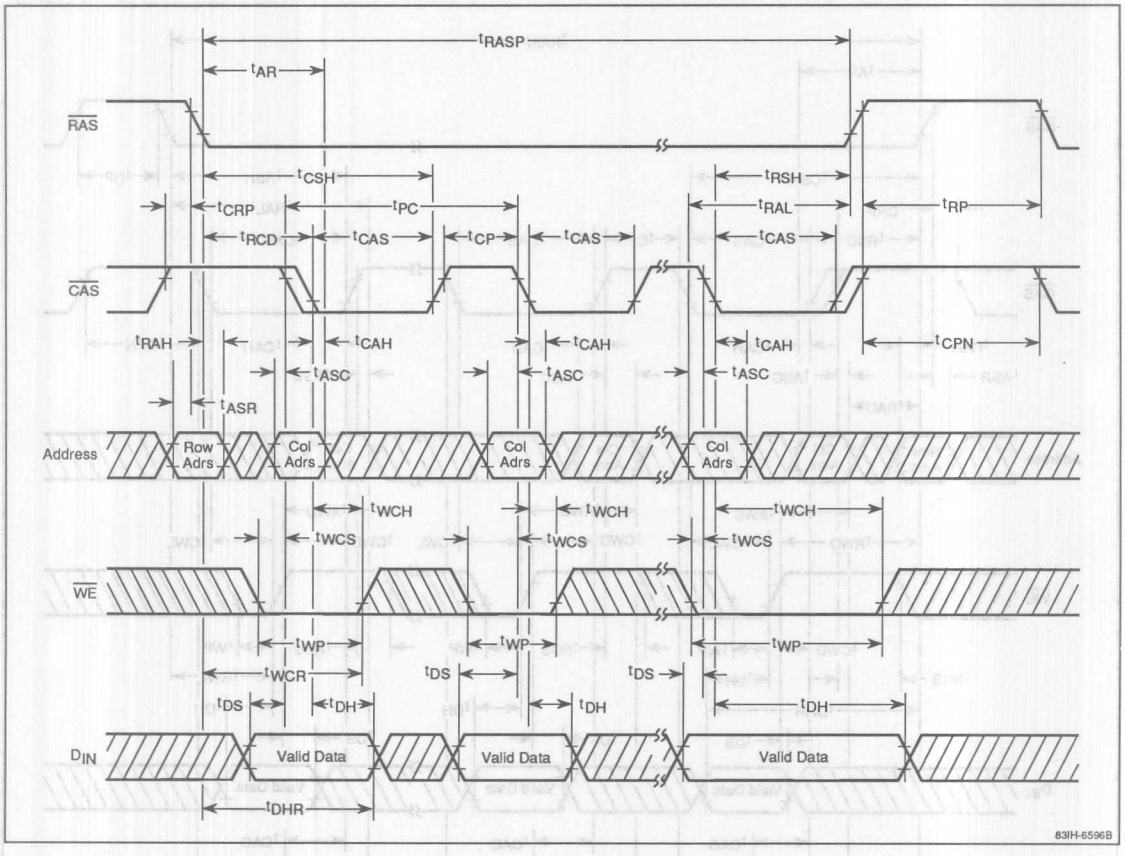
Timing Waveforms (cont)

Fast-Page Read Cycle



Timing Waveforms (cont)

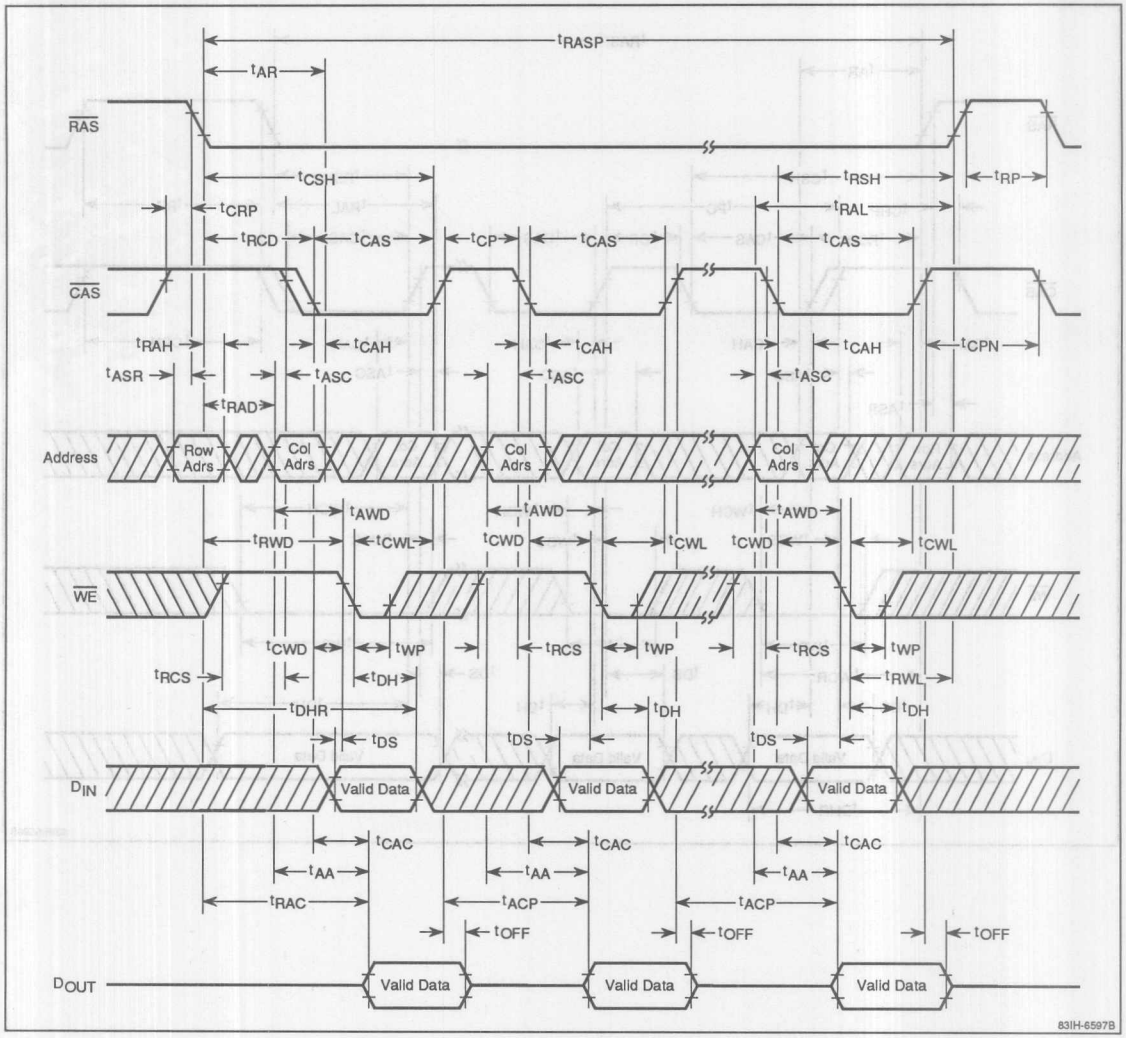
Fast-Page Early Write Cycle



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Timing Waveforms (cont)

Fast-Page Read-Write/Read-Modify-Write Cycle



μPD421001
1,048,576 x 1-Bit
Dynamic CMOS RAM

Description

The μPD421001 is a 1,048,576-word by 1-bit dynamic RAM designed with a nibble mode and to operate from a single +5-volt power supply. Advanced polycide technology using trench capacitors minimizes silicon area and provides high storage cell capacity, high performance, and high reliability. A single-transistor dynamic storage cell and advanced CMOS circuitry throughout ensure minimum power dissipation, while an on-chip circuit generates the negative-voltage substrate bias—automatically and transparently.

The three-state output is controlled by $\overline{CAS}$ independent of $\overline{RAS}$. After a valid read or read-modify-write cycle, data is held on the output by holding $\overline{CAS}$ low. Data output is returned to high impedance by returning $\overline{CAS}$ high. The device is capable of executing nibble read and write cycles by cycling $\overline{CAS}$.

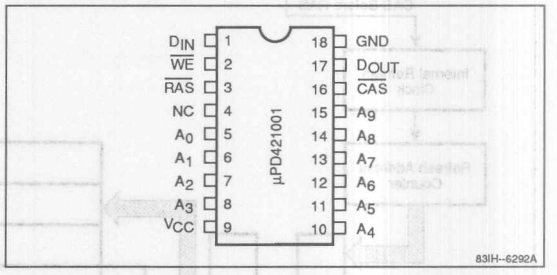
Refreshing may be accomplished by means of $\overline{CAS}$ before $\overline{RAS}$ cycles that internally generate the refresh address. Refreshing can also be accomplished by means of RAS-only refresh cycles or by normal read or write cycles on the 512 address combinations of A_0 through A_8 during an 8-ms period.

Features

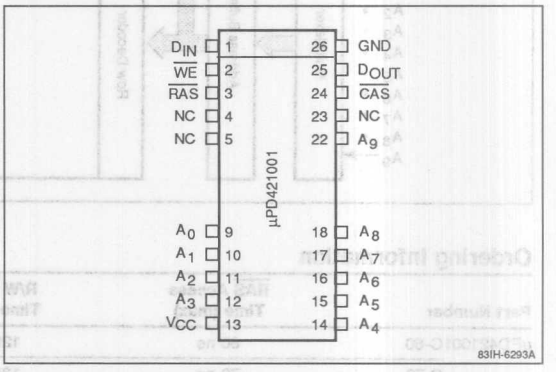
- 1,048,576-word by 1-bit organization
- Single +5-volt ±10% power supply
- Nibble option
- Low power dissipation
  - — 90 mA max (active) for 60 ns version
  - — 1 mA max (standby)
- $\overline{CAS}$ before $\overline{RAS}$ refresh cycles
- Multiplexed address inputs
- On-chip substrate bias generator
- Nonlatched, three-state outputs
- Low input capacitance
- TTL-compatible inputs and outputs
- 512 refresh cycles every 8 ms
- High-density 18-pin plastic DIP, 26/20-pin plastic SOJ, or 20-pin plastic ZIP packaging

Pin Configurations

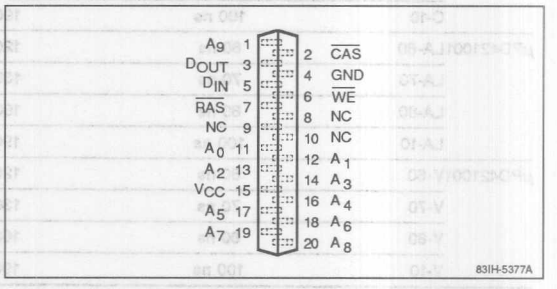
18-Pin Plastic DIP



26/20-Pin Plastic SOJ



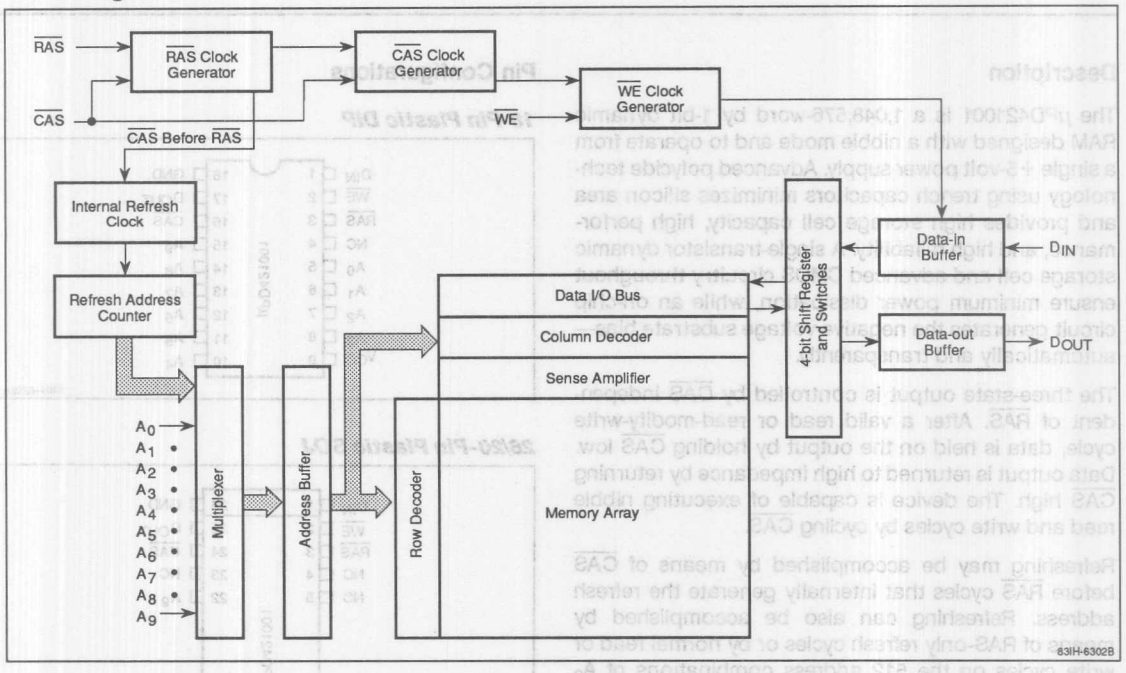
20-Pin Plastic ZIP



6

TSOP package will be available in 1991.

Block Diagram



Ordering Information

Part Number	$\overline{RAS}$ Access Time (max)	R/W Cycle Time (max)	Nibble Cycle (max)	Package
μPD421001C-60	60 ns	120 ns	40 ns	18-pin plastic DIP
C-70	70 ns	130 ns	40 ns	
C-80	80 ns	160 ns	40 ns	
C-10	100 ns	190 ns	45 ns	
μPD421001LA-60	60 ns	120 ns	40 ns	26/20-pin plastic SOJ
LA-70	70 ns	130 ns	40 ns	
LA-80	80 ns	160 ns	40 ns	
LA-10	100 ns	190 ns	45 ns	
μPD421001V-60	60 ns	120 ns	40 ns	20-pin plastic ZIP
V-70	70 ns	130 ns	40 ns	
V-80	80 ns	160 ns	40 ns	
V-10	100 ns	190 ns	45 ns	

Pin Identification

Name	Function
A_0 - A_9	Address inputs
D_{IN}	Data input
D_{OUT}	Data output
$\overline{RAS}$	Row address strobe
$\overline{CAS}$	Column address strobe
$\overline{WE}$	Write enable
GND	Ground
V_{CC}	+5-volt power supply
NC	No connection

Absolute Maximum Ratings

Voltage on any pin relative to GND, V_T	−1.0 to +7.0 V
Operating temperature, T_{OPR}	0 to +70°C
Storage temperature, T_{STG}	−55 to +125°C
Short-circuit output current, I_{OS}	50 mA
Power dissipation, P_D	1.0 W

Exposure to Absolute Maximum Ratings for extended periods may affect device reliability; exceeding the ratings could cause permanent damage. The device should be operated within the limits specified under DC and AC Characteristics.

Capacitance

T_A = 25 °C; f = 1 MHz

Parameter	Symbol	Max	Unit	Pins Under Test
Input capacitance	C_{I1}	6	pF	Address, D_{IN}
	C_{I2}	8	pF	$\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$
Output capacitance	C_D	7	pF	D_{OUT}

Recommended Operating Conditions

Parameter	Symbol	Min	Typ	Max	Unit
Supply voltage	V_{CC}	4.5	5.0	5.5	V
Input voltage, low	V_{IL}	−1.0		0.8	V
Input voltage, high	V_{IH}	2.4		V_{CC} + 1.0	V
Ambient temperature	T_A	0		70	°C

DC Characteristics

T_A = 0 to +70°C; V_{CC} = +5.0 V ±10%

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions
Standby current	I_{CC2}			2.0	mA	$\overline{RAS}$ = $\overline{CAS}$ = V_{IH}
				1.0	mA	$\overline{RAS}$ = $\overline{CAS}$ = V_{CC} − 0.2
Input leakage current	$I_{I(L)}$	−10		10	μA	V_{IN} = 0 to 5.5 V; all other pins not under test = 0 V
Output leakage current	$I_{O(L)}$	−10		10	μA	D_{OUT} disabled; V_{OUT} = 0 to 5.5 V
Output voltage, low	V_{OL}			0.4	V	I_{OL} = 4.2 mA
Output voltage, high	V_{OH}	2.4			V	I_{OH} = −5 mA

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AC Characteristics

T_A = 0 to +70°C; V_{CC} = +5.0 V ±10%

		-60		-70		-80		-10			
Parameter	**Symbol**	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**	**Unit**	**Test Conditions**
Operating current, average	I_{CC1}		90		80		70		60	mA	$\overline{RAS}$, $\overline{CAS}$ cycling; $t_{RC} = t_{RC}$ min (Note 5)
Operating current, $\overline{RAS}$-only refresh cycle, average	I_{CC3}		90		80		70		60	mA	$\overline{RAS}$ cycling; $\overline{CAS} = V_{IH}$; $t_{RC} = t_{RC}$ min (Note 5)
Operating current, nibble cycle, average	I_{CC4}		80		70		60		50	mA	$\overline{RAS} = V_{IL}$; $\overline{CAS}$ cycling; $t_{NC} = t_{NC}$ min (Note 5)
Operating current, $\overline{CAS}$ before $\overline{RAS}$ refresh cycle, average	I_{CC5}		90		80		70		60	mA	$\overline{RAS}$ cycling; $\overline{CAS}$ before $\overline{RAS}$; $t_{RC} = t_{RC}$ min (Note 5)
Access time from column address	t_{AA}		30		35		45		50	ns	(Notes 7, 10)
Column address hold time referenced to $\overline{RAS}$	t_{AR}	N/A		N/A		60		70		ns	(Note 18)
Column address setup time	t_{ASC}	0		0		0		0		ns	
Row address setup time	t_{ASR}	0		0		0		0		ns	
Column address to $\overline{WE}$ delay time	t_{AWD}	30		35		45		50		ns	(Note 17)
Access time from $\overline{CAS}$ (falling edge)	t_{CAC}		20		20		20		25	ns	(Notes 7, 9, 10)
Column address hold time	t_{CAH}	15		17		20		20		ns	
$\overline{CAS}$ pulse width	t_{CAS}	20	10,000	20	10,000	20	10,000	25	10,000	ns	
$\overline{CAS}$ hold time for $\overline{CAS}$ before $\overline{RAS}$ refresh cycle	t_{CHR}	15		15		15		20		ns	
$\overline{CAS}$ precharge time	t_{CPN}	10		10		10		10		ns	
$\overline{CAS}$ to $\overline{RAS}$ precharge time	t_{CRP}	10		10		10		10		ns	(Note 13)
$\overline{CAS}$ hold time	t_{CSH}	60		70		80		100		ns	
$\overline{CAS}$ setup time for $\overline{CAS}$ before $\overline{RAS}$ refresh cycle	t_{CSR}	10		10		10		10		ns	
$\overline{CAS}$ to $\overline{WE}$ delay	t_{CWD}	20		20		20		25		ns	(Note 17)
Write command to $\overline{CAS}$ lead time	t_{CWL}	15		15		15		20		ns	
Data-in hold time	t_{DH}	15		15		20		20		ns	(Note 16)
Data-in hold time referenced to $\overline{RAS}$	t_{DHR}	N/A		N/A		60		70		ns	(Note 18)
Data-in setup time	t_{DS}	0		0		0		0		ns	(Note 16)
Nibble access time	t_{NAC}		20		20		20		25	ns	(Note 7)

AC Characteristics (cont)

Parameter	Symbol	-60 Min	-60 Max	-70 Min	-70 Max	-80 Min	-80 Max	-10 Min	-10 Max	Unit	Test Conditions
$\overline{CAS}$ pulse width (nibble cycle)	t_{NAS}	20	10,000	20	10,000	20	10,000	25	10,000	ns	
Nibble cycle time	t_{NC}	40		40		40		45		ns	(Note 6)
$\overline{CAS}$ to $\overline{WE}$ delay (nibble cycle)	t_{NCWD}	20		20		20		25		ns	(Note 17)
Write command to $\overline{CAS}$ lead time (nibble cycle)	t_{NCWL}	15		15		20		25		ns	
$\overline{CAS}$ precharge (nibble cycle)	t_{NP}	10		10		10		10		ns	
$\overline{RAS}$ hold time (nibble read cycle)	t_{NRRSH}	20		20		20		25		ns	
$\overline{RAS}$ hold time (nibble write cycle)	t_{NWRSH}	20		20		20		25		ns	
Output buffer turnoff delay	t_{OFF}	0	15	0	15	0	20	0	25	ns	(Note 11)
Access time from $\overline{RAS}$	t_{RAC}		60		70		80		100	ns	(Notes 7, 8)
$\overline{RAS}$ to column address delay time	t_{RAD}	15	30	15	35	17	35	17	50	ns	(Note 10)
Row address hold time	t_{RAH}	10		10		12		12		ns	
Column address lead time referenced to $\overline{RAS}$ (rising edge)	t_{RAL}	30		35		45		50		ns	
$\overline{RAS}$ pulse width	t_{RAS}	60	10,000	70	10,000	80	10,000	100	10,000	ns	
$\overline{RAS}$ pulse width, nibble cycle	t_{RASP}	60	100,000	70	100,000	80	100,000	100	100,000	ns	
Random read or write cycle time	t_{RC}	120		130		160		190		ns	(Note 6)
$\overline{RAS}$ to $\overline{CAS}$ delay time	t_{RCD}	20	40	20	50	25	60	25	75	ns	(Note 12)
Read command hold time referenced to $\overline{CAS}$	t_{RCH}	0		0		0		0		ns	(Note 14)
Read command setup time	t_{RCS}	0		0		0		0		ns	
Refresh period	t_{REF}		8		8		8		8	ms	Addresses A_0 - A_8
$\overline{RAS}$ precharge time	t_{RP}	50		50		70		80		ns	
$\overline{RAS}$ precharge $\overline{CAS}$ hold time	t_{RPC}	10		10		0		0		ns	
Read command hold time referenced to $\overline{RAS}$	t_{RRH}	10		10		10		10		ns	(Note 14)
$\overline{RAS}$ hold time	t_{RSH}	20		20		20		25		ns	
Read-write cycle time	t_{RWC}	145		155		190		225		ns	(Note 6)
$\overline{RAS}$ to $\overline{WE}$ delay	t_{RWD}	60		70		80		100		ns	(Note 17)
Write command to $\overline{RAS}$ lead time	t_{RWL}	20		20		25		30		ns	

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AC Characteristics (cont)

Parameter	Symbol	-60 Min	-60 Max	-70 Min	-70 Max	-80 Min	-80 Max	-10 Min	-10 Max	Unit	Test Conditions
Rise and fall transition time	t_T	3	50	3	50	3	50	3	50	ns	(Note 4)
Write command hold time	t_{WCH}	15		15		15		20		ns	
Write command hold time referenced to $\overline{RAS}$	t_{WCR}	N/A		N/A		55		70		ns	(Note 18)
Write command setup time	t_{WCS}	0		0		0		0		ns	(Note 17)
Write command pulse width	t_{WP}	15		15		15		20		ns	(Note 15)

Notes:

(1) All voltages are referenced to GND.

(2) An initial pause of 100 μs is required after power-up, followed by any eight $\overline{RAS}$ cycles, before proper device operation is achieved.

(3) AC measurements assume t_T = 5 ns.

(4) V_{IH} (min) and V_{IL} (max) are reference levels for measuring the timing of input signals. Transition times are measured between V_{IH} and V_{IL}.

(5) I_{CC1}, I_{CC3}, I_{CC4}, and I_{CC5} depend on output loading and cycle rates. Specified values are obtained with the output open. I_{CC3} is measured assuming that all column address inputs are held at either a high level or a low level during $\overline{RAS}$-only refresh cycles. I_{CC4} is measured assuming that all column address inputs are switched only once during each nibble cycle.

(6) The minimum specifications are used only to indicate the cycle time at which proper operation over the full temperature range (T_A = 0 to +70°C) is assured.

(7) Load = 2 TTL (–1 mA, +4 mA) loads and 100 pF (V_{OH} = 2.0 V, V_{OL} = 0.8 V).

(8) Assumes that $t_{RCD} \leq t_{RCD}$ (max) and $t_{RAD} \leq t_{RAD}$ (max). If t_{RCD} or t_{RAD} is greater than the maximum recommended value in this table, t_{RAC} increases by the amount that t_{RCD} or t_{RAD} exceeds the value shown.

(9) Assumes that $t_{RCD} \geq t_{RCD}$ (max) and $t_{RAD} \leq t_{RAD}$ (max).

(10) If $t_{RAD} \geq t_{RAD}$ (max), then the access time is defined by t_{AA}.

(11) t_{OFF} (max) defines the time at which the output achieves the open-circuit condition and is not referenced to V_{OH} or V_{OL}.

(12) Operation within the t_{RCD} (max) limit assures that t_{RAC} (max) can be met. t_{RCD} (max) is specified as a reference point only; if t_{RCD} is greater than t_{RCD} (max), then access time is controlled exclusively by t_{CAC}.

(13) The t_{CRP} requirement should be applicable for $\overline{RAS}$/$\overline{CAS}$ cycles preceded by any cycle.

(14) Either t_{RRH} or t_{RCH} must be satisfied for a read cycle.

(15) Parameter t_{WP} is applicable for a delayed write cycle such as a read-write/read-modify-write cycle. For early write operation, both t_{WCS} and t_{WCH} must be met.

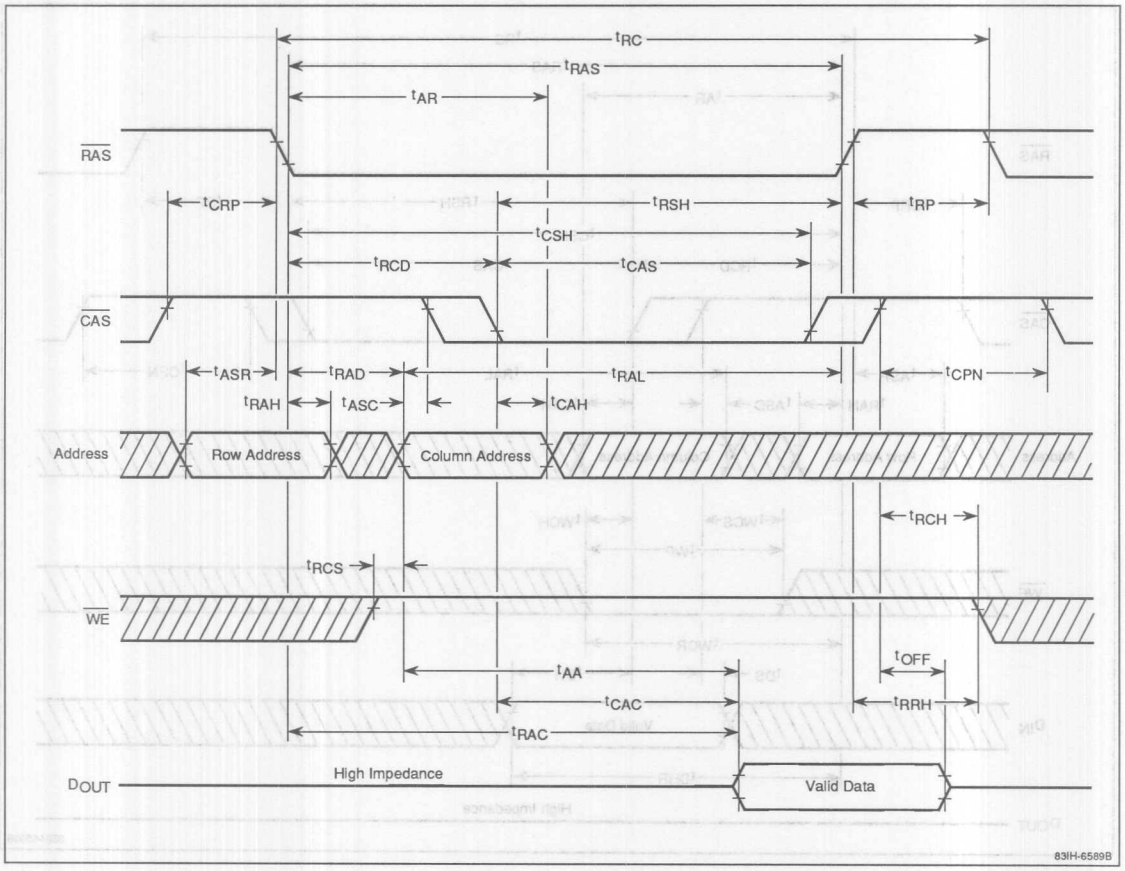
(16) These parameters are referenced to the falling edge of $\overline{CAS}$ for early write cycles and to the falling edge of $\overline{WE}$ for delayed write or read-modify-write cycles.

(17) t_{WCS}, t_{RWD}, t_{CWD}, and t_{AWD} are restrictive operating parameters in read-write/read-modify-write cycles only. If $t_{WCS} \geq t_{WCS}$ (min), the cycle is an early write cycle and the data output will remain open-circuit throughout the entire cycle. If $t_{CWD} \geq t_{CWD}$ (min), $t_{RWD} \geq t_{RWD}$ (min), and $t_{AWD} \geq t_{AWD}$ (min), the cycle is a read-write cycle and the data output will contain data read from the selected cell. If neither of the above conditions is met, the condition of the data output pin (at access time and until $\overline{CAS}$ returns to V_{IH}) is indeterminate.

(18) This parameter is not needed for the μPD421001-60 and μPD421001-70.

Timing Waveforms

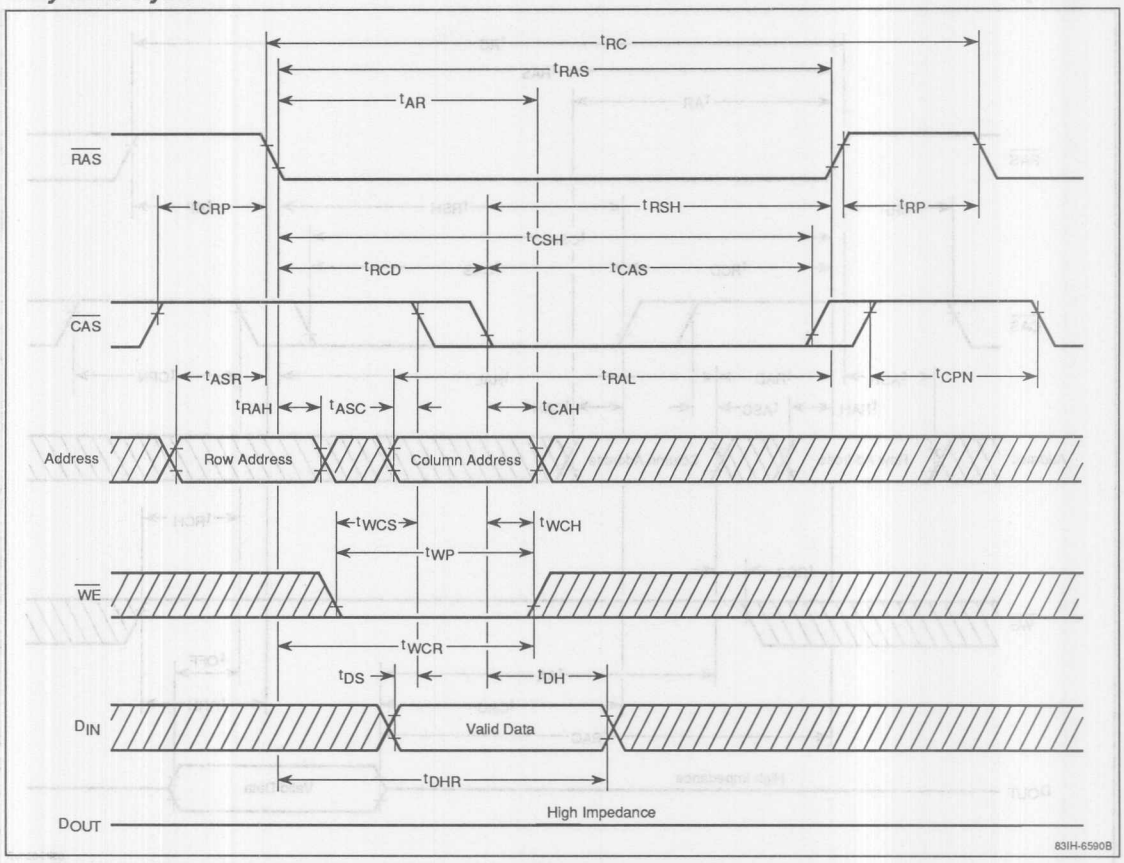
Read Cycle



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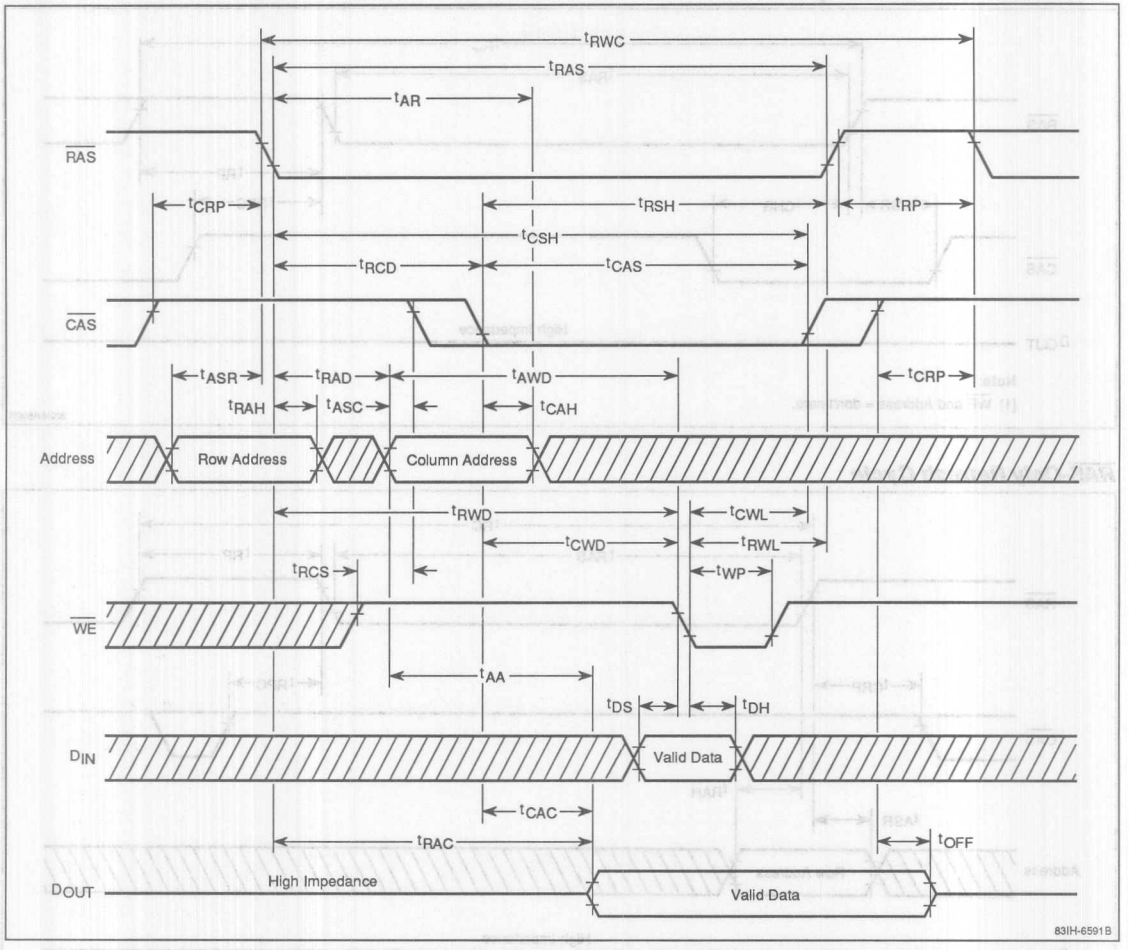
Timing Waveforms (cont)

Early Write Cycle



Timing Waveforms (cont)

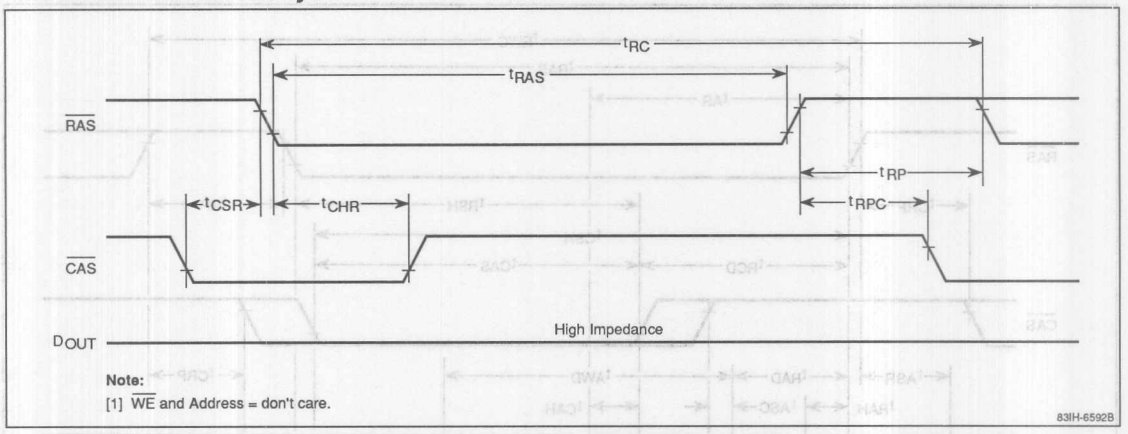
Read-Write/Read-Modify-Write Cycle



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Timing Waveforms (cont)

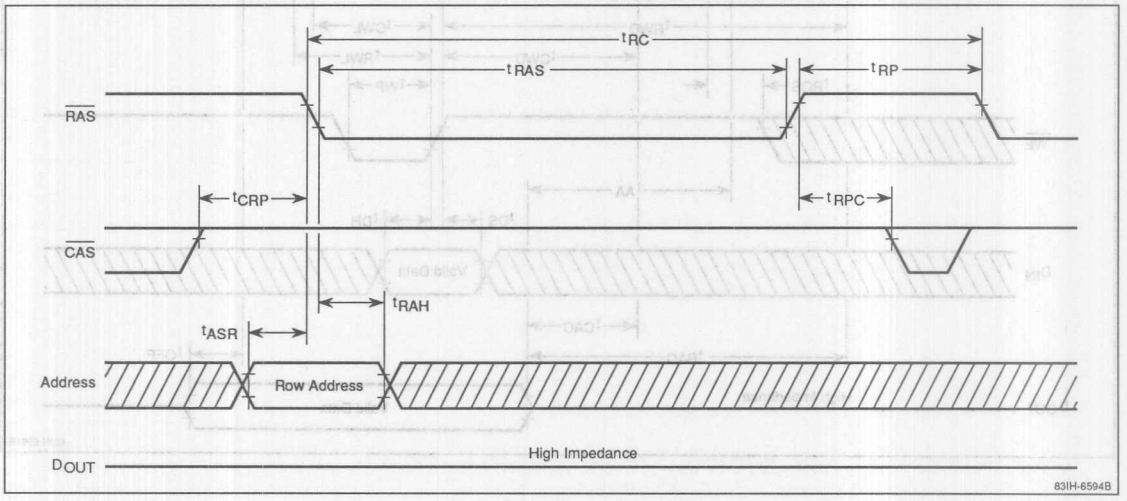
$\overline{CAS}$ Before $\overline{RAS}$ Refresh Cycle



Note:
[1] $\overline{WE}$ and Address = don't care.

83IH-6592B

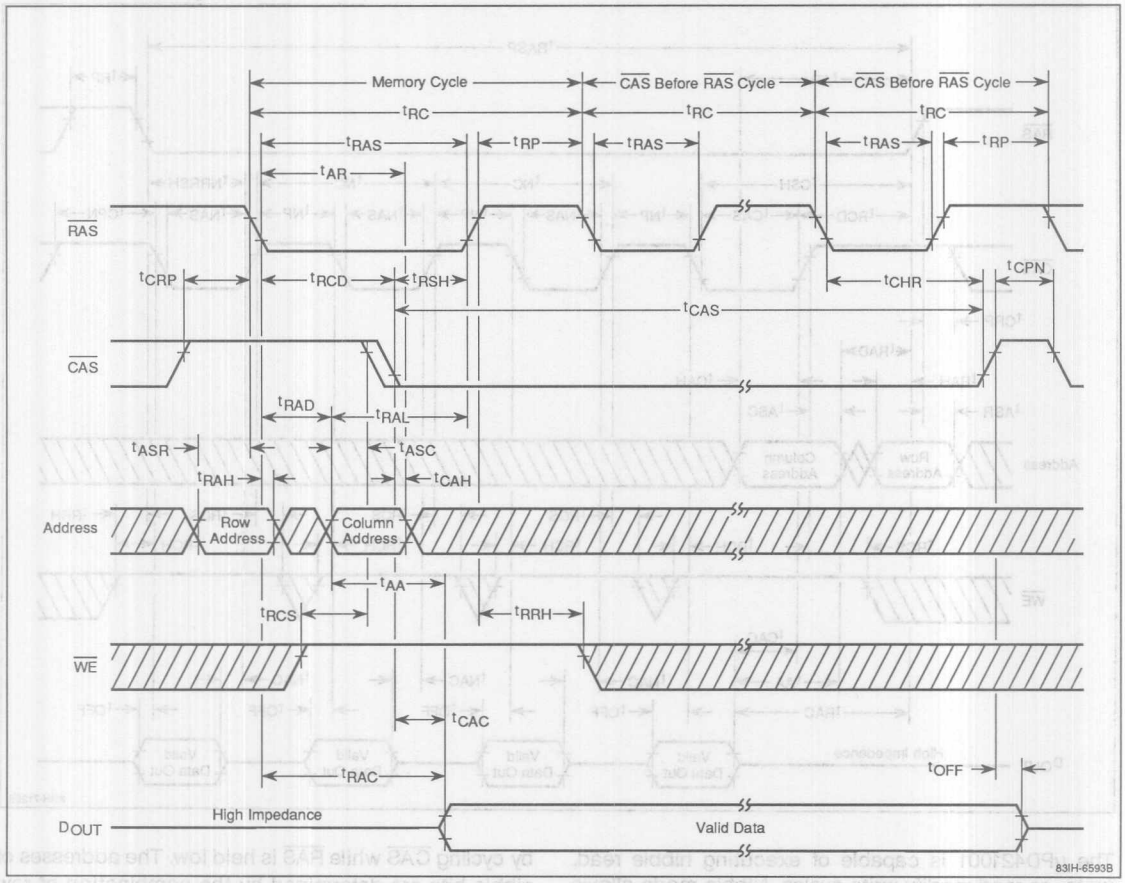
$\overline{RAS}$-Only Refresh Cycle



83IH-6594B

Timing Waveforms (cont)

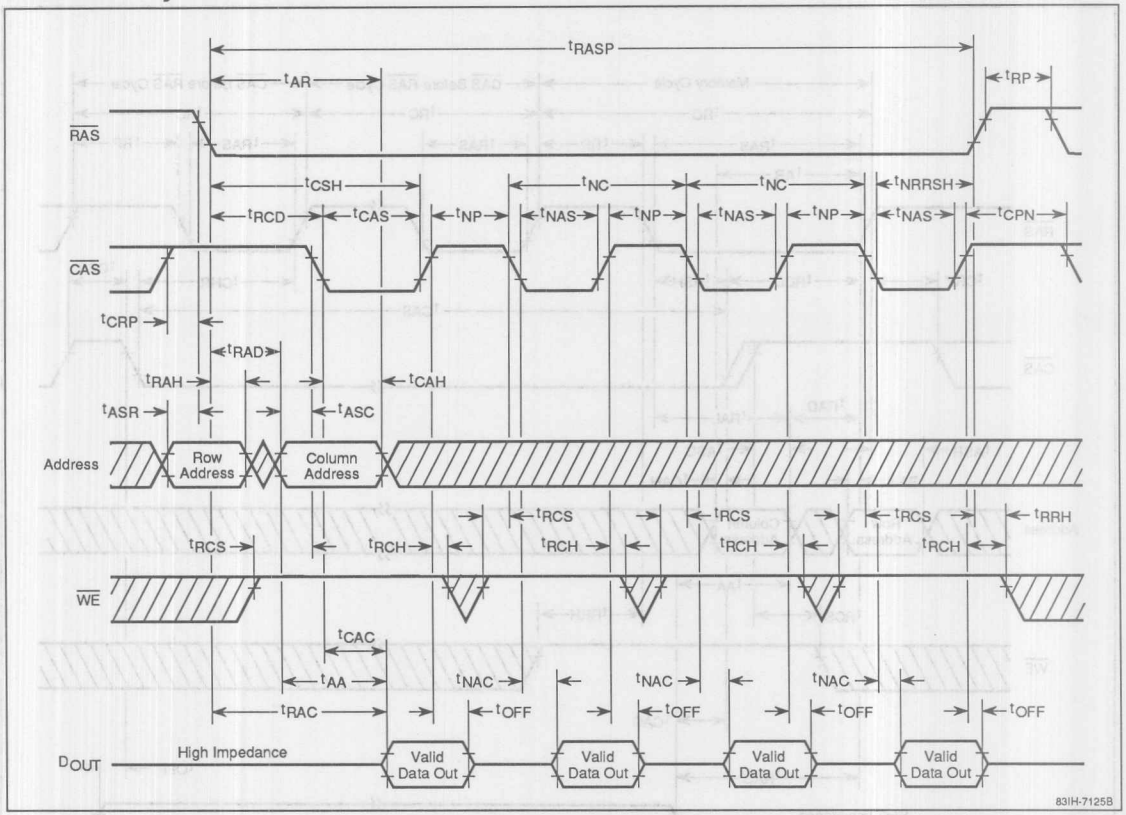
Hidden Refresh Cycle



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Timing Waveforms (cont)

Nibble Read Cycle

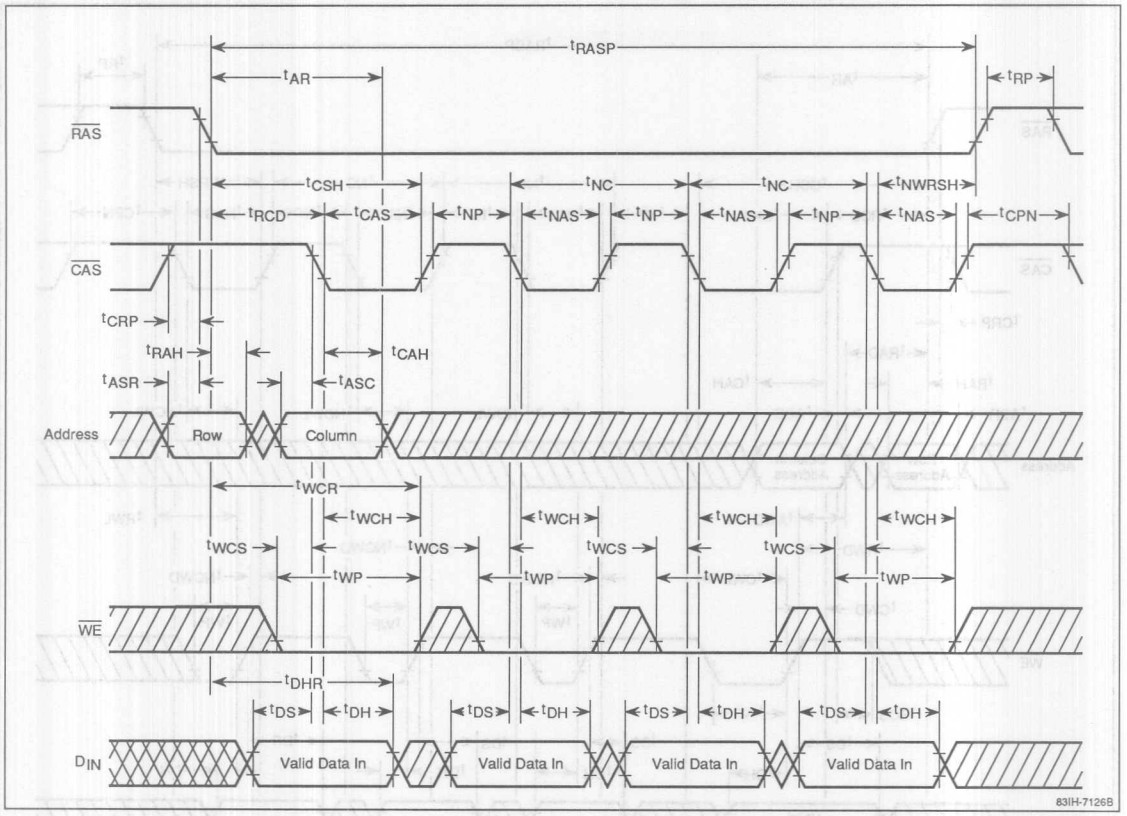


The μPD421001 is capable of executing nibble read, write, or read-modify-write cycles. Nibble mode allows high-speed serial access of maximum of 4 data bits. The first bit is determined by the row and column addresses, and the next bits are accessed automatically by cycling $\overline{CAS}$ while $\overline{RAS}$ is held low. The addresses of nibble bits are determined by the combination of row address A_9 and column address A_9 in the following sequence.

		Row Address										Column Address										
Sequence	Nibble Bit	A_9	A_8	A_7	A_6	A_5	A_4	A_3	A_2	A_1	A_0	A_9	A_8	A_7	A_6	A_5	A_4	A_3	A_2	A_1	A_0	Comment
$\overline{RAS}/\overline{CAS}$	1	0	0	1	0	0	0	1	0	1	0	0	1	1	0	1	0	1	0	0	0	Example: external address input
$\overline{CAS}$ cycling	2	1	0	1	0	0	0	1	0	1	0	0	1	1	0	1	0	1	0	0	0	Internal address generated
$\overline{CAS}$ cycling	3	0	0	1	0	0	0	1	0	1	0	1	1	1	0	1	0	1	0	0	0	
$\overline{CAS}$ cycling	4	1	0	1	0	0	0	1	0	1	0	1	1	1	0	1	0	1	0	0	0	
$\overline{CAS}$ cycling	1	0	0	1	0	0	0	1	0	1	0	0	1	1	0	1	0	1	0	0	0	Repeated sequence

Timing Waveforms (cont)

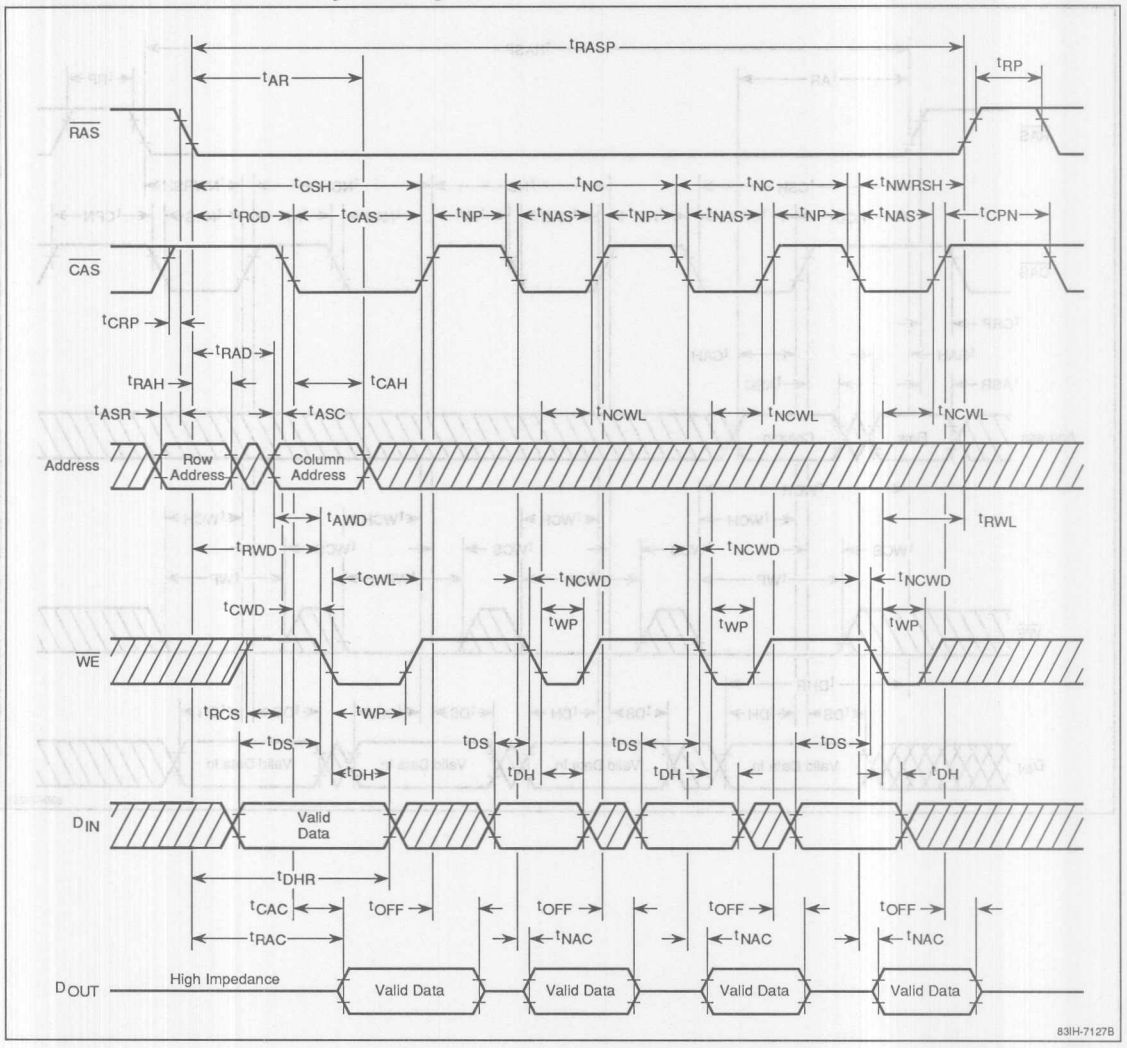
Nibble Early Write Cycle



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Timing Waveforms (cont)

Nibble Read-Write/Read-Modify-Write Cycle



μPD421002
1,048,576 x 1-Bit
Dynamic CMOS RAM

Description

The μPD421002 is a static-column dynamic RAM organized as 1,048,576 words by 1 bit and designed to operate from a single +5-volt power supply. Advanced polycide technology using trench capacitors minimizes silicon area and provides high storage cell capacity, high performance, and high reliability. A single-transistor dynamic storage cell and advanced CMOS circuitry ensure minimum power dissipation, while an on-chip circuit internally generates the negative-voltage substrate bias—automatically and transparently.

The three-state output is controlled by $\overline{CS}$ independent of $\overline{RAS}$. After a valid read or read-modify-write cycle, data is held on the output by holding $\overline{CS}$ low. The data output is returned to high impedance by returning $\overline{CS}$ high. Static-column read and write cycles may be executed by switching the column address inputs.

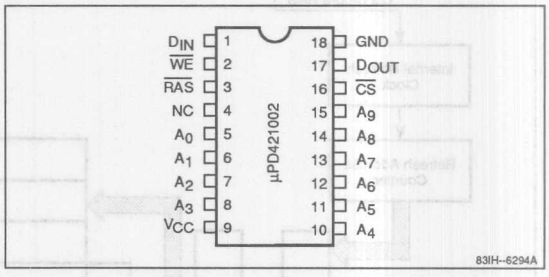
Refreshing may be accomplished by means of a $\overline{CS}$ before $\overline{RAS}$ cycle that internally generates the refresh address. Refreshing can also be accomplished by means of $\overline{RAS}$-only refresh cycles or by normal read or write cycles on the 512 address combinations of A_0 through A_8 during an 8-ms refresh period.

Features

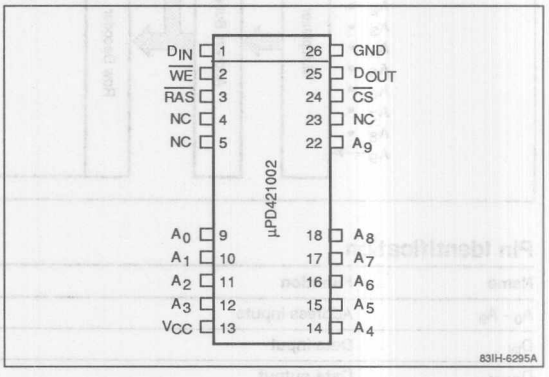
- 1,048,576-word by 1-bit organization
- Single +5-volt ±10% power supply
- Static-column option
- Low power dissipation
  - 70 mA max (active) for 80 ns version
  - 1 mA max (standby)
- $\overline{CS}$ before $\overline{RAS}$ refreshing
- Multiplexed address inputs
- On-chip substrate bias generator
- Nonlatched, three-state outputs
- Low input capacitance
- TTL-compatible inputs and outputs
- 512 refresh cycles every 8 ms
- High-density 18-pin plastic DIP, 26/20-pin plastic SOJ, or 20-pin plastic ZIP packaging

Pin Configurations

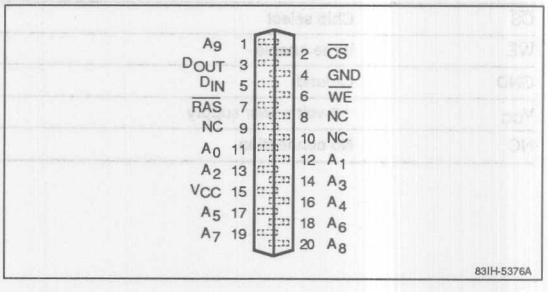
18-Pin Plastic DIP



26/20-Pin Plastic SOJ



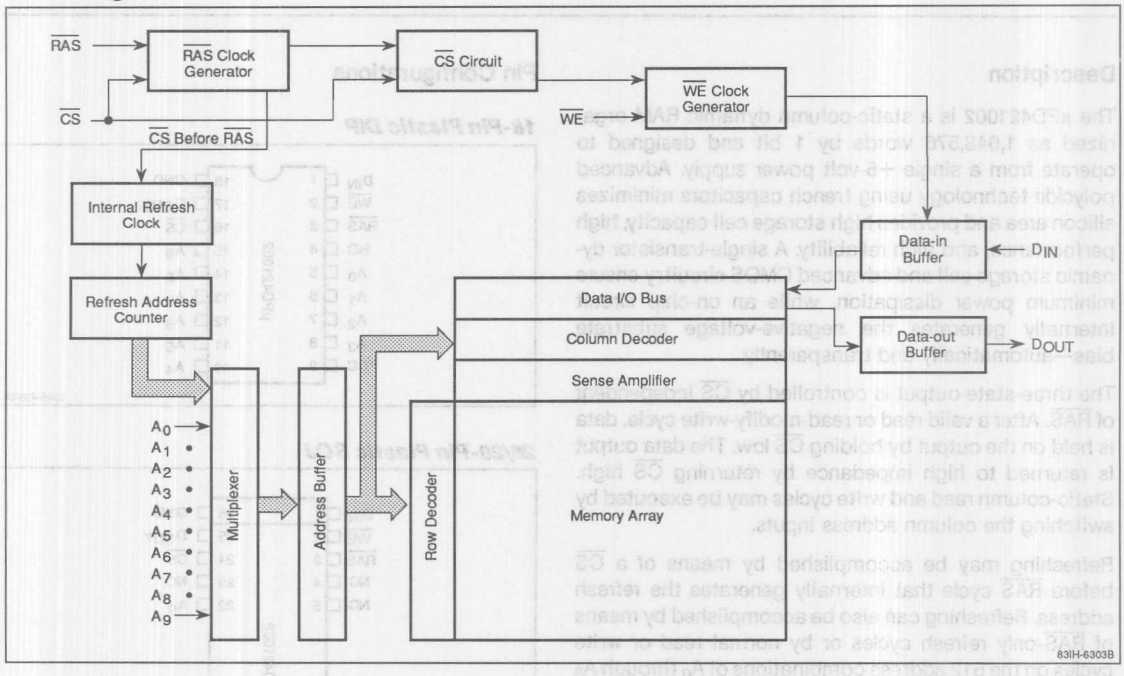
20-Pin Plastic ZIP



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TSOP package will be available in 1991.

Block Diagram



Pin Identification

Name	Function
A_0 - A_9	Address inputs
D_{IN}	Data input
D_{OUT}	Data output
$\overline{RAS}$	Row address strobe
$\overline{CS}$	Chip select
$\overline{WE}$	Write enable
GND	Ground
V_{CC}	+5-volt power supply
NC	No connection

Absolute Maximum Ratings

Voltage on any pin relative to GND	−1.0 to +7.0 V
Operating temperature, T_{OPR}	0 to +70°C
Storage temperature, T_{STG}	−55 to +125°C
Short-circuit output current, I_{OS}	50 mA
Power dissipation, P_D	1.0 W

Exposure to Absolute Maximum Ratings for extended periods may affect device reliability; exceeding the ratings could cause permanent damage. The device should be operated within the limits specified under DC and AC Characteristics.

Ordering Information

Part Number	$\overline{RAS}$ Access Time (max)	R/W Cycle Time (max)	Static-Column Access (max)	Package
μPD421002C-60	60 ns	120 ns	35 ns	20-pin plastic DIP
C-70	70 ns	130 ns	40 ns	
C-80	80 ns	160 ns	50 ns	
C-10	100 ns	190 ns	60 ns	
μPD421002LA-60	60 ns	120 ns	35 ns	26/20-pin plastic SOJ
LA-70	70 ns	130 ns	40 ns	
LA-80	80 ns	160 ns	50 ns	
LA-10	100 ns	190 ns	60 ns	
μPD421002V-60	60 ns	120 ns	35 ns	20-pin plastic ZIP
V-70	70 ns	130 ns	40 ns	
V-80	80 ns	160 ns	50 ns	
V-10	100 ns	190 ns	60 ns	

DC Characteristics

T_A = 0 to +70°C; V_{CC} = +5.0 V ±10%

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions
Standby current	I_{CC2}			3.0	mA	$\overline{RAS}$ = $\overline{CS}$ = V_{IH}
				1.0	mA	$\overline{RAS}$ = $\overline{CS}$ = V_{CC} – 0.2
Input leakage current	$I_{I(L)}$	–10		10	μA	V_{IN} = 0 V to V_{CC}; all other pins not under test = 0 V
Output leakage current	$I_{O(L)}$	–10		10	μA	D_{OUT} disabled; V_{OUT} = 0 V to V_{CC}
Output voltage, low	V_{OL}			0.4	V	I_{OL} = 4.2 mA
Output voltage, high	V_{OH}	2.4			V	I_{OH} = –5 mA

Capacitance

T_A = 25°C; f = 1 MHz

Parameter	Symbol	Max	Unit	Pins Under Test
Input capacitance	C_{I1}	6	pF	Address, D_{IN}
	C_{I2}	8	pF	$\overline{RAS}$, $\overline{CS}$, $\overline{WE}$
Output capacitance	C_O	7	pF	D_{OUT}

Recommended Operating Conditions

Parameter	Symbol	Min	Typ	Max	Unit
Input voltage, high	V_{IH}	2.4		V_{CC} + 1.0	V
Input voltage, low	V_{IL}	–1.0		0.8	V
Supply voltage	V_{CC}	4.5	5.0	5.5	V
Ambient temperature	T_A	0		70	°C

6

AC Characteristics

T_A = 0 to +70°C; V_{CC} = +5.0 V ±10%

		-60		-70		-80		-10			
Parameter	Symbol	Min	Max	Min	Max	Min	Max	Min	Max	Unit	Test Conditions
Operating current, average	I_{CC1}		90		80		70		60	mA	$\overline{RAS}$, $\overline{CS}$ cycling; $t_{RC} = t_{RC}$ min (Note 5)
Operating current, $\overline{RAS}$-only refresh cycle, average	I_{CC3}		90		80		70		60	mA	$\overline{RAS}$ cycling; $\overline{CS} = V_{IH}$; $t_{RC} = t_{RC}$ min (Note 5)
Static column operating current, average	I_{CC4}		80		70		60		50	mA	$\overline{RAS} = V_{IL}$; $\overline{CS} = V_{IL}$; addresses cycling; $t_{RSC} = t_{RSC}$ min or $t_{WSC} = t_{WSC}$ min (Note 5)
Operating current, $\overline{CS}$ before $\overline{RAS}$ refresh cycle, average	I_{CC5}		90		80		70		60	mA	$\overline{RAS}$ cycling; $\overline{CS}$ before $\overline{RAS}$; $t_{RC} = t_{RC}$ min (Note 5)
Access time from column address	t_{AA}		30		35		45		50	ns	(Notes 7, 10)
$\overline{RAS}$ to column address hold time	t_{AH}	15		15		15		15		ns	
Column address hold time referenced to $\overline{RAS}$	t_{AR}	N/A		N/A		80		100		ns	(Note 18)
Column address setup time	t_{ASC}	0		0		0		0		ns	
Row address setup time	t_{ASR}	0		0		0		0		ns	
Column address to $\overline{WE}$ delay time	t_{AWD}	30		35		45		50		ns	(Note 17)
Column address hold time rereferenced to $\overline{RAS}$ (write cycle)	t_{AWR}	N/A		N/A		60		60		ns	
Access time from $\overline{CS}$ (falling edge)	t_{CAC}		20		20		20		25	ns	(Notes 7, 9, 10)
Column address hold time	t_{CAH}	15		17		20		20		ns	
$\overline{CS}$ hold time for $\overline{CS}$ before $\overline{RAS}$ refresh cycle	t_{CHR}	15		15		15		20		ns	
$\overline{CS}$ precharge time	t_{CP}	10		10		10		10		ns	
$\overline{CS}$ to $\overline{RAS}$ precharge time	t_{CRP}	10		10		10		10		ns	(Note 13)
$\overline{CS}$ pulse width	t_{CS}	20	100,000	20	100,000	20	100,000	25	100,000	ns	
$\overline{CS}$ hold time	t_{CSH}	60		70		80		100		ns	
$\overline{CS}$ setup time for $\overline{CS}$ before $\overline{RAS}$ refresh cycle	t_{CSR}	10		10		10		10		ns	
$\overline{CS}$ to $\overline{WE}$ delay	t_{CWD}	20		20		20		25		ns	(Note 17)
Write command to $\overline{CS}$ lead time	t_{CWL}	15		15		15		20		ns	
Data-in hold time	t_{DH}	15		15		20		20		ns	(Note 16)
Data-in hold time referenced to $\overline{RAS}$	t_{DHR}	N/A		N/A		60		70		ns	(Note 18)
Data-in setup time	t_{DS}	0		0		0		0		ns	(Note 16)

AC Characteristics (cont)

Parameter	Symbol	-60 Min	-60 Max	-70 Min	-70 Max	-80 Min	-80 Max	-10 Min	-10 Max	Unit	Test Conditions
Output buffer turnoff delay	t_{OFF}	0	15	0	15	0	20	0	25	ns	(Note 11)
Output hold time from address	t_{OH}	5		5		5		5		ns	
Output hold time from $\overline{WE}$	t_{OHW}	10		10		10		10		ns	
Access time from previous $\overline{WE}$ (falling edge)	t_{PWA}		60		70		90		110	ns	(Notes 7, 18)
Column address hold time from previous $\overline{WE}$ (falling edge)	t_{PWH}	60		70		90		110		ns	
Access time from $\overline{RAS}$	t_{RAC}		60		70		80		100	ns	(Notes 7, 8)
$\overline{RAS}$ to column address delay time	t_{RAD}	15	30	15	35	17	35	17	50	ns	(Note 10)
Row address hold time	t_{RAH}	10		10		12		12		ns	
Column address lead time referenced to $\overline{RAS}$ (rising edge)	t_{RAL}	30		35		45		50		ns	
$\overline{RAS}$ pulse width	t_{RAS}	60	10,000	70	10,000	80	10,000	100	10,000	ns	
Static-column $\overline{RAS}$ pulse width	t_{RASC}	60	100,000	70	100,000	80	100,000	100	100,000	ns	
Random read or write cycle time	t_{RC}	120		130		160		190		ns	(Note 6)
$\overline{RAS}$ to $\overline{CS}$ delay time	t_{RCD}	20	40	20	50	25	60	25	75	ns	(Note 12)
Read command hold time referenced to $\overline{CS}$	t_{RCH}	0		0		0		0		ns	(Note 14)
Read command setup time	t_{RCS}	0		0		0		0		ns	
Refresh period	t_{REF}		8		8		8		8	ms	Addresses A_0 - A_8
$\overline{RAS}$ precharge time	t_{RP}	50		50		70		80		ns	
$\overline{RAS}$ precharge $\overline{CS}$ hold time	t_{RPC}	10		10		0		0		ns	
Read command hold time referenced to $\overline{RAS}$	t_{RRH}	10		10		10		10		ns	(Note 14)
Static-column read cycle time	t_{RSC}	35		40		50		60		ns	(Note 6)
$\overline{RAS}$ hold time	t_{RSH}	20		20		20		25		ns	
$\overline{RAS}$ to second $\overline{WE}$ delay	t_{RSW}	75		85		95		115		ns	
Read-write cycle time	t_{RWC}	145		155		190		225		ns	(Note 6)
$\overline{RAS}$ to $\overline{WE}$ delay	t_{RWD}	60		70		80		100		ns	(Note 17)

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AC Characteristics (cont)

Parameter	Symbol	-60 Min	-60 Max	-70 Min	-70 Max	-80 Min	-80 Max	-10 Min	-10 Max	Unit	Test Conditions
Write command to $\overline{RAS}$ lead time	t_{RWL}	20		20		25		30		ns	
Static-column read-write cycle time	t_{RWSC}	65		75		95		115		ns	(Note 6)
Rise and fall transition time	t_T	3	50	3	50	3	50	3	50	ns	(Note 4)
Previous $\overline{WE}$ (falling edge) to column address delay time	t_{WAD}	20	30	22	35	20	45	25	55	ns	(Note 18)
Write command hold time	t_{WCH}	15		15		15		20		ns	
Write command hold time referenced to $\overline{RAS}$	t_{WCR}	N/A		N/A		55		70		ns	(Note 18)
Write command setup time	t_{WCS}	0		0		0		0		ns	(Note 17)
Write invalid time	t_{WI}	10		10		10		10		ns	
Write command pulse width	t_{WP}	15		15		15		20		ns	(Note 15)
Static-column write cycle time	t_{WSC}	35		40		50		60		ns	(Note 6)

Notes:

(1) All voltages are referenced to GND.

(2) An initial pause of 100 μs is required after power-up, followed by any eight $\overline{RAS}$ cycles, before proper device operation is achieved.

(3) AC measurements assume $t_T = 5$ ns.

(4) V_{IH} (min) and V_{IL} (max) are reference levels for measuring the timing of input signals. Transition times are measured between V_{IH} and V_{IL}.

(5) I_{CC1}, I_{CC3}, I_{CC4}, and I_{CC5} depend on output loading and cycle rates. Specified values are obtained with the output open. I_{CC3} is measured assuming that all column address inputs are held at either a high level or a low level during $\overline{RAS}$-only refresh cycles. I_{CC4} is measured assuming that all column address inputs are switched only once during each fast-page cycle.

(6) The minimum specifications are used only to indicate the cycle time at which proper operation over the full temperature range (T_A = 0 to +70°C) is assured.

(7) Load = 2 TTL (–1 mA, +4 mA) loads and 100 pF (V_{OH} = 2.0 V, V_{OL} = 0.8 V).

(8) Assumes that $t_{RCD} \leq t_{RCD}$ (max) and $t_{RAD} \leq t_{RAD}$ (max). If t_{RCD} or t_{RAD} is greater than the maximum recommended value in this table, t_{RAC} increases by the amount that t_{RCD} or t_{RAD} exceeds the value shown.

(9) Assumes that $t_{RCD} \geq t_{RCD}$ (max) and $t_{RAD} \leq t_{RAD}$ (max).

(10) If $t_{RAD} \geq t_{RAD}$ (max), then the access time is defined by t_{AA}.

(11) t_{OFF} (max) defines the time at which the output achieves the open-circuit condition and is not referenced to V_{OH} or V_{OL}.

(12) Operation within the t_{RCD} (max) limit assures that t_{RAC} (max) can be met. t_{RCD} (max) is specified as a reference point only; if t_{RCD} is greater than t_{RCD} (max), then access time is controlled exclusively by t_{CAC}.

(13) The t_{CRP} requirement should be applicable for $\overline{RAS}$/$\overline{CS}$ cycles preceded by any cycle.

(14) Either t_{RRH} or t_{RCH} must be satisfied for a read cycle.

(15) Parameter t_{WP} is applicable for a delayed write cycle such as a read-write/read-modify-write cycle. For early write operation, both t_{WCS} and t_{WCH} must be met.

(16) These parameters are referenced to the falling edge of $\overline{CS}$ for early write cycles and to the falling edge of $\overline{WE}$ for delayed write or read-modify-write cycles.

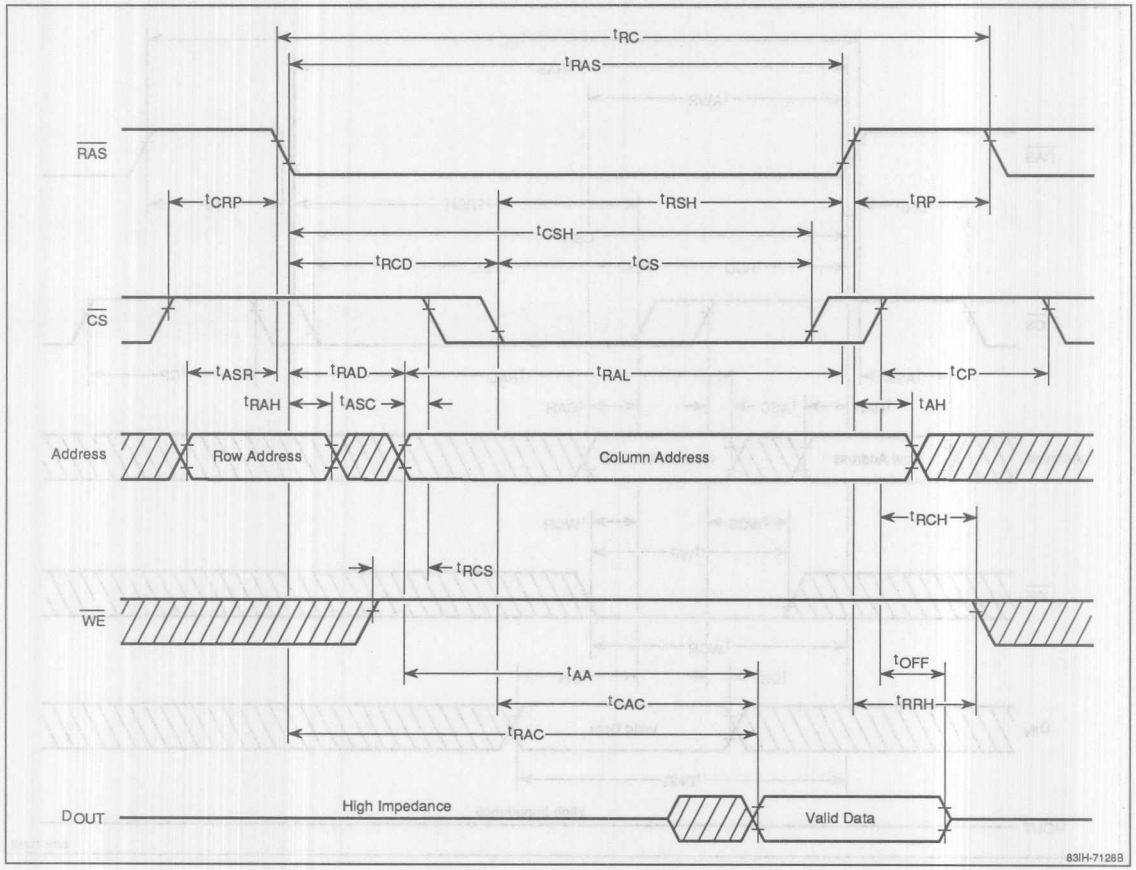
(17) t_{WCS}, t_{RWD}, t_{CWD}, and t_{AWD} are restrictive operating parameters in read-write/read-modify-write cycles only. If $t_{WCS} \geq t_{WCS}$ (min), the cycle is an early write cycle and the data output will remain open-circuit throughout the entire cycle. If $t_{CWD} \geq t_{CWD}$ (min), $t_{RWD} \geq t_{RWD}$ (min), and $t_{AWD} \geq t_{AWD}$ (min), the cycle is a read-write cycle and the data output will contain data read from the selected cell. If neither of the above conditions is met, the condition of the data output pin (at access time and until $\overline{CS}$ returns to V_{IH}) is indeterminate.

(18) This parameter is not needed for the μPD421002-60 and μPD421002-70.

(19) If $t_{WAD} \leq t_{WAD}$ (max), then access time is defined by t_{PWA}.

Timing Waveforms

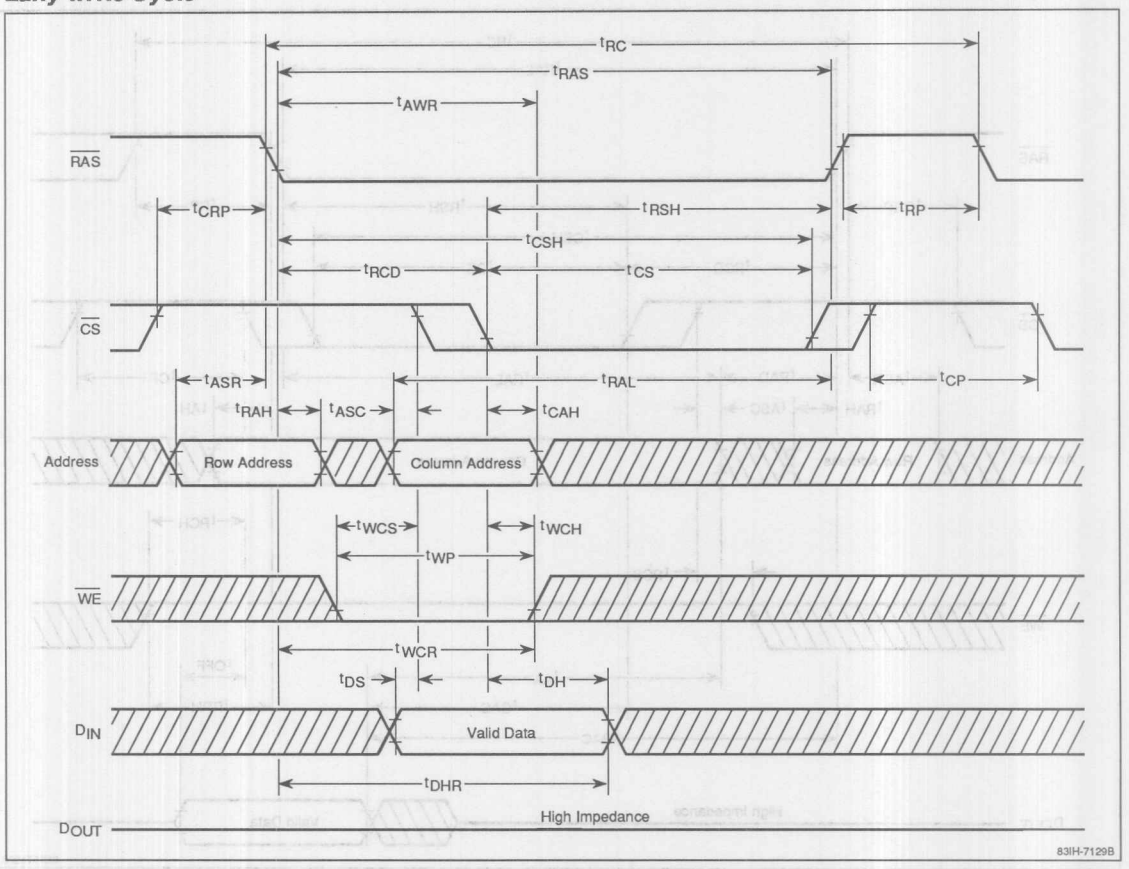
Read Cycle



6

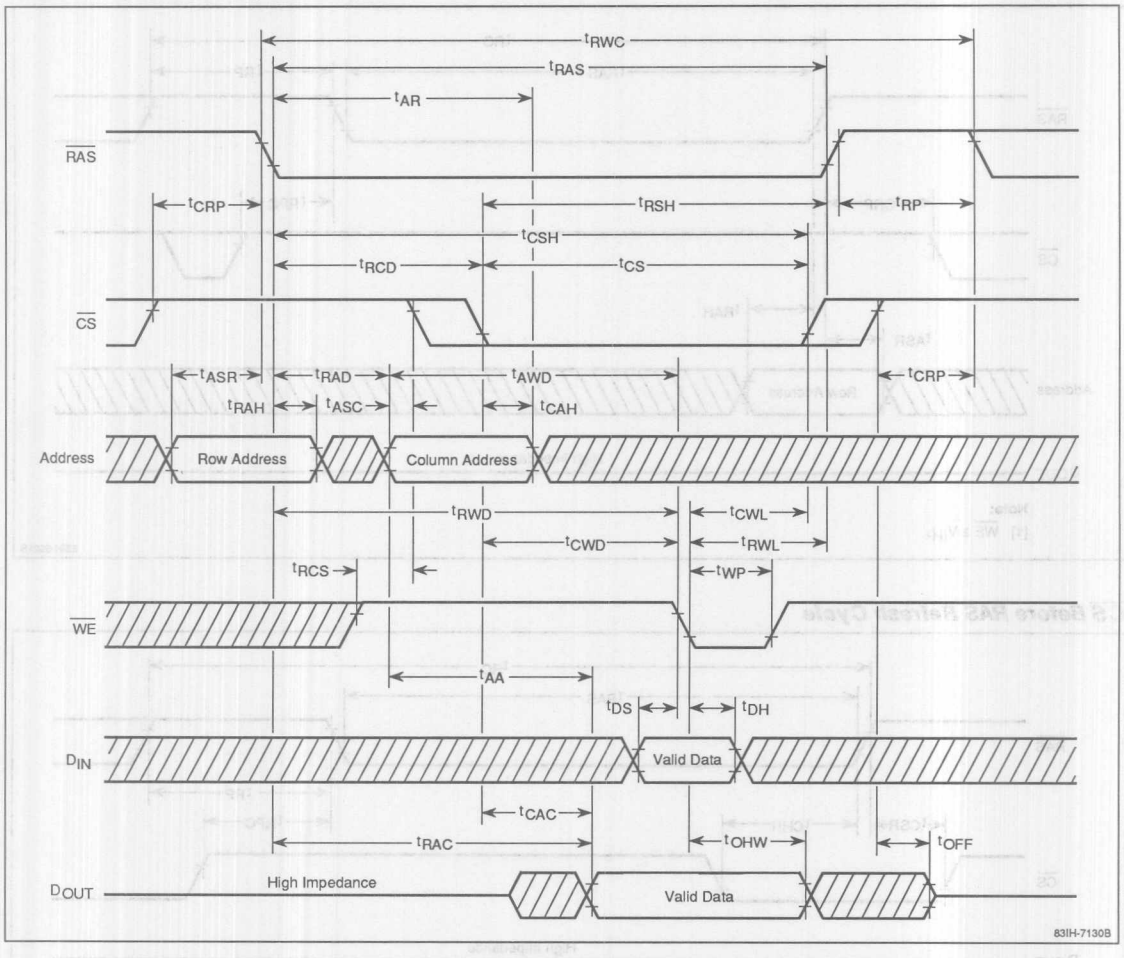
Timing Waveforms (cont)

Early Write Cycle



Timing Waveforms (cont)

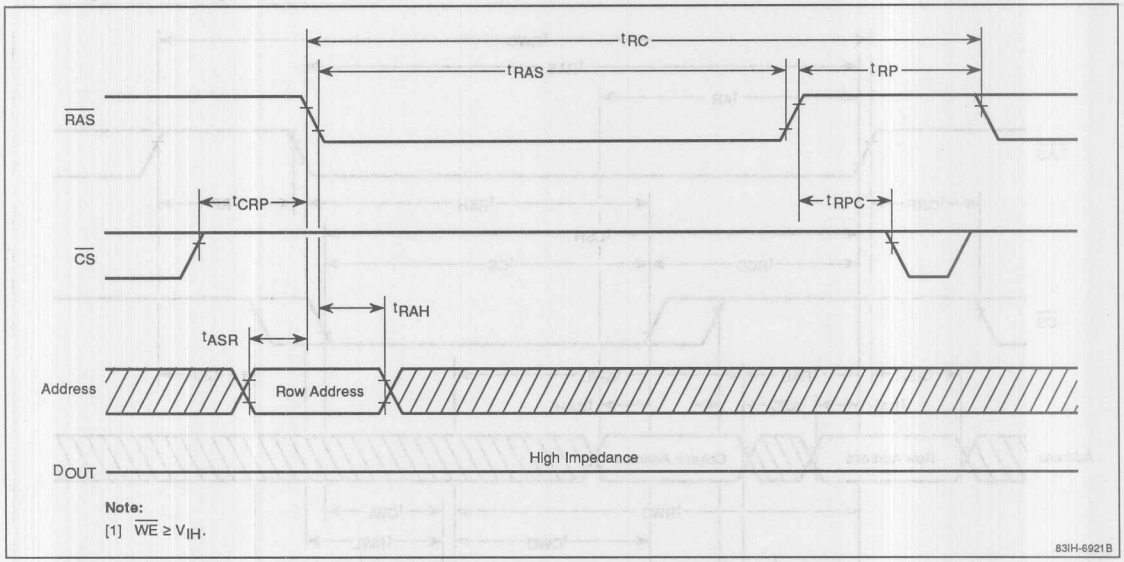
Read-Write/Read-Modify-Write Cycle



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Timing Waveforms (cont)

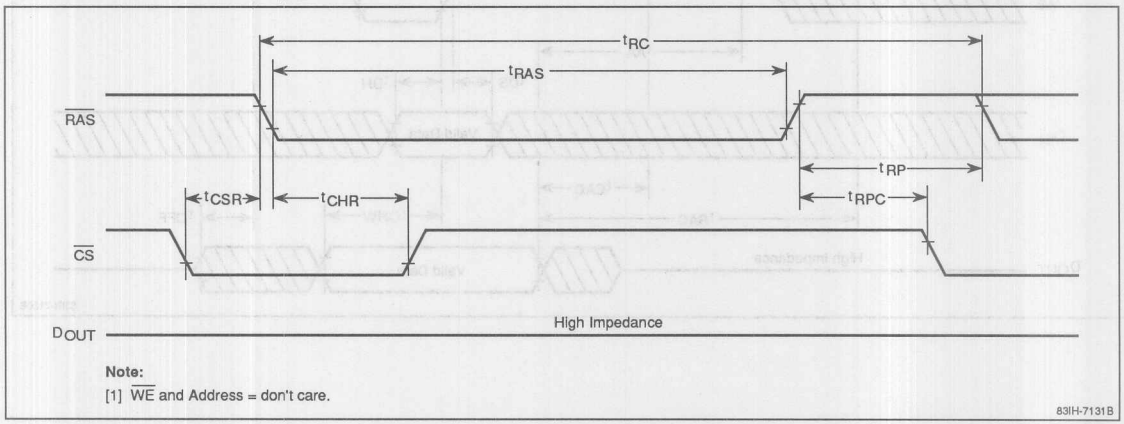
$\overline{RAS}$-Only Refresh Cycle



Note:
[1] $\overline{WE} \geq V_{IH}$.

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$\overline{CS}$ Before $\overline{RAS}$ Refresh Cycle

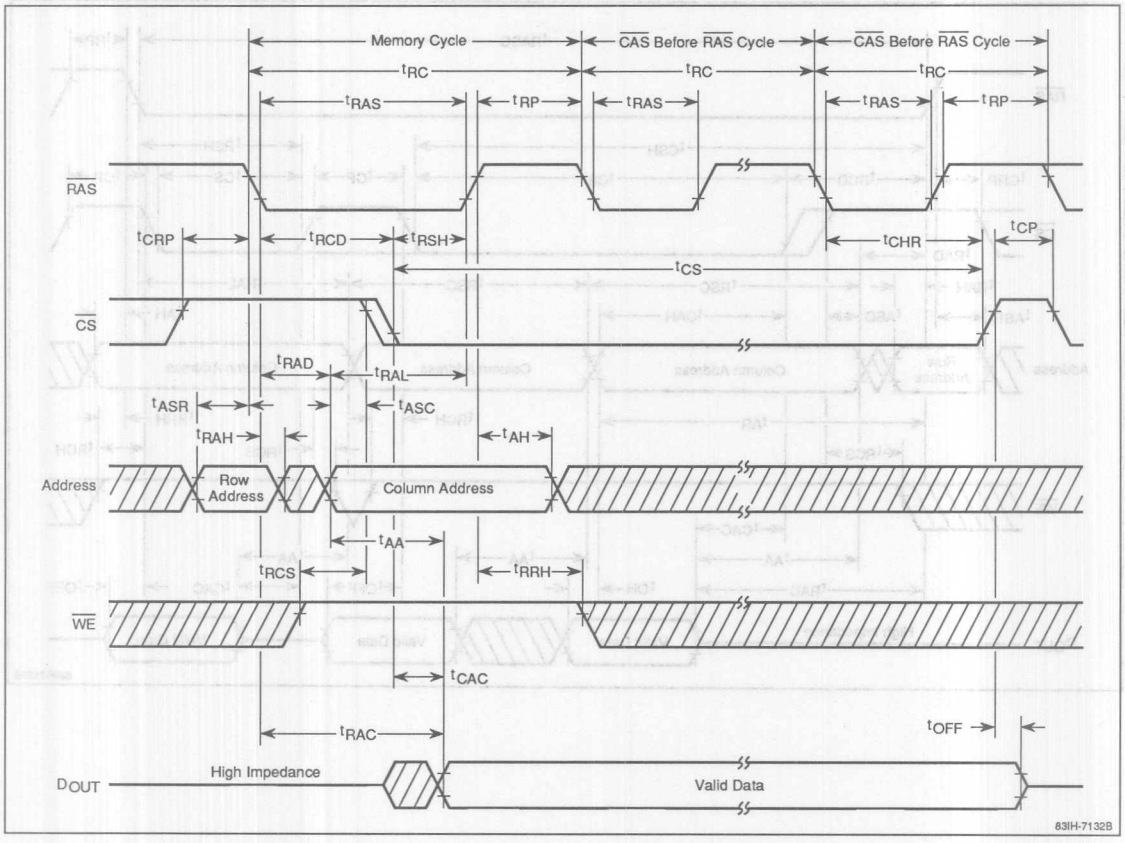


Note:
[1] $\overline{WE}$ and Address = don't care.

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Timing Waveforms (cont)

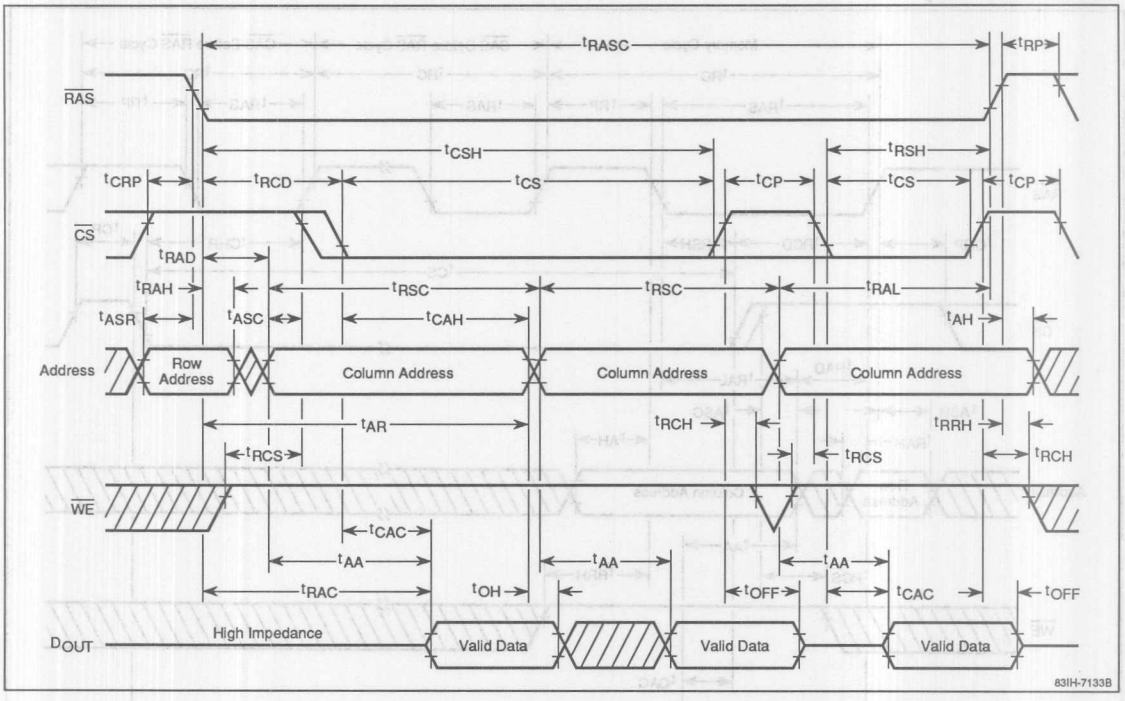
Hidden Refresh Cycle



6

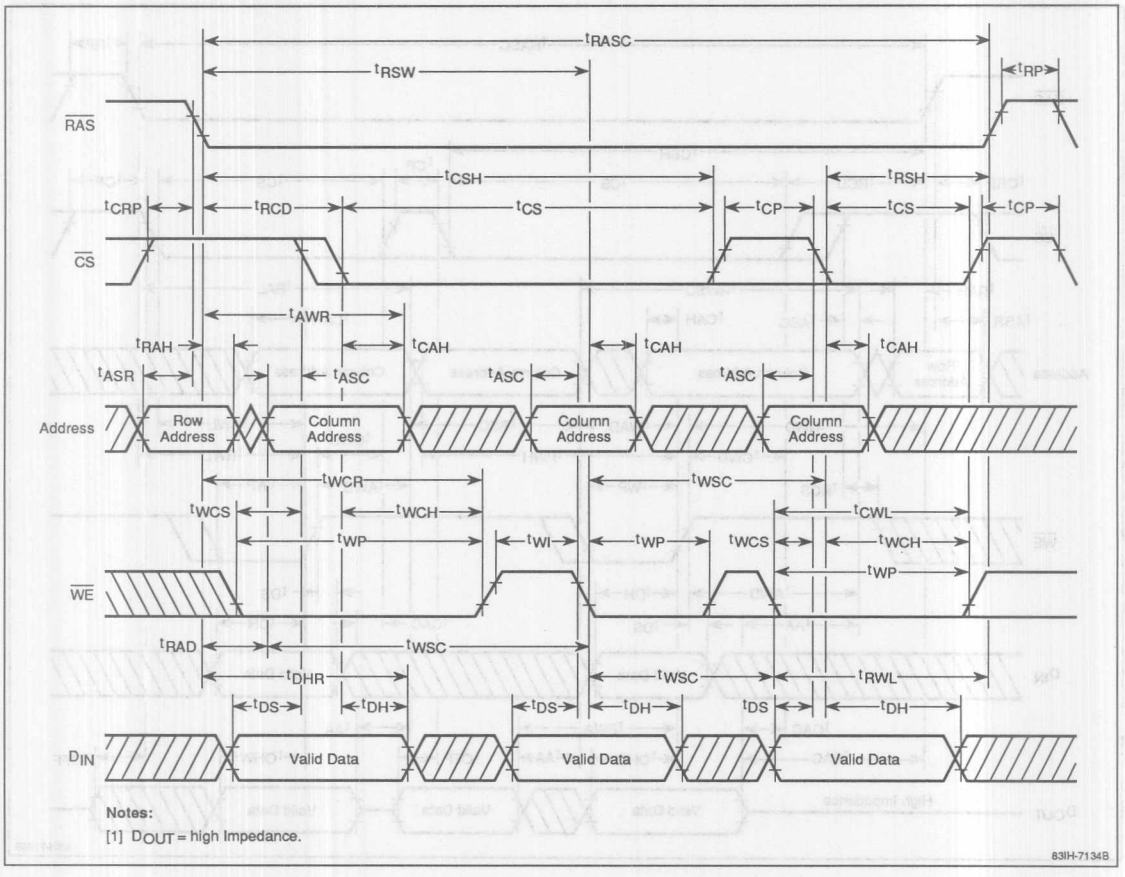
Timing Waveforms (cont)

Static-Column Read Cycle



Timing Waveforms (cont)

Static-Column Early Write Cycle



Notes:

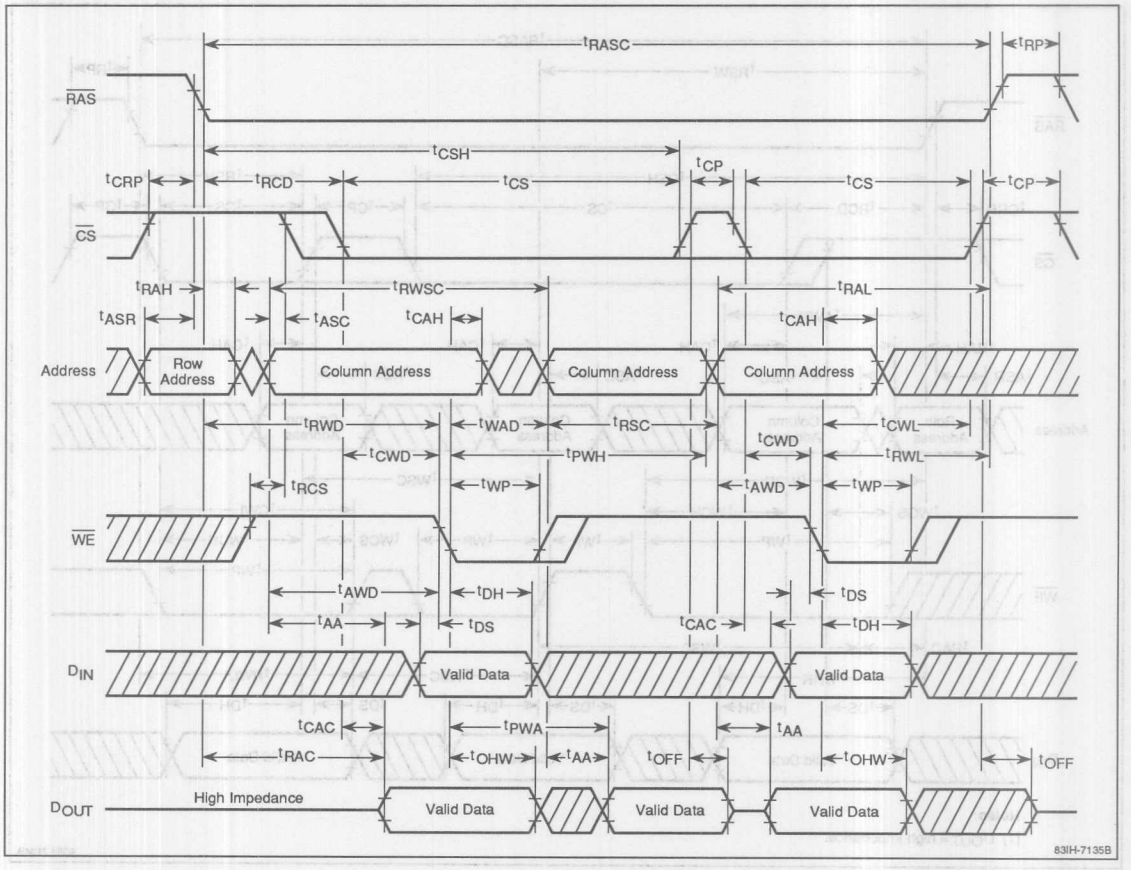
[1] D_{OUT} = high Impedance.

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Timing Waveforms (cont)

Static-Column Read-Write/Read-Modify-Write Cycle



Description

The μPD424256 is a fast-page dynamic RAM organized as 262,144 words by 4 bits and designed to operate from a single +5-volt power supply. Advanced polycide technology using trench capacitors minimizes silicon area and provides high storage cell capacity, high performance, and high reliability. A single-transistor dynamic storage cell and advanced CMOS circuitry throughout ensure minimum power dissipation, while an on-chip circuit generates the negative-voltage substrate bias automatically and transparently.

The three-state I/O pins are controlled by $\overline{CAS}$ independent of $\overline{RAS}$. After a valid read or read-modify-write cycle, data is held on the outputs by maintaining $\overline{CAS}$ low. The data outputs are returned to high impedance by returning $\overline{CAS}$ high. Fast-page read and write cycles can be executed by cycling $\overline{CAS}$.

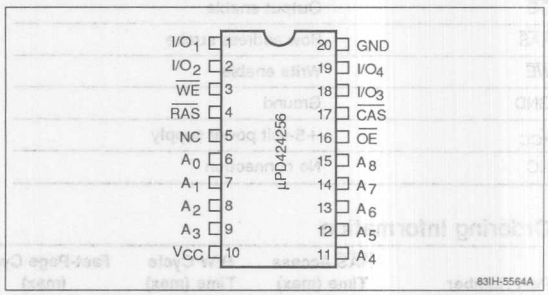
Refreshing may be accomplished by means of a $\overline{CAS}$ before $\overline{RAS}$ cycle whereby the refresh addresses are internally generated. Refreshing may also be accomplished by means of $\overline{RAS}$-only refresh cycles or by normal read or write cycles on the 512 address combinations of A_0 through A_8 during an 8-ms refresh period (64 ms for -L versions).

Features

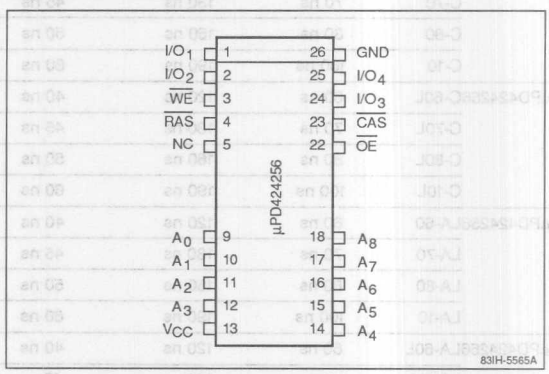
- 262,144-word by 4-bit organization
- Single +5-volt ±10% power supply
- Fast-page option
- Low power available in -L version
- $\overline{CAS}$ before $\overline{RAS}$ internal refreshing
- Multiplexed address inputs
- On-chip substrate bias generator
- Nonlatched, three-state I/O
- TTL-compatible inputs and outputs
- High-density 20-pin plastic DIP, 26/20-pin plastic SOJ, or 20-pin plastic ZIP packaging

Pin Configurations

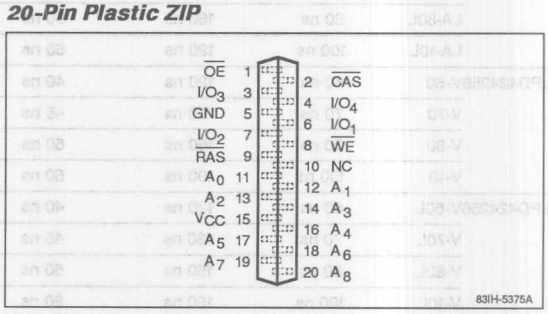
20-Pin Plastic DIP



26/20-Pin Plastic SOJ



20-Pin Plastic ZIP



6

Pin Identification

Name	Function
A_0 - A_8	Address inputs
I/O_1 - I/O_4	Data inputs and outputs
$\overline{CAS}$	Column address strobe
$\overline{OE}$	Output enable
$\overline{RAS}$	Row address strobe
$\overline{WE}$	Write enable
GND	Ground
V_{CC}	+5-volt power supply
NC	No connection

Absolute Maximum Ratings

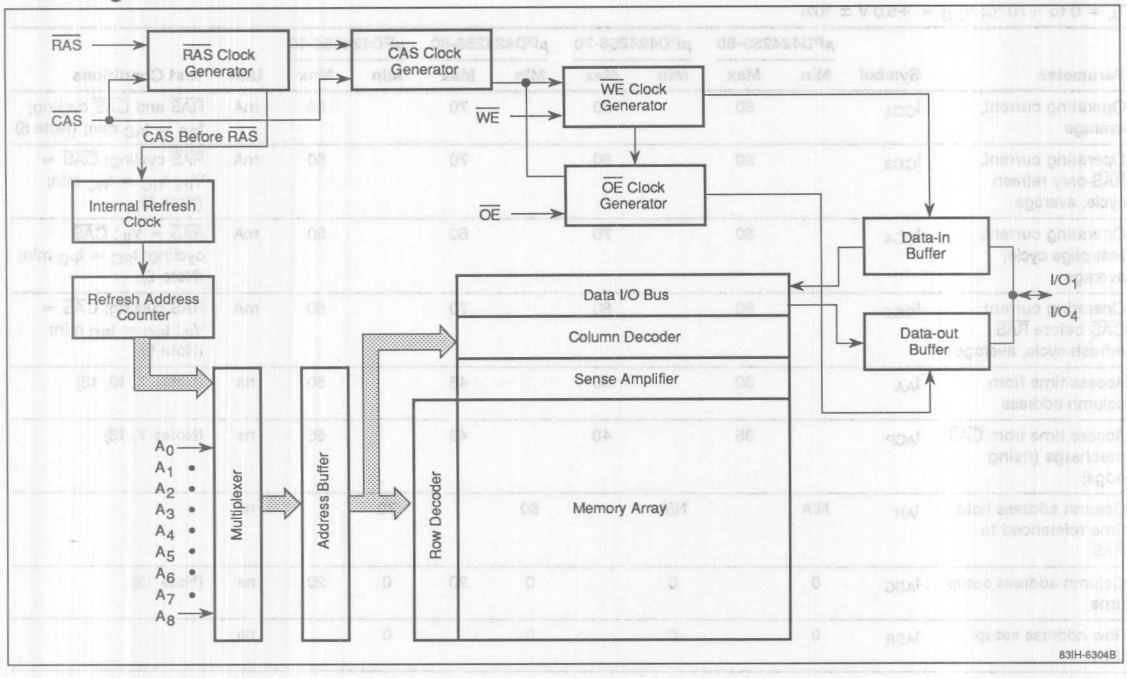
Voltage on any pin relative to GND	−1.0 to +7.0 V
Operating temperature, T_{OPR}	0 to +70 °C
Storage temperature, T_{STG}	−55 to +125 °C
Short-circuit output current, I_{OS}	50 mA
Power dissipation, P_D	1.0 W

Exposure to Absolute Maximum Ratings for extended periods may affect device reliability; exceeding the ratings could cause permanent damage. The device should be operated within the limits specified under DC and AC Characteristics.

Ordering Information

Part Number	$\overline{RAS}$ Access Time (max)	R/W Cycle Time (max)	Fast-Page Cycle (max)	Refresh Period	Standby Current (min)	Package
μPD424256C-60	60 ns	120 ns	40 ns	8 ms	1 mA	20-pin plastic DIP
C-70	70 ns	130 ns	45 ns			
C-80	80 ns	160 ns	50 ns			
C-10	100 ns	190 ns	60 ns			
μPD424256C-60L	60 ns	120 ns	40 ns	64 ms	200 μA	
C-70L	70 ns	130 ns	45 ns			
C-80L	80 ns	160 ns	50 ns			
C-10L	100 ns	190 ns	60 ns			
μPD424256LA-60	60 ns	120 ns	40 ns	8 ms	1 mA	26/20-pin plastic SOJ
LA-70	70 ns	130 ns	45 ns			
LA-80	80 ns	160 ns	50 ns			
LA-10	100 ns	190 ns	60 ns			
μPD424256LA-60L	60 ns	120 ns	40 ns	64 ms	200 μA	
LA-70L	70 ns	130 ns	45 ns			
LA-80L	80 ns	160 ns	50 ns			
LA-10L	100 ns	190 ns	60 ns			
μPD424256V-60	60 ns	120 ns	40 ns	8 ms	1 mA	20-pin plastic ZIP
V-70	70 ns	130 ns	45 ns			
V-80	80 ns	160 ns	50 ns			
V-10	100 ns	190 ns	60 ns			
μPD424256V-60L	60 ns	120 ns	40 ns	64 ms	200 μA	
V-70L	70 ns	130 ns	45 ns			
V-80L	80 ns	160 ns	50 ns			
V-10L	100 ns	190 ns	60 ns			

Block Diagram



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Recommended Operating Conditions

Parameter	Symbol	Min	Typ	Max	Unit
Input voltage, high	V_{IH}	2.4		V_{CC} + 1.0	V
Input voltage, low	V_{IL}	−1.0		0.8	V
Supply voltage	V_{CC}	4.5	5.0	5.5	V
Ambient temperature	T_A	0		70	°C

Capacitance

T_A = 25 °C; f = 1 MHz

Parameter	Symbol	Max	Unit	Pins Under Test
Input capacitance	C_{I1}	5	pF	Address
	C_{I2}	7	pF	$\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$, $\overline{OE}$
Input/output capacitance	C_{IO}	7	pF	I/O

DC Characteristics

T_A = 0 to +70°C; V_{CC} = +5.0 ±10%

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions
Standby current	I_{CC2}			2.0	mA	$\overline{RAS}$ = $\overline{CAS}$ = V_{IH}
				1.0	mA	$\overline{RAS}$ = $\overline{CAS}$ ≥ V_{CC} − 0.2 V
Input leakage current	$I_{I(L)}$	−10		10	μA	V_{IN} = 0 to 5.5 V; all other pins not under test = 0 V
Output leakage current	$I_{O(L)}$	−10		10	μA	D_{OUT} disabled; V_{OUT} = 0 to 5.5 V
Output voltage, low	V_{OL}			0.4	V	I_{OL} = 4.2 mA
Output voltage, high	V_{OH}	2.4			V	I_{OH} = −5 mA

AC Characteristics

T_A = 0 to +70 °C; V_{CC} = +5.0 V ± 10%

		μPD424256-60		μPD424256-70		μPD424256-80		μPD424256-10			
Parameter	**Symbol**	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**	**Unit**	**Test Conditions**
Operating current, average	I_{CC1}		90		80		70		60	mA	$\overline{RAS}$ and $\overline{CAS}$ cycling; $t_{RC} = t_{RC}$ min; (Note 5)
Operating current, $\overline{RAS}$-only refresh cycle, average	I_{CC3}		90		80		70		60	mA	$\overline{RAS}$ cycling; $\overline{CAS}$ = V_{IH}; $t_{RC} = t_{RC}$ min; (Note 5)
Operating current, fast-page cycle, average	I_{CC4}		80		70		60		50	mA	$\overline{RAS} = V_{IL}$; $\overline{CAS}$ cycling; $t_{PC} = t_{PC}$ min; (Note 5)
Operating current, $\overline{CAS}$ before $\overline{RAS}$ refresh cycle, average	I_{CC5}		90		80		70		60	mA	$\overline{RAS}$ cycling; $\overline{CAS}$ = V_{IL}; $t_{RC} = t_{RC}$ min; (Note 5)
Access time from column address	t_{AA}		30		35		45		50	ns	(Notes 7, 10, 13)
Access time from $\overline{CAS}$ precharge (rising edge)	t_{ACP}		35		40		45		55	ns	(Notes 7, 13)
Column address hold time referenced to $\overline{RAS}$	t_{AR}	N/A		N/A		60		70		ns	
Column address setup time	t_{ASC}	0		0		0	20	0	20	ns	(Note 13)
Row address setup time	t_{ASR}	0		0		0		0		ns	
Column address to $\overline{WE}$ delay time	t_{AWD}	50		55		70		80		ns	(Note 18)
Access time from $\overline{CAS}$ (falling edge)	t_{CAC}		20		20		20		25	ns	(Notes 7, 9, 10, 13)
Column address hold time	t_{CAH}	15		17		20		20		ns	
$\overline{CAS}$ pulse width	t_{CAS}	20	10,000	20	10,000	20	10,000	25	10,000	ns	
$\overline{CAS}$ hold time for $\overline{CAS}$ before $\overline{RAS}$ refresh cycle	t_{CHR}	15		15		15		20		ns	
$\overline{CAS}$ precharge time, fast-page cycle	t_{CP}	10		10	15	10	20	10	25	ns	(Note 13)
$\overline{CAS}$ precharge time, nonpage cycle	t_{CPN}	10		10		10		10		ns	
$\overline{CAS}$ to $\overline{RAS}$ precharge time	t_{CRP}	10		10		10		10		ns	(Note 14)
$\overline{CAS}$ hold time	t_{CSH}	60		70		80		100		ns	
$\overline{CAS}$ setup time for $\overline{CAS}$ before $\overline{RAS}$ refresh cycle	t_{CSR}	10		10		10		10		ns	
$\overline{CAS}$ to $\overline{WE}$ delay	t_{CWD}	40		40		45		55		ns	(Note 18)
Write command to $\overline{CAS}$ lead time	t_{CWL}	15		15		20		20		ns	
Data-in hold time	t_{DH}	15		15		20		20		ns	(Note 17)

AC Characteristics (cont)

Parameter	Symbol	μPD424256-60		μPD424256-70		μPD424256-80		μPD424256-10		Unit	Test Conditions
		Min	Max	Min	Max	Min	Max	Min	Max		
Data-in hold time referenced to $\overline{RAS}$	t_{DHR}	N/A		N/A		60		70		ns	
Data-in setup time	t_{DS}	0		0		0		0		ns	(Note 17)
Access time from $\overline{OE}$	t_{OEA}		20		20		20		25	ns	
$\overline{OE}$ data delay time	t_{OED}	15		15		20		25		ns	
$\overline{OE}$ command hold time	t_{OEH}	0		0		0		0		ns	
$\overline{OE}$ to $\overline{RAS}$ inactive setup time	t_{OES}	0		0		0		0		ns	
Output turnoff delay from $\overline{OE}$	t_{OEZ}	0	15	0	15	0	20	0	25	ns	(Note 11)
Output buffer turnoff delay	t_{OFF}	0	15	0	15	0	20	0	25	ns	(Note 11)
Fast-page cycle time	t_{PC}	40		45		50		60		ns	(Note 6)
Fast-page read-write cycle time	t_{PRWC}	85		90		105		125		ns	
Access time from $\overline{RAS}$	t_{RAC}		60		70		80		100	ns	(Notes 7, 8)
$\overline{RAS}$ to column address delay time	t_{RAD}	15	30	15	35	17	35	17	50	ns	(Note 10)
Row address hold time	t_{RAH}	10		10		12		12		ns	
Column address lead time referenced to $\overline{RAS}$ (rising edge)	t_{RAL}	30		35		45		50		ns	
$\overline{RAS}$ pulse width	t_{RAS}	60	10,000	70	10,000	80	10,000	100	10,000	ns	
$\overline{RAS}$ pulse width, fast-page cycle	t_{RASP}	160	100,000	70	100,000	80	100,000	100	100,000	ns	
Random read or write cycle time	t_{RC}	120		130		160		190		ns	(Note 6)
$\overline{RAS}$ to $\overline{CAS}$ delay time	t_{RCD}	20	40	20	50	25	60	25	75	ns	(Note 12)
Read command hold time referenced to $\overline{CAS}$	t_{RCH}	0		0		0		0		ns	(Note 15)
Read command setup time	t_{RCS}	0		0		0		0		ns	
Refresh period	t_{REF}		8		8		8		8	ms	Addresses A_0 - A_8; 64 ms for -L versions
$\overline{RAS}$ precharge time	t_{RP}	50		50		70		80		ns	
$\overline{RAS}$ precharge $\overline{CAS}$ hold time	t_{RPC}	10		10		10		10		ns	
Read command hold time referenced to $\overline{RAS}$	t_{RRH}	10		10		10		10		ns	(Note 15)
$\overline{RAS}$ hold time	t_{RSH}	20		20		20		25		ns	
Read-write cycle time	t_{RWC}	165		175		215		255		ns	(Note 6)
$\overline{RAS}$ to $\overline{WE}$ delay	t_{RWD}	80		90		105		130		ns	(Note 18)

AC Characteristics (cont)

Parameter	Symbol	μPD424256-60 Min	μPD424256-60 Max	μPD424256-70 Min	μPD424256-70 Max	μPD424256-80 Min	μPD424256-80 Max	μPD424256-10 Min	μPD424256-10 Max	Unit	Test Conditions
Write command to $\overline{RAS}$ lead time	t_{RWL}	20		20		25		30		ns	
Rise and fall transition time	t_T	3	50	3	50	3	50	3	50	ns	(Note 4)
Write command hold time	t_{WCH}	15		15		15		20		ns	
Write command hold time referenced to $\overline{RAS}$	t_{WCR}	N/A		N/A		55		70		ns	
Write command setup time	t_{WCS}	0		0		0		0		ns	(Note 18)
Write command pulse width	t_{WP}	15		15		15		20		ns	(Note 16)

Notes:

(1) All voltages are referenced to GND.

(2) An initial pause of 100 μs is required after power-up, followed by any eight $\overline{RAS}$ cycles, before proper device operation is achieved.

(3) Ac measurements assume t_T = 5 ns.

(4) V_{IH} (min) and V_{IL} (max) are reference levels for measuring the timing of input signals. Transition times are measured between V_{IH} and V_{IL}.

(5) I_{CC1}, I_{CC3}, I_{CC4}, and I_{CC5} depend on output loading and cycle rates. Specified values are obtained with the output open. I_{CC3} is measured assuming that all column address inputs are held at either a high level or a low level during $\overline{RAS}$-only refresh cycles. I_{CC4} is measured assuming that all column address inputs are switched only once during each fast-page cycle.

(6) The minimum specifications are used only to indicate the cycle time at which proper operation over the full temperature range (T_A=0 to +70 °C) is assured.

(7) Load = 2 TTL (–1 mA, +4 mA) loads and 100 pF (V_{OH}=2.0 V and V_{OL}=0.8 V).

(8) Assumes that $t_{RCD} \leq t_{RCD}$ (max) and $t_{RAD} \leq t_{RAD}$ (max). If t_{RCD} or t_{RAD} is greater than the maximum recommended value in this table, t_{RAC} increases by the amount that t_{RCD} or t_{RAD} exceeds the value shown.

(9) Assumes that $t_{RCD} \geq t_{RCD}$ (max) and $t_{RAD} \leq t_{RAD}$ (max).

(10) If $t_{RAD} \geq t_{RAD}$ (max), then the access time is defined by t_{AA}.

(11) t_{OFF} (max) and t_{OEZ} (max) define the time at which the outputs achieve the open-circuit condition and are not referenced to V_{OH} or V_{OL}.

(12) Operation with the t_{RCD} (max) limit assures that t_{RAC} (max) can be met. t_{RCD} (max) is specified as a reference point only; if t_{RCD} is greater than t_{RCD} (max), access time is controlled exclusively by t_{CAC}.

(13) For fast-page read operation, the definition of access time is as follows:

$\overline{CAS}$ and Column Address Input Conditions	Access Time Definition
$t_{CP} \leq t_{CP}$ (max), $t_{ASC} \geq t_{CP}$	t_{ACP}
$t_{CP} \leq _{CP}$ (max), $t_{ASC} \leq t_{CP}$	t_{AA}
$t_{CP} \geq _{CP}$ (max), $t_{ASC} \leq t_{ASC}$ (max)	t_{AA}
$t_{CP} \geq _{CP}$ (max), $t_{ASC} \geq t_{ASC}$ (max)	t_{CAC}

(14) The t_{CRP} requirement should be applicable for $\overline{RAS}$/$\overline{CAS}$ cycles preceded by any cycle.

(15) Either t_{RRH} or t_{RCH} must be satisfied for a read cycle.

(16) Parameter t_{WP} is applicable for a delayed write cycle such as a read-write/read-modify-write cycle. For early write cycles, both t_{WCS} and t_{WCH} must be met.

(17) These parameters are referenced to the falling edge of $\overline{CAS}$ for early write cycles and to the falling edge of $\overline{WE}$ for delayed write or read-modify-write cycles.

(18) t_{WCS}, t_{RWD}, t_{CWD}, and t_{AWD} are restrictive operating parameters in read-write/read-modify-write cycles only. If $t_{WCS} \geq t_{WCS}$ (min), the cycle is an early write cycle and the data I/O pins will remain open-circuit throughout the entire cycle. If $t_{CWD} \geq t_{CWD}$ (min), $t_{RWD} \geq t_{RWD}$ (min), and $t_{AWD} \geq t_{AWD}$ (min), then the cycle is a read-write cycle and the data I/O pins will contain data read from the selected cells. If neither of the above conditions is met, the condition of the data I/O pins (at access time and until $\overline{CAS}$ returns to V_{IH}) is indeterminate.

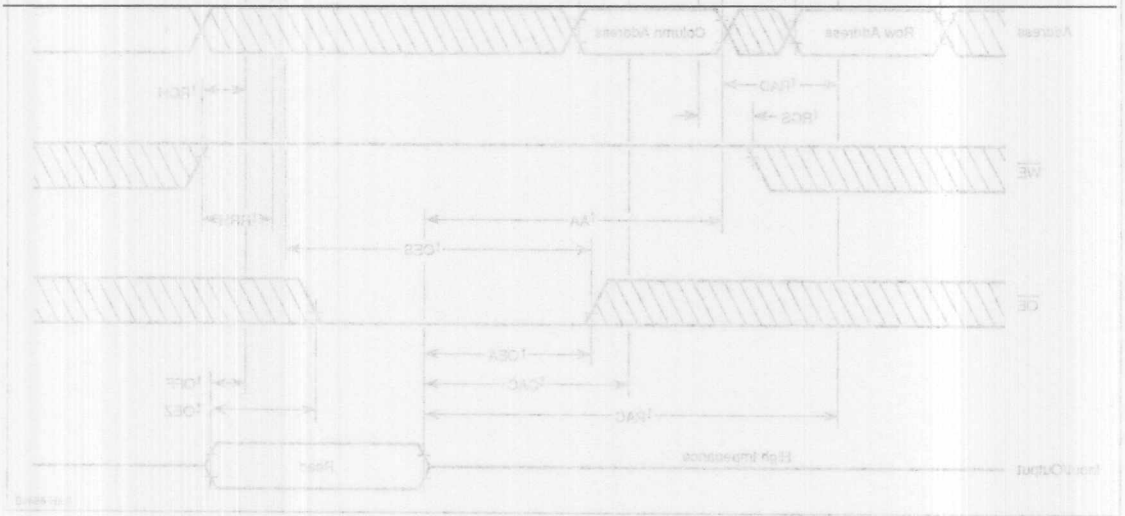
Low Power Battery Backup (-L Versions Only)

The μPD424256-L is capable of low power battery backup during times of reduced system power, when the input buffers and all nonessential internal circuits are turned off. For the input buffers to be turned off and the amount of leakage current flowing through them reduced, the μPD424256-L must be in standby and all control lines within 0.2 V of either V_{CC} or GND, as appropriate. When $\overline{RAS}$ and $\overline{CAS}$ are both within 0.2 V of V_{CC}, the internal circuits are inactive and power requirements reduced even further. Standby current can drop as low as 200 μA.

$\overline{CAS}$ before $\overline{RAS}$ refresh cycles are executed at a minimum rate to ensure that all 512 rows are refreshed only once every 64 ms. The time that $\overline{RAS}$ is low (t_{RAS}) and the μPD424256-L active needs to be as short as possible, typically less than 300 ns, to minimize power usage during refresh operation. The following table shows the conditions under which the lowest average standby current can be obtained.

Battery Backup Current

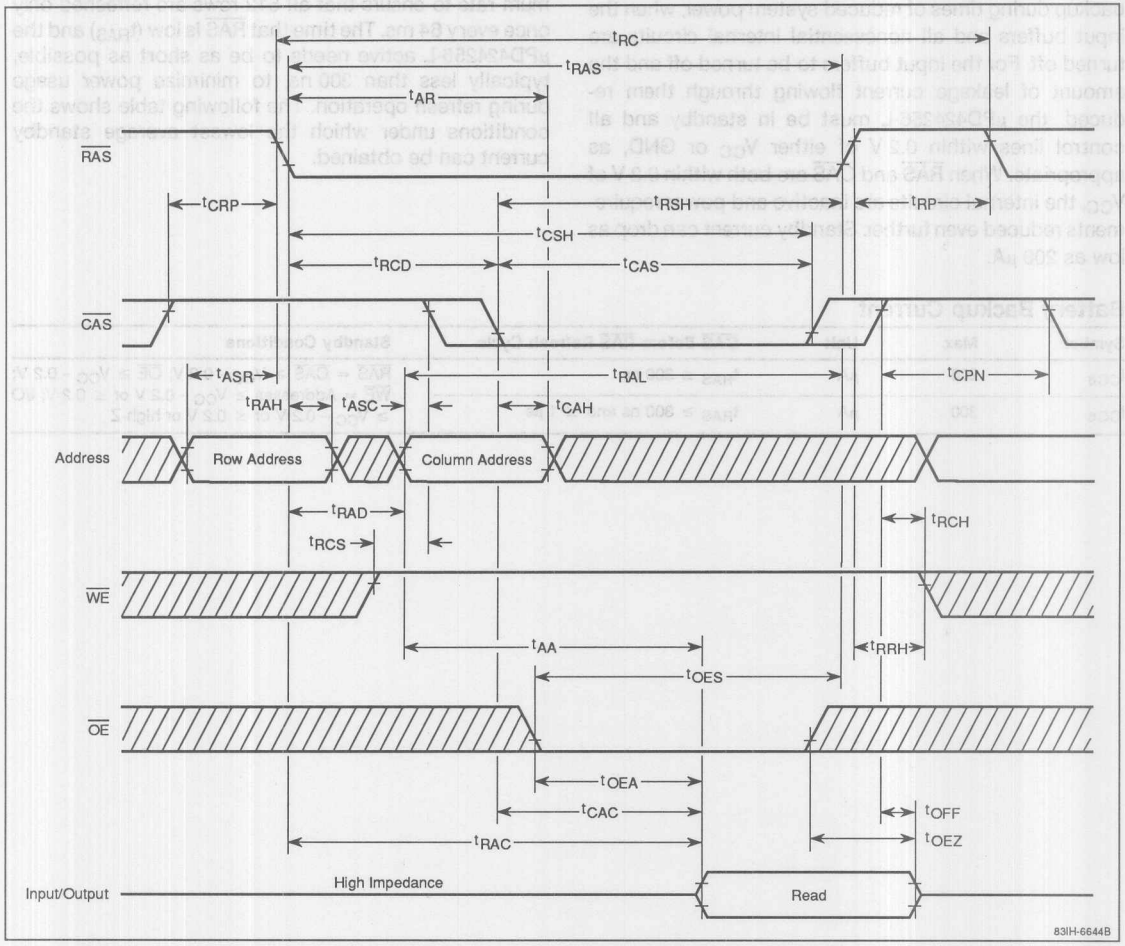
Symbol	Max	Unit	$\overline{CAS}$ Before $\overline{RAS}$ Refresh Cycle	Standby Conditions
I_{CC6}	200	μA	$t_{RAS} \leq 300$ ns	$\overline{RAS} = \overline{CAS} \geq V_{CC} - 0.2$ V; $\overline{OE} \geq V_{CC} - 0.2$ V; $\overline{WE}$ = Addresses $\geq V_{CC} - 0.2$ V or ≤ 0.2 V; I/O $\geq V_{CC} - 0.2$ V or ≤ 0.2 V or high-Z
I_{CC6}	300	μA	$t_{RAS} \geq 300$ ns and ≤ 1 μs	



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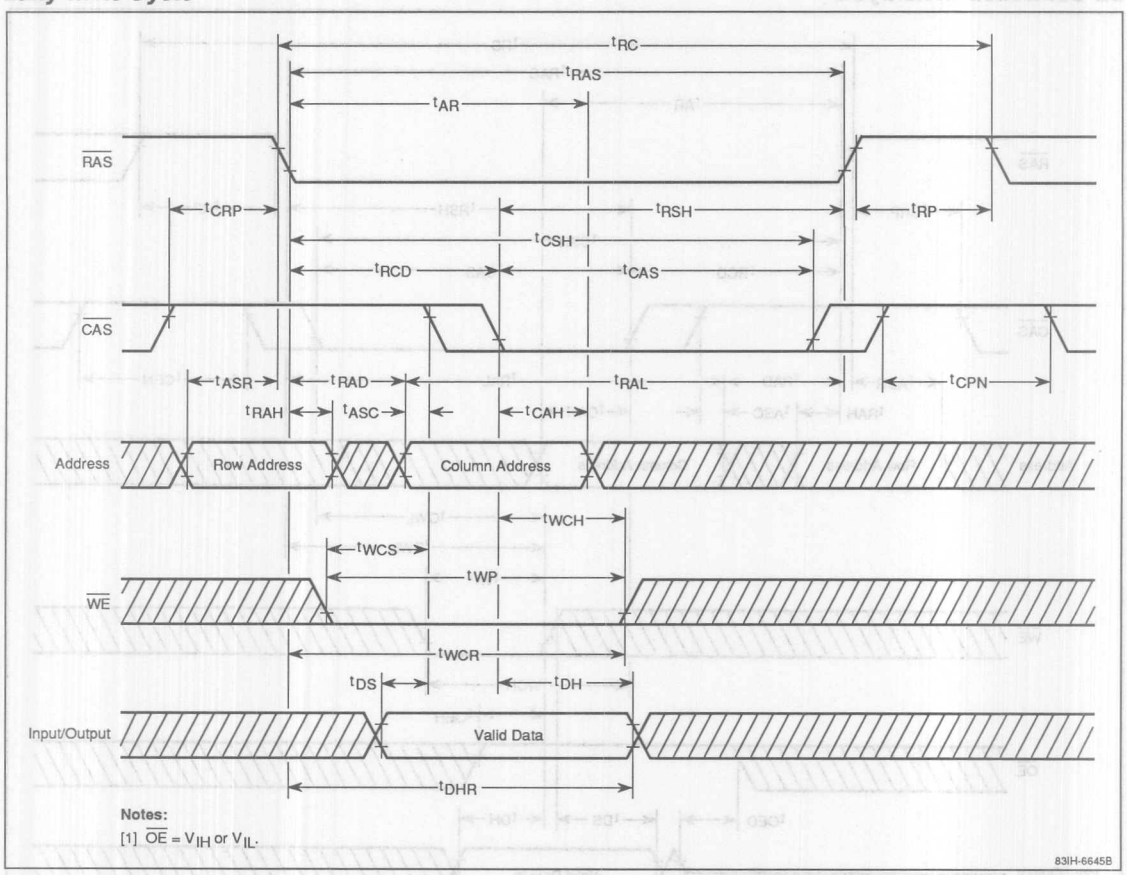
Timing Waveforms

Read Cycle



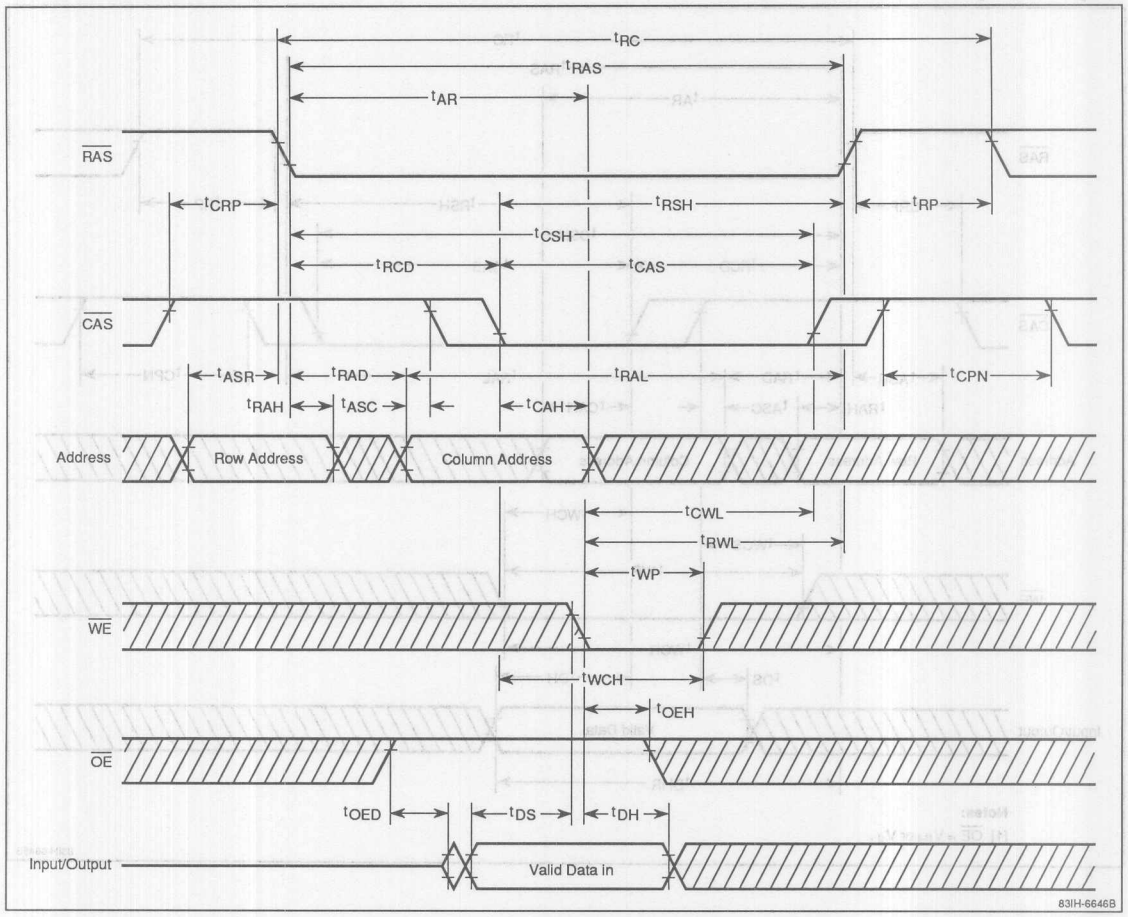
Timing Waveforms (cont)

Early Write Cycle



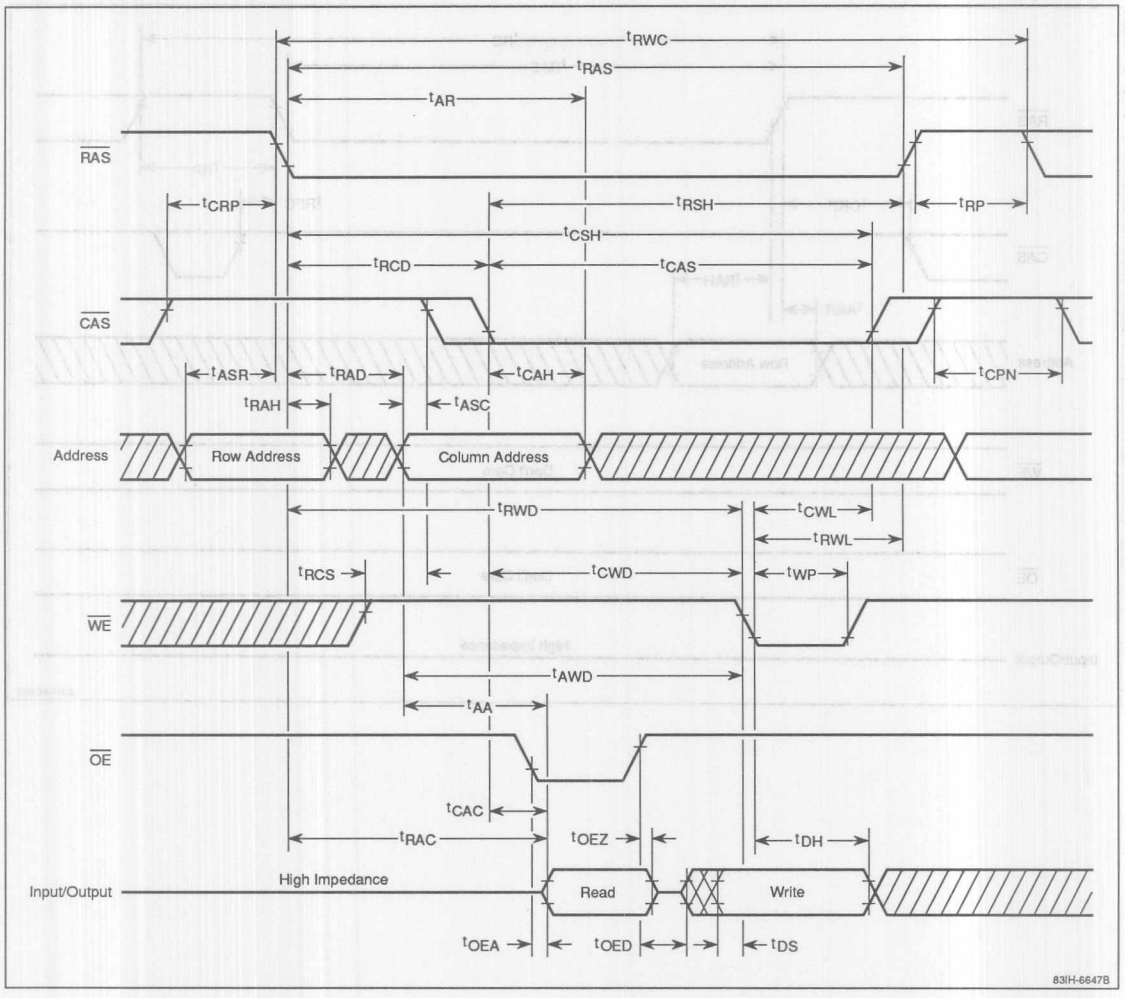
Timing Waveforms (cont)

$\overline{OE}$-Controlled Write Cycle



Timing Waveforms (cont)

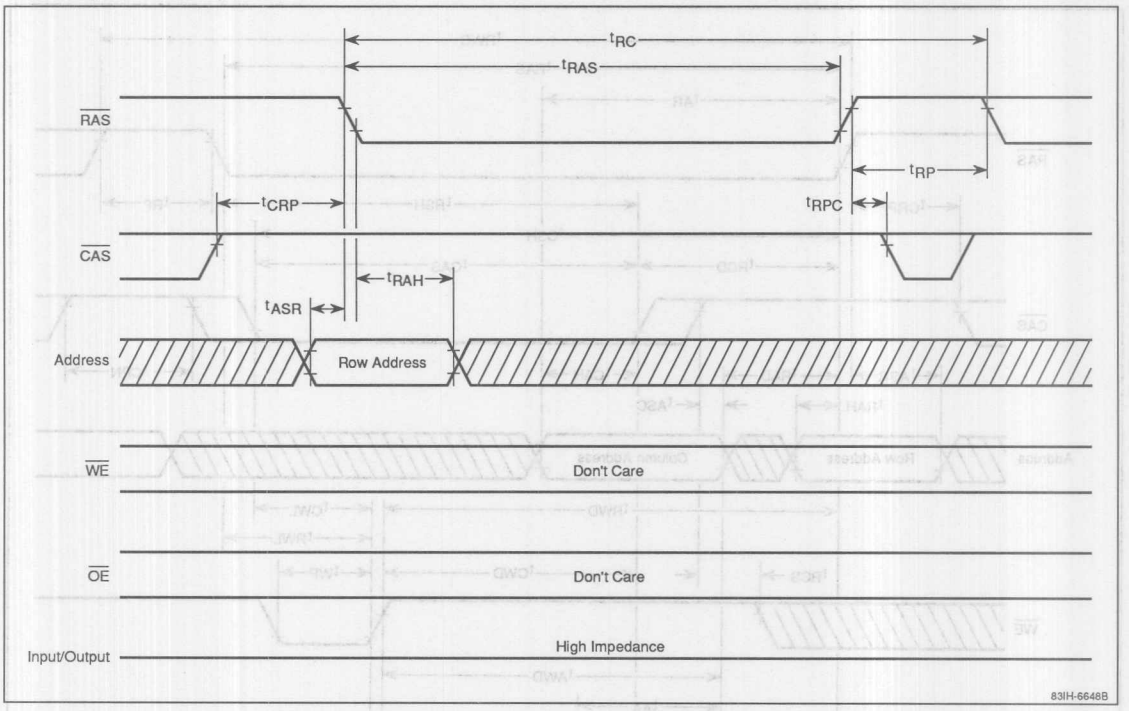
Read-Write/Read-Modify-Write Cycle



6

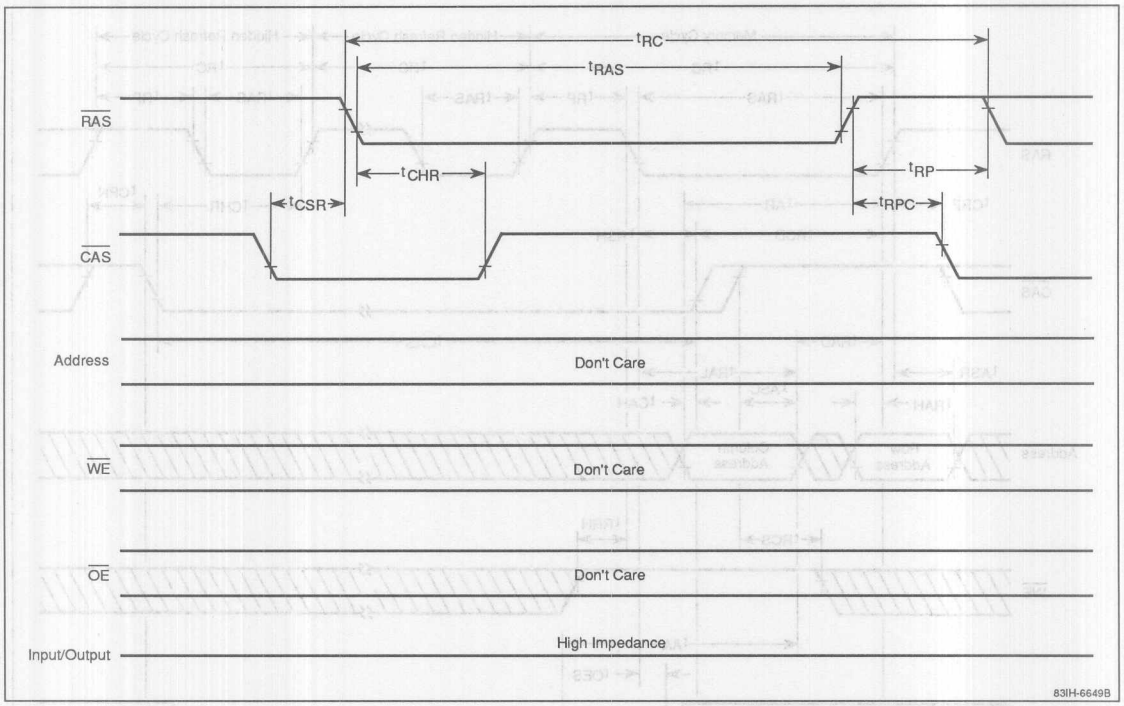
Timing Waveforms (cont)

$\overline{RAS}$-Only Refresh Cycle



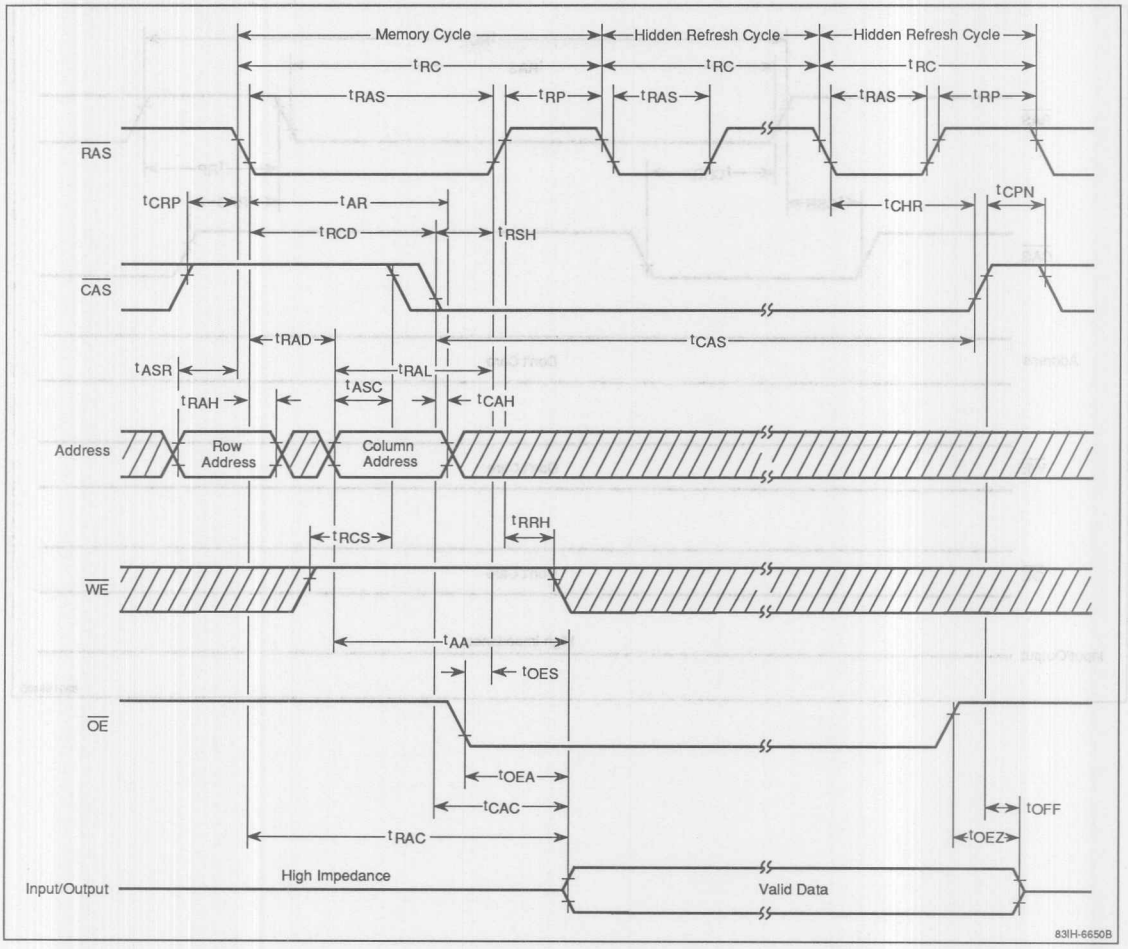
Timing Waveforms (cont)

$\overline{CAS}$ Before $\overline{RAS}$ Refresh Cycle



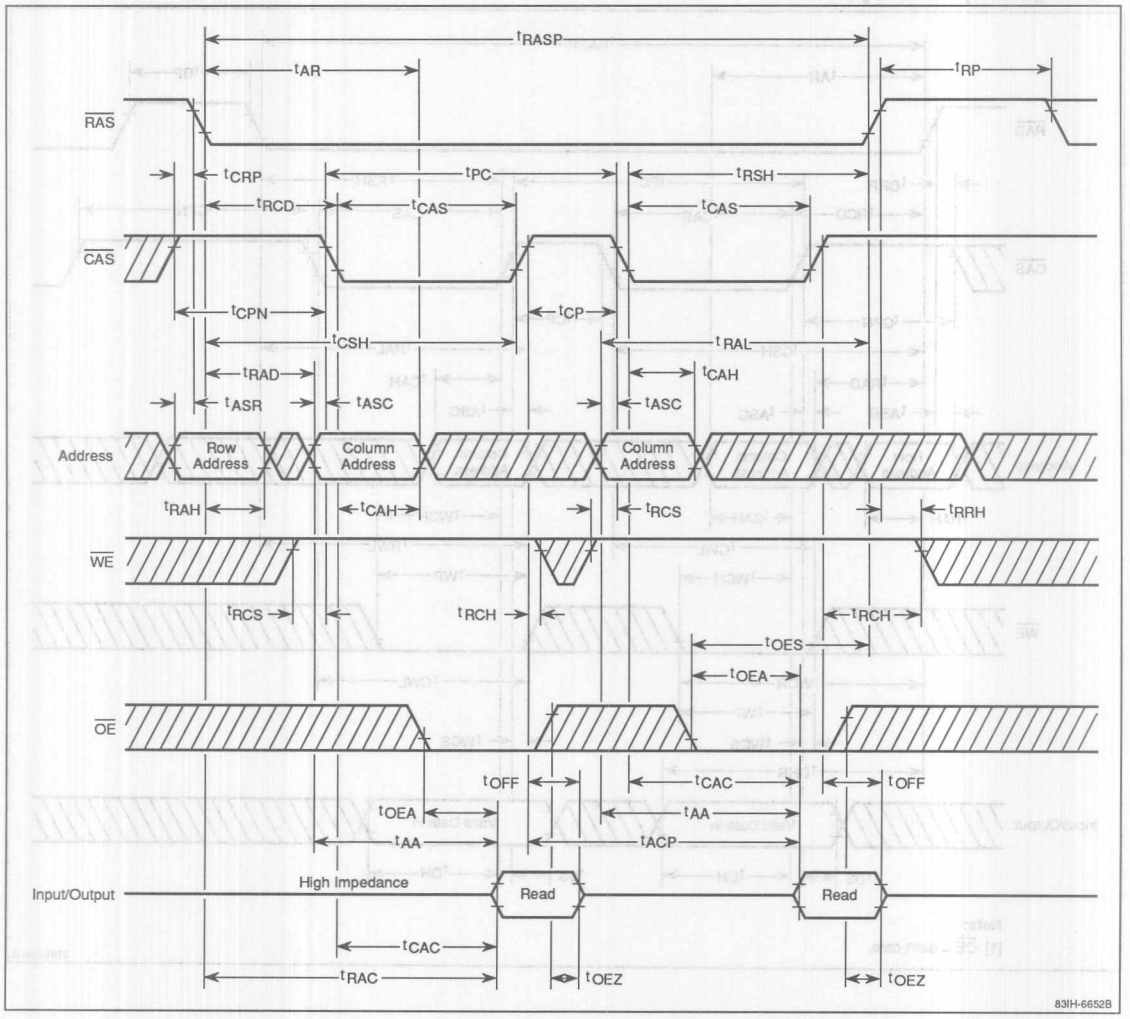
Timing Waveforms (cont)

Hidden Refresh Cycle



Timing Waveforms (cont)

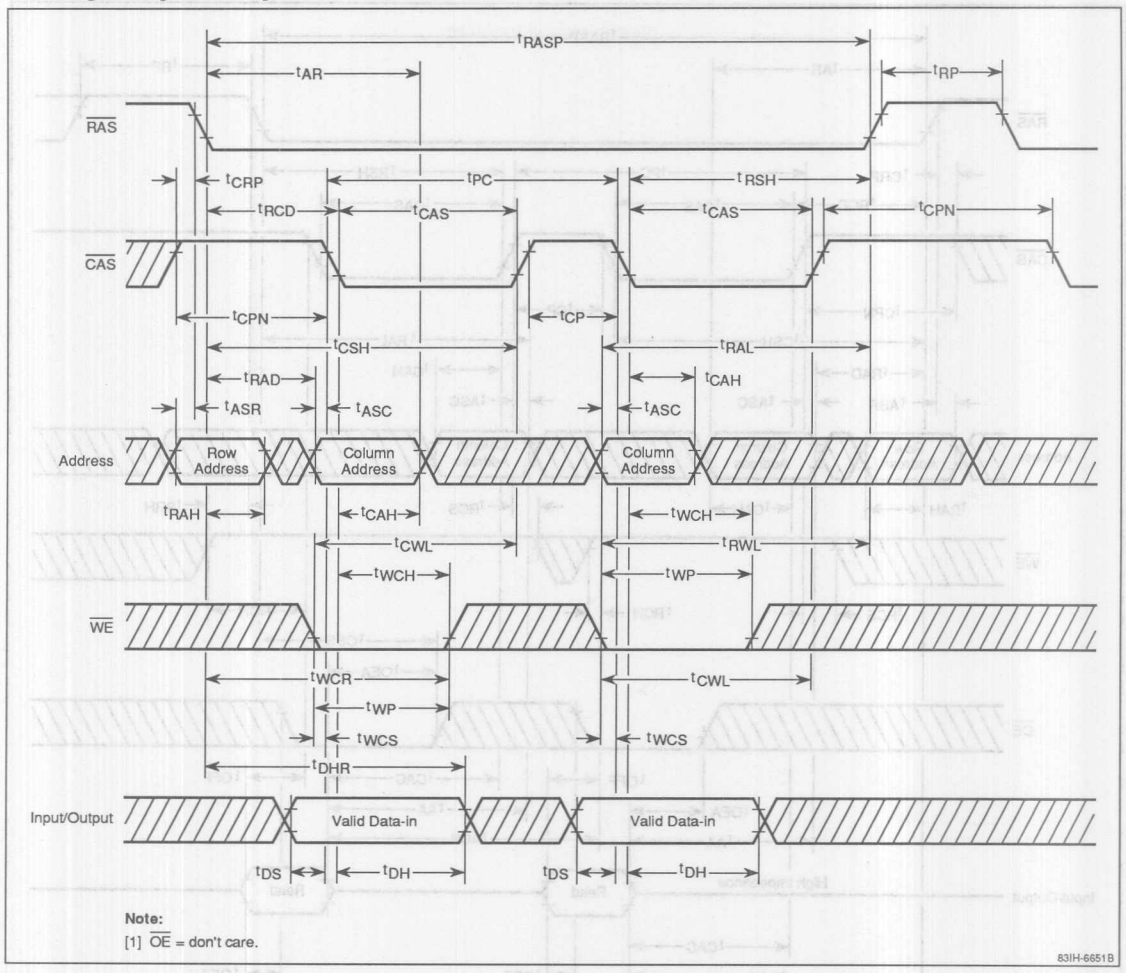
Fast-Page Read Cycle



6

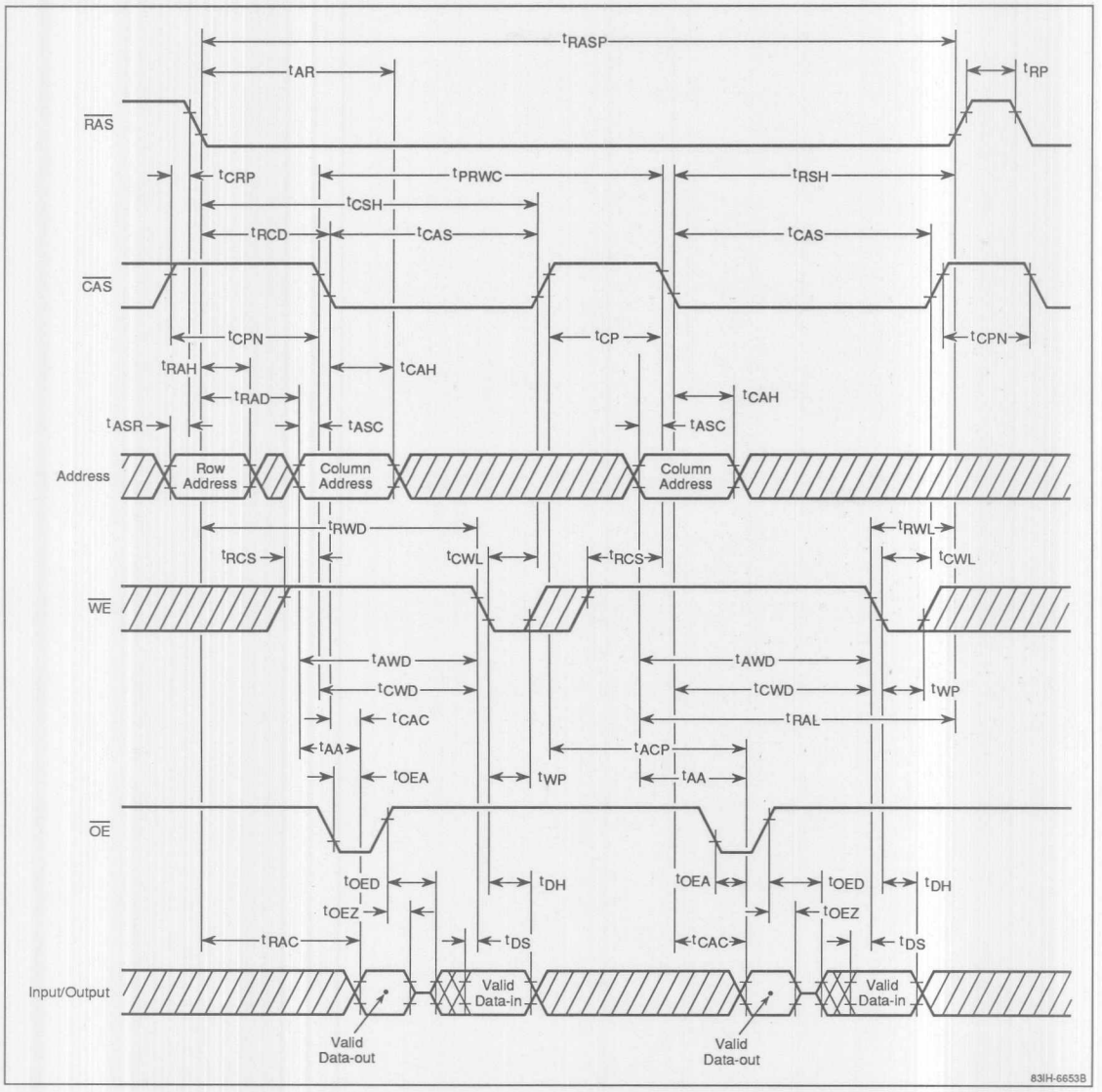
Timing Waveforms (cont)

Fast-Page Early Write Cycle

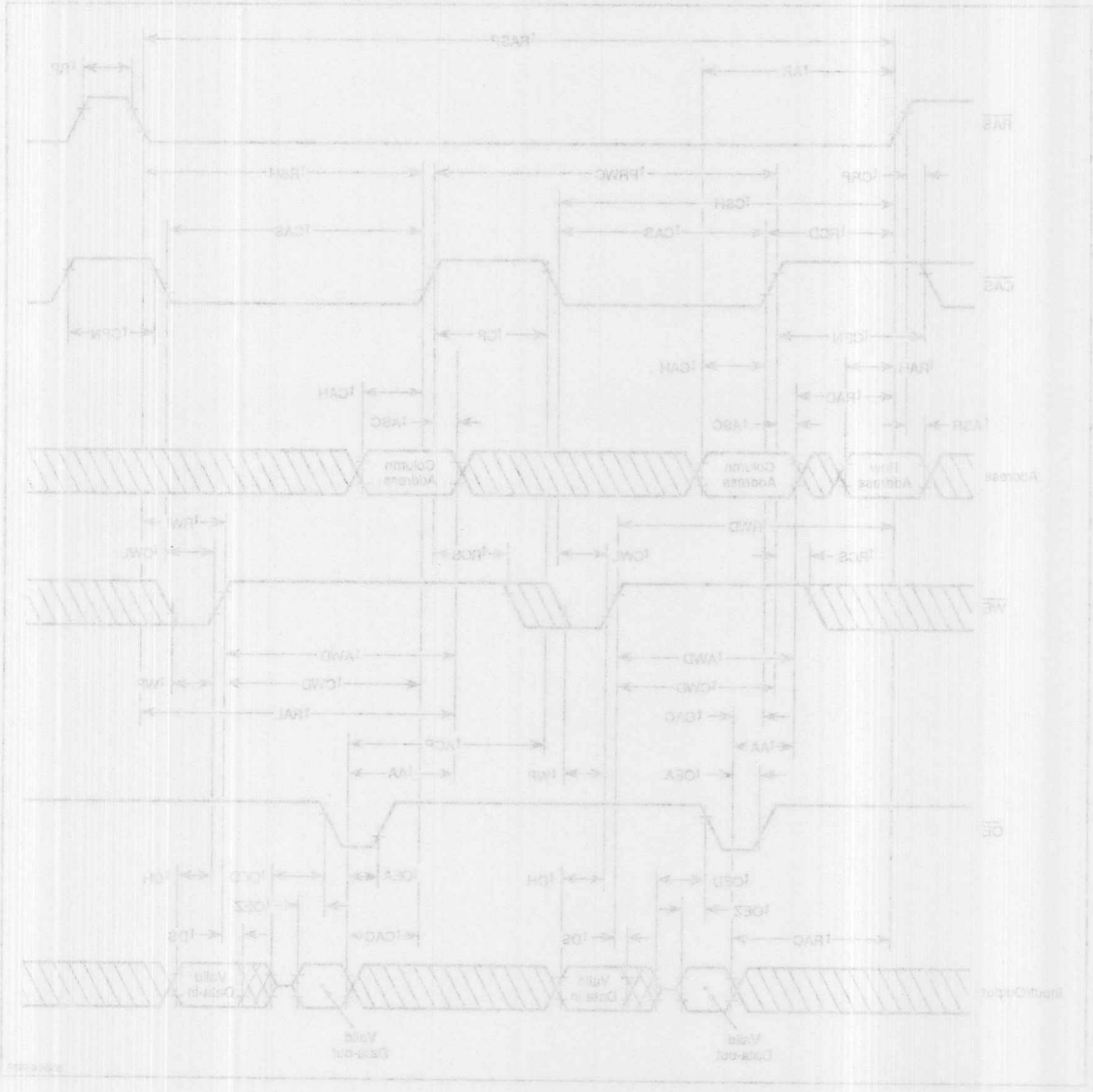


Timing Waveforms (cont)

Fast-Page Read-Write/Read-Modify-Write Cycle



6



μPD424258
262,144 x 4-Bit
Dynamic CMOS RAM

Description

The μPD424258 is a static-column dynamic RAM organized as 262,144 words by 4 bits and designed to operate from a single +5-volt power supply. Advanced polycide technology using trench capacitors minimizes silicon area and provides high storage cell capacity, high performance, and high reliability. A single-transistor dynamic storage cell and advanced CMOS circuitry throughout ensure minimum power dissipation, while an on-chip circuit generates the negative-voltage substrate bias—automatically and transparently.

The three-state I/O pins are controlled by $\overline{CS}$ independent of $\overline{RAS}$. After a valid read or read-modify-write cycle, data is held on the outputs by maintaining $\overline{CS}$ low. The data outputs are returned to high impedance by returning $\overline{CS}$ high. Static-column read and write cycles can be executed by switching the column address inputs.

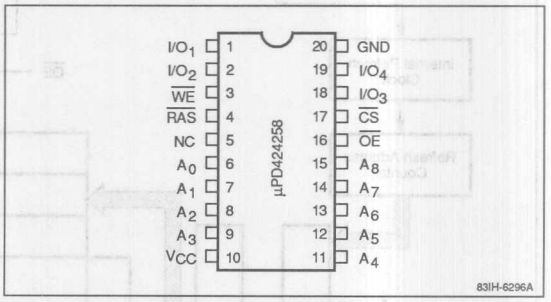
Refreshing may be accomplished by means of a $\overline{CS}$ before $\overline{RAS}$ cycle that internally generates the refresh address. Refreshing may also be accomplished by means of $\overline{RAS}$-only refresh cycles or by normal read and write cycles on the 512 address combinations of A_0 through A_8 during an 8-ms refresh period.

Features

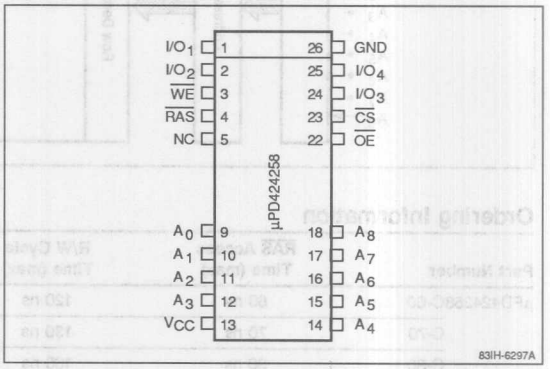
- 262,144-word by 4-bit organization
- Single +5-volt ±10% power supply
- Static-column option
- Low power dissipation
- $\overline{CS}$ before $\overline{RAS}$ internal refreshing
- Multiplexed address inputs
- On-chip substrate bias generator
- Nonlatched, three-state I/O
- Low input capacitance
- TTL-compatible inputs and outputs
- 512 refresh cycles every 8 ms
- High-density 20-pin plastic DIP, 26/20-pin plastic SOJ, or 20-pin plastic ZIP packaging

Pin Configurations

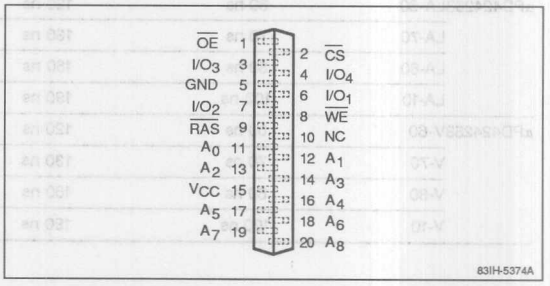
20-Pin Plastic DIP



26/20-Pin Plastic SOJ



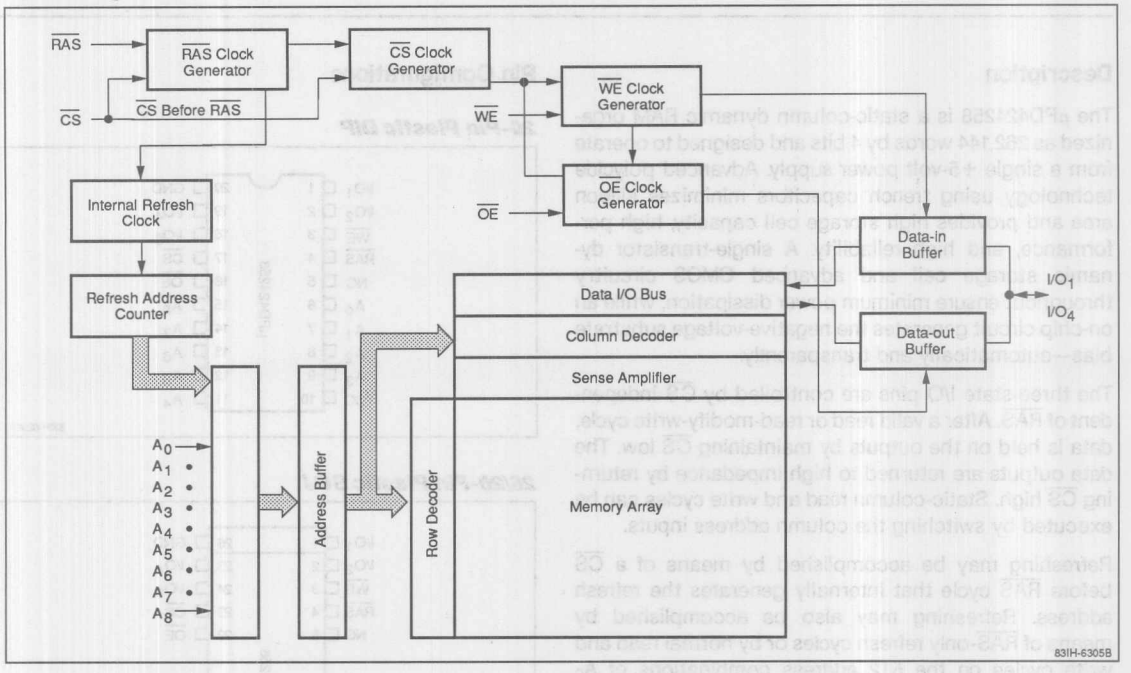
20-Pin Plastic ZIP



6

TSOP package will be available in 1991.

Block Diagram



Ordering Information

Part Number	RAS Access Time (max)	R/W Cycle Time (max)	Static-Column Access (max)	Package
μPD424258C-60	60 ns	120 ns	35 ns	20-pin plastic DIP
C-70	70 ns	130 ns	40 ns	
C-80	80 ns	160 ns	50 ns	
C-10	100 ns	190 ns	60 ns	
μPD424258LA-60	60 ns	120 ns	35 ns	26/20-pin plastic SOJ
LA-70	70 ns	130 ns	40 ns	
LA-80	80 ns	160 ns	50 ns	
LA-10	100 ns	190 ns	60 ns	
μPD424258V-60	60 ns	120 ns	35 ns	20-pin plastic ZIP
V-70	70 ns	130 ns	40 ns	
V-80	80 ns	160 ns	50 ns	
V-10	100 ns	190 ns	60 ns	

Pin Identification

Name	Function
A_0 - A_8	Address inputs
I/O_1 - I/O_4	Data inputs/outputs
$\overline{RAS}$	Row address strobe
$\overline{CS}$	Chip select
$\overline{WE}$	Write enable
$\overline{OE}$	Output enable
GND	Ground
V_{CC}	+5-volt power supply
NC	No connection

Absolute Maximum Ratings

Voltage on any pin relative to GND, V_T	−1.0 to +7.0 V
Operating temperature, T_{OPR}	0 to +70°C
Storage temperature, T_{STG}	−55 to +125°C
Short-circuit output current, I_{OS}	50 mA
Power dissipation, P_D	1.0 W

Exposure to Absolute Maximum Ratings for extended periods may affect device reliability; exceeding the ratings could cause permanent damage. The device should be operated within the limits specified under DC and AC Characteristics.

DC Characteristics

T_A = 0 to +70 °C; V_{CC} = +5.0 V ±10%

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions
Standby current	I_{CC2}			2.0	mA	$\overline{RAS}$ = $\overline{CS}$ = V_{IH}
				1.0	mA	$\overline{RAS}$ = $\overline{CS}$ ≥ V_{CC} − 0.2
Input leakage current	$I_{I(L)}$	−10		10	μA	V_{IN} = 0 V to V_{CC}; all other pins not under test = 0 V
Output leakage current	$I_{O(L)}$	−10		10	μA	D_{OUT} disabled; V_{OUT} = 0 V to V_{CC}
Output voltage, low	V_{OL}			0.4	V	I_{OL} = 4.2 mA
Output voltage, high	V_{OH}	2.4			V	I_{OH} = −5 mA

Capacitance

T_A = 25°C; f = 1 MHz

Parameter	Symbol	Max	Unit	Pins Under Test
Input capacitance	C_{I1}	5	pF	Address
	C_{I2}	7	pF	$\overline{RAS}$, $\overline{CS}$, $\overline{WE}$, $\overline{OE}$
Input/output capacitance	C_{IO}	7	pF	I/O_1 - I/O_4

Recommended Operating Conditions

Parameter	Symbol	Min	Typ	Max	Unit
Input voltage, high	V_{IH}	2.4		V_{CC} + 1.0	V
Input voltage, low	V_{IL}	−1.0		0.8	V
Supply voltage	V_{CC}	4.5	5.0	5.5	V
Ambient temperature	T_A	0		70	°C

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AC Characteristics

T_A = 0 to +70°C; V_{CC} = +5.0 V ±10%

		-60		-70		-80		-10			
Parameter	**Symbol**	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**	**Unit**	**Test Conditions**
Operating current, average	I_{CC1}		90		80		70		60	mA	$\overline{RAS}$, $\overline{CS}$ cycling; $t_{RC} = t_{RC}$ min (Note 5)
Operating current, $\overline{RAS}$-only refresh cycle, average	I_{CC3}		90		80		70		60	mA	$\overline{RAS}$ cycling; $\overline{CS} = V_{IH}$; $t_{RC} = t_{RC}$ min (Note 5)
Static-column operating current, average	I_{CC4}		80		70		60		50	mA	$\overline{RAS} = \overline{CS} = V_{IL}$; addresses cycling; $t_{RSC} = t_{RSC}$ min or $t_{WSC} = t_{WSC}$ min (Note 5)
Operating current, $\overline{CS}$ before $\overline{RAS}$ refresh cycle, average	I_{CC5}		90		80		70		60	mA	$\overline{RAS}$ cycling; $\overline{CS}$ before $\overline{RAS}$; $t_{RC} = t_{RC}$ min (Note 5)
Access time from column address	t_{AA}		30		35		45		50	ns	(Notes 7, 10)
Column address hold time referenced to $\overline{RAS}$ (rising edge)	t_{AH}	15		15		15		15		ns	
Column address hold time referenced to $\overline{RAS}$	t_{AR}	N/A		N/A		80		100		ns	(Note 18)
Column address setup time	t_{ASC}	0		0		0		0		ns	
Row address setup time	t_{ASR}	0		0		0		0		ns	
Column address to $\overline{WE}$ delay time	t_{AWD}	50		55		70		80		ns	(Note 17)
Column address hold time referenced to $\overline{RAS}$ (write cycle)	t_{AWR}	N/A		N/A		60		60		ns	
Access time from $\overline{CS}$ (falling edge)	t_{CAC}		20		20		20		25	ns	(Notes 7, 9, 10)
Column address hold time	t_{CAH}	15		17		20		20		ns	
$\overline{CS}$ hold time for $\overline{CS}$ before $\overline{RAS}$ refresh cycle	t_{CHR}	15		15		15		20		ns	
$\overline{CS}$ precharge time, static-column cycle	t_{CP}	10		10		10		10		ns	
$\overline{CS}$ to $\overline{RAS}$ precharge time	t_{CRP}	10		10		10		10		ns	(Note 13)
$\overline{CS}$ pulse width	t_{CS}	20	100,000	20	100,000	20	100,000	25	100,000	ns	
$\overline{CS}$ hold time	t_{CSH}	60		70		80		100		ns	
$\overline{CS}$ setup time for $\overline{CS}$ before $\overline{RAS}$ refresh cycle	t_{CSR}	10		10		10		10		ns	
$\overline{CS}$ to $\overline{WE}$ delay	t_{CWD}	40		40		45		55		ns	(Note 17)
Write command to $\overline{CS}$ lead time	t_{CWL}	15		15		20		20		ns	

AC Characteristics (cont)

Parameter	Symbol	-60 Min	-60 Max	-70 Min	-70 Max	-80 Min	-80 Max	-10 Min	-10 Max	Unit	Test Conditions
Data-in hold time	t_{DH}	15		15		20		20		ns	(Note 16)
Data-in hold time referenced to $\overline{RAS}$	t_{DHR}	N/A		N/A		60		70		ns	(Note 18)
Data-in setup time	t_{DS}	0		0		0		0		ns	(Note 16)
Access time from $\overline{OE}$	t_{OEA}		20		20		20		25	ns	(Note 7)
$\overline{OE}$ data delay time	t_{OED}	15		15		20		25		ns	
$\overline{OE}$ command hold time	t_{OEH}	0		0		0		0		ns	
$\overline{OE}$ to $\overline{RAS}$ inactive setup time	t_{OES}	0		0		0		0		ns	
Output turnoff delay from $\overline{OE}$	t_{OEZ}		15		15		20		25	ns	(Note 11)
Output buffer turnoff delay	t_{OFF}	0	15	0	15	0	20	0	25	ns	(Note 11)
Output hold time from address	t_{OH}	5		5		5		5		ns	
Output enable time from $\overline{WE}$	t_{OW}		25		25		25		30	ns	(Note 7)
Access time from previous $\overline{WE}$ (falling edge)	t_{PWA}		60		70		90		110	ns	(Notes 7, 19)
Column address hold time from previous $\overline{WE}$ (falling edge)	t_{PWH}	60		70		90		110		ns	
Access time from $\overline{RAS}$	t_{RAC}		60		70		80		100	ns	(Notes 7, 8)
$\overline{RAS}$ to column address delay time	t_{RAD}	15	30	15	35	17	35	17	50	ns	(Note 10)
Row address hold time	t_{RAH}	10		10		12		12		ns	
Column address lead time referenced to $\overline{RAS}$ (rising edge)	t_{RAL}	30		35		45		50		ns	
$\overline{RAS}$ pulse width	t_{RAS}	60	10,000	70	10,000	80	10,000	100	10,000	ns	
$\overline{RAS}$ pulse width, static-column cycle	t_{RASC}	60	100,000	70	100,000	80	100,000	100	100,000	ns	
Random read or write cycle time	t_{RC}	120		130		160		190		ns	(Note 6)
$\overline{RAS}$ to $\overline{CS}$ delay time	t_{RCD}	20	40	20	50	25	60	25	75	ns	(Note 12)
Read command hold time referenced to $\overline{CS}$	t_{RCH}	0		0		0		0		ns	(Note 14)
Read command setup time	t_{RCS}	0		0		0		0		ns	
Refresh period	t_{REF}		8		8		8		8	ms	Addresses A_0 - A_8
$\overline{RAS}$ precharge time	t_{RP}	50		50		70		80		ns	
$\overline{RAS}$ precharge $\overline{CS}$ hold time	t_{RPC}	10		10		0		0		ns	
Read command hold time referenced to $\overline{RAS}$	t_{RRH}	10		10		10		10		ns	(Note 14)
Static-column read cycle time	t_{RSC}	35		40		50		60		ns	(Note 6)

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AC Characteristics (cont)

Parameter	Symbol	-60 Min	-60 Max	-70 Min	-70 Max	-80 Min	-80 Max	-10 Min	-10 Max	Unit	Test Conditions
$\overline{RAS}$ hold time	t_{RSH}	20		20		20		25		ns	
$\overline{RAS}$ to second $\overline{WE}$ delay	t_{RSW}	75		85		95		115		ns	
Read-write cycle time	t_{RWC}	165		175		215		255		ns	(Note 6)
$\overline{RAS}$ to $\overline{WE}$ delay	t_{RWD}	80		90		105		130		ns	(Note 17)
Write command to $\overline{RAS}$ lead time	t_{RWL}	20		20		25		30		ns	
Static-column read-write cycle time	t_{RWSC}	85		95		120		145		ns	(Note 6)
Rise and fall transition time	t_T	3	50	3	50	3	50	3	50	ns	(Note 4)
Previous $\overline{WE}$ (falling edge) to column address delay time	t_{WAD}	20	30	22	35	20	45	25	55	ns	(Note 19)
Write command hold time	t_{WCH}	15		15		15		20		ns	
Write command hold time referenced to $\overline{RAS}$	t_{WCR}	N/A		N/A		55		70		ns	(Note 18)
Write command setup time	t_{WCS}	0		0		0		0		ns	(Note 17)
Write invalid time	t_{WI}	10		10		10		10		ns	
Write command pulse width	t_{WP}	15		15		15		20		ns	(Note 15)
Static-column write cycle time	t_{WSC}	35		40		50		60		ns	(Note 6)

Notes:

(1) All voltages are referenced to GND.

(2) An initial pause of 100 μs is required after power-up, followed by any eight $\overline{RAS}$ cycles, before proper device operation is achieved.

(3) AC measurements assume t_T = 5 ns.

(4) V_{IH} (min) and V_{IL} (max) are reference levels for measuring the timing of input signals. Transition times are measured between V_{IH} and V_{IL}.

(5) I_{CC1}, I_{CC3}, I_{CC4}, and I_{CC5} depend on output loading and cycle rates. Specified values are obtained with the output open. I_{CC3} is measured assuming that all column address inputs are held at either a high level or a low level during $\overline{RAS}$-only refresh cycles. I_{CC4} is measured assuming that all column address inputs are switched only once during each fast-page cycle.

(6) The minimum specifications are used only to indicate the cycle time at which proper operation over the full temperature range (T_A = 0 to +70°C) is assured.

(7) Load = 2 TTL (–1 mA, +4 mA) loads and 100 pF (V_{OH} = 2.0 V, V_{OL} = 0.8 V).

(8) Assumes that $t_{RCD} \leq t_{RCD}$ (max) and $t_{RAD} \leq t_{RAD}$ (max). If t_{RCD} or t_{RAD} is greater than the maximum recommended value in this table, t_{RAC} increases by the amount that t_{RCD} or t_{RAD} exceeds the value shown.

(9) Assumes that $t_{RCD} \geq t_{RCD}$ (max) and $t_{RAD} \leq t_{RAD}$ (max).

(10) If $t_{RAD} \geq t_{RAD}$ (max), then the access time is defined by t_{AA}.

(11) t_{OFF} (max) defines the time at which the output achieves the open-circuit condition and is not referenced to V_{OH} or V_{OL}.

(12) Operation within the t_{RCD} (max) limit assures that t_{RAC} (max) can be met. t_{RCD} (max) is specified as a reference point only; if t_{RCD} is greater than t_{RCD} (max), then access time is controlled exclusively by t_{CAC}, t_{AA} or t_{OEA}.

(13) The t_{CRP} requirement should be applicable for $\overline{RAS}$/$\overline{CS}$ cycles preceded by any cycle.

(14) Either t_{RRH} or t_{RCH} must be satisfied for a read cycle.

(15) Parameter t_{WP} is applicable for a delayed write cycle such as a read-write/read-modify-write cycle. For early write operation, both t_{WCS} and t_{WCH} must be met.

(16) These parameters are referenced to the falling edge of $\overline{CS}$ for early write cycles and to the falling edge of $\overline{WE}$ for delayed write or read-modify-write cycles.

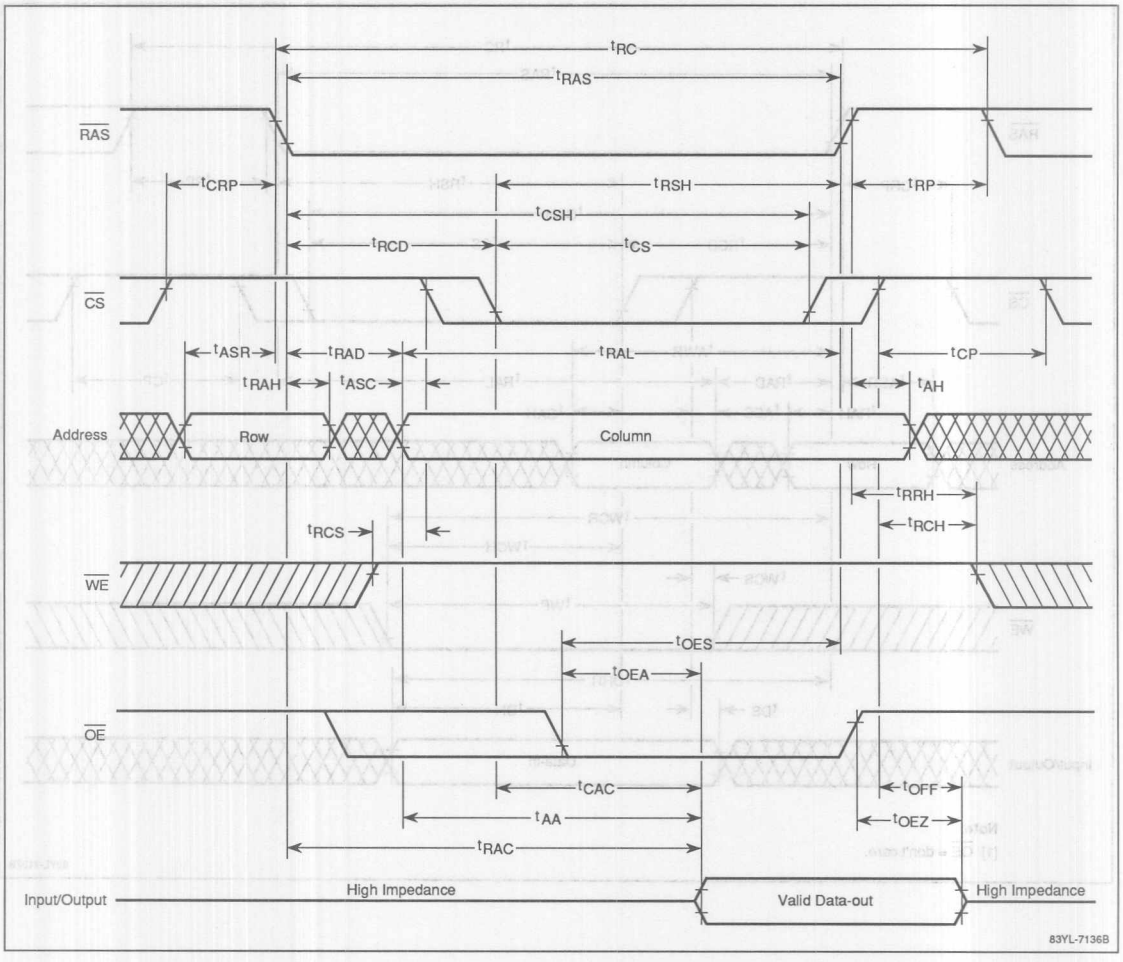
(17) t_{WCS}, t_{RWD}, t_{CWD}, and t_{AWD} are restrictive operating parameters in read-write/read-modify-write cycles only. If $t_{WCS} \geq t_{WCS}$ (min), the cycle is an early write cycle and the data output will remain open-circuit throughout the entire cycle. If $t_{CWD} \geq t_{CWD}$ (min), $t_{RWD} \geq t_{RWD}$ (min), and $t_{AWD} \geq t_{AWD}$ (min), the cycle is a read-write cycle and the data output will contain data read from the selected cell. If neither of the above conditions is met, the condition of the data output pin (at access time and until $\overline{CS}$ returns to V_{IH}) is indeterminate.

(18) This parameter is not needed for the μPD421000-60 and μPD421000-70.

(19) If $t_{WAD} \leq t_{WAD}$ (max), then access time is defined by t_{PWA}.

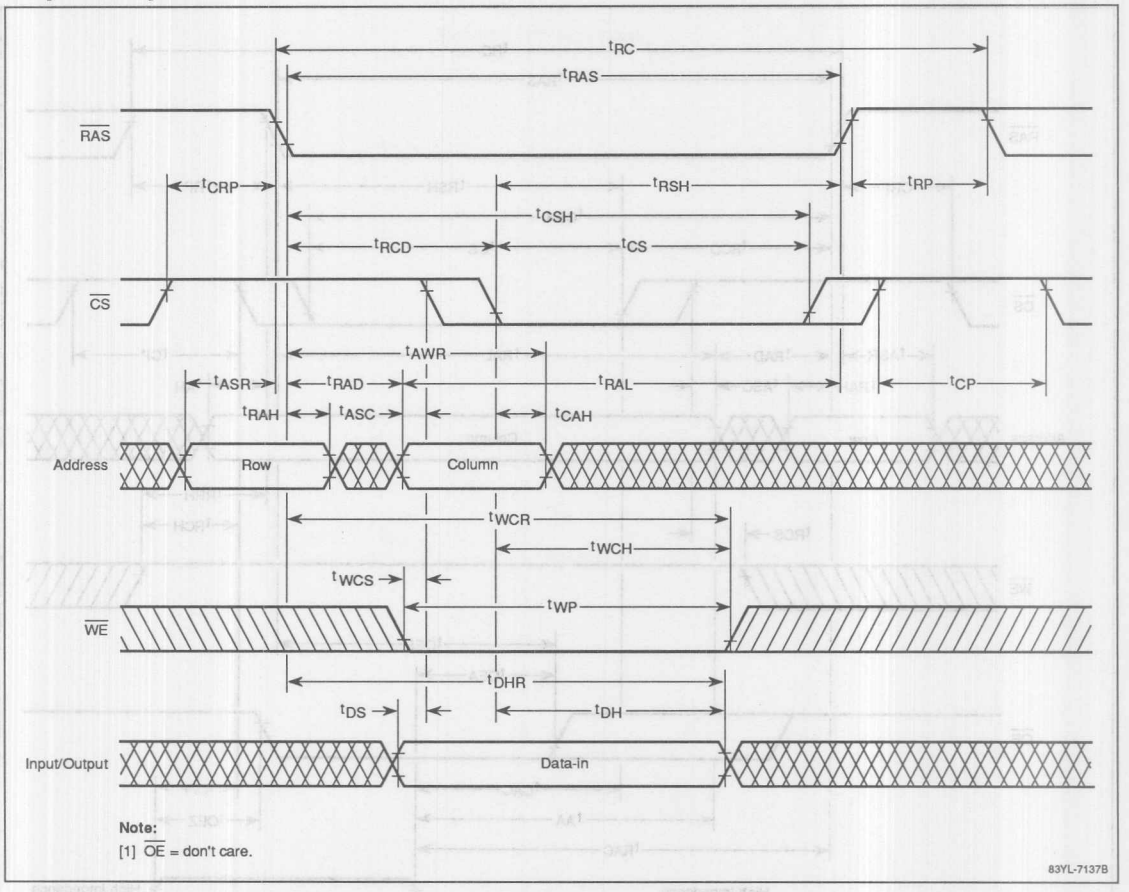
Timing Waveforms

Read Cycle



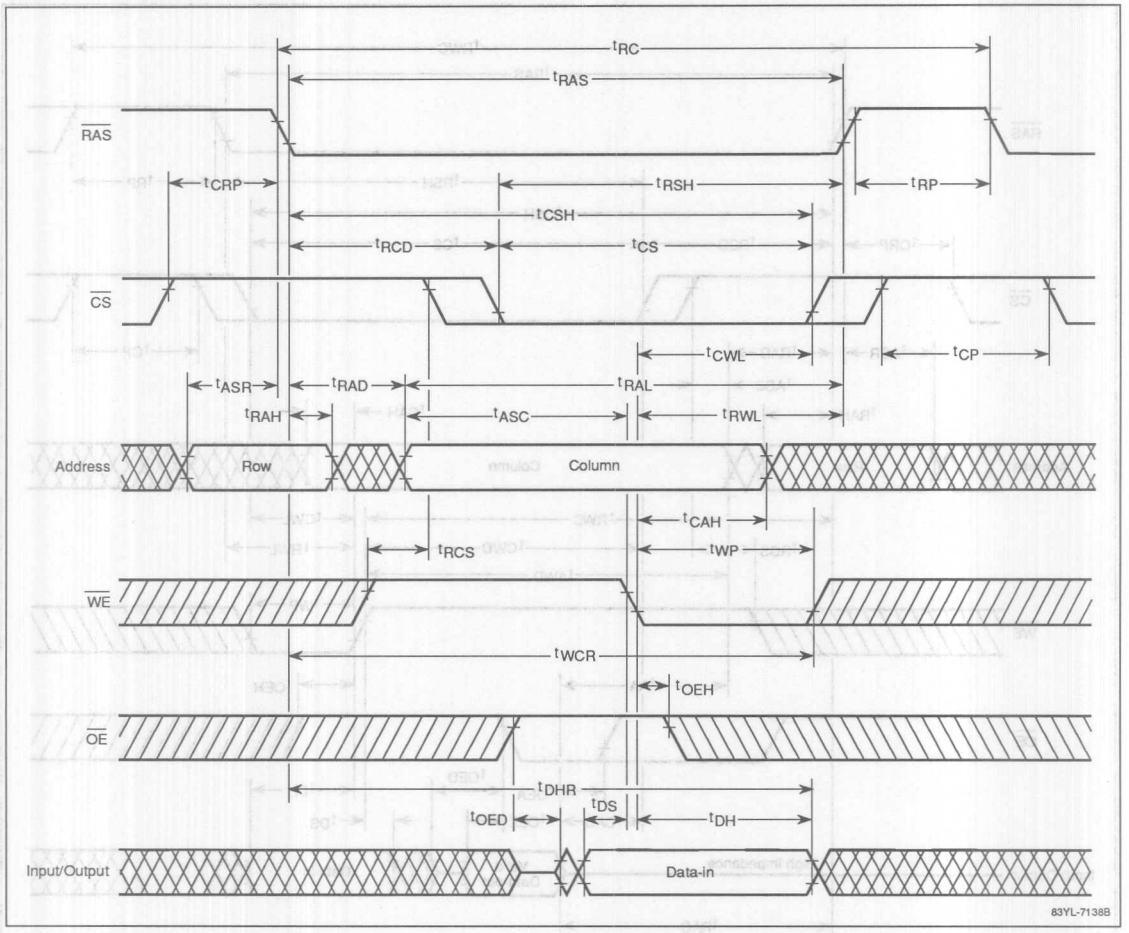
Timing Waveforms (cont)

Early Write Cycle



Timing Waveforms (cont)

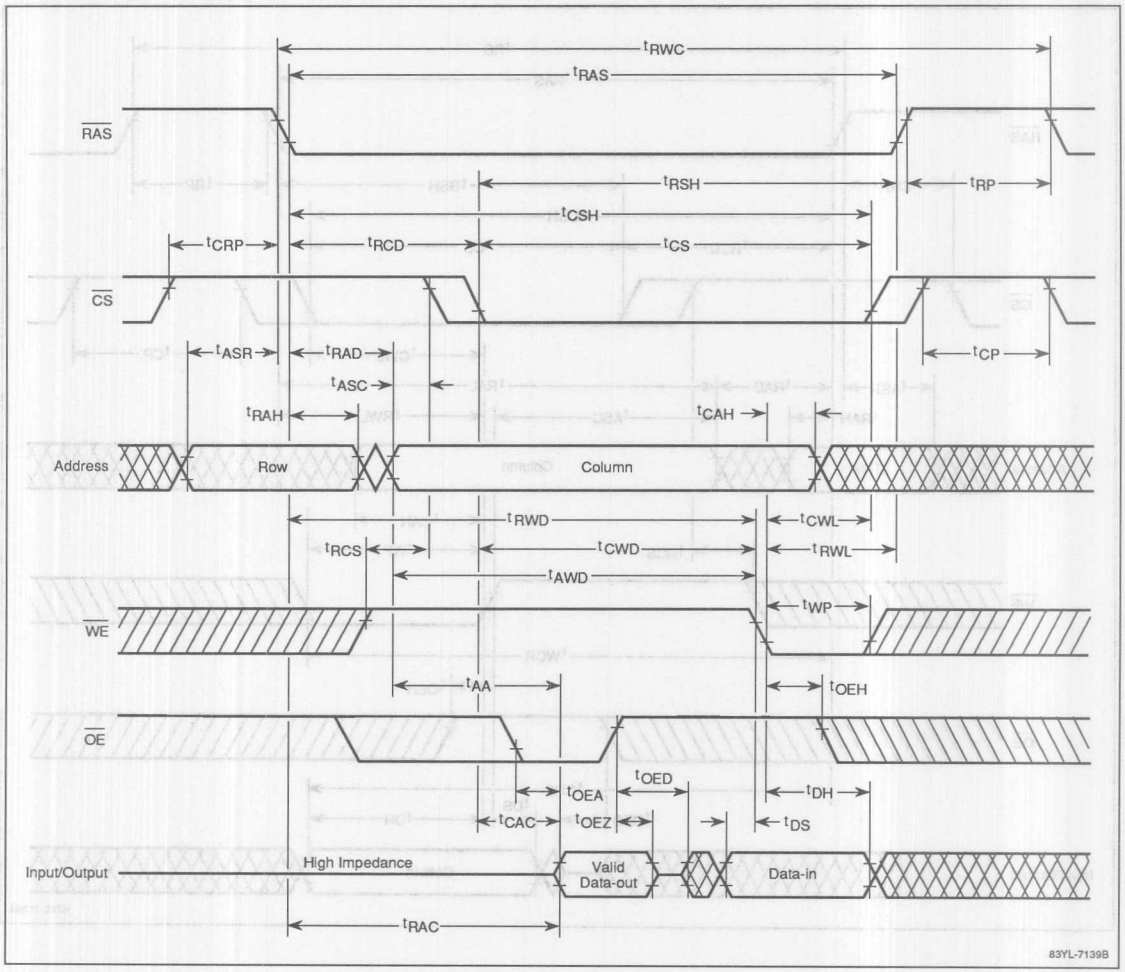
Late Write Cycle



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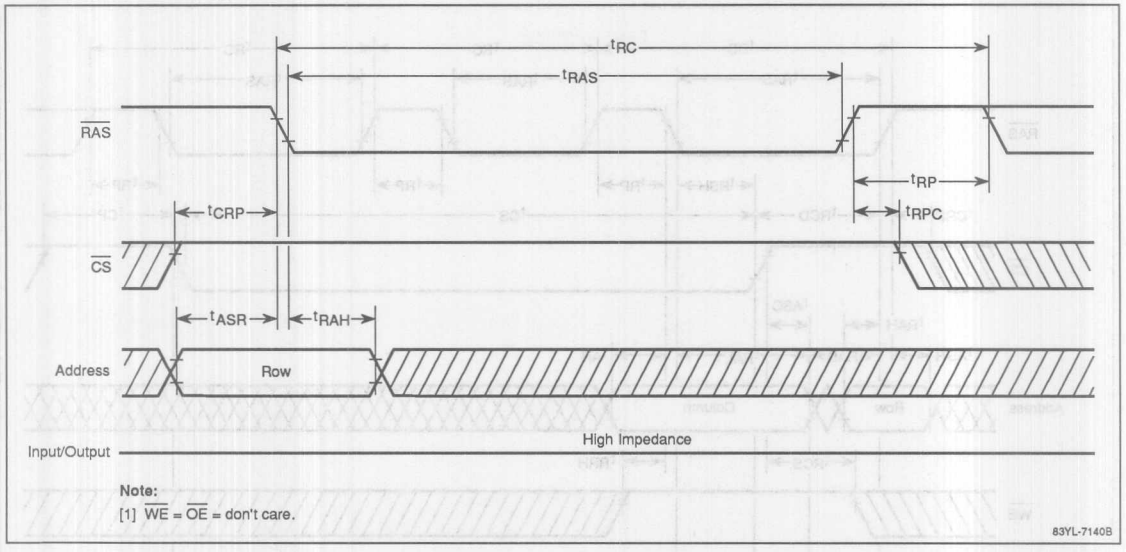
Timing Waveforms (cont)

Read-Modify-Write Cycle



Timing Waveforms (cont)

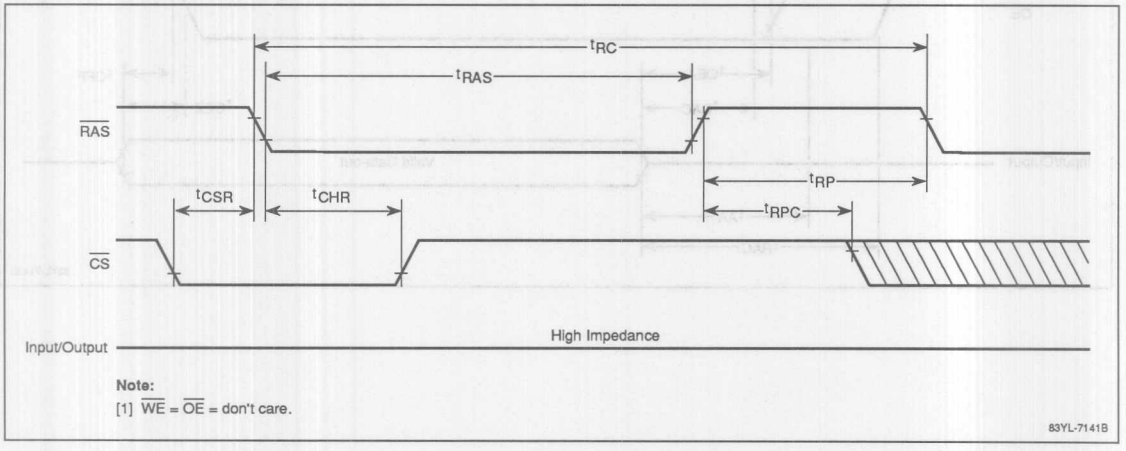
$\overline{\text{RAS}}$-Only Refresh Cycle



Note:
[1] $\overline{\text{WE}}$ = $\overline{\text{OE}}$ = don't care.

83YL-7140B

$\overline{\text{CS}}$ Before $\overline{\text{RAS}}$ Refresh Cycle



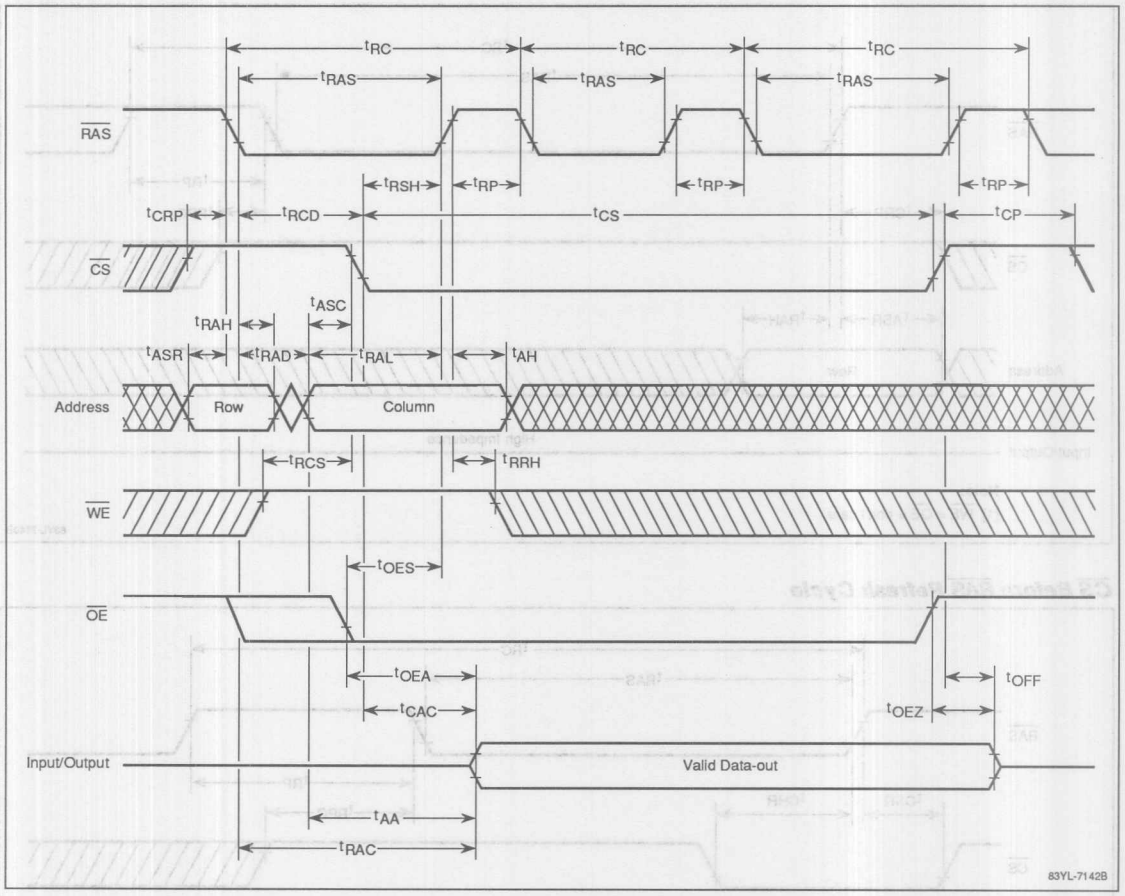
Note:
[1] $\overline{\text{WE}}$ = $\overline{\text{OE}}$ = don't care.

83YL-7141B

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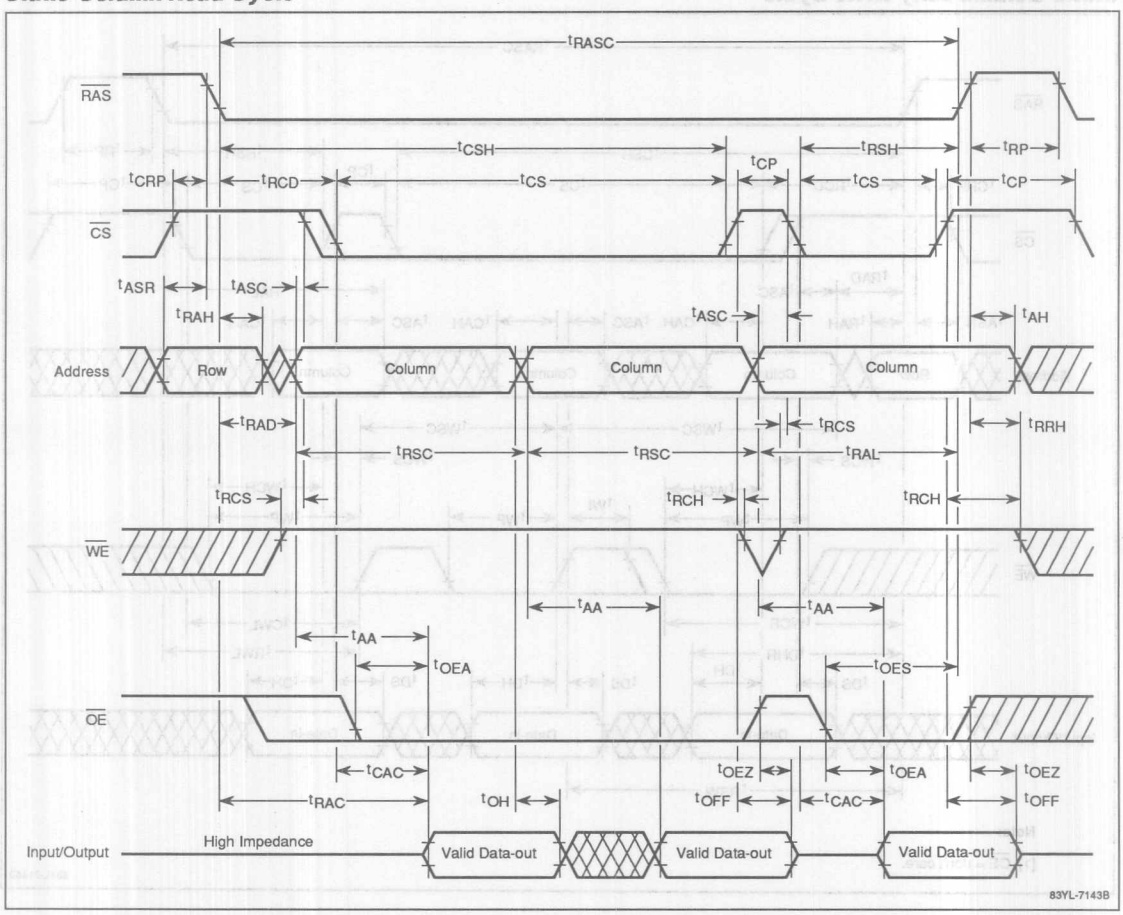
Timing Waveforms (cont)

Hidden Refresh Cycle



Timing Waveforms (cont)

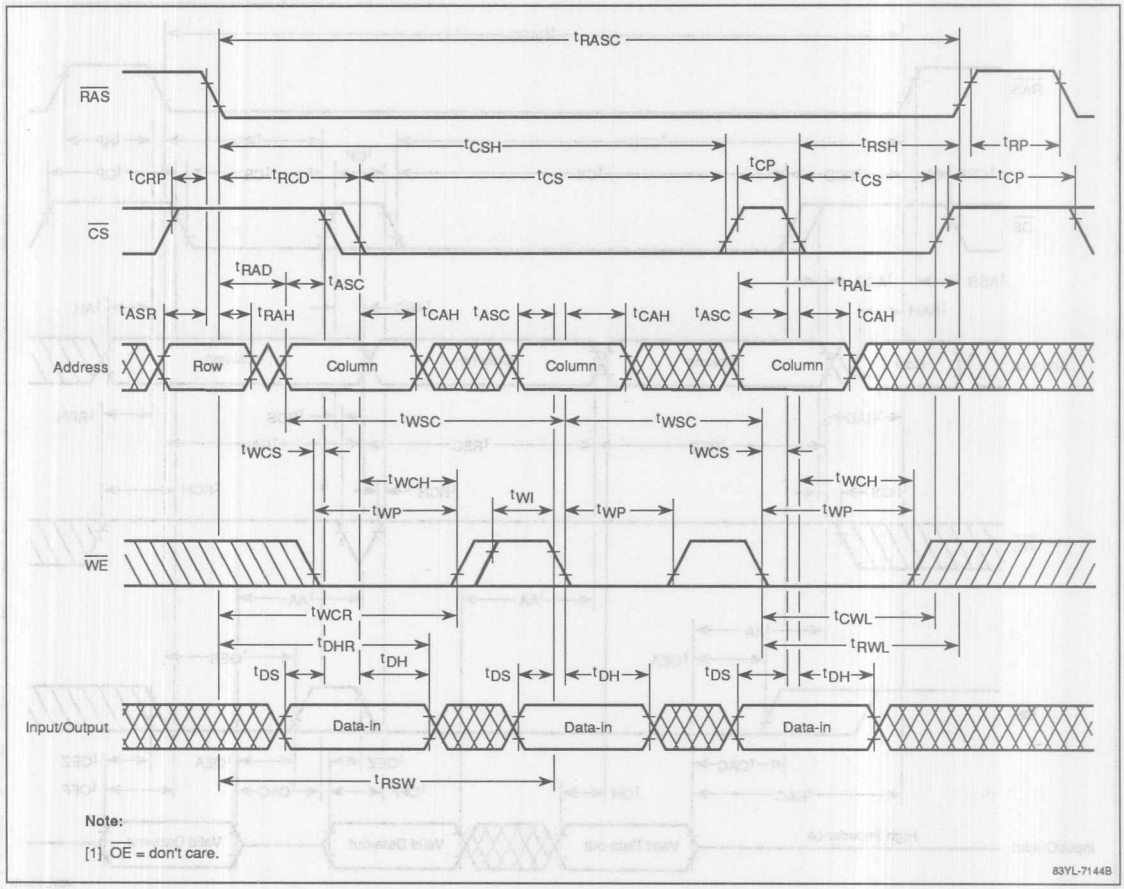
Static-Column Read Cycle



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Timing Waveforms (cont)

Static-Column Early Write Cycle



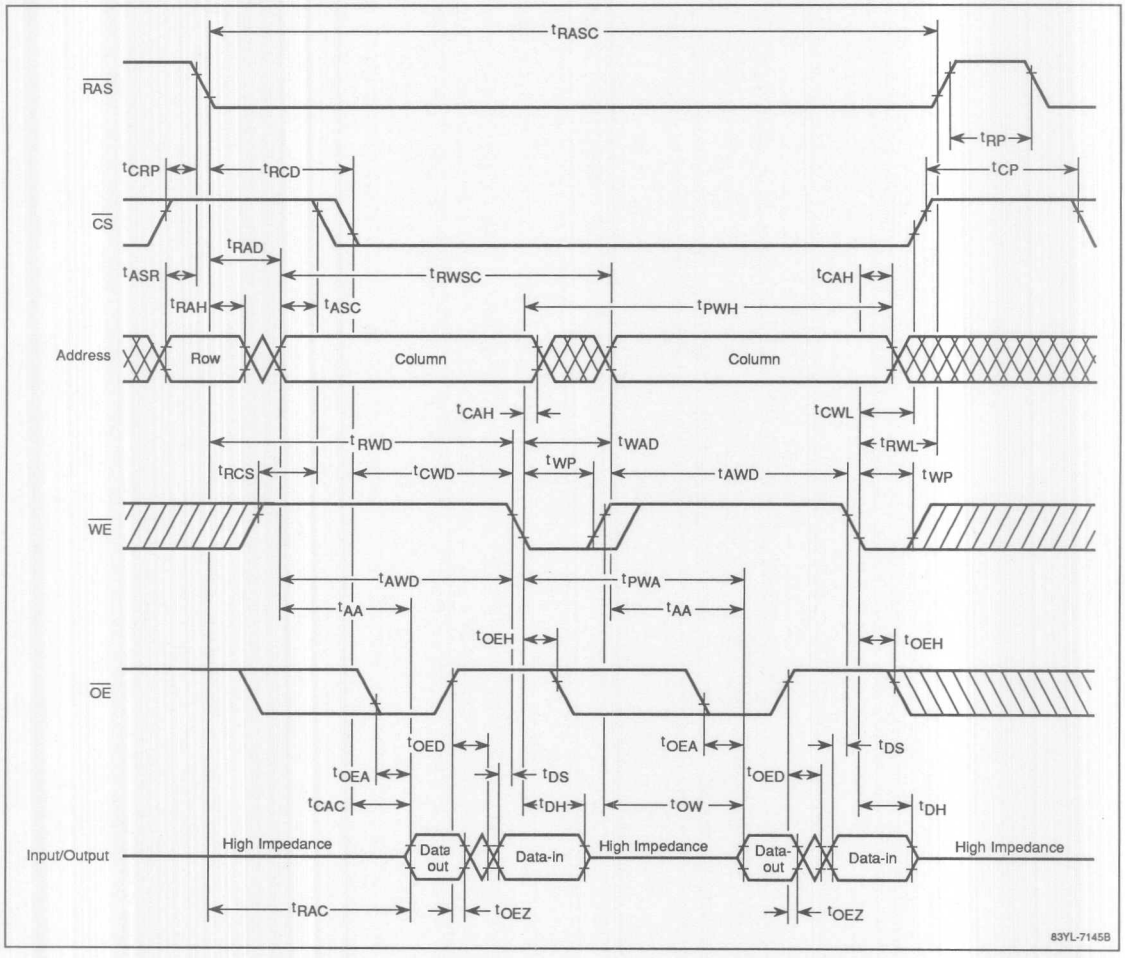
Note:

[1] $\overline{OE}$ = don't care.

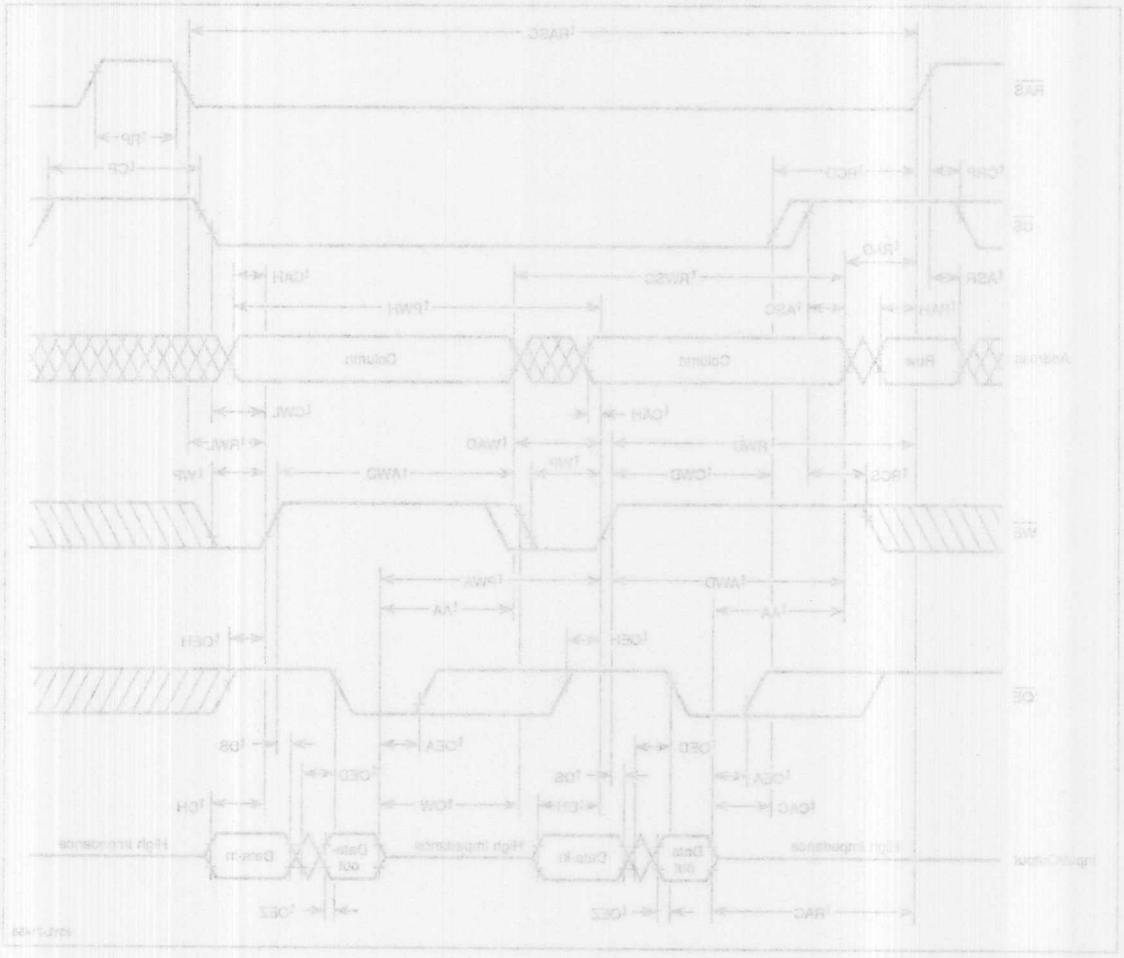
83YL-7144B

Timing Waveforms (cont)

Static-Column Read-Modify-Write Cycle



6



μPD424266
262,144 x 4-Bit
Dynamic CMOS RAM

Description

The μPD424266 is a 262,144 by 4-bit dynamic RAM designed with a write-per-bit option and to operate from a single + 5-volt power supply. Advanced polycide technology using trench capacitors minimizes silicon area and provides high storage cell capacity, high performance, and high reliability. A single-transistor dynamic storage cell and CMOS circuitry throughout ensure minimum power dissipation, while an on-chip circuit internally generates the negative-voltage substrate bias—automatically and transparently.

The three-state I/O pins are controlled by $\overline{CAS}$ independent of $\overline{RAS}$. After a valid read or read-modify-write cycle, data is held on the outputs by maintaining $\overline{CAS}$ low. Data outputs return to high impedance when $\overline{CAS}$ goes high. Fast-page read and write cycles can be executed by cycling $\overline{CAS}$.

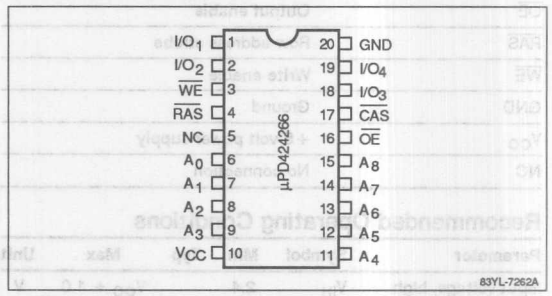
Refreshing may be accomplished by means of a $\overline{CAS}$ before $\overline{RAS}$ cycle that internally generates the refresh address. Refreshing may also be accomplished by means of $\overline{RAS}$-only refresh cycles or by normal read or write cycles on the 512 address combinations of A_0 through A_8 during an 8-ms refresh period.

Features

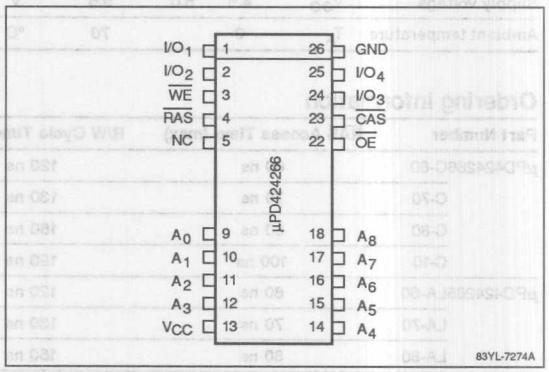
- 262,144 by 4-bit organization
- Single + 5-volt power supply
- Write-per-bit option
- Fast-page option
- Low power dissipation
- $\overline{CAS}$ before $\overline{RAS}$ internal refreshing
- Multiplexed address inputs
- On-chip substrate bias generator
- TTL-compatible inputs and outputs
- Nonlatched, three-state outputs
- Low input capacitance
- 512 refresh cycles every 8 ms
- High-density 20-pin plastic DIP, 26/20-pin plastic SOJ, or 20-pin plastic ZIP packaging

Pin Configurations

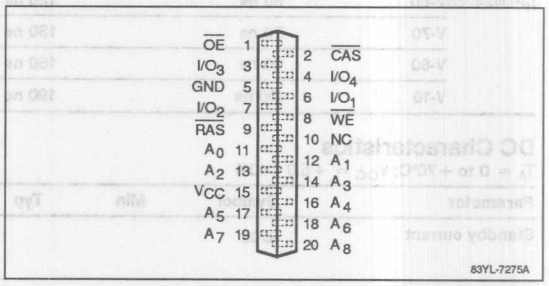
20-Pin Plastic DIP



26/20-Pin Plastic SOJ



20-Pin Plastic ZIP



6

TSOP package will be available in 1991.

Pin Identification

Name	Function
A_0 - A_8	Address inputs
I/O_1 - I/O_4	Data inputs and outputs
$\overline{CAS}$	Column address strobe
$\overline{OE}$	Output enable
$\overline{RAS}$	Row address strobe
$\overline{WE}$	Write enable
GND	Ground
V_{CC}	+5-volt power supply
NC	No connection

Recommended Operating Conditions

Parameter	Symbol	Min	Typ	Max	Unit
Input voltage, high	V_{IH}	2.4		V_{CC} + 1.0	V
Input voltage, low	V_{IL}	−1.0		0.8	V
Supply voltage	V_{CC}	4.5	5.0	5.5	V
Ambient temperature	T_A	0		70	°C

Capacitance

T_A = 25°C; f = 1 MHz

Parameter	Symbol	Max	Unit	Pins Under Test
Input capacitance	C_{I1}	5	pF	Addresses
	C_{I2}	7	pF	$\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$, $\overline{OE}$
Input/output capacitance	C_{IO}	7	pF	I/O_1 – I/O_4

Absolute Maximum Ratings

Voltage on any pin relative to GND, V_T	−1.0 to +7.0 V
Operating temperature, T_{OPR}	0 to +70°C
Storage temperature, T_{STG}	−55 to +125°C
Short-circuit output current, I_{OS}	50 mA
Power dissipation, P_D	1.0 W

Exposure to Absolute Maximum Ratings for extended periods may affect device reliability; exceeding the ratings could cause permanent damage. The device should be operated within the limits specified under DC and AC Characteristics.

Ordering Information

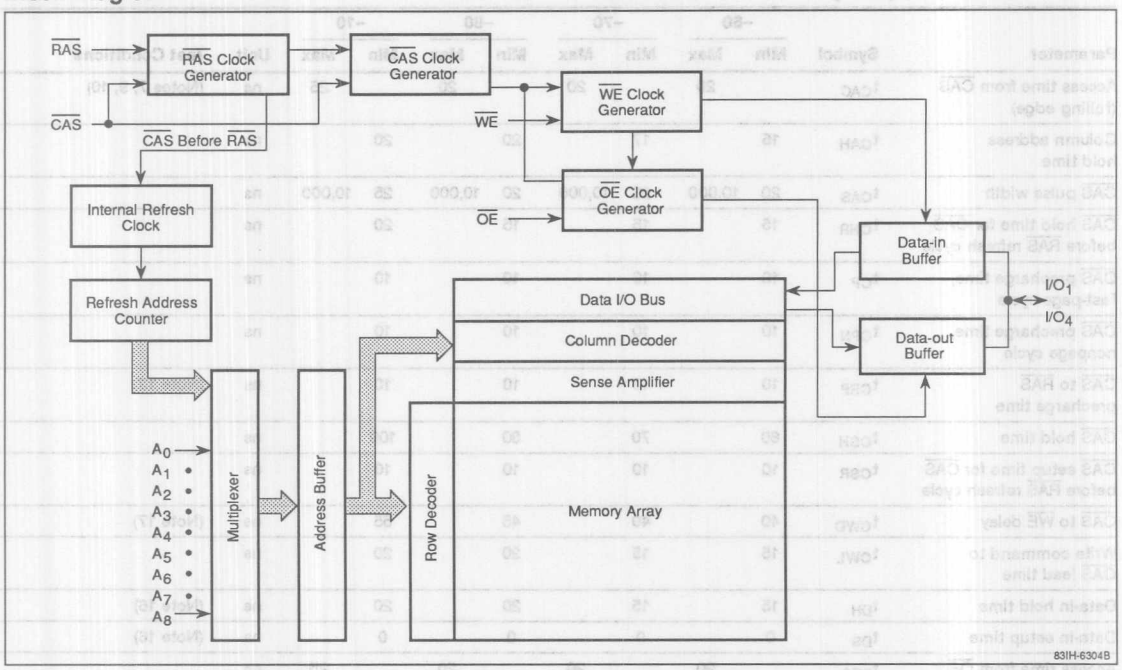
Part Number	$\overline{RAS}$ Access Time (max)	R/W Cycle Time (max)	Fast-Page Cycle (max)	Package
μPD424266C-60	60 ns	120 ns	40 ns	20-pin plastic DIP
C-70	70 ns	130 ns	45 ns	
C-80	80 ns	160 ns	50 ns	
C-10	100 ns	190 ns	60 ns	
μPD424266LA-60	60 ns	120 ns	40 ns	26/20-pin plastic SOJ
LA-70	70 ns	130 ns	45 ns	
LA-80	80 ns	160 ns	50 ns	
LA-10	100 ns	190 ns	60 ns	
μPD424266V-60	60 ns	120 ns	40 ns	20-pin plastic ZIP
V-70	70 ns	130 ns	45 ns	
V-80	80 ns	160 ns	50 ns	
V-10	100 ns	190 ns	60 ns	

DC Characteristics

T_A = 0 to +70°C; V_{CC} = +5.0 ±10%

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions
Standby current	I_{CC2}			2.0	mA	$\overline{RAS} \geq V_{IH}$ (min); I_O = 0 mA
				1.0	mA	$\overline{RAS}$ = $\overline{CAS} \geq V_{CC}$ − 0.2 V; I_O = 0 mA
Input leakage current	$I_{I(L)}$	−10		10	μA	V_{IN} = 0 V to V_{CC}; all other pins not under test = 0 V
Output leakage current	$I_{O(L)}$	−10		10	μA	D_{OUT} disabled; V_{OUT} = 0 V to V_{CC}
Output voltage, low	V_{OL}			0.4	V	I_{OL} = 4.2 mA
Output voltage, high	V_{OH}	2.4			V	I_{OH} = −5 mA

Block Diagram



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AC Characteristics

T_A = 0 to +70°C; V_{CC} = +5.0 V ±10%

		-60		-70		-80		-10			
Parameter	Symbol	Min	Max	Min	Max	Min	Max	Min	Max	Unit	Test Conditions
Operating current, average	I_{CC1}		90		80		70		60	mA	$\overline{RAS}$, $\overline{CAS}$ cycling; t_{RC} = t_{RC} min (Note 5)
Operating current, $\overline{RAS}$-only refresh cycle, average	I_{CC3}		90		80		70		60	mA	$\overline{RAS}$ cycling; $\overline{CAS}$ = V_{IH}; t_{RC} = t_{RC} min (Note 5)
Operating current, fast-page cycle, average	I_{CC4}		80		70		60		50	mA	$\overline{RAS}$ = V_{IL}; $\overline{CAS}$ cycling; t_{PC} = t_{PC} min (Note 5)
Operating current, $\overline{CAS}$ before $\overline{RAS}$ refresh cycle, average	I_{CC5}		90		80		70		60	mA	$\overline{RAS}$ cycling; $\overline{CAS}$ before $\overline{RAS}$; t_{RC} = t_{RC} min (Note 5)
Access time from column address	t_{AA}		30		35		40		50	ns	(Notes 7, 10)
Access time from $\overline{CAS}$ precharge (rising edge)	t_{ACP}		35		40		45		55	ns	(Notes 7)
Column address setup time	t_{ASC}	0		0		0		0		ns	
Row address setup time	t_{ASR}	0		0		0		0		ns	
Column address to $\overline{WE}$ delay time	t_{AWD}	50		55		65		80		ns	(Note 17)

AC Characteristics (cont)

Parameter	Symbol	-60 Min	-60 Max	-70 Min	-70 Max	-80 Min	-80 Max	-10 Min	-10 Max	Unit	Test Conditions
Access time from $\overline{CAS}$ (falling edge)	t_{CAC}		20		20		20		25	ns	(Notes 7, 9, 10)
Column address hold time	t_{CAH}	15		17		20		20		ns	
$\overline{CAS}$ pulse width	t_{CAS}	20	10,000	20	10,000	20	10,000	25	10,000	ns	
$\overline{CAS}$ hold time for $\overline{CAS}$ before $\overline{RAS}$ refresh cycle	t_{CHR}	15		15		15		20		ns	
$\overline{CAS}$ precharge time, fast-page cycle	t_{CP}	10		10		10		10		ns	
$\overline{CAS}$ precharge time, nonpage cycle	t_{CPN}	10		10		10		10		ns	
$\overline{CAS}$ to $\overline{RAS}$ precharge time	t_{CRP}	10		10		10		10		ns	(Note 13)
$\overline{CAS}$ hold time	t_{CSH}	60		70		80		100		ns	
$\overline{CAS}$ setup time for $\overline{CAS}$ before $\overline{RAS}$ refresh cycle	t_{CSR}	10		10		10		10		ns	
$\overline{CAS}$ to $\overline{WE}$ delay	t_{CWD}	40		40		45		55		ns	(Note 17)
Write command to $\overline{CAS}$ lead time	t_{CWL}	15		15		20		20		ns	
Data-in hold time	t_{DH}	15		15		20		20		ns	(Note 16)
Data-in setup time	t_{DS}	0		0		0		0		ns	(Note 16)
Access time from $\overline{OE}$	t_{OEA}		20		20		20		25	ns	
$\overline{OE}$ data delay time	t_{OED}	15		15		20		25		ns	
$\overline{OE}$ command hold time	t_{OEH}	0		0		0		0		ns	
$\overline{OE}$ to $\overline{RAS}$ inactive setup time	t_{OES}	0		0		0		0		ns	
Output turnoff delay from $\overline{OE}$	t_{OEZ}	0	15	0	15	0	20	0	25	ns	(Note 11)
Output buffer turnoff delay	t_{OFF}	0	15	0	15	0	20	0	25	ns	(Note 11)
Fast-page cycle time	t_{PC}	40		45		50		60		ns	(Note 6)
Fast-page read-modify-write cycle time	t_{PRWC}	85		90		105		125		ns	(Note 6)
Access time from $\overline{RAS}$	t_{RAC}		60		70		80		100	ns	(Notes 7, 8)

AC Characteristics (cont)

Parameter	Symbol	-60 Min	-60 Max	-70 Min	-70 Max	-80 Min	-80 Max	-10 Min	-10 Max	Unit	Test Conditions
$\overline{RAS}$ to column address delay time	t_{RAD}	15	30	15	35	17	40	17	50	ns	(Note 10)
Row address hold time	t_{RAH}	10		10		12		12		ns	
Column address lead time referenced to $\overline{RAS}$ (rising edge)	t_{RAL}	30		35		40		50		ns	
$\overline{RAS}$ pulse width	t_{RAS}	60	10,000	70	10,000	80	10,000	100	10,000	ns	
$\overline{RAS}$ pulse width, fast-page cycle	t_{RASP}	60	100,000	70	100,000	80	100,000	100	100,000	ns	
Random read or write cycle time	t_{RC}	120		130		160		190		ns	(Note 6)
$\overline{RAS}$ to $\overline{CAS}$ delay time	t_{RCD}	20	40	20	50	25	60	25	75	ns	(Note 12)
Read command hold time referenced to $\overline{CAS}$	t_{RCH}	0		0		0		0		ns	(Note 14)
Read command setup time	t_{RCS}	0		0		0		0		ns	
Refresh period	t_{REF}		8		8		8		8	ms	Addresses A_0 - A_8
$\overline{RAS}$ precharge time	t_{RP}	50		50		70		80		ns	
$\overline{RAS}$ precharge $\overline{CAS}$ hold time	t_{RPC}	10		10		0		0		ns	
Read command hold time referenced to $\overline{RAS}$	t_{RRH}	10		10		10		10		ns	(Note 14)
$\overline{RAS}$ hold time	t_{RSH}	20		20		20		25		ns	
Read-write cycle time	t_{RWC}	165		175		215		255		ns	(Note 6)
$\overline{RAS}$ to $\overline{WE}$ delay	t_{RWD}	80		90		105		130		ns	(Note 17)
Write command to $\overline{RAS}$ lead time	t_{RWL}	20		20		25		30		ns	
Rise and fall transition time	t_T	3	50	3	50	3	50	3	50	ns	(Note 4)
Write-per-bit hold time	t_{WBH}	10		10		10		10		ns	
Write-per-bit setup time	t_{WBS}	0		0		0		0		ns	
Write command hold time	t_{WCH}	15		15		15		20		ns	(Note 15)
Write command setup time	t_{WCS}	0		0		0		0		ns	(Note 16)

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AC Characteristics (cont)

Parameter	Symbol	-60 Min	-60 Max	-70 Min	-70 Max	-80 Min	-80 Max	-10 Min	-10 Max	Unit	Test Conditions
Write-per-bit mask data hold time	t_{WH}	10		10		10		10		ns	
Write command pulse width	t_{WP}	15		15		15		20		ns	(Note 15)
Write-per-bit mask data setup time	t_{WS}	0		0		0		0		ns	

Notes:

(1) All voltages are referenced to GND.

(2) An initial pause of 100 μs is required after power-up, followed by any eight $\overline{RAS}$ cycles, before proper device operation is achieved.

(3) AC measurements assume $t_T = 5$ ns.

(4) V_{IH} (min) and V_{IL} (max) are reference levels for measuring the timing of input signals. Transition times are measured between V_{IH} and V_{IL}.

(5) I_{CC1}, I_{CC3}, I_{CC4}, and I_{CC5} depend on output loading and cycle rates. Specified values are obtained with the output open. I_{CC3} is measured assuming that all column address inputs are held at either a high level or a low level during $\overline{RAS}$-only refresh cycles. I_{CC4} is measured assuming that all column address inputs are switched only once during each fast-page cycle.

(6) The minimum specifications are used only to indicate the cycle time at which proper operation over the full temperature range (T_A = 0 to +70°C) is assured.

(7) Load = 2 TTL (–1 mA, +4 mA) loads and 100 pF (V_{OH} = 2.0 V, V_{OL} = 0.8 V).

(8) Assumes that $t_{RCD} \leq t_{RCD}$ (max) and $t_{RAD} \leq t_{RAD}$ (max). If t_{RCD} or t_{RAD} is greater than the maximum recommended value in this table, t_{RAC} increases by the amount that t_{RCD} or t_{RAD} exceeds the value shown.

(9) Assumes that $t_{RCD} \geq t_{RCD}$ (max) and $t_{RAD} \leq t_{RAD}$ (max).

(10) If $t_{RAD} \geq t_{RAD}$ (max), then the access time is defined by t_{AA}.

(11) t_{OFF} (max) defines the time at which the output achieves the open-circuit condition and is not referenced to V_{OH} or V_{OL}.

(12) Operation within the t_{RCD} (max) limit assures that t_{RAC} (max) can be met. t_{RCD} (max) is specified as a reference point only; if t_{RCD} is greater than t_{RCD} (max), then access time is controlled exclusively by t_{CAC}.

(13) The t_{CRP} requirement should be applicable for $\overline{RAS}$/$\overline{CAS}$ cycles preceded by any cycle.

(14) Either t_{RRH} or t_{RCH} must be satisfied for a read cycle.

(15) Parameter t_{WP} is applicable for a delayed write cycle such as a read-write/read-modify-write cycle. For early write operation, both t_{WCS} and t_{WCH} must be met.

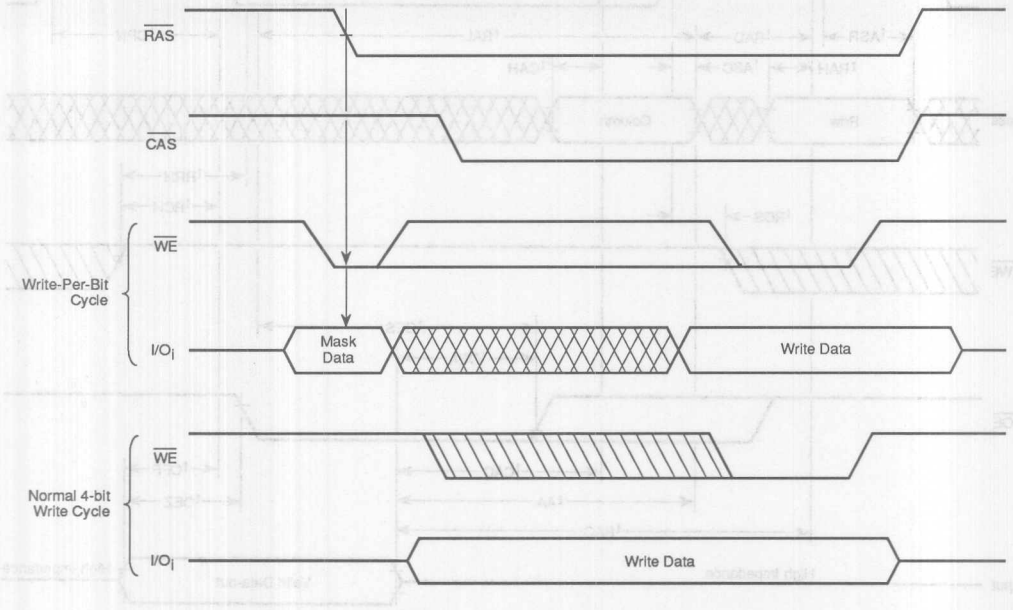
(16) These parameters are referenced to the falling edge of $\overline{CAS}$ for early write cycles and to the falling edge of $\overline{WE}$ for delayed write or read-modify-write cycles.

(17) t_{WCS}, t_{RWD}, t_{CWD}, and t_{AWD} are restrictive operating parameters in read-write/read-modify-write cycles only. If $t_{WCS} \geq t_{WCS}$ (min), the cycle is an early write cycle and the data output will remain open-circuit throughout the entire cycle. If $t_{CWD} \geq t_{CWD}$ (min), $t_{RWD} \geq t_{RWD}$ (min), and $t_{AWD} \geq t_{AWD}$ (min), the cycle is a read-write cycle and the data output will contain data read from the selected cell. If neither of the above conditions is met, the condition of the data output pin (at access time and until $\overline{CAS}$ returns to V_{IH}) is indeterminate.

Write-Per-Bit Option

The write-per-bit option may be used to allow a write cycle to change any number of bits in the 4-bit word. The mask is loaded from the four I/O lines at the falling edge of $\overline{RAS}$ if $\overline{WE} = V_{IL}$. If the I/O line is high, then the corresponding bit will be written when the write cycle executes. If an I/O line is low, the corresponding bit does not change. A mask loaded during fast-page operation will remain set and active for each write cycle that executes while $\overline{RAS}$ remains low. The mask may be changed at the falling edge of $\overline{RAS}$ only.

Comparison of Write-Per-Bit Cycle Versus Standard 4-Bit Write Cycle



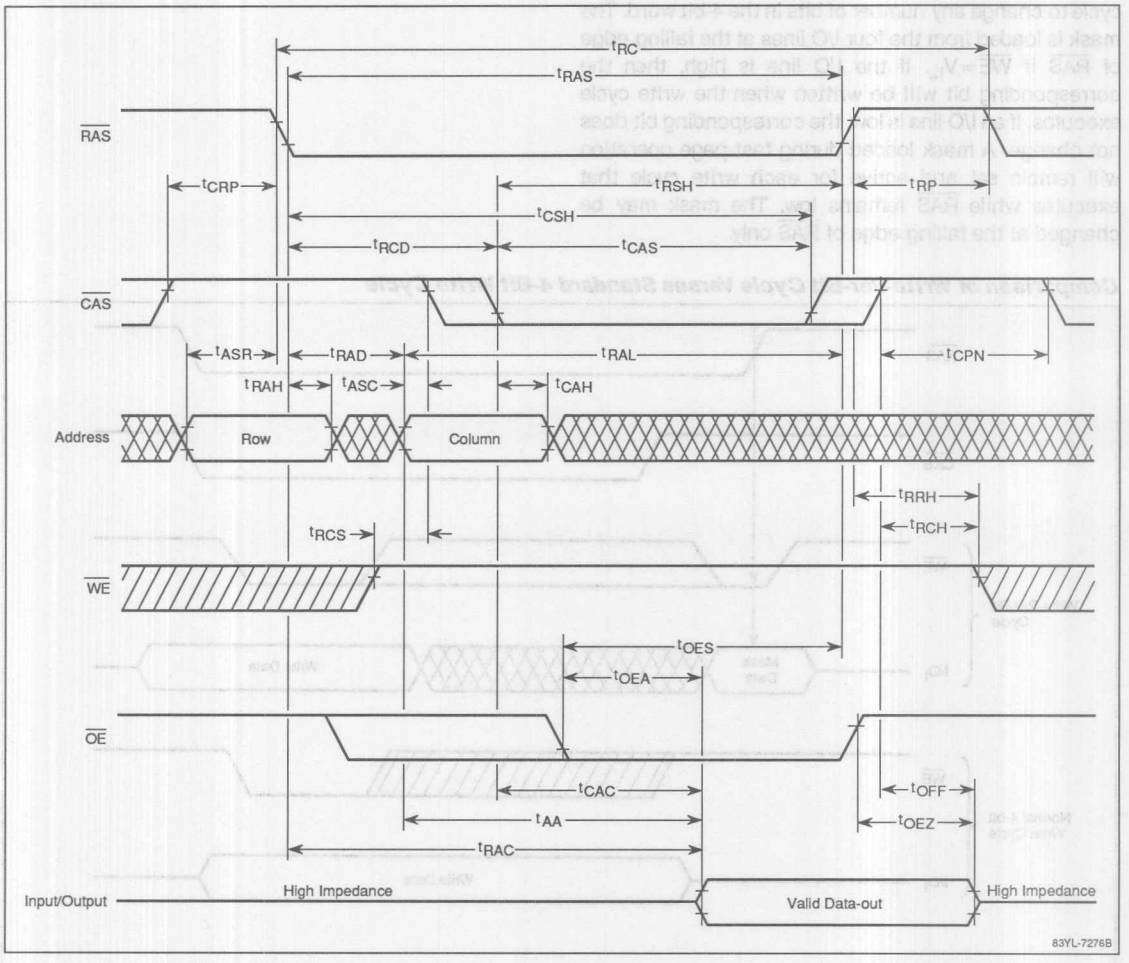
I/O	Mask Data		Write Operation
I/O_1	1	(High)	Write Bit
	0	(Low)	Disable Bit Write
I/O_2	1	(High)	Write Bit
	0	(Low)	Disable Bit Write
I/O_3	1	(High)	Write Bit
	0	(Low)	Disable Bit Write
I/O_4	1	(High)	Write Bit
	0	(Low)	Disable Bit Write

83VB-6778B

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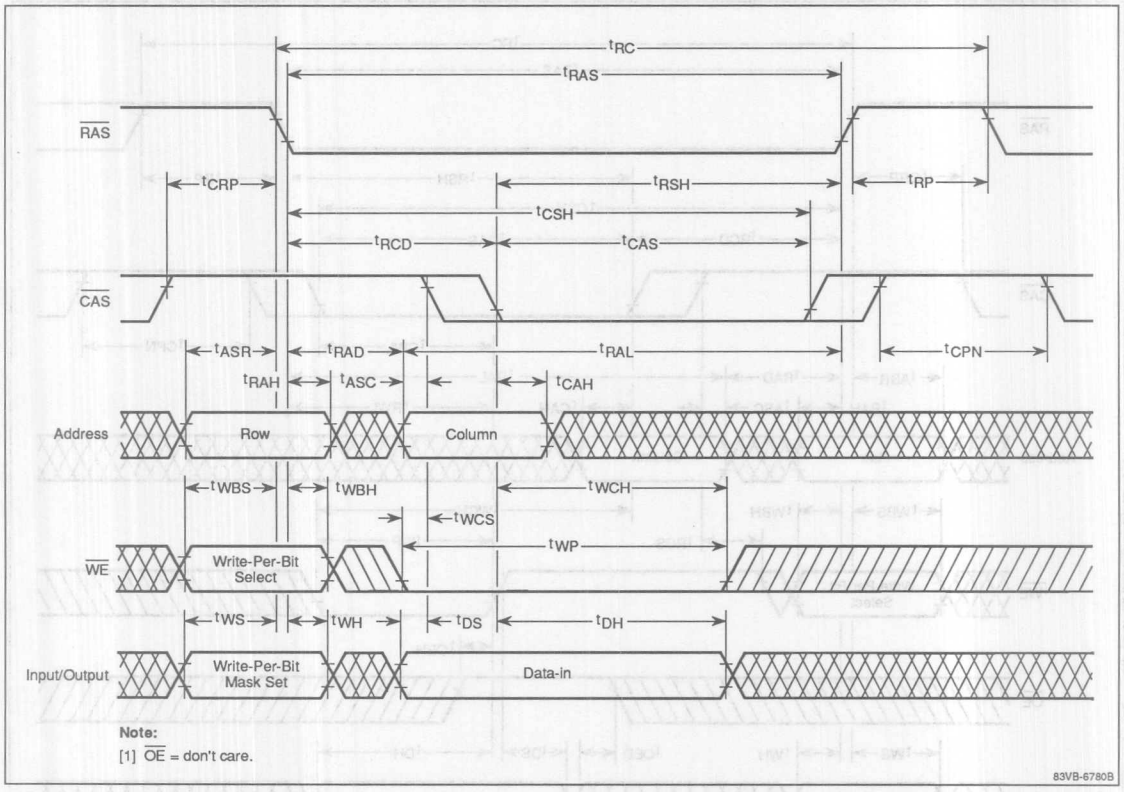
Timing Waveforms

Read Cycle



Timing Waveforms (cont)

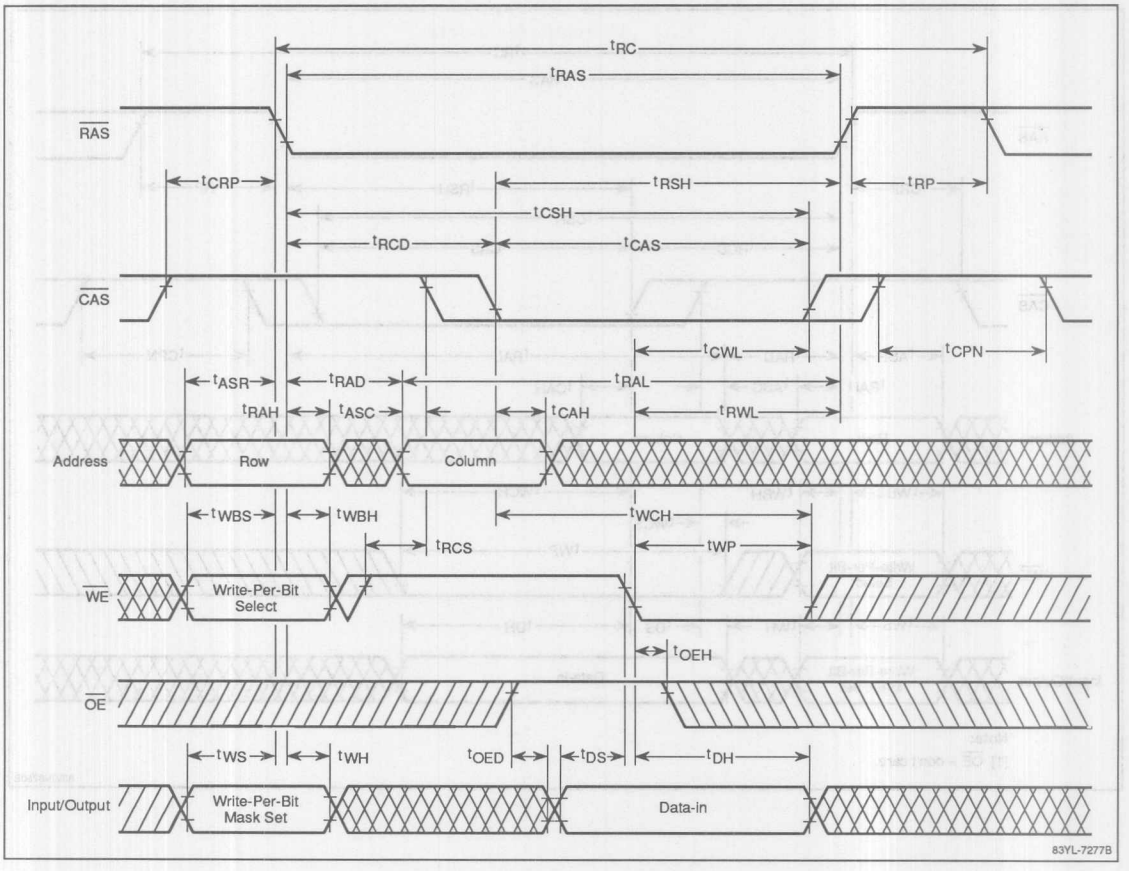
Early Write Cycle



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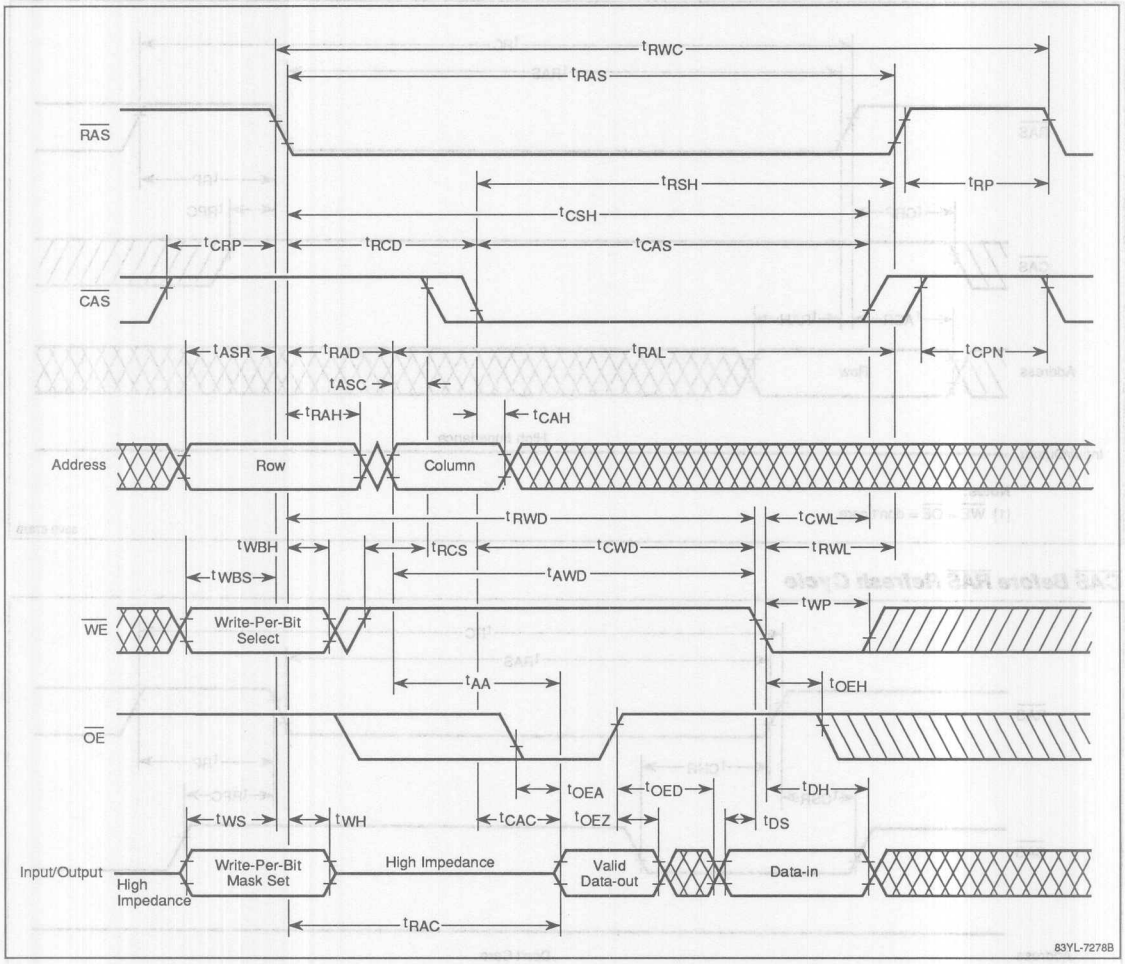
Timing Waveforms (cont)

Late Write Cycle



Timing Waveforms (cont)

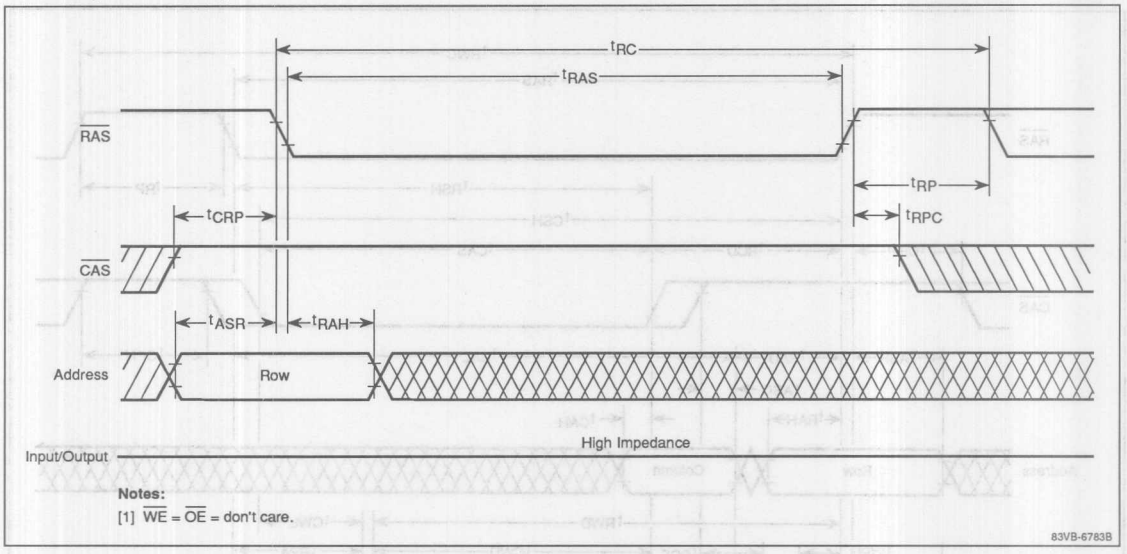
Read-Write/Read-Modify-Write Cycle



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Timing Waveforms (cont)

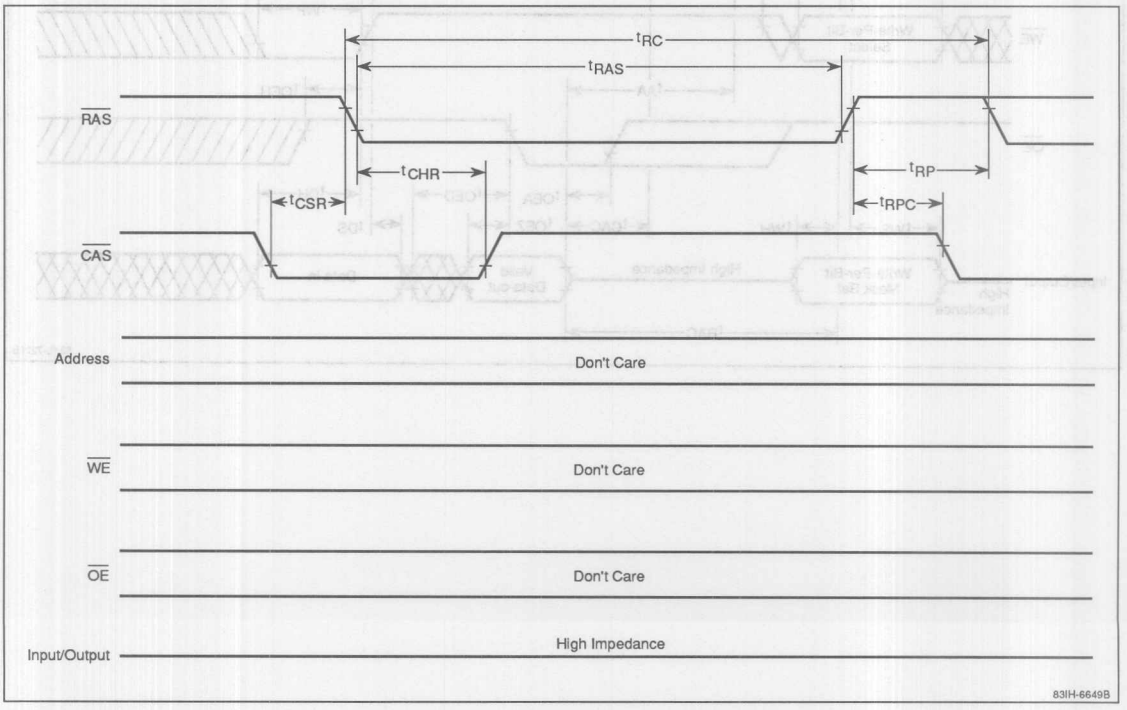
$\overline{RAS}$-Only Refresh Cycle



Notes:
[1] $\overline{WE}$ = $\overline{OE}$ = don't care.

83VB-6783B

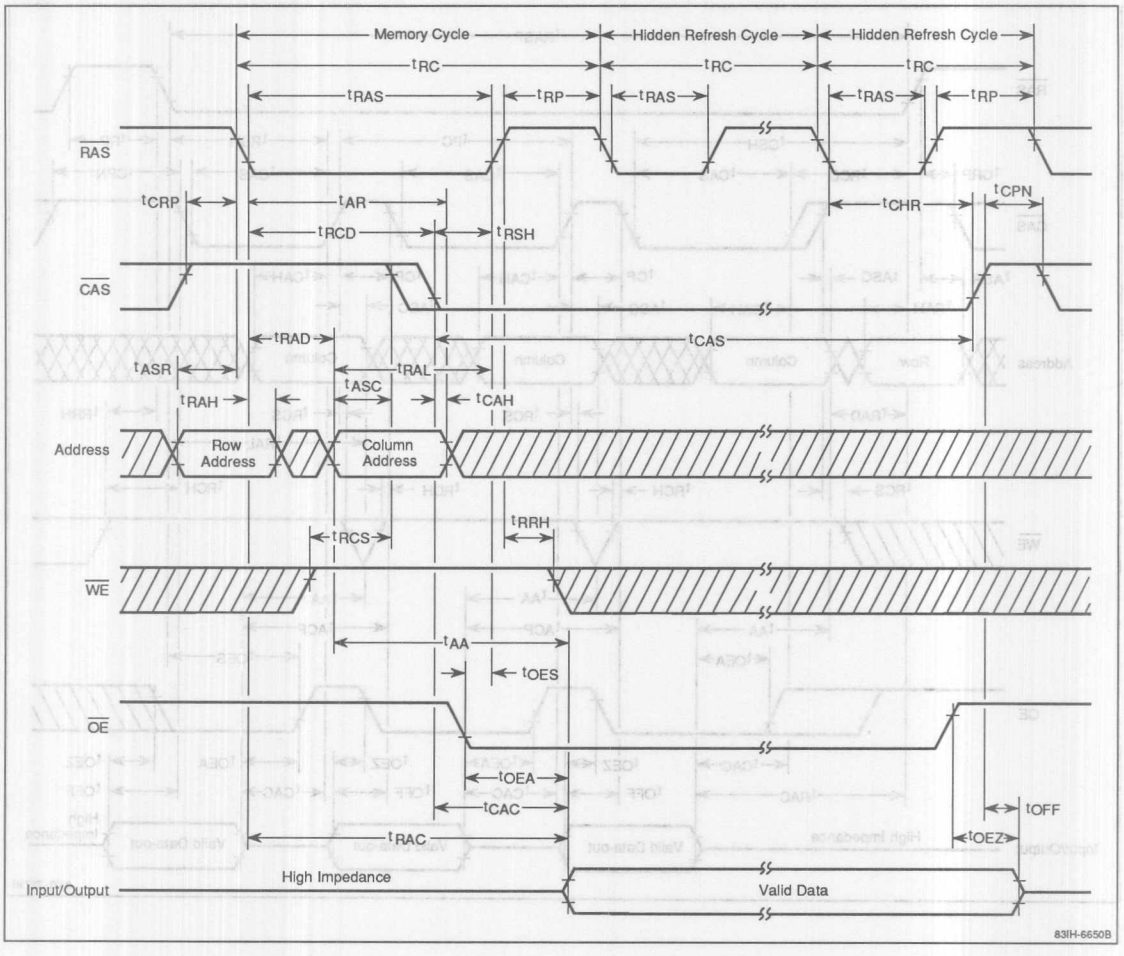
$\overline{CAS}$ Before $\overline{RAS}$ Refresh Cycle



83IH-6649B

Timing Waveforms (cont)

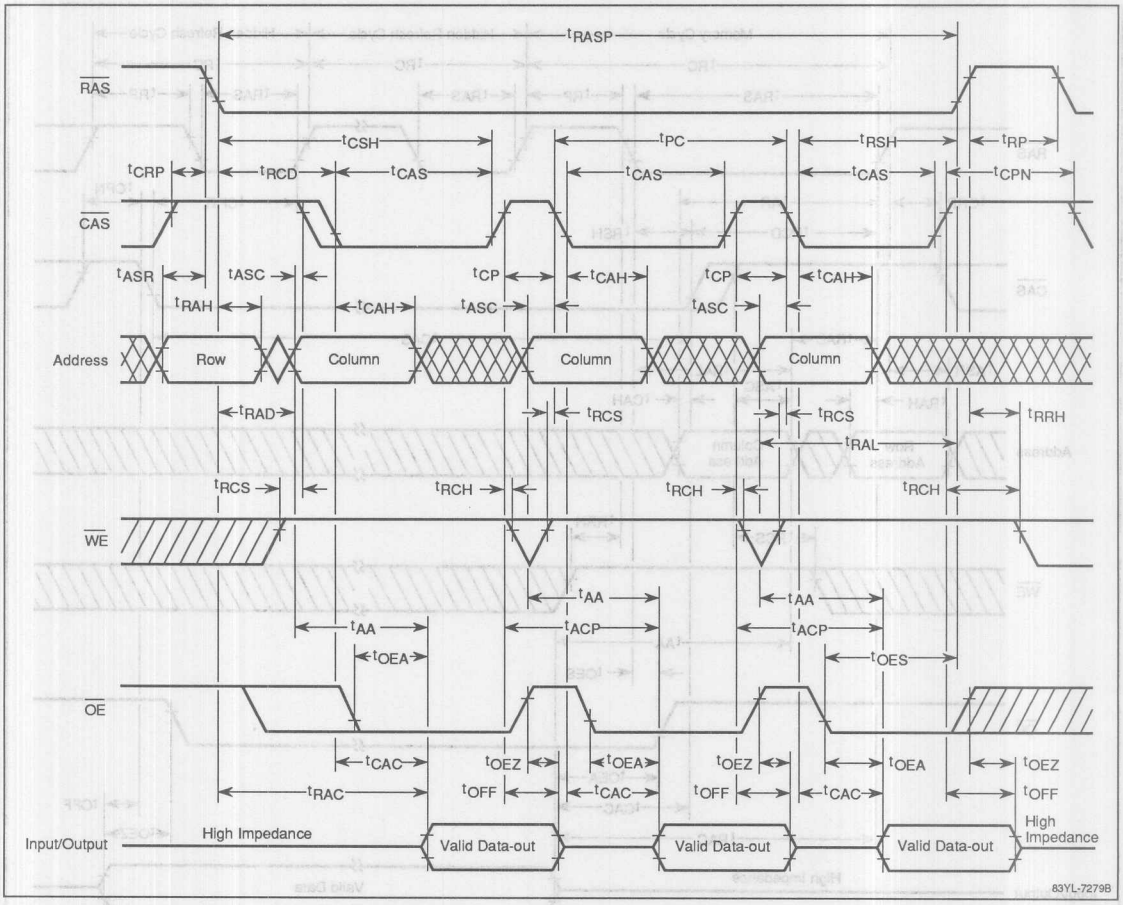
Hidden Refresh Cycle



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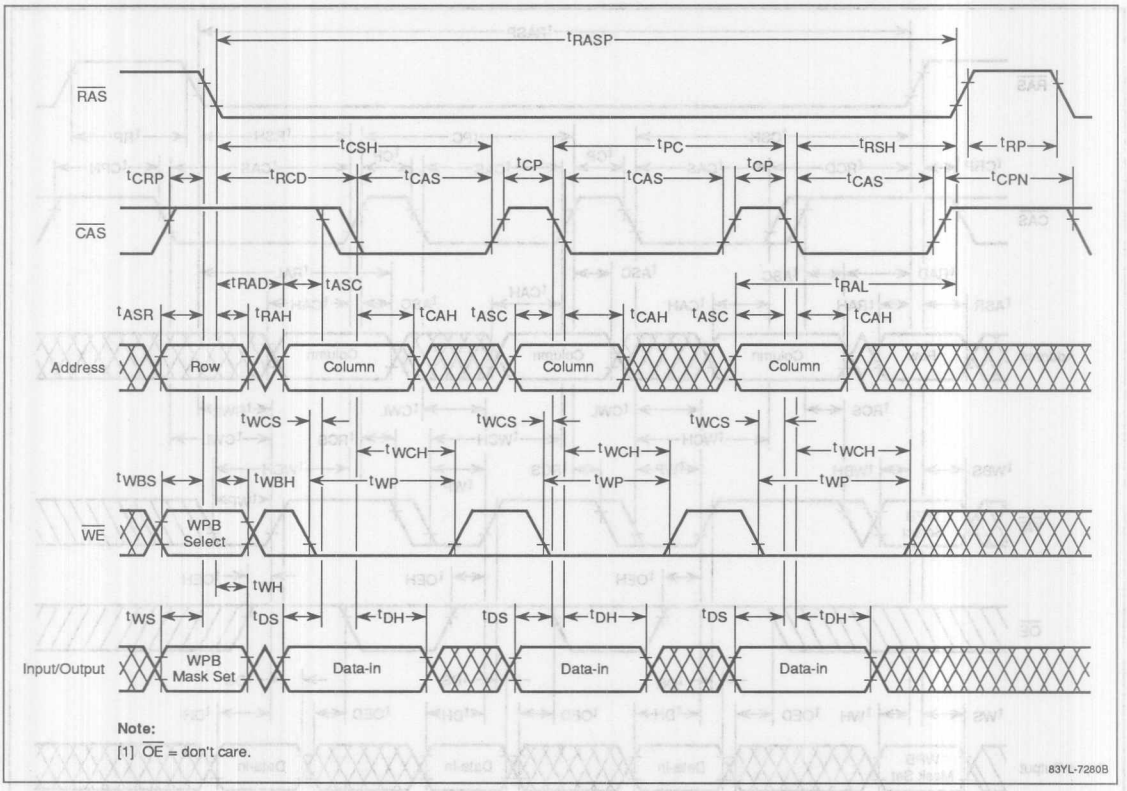
Timing Waveforms (cont)

Fast-Page Read Cycle



Timing Waveforms (cont)

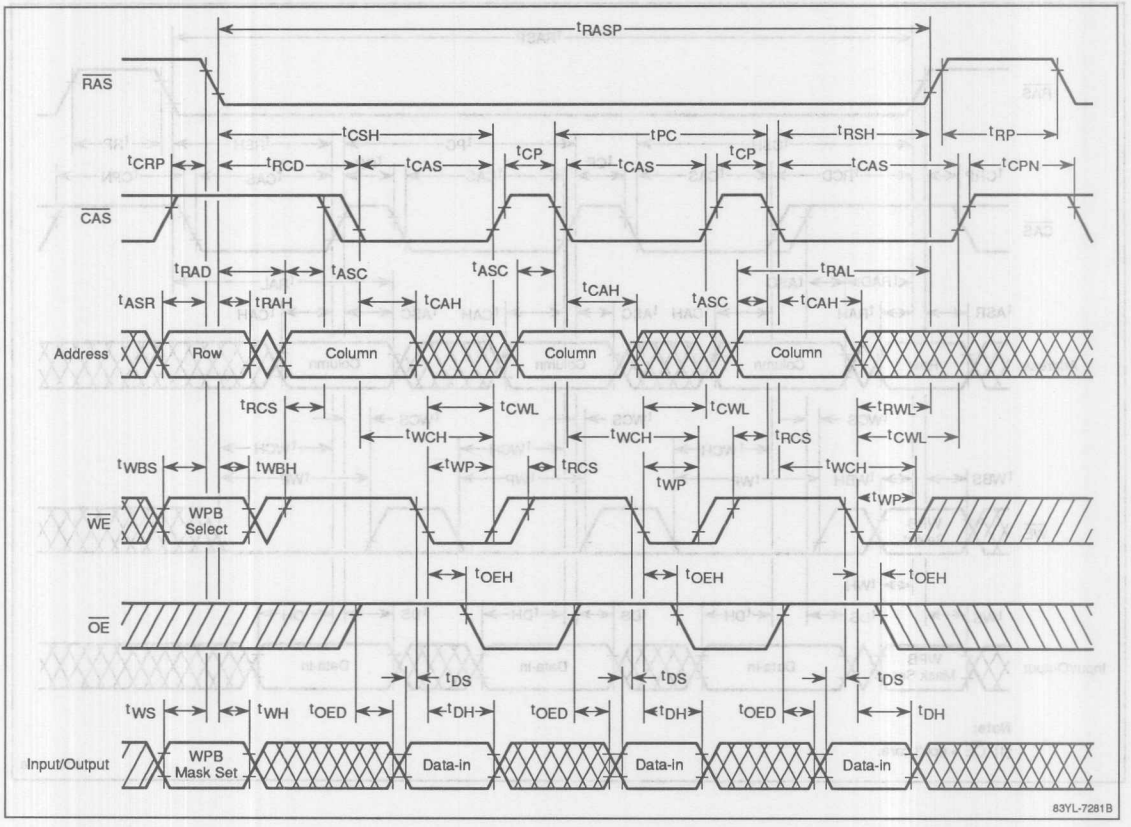
Fast-Page Early Write Cycle



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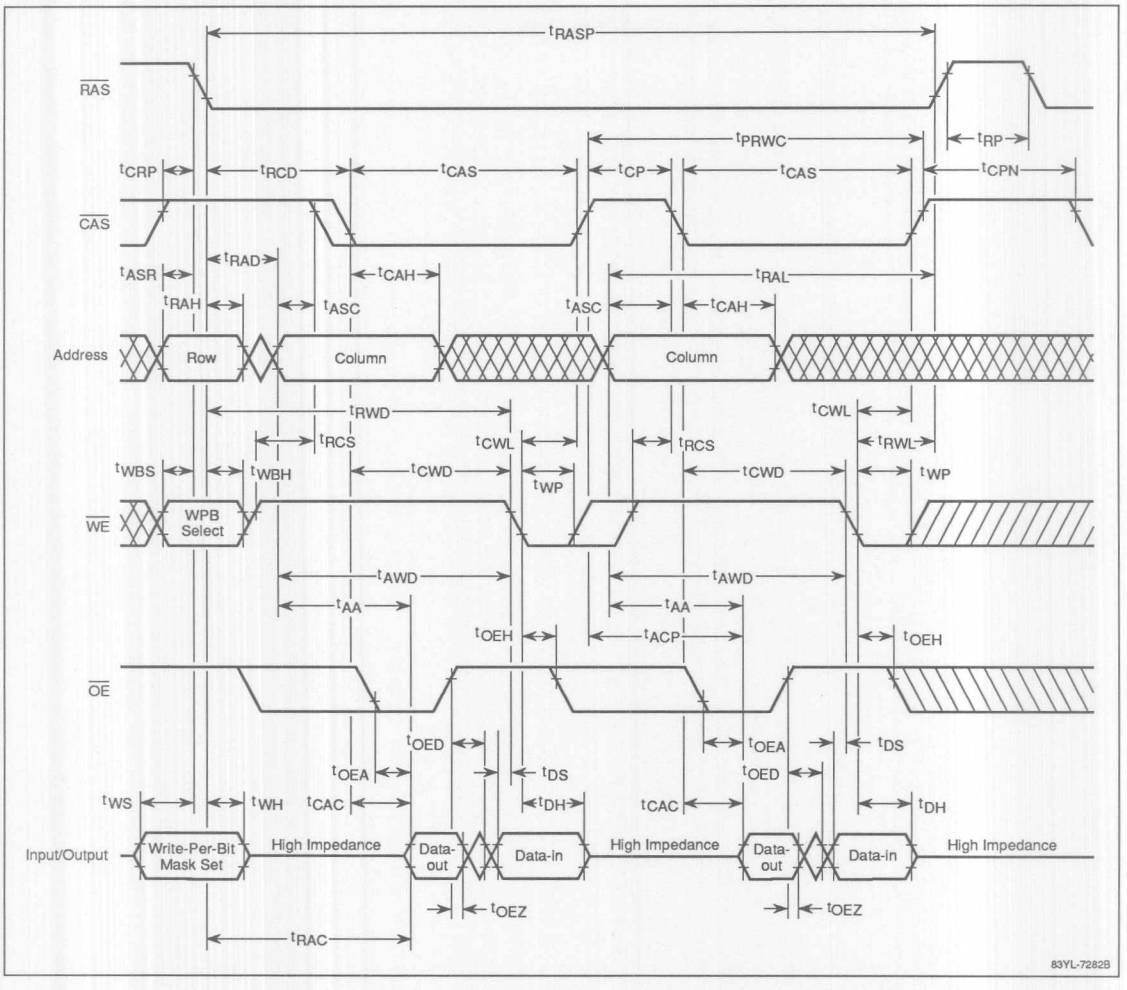
Timing Waveforms (cont)

Fast-Page Late Write Cycle

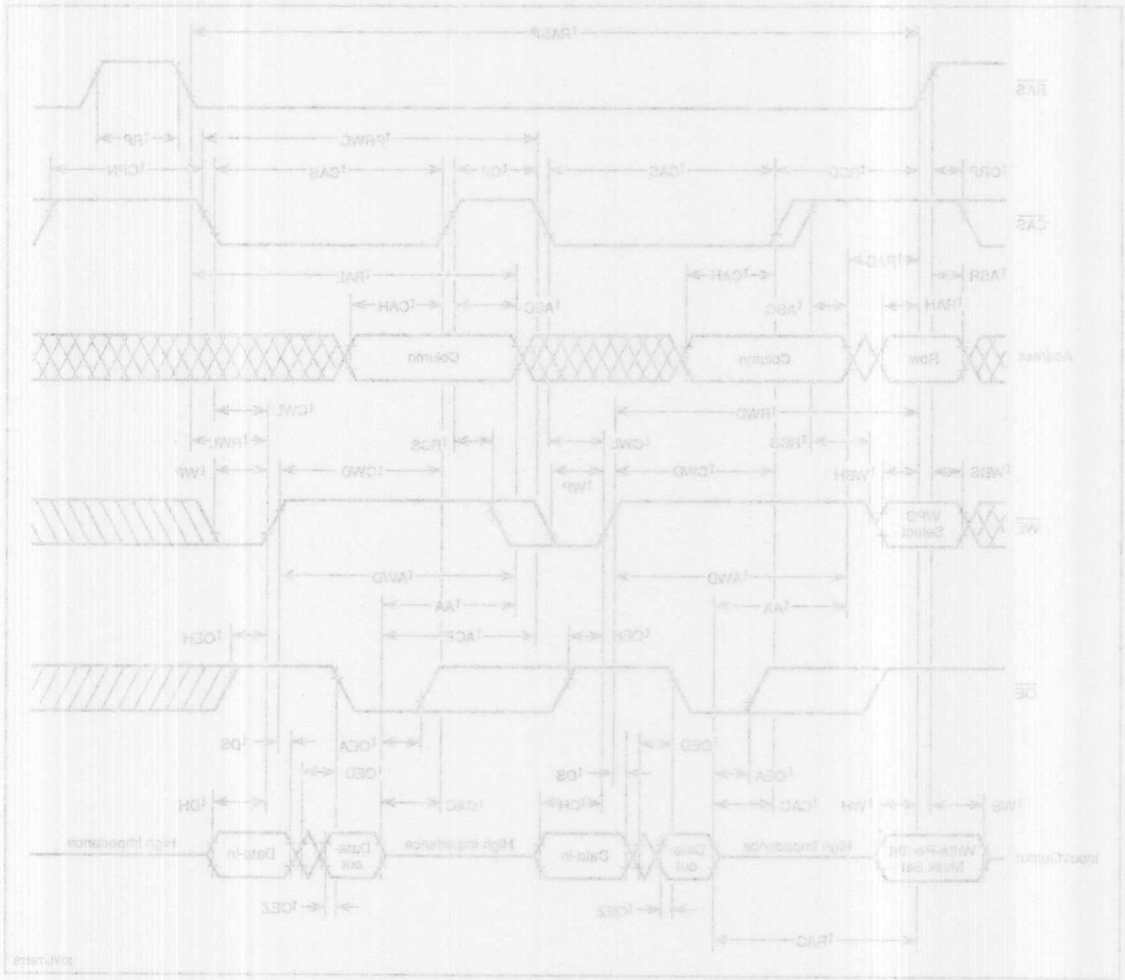


Timing Waveforms (cont)

Fast-Page Read-Write/Read-Modify-Write Cycle



6



NEC Electronics Inc.

μPD424268
262,144 x 4-Bit Dynamic CMOS RAM

Description

The μPD424268 is a 262,144 by 4-bit dynamic RAM designed with a write-per-bit option to operate from a single + 5-volt power supply. Advanced polycide technology using trench capacitors minimizes silicon area and provides high storage cell capacity, high performance, and high reliability. A single-transistor dynamic storage cell and CMOS circuitry throughout ensure minimum power dissipation, while an on-chip circuit internally generates the negative-voltage substrate bias—automatically and transparently.

The three-state I/O pins are controlled by $\overline{CS}$ independent of $\overline{RAS}$. After a valid read or read-modify-write cycle, data is held on the outputs by maintaining $\overline{CS}$ low. Data outputs return to high impedance when $\overline{CS}$ goes high. Static-column read and write cycles can be executed by switching the column address inputs.

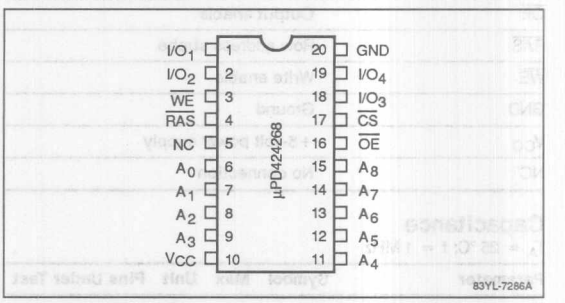
Refreshing may be accomplished by means of a $\overline{CS}$ before $\overline{RAS}$ cycle that internally generates the refresh address. Refreshing may also be accomplished by means of $\overline{RAS}$-only refresh cycles or by normal read or write cycles on the 512 address combinations of A_0 through A_8 during an 8-ms refresh period.

Features

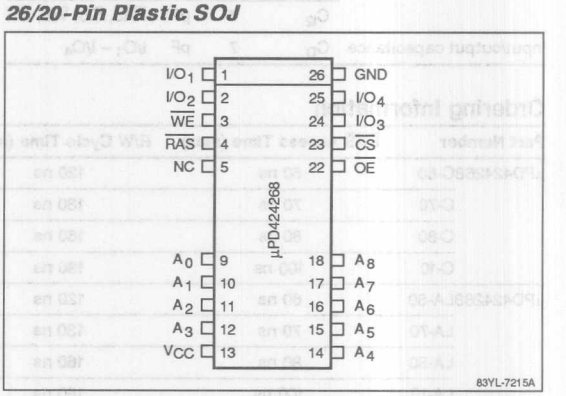
- 262,144 by 4-bit organization
- Single + 5-volt power supply
- Write-per-bit option
- Static-column option
- Low power dissipation
- $\overline{CS}$ before $\overline{RAS}$ internal refreshing
- Multiplexed address inputs
- On-chip substrate bias generator
- TTL-compatible inputs and outputs
- Nonlatched, three-state outputs
- Low input capacitance
- 512 refresh cycles every 8 ms
- High-density 20-pin plastic DIP, 26/20-pin plastic SOJ, or 20-pin plastic ZIP packaging

Pin Configurations

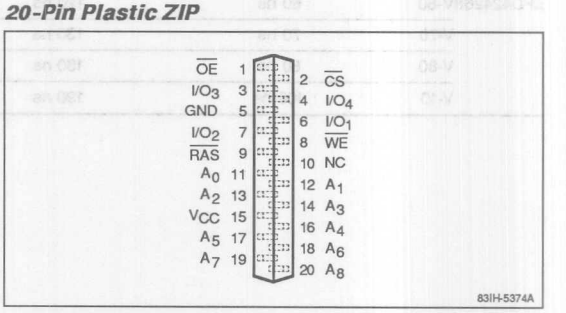
20-Pin Plastic DIP



26/20-Pin Plastic SOJ



20-Pin Plastic ZIP



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TSOP package will be available in 1991.

Pin Identification

Name	Function
A_0 - A_8	Address inputs
I/O_1 - I/O_4	Data inputs and outputs
$\overline{CS}$	Chip select
$\overline{OE}$	Output enable
$\overline{RAS}$	Row address strobe
$\overline{WE}$	Write enable
GND	Ground
V_{CC}	+5-volt power supply
NC	No connection

Capacitance

T_A = 25 °C; f = 1 MHz

Parameter	Symbol	Max	Unit	Pins Under Test
Input capacitance	C_{I1}	5	pF	Addresses
	C_{I2}	7	pF	$\overline{RAS}$, $\overline{CS}$, $\overline{WE}$, $\overline{OE}$
Input/output capacitance	C_D	7	pF	I/O_1 – I/O_4

Recommended Operating Conditions

Parameter	Symbol	Min	Typ	Max	Unit
Input voltage, high	V_{IH}	2.4		V_{CC} + 1.0	V
Input voltage, low	V_{IL}	−1.0		0.8	V
Supply voltage	V_{CC}	4.5	5.0	5.5	V
Ambient temperature	T_A	0		70	°C

Absolute Maximum Ratings

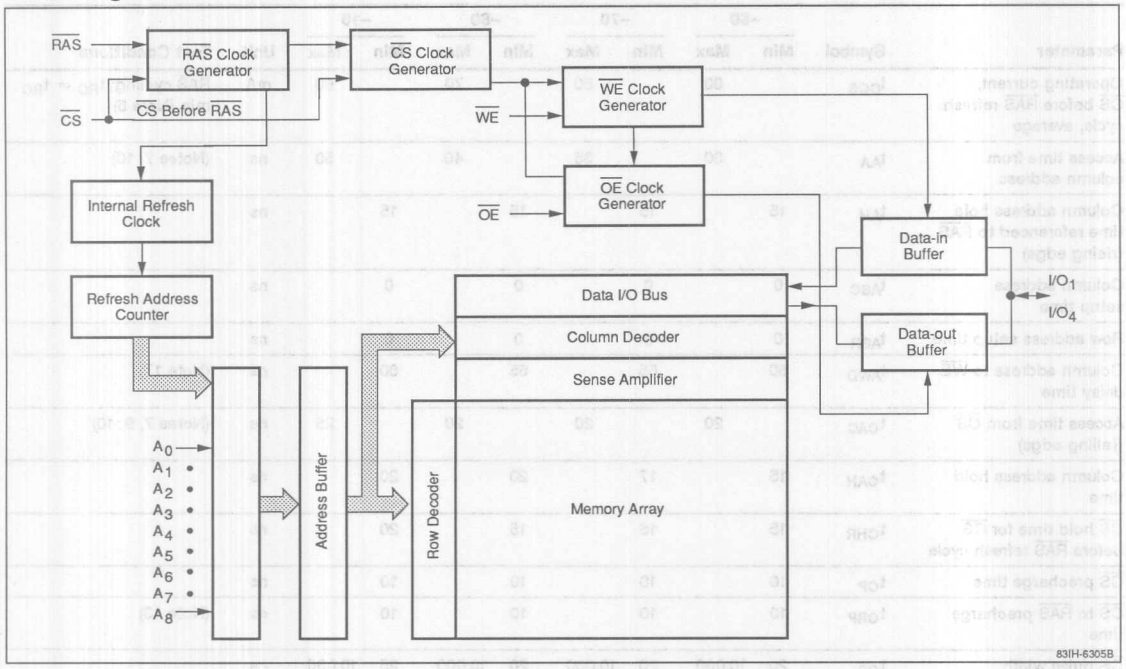
Voltage on any pin relative to GND, V_T	−1.0 to +7.0 V
Operating temperature, T_{OPR}	0 to +70 °C
Storage temperature, T_{STG}	−55 to +125 °C
Short-circuit output current, I_{OS}	50 mA
Power dissipation, P_D	1.0 W

Exposure to Absolute Maximum Ratings for extended periods may affect device reliability; exceeding the ratings could cause permanent damage. The device should be operated within the limits specified under DC and AC Characteristics.

Ordering Information

Part Number	$\overline{RAS}$ Access Time (max)	R/W Cycle Time (max)	Static-Column Cycle (max)	Package
μPD424268C-60	60 ns	120 ns	35 ns	20-pin plastic DIP
C-70	70 ns	130 ns	40 ns	
C-80	80 ns	160 ns	45 ns	
C-10	100 ns	190 ns	55 ns	
μPD424268LA-60	60 ns	120 ns	35 ns	26/20-pin plastic SOJ
LA-70	70 ns	130 ns	40 ns	
LA-80	80 ns	160 ns	45 ns	
LA-10	100 ns	190 ns	55 ns	
μPD424268V-60	60 ns	120 ns	35 ns	20-pin plastic ZIP
V-70	70 ns	130 ns	40 ns	
V-80	80 ns	160 ns	45 ns	
V-10	100 ns	190 ns	55 ns	

Block Diagram



DC Characteristics

T_A = 0 to +70°C; V_{CC} = +5.0 ±10%

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions
Standby current	I_{CC2}			2.0	mA	$\overline{RAS} \geq V_{IH}$ (min); I_O = 0 mA
				1.0	mA	$\overline{RAS} = \overline{CS} \geq V_{CC} - 0.2$ V; I_O = 0 mA
Input leakage current	$I_{I(L)}$	−10		10	μA	V_{IN} = 0 V to V_{CC}; all other pins not under test = 0 V
Output leakage current	$I_{O(L)}$	−10		10	μA	D_{OUT} disabled; V_{OUT} = 0 V to V_{CC}
Output voltage, low	V_{OL}			0.4	V	I_{OL} = 4.2 mA
Output voltage, high	V_{OH}	2.4			V	I_{OH} = −5 mA

AC Characteristics

T_A = 0 to +70°C; V_{CC} = +5.0 V ±10%

		−60		−70		−80		−10			
Parameter	Symbol	Min	Max	Min	Max	Min	Max	Min	Max	Unit	Test Conditions
Operating current, average	I_{CC1}		90		80		70		60	mA	$\overline{RAS}$, $\overline{CS}$ cycling; $t_{RC} = t_{RC}$ min (Note 5)
Operating current, $\overline{RAS}$-only refresh cycle, average	I_{CC3}		90		80		70		60	mA	$\overline{RAS}$ cycling; $\overline{CS} = V_{IH}$; $t_{RC} = t_{RC}$ min (Note 5)
Operating current, static-column cycle, average	I_{CC4}		80		70		60		50	mA	$\overline{RAS} = \overline{CS} = V_{IL}$; $t_{RSC} = t_{RSC}$ min or $t_{WSC} = t_{WSC}$ min (Note 5)

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AC Characteristics (cont)

Parameter	Symbol	-60 Min	-60 Max	-70 Min	-70 Max	-80 Min	-80 Max	-10 Min	-10 Max	Unit	Test Conditions
Operating current, $\overline{CS}$ before $\overline{RAS}$ refresh cycle, average	I_{CC5}		90		80		70		60	mA	$\overline{RAS}$ cycling; $t_{RC} = t_{RC}$ min (Note 5)
Access time from column address	t_{AA}		30		35		40		50	ns	(Notes 7, 10)
Column address hold time referenced to $\overline{RAS}$ (rising edge)	t_{AH}	15		15		15		15		ns	
Column address setup time	t_{ASC}	0		0		0		0		ns	
Row address setup time	t_{ASR}	0		0		0		0		ns	
Column address to $\overline{WE}$ delay time	t_{AWD}	50		55		65		80		ns	(Note 17)
Access time from $\overline{CS}$ (falling edge)	t_{CAC}		20		20		20		25	ns	(Notes 7, 9, 10)
Column address hold time	t_{CAH}	15		17		20		20		ns	
$\overline{CS}$ hold time for $\overline{CS}$ before $\overline{RAS}$ refresh cycle	t_{CHR}	15		15		15		20		ns	
$\overline{CS}$ precharge time	t_{CP}	10		10		10		10		ns	
$\overline{CS}$ to $\overline{RAS}$ precharge time	t_{CRP}	10		10		10		10		ns	(Note 13)
$\overline{CS}$ pulse width	t_{CS}	20	10,000	20	10,000	20	10,000	25	10,000	ns	
$\overline{CS}$ hold time	t_{CSH}	60		70		80		100		ns	
$\overline{CS}$ setup time for $\overline{CS}$ before $\overline{RAS}$ refresh cycle	t_{CSR}	10		10		10		10		ns	
$\overline{CS}$ to $\overline{WE}$ delay	t_{CWD}	40		40		45		55		ns	(Note 17)
Write command to $\overline{CS}$ lead time	t_{CWL}	15		15		20		20		ns	
Data-in hold time	t_{DH}	15		15		20		20		ns	(Note 16)
Data-in setup time	t_{DS}	0		0		0		0		ns	(Note 16)
Access time from $\overline{OE}$	t_{OEA}		20		20		20		25	ns	(Note 7)
$\overline{OE}$ data delay time	t_{OED}	15		15		20		25		ns	
$\overline{OE}$ command hold time	t_{OEH}	0		0		0		0		ns	
$\overline{OE}$ to $\overline{RAS}$ inactive setup time	t_{OES}	0		0		0		0		ns	
Output turnoff delay from $\overline{OE}$	t_{OEZ}	0	15	0	15	0	20	0	25	ns	(Note 11)
Output buffer turnoff delay	t_{OFF}	0	15	0	15	0	20	0	25	ns	(Note 11)
Output hold time from address	t_{OH}	5		5		5		5		ns	
Output enable time from $\overline{WE}$	t_{OW}		25		25		25		25	ns	(Note 7)
Access time from $\overline{WE}$	t_{PWA}		60		70		80		100	ns	(Notes 7, 18)

AC Characteristics (cont)

Parameter	Symbol	-60 Min	-60 Max	-70 Min	-70 Max	-80 Min	-80 Max	-10 Min	-10 Max	Unit	Test Conditions
Column address hold time referenced to $\overline{WE}$	t_{PWH}	60		70		80		100		ns	
Access time from $\overline{RAS}$	t_{RAC}		60		70		80		100	ns	(Notes 7, 8)
$\overline{RAS}$ to column address delay time	t_{RAD}	15	30	15	35	17	40	17	50	ns	(Note 10)
Row address hold time	t_{RAH}	10		10		12		12		ns	
Column address lead time referenced to $\overline{RAS}$ (rising edge)	t_{RAL}	30		35		40		50		ns	
$\overline{RAS}$ pulse width	t_{RAS}	60	10,000	70	10,000	80	10,000	100	10,000	ns	
$\overline{RAS}$ pulse width, static-column cycle	t_{RASC}	60	100,000	70	100,000	80	100,000	100	100,000	ns	
Random read or write cycle time	t_{RC}	120		130		160		190		ns	(Note 6)
$\overline{RAS}$ to $\overline{CS}$ delay time	t_{RCD}	20	40	20	50	25	60	25	75	ns	(Note 12)
Read command hold time referenced to $\overline{CS}$	t_{RCH}	0		0		0		0		ns	(Note 14)
Read command setup time	t_{RCS}	0		0		0		0		ns	
Refresh period	t_{REF}		8		8		8		8	ms	Addresses A_0 - A_8
$\overline{RAS}$ precharge time	t_{RP}	50		50		70		80		ns	
$\overline{RAS}$ precharge $\overline{CS}$ hold time	t_{RPC}	10		10		10		10		ns	
Read command hold time referenced to $\overline{RAS}$	t_{RRH}	10		10		10		10		ns	(Note 14)
Static-column read cycle time	t_{RSC}	35		40		45		55		ns	(Note 6)
$\overline{RAS}$ hold time	t_{RSH}	20		20		20		25		ns	
$\overline{RAS}$ to second $\overline{WE}$ delay time	t_{RSW}	75		85		95		115		ns	
Read-write cycle time	t_{RWC}	165		175		215		255		ns	(Note 6)
$\overline{RAS}$ to $\overline{WE}$ delay	t_{RWD}	80		90		105		130		ns	(Note 17)
Write command to $\overline{RAS}$ lead time	t_{RWL}	20		20		25		30		ns	
Static-column read-modify-write cycle time	t_{RWSC}	85		95		110		135		ns	(Note 6)
Rise and fall transition time	t_T	3	50	3	50	3	50	3	50	ns	(Note 4)
$\overline{WE}$ to column address delay time	t_{WAD}	20	30	22	35	25	40	25	50	ns	(Note 18)
Write-per-bit hold time	t_{WBH}	10		10		10		10		ns	
Write-per-bit setup time	t_{WBS}	0		0		0		0		ns	
Write command hold time	t_{WCH}	15		15		15		20		ns	
Write command setup time	t_{WCS}	0		0		0		0		ns	(Note 17)

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AC Characteristics (cont)

Parameter	Symbol	-60 Min	-60 Max	-70 Min	-70 Max	-80 Min	-80 Max	-10 Min	-10 Max	Unit	Test Conditions
Write-per-bit mask data hold time	t_{WH}	10		10		10		10		ns	
Write-per-bit mask data setup time	t_{WS}	0		0		0		0		ns	
Write invalid time	t_{WI}	10		10		10		10		ns	
Write command pulse width	t_{WP}	15		15		15		20		ns	(Note 15)
Static-column write cycle time	t_{WSC}	35		40		45		55		ns	(Note 6)

Notes:

(1) All voltages are referenced to GND.

(2) An initial pause of 100 μs is required after power-up, followed by any eight $\overline{RAS}$ cycles, before proper device operation is achieved.

(3) AC measurements assume t_T = 5 ns.

(4) V_{IH} (min) and V_{IL} (max) are reference levels for measuring the timing of input signals. Transition times are measured between V_{IH} and V_{IL}.

(5) I_{CC1}, I_{CC3}, I_{CC4}, and I_{CC5} depend on output loading and cycle rates. Specified values are obtained with the output open. I_{CC3} is measured assuming that all column address inputs are held at either a high level or a low level during $\overline{RAS}$-only refresh cycles. I_{CC4} is measured assuming that all column address inputs are switched only once during each static-column cycle.

(6) The minimum specifications are used only to indicate the cycle time at which proper operation over the full temperature range (T_A = 0 to +70°C) is assured.

(7) Load = 2 TTL (–1 mA, +4 mA) loads and 100 pF (V_{OH} = 2.4 V, V_{OL} = 0.4 V).

(8) Assumes that $t_{RCD} \leq t_{RCD}$ (max) and $t_{RAD} \leq t_{RAD}$ (max). If t_{RCD} or t_{RAD} is greater than the maximum recommended value in this table, t_{RAC} increases by the amount that t_{RCD} or t_{RAD} exceeds the value shown.

(9) Assumes that $t_{RCD} \geq t_{RCD}$ (max) and $t_{RAD} \leq t_{RAD}$ (max).

(10) If $t_{RAD} \geq t_{RAD}$ (max), then the access time is defined by t_{AA}.

(11) t_{OFF} (max) and t_{OEZ} (max) define the time at which the outputs achieve the open-circuit condition and are not referenced to V_{OH} or V_{OL}.

(12) Operation within the t_{RCD} (max) limit assures that t_{RAC} (max) can be met. t_{RCD} (max) is specified as a reference point only; if t_{RCD} is greater than t_{RCD} (max), then access time is controlled exclusively by t_{CAC}, t_{AA}, or t_{OEA}.

(13) The t_{CRP} requirement should be applicable for $\overline{RAS}$/$\overline{CS}$ cycles preceded by any cycle.

(14) Either t_{RRH} or t_{RCH} must be satisfied for a read cycle.

(15) Parameter t_{WP} is applicable for a delayed write cycle such as a read-write/read-modify-write cycle. For early write operation, both t_{WCS} and t_{WCH} must be met.

(16) These parameters are referenced to the falling edge of $\overline{CS}$ for early write cycles and to the falling edge of $\overline{WE}$ for delayed write or read-modify-write cycles.

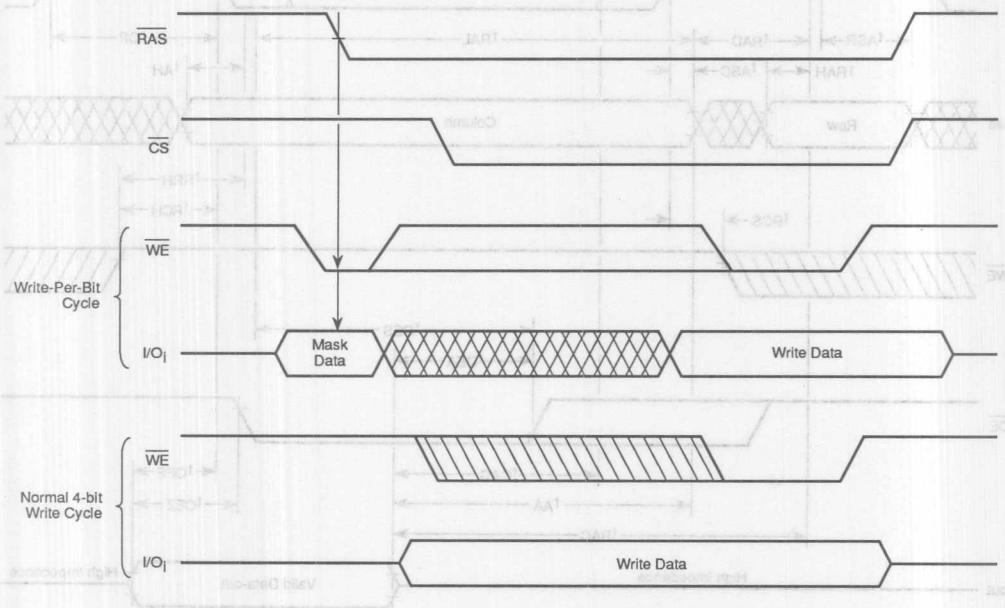
(17) t_{WCS}, t_{RWD}, t_{CWD}, and t_{AWD} are restrictive operating parameters in read-write/read-modify-write cycles only. If $t_{WCS} \geq t_{WCS}$ (min), the cycle is an early write cycle and the data I/O pins will remain open-circuit throughout the entire cycle. If $t_{CWD} \geq t_{CWD}$ (min), $t_{RWD} \geq t_{RWD}$ (min), and $t_{AWD} \geq t_{AWD}$ (min), the cycle is a read-write cycle and the data I/O pins will contain data read from the selected cells. If neither of the above conditions is met, the condition of the data I/O pins (at access time and until $\overline{CS}$ returns to V_{IH}) is indeterminate.

(18) If $t_{WAD} \leq t_{WAD}$ (max), then the access time is defined by t_{PWA}.

Write-Per-Bit Option

The write-per-bit option may be used to allow a write cycle to change any number of bits in the 4-bit word. The mask is loaded from the four I/O lines at the falling edge of $\overline{RAS}$ if $\overline{WE} = V_{IL}$. If the I/O line is high, then the corresponding bit will be written when the write cycle executes. If an I/O line is low, the corresponding bit does not change. A mask loaded during static-column operation will remain set and active for each write cycle that executes while $\overline{RAS}$ remains low. The mask may be changed at the falling edge of $\overline{RAS}$ only.

Comparison of Write-Per-Bit Cycle Versus Standard 4-Bit Write Cycle



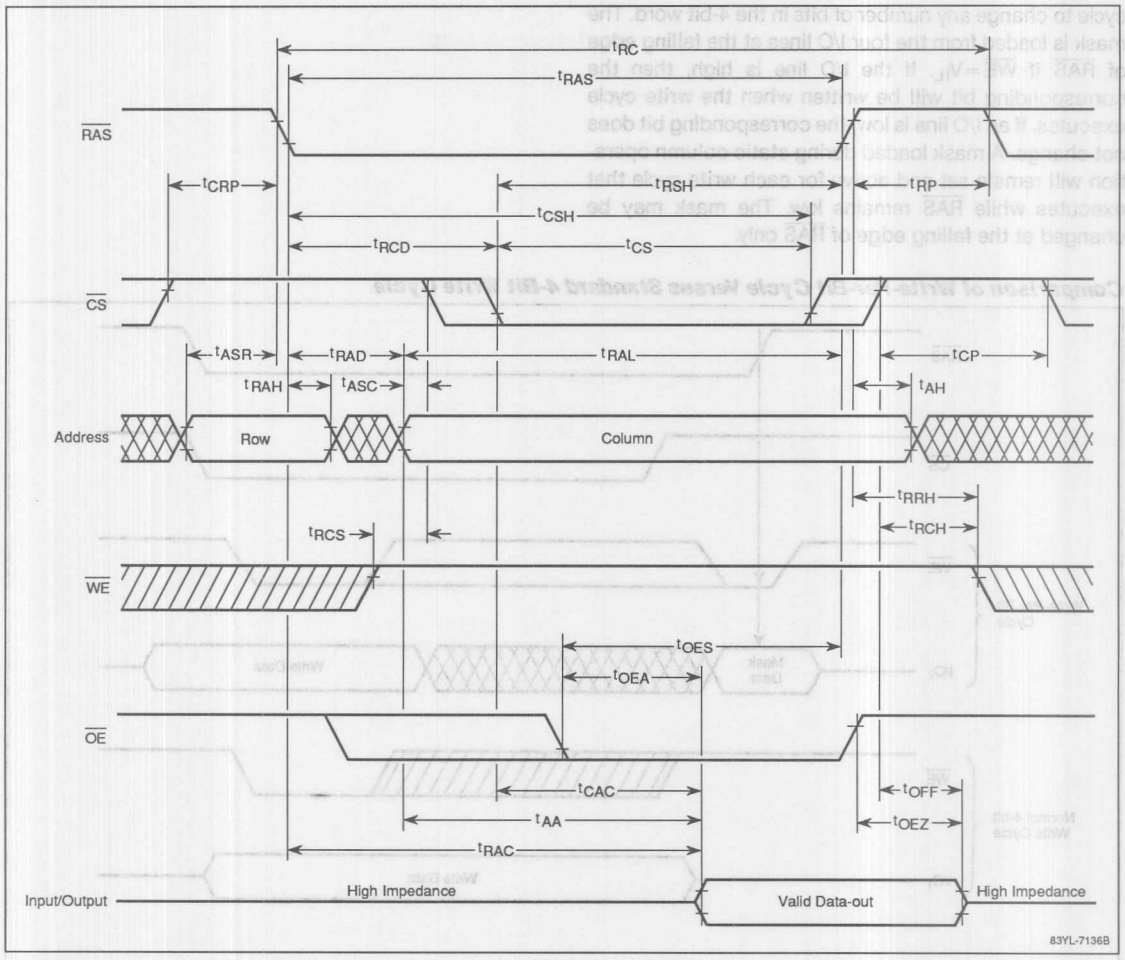
I/O	Mask Data		Write Operation
I/O_1	1	(High)	Write Bit
	0	(Low)	Disable Bit Write
I/O_2	1	(High)	Write Bit
	0	(Low)	Disable Bit Write
I/O_3	1	(High)	Write Bit
	0	(Low)	Disable Bit Write
I/O_4	1	(High)	Write Bit
	0	(Low)	Disable Bit Write

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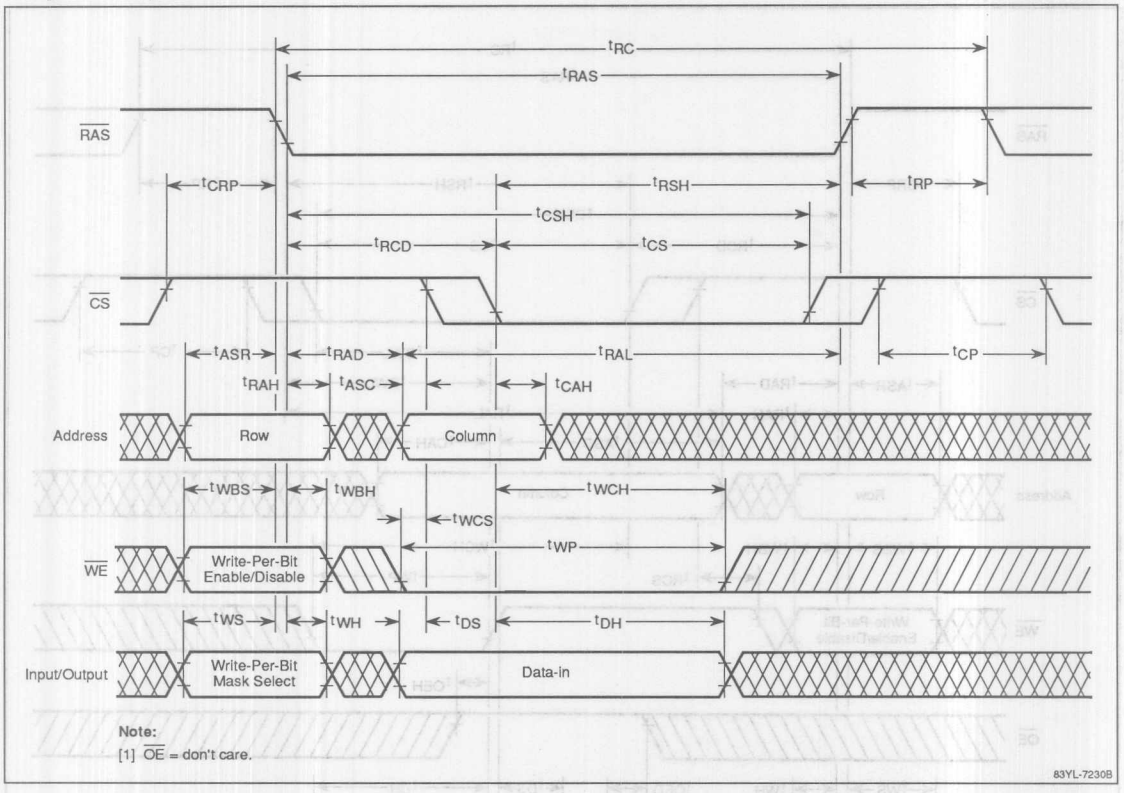
Timing Waveforms

Read Cycle



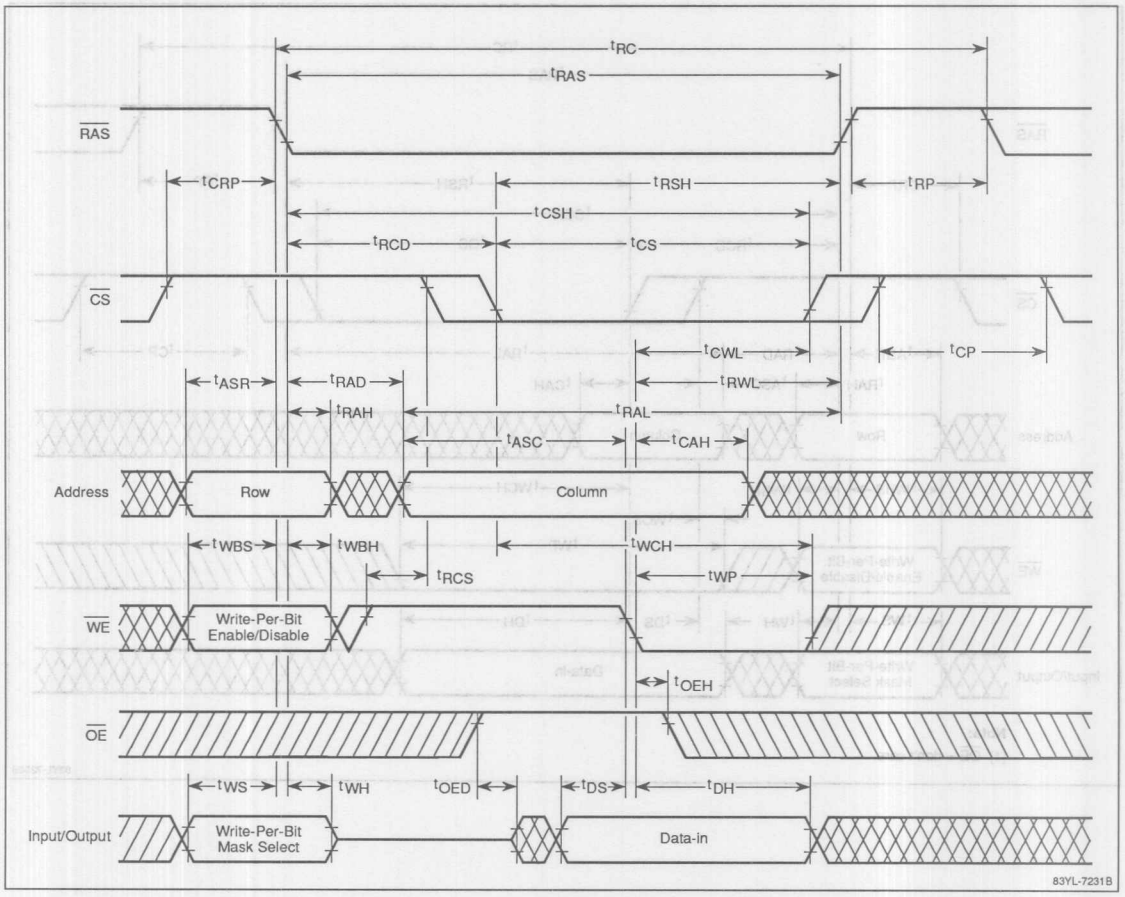
Timing Waveforms (cont)

Early Write Cycle



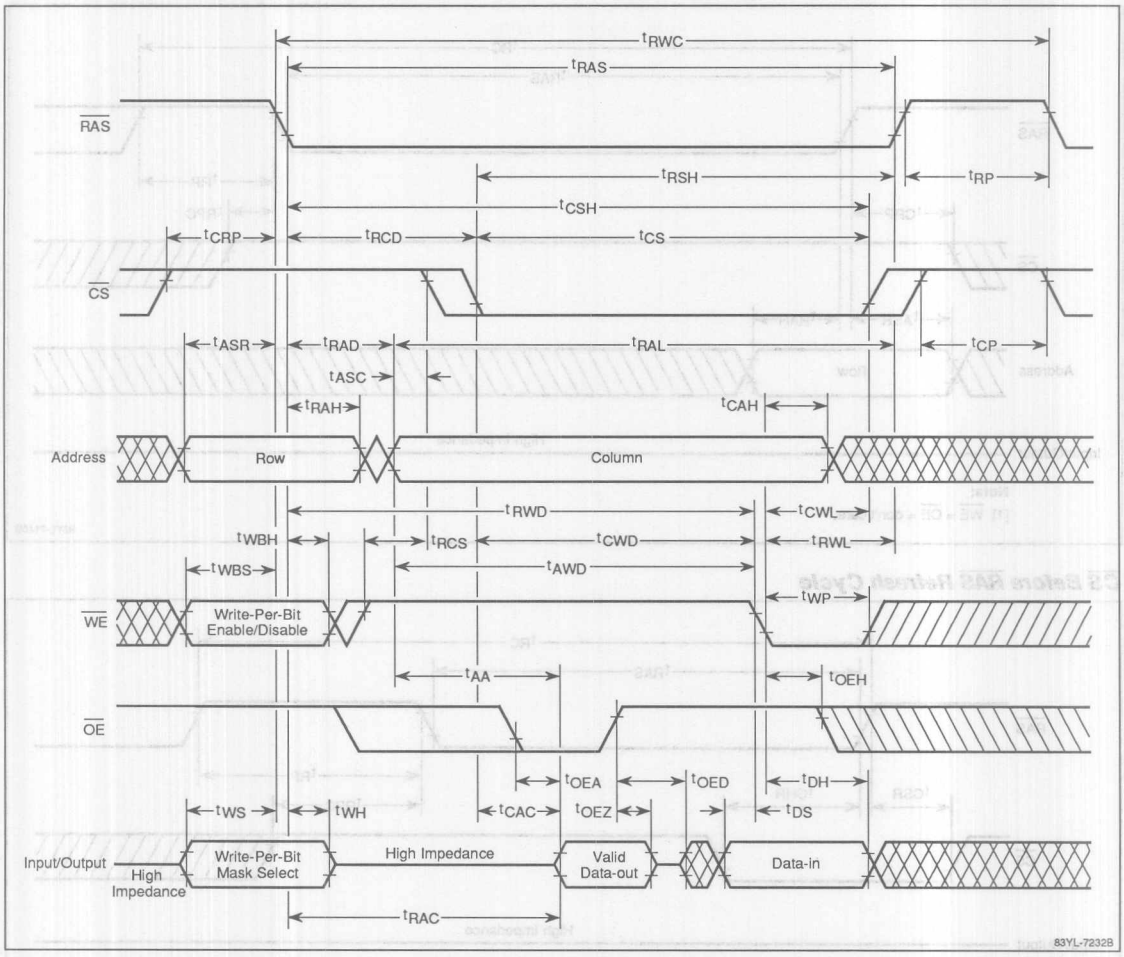
Timing Waveforms (cont)

Late Write Cycle



Timing Waveforms (cont)

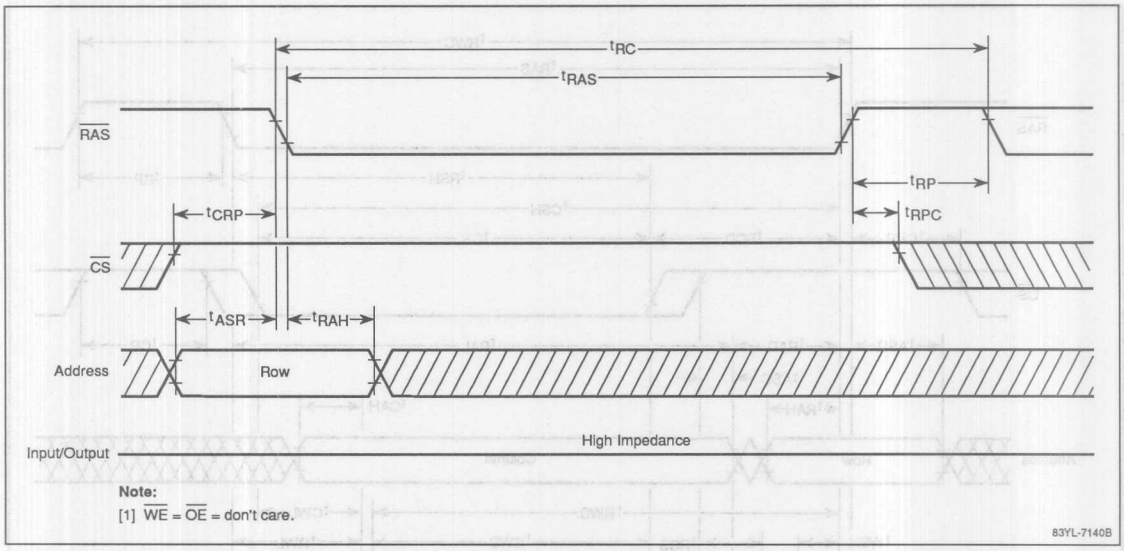
Read-Write/Read-Modify-Write Cycle



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Timing Waveforms (cont)

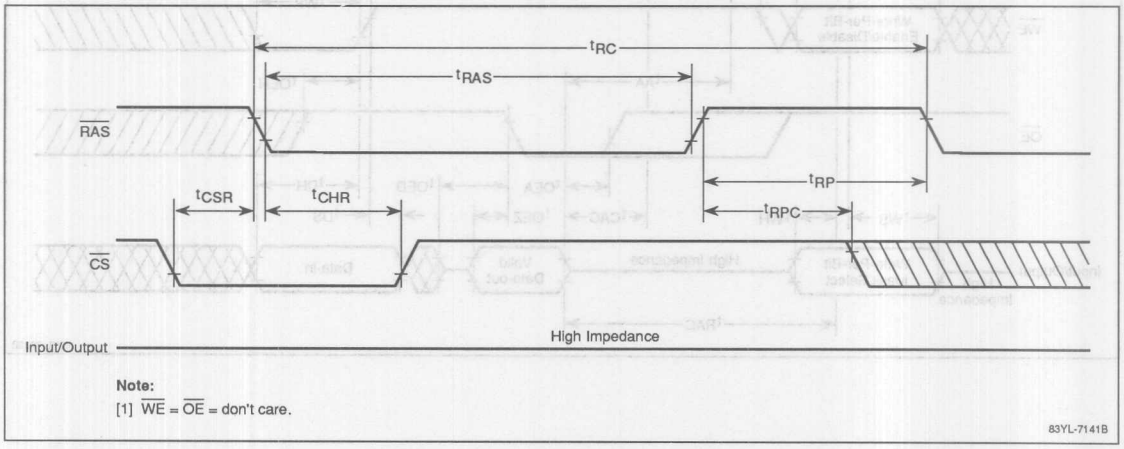
$\overline{RAS}$-Only Refresh Cycle



Note:
[1] $\overline{WE}$ = $\overline{OE}$ = don't care.

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$\overline{CS}$ Before $\overline{RAS}$ Refresh Cycle

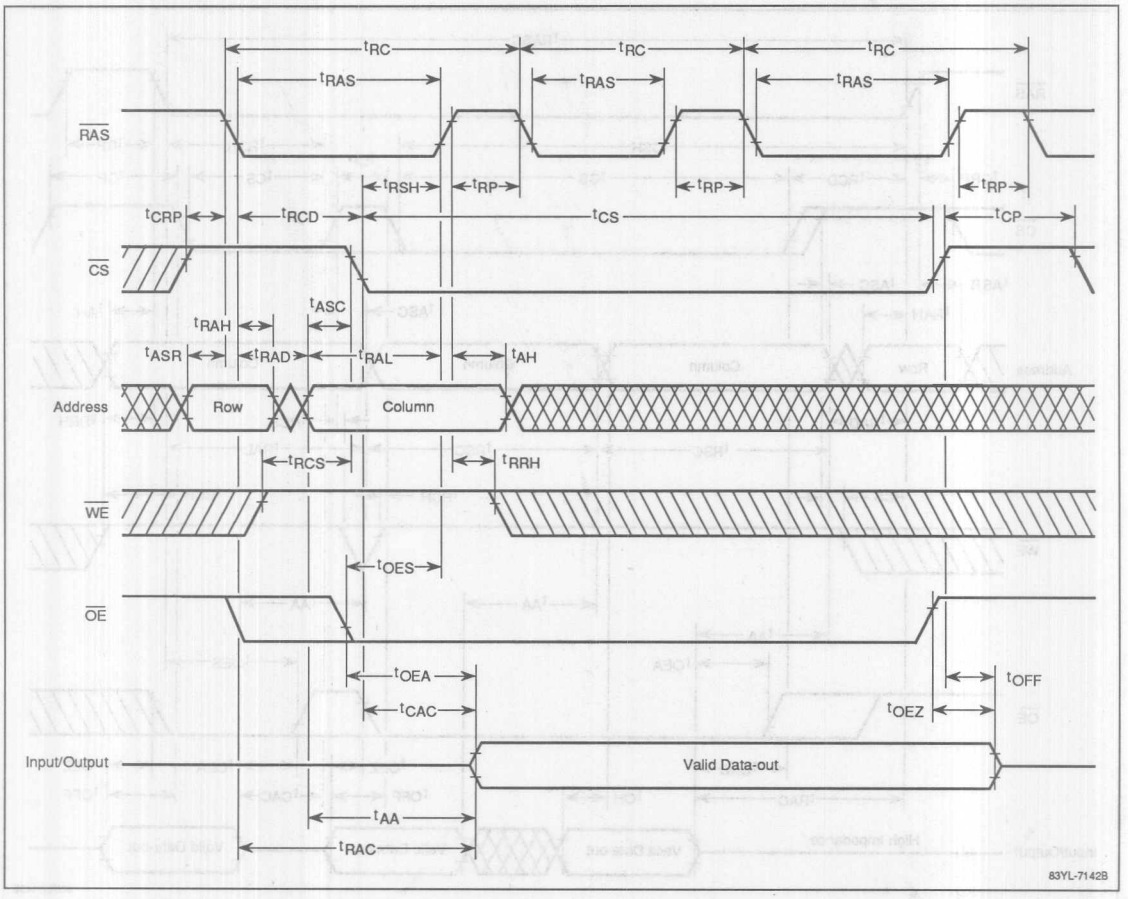


Note:
[1] $\overline{WE}$ = $\overline{OE}$ = don't care.

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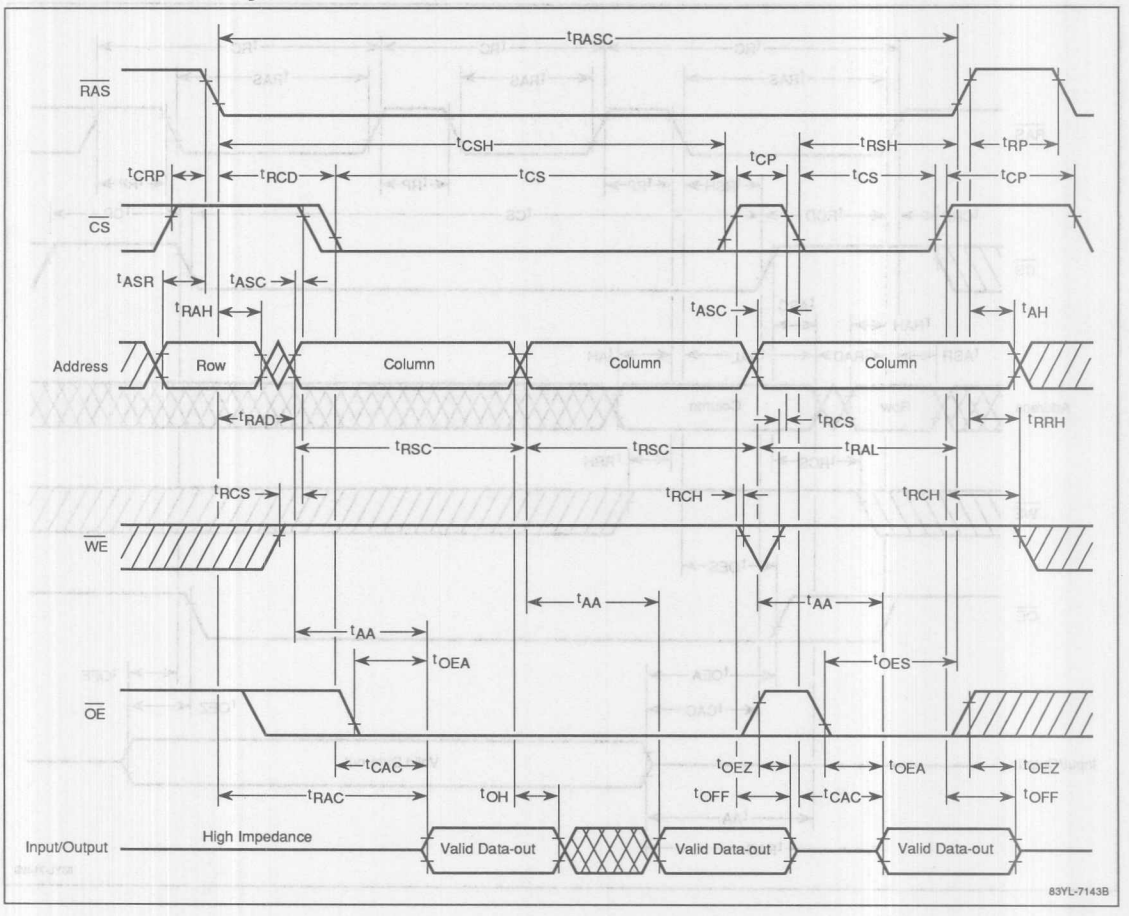
Timing Waveforms (cont)

Hidden Refresh Cycle



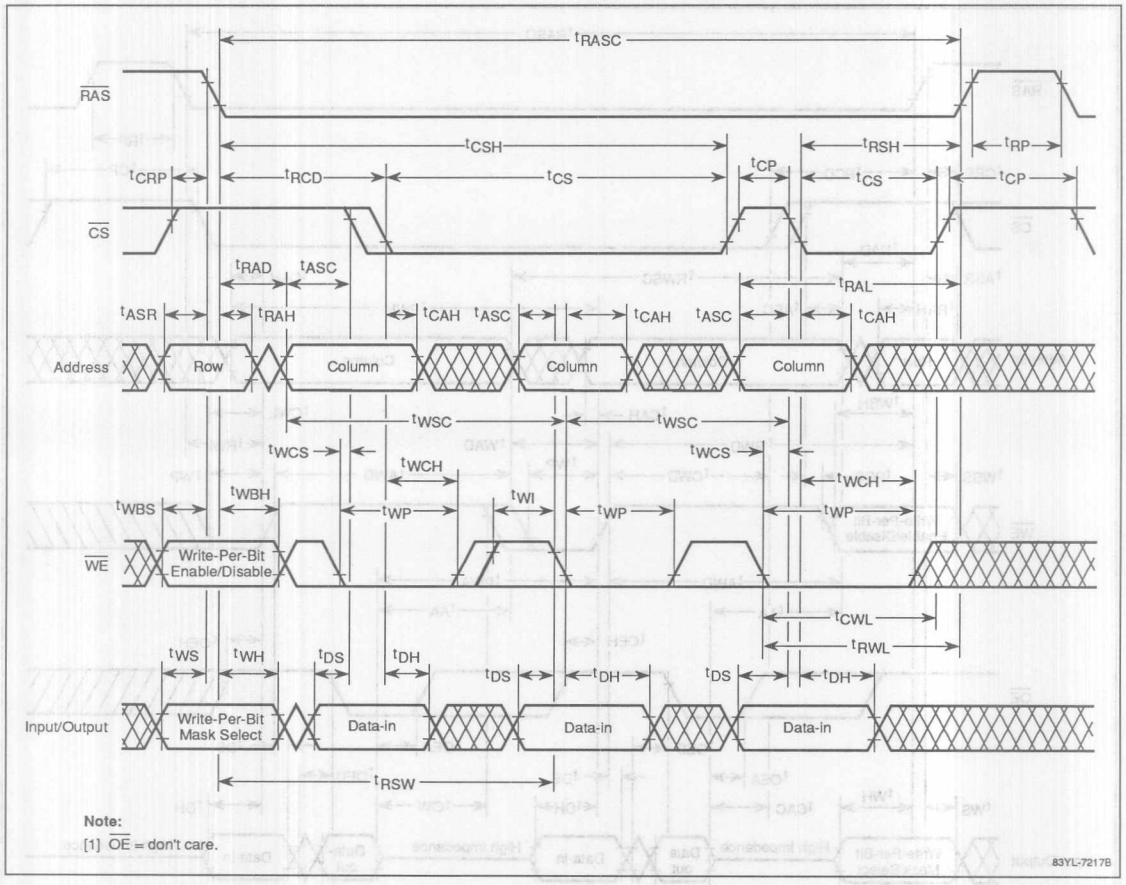
Timing Waveforms (cont)

Static-Column Read Cycle



Timing Waveforms (cont)

Static-Column Early Write Cycle



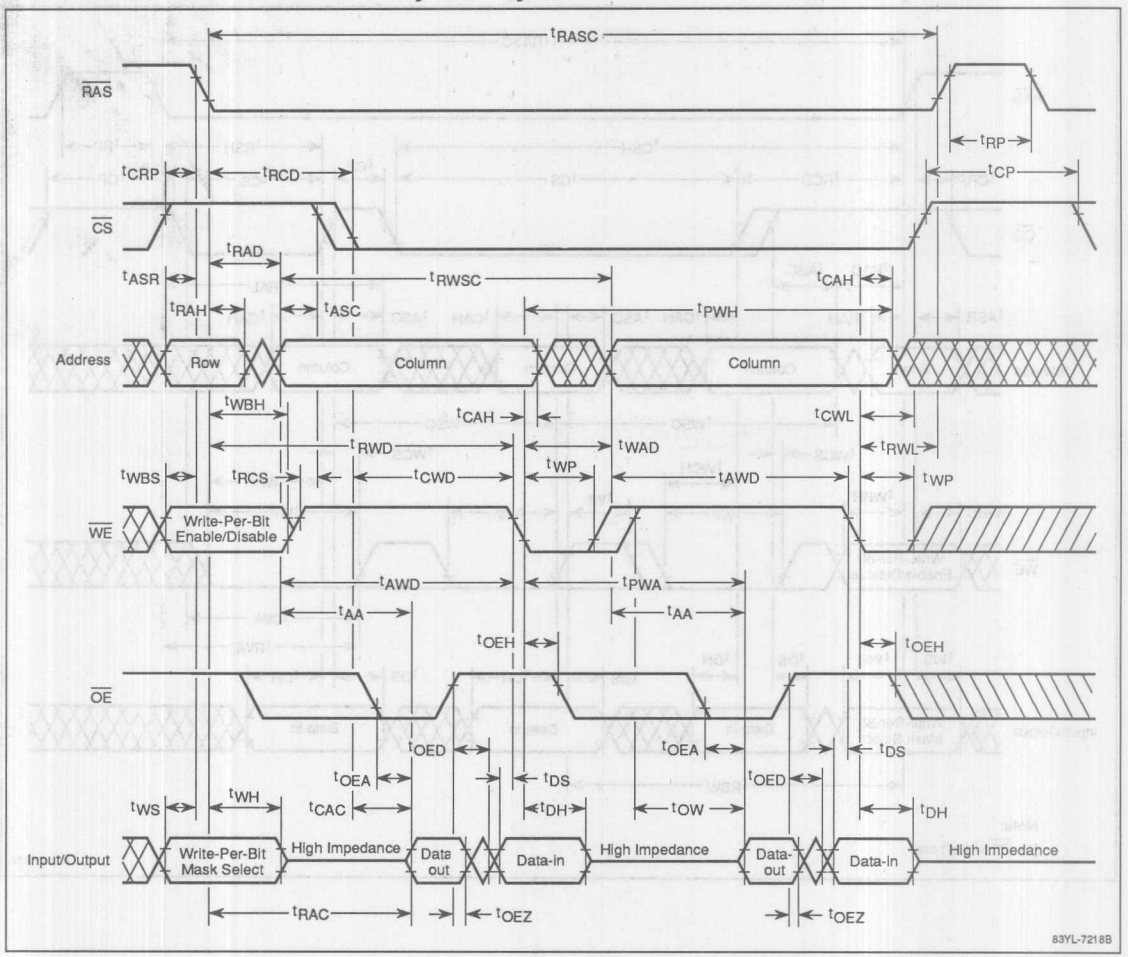
Note:
[1] $\overline{OE}$ = don't care.

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Timing Waveforms (cont)

Static-Column Read-Write/Read-Modify-Write Cycle



μPD424100
4,194,304 x 1-Bit
Dynamic CMOS RAM

Description

The μPD424100 is a fast-page dynamic RAM organized as 4,194,304 words by 1 bit and designed to operate from a single + 5-volt power supply. Advanced polycide technology using trench capacitors minimizes silicon area and provides high storage cell capacity, high performance, and high reliability. A single-transistor dynamic storage cell and advanced CMOS circuitry throughout ensure minimum power dissipation, while an on-chip circuit internally generates the negative-voltage substrate bias—automatically and transparently.

The three-state output is controlled by $\overline{CAS}$ independent of $\overline{RAS}$. After a valid read or read-modify-write cycle, data is held on the output by holding $\overline{CAS}$ low. The data output is returned to high impedance by returning $\overline{CAS}$ high. Fast-page read and write cycles can be executed by cycling $\overline{CAS}$.

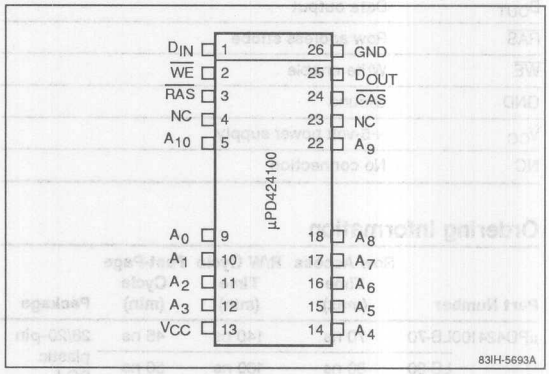
Refreshing may be accomplished by means of a $\overline{CAS}$ before $\overline{RAS}$ cycle that internally generates the refresh address. Refreshing can also be accomplished by means of $\overline{RAS}$-only refresh cycles or by normal read or write cycles on the 1024 address combinations of A_0 through A_9 during a 16-ms refresh period.

Features

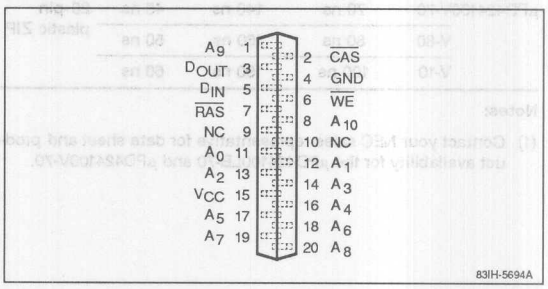
- 4,194,304-word by 1-bit organization
- Single + 5-volt ±10% power supply
- Fast-page option
- Low power dissipation
- $\overline{CAS}$ before $\overline{RAS}$ refresh cycles
- Multiplexed address inputs
- On-chip substrate bias generator
- Nonlatched, three-state outputs
- Low input capacitance
- TTL-compatible inputs and outputs
- 1024 refresh cycles every 16 ms
- 26/20-pin SOJ or 20-pin plastic ZIP packaging

Pin Configurations

26/20-Pin Plastic SOJ



20-Pin Plastic ZIP



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New speeds (60 and 70 ns) and packages (TSOP and 300-mil SOJ) will be available in 1991.

Pin Identification

Name	Function
A_0 - A_{10}	Address inputs
$\overline{CAS}$	Column address strobe
D_{IN}	Data input
D_{OUT}	Data output
$\overline{RAS}$	Row address strobe
$\overline{WE}$	Write enable
GND	Ground
V_{CC}	+5-volt power supply
NC	No connection

Ordering Information

Part Number		Row Access Time (max)	R/W Cycle Time (min)	Fast-Page Cycle (min)	Package
μPD424100	LB-70	70 ns	140 ns	45 ns	26/20-pin plastic SOJ
	LB-80	80 ns	160 ns	50 ns	
	LB-10	100 ns	190 ns	60 ns	
μPD424100	V-70	70 ns	140 ns	45 ns	20-pin plastic ZIP
	V-80	80 ns	160 ns	50 ns	
	V-10	100 ns	190 ns	60 ns	

Notes:

(1) Contact your NEC sales representative for data sheet and product availability for the μPD424100LB-70 and μPD424100V-70.

Absolute Maximum Ratings

Voltage on any pin relative to GND	−1.0 to +7.0 V
Operating temperature, T_{OPR}	0 to +70°C
Storage temperature, T_{STG}	−55 to +125°C
Short-circuit output current, I_{OS}	50 mA
Power dissipation, P_D	1.0 W

Exposure to Absolute Maximum Ratings for extended periods may affect device reliability; exceeding the ratings could cause permanent damage. The device should be operated within the limits specified under DC and AC Characteristics.

Recommended Operating Conditions

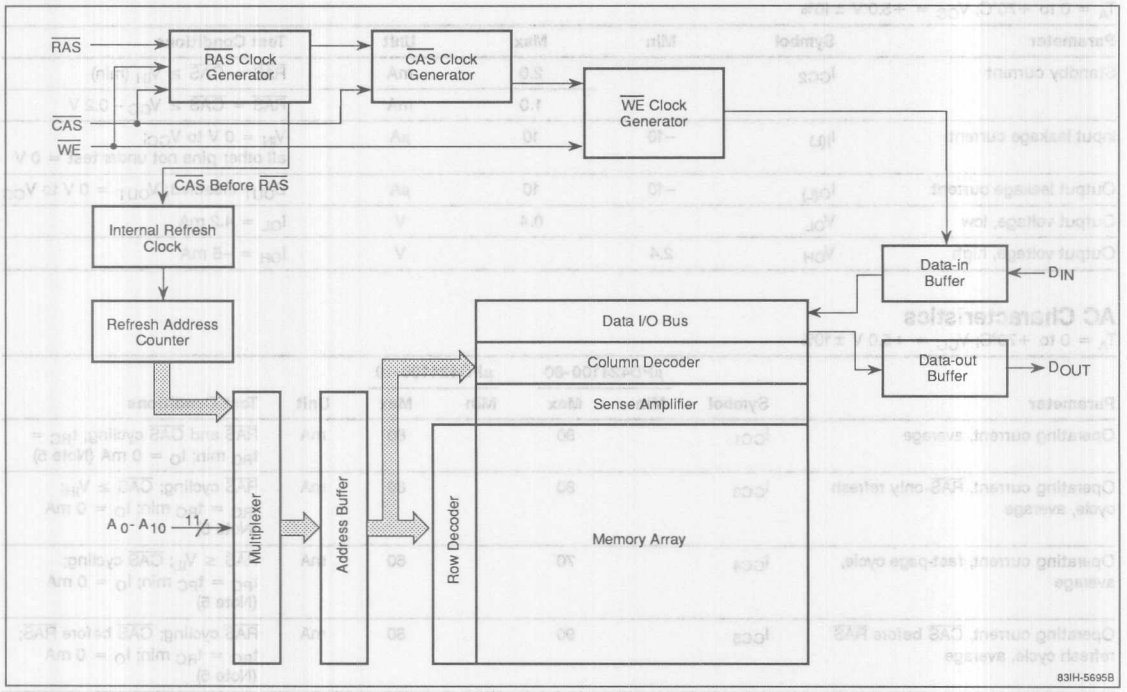
Parameter	Symbol	Min	Typ	Max	Unit
Input voltage, high	V_{IH}	2.4		V_{CC} + 1.0	V
Input voltage, low	V_{IL}	−1.0		0.8	V
Supply voltage	V_{CC}	4.5	5.0	5.5	V
Ambient temperature	T_A	0		70	°C

Capacitance

T_A = 25°C; f = 1 MHz

Parameter	Symbol	Max	Unit	Pins Under Test
Input capacitance	C_{I1}	5	pF	Address, D_{IN}
	C_{I2}	7	pF	$\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$
Output capacitance	C_O	7	pF	D_{OUT}

Block Diagram



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DC Characteristics

T_A = 0 to +70°C; V_{CC} = +5.0 V ±10%

Parameter	Symbol	Min	Max	Unit	Test Conditions
Standby current	I_{CC2}		2.0	mA	$\overline{RAS}$ = $\overline{CAS}$ ≥ V_{IH} (min)
			1.0	mA	$\overline{RAS}$ = $\overline{CAS}$ ≥ V_{CC} – 0.2 V
Input leakage current	$I_{I(L)}$	–10	10	μA	V_{IN} = 0 V to V_{CC}; all other pins not under test = 0 V
Output leakage current	$I_{O(L)}$	–10	10	μA	D_{OUT} disabled; V_{OUT} = 0 V to V_{CC}
Output voltage, low	V_{OL}		0.4	V	I_{OL} = 4.2 mA
Output voltage, high	V_{OH}	2.4		V	I_{OH} = –5 mA

AC Characteristics

T_A = 0 to +70°C; V_{CC} = +5.0 V ±10%

		μPD424100-80		μPD424100-10			
Parameter	Symbol	Min	Max	Min	Max	Unit	Test Conditions
Operating current, average	I_{CC1}		90		80	mA	$\overline{RAS}$ and $\overline{CAS}$ cycling; t_{RC} = t_{RC} min; I_O = 0 mA (Note 5)
Operating current, $\overline{RAS}$-only refresh cycle, average	I_{CC3}		90		80	mA	$\overline{RAS}$ cycling; $\overline{CAS}$ ≥ V_{IH}; t_{RC} = t_{RC} min; I_O = 0 mA (Note 5)
Operating current, fast-page cycle, average	I_{CC4}		70		60	mA	$\overline{RAS}$ ≤ V_{IL}; $\overline{CAS}$ cycling; t_{PC} = t_{PC} min; I_O = 0 mA (Note 5)
Operating current, $\overline{CAS}$ before $\overline{RAS}$ refresh cycle, average	I_{CC5}		90		80	mA	$\overline{RAS}$ cycling; $\overline{CAS}$ before $\overline{RAS}$; t_{RC} = t_{RC} min; I_O = 0 mA (Note 5)
Access time from column address	t_{AA}		40		50	ns	(Notes 7, 9)
Access time from $\overline{CAS}$ precharge (rising edge)	t_{ACP}		45		55	ns	(Notes 7, 9)
Column address setup time	t_{ASC}	0		0		ns	
Row address setup time	t_{ASR}	0		0		ns	
Column address to $\overline{WE}$ delay time	t_{AWD}	40		50		ns	(Note 16)
Access time from $\overline{CAS}$ (falling edge)	t_{CAC}		20		25	ns	(Notes 7, 9)
Column address hold time	t_{CAH}	15		20		ns	
$\overline{CAS}$ pulse width	t_{CAS}	20	10,000	25	10,000	ns	
$\overline{CAS}$ hold time for $\overline{CAS}$ before $\overline{RAS}$ refresh cycle	t_{CHR}	15		20		ns	
$\overline{CAS}$ to output in low impedance	t_{CLZ}	0		0		ns	(Note 7)
$\overline{CAS}$ precharge time, fast-page cycle	t_{CP}	10		10		ns	
$\overline{CAS}$ precharge time, nonpage cycle	t_{CPN}	10		10		ns	
$\overline{CAS}$ to $\overline{RAS}$ precharge time	t_{CRP}	10		10		ns	(Note 12)
$\overline{CAS}$ hold time	t_{CSH}	80		100		ns	
$\overline{CAS}$ setup time for $\overline{CAS}$ before $\overline{RAS}$ refresh cycle	t_{CSR}	10		10		ns	
$\overline{CAS}$ to $\overline{WE}$ delay	t_{CWD}	20		25		ns	(Note 16)
Write command to $\overline{CAS}$ lead time	t_{CWL}	15		20		ns	
Data-in hold time	t_{DH}	15		20		ns	(Note 15)

AC Characteristics (cont)

Parameter	Symbol	μPD424100-80 Min	μPD424100-80 Max	μPD424100-10 Min	μPD424100-10 Max	Unit	Test Conditions
Data-in setup time	t_{DS}	0		0		ns	(Note 15)
Output buffer turnoff delay	t_{OFF}	0	20	0	25	ns	(Note 10)
Fast-page cycle time	t_{PC}	50		60		ns	(Note 6)
Fast-page read-modify-write cycle time	t_{PRWC}	80		95		ns	(Note 6)
Access time from $\overline{RAS}$	t_{RAC}		80		100	ns	(Notes 7, 8)
$\overline{RAS}$ to column address delay time	t_{RAD}	17	40	17	50	ns	(Note 9)
Row address hold time	t_{RAH}	12		12		ns	
Column address lead time referenced to $\overline{RAS}$ (rising edge)	t_{RAL}	40		50		ns	
$\overline{RAS}$ pulse width	t_{RAS}	80	10,000	100	10,000	ns	
$\overline{RAS}$ pulse width, fast-page cycle	t_{RASP}	80	125,000	100	125,000	ns	
Random read or write cycle time	t_{RC}	160		190		ns	(Note 6)
$\overline{RAS}$ to $\overline{CAS}$ delay time	t_{RCD}	25	60	25	75	ns	(Note 11)
Read command hold time referenced to $\overline{CAS}$	t_{RCH}	0		0		ns	(Note 13)
Read command setup time	t_{RCS}	0		0		ns	
Refresh period	t_{REF}		16		16	ms	Addresses A_0 - A_9
$\overline{RAS}$ precharge time	t_{RP}	70		80		ns	
$\overline{RAS}$ precharge $\overline{CAS}$ hold time	t_{RPC}	10		10		ns	
Read command hold time referenced to $\overline{RAS}$	t_{RRH}	10		10		ns	(Note 13)
$\overline{RAS}$ hold time	t_{RSH}	20		25		ns	
Read-write cycle time	t_{RWC}	185		220		ns	(Note 6)
$\overline{RAS}$ to $\overline{WE}$ delay	t_{RWD}	80		100		ns	(Note 16)
Write command to $\overline{RAS}$ lead time	t_{RWL}	20		25		ns	
Rise and fall transition time	t_T	3	50	3	50	ns	(Note 3)
Write command hold time	t_{WCH}	15		20		ns	
Write command setup time	t_{WCS}	0		0		ns	(Note 16)
$\overline{WE}$ hold time	t_{WHR}	15		20		ns	
Write command pulse width	t_{WP}	15		20		ns	(Note 14)
$\overline{WE}$ setup time	t_{WSR}	10		10		ns	

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Notes:

(1) All voltages are referenced to GND.

(2) An initial pause of 100 μs is required after power-up, followed by any eight $\overline{RAS}$ cycles, before proper device operation is achieved. At the end of the initial power-up sequence, it is recommended that either a $\overline{RAS}$-only refresh or a $\overline{CAS}$ before $\overline{RAS}$ refresh cycle be executed while $\overline{WE} \geq V_{IH}$ to ensure normal operation.

(3) AC measurements assume $t_T = 5$ ns.

(4) V_{IH} (min) and V_{IL} (max) are reference levels for measuring the timing of input signals. Transition times are measured between V_{IH} and V_{IL}.

(5) I_{CC1}, I_{CC3}, I_{CC4}, and I_{CC5} depend on output loading and cycle rates. Specified values are obtained with the output open. I_{CC3} is measured assuming that all column address inputs are held at either a high level or a low level during $\overline{RAS}$-only refresh cycles. I_{CC4} is measured assuming that all column address inputs are switched only once during each fast-page cycle.

(6) The minimum specifications are used only to indicate the cycle time at which proper operation over the full temperature range (T_A = 0 to +70°C) is assured.

(7) Load = 2 TTL (–1 mA, +4 mA) loads and 100 pF (V_{OH} = 2.0 V, V_{OL} = 0.8 V).

(8) Assumes that $t_{RCD} \leq t_{RCD}$ (max) and $t_{RAD} \leq t_{RAD}$ (max). If t_{RCD} or t_{RAD} is greater than the maximum recommended value in this table, t_{RAC} increases by the amount that t_{RCD} or t_{RAD} exceeds the value shown.

(9) If $t_{RAD} \geq t_{RAD}$ (max), then the access time is defined by t_{AA}.

(10) t_{OFF} (max) defines the time at which the output achieves the open-circuit condition an is not referenced to V_{OH} or V_{OL}.

(11) Operation within the t_{RCD} (max) limit assures that t_{RAC} (max) can be met. t_{RCD} (max) is specified as a reference point only; if t_{RCD} is greater than t_{RCD} (max), then access time is controlled exclusively by t_{CAC}.

(12) The t_{CRP} requirement should be applicable for $\overline{RAS}$/$\overline{CAS}$ cycles preceded by any cycle.

(13) Either t_{RRH} or t_{RCH} must be satisfied for a read cycle.

(14) Parameter t_{WP} is applicable for a delayed write cycle such as a read-write/read-modify-write cycle. For early write operation, both t_{WCS} and t_{WCH} must be met.

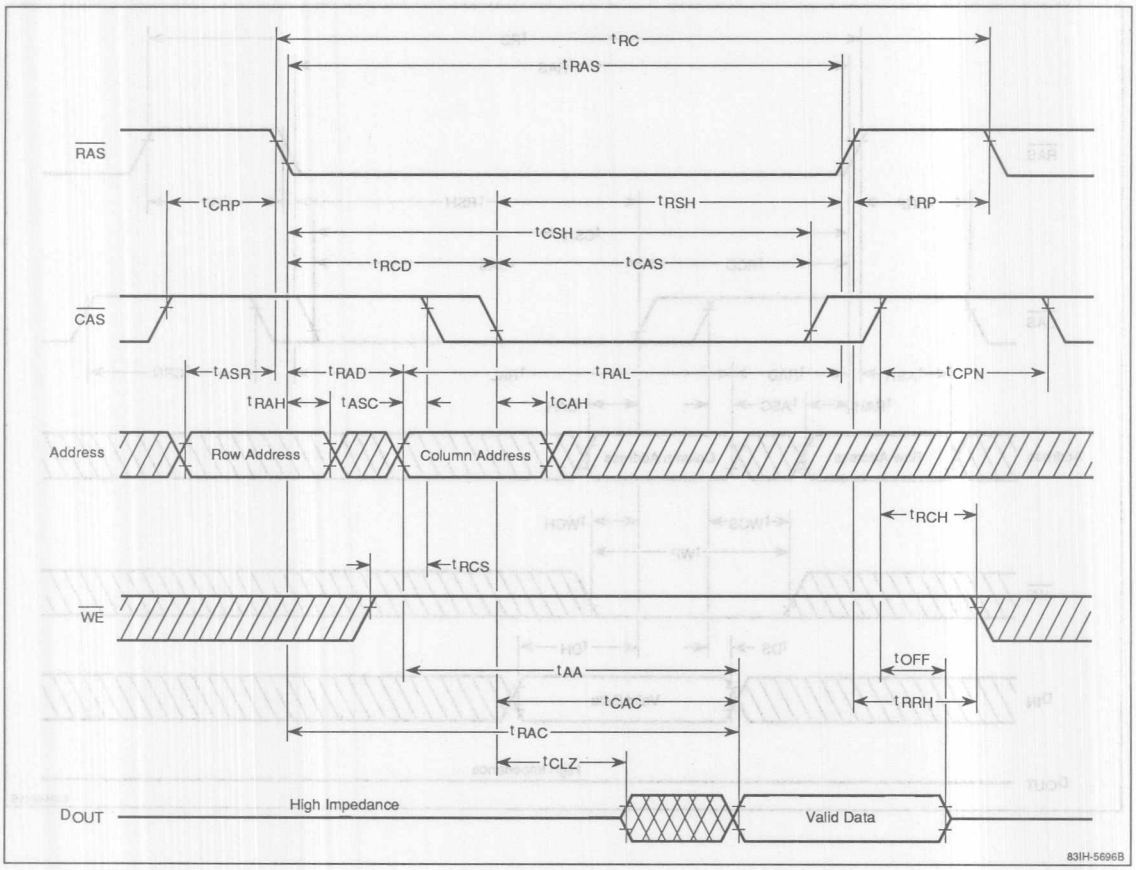
(15) These parameters are referenced to the falling edge of $\overline{CAS}$ for early write cycles and to the falling edge of $\overline{WE}$ for delayed write or read-modify-write cycles.

(16) t_{WCS}, t_{RWD}, t_{CWD}, and t_{AWD} are restrictive operating parameters in read-write/read-modify-write cycles only. If $t_{WCS} \geq t_{WCS}$ (min), the cycle is an early write cycle and the data output will remain open-circuit throughout the entire cycle. If $t_{CWD} \geq t_{CWD}$ (min), $t_{RWD} \geq t_{RWD}$ (min), and $t_{AWD} \geq t_{AWD}$ (min), the cycle is a read-write cycle and the data output will contain data read from the selected cell. If neither of the above conditions is met, the condition of the data output pin (at access time and until $\overline{CAS}$ returns to V_{IH}) is indeterminate.

(17) A test mode may be initiated by executing a $\overline{CAS}$ before $\overline{RAS}$ refresh cycle with $\overline{WE}$ held at V_{IL}. This mode also may inadvertently be initiated during power-up because external control of the signal lines is very difficult during this period. It is therefore recommended that while $\overline{WE}$ is held at V_{IH}, either a $\overline{RAS}$-only or $\overline{CAS}$ before $\overline{RAS}$ refresh cycle should be executed at any time after the end of the initial power-up sequence to ensure normal device operation.

Timing Waveforms

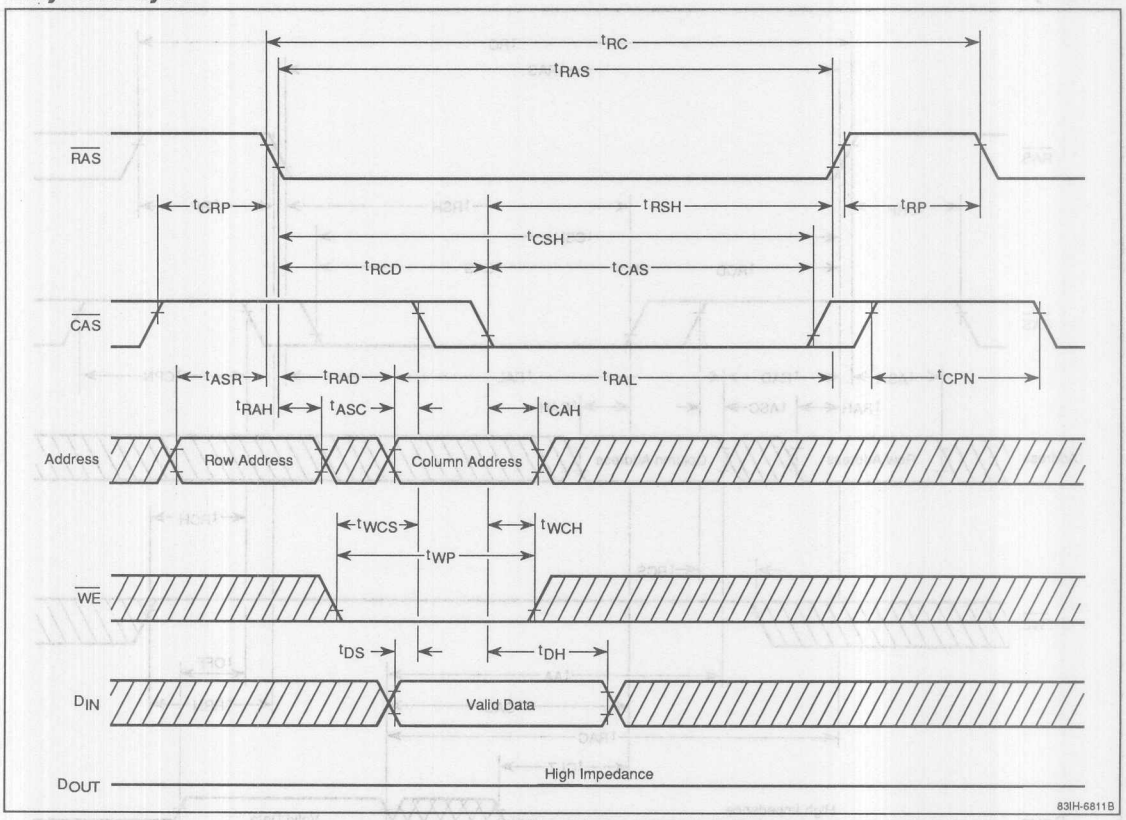
Read Cycle



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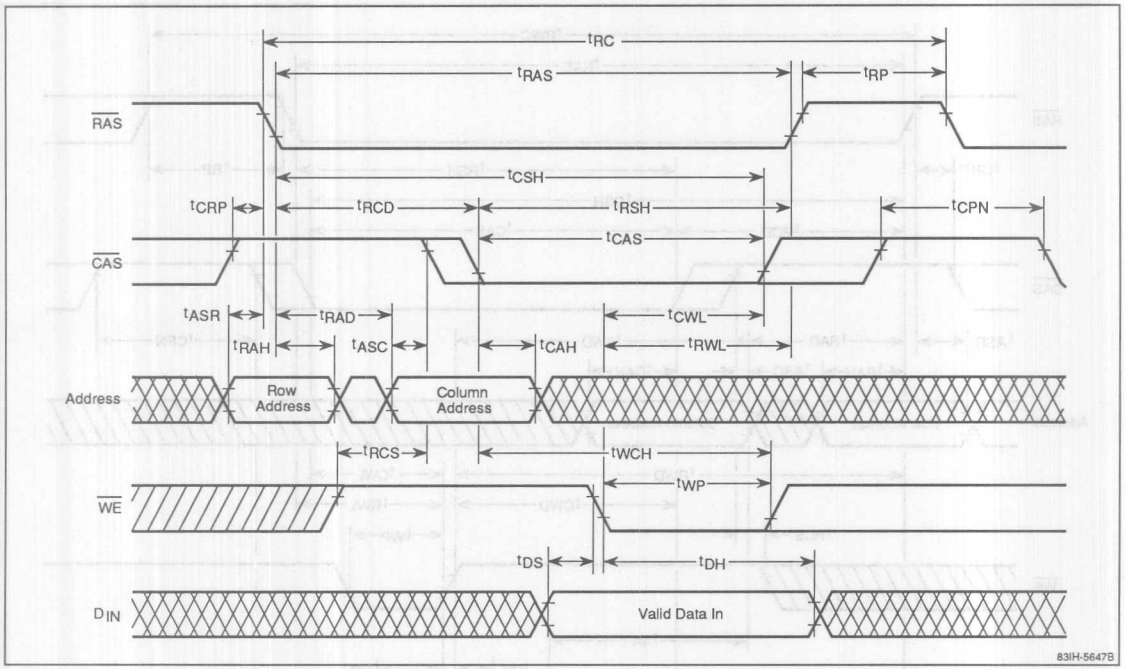
Timing Waveforms (cont)

Early Write Cycle



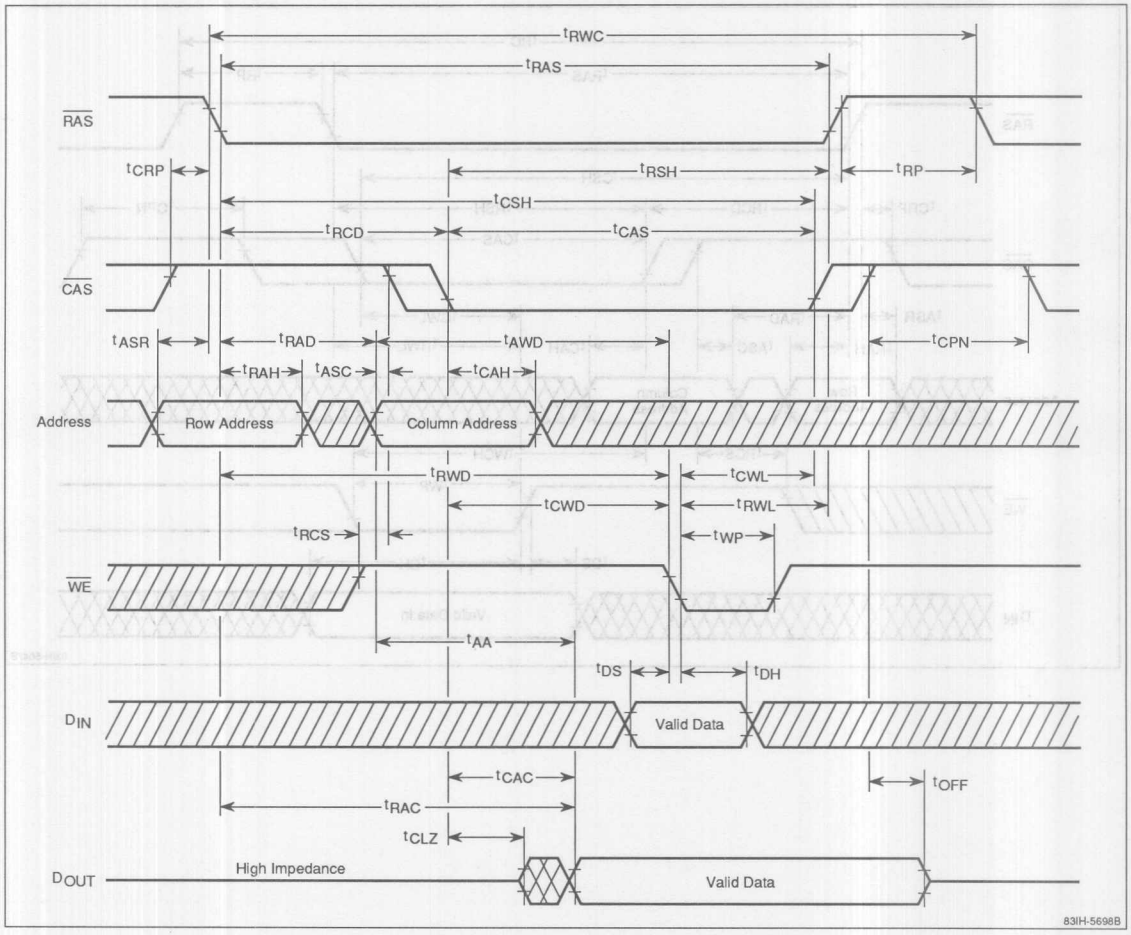
Timing Waveforms (cont)

Late Write Cycle



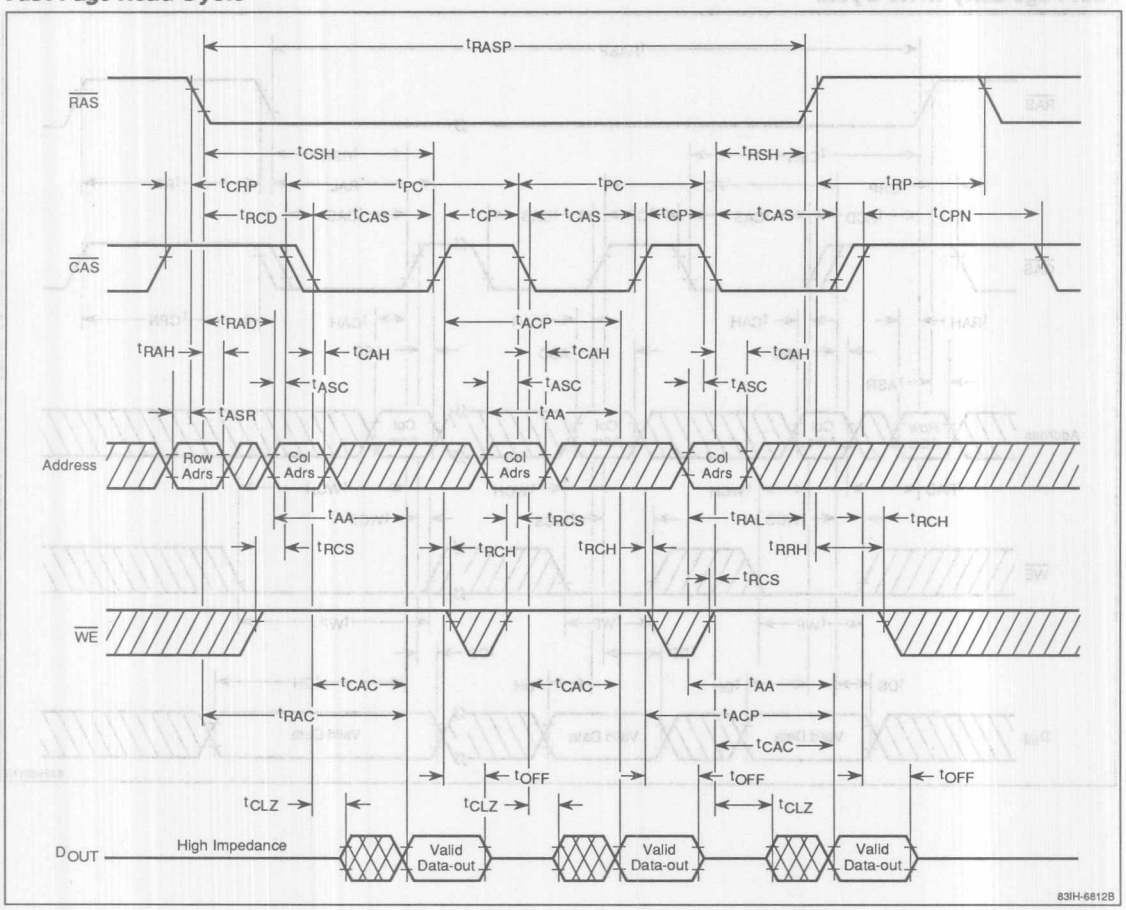
Timing Waveforms (cont)

Read-Write/Read-Modify-Write Cycle



Timing Waveforms (cont)

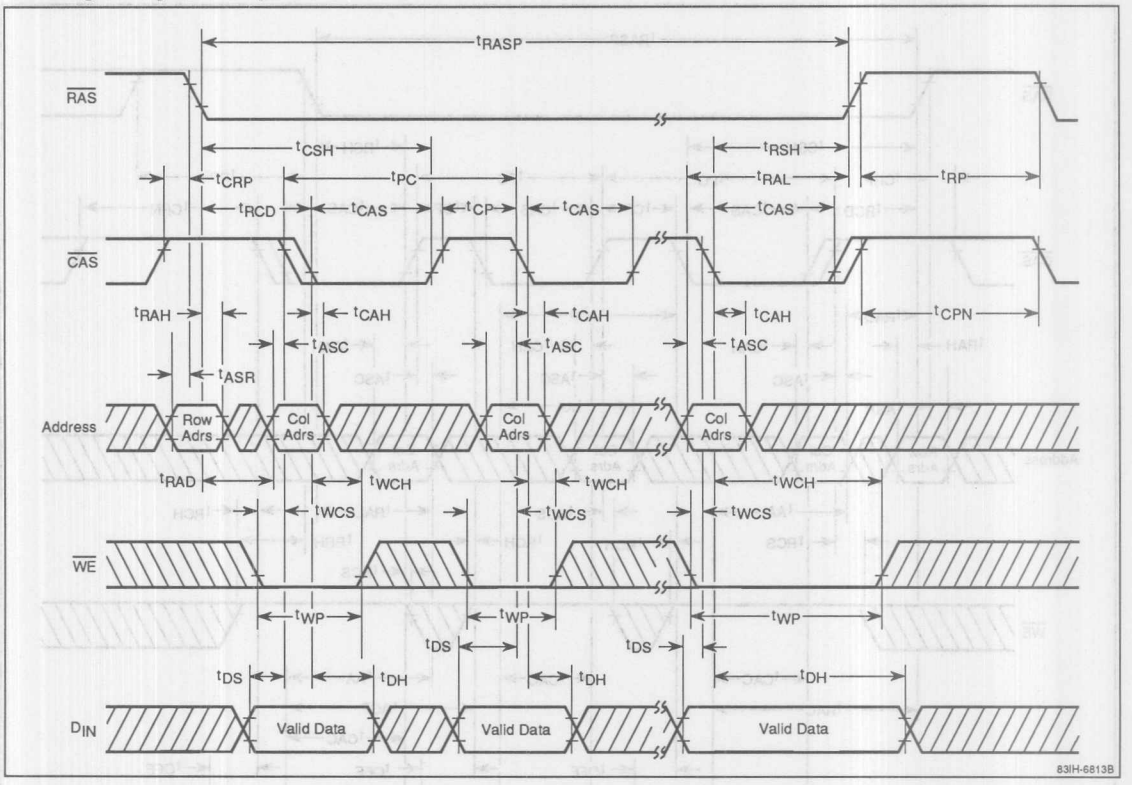
Fast-Page Read Cycle



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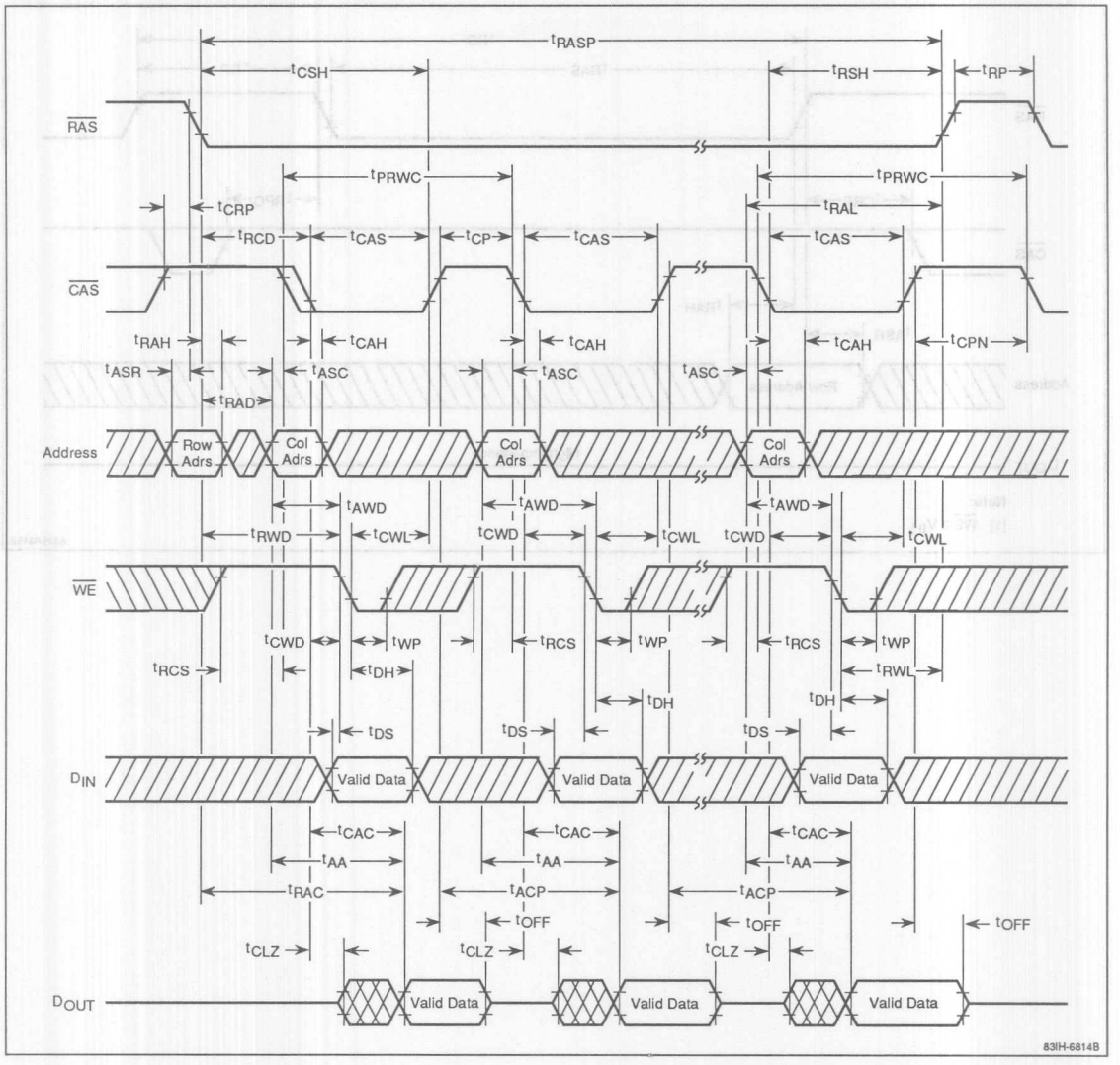
Timing Waveforms (cont)

Fast-Page Early Write Cycle



Timing Waveforms (cont)

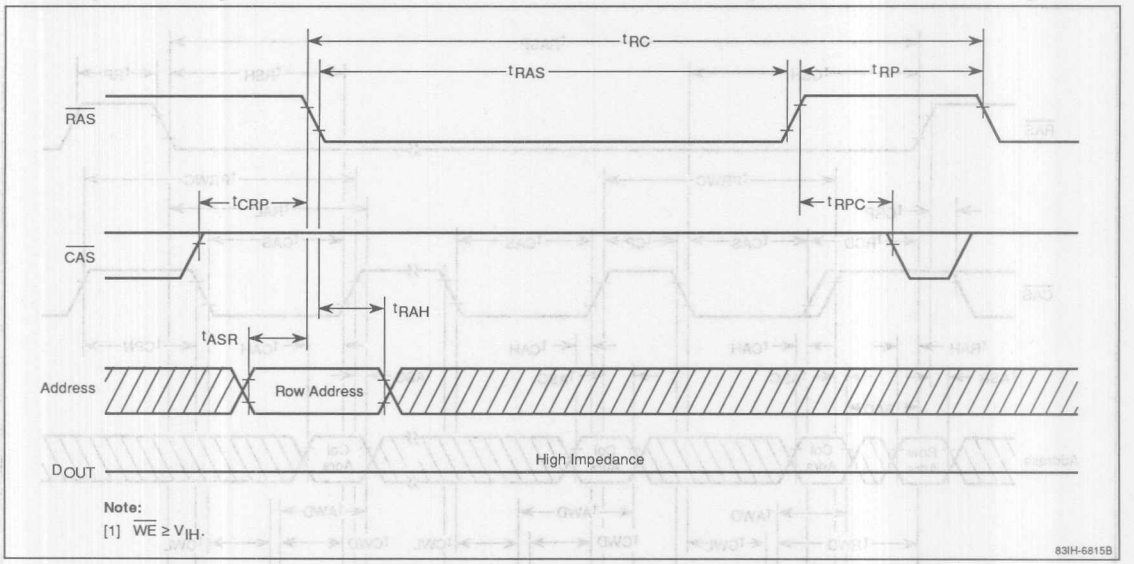
Fast-Page Read-Write/Read-Modify-Write Cycle



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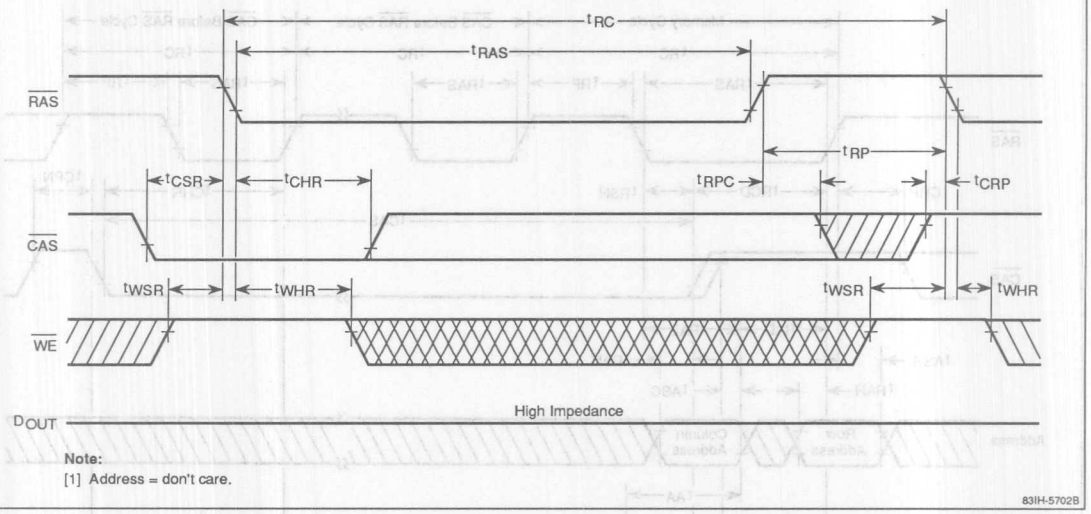
Timing Waveforms (cont)

$\overline{\text{RAS}}$-Only Refresh Cycle



Timing Waveforms (cont)

$\overline{CAS}$ Before $\overline{RAS}$ Refresh Cycle

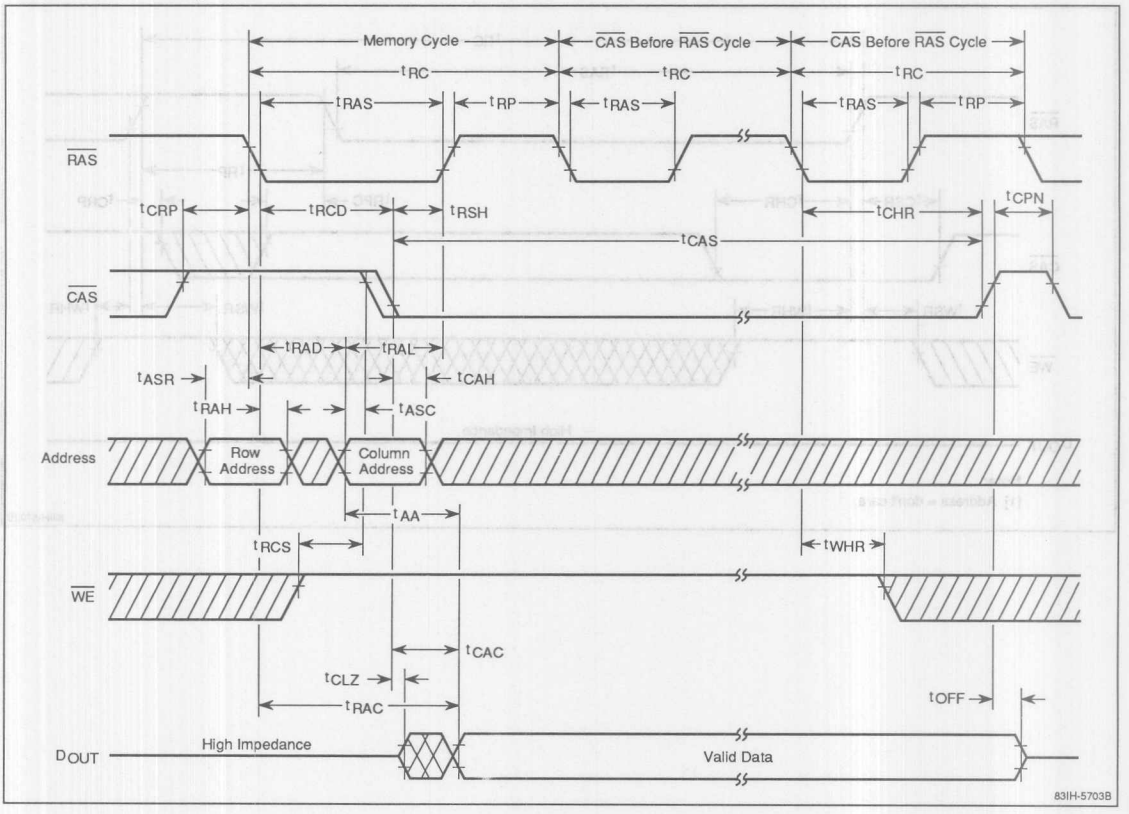


Note:
[1] Address = don't care.

83IH-5702B

Timing Waveforms (cont)

Hidden Refresh Cycle



μPD424101
4,194,304 x 1-Bit
Dynamic CMOS RAM

Description

The μPD424101 is a nibble mode dynamic RAM organized as 4,194,304 words by 1 bit and designed to operate from a single + 5-volt power supply. Advanced polycide technology using trench capacitors minimizes silicon area and provides high storage cell capacity, high performance, and high reliability. A single-transistor dynamic storage cell and advanced CMOS circuitry throughout ensure minimum power dissipation, while an on-chip circuit internally generates the negative-voltage substrate bias—automatically and transparently.

The three-state output is controlled by $\overline{CAS}$ independent of $\overline{RAS}$. After a valid read or read-modify-write cycle, data is held on the output by holding $\overline{CAS}$ low. The data output is returned to high impedance by returning $\overline{CAS}$ high. Nibble mode read and write cycles can be executed by cycling $\overline{CAS}$.

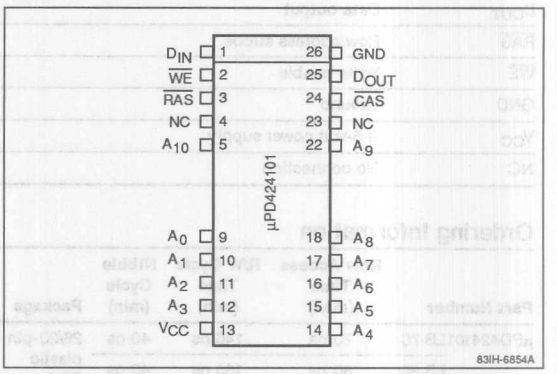
Refreshing may be accomplished by means of a $\overline{CAS}$ before $\overline{RAS}$ cycle that internally generates the refresh address. Refreshing can also be accomplished by means of $\overline{RAS}$-only refresh cycles or by normal read or write cycles on the 1024 address combinations of A_0 through A_9 during a 16-ms refresh period.

Features

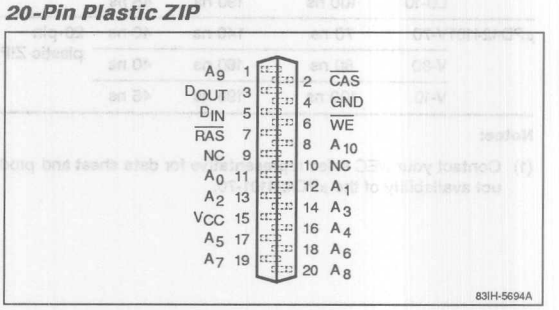
- 4,194,304-word by 1-bit organization
- Single + 5-volt ±10% power supply
- Nibble mode option
- Low power dissipation
- $\overline{CAS}$ before $\overline{RAS}$ refresh cycles
- Multiplexed address inputs
- On-chip substrate bias generator
- Nonlatched, three-state outputs
- Low input capacitance
- TTL-compatible inputs and outputs
- 1024 refresh cycles every 16 ms
- 26/20-pin SOJ or 20-pin plastic ZIP packaging

Pin Configurations

26/20-Pin Plastic SOJ



20-Pin Plastic ZIP



6

New speeds (60 and 70 ns) and packages (TSOP and 300-mil SOJ) will be available in 1991.

Pin Identification

Name	Function
A_0 - A_{10}	Address inputs
$\overline{CAS}$	Column address strobe
D_{IN}	Data input
D_{OUT}	Data output
$\overline{RAS}$	Row address strobe
$\overline{WE}$	Write enable
GND	Ground
V_{CC}	+5-volt power supply
NC	No connection

Ordering Information

Part Number		Row Access Time (max)	R/W Cycle Time (min)	Nibble Cycle (min)	Package
μPD424101	LB-70	70 ns	140 ns	40 ns	26/20-pin plastic SOJ
	LB-80	80 ns	160 ns	40 ns	
	LB-10	100 ns	190 ns	45 ns	
μPD424101	V-70	70 ns	140 ns	40 ns	20-pin plastic ZIP
	V-80	80 ns	160 ns	40 ns	
	V-10	100 ns	190 ns	45 ns	

Notes:

(1) Contact your NEC sales representative for data sheet and product availability of the μPD424101-70.

Absolute Maximum Ratings

Voltage on any pin relative to GND, V_T	−1.0 to +7.0 V
Operating temperature, T_{OPR}	0 to +70°C
Storage temperature, T_{STG}	−55 to +125°C
Short-circuit output current, I_{OS}	50 mA
Power dissipation, P_D	1.0 W

Exposure to Absolute Maximum Ratings for extended periods may affect device reliability; exceeding the ratings could cause permanent damage. The device should be operated within the limits specified under DC and AC Characteristics.

Recommended Operating Conditions

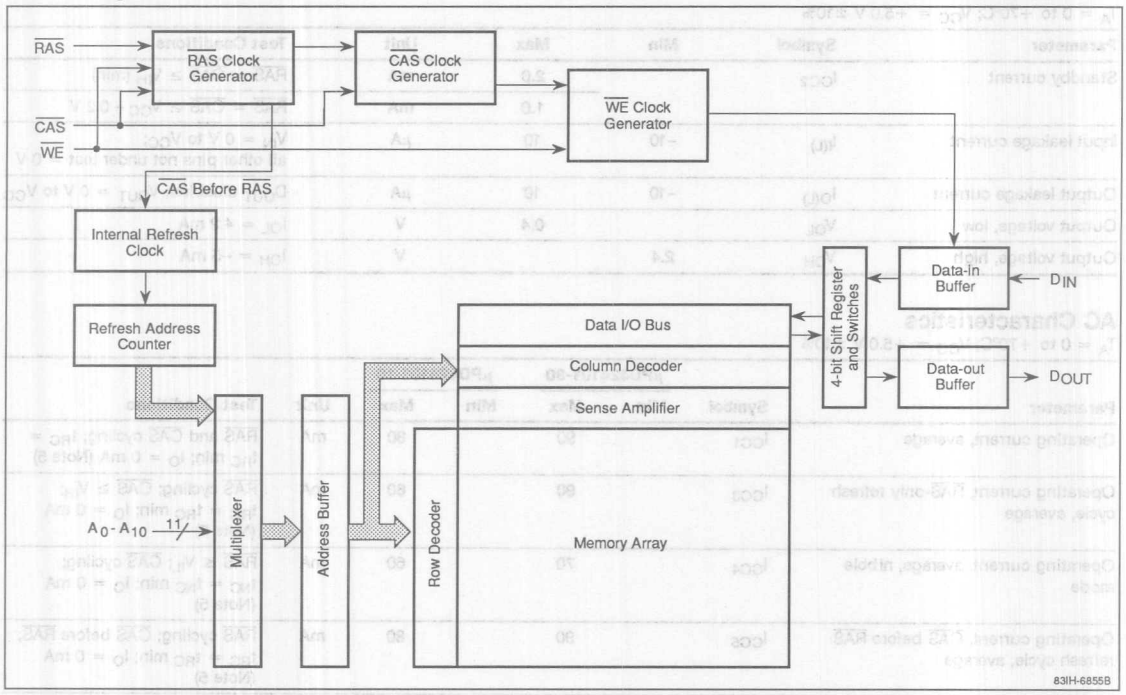
Parameter	Symbol	Min	Typ	Max	Unit
Input voltage, high	V_{IH}	2.4		V_{CC} + 1.0	V
Input voltage, low	V_{IL}	−1.0		0.8	V
Supply voltage	V_{CC}	4.5	5.0	5.5	V
Ambient temperature	T_A	0		70	°C

Capacitance

T_A = 25°C; f = 1 MHz

Parameter	Symbol	Max	Unit	Pins Under Test
Input capacitance	C_{I1}	5	pF	Address, D_{IN}
	C_{I2}	7	pF	$\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$
Output capacitance	C_O	7	pF	D_{OUT}

Block Diagram



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DC Characteristics

T_A = 0 to +70°C; V_{CC} = +5.0 V ±10%

Parameter	Symbol	Min	Max	Unit	Test Conditions
Standby current	I_{CC2}		2.0	mA	$\overline{RAS}$ = $\overline{CAS}$ ≥ V_{IH} (min)
			1.0	mA	$\overline{RAS}$ = $\overline{CAS}$ ≥ V_{CC} – 0.2 V
Input leakage current	$I_{I(L)}$	–10	10	μA	V_{IN} = 0 V to V_{CC}; all other pins not under test = 0 V
Output leakage current	$I_{O(L)}$	–10	10	μA	D_{OUT} disabled; V_{OUT} = 0 V to V_{CC}
Output voltage, low	V_{OL}		0.4	V	I_{OL} = 4.2 mA
Output voltage, high	V_{OH}	2.4		V	I_{OH} = –5 mA

AC Characteristics

T_A = 0 to +70°C; V_{CC} = +5.0 V ±10%

		μPD424101-80		μPD424101-10			
Parameter	Symbol	Min	Max	Min	Max	Unit	Test Conditions
Operating current, average	I_{CC1}		90		80	mA	$\overline{RAS}$ and $\overline{CAS}$ cycling; t_{RC} = t_{RC} min; I_O = 0 mA (Note 5)
Operating current, $\overline{RAS}$-only refresh cycle, average	I_{CC3}		90		80	mA	$\overline{RAS}$ cycling; $\overline{CAS}$ ≥ V_{IH}; t_{RC} = t_{RC} min; I_O = 0 mA (Note 5)
Operating current, average, nibble mode	I_{CC4}		70		60	mA	$\overline{RAS}$ ≤ V_{IL}; $\overline{CAS}$ cycling; t_{NC} = t_{NC} min; I_O = 0 mA (Note 5)
Operating current, $\overline{CAS}$ before $\overline{RAS}$ refresh cycle, average	I_{CC5}		90		80	mA	$\overline{RAS}$ cycling; $\overline{CAS}$ before $\overline{RAS}$; t_{RC} = t_{RC} min; I_O = 0 mA (Note 5)
Access time from column address	t_{AA}		40		50	ns	(Notes 7, 9)
Column address setup time	t_{ASC}	0		0		ns	
Row address setup time	t_{ASR}	0		0		ns	
Column address to $\overline{WE}$ delay time	t_{AWD}	40		50		ns	(Note 16)
Access time from $\overline{CAS}$ (falling edge)	t_{CAC}		20		25	ns	(Notes 7, 9)
Column address hold time	t_{CAH}	15		20		ns	
$\overline{CAS}$ pulse width	t_{CAS}	20	10,000	25	10,000	ns	
$\overline{CAS}$ hold time for $\overline{CAS}$ before $\overline{RAS}$ refresh cycle	t_{CHR}	15		20		ns	
$\overline{CAS}$ precharge time, non-nibble cycle	t_{CPN}	10		10		ns	
$\overline{CAS}$ to $\overline{RAS}$ precharge time	t_{CRP}	10		10		ns	(Note 12)
$\overline{CAS}$ hold time	t_{CSH}	80		100		ns	
$\overline{CAS}$ setup time for $\overline{CAS}$ before $\overline{RAS}$ refresh cycle	t_{CSR}	10		10		ns	
$\overline{CAS}$ to $\overline{WE}$ delay	t_{CWD}	20		25		ns	(Note 16)
Write command to $\overline{CAS}$ lead time	t_{CWL}	15		20		ns	
Data-in hold time	t_{DH}	15		20		ns	(Note 15)
Data-in setup time	t_{DS}	0		0		ns	(Note 15)
Nibble mode access time	t_{NAC}		20		25	ns	
$\overline{CAS}$ pulse width in nibble mode	t_{NAS}	20		25		ns	
Nibble mode cycle time	t_{NC}	40		45		ns	

AC Characteristics (cont)

Parameter	Symbol	μPD424101-80 Min	μPD424101-80 Max	μPD424101-10 Min	μPD424101-10 Max	Unit	Test Conditions
$\overline{CAS}$ to $\overline{WE}$ delay in nibble mode	t_{NCWD}	20		25		ns	
Write command to $\overline{CAS}$ lead time in nibble mode	t_{NCWL}	20		25		ns	
$\overline{CAS}$ precharge time in nibble mode	t_{NP}	10		10		ns	
$\overline{RAS}$ hold time for nibble read cycle	t_{NRRSH}	20		25		ns	
$\overline{RAS}$ hold time for nibble write cycle	t_{NWRSH}	20		25		ns	
Output buffer turnoff delay	t_{OFF}	0	20	0	25	ns	(Note 10)
Access time from $\overline{RAS}$	t_{RAC}		80		100	ns	(Notes 7, 8)
$\overline{RAS}$ to column address delay time	t_{RAD}	17	40	17	50	ns	(Note 9)
Row address hold time	t_{RAH}	12		12		ns	
Column address lead time referenced to $\overline{RAS}$ (rising edge)	t_{RAL}	40		50		ns	
$\overline{RAS}$ pulse width	t_{RAS}	80	10,000	100	10,000	ns	
$\overline{RAS}$ pulse width in nibble mode	t_{RASP}	80	125,000	100	125,000	ns	
Random read or write cycle time	t_{RC}	160		190		ns	(Note 6)
$\overline{RAS}$ to $\overline{CAS}$ delay time	t_{RCD}	25	60	25	75	ns	(Note 11)
Read command hold time referenced to $\overline{CAS}$	t_{RCH}	0		0		ns	(Note 13)
Read command setup time	t_{RCS}	0		0		ns	
Refresh period	t_{REF}		16		16	ms	Addresses A_0 - A_9
$\overline{RAS}$ precharge time	t_{RP}	70		80		ns	
$\overline{RAS}$ precharge $\overline{CAS}$ hold time	t_{RPC}	10		10		ns	
Read command hold time referenced to $\overline{RAS}$	t_{RRH}	10		10		ns	(Note 13)
$\overline{RAS}$ hold time	t_{RSH}	20		25		ns	
Read-write cycle time	t_{RWC}	185		220		ns	(Note 6)
$\overline{RAS}$ to $\overline{WE}$ delay	t_{RWD}	80		100		ns	(Note 16)
Write command to $\overline{RAS}$ lead time	t_{RWL}	20		25		ns	
Rise and fall transition time	t_T	3	50	3	50	ns	(Note 3)
Write command hold time	t_{WCH}	15		20		ns	
Write command setup time	t_{WCS}	0		0		ns	(Note 16)
$\overline{WE}$ hold time	t_{WHR}	15		20		ns	
Write command pulse width	t_{WP}	15		20		ns	(Note 14)
$\overline{WE}$ setup time	t_{WSR}	10		10		ns	

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Notes:

(1) All voltages are referenced to GND.

(2) An initial pause of 100 μs is required after power-up, followed by any eight $\overline{RAS}$ cycles, before proper device operation is achieved. At the end of the initial power-up sequence, it is recommended that either a $\overline{RAS}$-only refresh or a $\overline{CAS}$ before $\overline{RAS}$ refresh cycle be executed while $\overline{WE} \geq V_{IH}$ to ensure normal operation.

(3) AC measurements assume $t_T = 5$ ns.

(4) V_{IH} (min) and V_{IL} (max) are reference levels for measuring the timing of input signals. Transition times are measured between V_{IH} and V_{IL}.

(5) I_{CC1}, I_{CC3}, I_{CC4}, and I_{CC5} depend on output loading and cycle rates. Specified values are obtained with the output open. I_{CC3} is measured assuming that all column address inputs are held at either a high level or a low level during $\overline{RAS}$-only refresh cycles. I_{CC4} is measured assuming that all column address inputs are switched only once during each nibble cycle.

(6) The minimum specifications are used only to indicate the cycle time at which proper operation over the full temperature range (T_A = 0 to +70°C) is assured.

(7) Load = 2 TTL (–1 mA, +4 mA) loads and 100 pF (V_{OH} = 2.0 V, V_{OL} = 0.8 V).

(8) Assumes that $t_{RCD} \leq t_{RCD}$ (max) and $t_{RAD} \leq t_{RAD}$ (max). If t_{RCD} or t_{RAD} is greater than the maximum recommended value in this table, t_{RAC} increases by the amount that t_{RCD} or t_{RAD} exceeds the value shown.

(9) If $t_{RAD} \geq t_{RAD}$ (max), then the access time is defined by t_{AA}.

(10) t_{OFF} (max) defines the time at which the output achieves the open-circuit condition an is not referenced to V_{OH} or V_{OL}.

(11) Operation within the t_{RCD} (max) limit assures that t_{RAC} (max) can be met. t_{RCD} (max) is specified as a reference point only; if t_{RCD} is greater than t_{RCD} (max), then access time is controlled exclusively by t_{CAC}.

(12) The t_{CRP} requirement should be applicable for $\overline{RAS}$/$\overline{CAS}$ cycles preceded by any cycle.

(13) Either t_{RRH} or t_{RCH} must be satisfied for a read cycle.

(14) Parameter t_{WP} is applicable for a delayed write cycle such as a read-write/read-modify-write cycle. For early write operation, both t_{WCS} and t_{WCH} must be met.

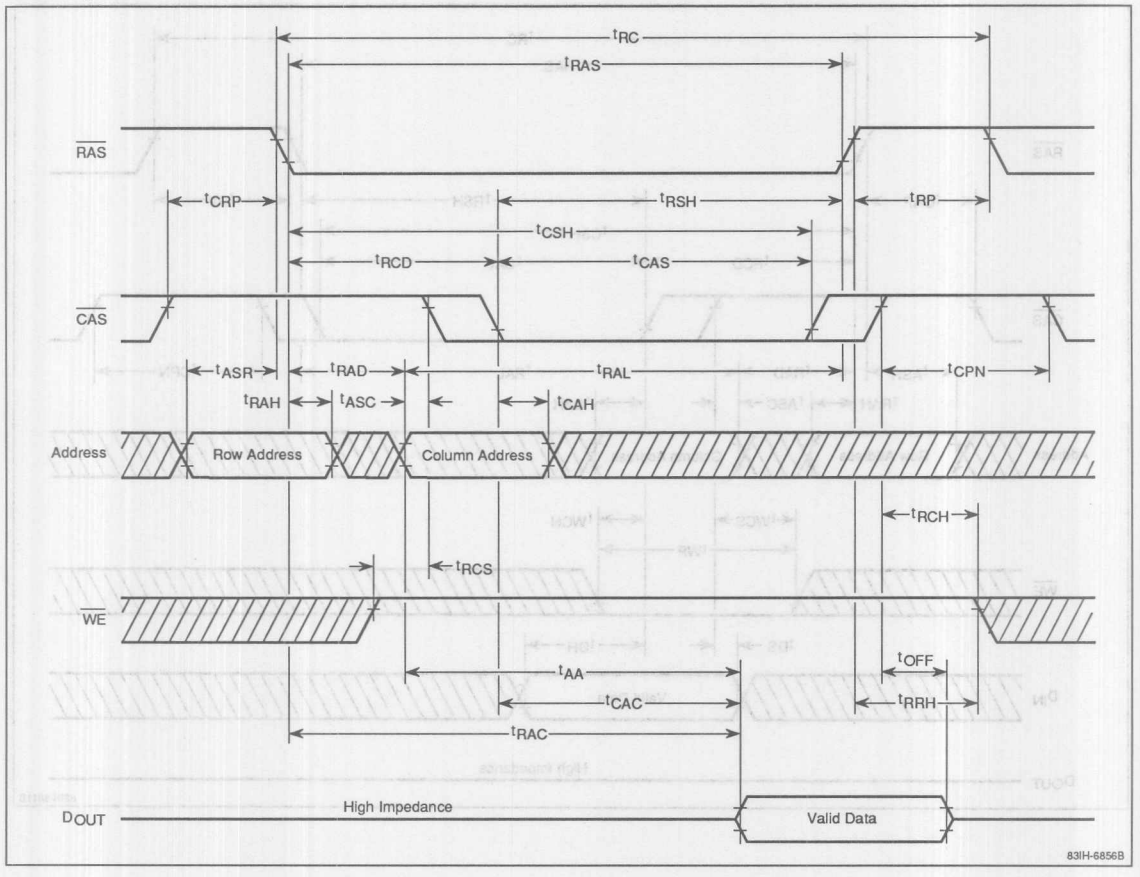
(15) These parameters are referenced to the falling edge of $\overline{CAS}$ for early write cycles and to the falling edge of $\overline{WE}$ for delayed write or read-modify-write cycles.

(16) t_{WCS}, t_{RWD}, t_{CWD}, and t_{AWD} are restrictive operating parameters in read-write/read-modify-write cycles only. If $t_{WCS} \geq t_{WCS}$ (min), the cycle is an early write cycle and the data output will remain open-circuit throughout the entire cycle. If $t_{CWD} \geq t_{CWD}$ (min), $t_{RWD} \geq t_{RWD}$ (min), and $t_{AWD} \geq t_{AWD}$ (min), the cycle is a read-write cycle and the data output will contain data read from the selected cell. If neither of the above conditions is met, the condition of the data output pin (at access time and until $\overline{CAS}$ returns to V_{IH}) is indeterminate.

(17) A test mode may be initiated by executing a $\overline{CAS}$ before $\overline{RAS}$ refresh cycle with $\overline{WE}$ held at V_{IL}. This mode also may inadvertently be initiated during power-up because external control of the signal lines is very difficult during this period. It is therefore recommended that while $\overline{WE}$ is held at V_{IH}, either a $\overline{RAS}$-only or $\overline{CAS}$ before $\overline{RAS}$ refresh cycle should be executed at any time after the end of the initial power-up sequence to ensure normal device operation.

Timing Waveforms

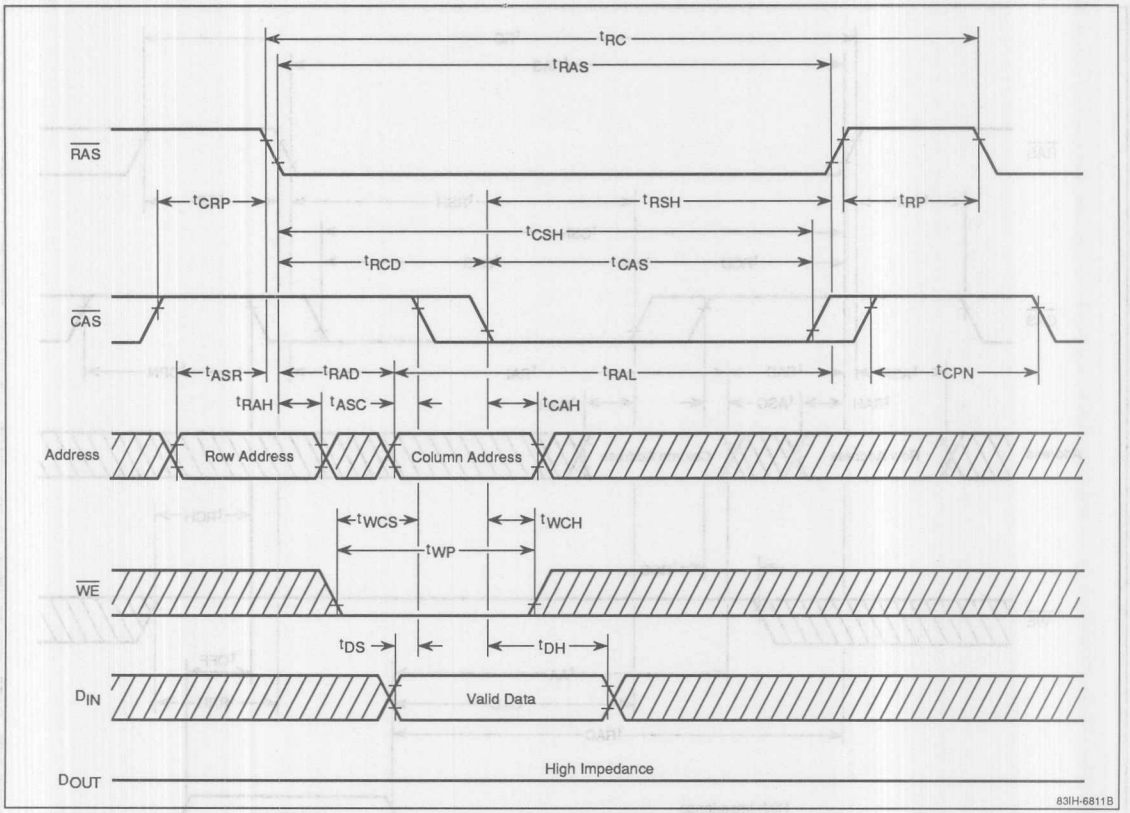
Read Cycle



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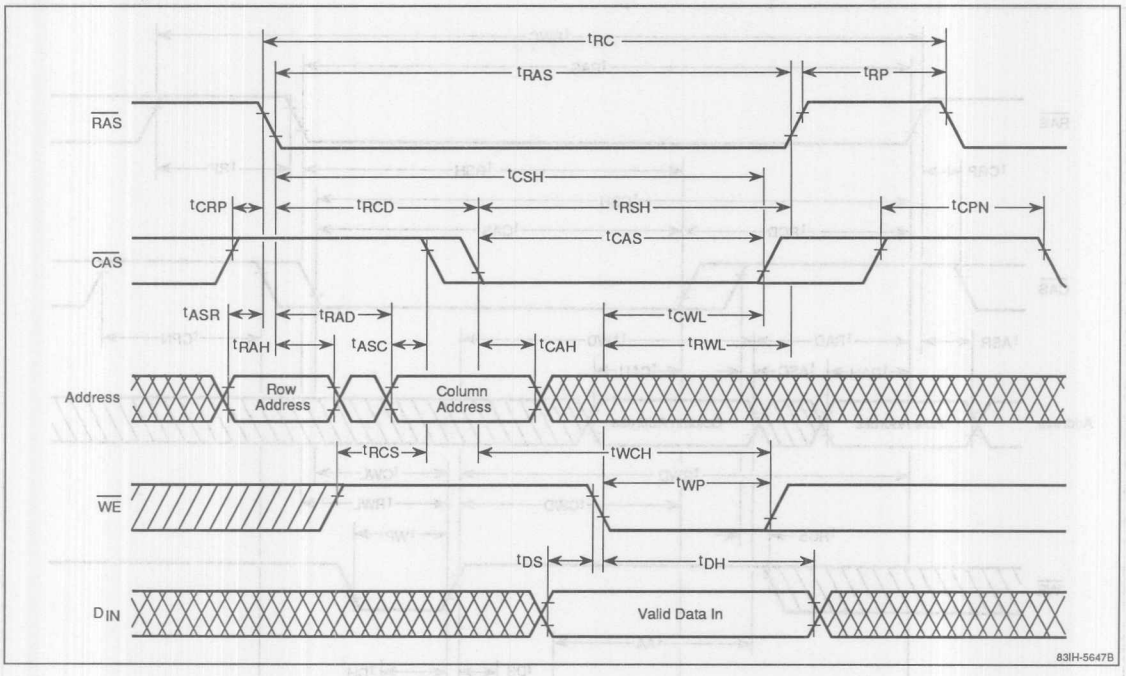
Timing Waveforms (cont)

Early Write Cycle



Timing Waveforms (cont)

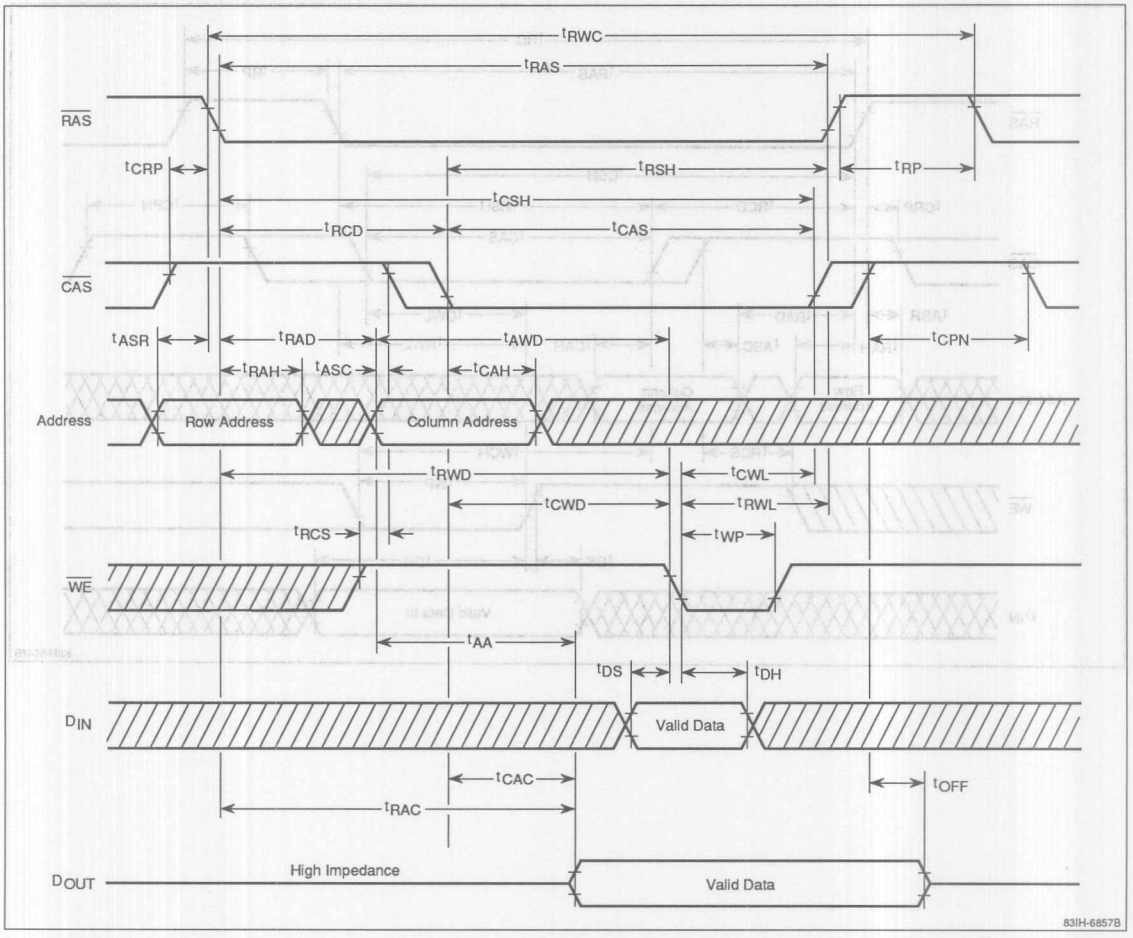
Late Write Cycle



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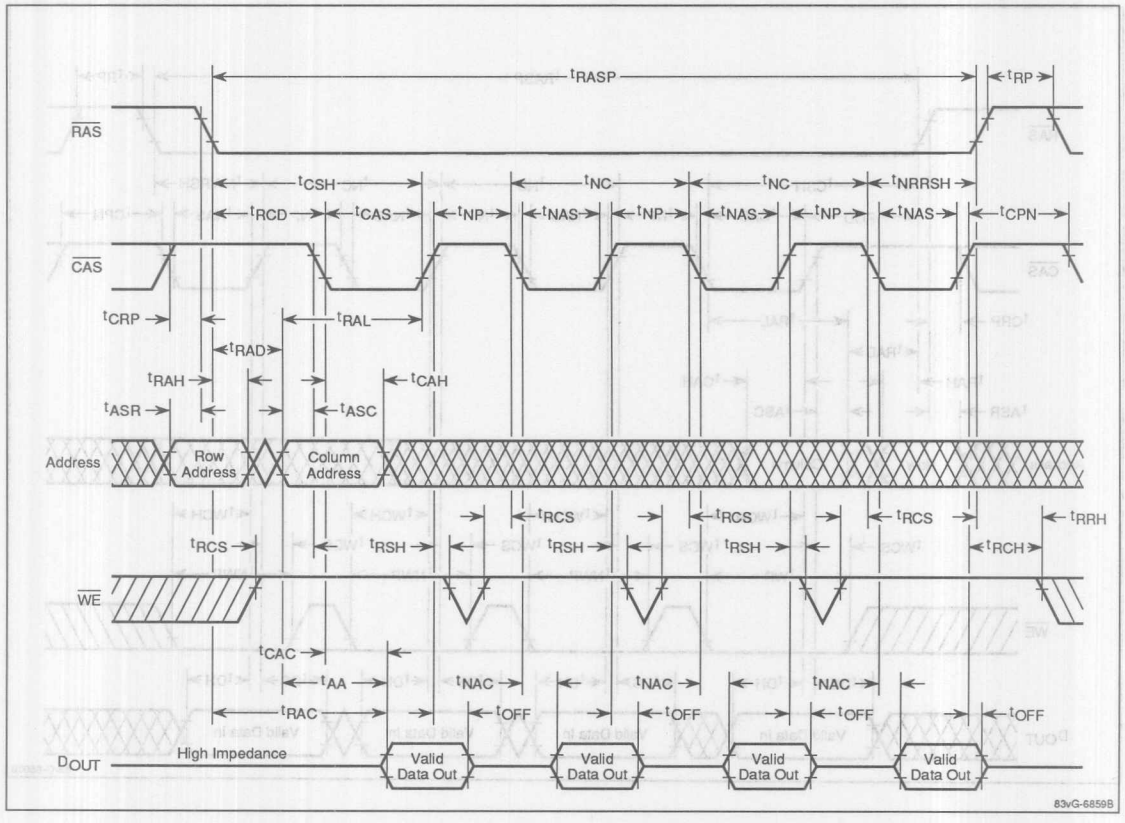
Timing Waveforms (cont)

Read-Write/Read-Modify-Write Cycle



Timing Waveforms (cont)

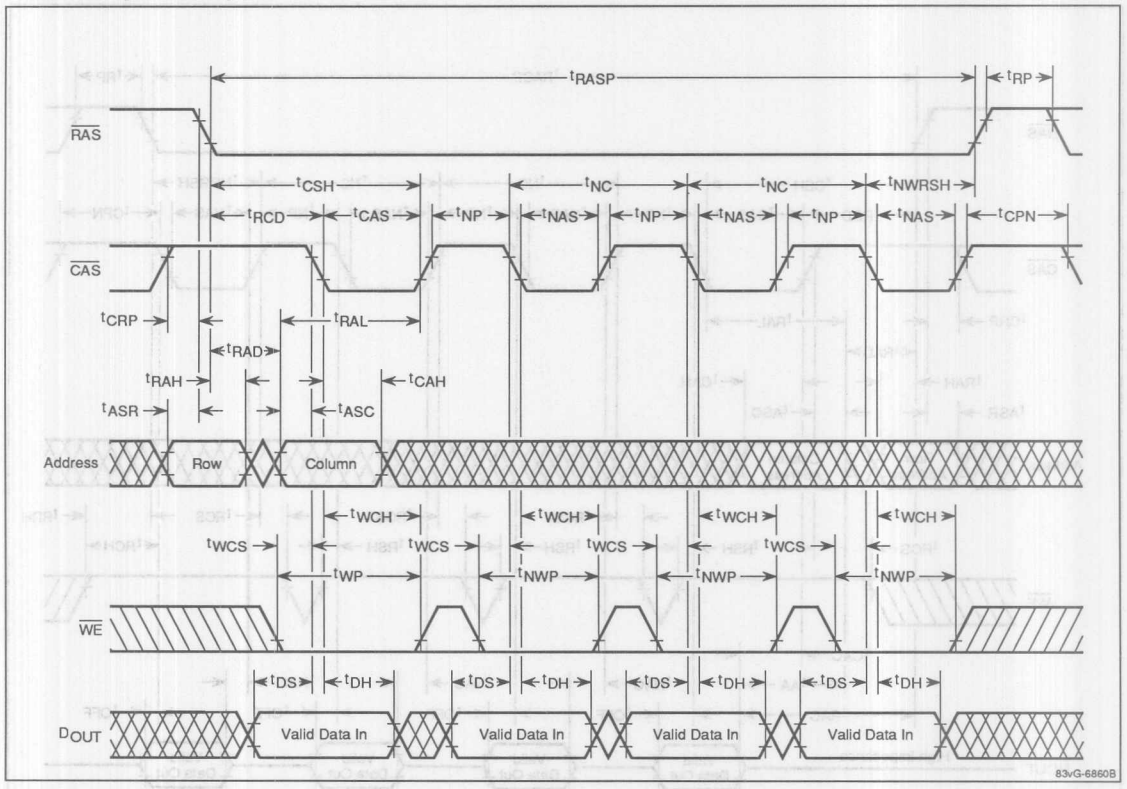
Nibble Read Cycle



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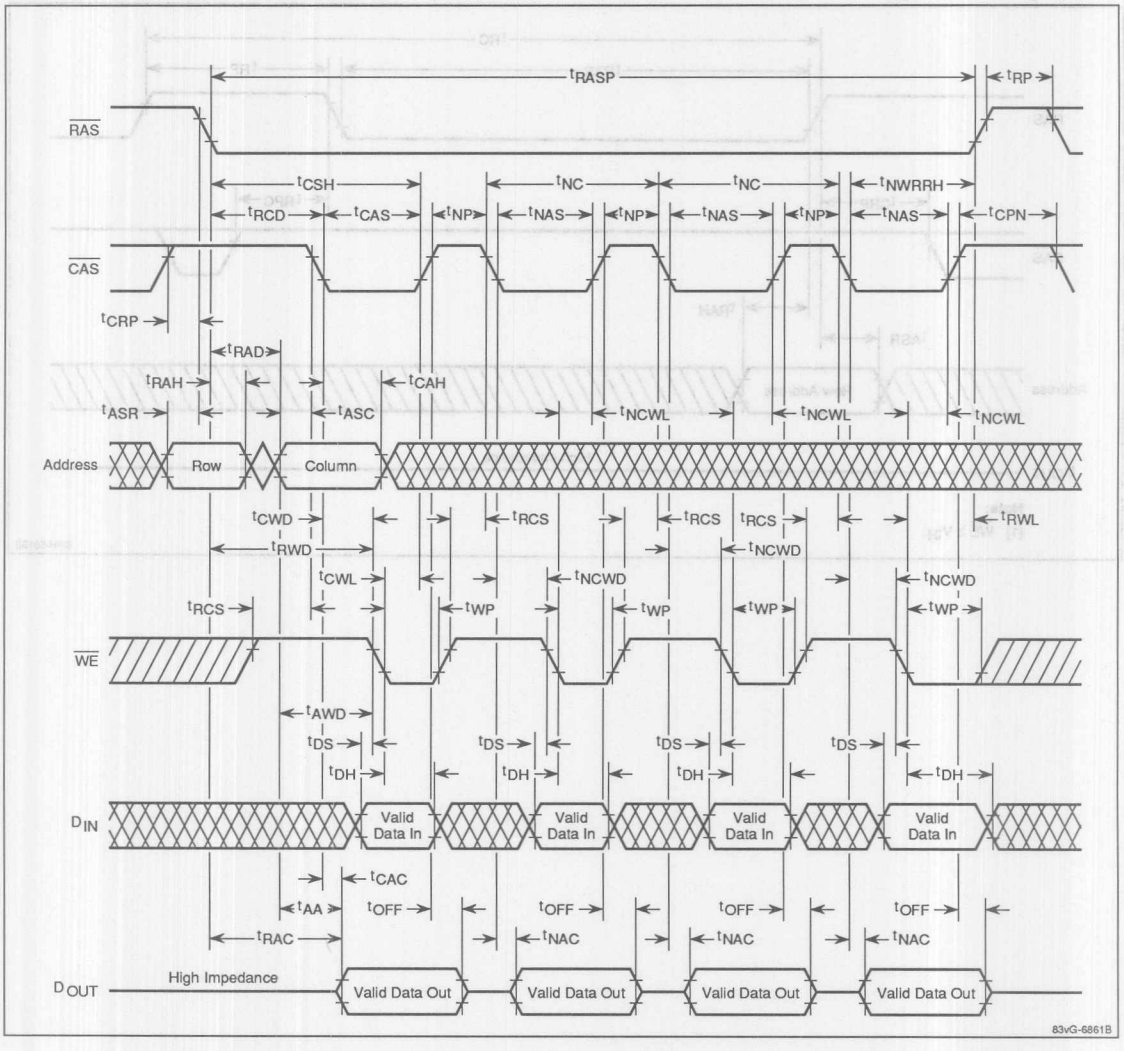
Timing Waveforms (cont)

Nibble Early Write Cycle



Timing Waveforms (cont)

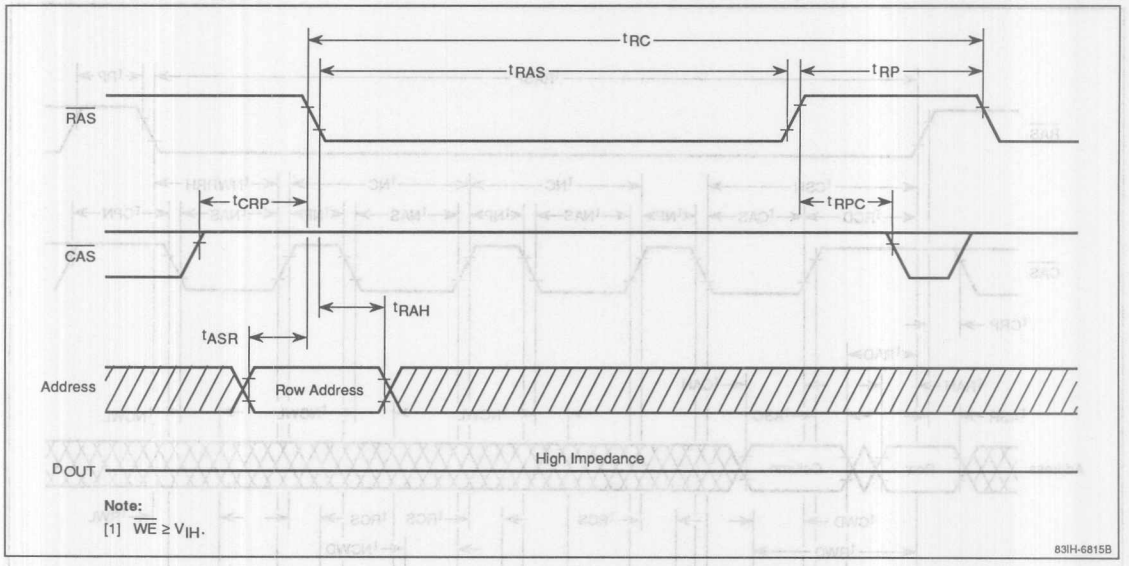
Nibble Read-Write/Read-Modify-Write Cycle



6

Timing Waveforms (cont)

$\overline{RAS}$-Only Refresh Cycle

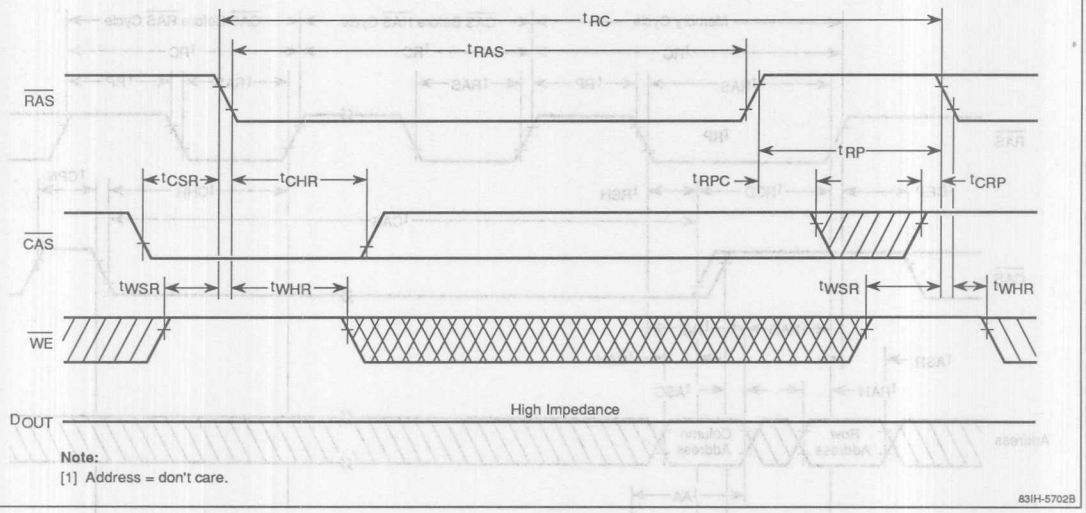


Note:
[1] $\overline{WE} \geq V_{IH}$.

83IH-6815B

Timing Waveforms (cont)

$\overline{CAS}$ Before $\overline{RAS}$ Refresh Cycle

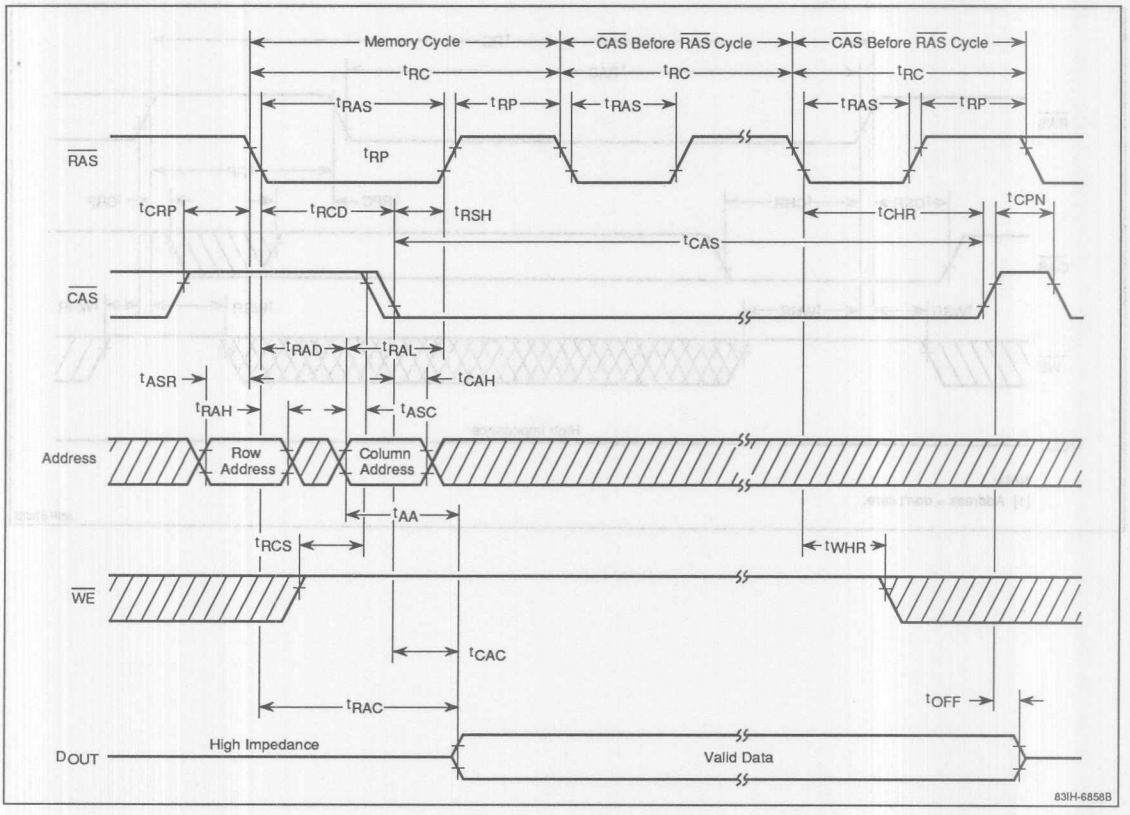


Note:
[1] Address = don't care.

83IH-5702B

Timing Waveforms (cont)

Hidden Refresh Cycle



Description

The μPD424102 is a static-column dynamic RAM organized as 4,194,304 words by 1 bit and designed to operate from a single + 5-volt power supply. Advanced polycide technology using trench capacitors minimizes silicon area and provides high storage cell capacity, high performance, and high reliability. A single-transistor dynamic storage cell and advanced CMOS circuitry throughout ensure minimum power dissipation, while an on-chip circuit internally generates the negative-voltage substrate bias—automatically and transparently.

The three-state output is controlled by $\overline{CS}$ independent of $\overline{RAS}$. After a valid read or read-modify-write cycle, data is held on the output by holding $\overline{CS}$ low. The data output is returned to high impedance by returning $\overline{CS}$ high. Static-column read and write cycles can be executed by cycling $\overline{CS}$.

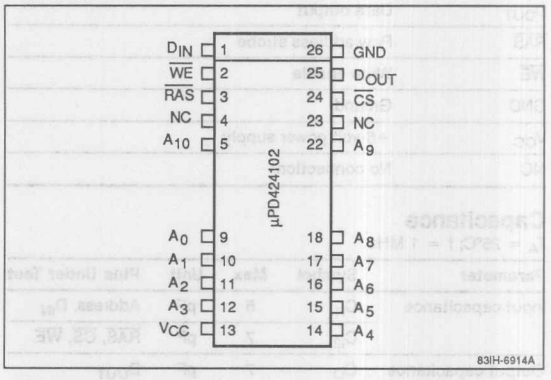
Refreshing may be accomplished by means of a $\overline{CS}$ before $\overline{RAS}$ cycle that internally generates the refresh address. Refreshing can also be accomplished by means of $\overline{RAS}$-only refresh cycles or by normal read or write cycles on the 1024 address combinations of A_0 through A_9 during a 16-ms refresh period.

Features

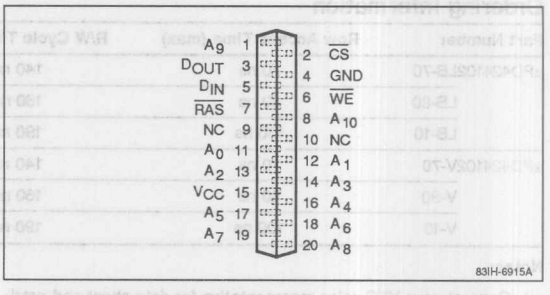
- 4,194,304-word by 1-bit organization
- Single + 5-volt ±10% power supply
- Static-column option
- Low power dissipation
- $\overline{CS}$ before $\overline{RAS}$ refresh cycles
- Multiplexed address inputs
- On-chip substrate bias generator
- Nonlatched, three-state outputs
- Low input capacitance
- TTL-compatible inputs and outputs
- 1024 refresh cycles every 16 ms
- 26/20-pin SOJ or 20-pin plastic ZIP packaging

Pin Configurations

26/20-Pin Plastic SOJ



20-Pin Plastic ZIP



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Pin Identification

Name	Function
A_0 - A_{10}	Address inputs
$\overline{CS}$	Chip select
D_{IN}	Data input
D_{OUT}	Data output
$\overline{RAS}$	Row address strobe
$\overline{WE}$	Write enable
GND	Ground
V_{CC}	+5-volt power supply
NC	No connection

Capacitance

T_A = 25°C; f = 1 MHz

Parameter	Symbol	Max	Unit	Pins Under Test
Input capacitance	C_{I1}	5	pF	Address, D_{IN}
	C_{I2}	7	pF	$\overline{RAS}$, $\overline{CS}$, $\overline{WE}$
Output capacitance	C_O	7	pF	D_{OUT}

Recommended Operating Conditions

Parameter	Symbol	Min	Typ	Max	Unit
Input voltage, high	V_{IH}	2.4		V_{CC} + 1.0	V
Input voltage, low	V_{IL}	−1.0		0.8	V
Supply voltage	V_{CC}	4.5	5.0	5.5	V
Ambient temperature	T_A	0		70	°C

Absolute Maximum Ratings

Voltage on any pin relative to GND	−1.0 to +7.0 V
Operating temperature, T_{OPR}	0 to +70°C
Storage temperature, T_{STG}	−55 to +125°C
Short-circuit output current, I_{OS}	50 mA
Power dissipation, P_D	1.0 W

Exposure to Absolute Maximum Ratings for extended periods may affect device reliability; exceeding the ratings could cause permanent damage. The device should be operated within the limits specified under DC and AC Characteristics.

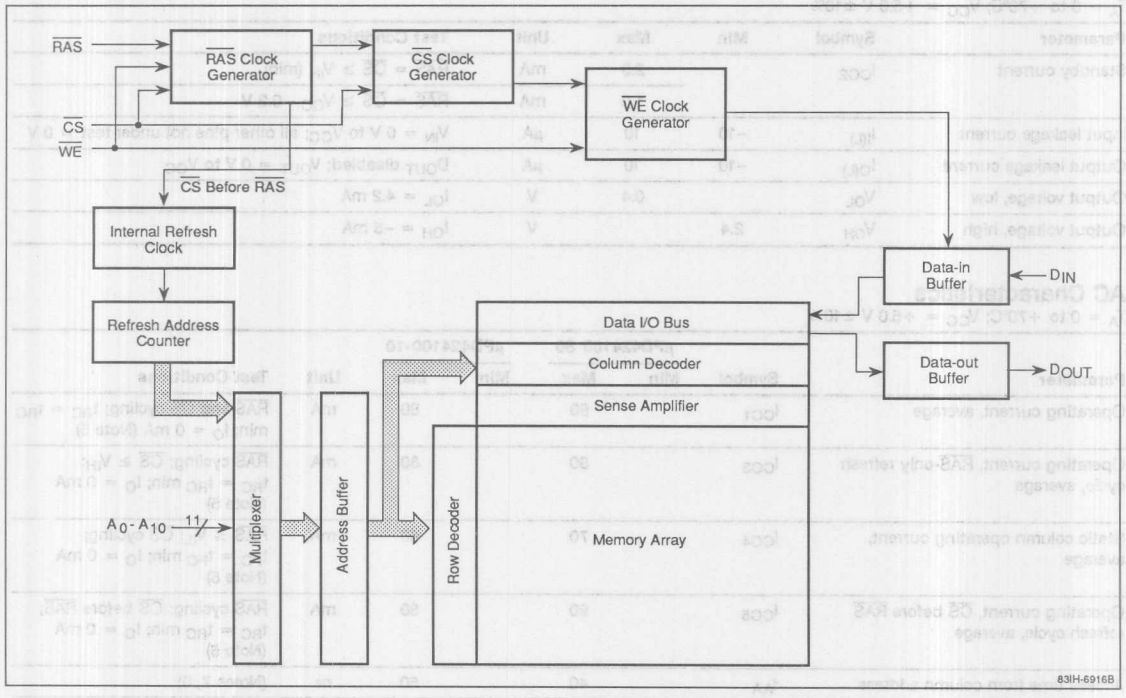
Ordering Information

Part Number	Row Access Time (max)	R/W Cycle Time (min)	Static-Column Cycle (min)	Package
μPD424102LB-70	70 ns	140 ns	40 ns	26/20-pin plastic SOJ
LB-80	80 ns	160 ns	50 ns	
LB-10	100 ns	190 ns	60 ns	
μPD424102V-70	70 ns	140 ns	40 ns	20-pin plastic ZIP
V-80	80 ns	160 ns	50 ns	
V-10	100 ns	190 ns	60 ns	

Notes:

(1) Contact your NEC sales representative for data sheet and product availability of the μPD424102-70.

Block Diagram



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DC Characteristics

T_A = 0 to +70°C; V_{CC} = +5.0 V ±10%

Parameter	Symbol	Min	Max	Unit	Test Conditions
Standby current	I_{CC2}		2.0	mA	$\overline{RAS}$ = $\overline{CS}$ ≥ V_{IH} (min)
			1.0	mA	$\overline{RAS}$ = $\overline{CS}$ ≥ V_{CC} – 0.2 V
Input leakage current	$I_{I(L)}$	–10	10	μA	V_{IN} = 0 V to V_{CC}; all other pins not under test = 0 V
Output leakage current	$I_{O(L)}$	–10	10	μA	D_{OUT} disabled; V_{OUT} = 0 V to V_{CC}
Output voltage, low	V_{OL}		0.4	V	I_{OL} = 4.2 mA
Output voltage, high	V_{OH}	2.4		V	I_{OH} = –5 mA

AC Characteristics

T_A = 0 to +70°C; V_{CC} = +5.0 V ±10%

		μPD424100-80		μPD424100-10			
Parameter	Symbol	Min	Max	Min	Max	Unit	Test Conditions
Operating current, average	I_{CC1}		90		80	mA	$\overline{RAS}$ and $\overline{CS}$ cycling; t_{RC} = t_{RC} min; I_O = 0 mA (Note 5)
Operating current, $\overline{RAS}$-only refresh cycle, average	I_{CC3}		90		80	mA	$\overline{RAS}$ cycling; $\overline{CS}$ ≥ V_{IH}; t_{RC} = t_{RC} min; I_O = 0 mA (Note 5)
Static column operating current, average	I_{CC4}		70		60	mA	$\overline{RAS}$ ≤ V_{IL}; $\overline{CS}$ cycling; t_{PC} = t_{PC} min; I_O = 0 mA (Note 5)
Operating current, $\overline{CS}$ before $\overline{RAS}$ refresh cycle, average	I_{CC5}		90		80	mA	$\overline{RAS}$ cycling; $\overline{CS}$ before $\overline{RAS}$; t_{RC} = t_{RC} min; I_O = 0 mA (Note 5)
Access time from column address	t_{AA}		40		50	ns	(Notes 7, 9)
Column address hold time referenced to $\overline{RAS}$ (rising edge)	t_{AH}	15		15		ns	
Column address setup time	t_{ASC}	0		0		ns	
Row address setup time	t_{ASR}	0		0		ns	
Column address to $\overline{WE}$ delay time	t_{AWD}	40		50		ns	(Note 15)
Access time from $\overline{CS}$ (falling edge)	t_{CAC}		20		25	ns	(Notes 7, 8, 9)
Column address hold time	t_{CAH}	15		20		ns	
$\overline{CS}$ hold time for $\overline{CS}$ before $\overline{RAS}$ refresh cycle	t_{CHR}	15		20		ns	
$\overline{CS}$ precharge time, static-column	t_{CP}	10		10		ns	
$\overline{CS}$ precharge time, nonpage cycle	t_{CPN}	10		10		ns	
$\overline{CS}$ to $\overline{RAS}$ precharge time	t_{CRP}	10		10		ns	(Note 11)
$\overline{CS}$ pulse width	t_{CS}	20	100,000	25	100,000	ns	
$\overline{CS}$ hold time	t_{CSH}	80		100		ns	
$\overline{CS}$ setup time for $\overline{CS}$ before $\overline{RAS}$ refresh cycle	t_{CSR}	10		10		ns	
$\overline{CS}$ to $\overline{WE}$ delay	t_{CWD}	20		25		ns	(Note 15)
Write command to $\overline{CS}$ lead time	t_{CWL}	15		20		ns	
Data-in hold time	t_{DH}	15		20		ns	(Note 14)
Data-in setup time	t_{DS}	0		0		ns	(Note 14)
Output buffer turnoff delay	t_{OFF}	0	20	0	25	ns	(Note 10)

AC Characteristics (cont)

Parameter	Symbol	μPD424100-80 Min	μPD424100-80 Max	μPD424100-10 Min	μPD424100-10 Max	Unit	Test Conditions
Output hold time from address	t_{OH}	5		5		ns	
Output hold time from $\overline{WE}$	t_{OHW}	10		10		ns	
Access time from previous $\overline{WE}$	t_{PWA}		90		110	ns	(Note 7, 17)
Column address hold time referenced to previous $\overline{WE}$	t_{PWH}	90		110		ns	
Access time from $\overline{RAS}$	t_{RAC}		80		100	ns	(Notes 7, 8)
$\overline{RAS}$ to column address delay time	t_{RAD}	17	40	17	50	ns	(Note 9)
Row address hold time	t_{RAH}	12		12		ns	
Column address lead time referenced to $\overline{RAS}$ (rising edge)	t_{RAL}	40		50		ns	
$\overline{RAS}$ pulse width	t_{RAS}	80	10,000	100	10,000	ns	
Static-column $\overline{RAS}$ pulse width	t_{RASC}	80	100,000	100	100,000	ns	
Random read or write cycle time	t_{RC}	160		190		ns	(Note 6)
$\overline{RAS}$ to $\overline{CS}$ delay time	t_{RCD}	25	60	25	75	ns	(Note 8)
Read command hold time referenced to $\overline{CS}$	t_{RCH}	0		0		ns	(Note 12)
Read command setup time	t_{RCS}	0		0		ns	
Refresh period	t_{REF}		16		16	ms	Addresses A_0 - A_9
$\overline{RAS}$ precharge time	t_{RP}	70		80		ns	
$\overline{RAS}$ precharge $\overline{CS}$ hold time	t_{RPC}	10		10		ns	
Read command hold time referenced to $\overline{RAS}$	t_{RRH}	10		10		ns	(Note 12)
Read cycle time	t_{RSC}	50		60		ns	
$\overline{RAS}$ hold time	t_{RSH}	20		25		ns	
$\overline{RAS}$ to second $\overline{WE}$ delay time	t_{RSW}	95		115		ns	
Read-write cycle time	t_{RWC}	185		220		ns	(Note 6)
$\overline{RAS}$ to $\overline{WE}$ delay	t_{RWD}	80		100		ns	(Note 15)
Write command to $\overline{RAS}$ lead time	t_{RWL}	20		25		ns	
Static-column read/write cycle time	t_{RWSC}	95		115		ns	
Rise and fall transition time	t_T	3	50	3	50	ns	(Note 3)
$\overline{WE}$ to column address delay time	t_{WAD}	20	45	25	55	ns	(Note 17)
Write command hold time	t_{WCH}	15		20		ns	
Write command setup time	t_{WCS}	0		0		ns	(Note 15)
$\overline{WE}$ hold time	t_{WHR}	15		20		ns	
Write invalid time	t_{WI}	10		10		ns	
Write command pulse width	t_{WP}	15		20		ns	(Note 13)
Write cycle time	t_{WSC}	50		60		ns	
$\overline{WE}$ setup time	t_{WSR}	10		10		ns	

Notes:

(1) All voltages are referenced to GND.

(2) An initial pause of 100 μs is required after power-up, followed by any eight $\overline{RAS}$ cycles, before proper device operation is achieved. At the end of the initial power-up sequence, it is recommended that either a $\overline{RAS}$-only refresh or a $\overline{CS}$ before $\overline{RAS}$ refresh cycle be executed while $\overline{WE} \geq V_{IH}$ to ensure normal operation.

(3) AC measurements assume $t_T = 5$ ns.

(4) V_{IH} (min) and V_{IL} (max) are reference levels for measuring the timing of input signals. Transition times are measured between V_{IH} and V_{IL}.

(5) I_{CC1}, I_{CC3}, I_{CC4}, and I_{CC5} depend on output loading and cycle rates. Specified values are obtained with the output open. I_{CC3} is measured assuming that all column address inputs are held at either a high level or a low level during $\overline{RAS}$-only refresh cycles. I_{CC4} is measured assuming that all column address inputs are switched only once during each fast-page cycle.

(6) The minimum specifications are used only to indicate the cycle time at which proper operation over the full temperature range (T_A = 0 to +70°C) is assured.

(7) Load = 2 TTL (–1 mA, +4 mA) loads and 100 pF (V_{OH} = 2.0 V, V_{OL} = 0.8 V).

(8) Assumes that $t_{RCD} \leq t_{RCD}$ (max) and $t_{RAD} \leq t_{RAD}$ (max). If t_{RCD} or t_{RAD} is greater than the maximum recommended value in this table, t_{RAC} increases by the amount that t_{RCD} or t_{RAD} exceeds the value shown.

(9) If $t_{RAD} \geq t_{RAD}$ (max), then the access time is defined by t_{AA}.

(10) t_{OFF} (max) defines the time at which the output achieves the open-circuit condition and is not referenced to V_{OH} or V_{OL}.

(11) The t_{CRP} requirement should be applicable for $\overline{RAS}$/$\overline{CS}$ cycles preceded by any cycle.

(12) Either t_{RRH} or t_{RCH} must be satisfied for a read cycle.

(13) Parameter t_{WP} is applicable for a delayed write cycle such as a read-write/read-modify-write cycle. For early write operation, both t_{WCS} and t_{WCH} must be met.

(14) These parameters are referenced to the falling edge of $\overline{CS}$ for early write cycles and to the falling edge of $\overline{WE}$ for delayed write or read-modify-write cycles.

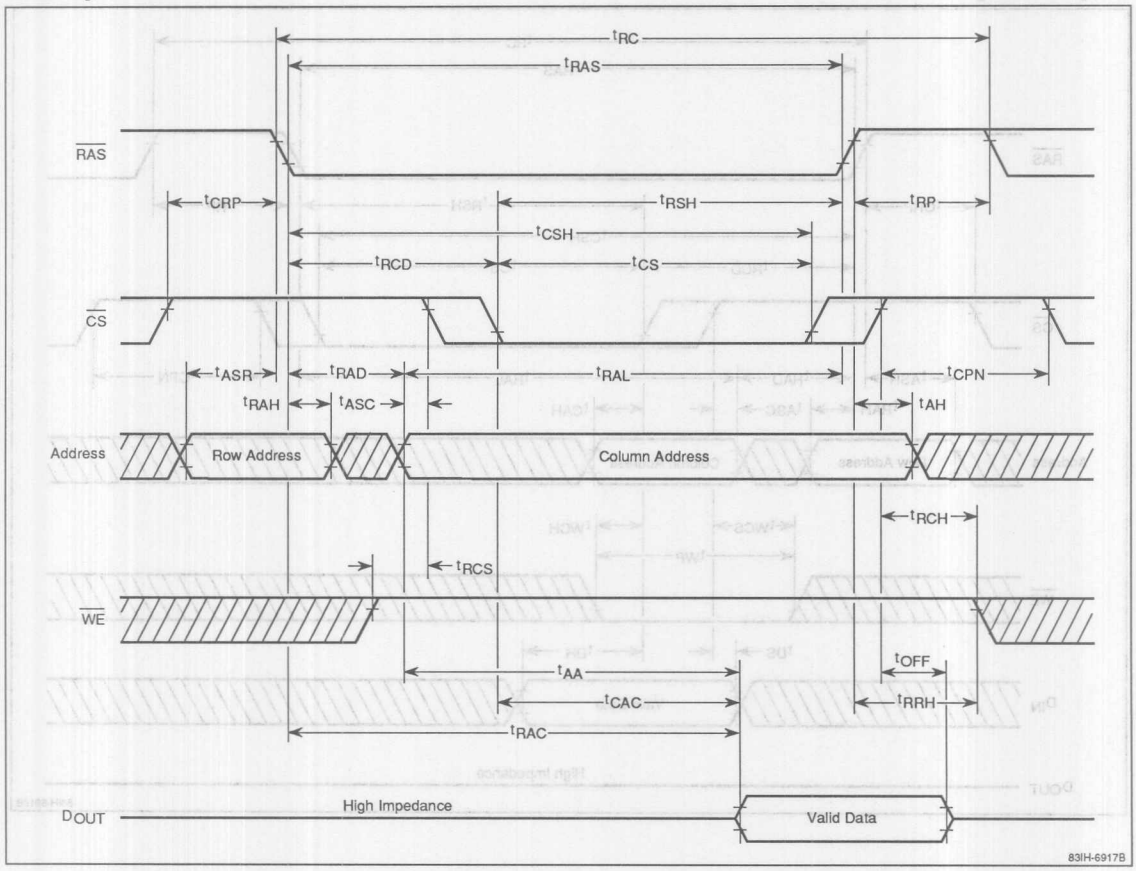
(15) t_{WCS}, t_{RWD}, t_{CWD}, and t_{AWD} are restrictive operating parameters in read-write/read-modify-write cycles only. If $t_{WCS} \geq t_{WCS}$ (min), the cycle is an early write cycle and the data output will remain open-circuit throughout the entire cycle. If $t_{CWD} \geq t_{CWD}$ (min), $t_{RWD} \geq t_{RWD}$ (min), and $t_{AWD} \geq t_{AWD}$ (min), the cycle is a read-write cycle and the data output will contain data read from the selected cell. If neither of the above conditions is met, the condition of the data output pin (at access time and until $\overline{CS}$ returns to V_{IH}) is indeterminate.

(16) A test mode may be initiated by executing a $\overline{CS}$ before $\overline{RAS}$ refresh cycle with $\overline{WE}$ held at V_{IL}. This mode also may inadvertently be initiated during power-up because external control of the signal lines is very difficult during this period. It is therefore recommended that while $\overline{WE}$ is held at V_{IH}, either a $\overline{RAS}$-only or $\overline{CS}$ before $\overline{RAS}$ refresh cycle should be executed at any time after the end of the initial power-up sequence to ensure normal device operation.

(17) Assumes that $t_{WAD} \leq t_{WAD}$ (max).

Timing Waveforms

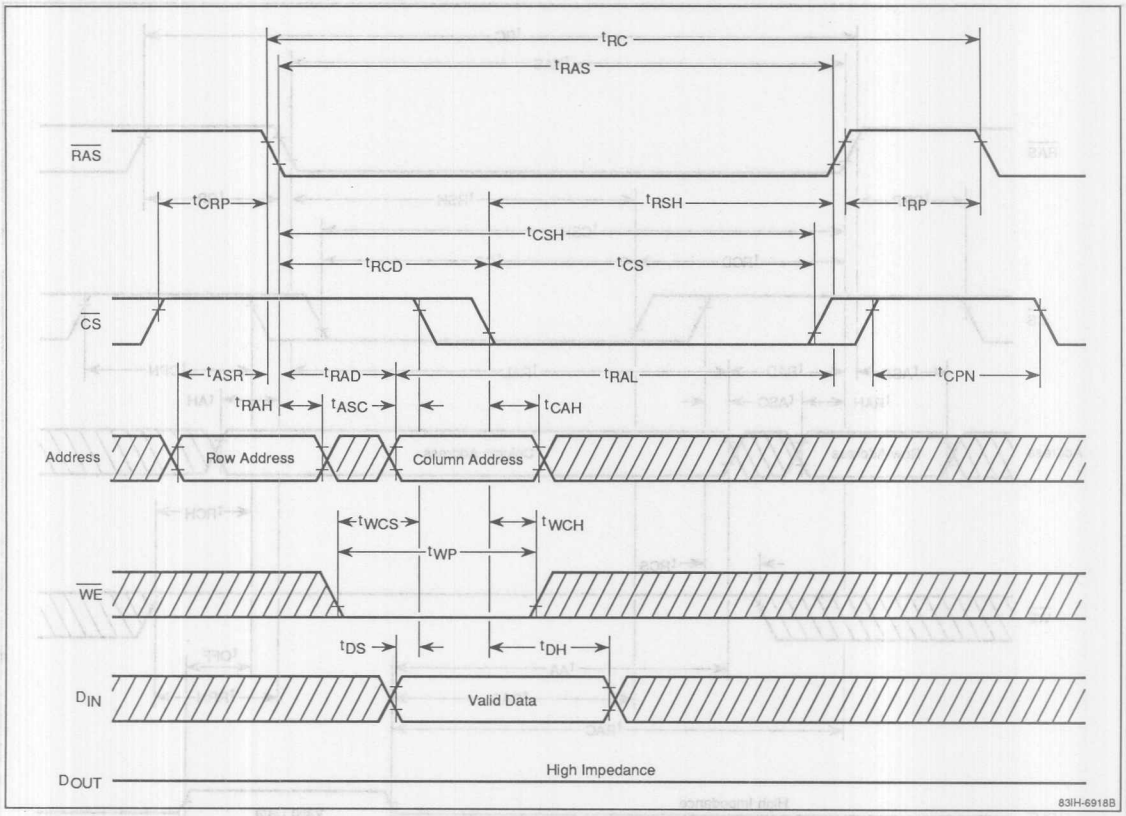
Read Cycle



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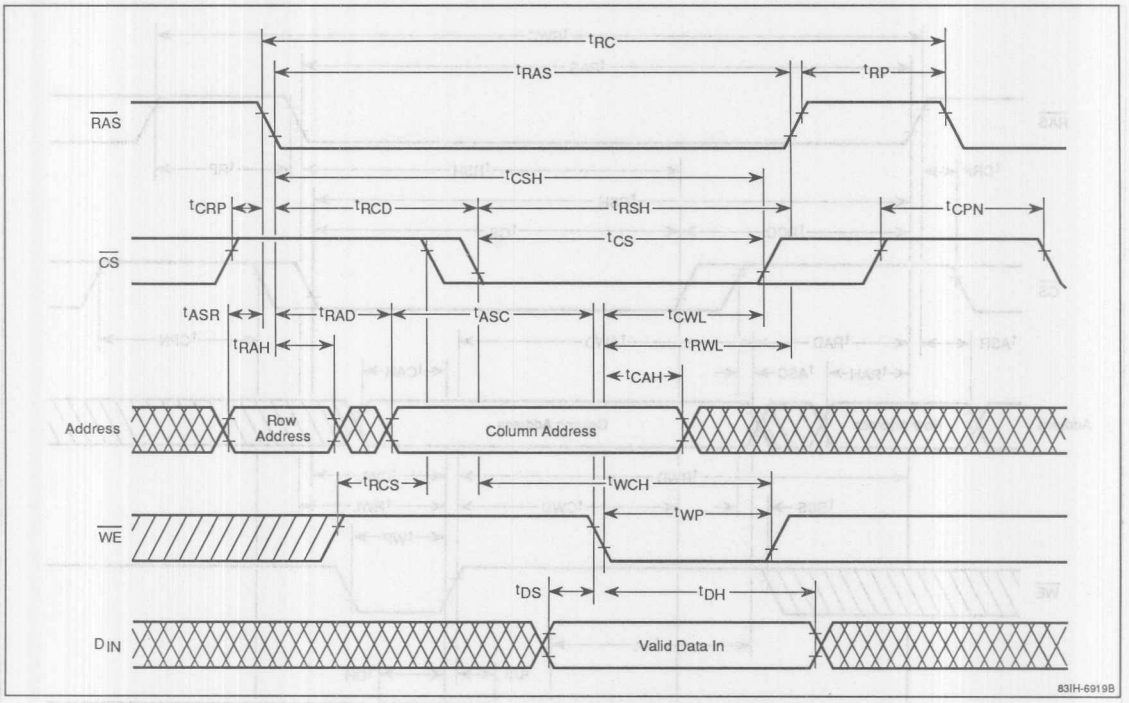
Timing Waveforms (cont)

Early Write Cycle



Timing Waveforms (cont)

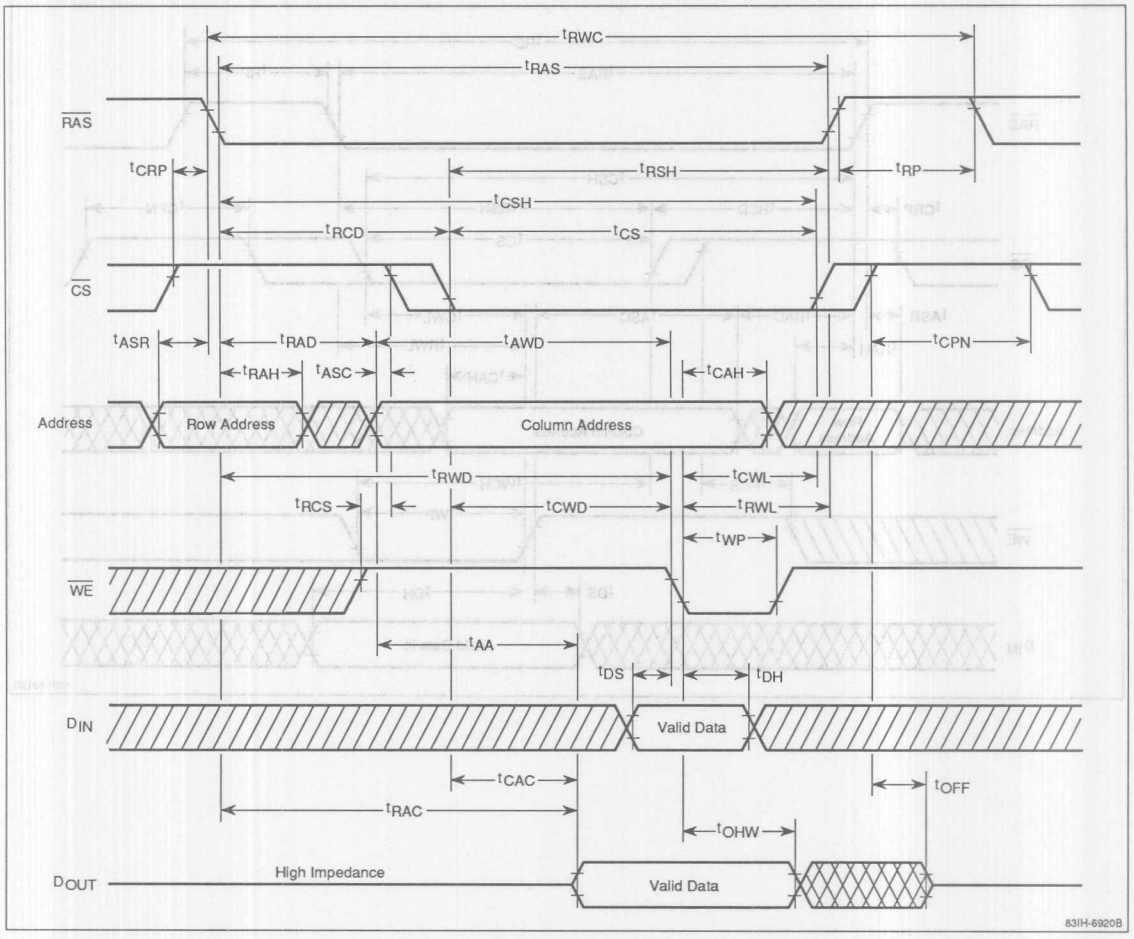
Late Write Cycle



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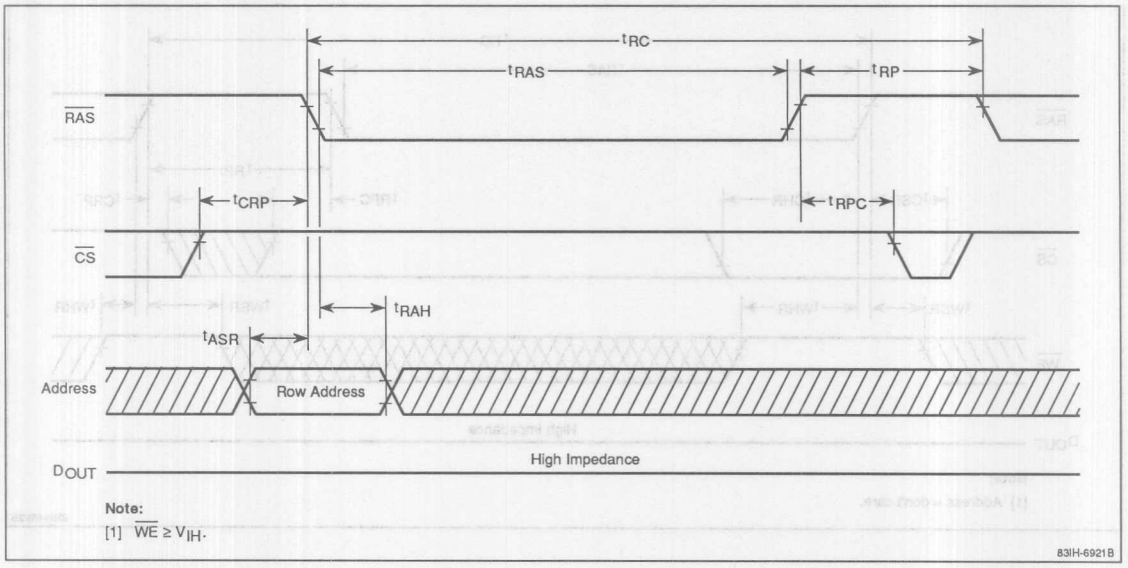
Timing Waveforms (cont)

Read-Write/Read-Modify-Write Cycle



Timing Waveforms (cont)

$\overline{RAS}$-Only Refresh Cycle



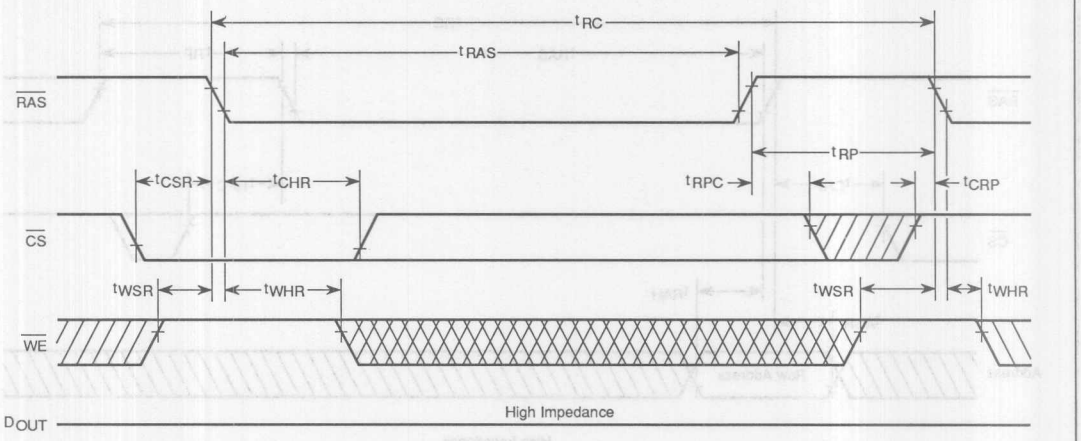
Note:
[1] $\overline{WE} \geq V_{IH}$.

83IH-6921B

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Timing Waveforms (cont)

$\overline{CS}$ Before $\overline{RAS}$ Refresh Cycle

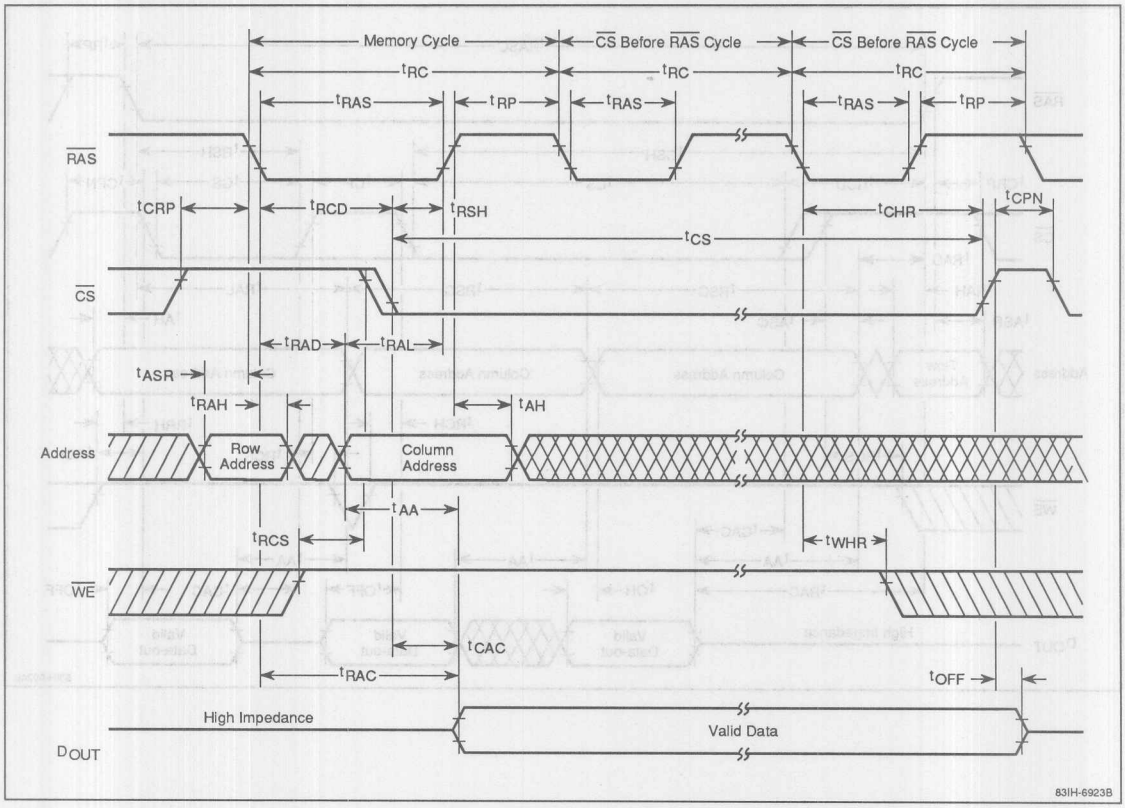


Note:
[1] Address = don't care.

83IH-6922B

Timing Waveforms (cont)

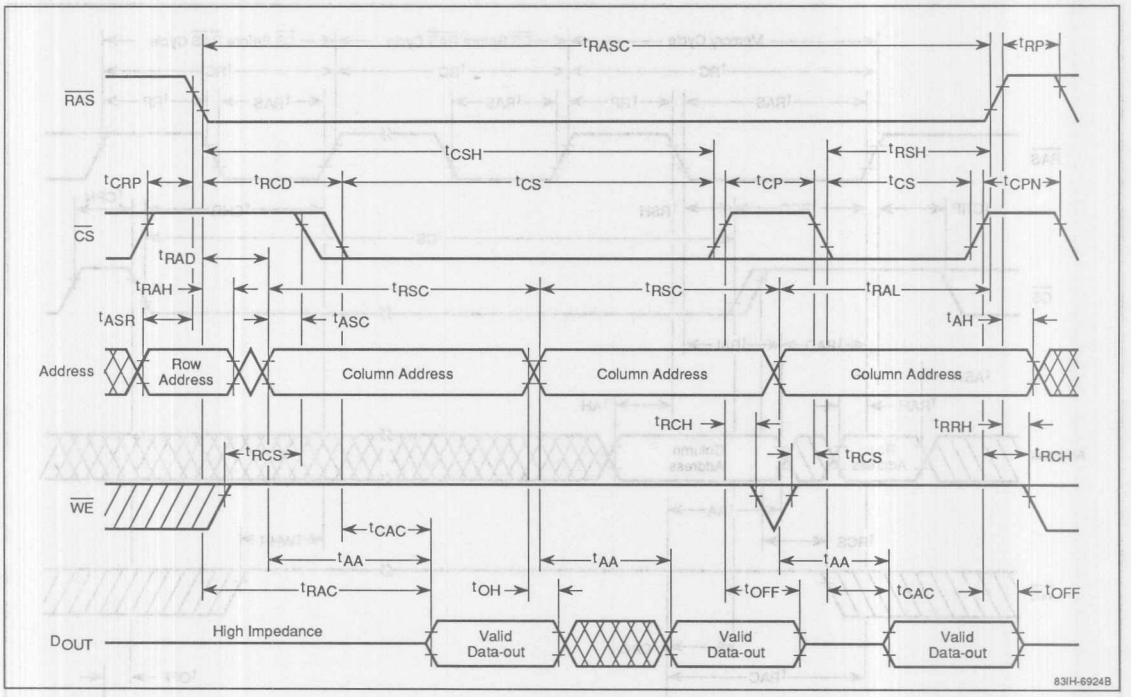
Hidden Refresh Cycle



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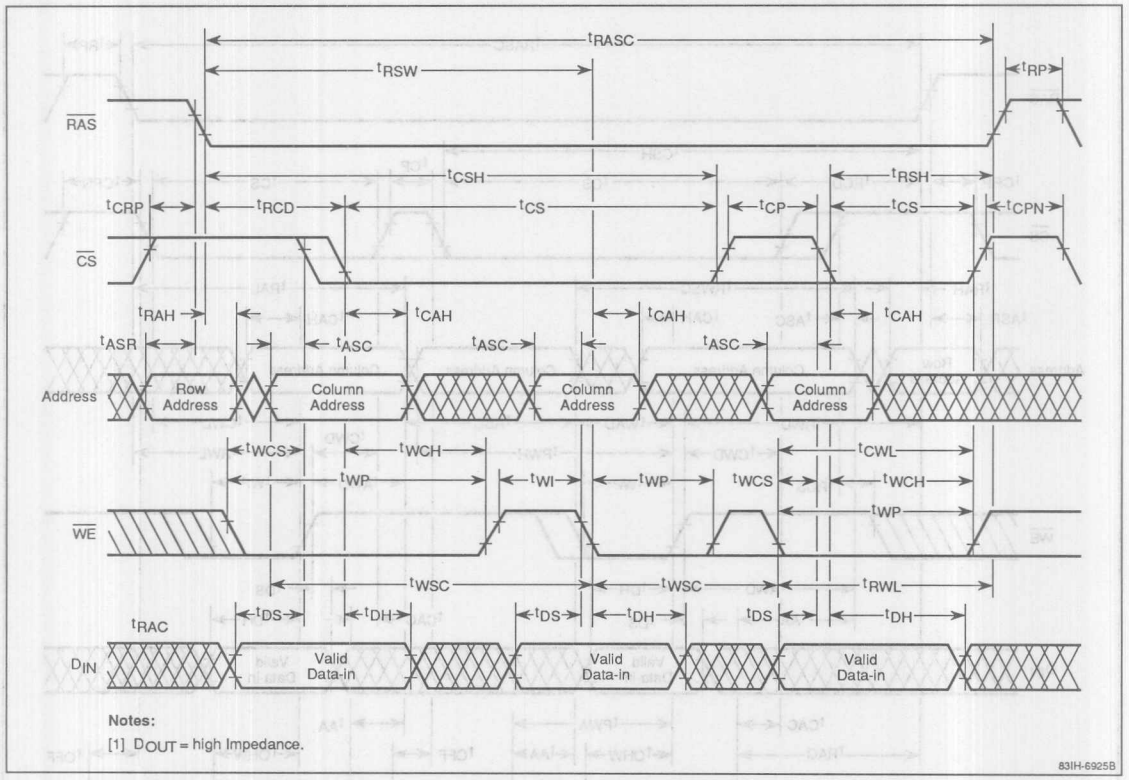
Timing Waveforms (cont)

Static-Column Read Cycle



Timing Waveforms (Cont)

Static-Column Early Write Cycle



Notes:

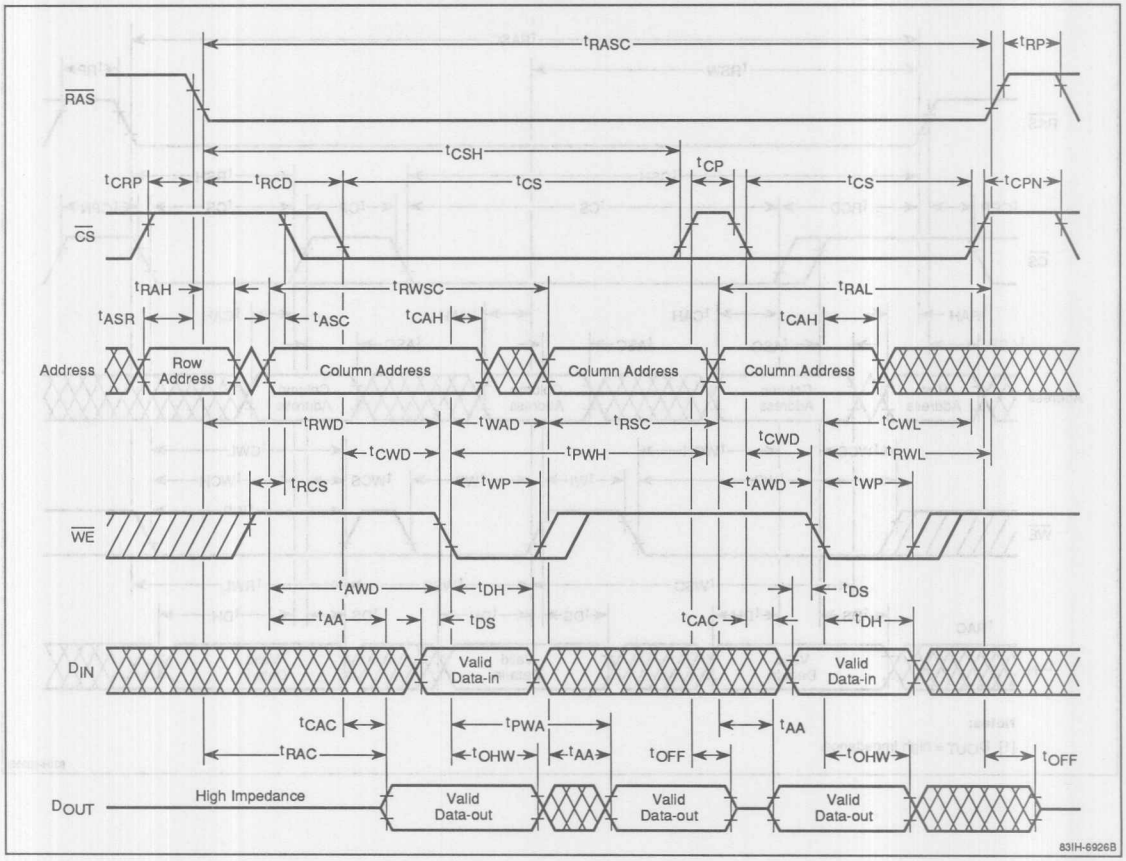
[1] D_{OUT} = high impedance.

83IH-6925B

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Timing Waveforms (cont)

Static-Column Read-Write/Read-Modify-Write Cycle



μPD424400
1,048,576 x 4-Bit
Dynamic CMOS RAM

Description

The μPD424400 is a fast-page dynamic RAM organized as 1,048,576 words by 4 bits and designed to operate from a single +5-volt power supply. Advanced polycide technology using trench capacitors minimizes silicon area and provides high storage cell capacity, high performance, and high reliability. A single-transistor dynamic storage cell and CMOS circuitry throughout ensure minimum power dissipation, while an on-chip circuit internally generates the negative-voltage substrate bias—automatically and transparently.

The three-state I/O pins are controlled by $\overline{CAS}$ independent of $\overline{RAS}$. After a valid read or read-modify-write cycle, data is held on the outputs by maintaining $\overline{CAS}$ low. Data outputs return to high impedance when $\overline{CAS}$ goes high. Fast-page read and write cycles can be be executed by cycling $\overline{CAS}$.

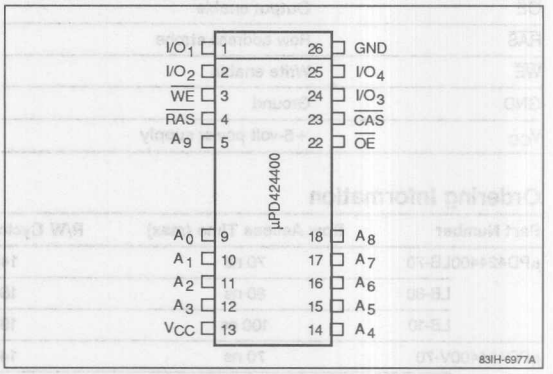
Refreshing may be accomplished by means of a $\overline{CAS}$ before $\overline{RAS}$ cycle that internally generates the refresh address. Refreshing may also be accomplished by means of $\overline{RAS}$-only refresh cycles or by normal read or write cycles on the 1,024 address combinations of A_0 through A_9 during a 16-ms refresh period.

Features

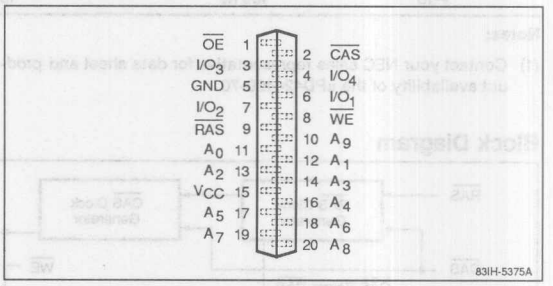
- 1,048,576 by 4-bit organization
- Single +5-volt ±10% power supply
- Fast-page option
- Low power dissipation
- $\overline{CAS}$ before $\overline{RAS}$ refreshing
- Multiplexed address inputs
- On-chip substrate bias generator
- TTL-compatible inputs and outputs
- Nonlatched, three-state outputs
- Low input capacitance
- 1024 refresh cycles every 16 ms
- 26/20-pin plastic SOJ or 20-pin plastic ZIP packaging

Pin Configurations

26/20-Pin Plastic SOJ



20-Pin Plastic ZIP



6

New speeds (60 and 70 ns) and packages (TSOP and 300-mil SOJ) will be available in 1991.

Pin Identification

Name	Function
A_0 - A_9	Address inputs
I/O_1 - I/O_4	Data inputs and outputs
$\overline{CAS}$	Column address strobe
$\overline{OE}$	Output enable
$\overline{RAS}$	Row address strobe
$\overline{WE}$	Write enable
GND	Ground
V_{CC}	+5-volt power supply

Absolute Maximum Ratings

Voltage on any pin relative to GND	−1.0 to +7.0 V
Operating temperature, T_{OPR}	0 to +70 °C
Storage temperature, T_{STG}	−55 to +125 °C
Short-circuit output current, I_{OS}	50 mA
Power dissipation, P_D	1.0 W

Exposure to Absolute Maximum Ratings for extended periods may affect device reliability; exceeding the ratings could cause permanent damage. The device should be operated within the limits specified under DC and AC Characteristics.

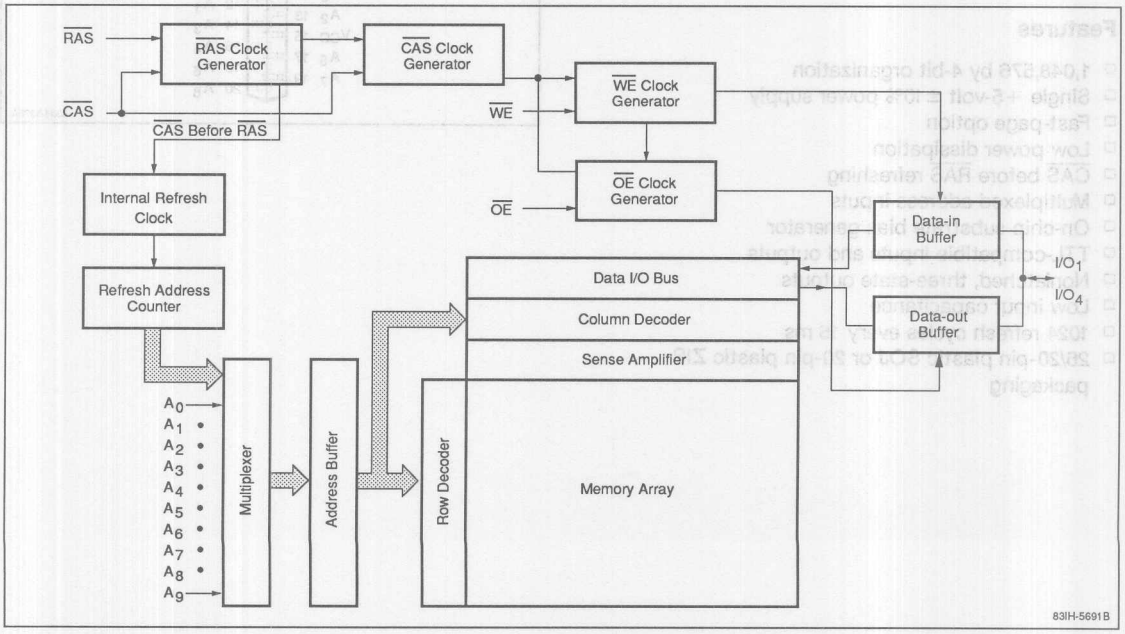
Ordering Information

Part Number	Row Access Time (max)	R/W Cycle Time (min)	Fast-Page Cycle (min)	Package
μPD424400LB-70	70 ns	140 ns	45 ns	26/20-pin plastic SOJ
LB-80	80 ns	160 ns	50 ns	
LB-10	100 ns	190 ns	60 ns	
μPD424400V-70	70 ns	140 ns	45 ns	20-pin plastic ZIP
V-80	80 ns	160 ns	50 ns	
V-10	100 ns	190 ns	60 ns	

Notes:

(1) Contact your NEC sales representative for data sheet and product availability of the μPD424400-70.

Block Diagram



Recommended Operating Conditions

Parameter	Symbol	Min	Typ	Max	Unit
Input voltage, high	V_{IH}	2.4		V_{CC} + 1.0	V
Input voltage, low	V_{IL}	−1.0		0.8	V
Supply voltage	V_{CC}	4.5	5.0	5.5	V
Ambient temperature	T_A	0		70	°C

Capacitance

T_A = 25 °C; f = 1 MHz

Parameter	Symbol	Max	Unit	Pins Under Test
Input capacitance	C_{I1}	5	pF	Addresses
	C_{I2}	7	pF	$\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$, $\overline{OE}$
Input/output capacitance	C_O	7	pF	I/O_1 - I/O_4

DC Characteristics

T_A = 0 to +70°C; V_{CC} = +5.0 ±10%

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions
Standby current	I_{CC2}			2.0	mA	$\overline{RAS}$ = $\overline{CAS}$ ≥ V_{IH} (min); I_O = 0 mA
				1.0	mA	$\overline{RAS}$ = $\overline{CAS}$ ≥ V_{CC} − 0.2 V; I_O = 0 mA
Input leakage current	$I_{I(L)}$	−10		10	μA	V_{IN} = 0 V to V_{CC}; all other pins not under test = 0 V
Output leakage current	$I_{O(L)}$	−10		10	μA	D_{OUT} disabled; V_{OUT} = 0 V to V_{CC}
Output voltage, low	V_{OL}			0.4	V	I_{OL} = 4.2 mA
Output voltage, high	V_{OH}	2.4			V	I_{OH} = −5 mA

AC Characteristics

T_A = 0 to +70 °C; V_{CC} = +5.0 V ± 10%

		μPD424400-80		μPD424400-10			
Parameter	Symbol	Min	Max	Min	Max	Unit	Test Conditions
Operating current, average	I_{CC1}		90		80	mA	$\overline{RAS}$, $\overline{CAS}$ cycling; t_{RC} = t_{RC} min (Note 5)
Operating current, $\overline{RAS}$-only refresh cycle, average	I_{CC3}		90		80	mA	$\overline{RAS}$ cycling; $\overline{CAS}$ ≥ V_{IH} min; t_{RC} = t_{RC} min (Note 5)
Operating current, fast-page cycle, average	I_{CC4}		70		60	mA	$\overline{RAS}$ ≤ V_{IL}; $\overline{CAS}$ cycling; t_{PC} = t_{PC} min (Note 5)
Operating current, $\overline{CAS}$ before $\overline{RAS}$ refresh cycle, average	I_{CC5}		90		80	mA	$\overline{RAS}$ cycling; $\overline{CAS}$ ≤ V_{IL} max; t_{RC} = t_{RC} min (Note 5)
Access time from column address	t_{AA}		40		50	ns	(Notes 3, 4, 7, 8)
Access time from $\overline{CAS}$ precharge (rising edge)	t_{ACP}		45		55	ns	(Notes 3, 4, 7, 8)
Column address setup time	t_{ASC}	0		0		ns	
Row address setup time	t_{ASR}	0		0		ns	
Column address to $\overline{WE}$ delay time	t_{AWD}	65		80		ns	(Note 14)
Access time from $\overline{CAS}$ (falling edge)	t_{CAC}		20		25	ns	(Notes 3, 4, 7, 8)
Column address hold time	t_{CAH}	15		20		ns	
$\overline{CAS}$ pulse width	t_{CAS}	20	10,000	25	10,000	ns	
$\overline{CAS}$ hold time for $\overline{CAS}$ before $\overline{RAS}$ refreshing	t_{CHR}	15		20		ns	
$\overline{CAS}$ to output in low-Z	t_{CLZ}	0		0		ns	(Note 4, 7)
$\overline{CAS}$ precharge time, fast-page cycle	t_{CP}	10		10		ns	
$\overline{CAS}$ precharge time	t_{CPN}	10		10		ns	
$\overline{CAS}$ to $\overline{RAS}$ precharge time	t_{CRP}	10		10		ns	(Note 10)
$\overline{CAS}$ hold time	t_{CSH}	80		100		ns	
$\overline{CAS}$ setup time for $\overline{CAS}$ before $\overline{RAS}$ refresh cycle	t_{CSR}	10		10		ns	

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AC Characteristics (cont)

Parameter	Symbol	μPD424400-80 Min	μPD424400-80 Max	μPD424400-10 Min	μPD424400-10 Max	Unit	Test Conditions
$\overline{CAS}$ to $\overline{WE}$ delay	t_{CWD}	45		55		ns	(Note 14)
Write command referenced to $\overline{CAS}$ lead time	t_{CWL}	15		20		ns	
Data-in hold time	t_{DH}	15		20		ns	(Note 13)
Data-in setup time	t_{DS}	0		0		ns	(Note 13)
Access time from $\overline{OE}$	t_{OEA}		20		25	ns	(Notes 3, 4, 7, 8)
$\overline{OE}$ data delay time	t_{OED}	20		25		ns	
$\overline{OE}$ command hold time	t_{OEH}	0		0		ns	
$\overline{OE}$ to $\overline{RAS}$ inactive setup time	t_{OES}	0		0		ns	
Output turnoff delay from $\overline{OE}$	t_{OEZ}	0	20	0	25	ns	(Note 9)
Output buffer turnoff delay	t_{OFF}	0	20	0	25	ns	(Note 9)
$\overline{OE}$ to output in low-Z	t_{OLZ}	0		0		ns	(Note 5, 7)
Fast-page read or write cycle time	t_{PC}	50		60		ns	(Note 6)
Fast-page read-modify-write cycle time	t_{PRWC}	100		120		ns	(Note 6)
Access time from $\overline{RAS}$	t_{RAC}		80		100	ns	(Notes 3, 4, 7, 8)
$\overline{RAS}$ to column address delay time	t_{RAD}	17	40	17	50	ns	(Note 8)
Row address hold time	t_{RAH}	12		12		ns	
Column address lead time referenced to $\overline{RAS}$ (rising edge)	t_{RAL}	40		50		ns	
$\overline{RAS}$ pulse width	t_{RAS}	80	10,000	100	10,000	ns	
$\overline{RAS}$ pulse width, fast-page cycle	t_{RASP}	80	125,000	100	125,000	ns	
Random read or write cycle time	t_{RC}	160		190		ns	(Note 6)
$\overline{RAS}$ to $\overline{CAS}$ delay time	t_{RCD}	25	60	25	75	ns	(Note 8)
Read command hold time referenced to $\overline{CAS}$	t_{RCH}	0		0		ns	(Note 11)
Read command setup time	t_{RCS}	0		0		ns	
Refresh period	t_{REF}		16		16	ms	Address A_0 through A_9
$\overline{RAS}$ precharge time	t_{RP}	70		80		ns	
$\overline{RAS}$ precharge $\overline{CAS}$ hold time	t_{RPC}	10		10		ns	
Read command hold time referenced to $\overline{RAS}$	t_{RRH}	10		10		ns	(Note 11)
$\overline{RAS}$ hold time	t_{RSH}	20		25		ns	
Read-modify-write cycle time	t_{RWC}	210		250		ns	(Note 6)
$\overline{RAS}$ to $\overline{WE}$ delay	t_{RWD}	105		130		ns	(Note 14)
Write command referenced to $\overline{RAS}$ lead time	t_{RWL}	20		25		ns	
Rise and fall transition time	t_T	3	50	3	50	ns	(Note 4)
Write command hold time	t_{WCH}	15		20		ns	(Note 12)
Write command setup time	t_{WCS}	0		0		ns	(Note 14)
$\overline{WE}$ command hold time for $\overline{CAS}$ before $\overline{RAS}$ refreshing	t_{WHR}	15		20		ns	
Write command pulse width	t_{WP}	15		20		ns	(Note 12)
$\overline{WE}$ command setup time for $\overline{CAS}$ before $\overline{RAS}$ refreshing	t_{WSR}	10		10		ns	

Notes:

(1) All voltages are referenced to GND.

(2) An initial pause of 100 μs is required after power-up, followed by any eight $\overline{RAS}$ cycles, before proper device operation is achieved. At the end of the initial power-up sequence, it is recommended that either a $\overline{RAS}$-only refresh or a $\overline{CAS}$ before $\overline{RAS}$ refresh cycle be executed while $\overline{WE} \geq V_{IH}$ to ensure normal operation.

(3) Ac measurements assume $t_T = 5$ ns.

(4) V_{IH} (min) and V_{IL} (max) are reference levels for measuring the timing of input signals. Transition times are measured between V_{IH} and V_{IL}.

(5) I_{CC1}, I_{CC3}, I_{CC4}, and I_{CC5} depend on output loading and cycle rates. Specified values are obtained with the output open. I_{CC3} is measured assuming that all column address inputs are held at either a high level or a low level during $\overline{RAS}$-only refresh cycles. I_{CC4} is measured assuming that all column address inputs are switched only once during each fast-page cycle.

(6) The minimum specifications are used only to indicate the cycle time at which proper operation over the full temperature range ($T_A = 0$ to $+70$ °C) is assured.

(7) Load = 2 TTL (−1 mA, +4 mA) loads and 100 pF ($V_{OH} = 2.0$ V and $V_{OL} = 0.8$ V).

(8) If $t_{RCD} \leq t_{RCS}$ (max) and $t_{RAD} \leq t_{RAD}$ (max) access time is defined by t_{RAC} (max). If $t_{RCD} \geq t_{RCD}$ (max) access time is defined by t_{CAC} (max) and if $t_{RAD} \geq t_{RAD}$ (max) access time is defined by t_{AA} (max).

(9) t_{OFF} (max) and t_{OEZ} (max) define the time at which the outputs achieve the open-circuit condition and are not referenced to V_{OH} or V_{OL}.

(10) The t_{CRP} requirement should be applicable for $\overline{RAS}/\overline{CAS}$ cycles preceded by any cycle.

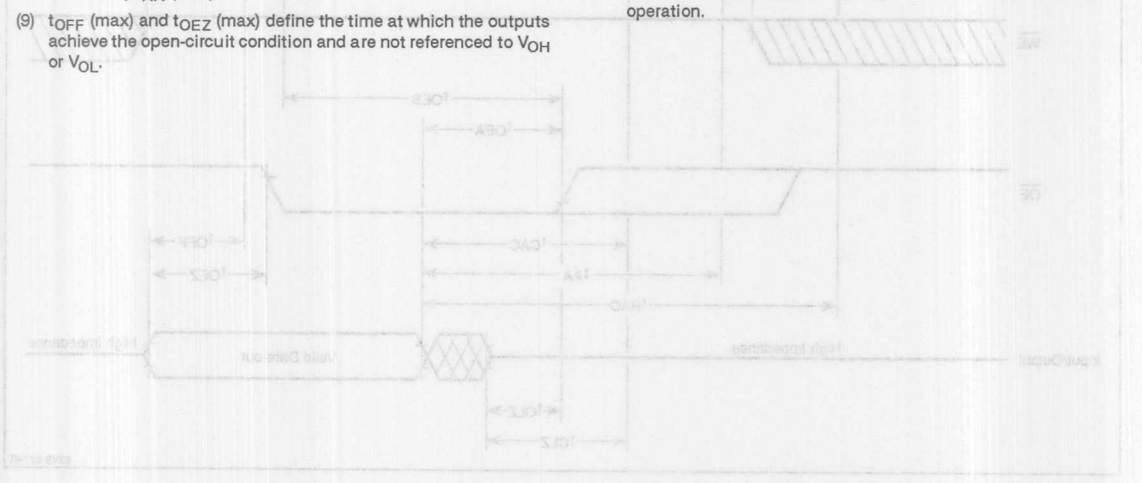
(11) Either t_{RRH} or t_{RCH} must be satisfied for a read cycle.

(12) Parameter t_{WP} is applicable for a delayed write cycle such as a read-write/read-modify-write cycle. For early write cycles, both t_{WCS} and t_{WCH} must be met.

(13) These parameters are referenced to the falling edge of $\overline{CAS}$ for early write cycles and to the falling edge of $\overline{WE}$ for delayed write or read-modify-write cycles.

(14) t_{WCS}, t_{RWD}, t_{CWD}, and t_{AWD} are restrictive operating parameters in read-write/read-modify-write cycles only. If $t_{WCS} \geq t_{WCS}$ (min), the cycle is an early write cycle and the data I/O pins will remain open-circuit throughout the entire cycle. If $t_{CWD} \geq t_{CWD}$ (min), $t_{RWD} \geq t_{RWD}$ (min), and $t_{AWD} \geq t_{AWD}$ (min), then the cycle is a read-write cycle and the data I/O pins will contain data read from the selected cells. If neither of the above conditions is met, the condition of the data I/O pins (at access time and until $\overline{CAS}$ returns to V_{IH}) is indeterminate.

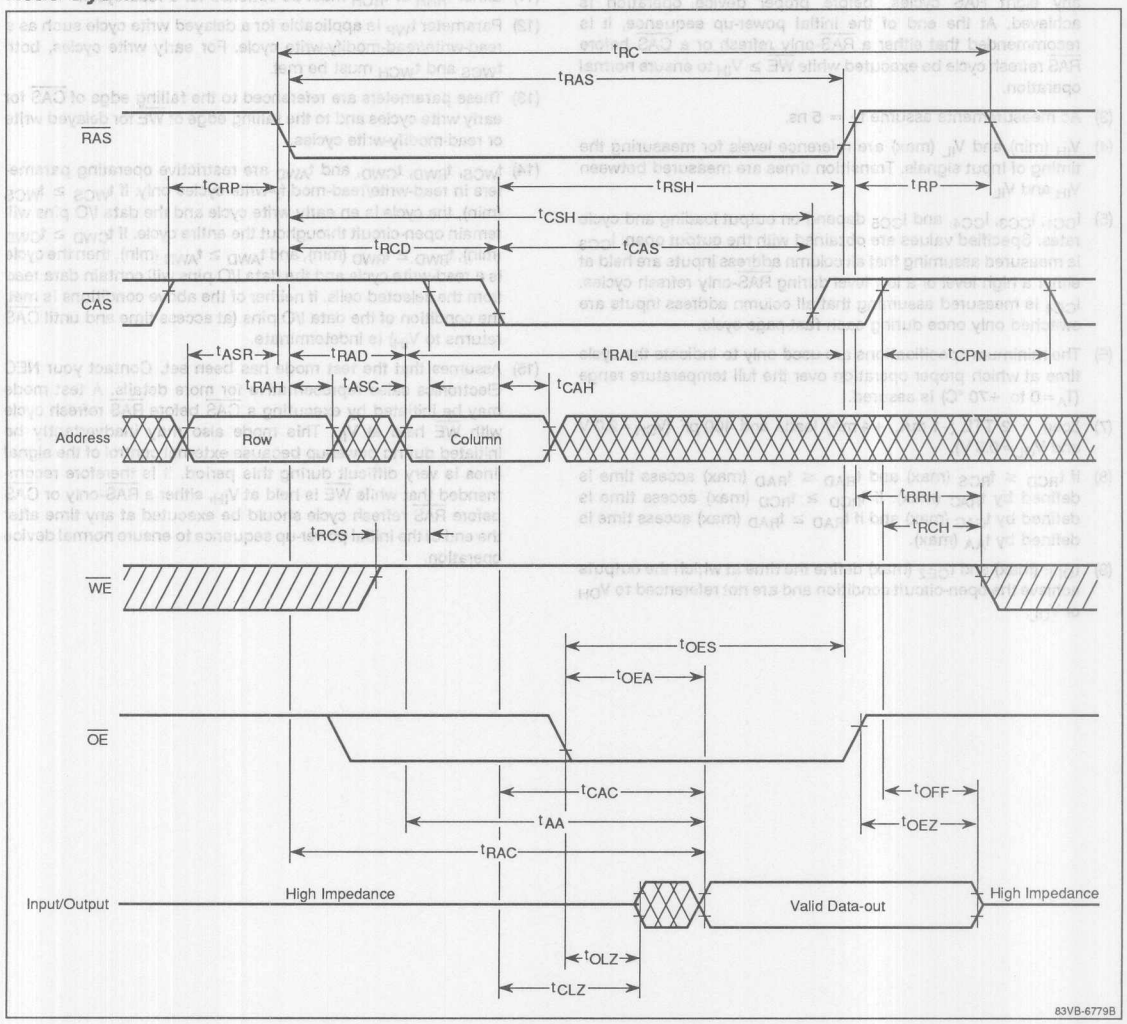
(15) Assumes that the test mode has been set. Contact your NEC Electronics sales representative for more details. A test mode may be initiated by executing a $\overline{CAS}$ before $\overline{RAS}$ refresh cycle with $\overline{WE}$ held at V_{IL}. This mode also may inadvertantly be initiated during power-up because external control of the signal lines is very difficult during this period. It is therefore recommended that while $\overline{WE}$ is held at V_{IH}, either a $\overline{RAS}$-only or $\overline{CAS}$ before $\overline{RAS}$ refresh cycle should be executed at any time after the end of the initial power-up sequence to ensure normal device operation.



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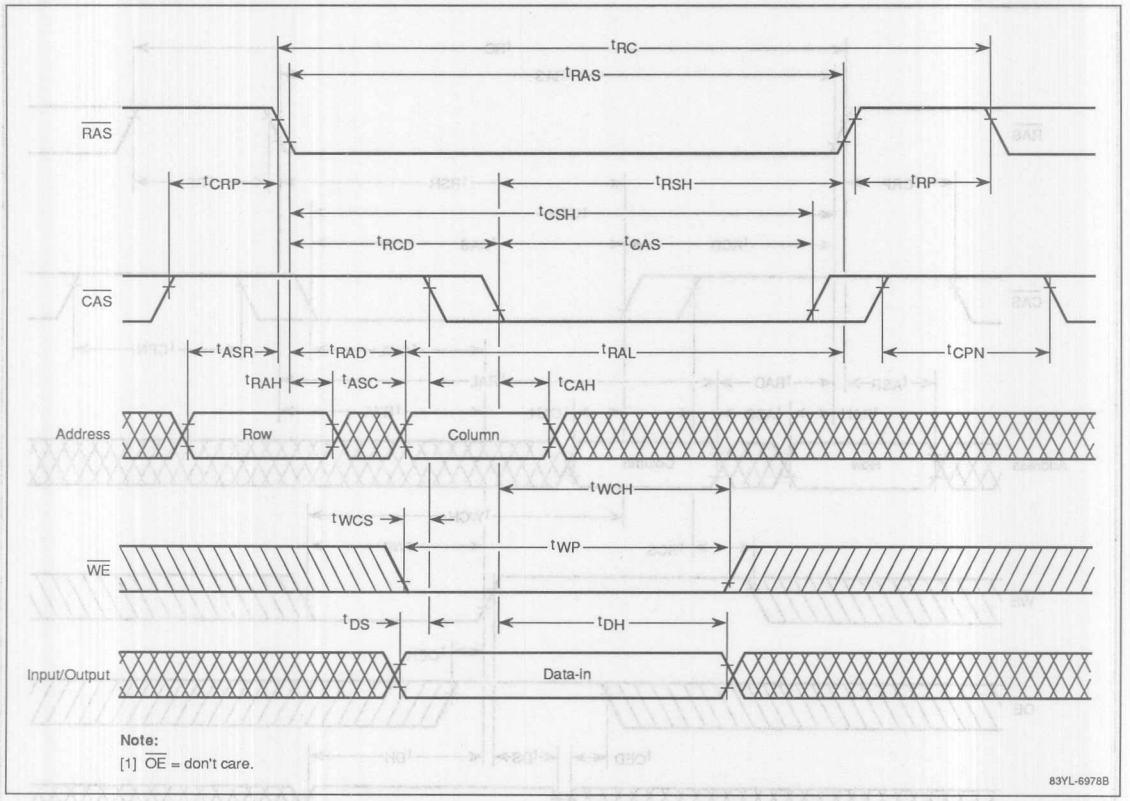
Timing Waveforms

Read Cycle



Timing Waveforms (cont)

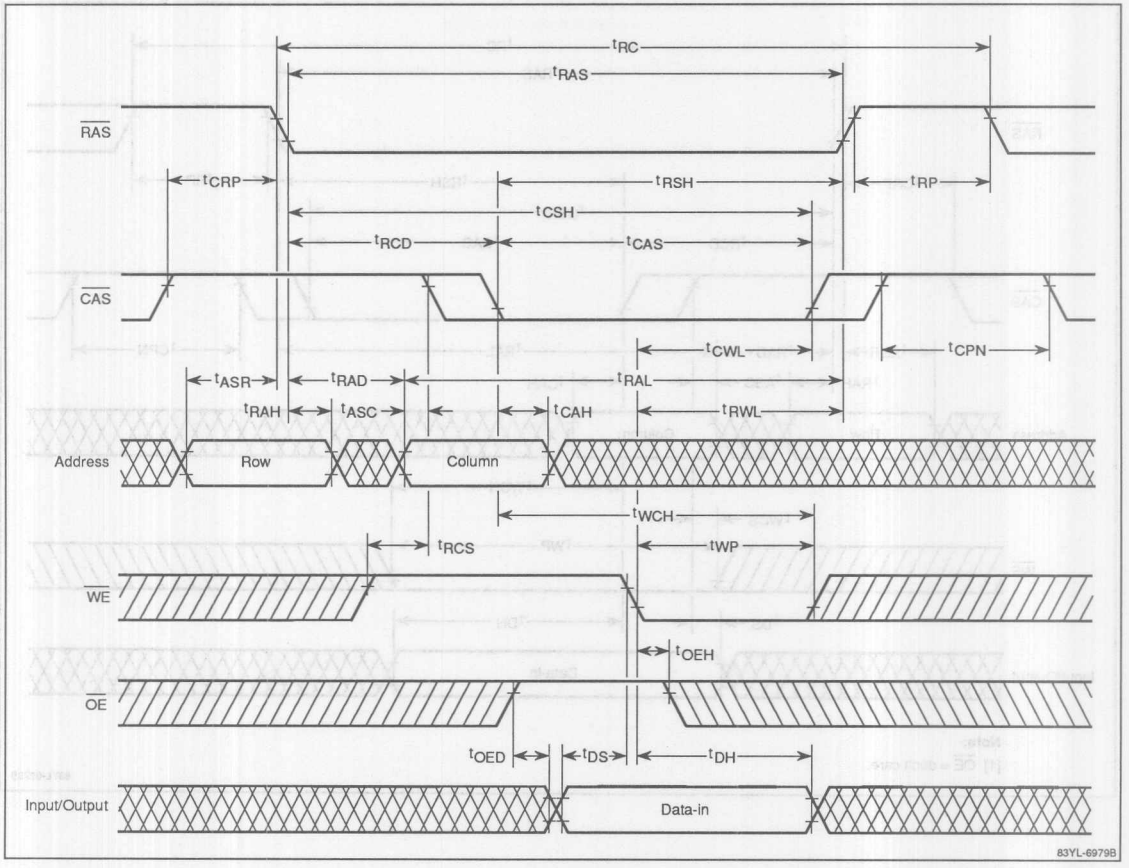
Early Write Cycle



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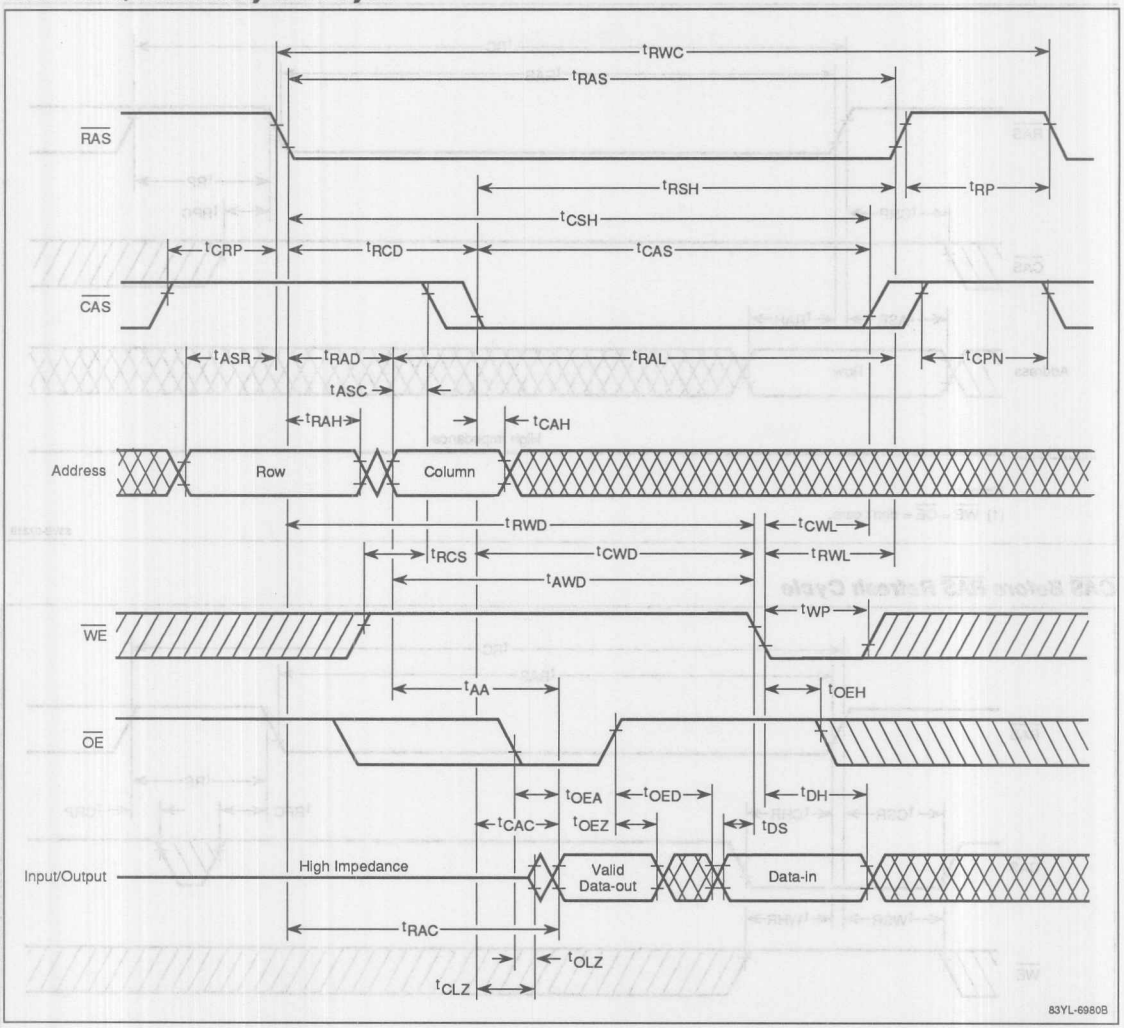
Timing Waveforms (cont)

Late Write Cycle



Timing Waveforms (cont)

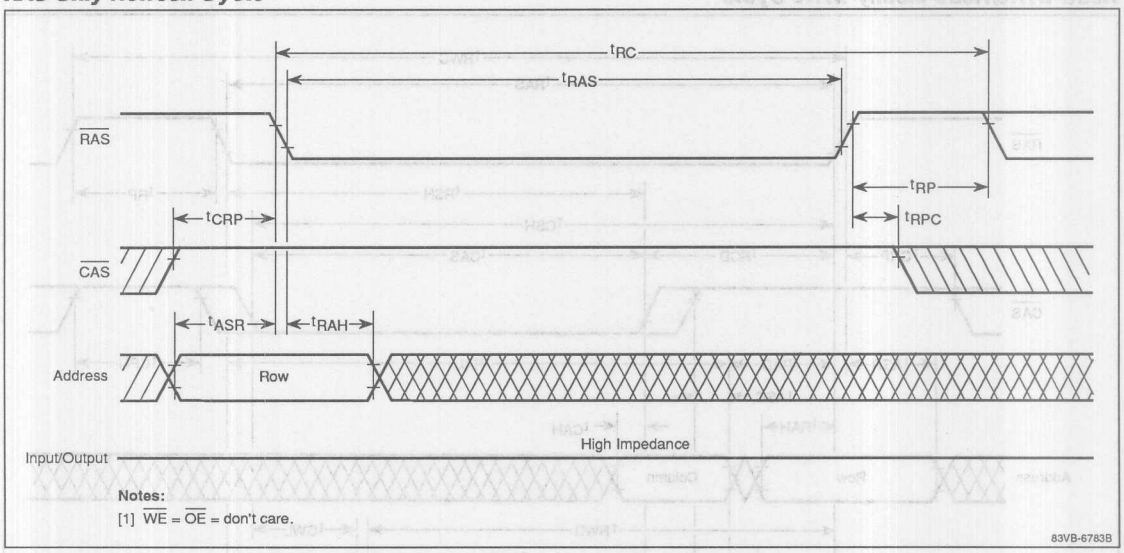
Read-Write/Read-Modify-Write Cycle



6

Timing Waveforms (cont)

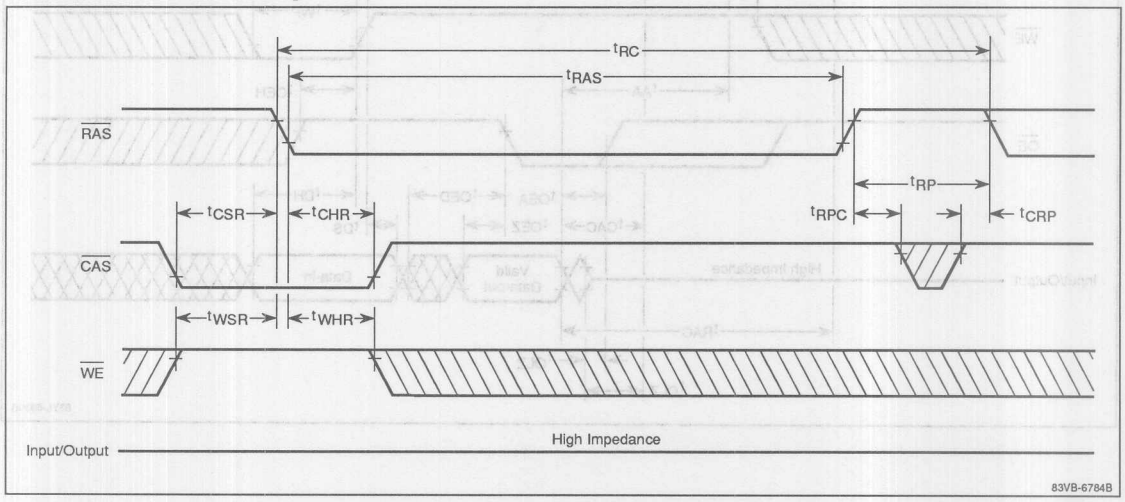
$\overline{RAS}$-Only Refresh Cycle



Notes:
[1] $\overline{WE}$ = $\overline{OE}$ = don't care.

83VB-6783B

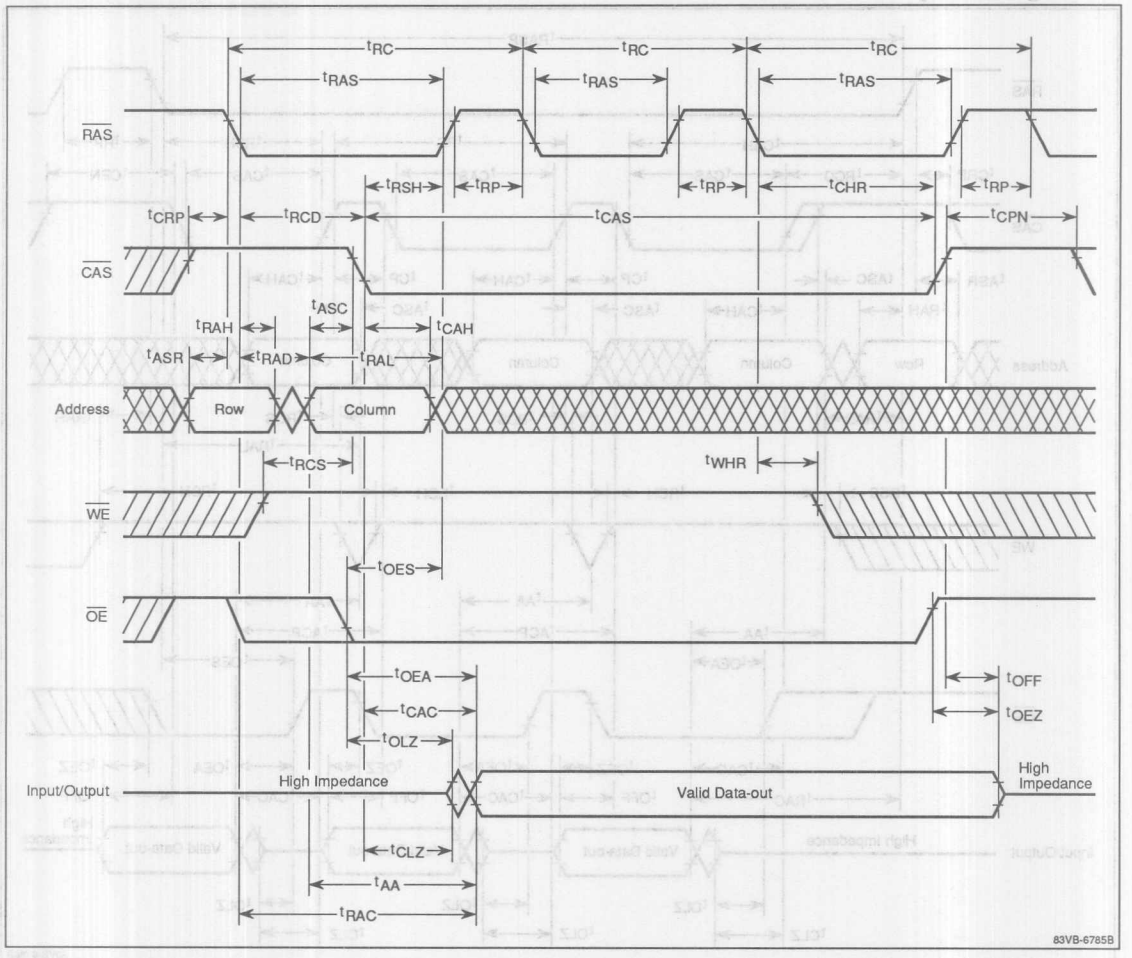
$\overline{CAS}$ Before $\overline{RAS}$ Refresh Cycle



83VB-6784B

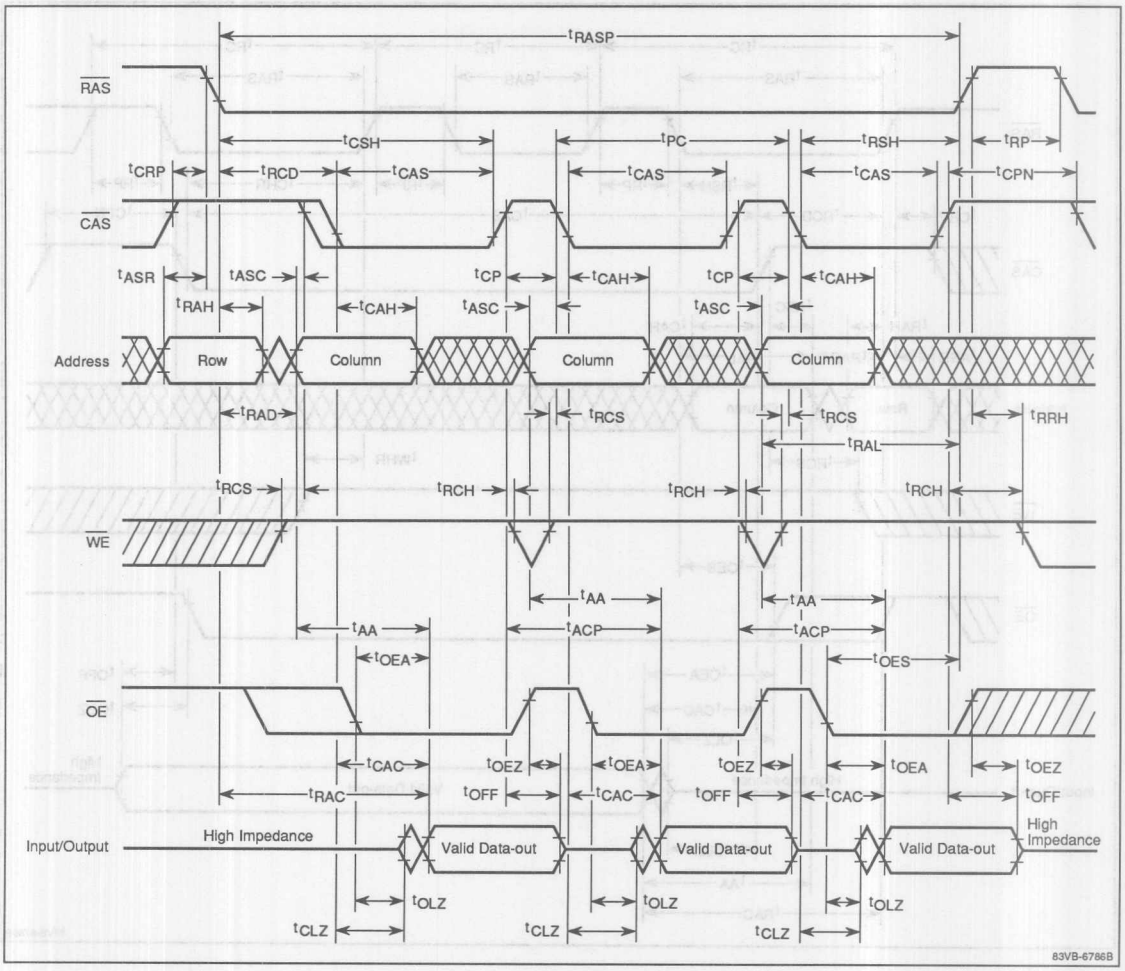
Timing Waveforms (cont)

Hidden Refresh Cycle



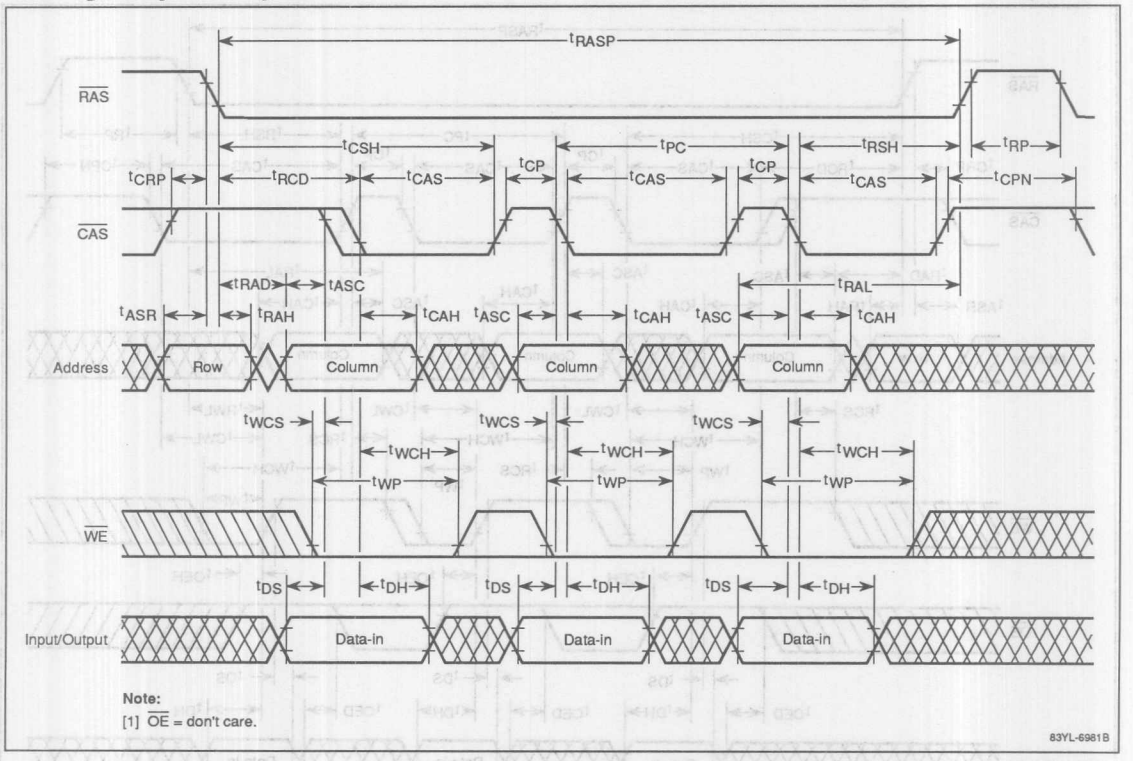
Timing Waveforms (cont)

Fast-Page Read Cycle



Timing Waveforms (cont)

Fast-Page Early Write Cycle



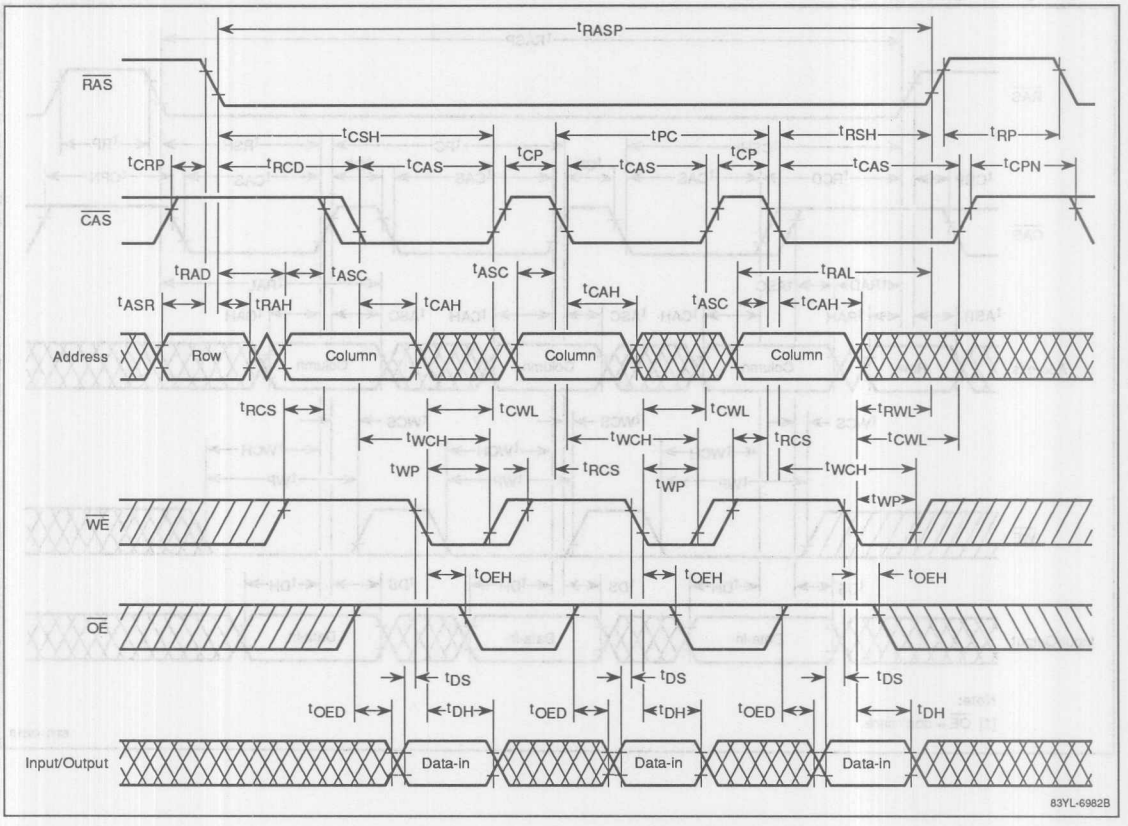
Note:
[1] $\overline{OE}$ = don't care.

83YL-6981B

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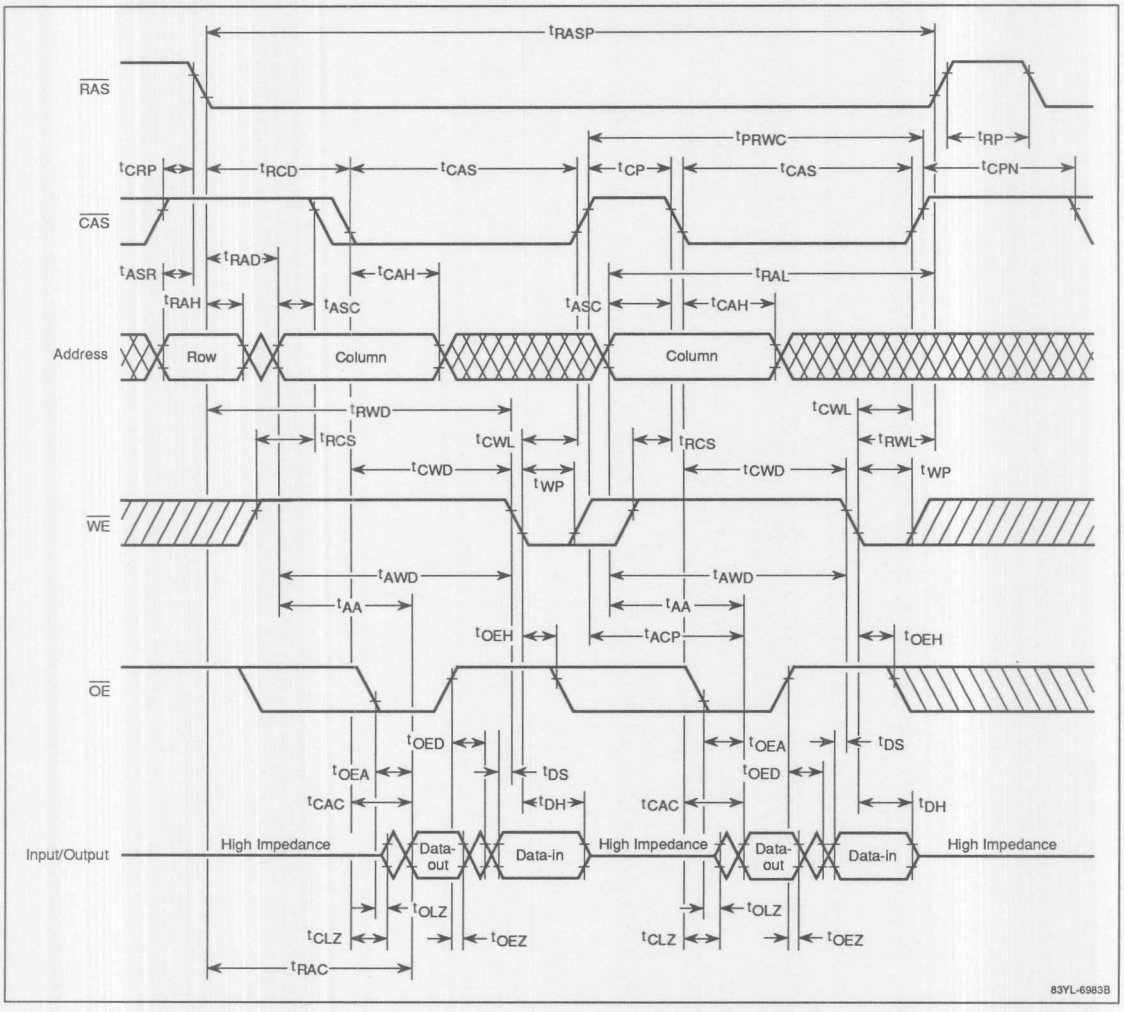
Timing Waveforms (cont)

Fast-Page Late Write Cycle

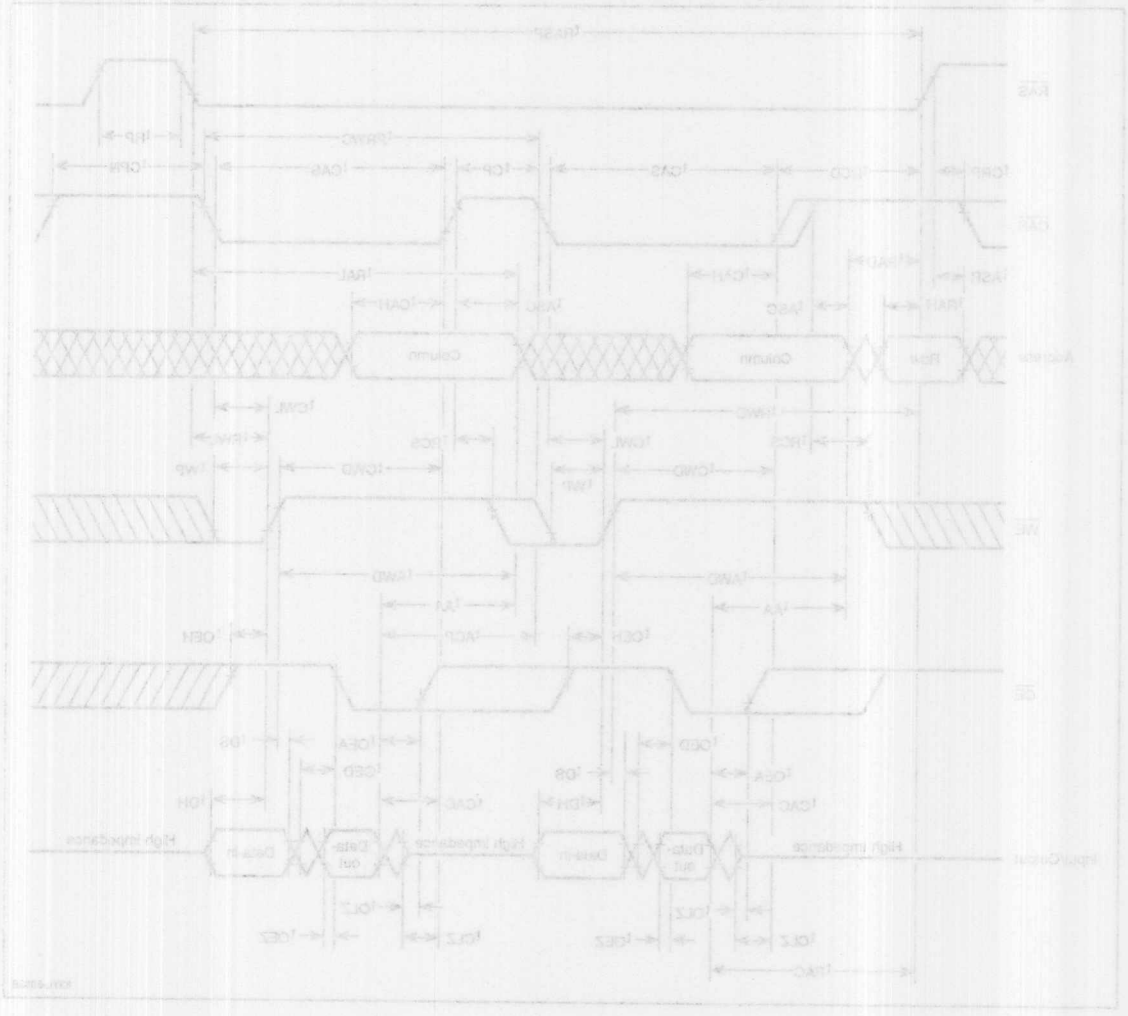


Timing Waveforms (cont)

Fast-Page Read-Write/Read-Modify-Write Cycle



6



μPD424402
1,048,576 x 4-Bit
Dynamic CMOS RAM

Description

The μPD424402 is a static-column dynamic RAM organized as 1,048,576 by 4 bits and designed to operate from a single +5-volt power supply. Advanced polycide technology using trench capacitors minimizes silicon area and provides high storage cell capacity, high performance, and high reliability. A single-transistor dynamic storage cell and CMOS circuitry throughout ensure minimum power dissipation, while an on-chip circuit internally generates the negative-voltage substrate bias —automatically and transparently.

The three-state I/O pins are controlled by $\overline{CS}$ independent of $\overline{RAS}$. After a valid read or read-modify-write cycle, data is held on the outputs by maintaining $\overline{CS}$ low. Data outputs return to high impedance when $\overline{CS}$ goes high. Static column read and write cycles can be executed by cycling $\overline{CS}$.

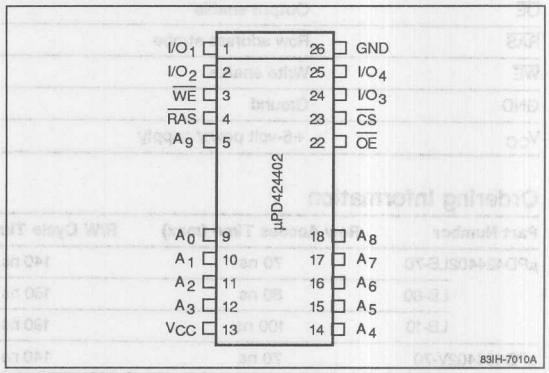
Refreshing may be accomplished by means of a $\overline{CS}$ before $\overline{RAS}$ cycle that internally generates the refresh address. Refreshing may also be accomplished by means of $\overline{RAS}$-only refresh cycles or by normal read or write cycles on the 1,024 address combinations of A_0 through A_9 during a 16-ms refresh period.

Features

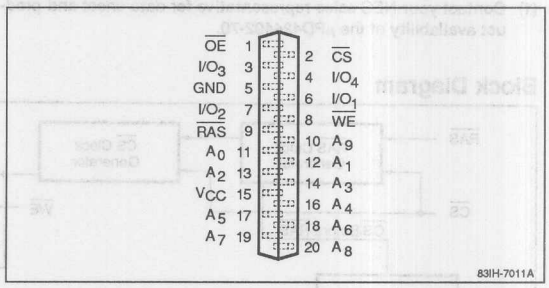
- 1,048,576 by 4-bit organization
- Single +5-volt ±10% power supply
- Static-column option
- Low power dissipation
- $\overline{CS}$ before $\overline{RAS}$ refreshing
- Multiplexed address inputs
- On-chip substrate bias generator
- TTL-compatible inputs and outputs
- Nonlatched, three-state outputs
- Low input capacitance
- 1024 refresh cycles every 16 ms
- 26/20-pin plastic SOJ or 20-pin plastic ZIP packaging

Pin Configurations

26/20-Pin Plastic SOJ



20-Pin Plastic ZIP



6

New speeds (60 and 70 ns) and packages (TSOP and 300-mil SOJ) will be available in 1991.

Pin Identification

Name	Function
A_0 - A_9	Address inputs
I/O_1 - I/O_4	Data inputs and outputs
$\overline{CS}$	Column address strobe
$\overline{OE}$	Output enable
$\overline{RAS}$	Row address strobe
$\overline{WE}$	Write enable
GND	Ground
V_{CC}	+5-volt power supply

Absolute Maximum Ratings

Voltage on any pin relative to GND	−1.0 to +7.0 V
Operating temperature, T_{OPR}	0 to +70 °C
Storage temperature, T_{STG}	−55 to +125 °C
Short-circuit output current, I_{OS}	50 mA
Power dissipation, P_D	1.0 W

Exposure to Absolute Maximum Ratings for extended periods may affect device reliability; exceeding the ratings could cause permanent damage. The device should be operated within the limits specified under DC and AC Characteristics.

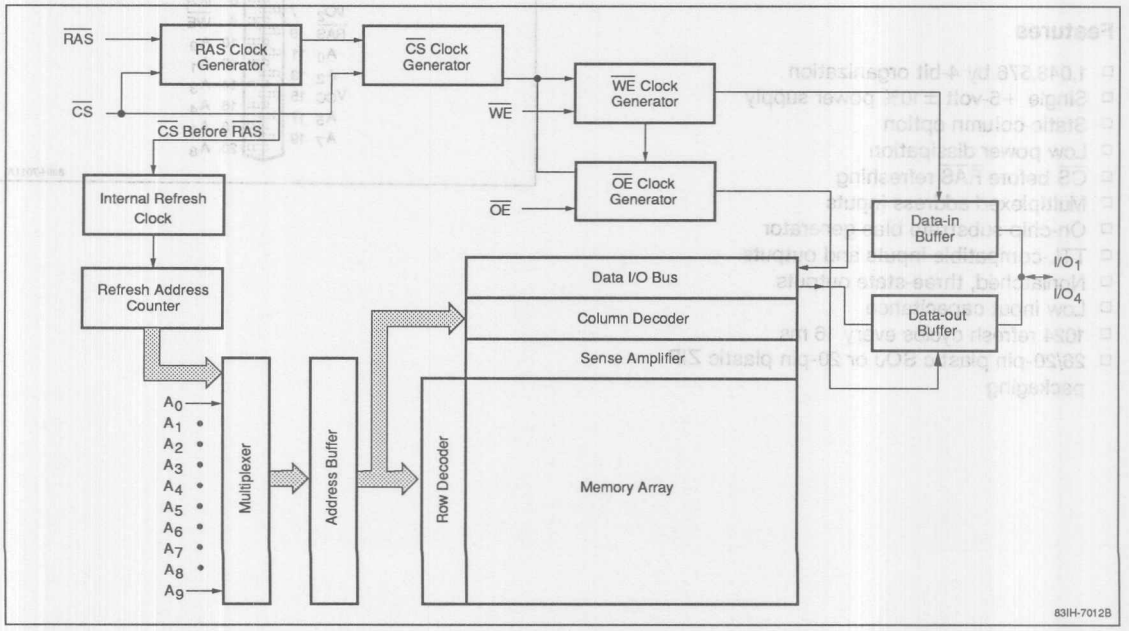
Ordering Information

Part Number	Row Access Time (max)	R/W Cycle Time (min)	Static-Column Cycle (min)	Package
μPD424402LB-70	70 ns	140 ns	40 ns	26/20-pin plastic SOJ
LB-80	80 ns	160 ns	50 ns	
LB-10	100 ns	190 ns	60 ns	
μPD424402V-70	70 ns	140 ns	40 ns	20-pin plastic ZIP
V-80	80 ns	160 ns	50 ns	
V-10	100 ns	190 ns	60 ns	

Notes:

(1) Contact your NEC sales representative for data sheet and product availability of the μPD424402-70.

Block Diagram



Recommended Operating Conditions

Parameter	Symbol	Min	Typ	Max	Unit
Input voltage, high	V_{IH}	2.4		V_{CC} + 1.0	V
Input voltage, low	V_{IL}	−1.0		0.8	V
Supply voltage	V_{CC}	4.5	5.0	5.5	V
Ambient temperature	T_A	0		70	°C

Capacitance

T_A = 25 °C; f = 1 MHz

Parameter	Symbol	Max	Unit	Pins Under Test
Input capacitance	C_{I1}	5	pF	Addresses
	C_{I2}	7	pF	$\overline{RAS}$, $\overline{CS}$, $\overline{WE}$, $\overline{OE}$
Input/output capacitance	C_O	7	pF	I/O_1 - I/O_4

DC Characteristics

T_A = 0 to +70°C; V_{CC} = +5.0 ±10%

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions
Standby current	I_{CC2}			2.0	mA	$\overline{RAS}$ = $\overline{CS}$ ≥ V_{IH} (min); I_O = 0 mA
				1.0	mA	$\overline{RAS}$ = $\overline{CS}$ ≥ V_{CC} − 0.2 V; I_O = 0 mA
Input leakage current	$I_{I(L)}$	−10		10	μA	V_{IN} = 0 V to V_{CC}; all other pins not under test = 0 V
Output leakage current	$I_{O(L)}$	−10		10	μA	D_{OUT} disabled; V_{OUT} = 0 V to V_{CC}
Output voltage, low	V_{OL}			0.4	V	I_{OL} = 4.2 mA
Output voltage, high	V_{OH}	2.4			V	I_{OH} = −5 mA

AC Characteristics

T_A = 0 to +70 °C; V_{CC} = +5.0 V ± 10%

		μPD424402-80		μPD424402-10			
Parameter	Symbol	Min	Max	Min	Max	Unit	Test Conditions
Operating current, average	I_{CC1}		90		80	mA	$\overline{RAS}$, $\overline{CS}$ cycling; t_{RC} = t_{RC} min (Note 5)
Operating current, $\overline{RAS}$-only refresh cycle, average	I_{CC3}		90		80	mA	$\overline{RAS}$ cycling; $\overline{CS}$ ≥ V_{IH} min; t_{RC} = t_{RC} min (Note 5)
Operating current, static-column cycle, average	I_{CC4}		70		60	mA	$\overline{RAS}$ ≤ V_{IL}; $\overline{CS}$ cycling; t_{RSC} = t_{RSC} min or t_{WSC} = t_{WSC} min (Note 5)
Operating current, $\overline{CS}$ before $\overline{RAS}$ refreshing, average	I_{CC5}		90		80	mA	$\overline{RAS}$ cycling; $\overline{CS}$ ≤ V_{IL} max; t_{RC} = t_{RC} min (Note 5)
Access time from column address	t_{AA}		40		50	ns	(Notes 3, 4, 7, 8)
Column address hold time referenced to $\overline{RAS}$ (rising edge)	t_{AH}	15		15		ns	
Column address setup time	t_{ASC}	0		0		ns	
Row address setup time	t_{ASR}	0		0		ns	
Column address to $\overline{WE}$ delay time	t_{AWD}	65		80		ns	(Note 15)
Access time from $\overline{CS}$ (falling edge)	t_{CAC}		20		25	ns	(Notes 3, 4, 7, 8)
Column address hold time	t_{CAH}	15		20		ns	
$\overline{CS}$ hold time for $\overline{CS}$ before $\overline{RAS}$ refreshing	t_{CHR}	15		20		ns	
$\overline{CS}$ precharge time, static-column cycle	t_{CP}	10		10		ns	
$\overline{CS}$ precharge time	t_{CPN}	10		10		ns	
$\overline{CS}$ to $\overline{RAS}$ precharge time	t_{CRP}	10		10		ns	(Note 11)
$\overline{CS}$ pulse width	t_{CS}	20	100,000	25	100,000	ns	
$\overline{CS}$ hold time	t_{CSH}	80		100		ns	
$\overline{CS}$ setup time for $\overline{CS}$ before $\overline{RAS}$ refreshing	t_{CSR}	10		10		ns	

6

AC Characteristics (cont)

Parameter	Symbol	μPD424402-80 Min	μPD424402-80 Max	μPD424402-10 Min	μPD424402-10 Max	Unit	Test Conditions
$\overline{CS}$ to $\overline{WE}$ delay	t_{CWD}	45		55		ns	(Note 15)
Write command referenced to $\overline{CS}$ lead time	t_{CWL}	15		20		ns	
Data-in hold time	t_{DH}	15		20		ns	(Note 14)
Data-in setup time	t_{DS}	0		0		ns	(Note 14)
Access time from $\overline{OE}$	t_{OEA}		20		25	ns	(Notes 3, 4, 7, 8)
$\overline{OE}$ data delay time	t_{OED}	20		25		ns	
$\overline{OE}$ command hold time	t_{OEH}	0		0		ns	
$\overline{OE}$ to $\overline{RAS}$ inactive setup time	t_{OES}	0		0		ns	
Output turnoff delay from $\overline{OE}$	t_{OEZ}	0	20	0	25	ns	(Note 10)
Output buffer turnoff delay	t_{OFF}	0	20	0	25	ns	(Note 10)
Output hold time for address	t_{OH}	5		5		ns	
Output enable time from $\overline{WE}$	t_{OW}		25		30	ns	
Access time from $\overline{WE}$	t_{PWA}		90		110	ns	(Notes 7, 16)
Column address hold time referenced to $\overline{WE}$	t_{PWH}	90		110		ns	
Access time from $\overline{RAS}$	t_{RAC}		80		100	ns	(Notes 3, 4, 7, 8)
$\overline{RAS}$ to column address delay time	t_{RAD}	17	40	17	50	ns	(Note 9)
Row address hold time	t_{RAH}	12		12		ns	
Column address lead time referenced to $\overline{RAS}$ (rising edge)	t_{RAL}	40		50		ns	
$\overline{RAS}$ pulse width	t_{RAS}	80	10,000	100	10,000	ns	
$\overline{RAS}$ pulse width, static-column cycle	t_{RASC}	80	100,000	100	100,000	ns	
Random read or write cycle time	t_{RC}	160		190		ns	(Note 6)
$\overline{RAS}$ to $\overline{CS}$ delay time	t_{RCD}	25	60	25	75	ns	(Note 8)
Read command hold time referenced to $\overline{CS}$	t_{RCH}	0		0		ns	(Note 12)
Read command setup time	t_{RCS}	0		0		ns	
Refresh period	t_{REF}		16		16	ms	Address A_0 through A_9
$\overline{RAS}$ precharge time	t_{RP}	70		80		ns	
$\overline{RAS}$ precharge $\overline{CS}$ hold time	t_{RPC}	10		10		ns	
Read command hold time referenced to $\overline{RAS}$	t_{RRH}	10		10		ns	(Note 12)
Read cycle time	t_{RSC}	50		60		ns	
$\overline{RAS}$ hold time	t_{RSH}	20		25		ns	
$\overline{RAS}$ to second $\overline{WE}$ delay time	t_{RSW}	95		115		ns	
Read-modify-write cycle time	t_{RWC}	210		250		ns	(Note 6)
$\overline{RAS}$ to $\overline{WE}$ delay	t_{RWD}	105		130		ns	(Note 15)
Write command referenced to $\overline{RAS}$ lead time	t_{RWL}	20		25		ns	
Read/write cycle time	t_{RWSC}	120		145		ns	
Rise and fall transition time	t_T	3	50	3	50	ns	(Note 4)
$\overline{WE}$ to column address delay time	t_{WAD}	20	45	25	55	ns	(Note 16)
Write command hold time	t_{WCH}	15		20		ns	(Note 13)
Write command setup time	t_{WCS}	0		0		ns	(Note 15)

AC Characteristics (cont)

Parameter	Symbol	μPD424402-80 Min	μPD424402-80 Max	μPD424402-10 Min	μPD424402-10 Max	Unit	Test Conditions
$\overline{WE}$ command hold time for $\overline{CS}$ before $\overline{RAS}$ refreshing	t_{WHR}	15		20		ns	
Write invalid time	t_{WI}	10		10		ns	
Write command pulse width	t_{WP}	15		20		ns	(Note 13)
Write cycle time	t_{WSC}	50		60		ns	
$\overline{WE}$ command setup time for $\overline{CS}$ before $\overline{RAS}$ refreshing	t_{WSR}	10		10		ns	

Notes:

(1) All voltages are referenced to GND.

(2) An initial pause of 100 μs is required after power-up, followed by any eight $\overline{RAS}$ cycles, before proper device operation is achieved. At the end of the initial power up sequence, it is recommended that either a $\overline{RAS}$-only refresh or a $\overline{CS}$ before $\overline{RAS}$ refresh cycle be executed while $\overline{WE} \geq V_{IH}$ to ensure normal operation.

(3) AC measurements assume $t_T = 5$ ns.

(4) V_{IH} (min) and V_{IL} (max) are reference levels for measuring the timing of input signals. Transition times are measured between V_{IH} and V_{IL}.

(5) I_{CC1}, I_{CC3}, I_{CC4}, and I_{CC5} depend on output loading and cycle rates. Specified values are obtained with the output open. I_{CC3} is measured assuming that all column address inputs are held at either a high level or a low level during $\overline{RAS}$-only refresh cycles. I_{CC4} is measured assuming that all column address inputs are switched only once during each static column cycle.

(6) The minimum specifications are used only to indicate the cycle time at which proper operation over the full temperature range ($T_A = 0$ to $+70$ °C) is assured.

(7) Load = 2 TTL (−1 mA, +4 mA) loads and 100 pF ($V_{OH} = 2.0$ V and $V_{OL} = 0.8$ V).

(8) If $t_{RCD} \leq$ exceeds t_{RAD} max, then t_{RAC} will increase by the amount t_{RCD} exceeds t_{RCD} (max).

(9) If $t_{RAD} \geq t_{RAD}$ (max), then the access time is defined by t_{AA}.

(10) t_{OFF} (max) and t_{OEZ} (max) define the time at which the outputs achieve the open-circuit condition and are not referenced to V_{OH} or V_{OL}.

(11) The t_{CRP} requirement should be applicable for $\overline{RAS}/\overline{CS}$ cycles preceded by any cycle.

(12) Either t_{RRH} or t_{RCH} must be satisfied for a read cycle.

(13) Parameter t_{WP} is applicable for a delayed write cycle such as a read-write/read-modify-write cycle. For early write cycles, both t_{WCS} and t_{WCH} must be met.

(14) These parameters are referenced to the falling edge of $\overline{CS}$ for early write cycles and to the falling edge of $\overline{WE}$ for delayed write or read-modify-write cycles.

(15) t_{WCS}, t_{RWD}, t_{CWD}, and t_{AWD} are restrictive operating parameters in read-write/read-modify-write cycles only. If $t_{WCS} \geq t_{WCS}$ (min), the cycle is an early write cycle and the data I/O pins will remain open-circuit throughout the entire cycle. If $t_{CWD} \geq t_{CWD}$ (min), $t_{RWD} \geq t_{RWD}$ (min), and $t_{AWD} \geq t_{AWD}$ (min), then the cycle is a read-write cycle and the data I/O pins will contain data read from the selected cells. If neither of the above conditions is met, the condition of the data I/O pins (at access time and until $\overline{CS}$ returns to V_{IH}) is indeterminate.

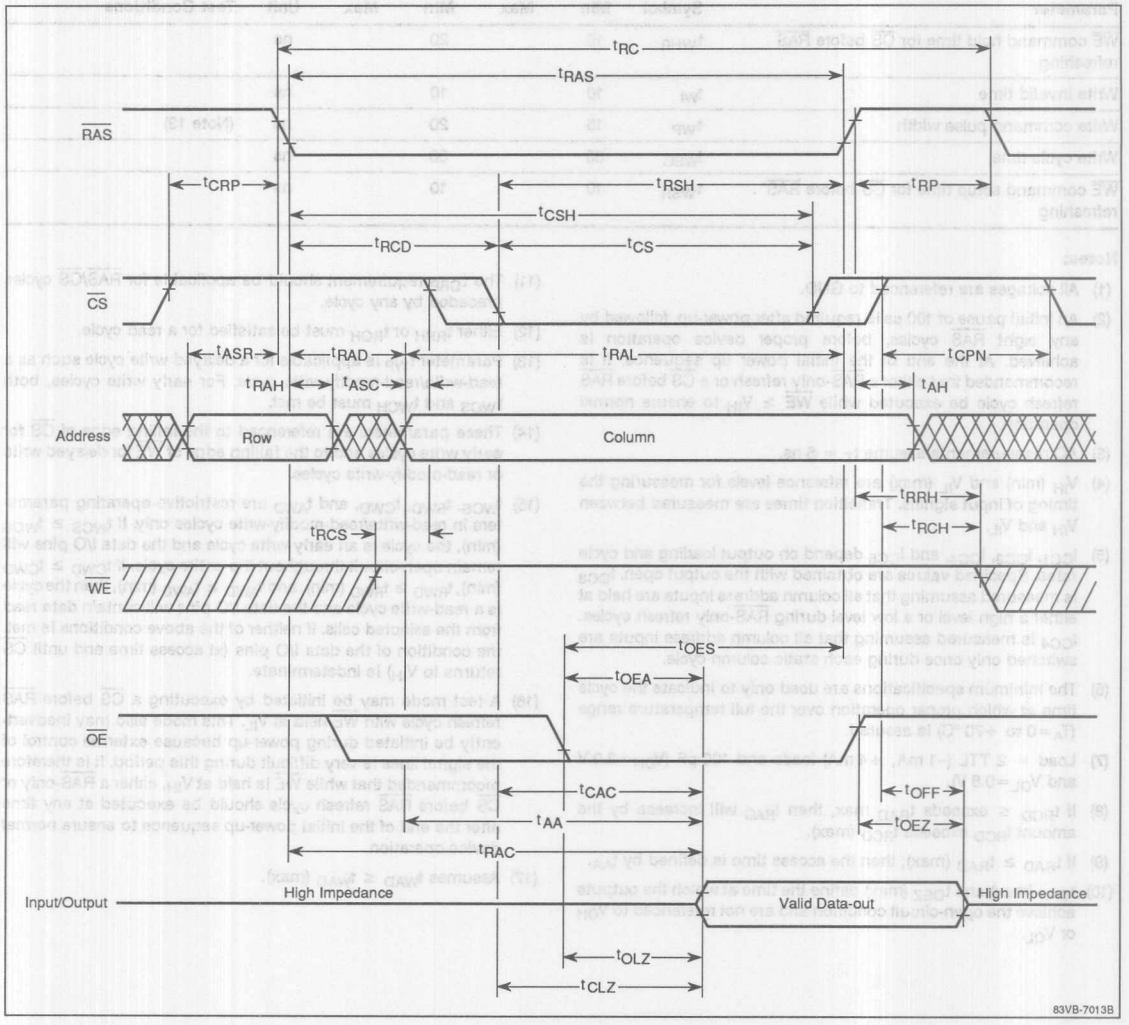
(16) A test mode may be initiated by executing a $\overline{CS}$ before $\overline{RAS}$ refresh cycle with $\overline{WE}$ held at V_{IL}. This mode also may inadvertently be initiated during power-up because external control of the signal lines is very difficult during this period. It is therefore recommended that while $\overline{WE}$ is held at V_{IH}, either a $\overline{RAS}$-only or $\overline{CS}$ before $\overline{RAS}$ refresh cycle should be executed at any time after the end of the initial power-up sequence to ensure normal device operation.

(17) Assumes $t_{WAD} \leq t_{WAD}$ (max).

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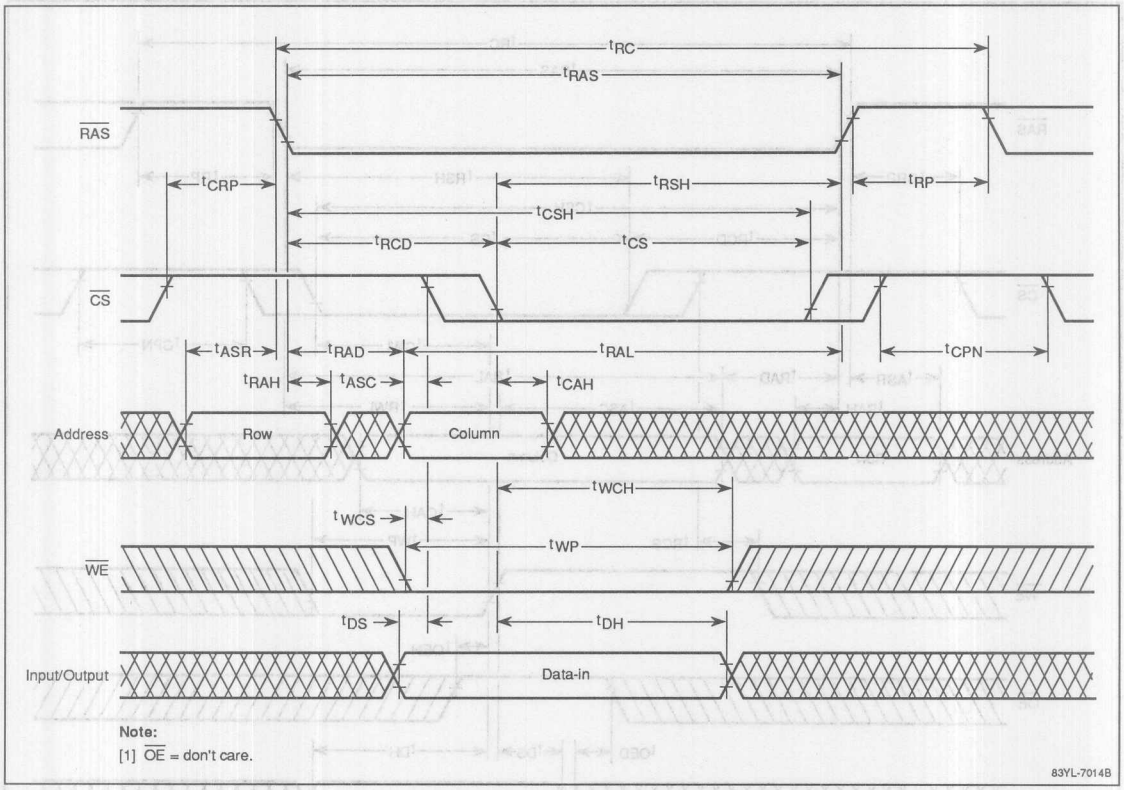
Timing Waveforms

Read Cycle



Timing Waveforms (cont)

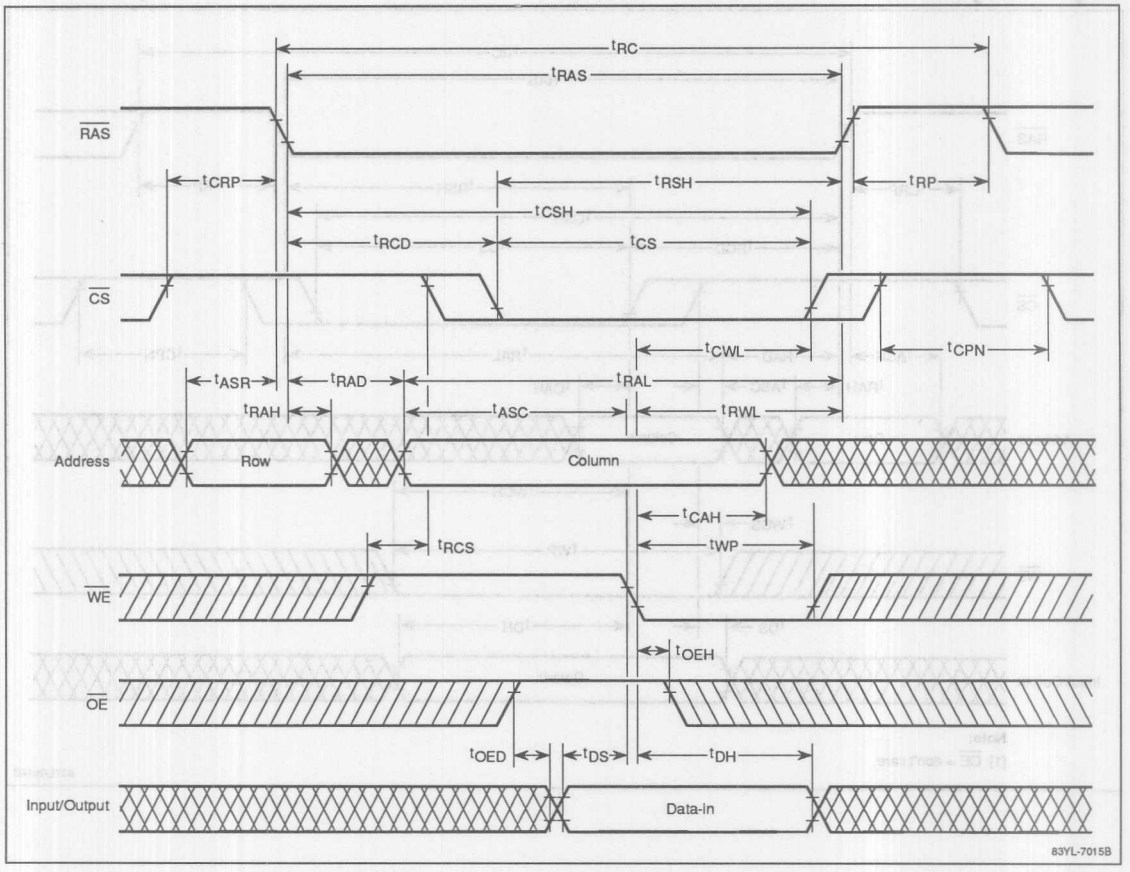
Early Write Cycle



Note:
[1] $\overline{OE}$ = don't care.

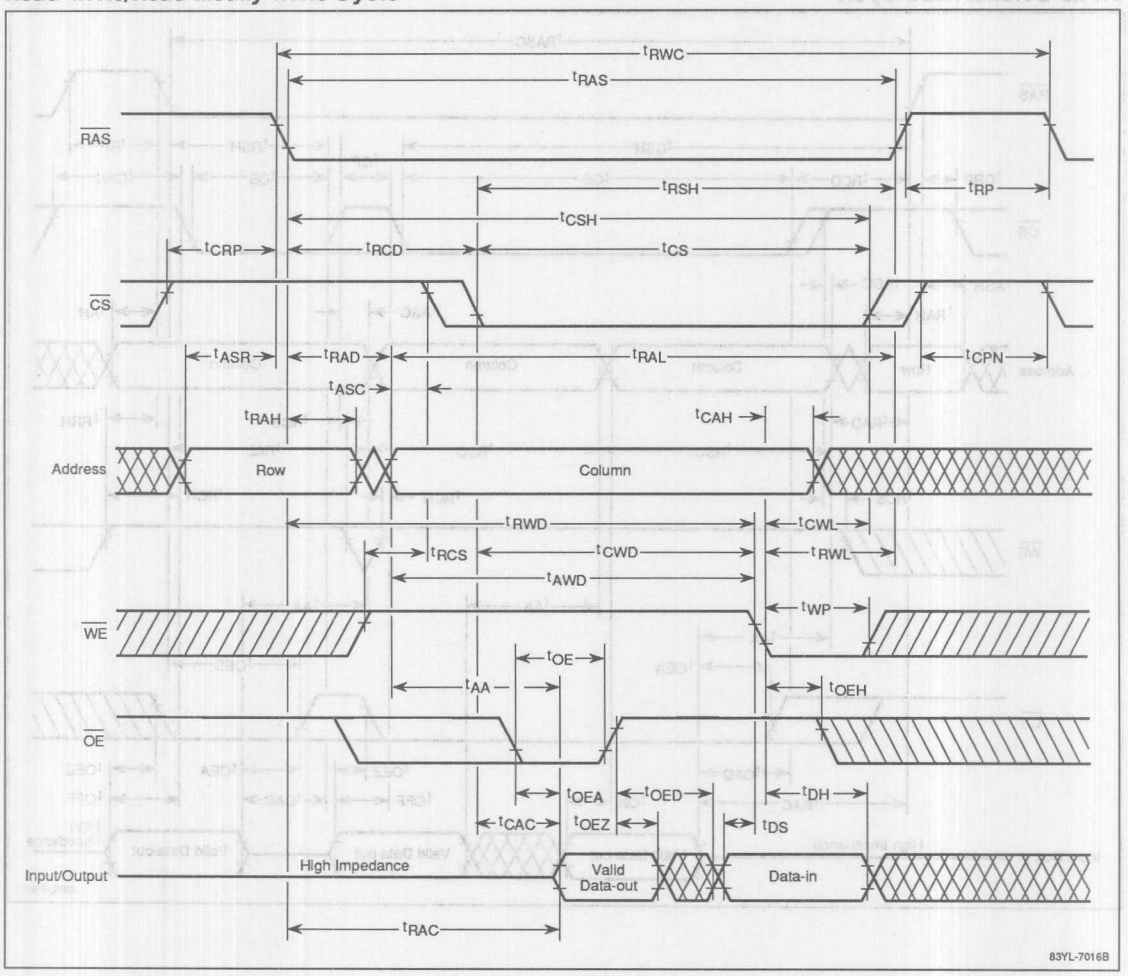
Timing Waveforms (cont)

Late Write Cycle



Timing Waveforms (cont)

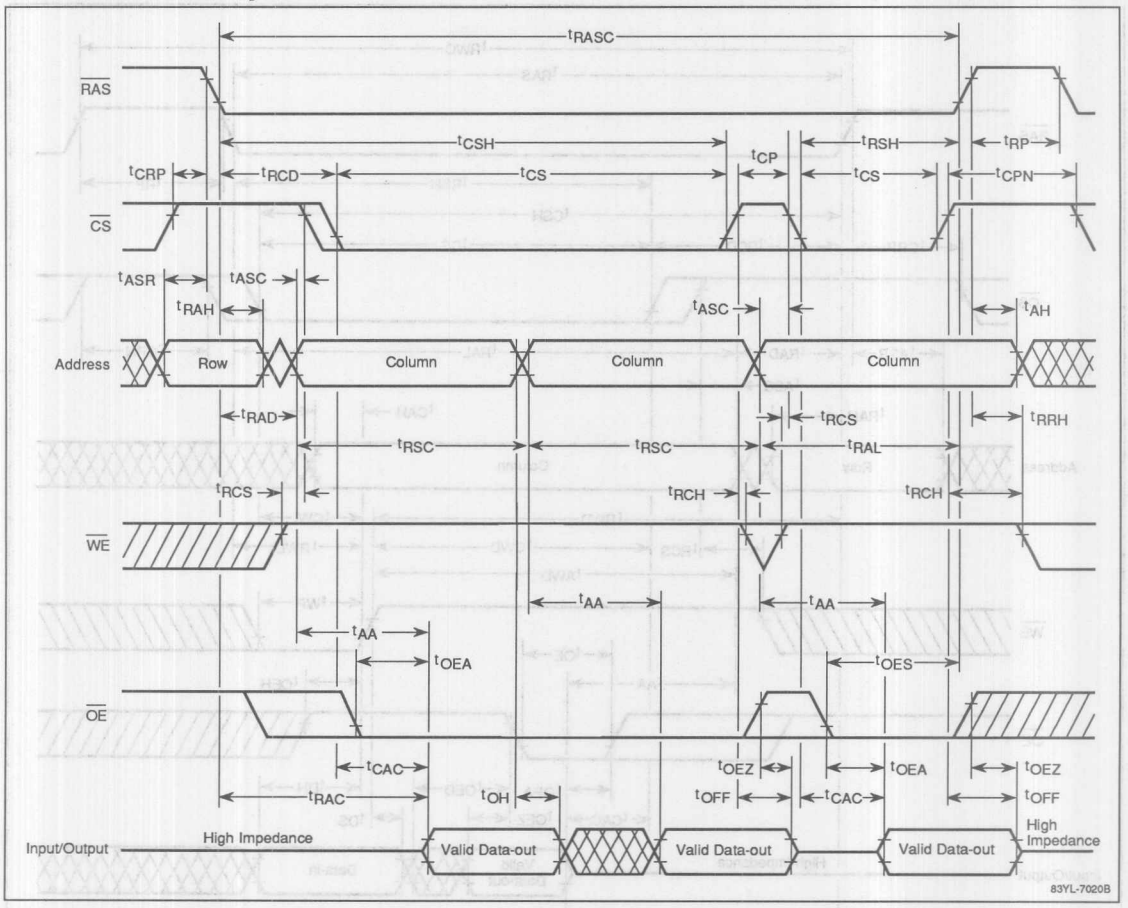
Read-Write/Read-Modify-Write Cycle



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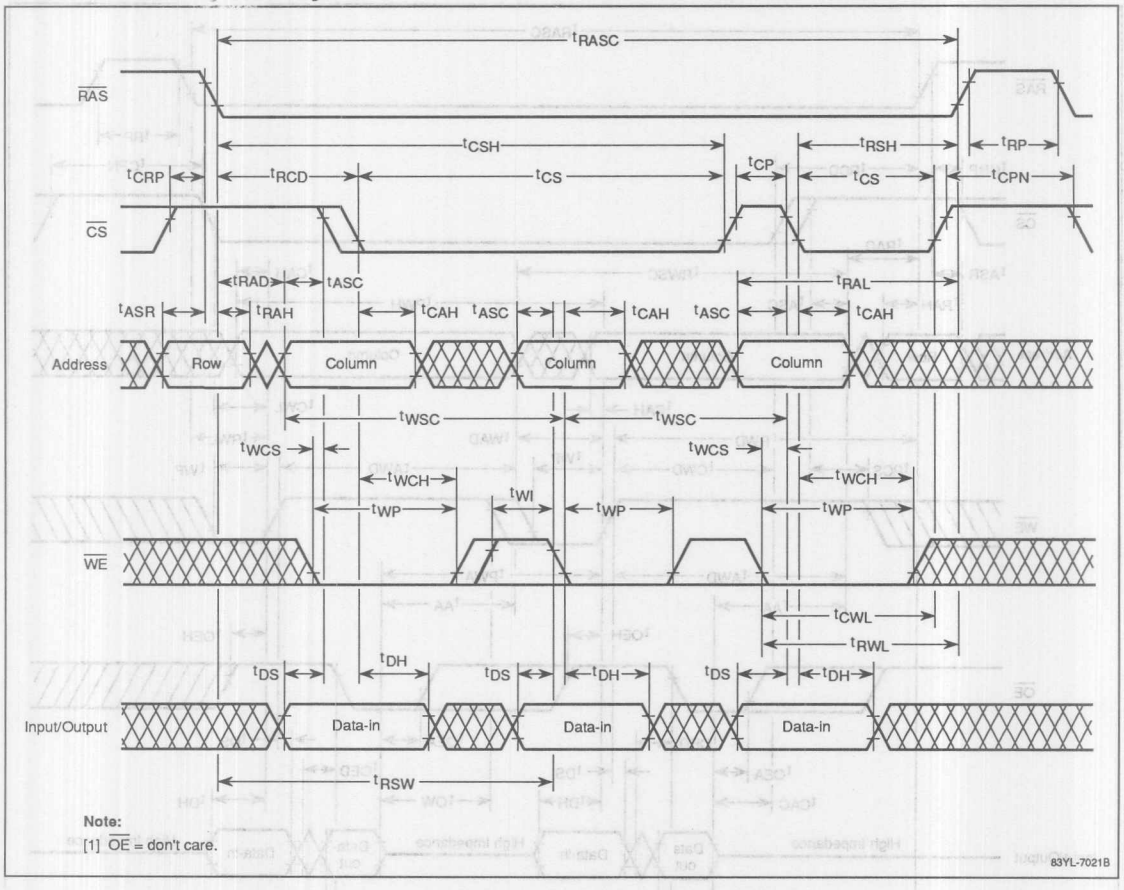
Timing Waveforms (cont)

Static-Column Read Cycle



Timing Waveforms (cont)

Static-Column Early Write Cycle



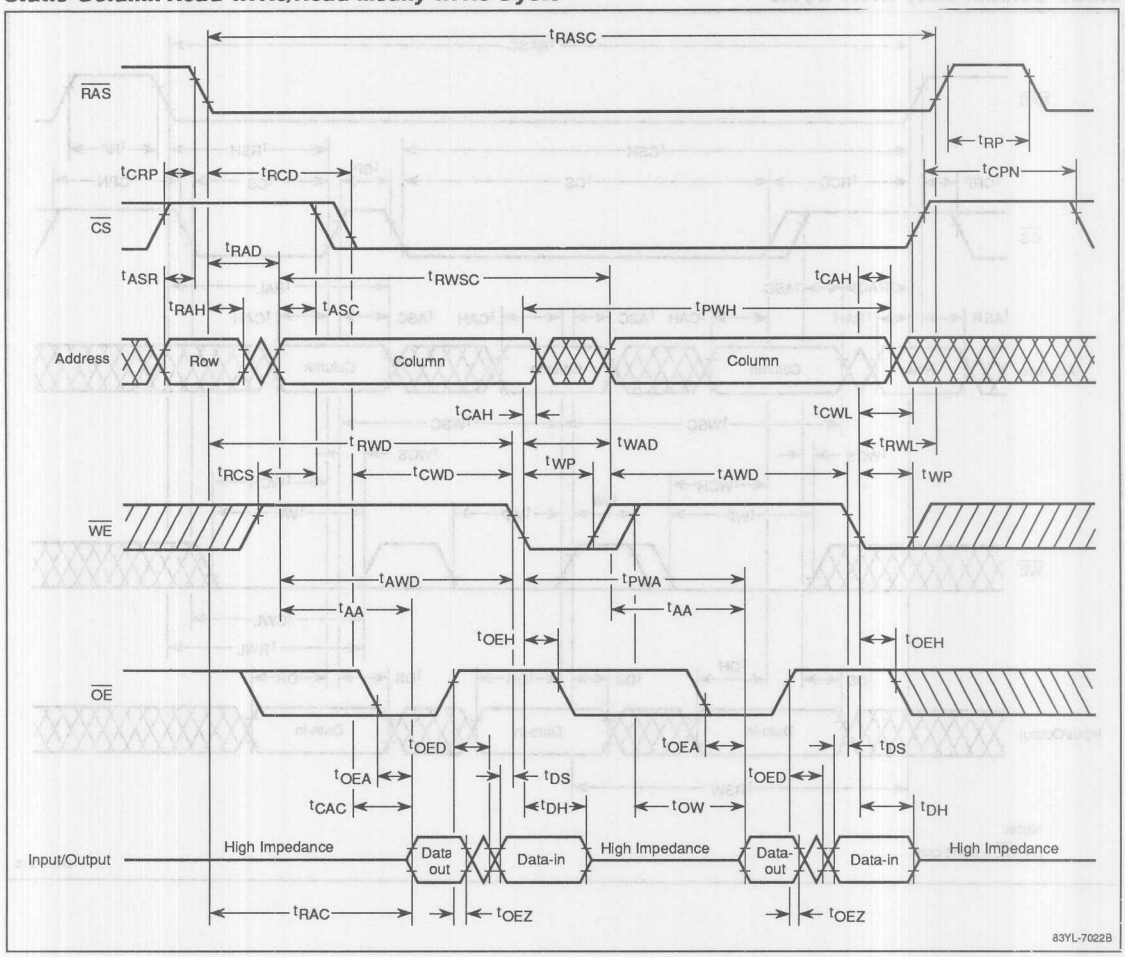
Note:
[1] $\overline{OE}$ = don't care.

83YL-7021B

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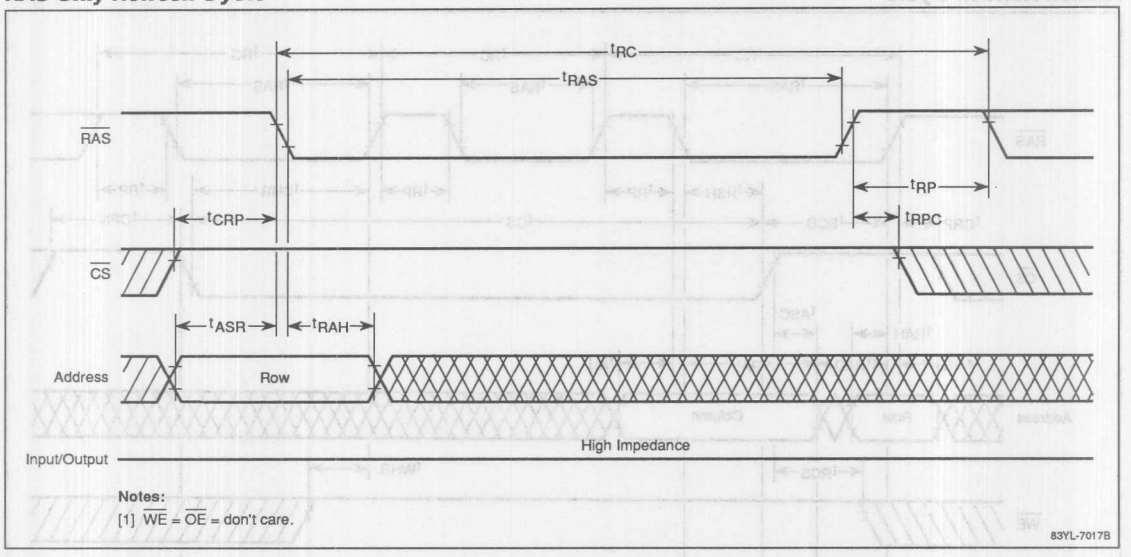
Timing Waveforms (cont)

Static-Column Read-Write/Read-Modify-Write Cycle



Timing Waveforms (cont)

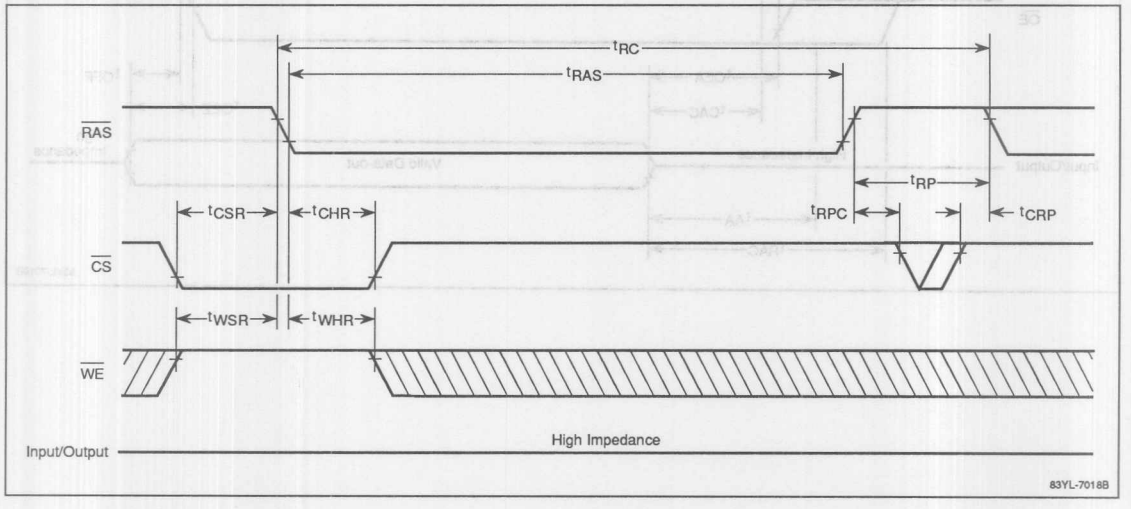
$\overline{RAS}$-Only Refresh Cycle



Notes:
[1] $\overline{WE}$ = $\overline{OE}$ = don't care.

83YL-7017B

$\overline{CS}$ Before $\overline{RAS}$ Refresh Cycle

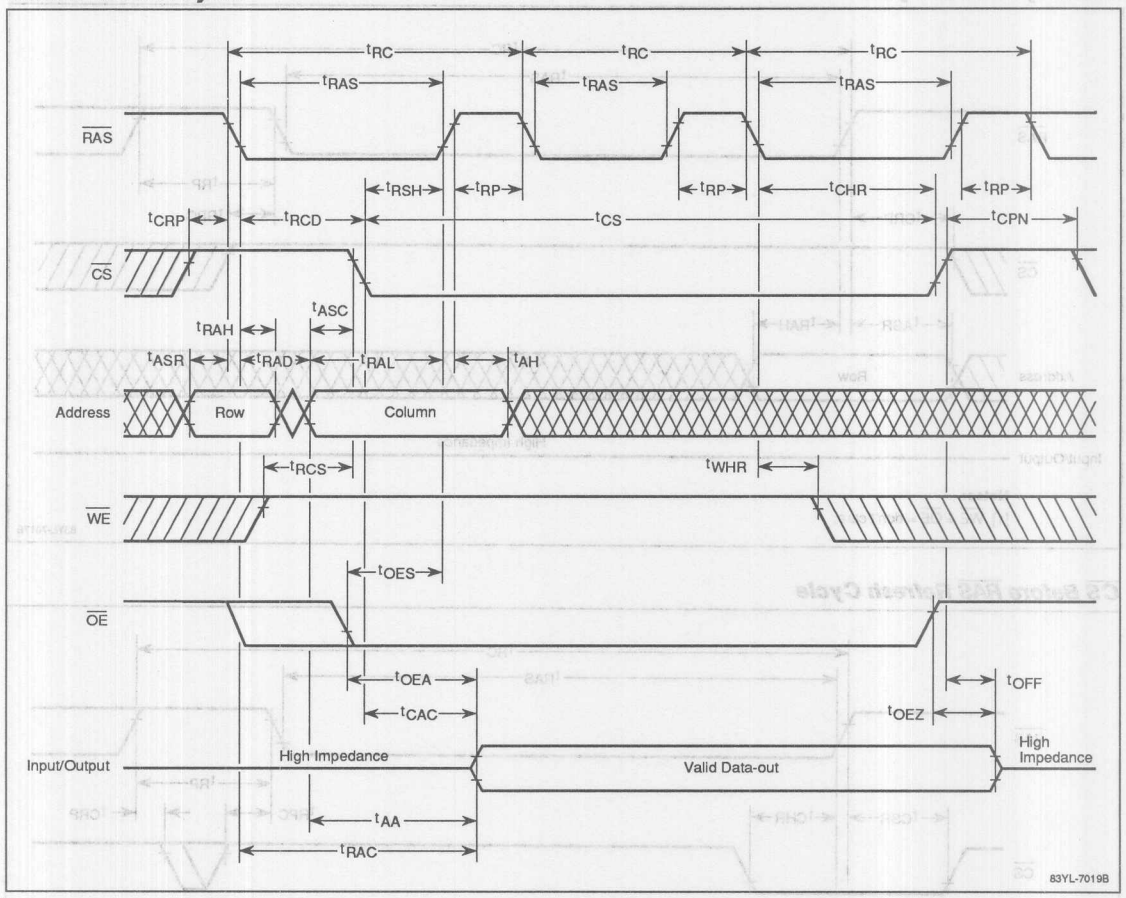


83YL-7018B

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Timing Waveforms (cont)

Hidden Refresh Cycle



μPD424410
1,048,576 x 4-Bit
Dynamic CMOS RAM

Description

The μPD424410 is a 1,048,576 by 4-bit dynamic RAM designed with a write-per-bit option to operate from a single + 5-volt power supply. Advanced polycide technology using trench capacitors minimizes silicon area and provides high storage cell capacity, high performance, and high reliability. A single-transistor dynamic storage cell and CMOS circuitry throughout ensure minimum power dissipation, while an on-chip circuit internally generates the negative-voltage substrate bias—automatically and transparently.

The three-state I/O pins are controlled by $\overline{CAS}$ independent of $\overline{RAS}$. After a valid read or read-modify-write cycle, data is held on the outputs by maintaining $\overline{CAS}$ low. Data outputs return to high impedance when $\overline{CAS}$ goes high. Fast-page read and write cycles can be executed by cycling $\overline{CAS}$.

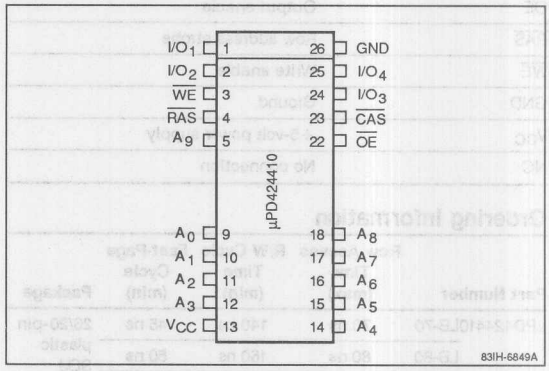
Refreshing may be accomplished by means of a $\overline{CAS}$ before $\overline{RAS}$ cycle that internally generates the refresh address. Refreshing may also be accomplished by means of $\overline{RAS}$-only refresh cycles or by normal read or write cycles on the 1,024 address combinations of A_0 through A_9 during a 16-ms refresh period.

Features

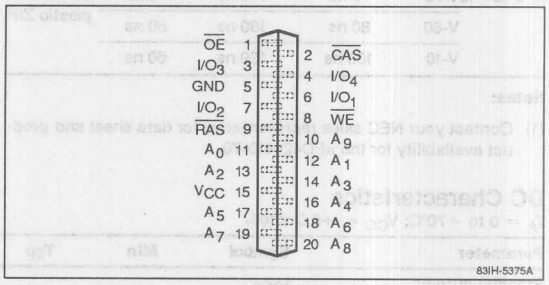
- 1,048,576 by 4-bit organization
- Single + 5-volt ±10% power supply
- Write-per-bit option
- Fast-page option
- Low power dissipation
- $\overline{CAS}$ before $\overline{RAS}$ internal refreshing
- Multiplexed address inputs
- On-chip substrate bias generator
- TTL-compatible inputs and outputs
- Nonlatched, three-state outputs
- Low input capacitance
- 1024 refresh cycles every 16 ms
- High-density 26/20-pin plastic SOJ or 20-pin plastic ZIP packaging

Pin Configurations

26/20-Pin Plastic SOJ



20-Pin Plastic ZIP



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Pin Identification

Name	Function
A_0 - A_9	Address inputs
I/O_1 - I/O_4	Data inputs and outputs
$\overline{CAS}$	Column address strobe
$\overline{OE}$	Output enable
$\overline{RAS}$	Row address strobe
$\overline{WE}$	Write enable
GND	Ground
V_{CC}	+5-volt power supply
NC	No connection

Ordering Information

Part Number	Row Access Time (max)	R/W Cycle Time (min)	Fast-Page Cycle (min)	Package
μPD424410LB-70	70 ns	140 ns	45 ns	26/20-pin plastic SOJ
LB-80	80 ns	160 ns	50 ns	
LB-10	100 ns	190 ns	60 ns	
μPD424410V-70	70 ns	140 ns	45 ns	20-pin plastic ZIP
V-80	80 ns	160 ns	50 ns	
V-10	100 ns	190 ns	60 ns	

Notes:

(1) Contact your NEC sales representative for data sheet and product availability for the μPD424410-70.

Absolute Maximum Ratings

Voltage on any pin relative to GND, V_T	−1.0 to +7.0 V
Operating temperature, T_{OPR}	0 to +70 °C
Storage temperature, T_{STG}	−55 to +125 °C
Short-circuit output current, I_{OS}	50 mA
Power dissipation, P_D	1.0 W

Exposure to Absolute Maximum Ratings for extended periods may affect device reliability; exceeding the ratings could cause permanent damage. The device should be operated within the limits specified under DC and AC Characteristics.

Recommended Operating Conditions

Parameter	Symbol	Min	Typ	Max	Unit
Input voltage, high	V_{IH}	2.4		V_{CC} + 1.0	V
Input voltage, low	V_{IL}	−1.0		0.8	V
Supply voltage	V_{CC}	4.5	5.0	5.5	V
Ambient temperature	T_A	0		70	°C

Capacitance

T_A = 25 °C; f = 1 MHz

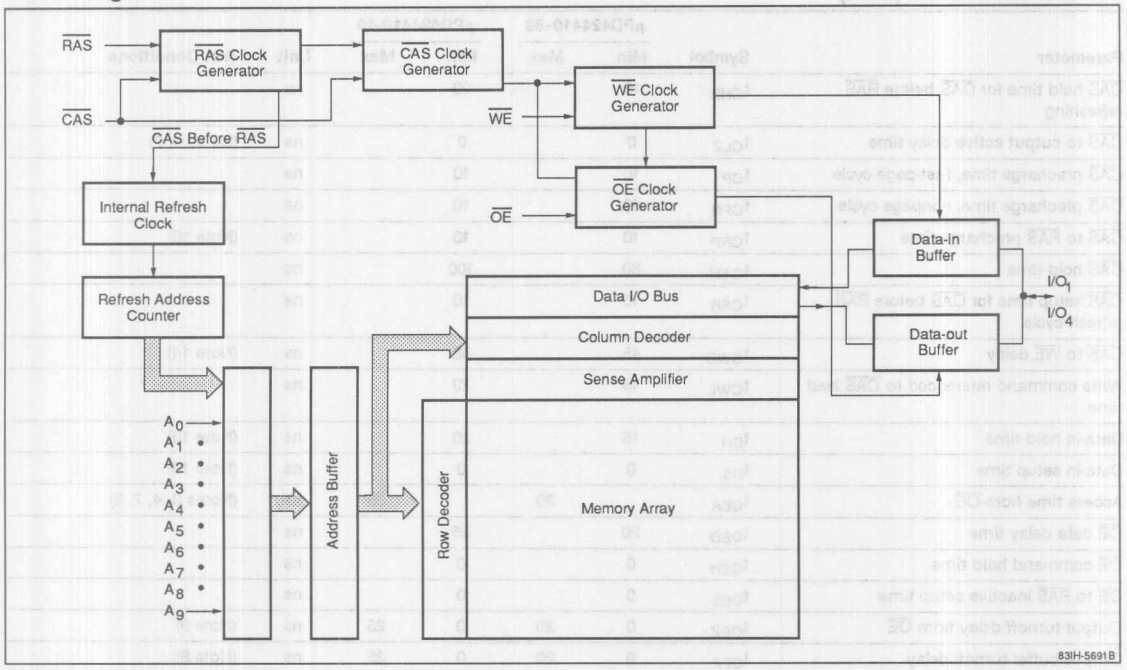
Parameter	Symbol	Max	Unit	Pins Under Test
Input capacitance	C_{I1}	5	pF	Addresses
	C_{I2}	7	pF	$\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$, $\overline{OE}$
Input/output capacitance	C_D	7	pF	I/O_1 – I/O_4

DC Characteristics

T_A = 0 to +70°C; V_{CC} = +5.0 ±10%

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions
Standby current	I_{CC2}			2.0	mA	$\overline{RAS} \geq V_{IH}$ (min); I_O = 0 mA
				1.0	mA	$\overline{RAS} = \overline{CAS} \geq V_{CC}$ – 0.2 V; I_O = 0 mA
Input leakage current	$I_{I(L)}$	−10		10	μA	V_{IN} = 0 V to V_{CC}; all other pins not under test = 0 V
Output leakage current	$I_{O(L)}$	−10		10	μA	D_{OUT} disabled; V_{OUT} = 0 V to V_{CC}
Output voltage, low	V_{OL}			0.4	V	I_{OL} = 4.2 mA
Output voltage, high	V_{OH}	2.4			V	I_{OH} = −5 mA

Block Diagram



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AC Characteristics

T_A = 0 to +70 °C; V_{CC} = +5.0 V ± 10%

Parameter	Symbol	μPD424410-80 Min	μPD424410-80 Max	μPD424410-10 Min	μPD424410-10 Max	Unit	Test Conditions
Operating current, average	I_{CC1}		90		80	mA	$\overline{RAS}$, $\overline{CAS}$ cycling; $t_{RC} = t_{RC}$ min (Note 5)
Operating current, $\overline{RAS}$-only refresh cycle, average	I_{CC3}		90		80	mA	$\overline{RAS}$ cycling; $\overline{CAS} \geq V_{IH}$ min; $t_{RC} = t_{RC}$ min (Note 5)
Operating current, fast-page cycle, average	I_{CC4}		70		60	mA	$\overline{RAS} \leq V_{IL}$; $\overline{CAS}$ cycling; $t_{PC} = t_{PC}$ min (Note 5)
Operating current, $\overline{CAS}$ before $\overline{RAS}$ refresh cycle, average	I_{CC5}		90		80	mA	$\overline{RAS}$ cycling; $\overline{CAS} \leq V_{IL}$ max; $t_{RC} = t_{RC}$ min (Note 5)
Access time from column address	t_{AA}		40		50	ns	(Notes 3, 4, 7, 8)
Access time from $\overline{CAS}$ precharge (rising edge)	t_{ACP}		45		55	ns	(Notes 3, 4, 7, 8)
Column address setup time	t_{ASC}	0		0		ns	
Row address setup time	t_{ASR}	0		0		ns	
Column address to $\overline{WE}$ delay time	t_{AWD}	65		80		ns	(Note 14)
Access time from $\overline{CAS}$ (falling edge)	t_{CAC}		20		25	ns	(Notes 3, 4, 7, 8)
Column address hold time	t_{CAH}	15		20		ns	
$\overline{CAS}$ pulse width	t_{CAS}	20	10,000	25	10,000	ns	

AC Characteristics (cont)

Parameter	Symbol	μPD424410-80 Min	μPD424410-80 Max	μPD424410-10 Min	μPD424410-10 Max	Unit	Test Conditions
$\overline{CAS}$ hold time for $\overline{CAS}$ before $\overline{RAS}$ refreshing	t_{CHR}	15		20		ns	
$\overline{CAS}$ to output active delay time	t_{CLZ}	0		0		ns	(Notes 4, 7)
$\overline{CAS}$ precharge time, fast-page cycle	t_{CP}	10		10		ns	
$\overline{CAS}$ precharge time, nonpage cycle	t_{CPN}	10		10		ns	
$\overline{CAS}$ to $\overline{RAS}$ precharge time	t_{CRP}	10		10		ns	(Note 10)
$\overline{CAS}$ hold time	t_{CSH}	80		100		ns	
$\overline{CAS}$ setup time for $\overline{CAS}$ before $\overline{RAS}$ refresh cycle	t_{CSR}	10		10		ns	
$\overline{CAS}$ to $\overline{WE}$ delay	t_{CWD}	45		55		ns	(Note 14)
Write command referenced to $\overline{CAS}$ lead time	t_{CWL}	15		20		ns	
Data-in hold time	t_{DH}	15		20		ns	(Note 13)
Data-in setup time	t_{DS}	0		0		ns	(Note 13)
Access time from $\overline{OE}$	t_{OEA}		20		25	ns	(Notes 3, 4, 7, 8)
$\overline{OE}$ data delay time	t_{OED}	20		25		ns	
$\overline{OE}$ command hold time	t_{OEH}	0		0		ns	
$\overline{OE}$ to $\overline{RAS}$ inactive setup time	t_{OES}	0		0		ns	
Output turnoff delay from $\overline{OE}$	t_{OEZ}	0	20	0	25	ns	(Note 9)
Output buffer turnoff delay	t_{OFF}	0	20	0	25	ns	(Note 9)
$\overline{OE}$ to output active delay time	t_{OLZ}	0		0		ns	(Notes 5, 7)
Fast-page read or write cycle time	t_{PC}	50		60		ns	(Note 6)
Fast page read-modify-write cycle time	t_{PRWC}	100		120		ns	(Note 6)
Access time from $\overline{RAS}$	t_{RAC}		80		100	ns	(Notes 3, 4, 7, 8)
$\overline{RAS}$ to column address delay time	t_{RAD}	17	40	17	50	ns	(Note 8)
Row address hold time	t_{RAH}	12		12		ns	
Column address lead time referenced to $\overline{RAS}$ (rising edge)	t_{RAL}	40		50		ns	
$\overline{RAS}$ pulse width	t_{RAS}	80	10,000	100	10,000	ns	
$\overline{RAS}$ pulse width, fast-page cycle	t_{RASP}	80	125,000	100	125,000	ns	
Random read or write cycle time	t_{RC}	160		190		ns	(Note 6)
$\overline{RAS}$ to $\overline{CAS}$ delay time	t_{RCD}	25	60	25	75	ns	(Note 8)
Read command hold time referenced to $\overline{CAS}$	t_{RCH}	0		0		ns	(Note 11)
Read command setup time	t_{RCS}	0		0		ns	
Refresh period	t_{REF}		16		16	ms	Address A_0 through A_9
$\overline{RAS}$ precharge time	t_{RP}	70		80		ns	
$\overline{RAS}$ precharge $\overline{CAS}$ hold time	t_{RPC}	10		10		ns	
Read command hold time referenced to $\overline{RAS}$	t_{RRH}	10		10		ns	(Note 11)
$\overline{RAS}$ hold time	t_{RSH}	20		25		ns	
Read-modify-write cycle time	t_{RWC}	210		250		ns	(Note 6)

AC Characteristics (cont)

Parameter	Symbol	μPD424410-80 Min	μPD424410-80 Max	μPD424410-10 Min	μPD424410-10 Max	Unit	Test Conditions
$\overline{RAS}$ to $\overline{WE}$ delay	t_{RWD}	105		130		ns	(Note 14)
Write command referenced to $\overline{RAS}$ lead time	t_{RWL}	20		25		ns	
Rise and fall transition time	t_T	3	50	3	50	ns	(Note 3)
Write-per-bit hold time	t_{WBH}	15		20		ns	
Write-per-bit setup time	t_{WBS}	10		10		ns	
Write command hold time	t_{WCH}	15		20		ns	(Note 12)
Write command setup time	t_{WCS}	0		0		ns	(Note 14)
Write-per-bit mask data hold time	t_{WH}	15		20		ns	
$\overline{WE}$ command hold time for $\overline{CAS}$ before $\overline{RAS}$ refreshing	t_{WHR}	15		20		ns	
Write command pulse width	t_{WP}	15		20		ns	(Note 12)
Write-per-bit mask data setup time	t_{WS}	10		10		ns	
$\overline{WE}$ command setup time for $\overline{CAS}$ before $\overline{RAS}$ refreshing	t_{WSR}	10		10		ns	

Notes:

(1) All voltages are referenced to GND.

(2) An initial pause of 100 μs is required after power-up, followed by any eight $\overline{RAS}$ cycles, before proper device operation is achieved. At the end of the initial power-up sequence, either a $\overline{RAS}$-only or $\overline{CAS}$ before $\overline{RAS}$ refresh cycle should be executed while $\overline{WE} \geq V_{IH}$ to ensure normal operation.

(3) Ac measurements assume $t_T = 5$ ns.

(4) V_{IH} (min) and V_{IL} (max) are reference levels for measuring the timing of input signals. Transition times are measured between V_{IH} and V_{IL}.

(5) I_{CC1}, I_{CC3}, I_{CC4}, and I_{CC5} depend on output loading and cycle rates. Specified values are obtained with the output open. I_{CC3} is measured assuming that all column address inputs are held at either a high level or a low level during $\overline{RAS}$-only refresh cycles. I_{CC4} is measured assuming that all column address inputs are switched only once during each fast-page cycle.

(6) The minimum specifications are used only to indicate the cycle time at which proper operation over the full temperature range (T_A = 0 to +70 °C) is assured.

(7) Load = 2 TTL (–1 mA, +4 mA) loads and 100 pF (V_{OH} = 2.0 V and V_{OL} = 0.8 V).

(8) If $t_{RCD} \leq t_{RCD}$ (max) and $t_{RAD} \leq t_{RAD}$ (max), access time is defined by t_{RAC} (max). If $t_{RCD} \geq t_{RCD}$ (max), access time is defined by t_{CAC} (max). If $t_{RAD} \geq t_{RAD}$ (max), access time is defined by t_{AA} (max).

(9) t_{OFF} (max) and t_{OEZ} (max) define the time at which the outputs achieve the open-circuit condition and are not referenced to V_{OH} or V_{OL}.

(10) The t_{CRP} requirement should be applicable for $\overline{RAS}$/$\overline{CAS}$ cycles preceded by any cycle.

(11) Either t_{RRH} or t_{RCH} must be satisfied for a read cycle.

(12) Parameter t_{WP} is applicable for a delayed write cycle such as a read-write/read-modify-write cycle. For early write cycles, both t_{WCS} and t_{WCH} must be met.

(13) These parameters are referenced to the falling edge of $\overline{CAS}$ for early write cycles and to the falling edge of $\overline{WE}$ for delayed write or read-modify-write cycles.

(14) t_{WCS}, t_{RWD}, t_{CWD}, and t_{AWD} are restrictive operating parameters in read-write/read-modify-write cycles only. If $t_{WCS} \geq t_{WCS}$ (min), the cycle is an early write cycle and the data I/O pins will remain open-circuit throughout the entire cycle. If $t_{CWD} \geq t_{CWD}$ (min), $t_{RWD} \geq t_{RWD}$ (min), and $t_{AWD} \geq t_{AWD}$ (min), then the cycle is a read-write cycle and the data I/O pins will contain data read from the selected cells. If neither of the above conditions is met, the condition of the data I/O pins (at access time and until $\overline{CAS}$ returns to V_{IH}) is indeterminate.

(15) A test mode may be initiated by executing a $\overline{CAS}$ before $\overline{RAS}$ refresh cycle with $\overline{WE}$ held at V_{IL}. This mode also may inadvertently be initiated during power-up because external control of the signal lines is very difficult during this period. It is therefore recommended that while $\overline{WE}$ is held at V_{IH}, either a $\overline{RAS}$-only or $\overline{CAS}$ before $\overline{RAS}$ refresh cycle should be executed at any time after the end of the initial power-up sequence to ensure normal device operation.

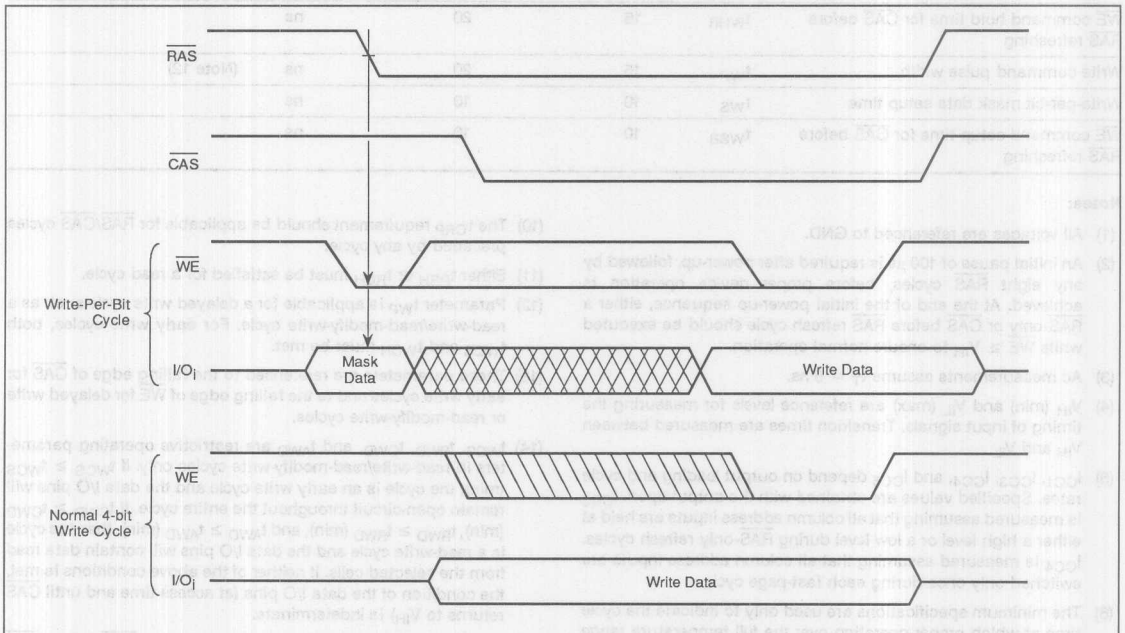
(16) These parameters define a read-modify-write cycle.

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Write-Per-Bit Option

The write-per-bit option may be used to allow a write cycle to change any number of bits in the 4-bit word. The mask is loaded from the four I/O lines at the falling edge of $\overline{RAS}$ if $\overline{WE} = V_{IL}$. If the I/O line is high, then the corresponding bit will be written when the write cycle executes. If an I/O line is low, the corresponding bit does not change. A mask loaded during fast-page operation will remain set and active for each write cycle that executes while $\overline{RAS}$ remains low. The mask may be changed at the falling edge of $\overline{RAS}$ only.

Comparison of Write-Per-Bit Cycle Versus Standard 4-Bit Write Cycle

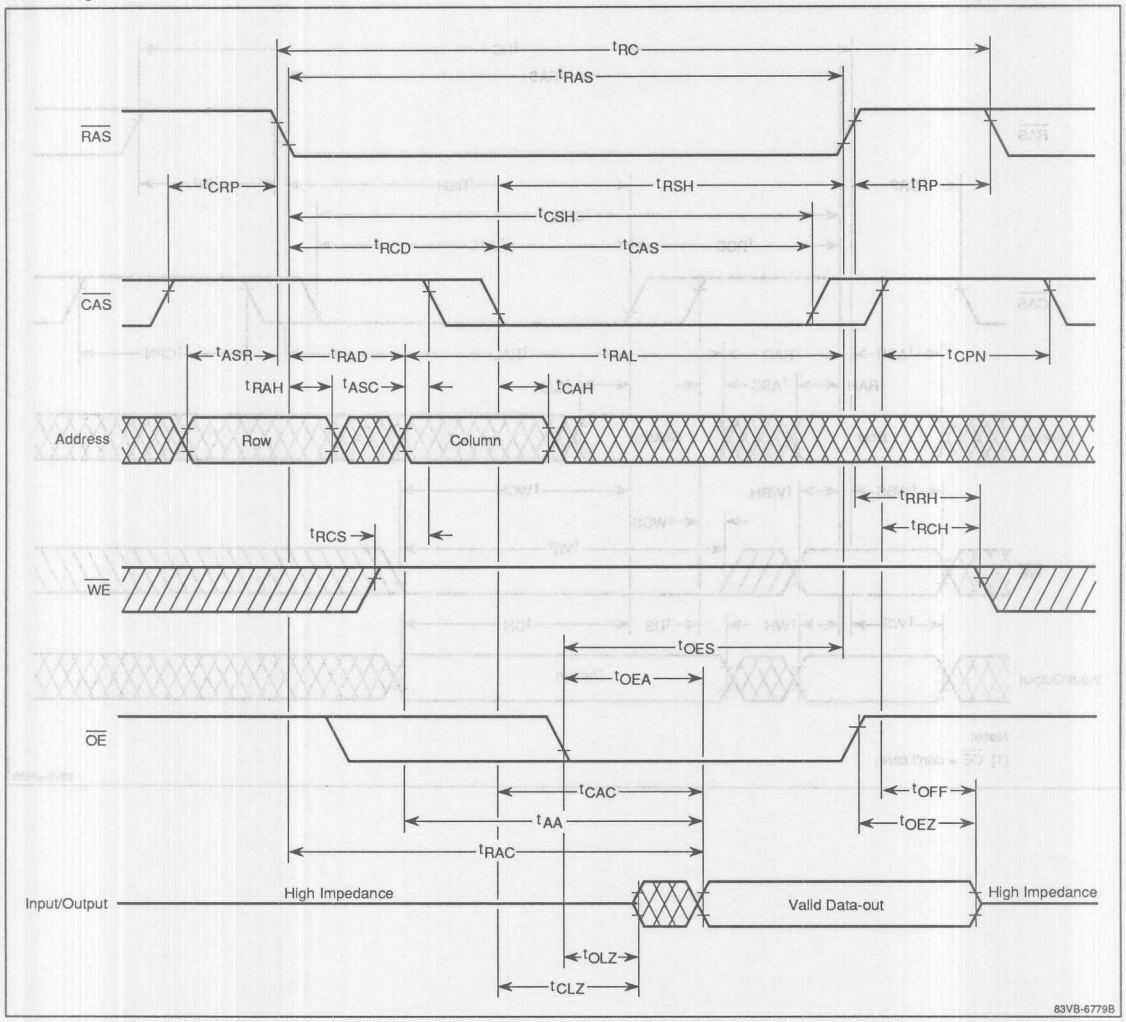


I/O	Mask Data		Write Operation
I/O_1	1	(High)	Write Bit
	0	(Low)	Disable Bit Write
I/O_2	1	(High)	Write Bit
	0	(Low)	Disable Bit Write
I/O_3	1	(High)	Write Bit
	0	(Low)	Disable Bit Write
I/O_4	1	(High)	Write Bit
	0	(Low)	Disable Bit Write

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Timing Waveforms

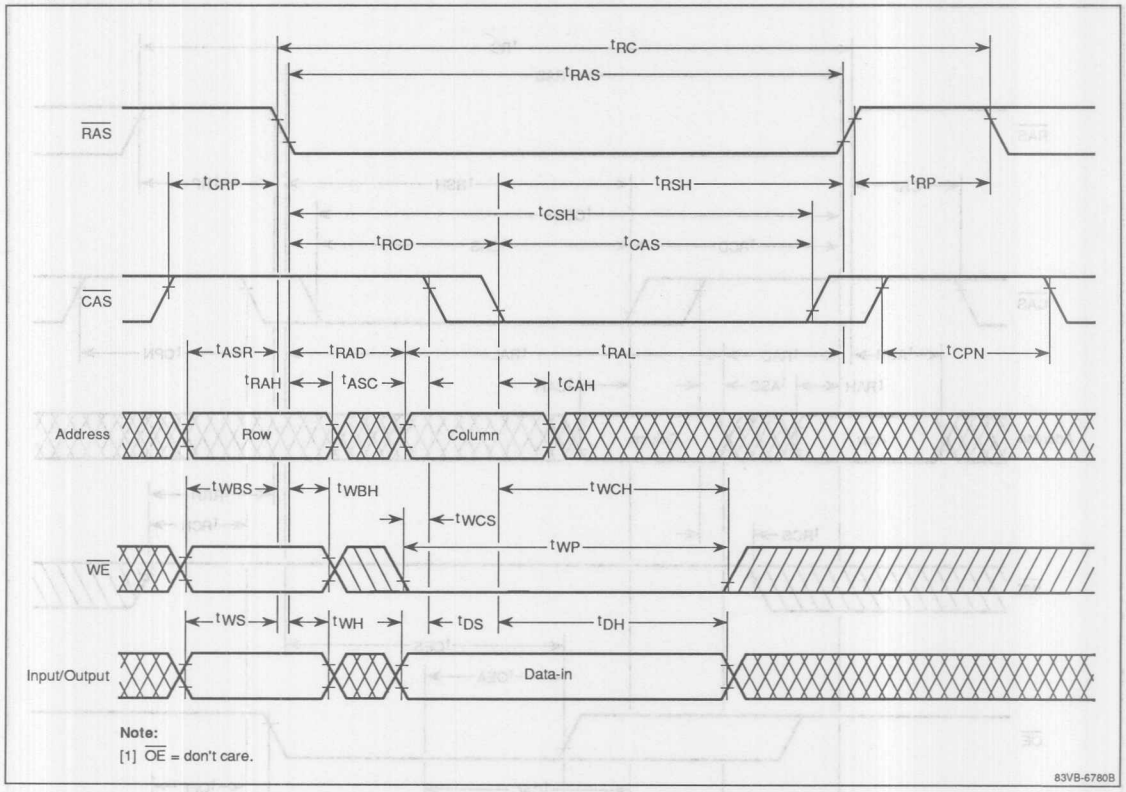
Read Cycle



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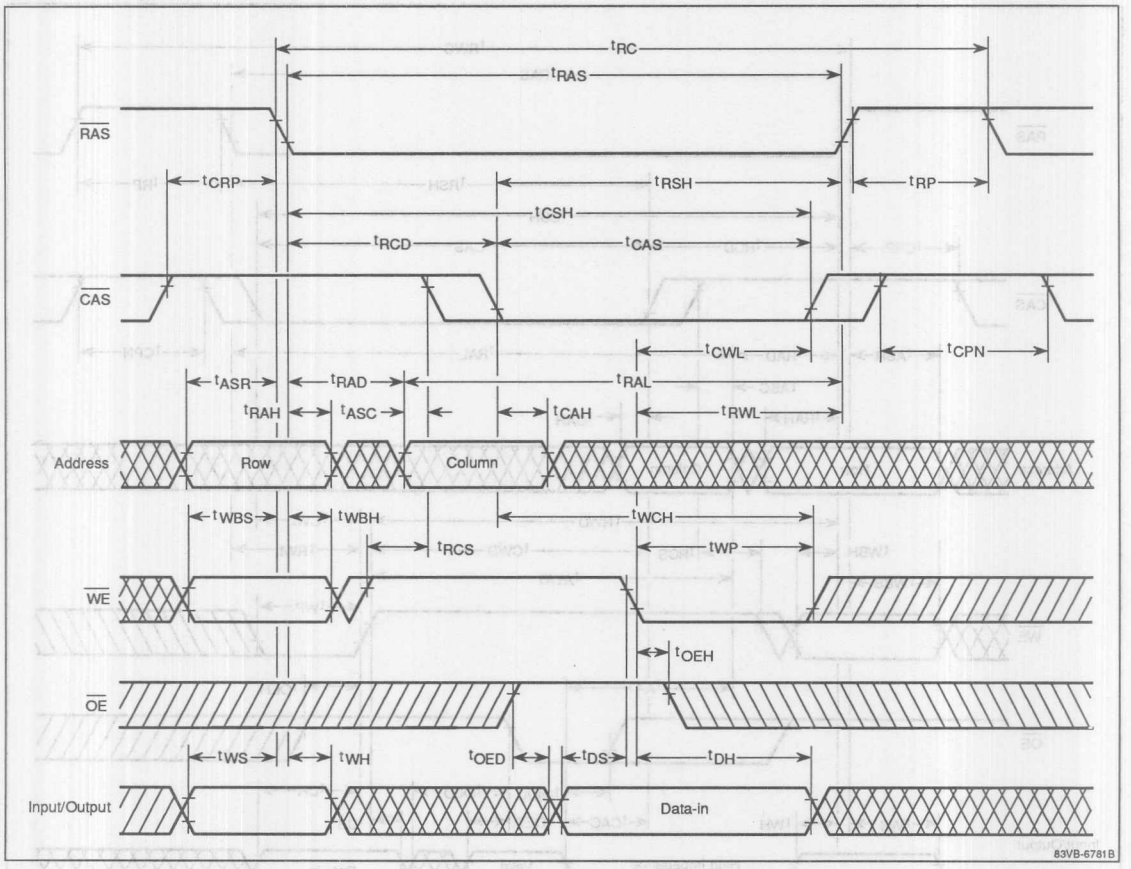
Timing Waveforms (cont)

Early Write Cycle



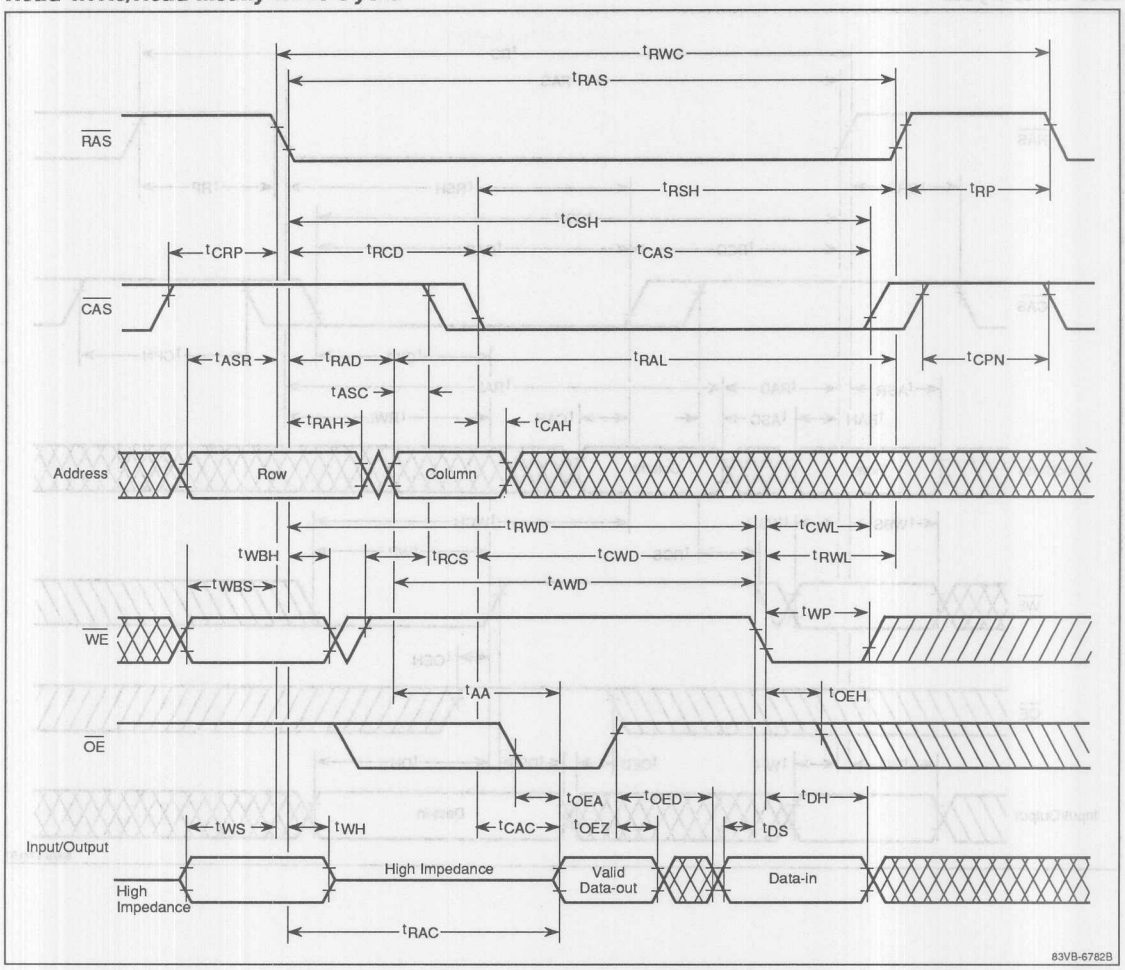
Timing Waveforms (cont)

Late Write Cycle



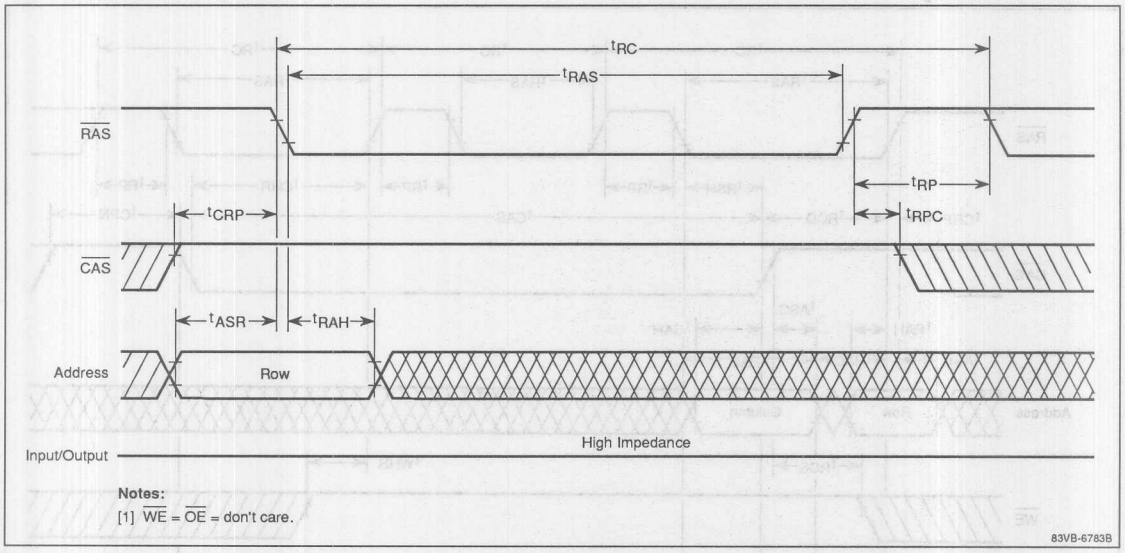
Timing Waveforms (cont)

Read-Write/Read-Modify-Write Cycle



Timing Waveforms (cont)

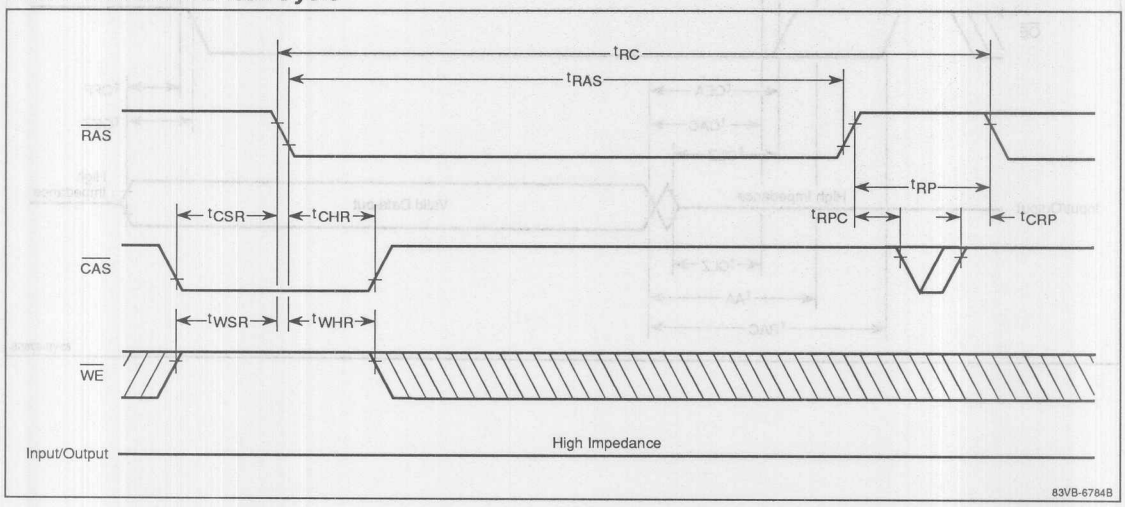
$\overline{RAS}$-Only Refresh Cycle



Notes:
[1] $\overline{WE}$ = $\overline{OE}$ = don't care.

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$\overline{CAS}$ Before $\overline{RAS}$ Refresh Cycle

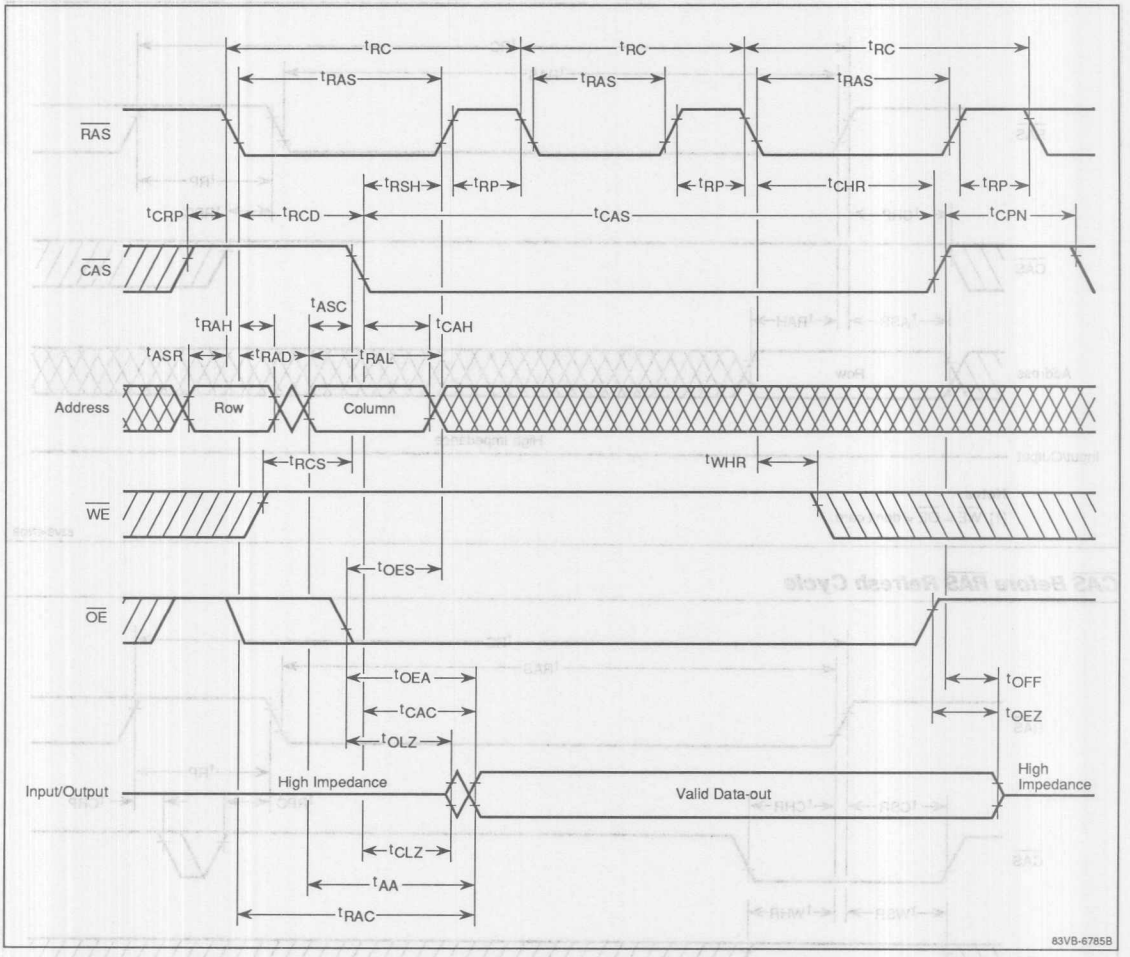


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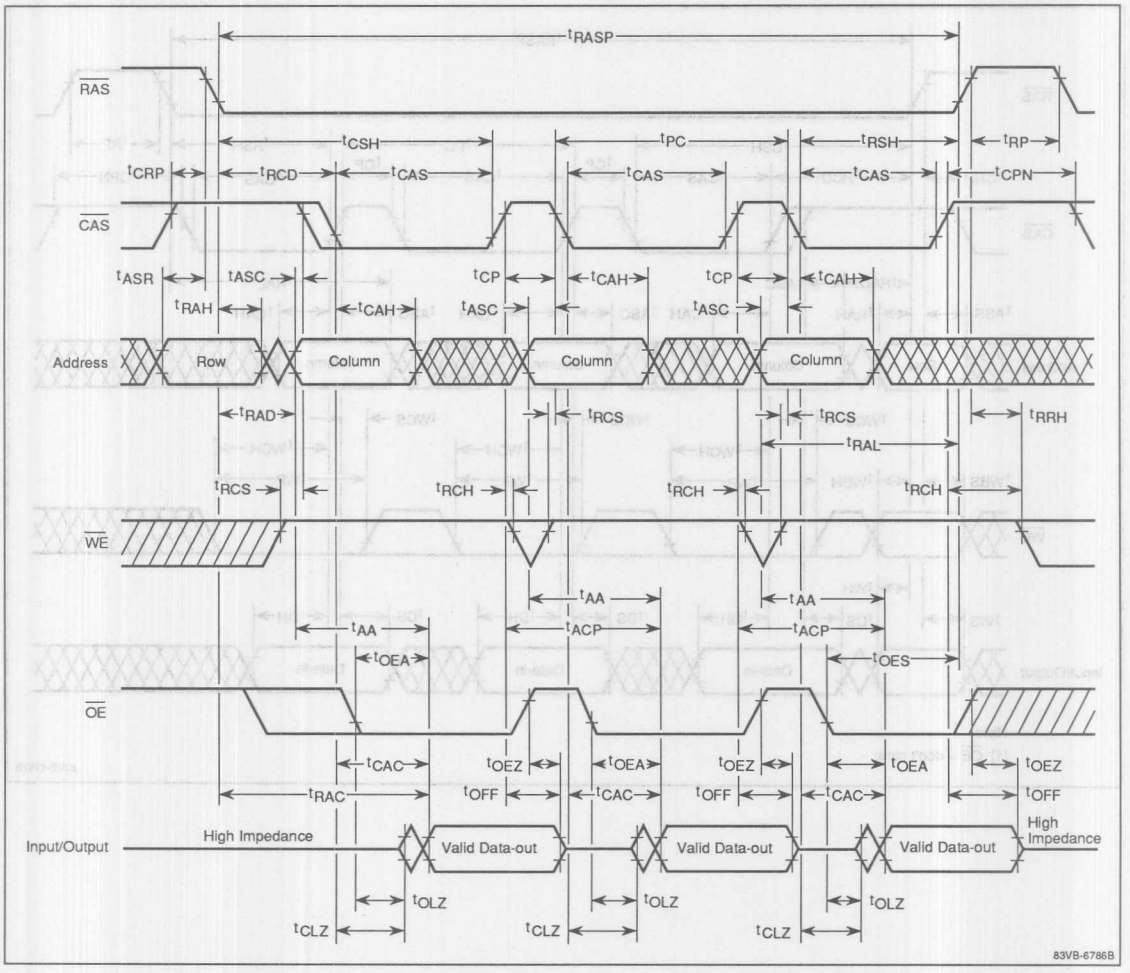
Timing Waveforms (cont)

Hidden Refresh Cycle



Timing Waveforms (cont)

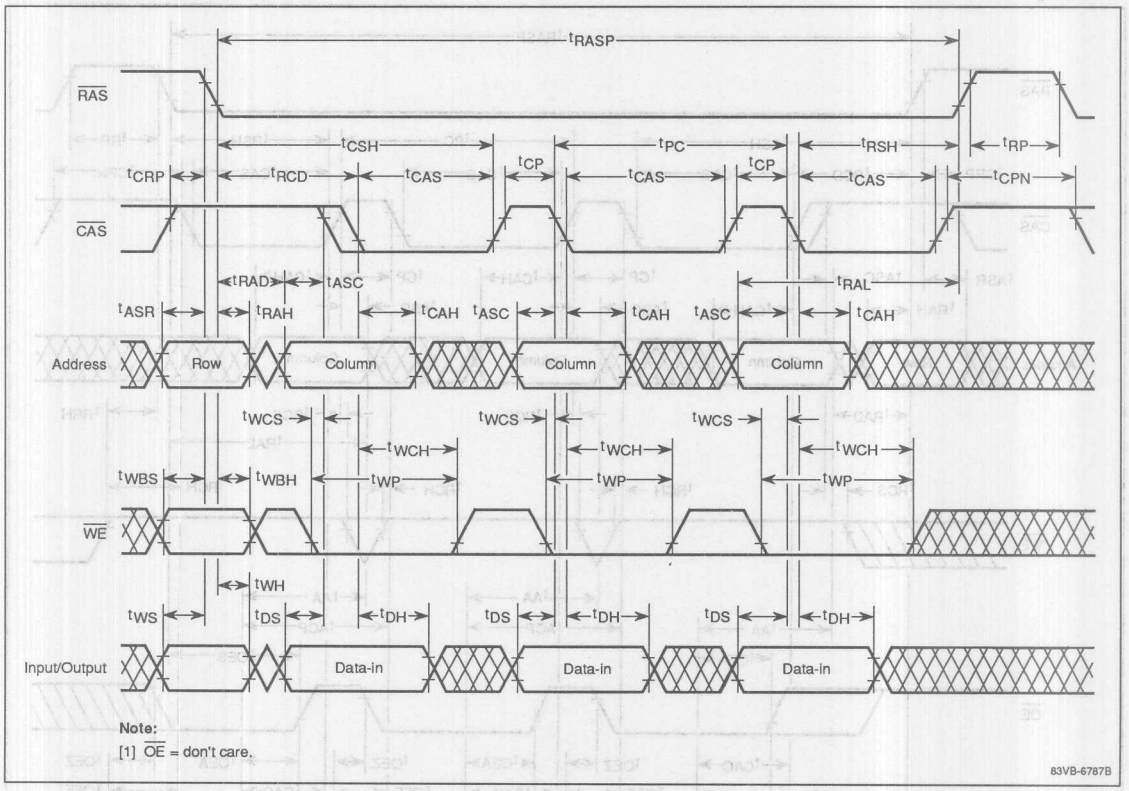
Fast-Page Read Cycle



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Timing Waveforms (cont)

Fast-Page Early Write Cycle



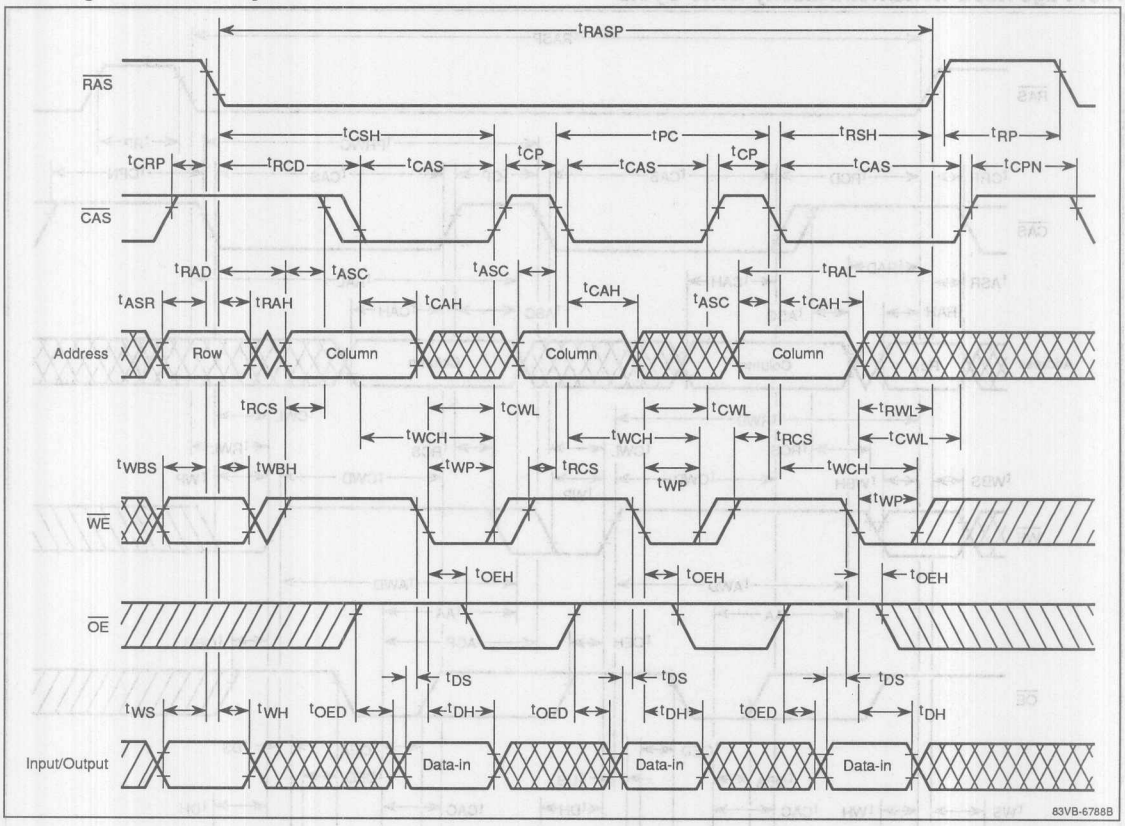
Note:

[1] $\overline{OE}$ = don't care.

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Timing Waveforms (cont)

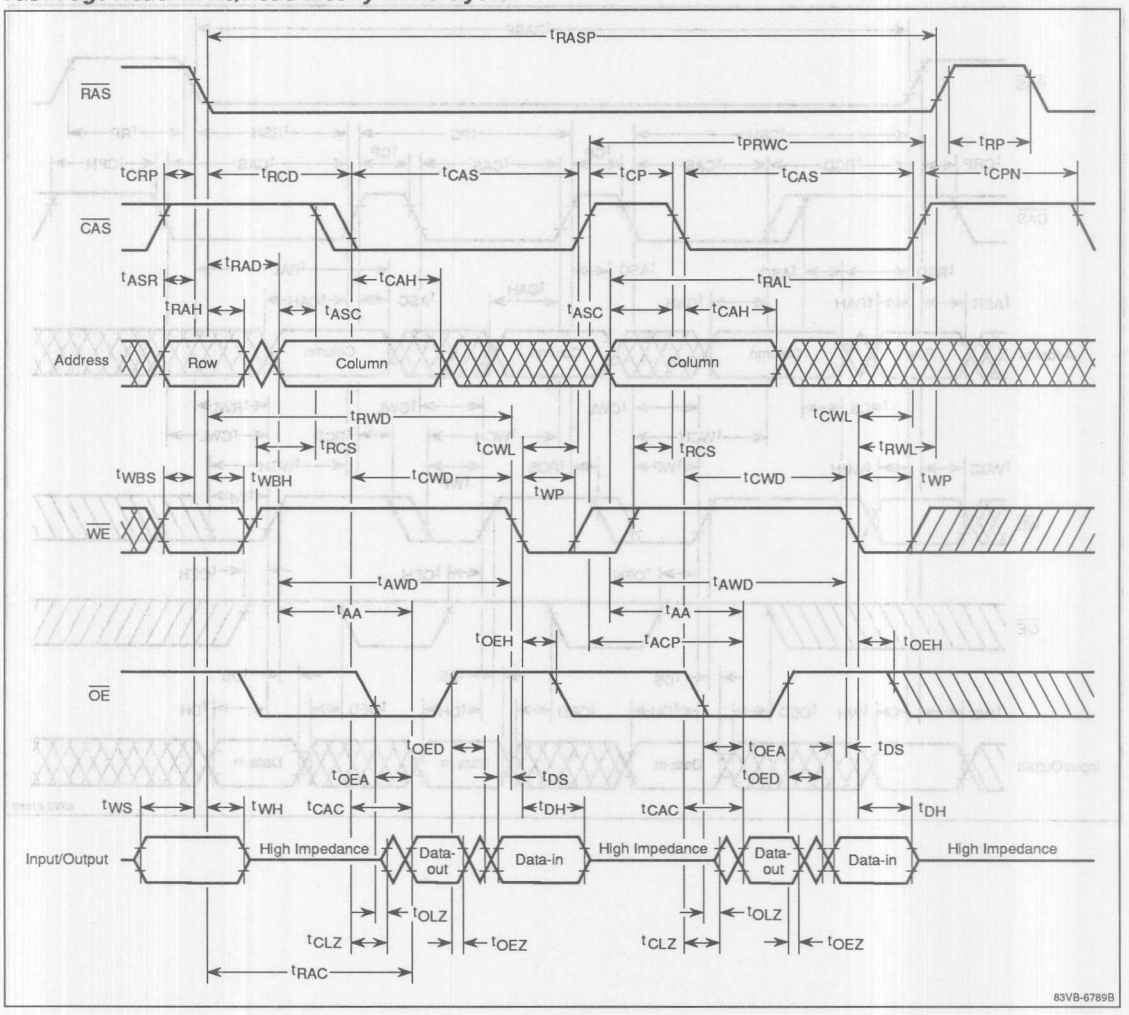
Fast-Page Late Write Cycle



6

Timing Waveforms (cont)

Fast-Page Read-Write/Read-Modify-Write Cycle



μPD424412
1,048,576 x 4-Bit
Dynamic CMOS RAM

Description

The μPD424412 is a static-column 1,048,576 by 4-bit dynamic RAM designed with a write-per-bit option to operate from a single + 5-volt power supply. Advanced polycide technology using trench capacitors minimizes silicon area and provides high storage cell capacity, high performance, and high reliability. A single-transistor dynamic storage cell and CMOS circuitry throughout ensure minimum power dissipation, while an on-chip circuit internally generates the negative-voltage substrate bias—automatically and transparently.

The three-state I/O pins are controlled by $\overline{CS}$ independent of $\overline{RAS}$. After a valid read or read-modify-write cycle, data is held on the outputs by maintaining $\overline{CS}$ low. Data outputs return to high impedance when $\overline{CS}$ goes high. Static-column read and write cycles can be executed by cycling $\overline{CS}$.

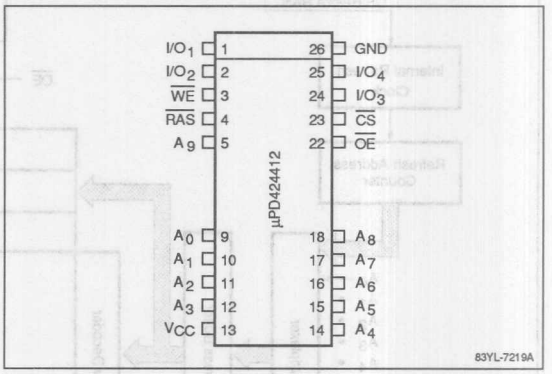
Refreshing may be accomplished by means of a $\overline{CS}$ before $\overline{RAS}$ cycle that internally generates the refresh address. Refreshing may also be accomplished by means of $\overline{RAS}$-only refresh cycles or by normal read or write cycles on the 1,024 address combinations of A_0 through A_9 during a 16-ms refresh period.

Features

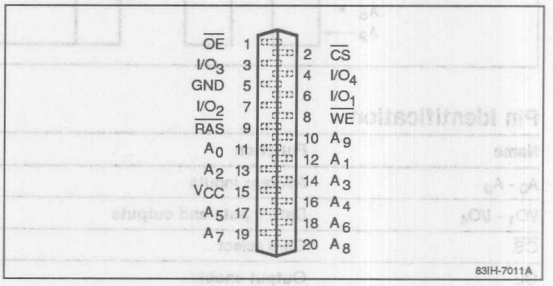
- 1,048,576 by 4-bit organization
- Single + 5-volt power supply
- Write-per-bit option
- Static-column option
- Low power dissipation
- $\overline{CS}$ before $\overline{RAS}$ internal refreshing
- Multiplexed address inputs
- On-chip substrate bias generator
- TTL-compatible inputs and outputs
- Nonlatched, three-state outputs
- Low input capacitance
- 1024 refresh cycles every 16 ms
- High-density 26/20-pin plastic SOJ or 20-pin plastic ZIP packaging

Pin Configurations

26/20-Pin Plastic SOJ



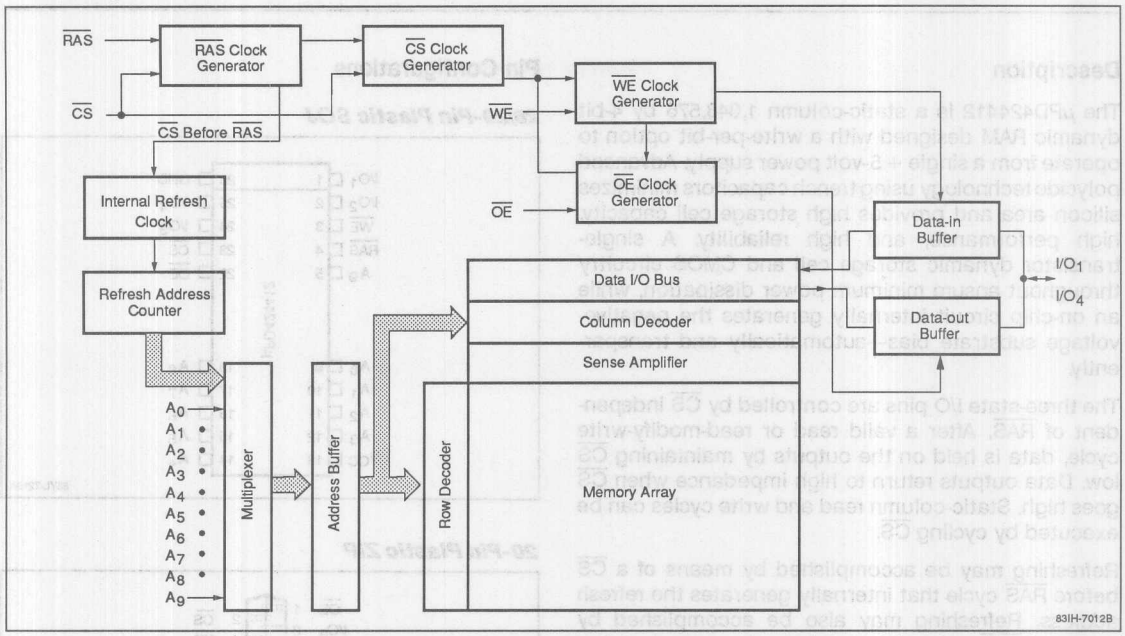
20-Pin Plastic ZIP



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New speeds (60 and 70 ns) and packages (TSOP and 300-mil SOJ) will be available in 1991.

Block Diagram



Pin Identification

Name	Function
A_0 - A_9	Address inputs
I/O_1 - I/O_4	Data inputs and outputs
$\overline{CS}$	Chip select
$\overline{OE}$	Output enable
$\overline{RAS}$	Row address strobe
$\overline{WE}$	Write enable
GND	Ground
V_{CC}	+5-volt power supply

Capacitance

T_A = 25°C; f = 1 MHz

Parameter	Symbol	Max	Unit	Pins Under Test
Input capacitance	C_{I1}	5	pF	Addresses
	C_{I2}	7	pF	$\overline{RAS}$, $\overline{CS}$, $\overline{WE}$, $\overline{OE}$
Input/output capacitance	C_O	7	pF	I/O_1 – I/O_4

Absolute Maximum Ratings

Voltage on any pin relative to GND, V_T	−1.0 to +7.0 V
Operating temperature, T_{OPR}	0 to +70°C
Storage temperature, T_{STG}	−55 to +125°C
Short-circuit output current, I_{OS}	50 mA
Power dissipation, P_D	1.0 W

Exposure to Absolute Maximum Ratings for extended periods may affect device reliability; exceeding the ratings could cause permanent damage. The device should be operated within the limits specified under DC and AC Characteristics.

Recommended Operating Conditions

Parameter	Symbol	Min	Typ	Max	Unit
Input voltage, high	V_{IH}	2.4		V_{CC} + 1.0	V
Input voltage, low	V_{IL}	−1.0		0.8	V
Supply voltage	V_{CC}	4.5	5.0	5.5	V
Ambient temperature	T_A	0		70	°C

Ordering Information

Part Number	Row Access Time (max)	R/W Cycle Time (min)	Static-Column Cycle (min)	Package
μPD424412LB-70	70 ns	140 ns	40 ns	26/20-pin plastic SOJ
LB-80	80 ns	160 ns	50 ns	
LB-10	100 ns	190 ns	60 ns	
μPD424412V-70	70 ns	140 ns	40 ns	20-pin plastic ZIP
V-80	80 ns	160 ns	50 ns	
V-10	100 ns	190 ns	60 ns	

Notes:

(1) Contact your NEC sales representative for data sheet and product availability for the μPD424412-70.

DC Characteristics

T_A = 0 to +70°C; V_{CC} = +5.0 ±10%

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions
Standby current	I_{CC2}			2.0	mA	$\overline{RAS}$ = $\overline{CS}$ ≥ V_{IH} (min); I_O = 0 mA
				1.0	mA	$\overline{RAS}$ = $\overline{CS}$ ≥ V_{CC} – 0.2 V; I_O = 0 mA
Input leakage current	$I_{I(L)}$	–10		10	μA	V_{IN} = 0 V to V_{CC}; all other pins not under test = 0 V
Output leakage current	$I_{O(L)}$	–10		10	μA	D_{OUT} disabled; V_{OUT} = 0 V to V_{CC}
Output voltage, low	V_{OL}			0.4	V	I_{OL} = 4.2 mA
Output voltage, high	V_{OH}	2.4			V	I_{OH} = –5 mA

AC Characteristics

T_A = 0 to +70°C; V_{CC} = +5.0 V ± 10%

		μPD424412-80		μPD424412-10			
Parameter	Symbol	Min	Max	Min	Max	Unit	Test Conditions
Operating current, average	I_{CC1}		90		80	mA	$\overline{RAS}$, $\overline{CS}$ cycling; t_{RC} = t_{RC} min (Note 5)
Operating current, $\overline{RAS}$-only refresh cycle, average	I_{CC3}		90		80	mA	$\overline{RAS}$ cycling; $\overline{CS}$ ≥ V_{IH} min; t_{RC} = t_{RC} min (Note 5)
Operating current, static-column cycle, average	I_{CC4}		70		60	mA	$\overline{RAS}$ ≤ V_{IL}; $\overline{CS}$ cycling; t_{RSC} = t_{RSC} min or t_{WSC} = t_{WSC} min (Note 5)
Operating current, $\overline{CS}$ before $\overline{RAS}$ refreshing, average	I_{CC5}		90		80	mA	$\overline{RAS}$ cycling; $\overline{CS}$ ≤ V_{IL} max; t_{RC} = t_{RC} min (Note 5)
Access time from column address	t_{AA}		40		50	ns	(Notes 3, 4, 7, 8)
Colum address hold time referenced to $\overline{RAS}$ (rising edge)	t_{AH}	15		15		ns	
Column address setup time	t_{ASC}	0		0		ns	
Row address setup time	t_{ASR}	0		0		ns	
Column address to $\overline{WE}$ delay time	t_{AWD}	65		80		ns	(Note 15)
Access time from $\overline{CS}$ (falling edge)	t_{CAC}		20		25	ns	(Notes 3, 4, 7, 8)
Column address hold time	t_{CAH}	15		20		ns	

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AC Characteristics (cont)

Parameter	Symbol	μPD424412-80 Min	μPD424412-80 Max	μPD424412-10 Min	μPD424412-10 Max	Unit	Test Conditions
$\overline{CS}$ hold time for $\overline{CS}$ before $\overline{RAS}$ refreshing	t_{CHR}	15		20		ns	
$\overline{CS}$ precharge time, static-column cycle	t_{CP}	10		10		ns	
$\overline{CS}$ precharge time	t_{CPN}	10		10		ns	
$\overline{CS}$ to $\overline{RAS}$ precharge time	t_{CRP}	10		10		ns	(Note 11)
$\overline{CS}$ pulse width	t_{CS}	20	100,000	25	100,000	ns	
$\overline{CS}$ hold time	t_{CSH}	80		100		ns	
$\overline{CS}$ setup time for $\overline{CS}$ before $\overline{RAS}$ refreshing	t_{CSR}	10		10		ns	
$\overline{CS}$ to $\overline{WE}$ delay	t_{CWD}	45		55		ns	(Note 15)
Write command referenced to $\overline{CS}$ lead time	t_{CWL}	15		20		ns	
Data-in hold time	t_{DH}	15		20		ns	(Note 14)
Data-in setup time	t_{DS}	0		0		ns	(Note 14)
Access time from $\overline{OE}$	t_{OEA}		20		25	ns	(Notes 3, 4, 7, 8)
$\overline{OE}$ data delay time	t_{OED}	20		25		ns	
$\overline{OE}$ command hold time	t_{OEH}	0		0		ns	
$\overline{OE}$ to $\overline{RAS}$ inactive setup time	t_{OES}	0		0		ns	
Output turnoff delay from $\overline{OE}$	t_{OEZ}	0	20	0	25	ns	(Note 10)
Output buffer turnoff delay	t_{OFF}	0	20	0	25	ns	(Note 10)
Output hold time for address	t_{OH}	5		5		ns	
Output enable time from $\overline{WE}$	t_{OW}		25		30	ns	
Access time from $\overline{WE}$	t_{PWA}		90		110	ns	(Notes 7, 16)
Column address hold time referenced to $\overline{WE}$	t_{PWH}	90		110		ns	
Access time from $\overline{RAS}$	t_{RAC}		80		100	ns	(Notes 3, 4, 7, 8)
$\overline{RAS}$ to column address delay time	t_{RAD}	17	40	17	50	ns	(Note 9)
Row address hold time	t_{RAH}	12		12		ns	
Column address lead time referenced to $\overline{RAS}$ (rising edge)	t_{RAL}	40		50		ns	
$\overline{RAS}$ pulse width	t_{RAS}	80	10,000	100	10,000	ns	
$\overline{RAS}$ pulse width, static-column cycle	t_{RASC}	80	100,000	100	100,000	ns	
Random read or write cycle time	t_{RC}	160		190		ns	(Note 6)
$\overline{RAS}$ to $\overline{CS}$ delay time	t_{RCD}	25	60	25	75	ns	(Note 8)
Read command hold time referenced to $\overline{CS}$	t_{RCH}	0		0		ns	(Note 12)
Read command setup time	t_{RCS}	0		0		ns	
Refresh period	t_{REF}		16		16	ms	Addresses A_0 through A_9
$\overline{RAS}$ precharge time	t_{RP}	70		80		ns	
$\overline{RAS}$ precharge $\overline{CS}$ hold time	t_{RPC}	10		10		ns	
Read command hold time referenced to $\overline{RAS}$	t_{RRH}	10		10		ns	(Note 12)
Read cycle time	t_{RSC}	50		60		ns	
$\overline{RAS}$ hold time	t_{RSH}	20		25		ns	
$\overline{RAS}$ to second $\overline{WE}$ delay time	t_{RSW}	95		115		ns	
Read-modify-write cycle time	t_{RWC}	210		250		ns	(Note 6)

AC Characteristics (cont)

Parameter	Symbol	μPD424412-80 Min	μPD424412-80 Max	μPD424412-10 Min	μPD424412-10 Max	Unit	Test Conditions
$\overline{RAS}$ to $\overline{WE}$ delay	t_{RWD}	105		130		ns	(Note 15)
Write command referenced to $\overline{RAS}$ lead time	t_{RWL}	20		25		ns	
Read/write cycle time	t_{RWSC}	120		145		ns	
Rise and fall transition time	t_T	3	50	3	50	ns	(Note 4)
$\overline{WE}$ to column address delay time	t_{WAD}	20	45	25	55	ns	(Note 16)
Write-per-bit hold time	t_{WBH}	15		20		ns	
Write-per-bit setup time	t_{WBS}	10		10		ns	
Write command hold time	t_{WCH}	15		20		ns	(Note 13)
Write command setup time	t_{WCS}	0		0		ns	(Note 15)
Write-per-bit mask data hold time	t_{WH}	15		20		ns	
$\overline{WE}$ command hold time for $\overline{CS}$ before $\overline{RAS}$ refreshing	t_{WHR}	15		20		ns	
Write invalid time	t_{WI}	10		10		ns	
Write command pulse width	t_{WP}	15		20		ns	(Note 13)
Write-per-bit mask data setup time	t_{WS}	10		10		ns	
Write cycle time	t_{WSC}	50		60		ns	
$\overline{WE}$ command setup time for $\overline{CS}$ before $\overline{RAS}$ refreshing	t_{WSR}	10		10		ns	

Notes:

(1) All voltages are referenced to GND.

(2) An initial pause of 100 μs is required after power-up, followed by any eight $\overline{RAS}$ cycles, before proper device operation is achieved. At the end of the initial power up sequence, it is recommended that either a $\overline{RAS}$-only refresh or a $\overline{CS}$ before $\overline{RAS}$ refresh cycle be executed while $\overline{WE} \geq V_{IH}$ to ensure normal operation.

(3) AC measurements assume $t_T = 5$ ns.

(4) V_{IH} (min) and V_{IL} (max) are reference levels for measuring the timing of input signals. Transition times are measured between V_{IH} and V_{IL}.

(5) I_{CC1}, I_{CC3}, I_{CC4}, and I_{CC5} depend on output loading and cycle rates. Specified values are obtained with the output open. I_{CC3} is measured assuming that all column address inputs are held at either a high level or a low level during $\overline{RAS}$-only refresh cycles. I_{CC4} is measured assuming that all column address inputs are switched only once during each static column cycle.

(6) The minimum specifications are used only to indicate the cycle time at which proper operation over the full temperature range (T_A = 0 to +70°C) is assured.

(7) Load = 2 TTL (–1 mA, +4 mA) loads and 100 pF (V_{OH} = 2.0 V and V_{OL} = 0.8 V).

(8) If $t_{RCD} \leq$ exceeds t_{RAD} max, then t_{RAC} will increase by the amount t_{RCD} exceeds t_{RCD} (max).

(9) If $t_{RAD} \geq t_{RAD}$ (max), then the access time is defined by t_{AA}.

(10) t_{OFF} (max) and t_{OEZ} (max) define the time at which the outputs achieve the open-circuit condition and are not referenced to V_{OH} or V_{OL}.

(11) The t_{CRP} requirement should be applicable for $\overline{RAS}/\overline{CS}$ cycles preceded by any cycle.

(12) Either t_{RRH} or t_{RCH} must be satisfied for a read cycle.

(13) Parameter t_{WP} is applicable for a delayed write cycle such as a read-write/read-modify-write cycle. For early write cycles, both t_{WCS} and t_{WCH} must be met.

(14) These parameters are referenced to the falling edge of $\overline{CS}$ for early write cycles and to the falling edge of $\overline{WE}$ for delayed write or read-modify-write cycles.

(15) t_{WCS}, t_{RWD}, t_{CWD}, and t_{AWD} are restrictive operating parameters in read-write/read-modify-write cycles only. If $t_{WCS} \geq t_{WCS}$ (min), the cycle is an early write cycle and the data I/O pins will remain open-circuit throughout the entire cycle. If $t_{CWD} \geq t_{CWD}$ (min), $t_{RWD} \geq t_{RWD}$ (min), and $t_{AWD} \geq t_{AWD}$ (min), then the cycle is a read-write cycle and the data I/O pins will contain data read from the selected cells. If neither of the above conditions is met, the condition of the data I/O pins (at access time and until $\overline{CS}$ returns to V_{IH}) is indeterminate.

(16) A test mode may be initiated by executing a $\overline{CS}$ before $\overline{RAS}$ refresh cycle with $\overline{WE}$ held at V_{IL}. This mode also may inadvertently be initiated during power-up because external control of the signal lines is very difficult during this period. It is therefore recommended that while $\overline{WE}$ is held at V_{IH}, either a $\overline{RAS}$-only or $\overline{CS}$ before $\overline{RAS}$ refresh cycle should be executed at any time after the end of the initial power-up sequence to ensure normal device operation.

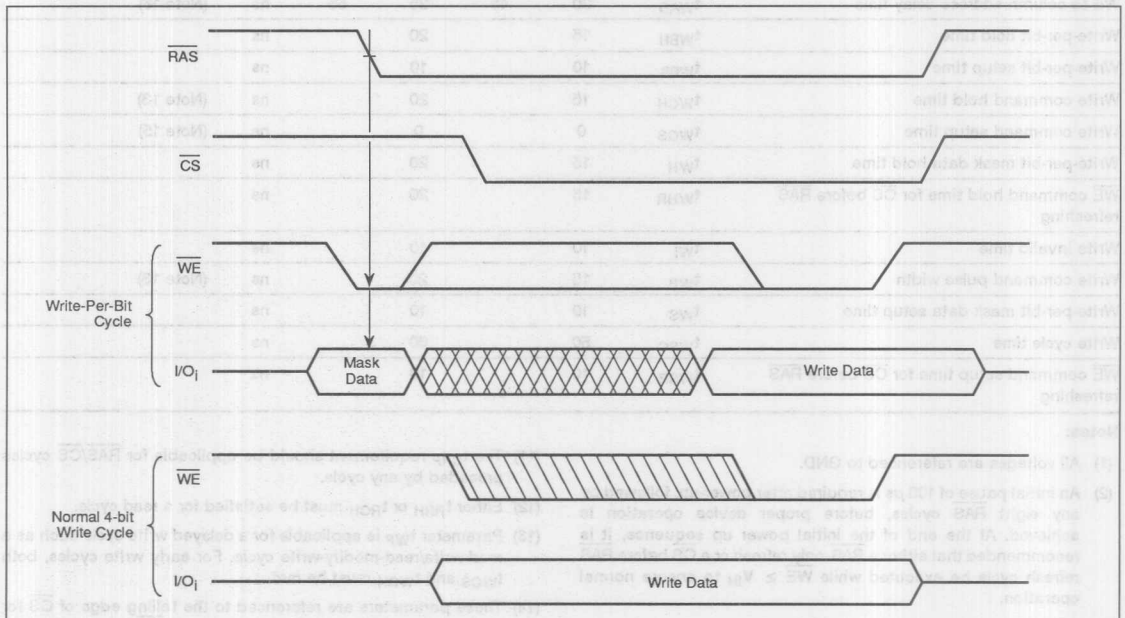
(17) Assumes $t_{WAD} \leq t_{WAD}$ (max).

6

Write-Per-Bit Option

The write-per-bit option may be used to allow a write cycle to change any number of bits in the 4-bit word. The mask is loaded from the four I/O lines at the falling edge of $\overline{RAS}$ if $\overline{WE} = V_{IL}$. If the I/O line is high, then the corresponding bit will be written when the write cycle executes. If an I/O line is low, the corresponding bit does not change. A mask loaded during static-column operation will remain set and active for each write cycle that executes while $\overline{RAS}$ remains low. The mask may be changed at the falling edge of $\overline{RAS}$ only.

Comparison of Write-Per-Bit Cycle Versus Standard 4-Bit Write Cycle

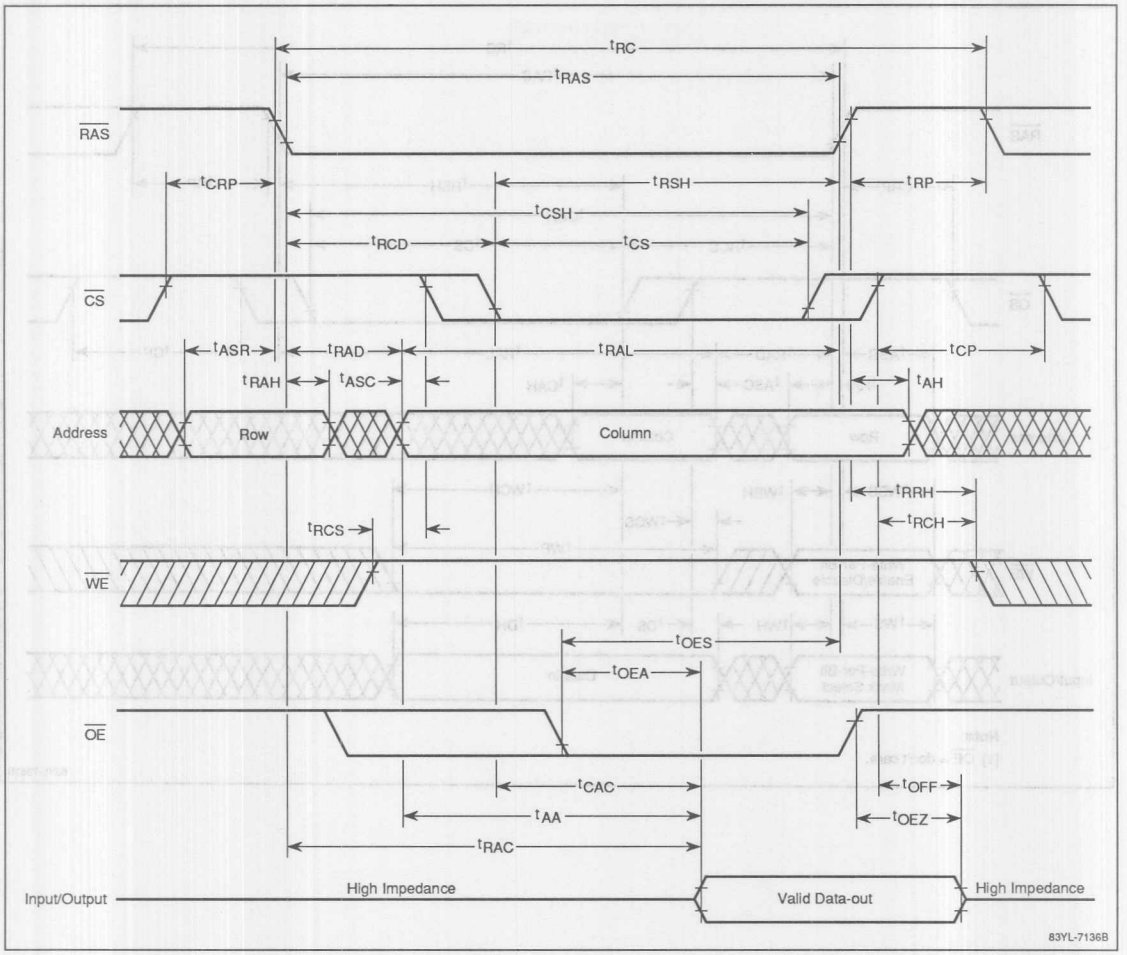


I/O	Mask Data		Write Operation
I/O_1	1	(High)	Write Bit
	0	(Low)	Disable Bit Write
I/O_2	1	(High)	Write Bit
	0	(Low)	Disable Bit Write
I/O_3	1	(High)	Write Bit
	0	(Low)	Disable Bit Write
I/O_4	1	(High)	Write Bit
	0	(Low)	Disable Bit Write

83YL-7216B

Timing Waveforms

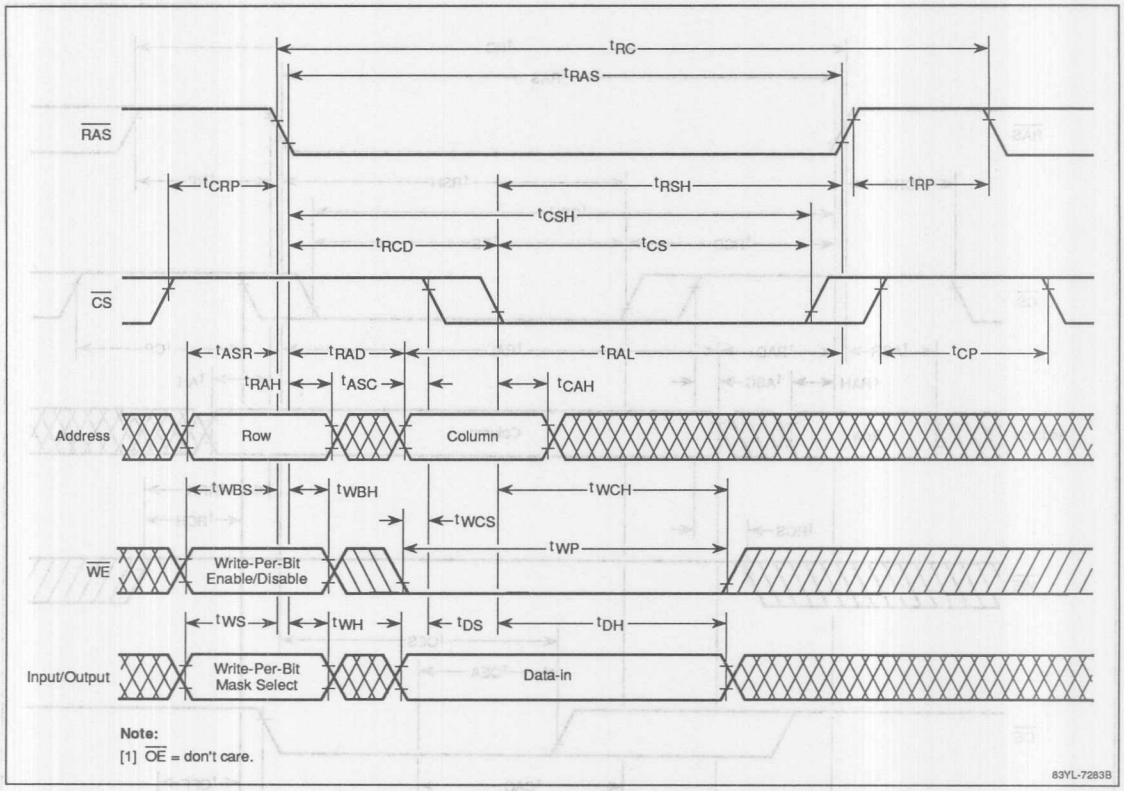
Read Cycle



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Timing Waveforms (cont)

Early Write Cycle

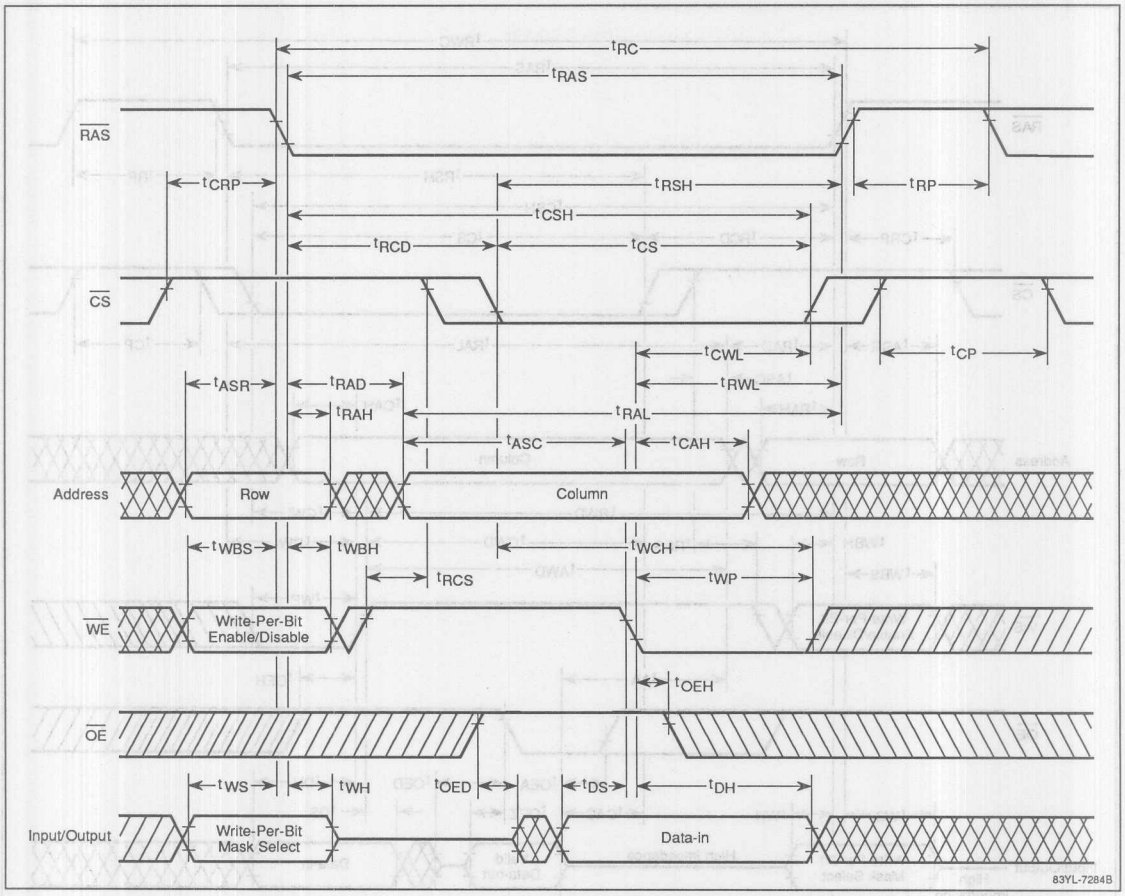


Note:
[1] $\overline{OE}$ = don't care.

83YL-7283B

Timing Waveforms (cont)

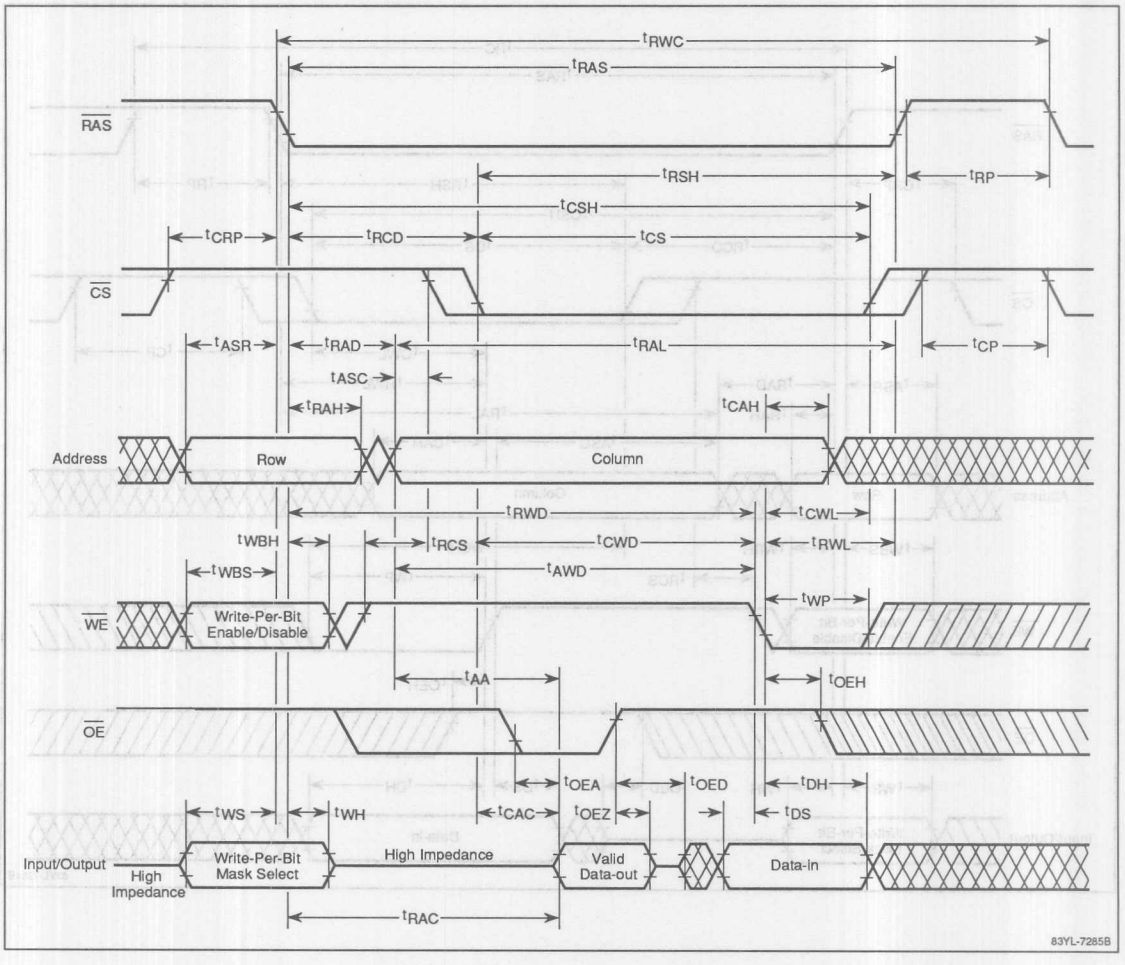
Late Write Cycle



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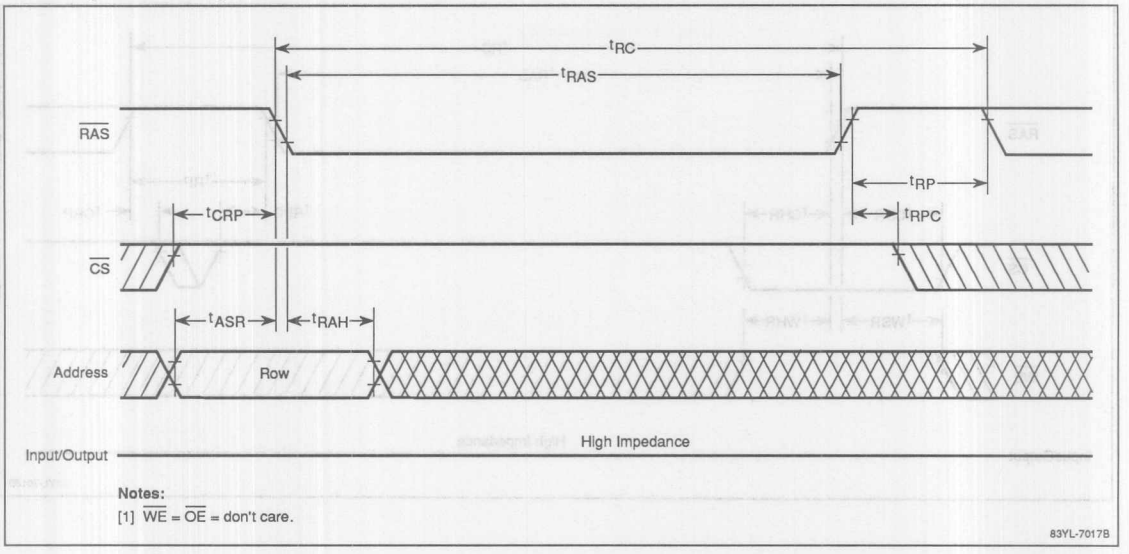
Timing Waveforms (cont)

Read-Write/Read-Modify-Write Cycle



Timing Waveforms (cont)

$\overline{RAS}$-Only Refresh Cycle



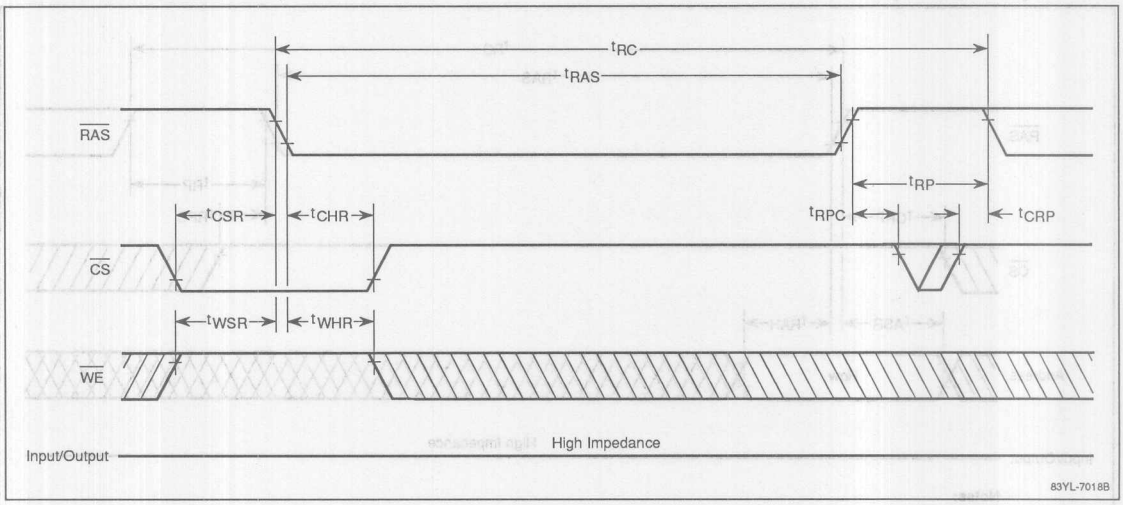
Notes:
[1] $\overline{WE}$ = $\overline{OE}$ = don't care.

83YL-7017B

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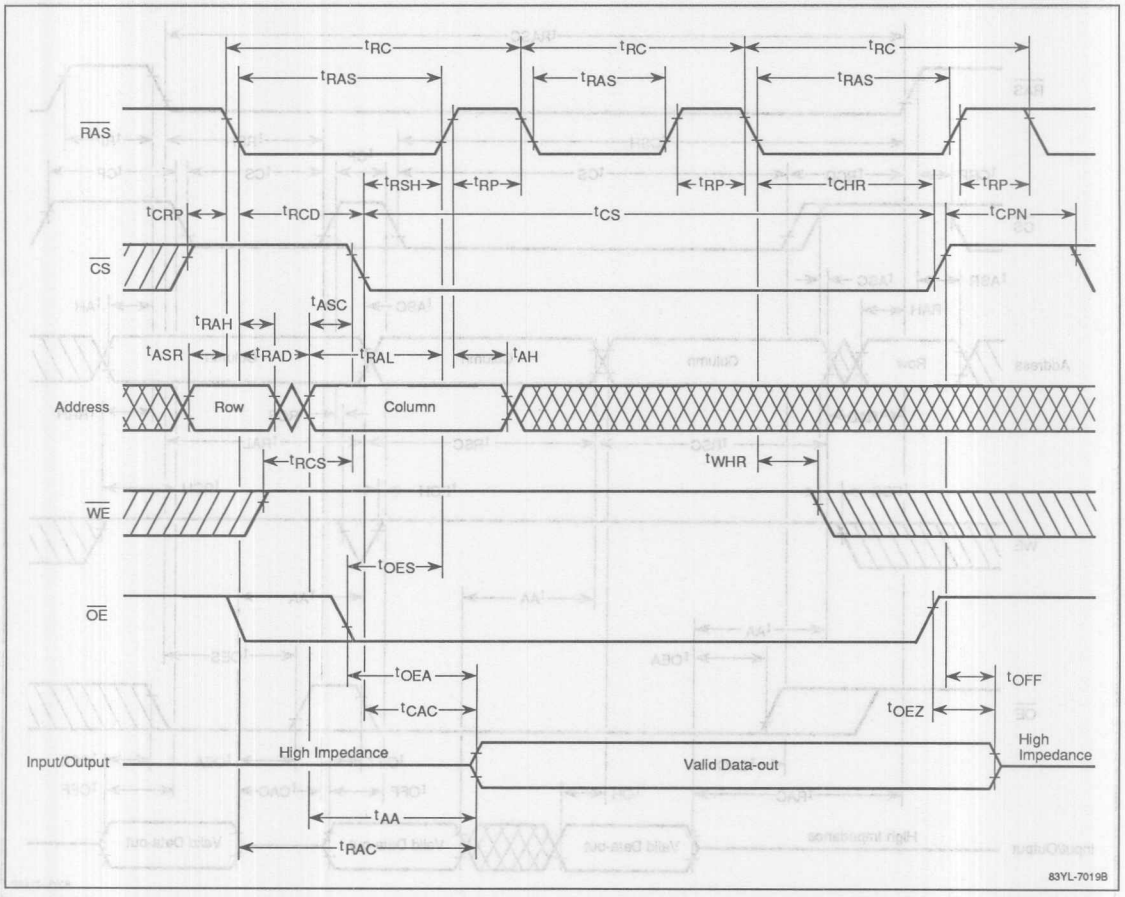
Timing Waveforms (cont)

$\overline{CS}$ Before $\overline{RAS}$ Refresh Cycle



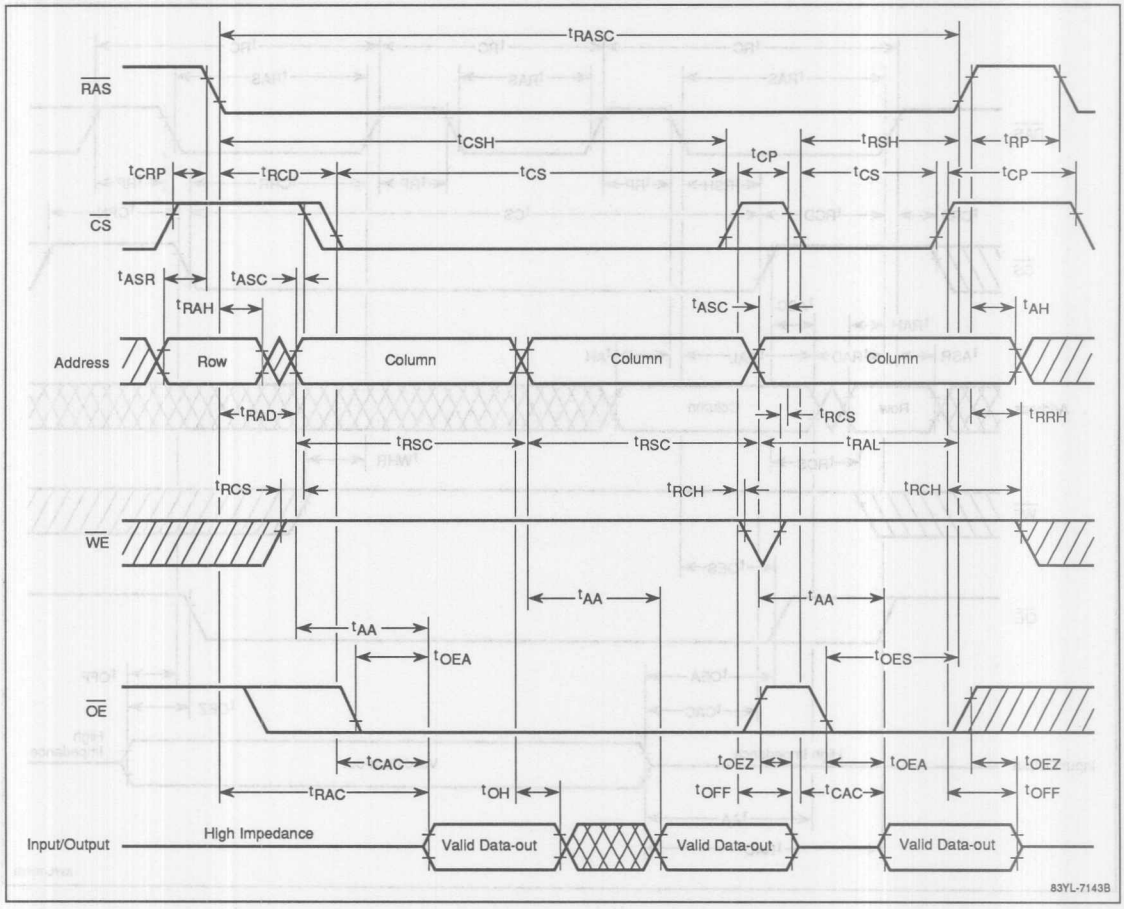
Timing Waveforms (cont)

Hidden Refresh Cycle



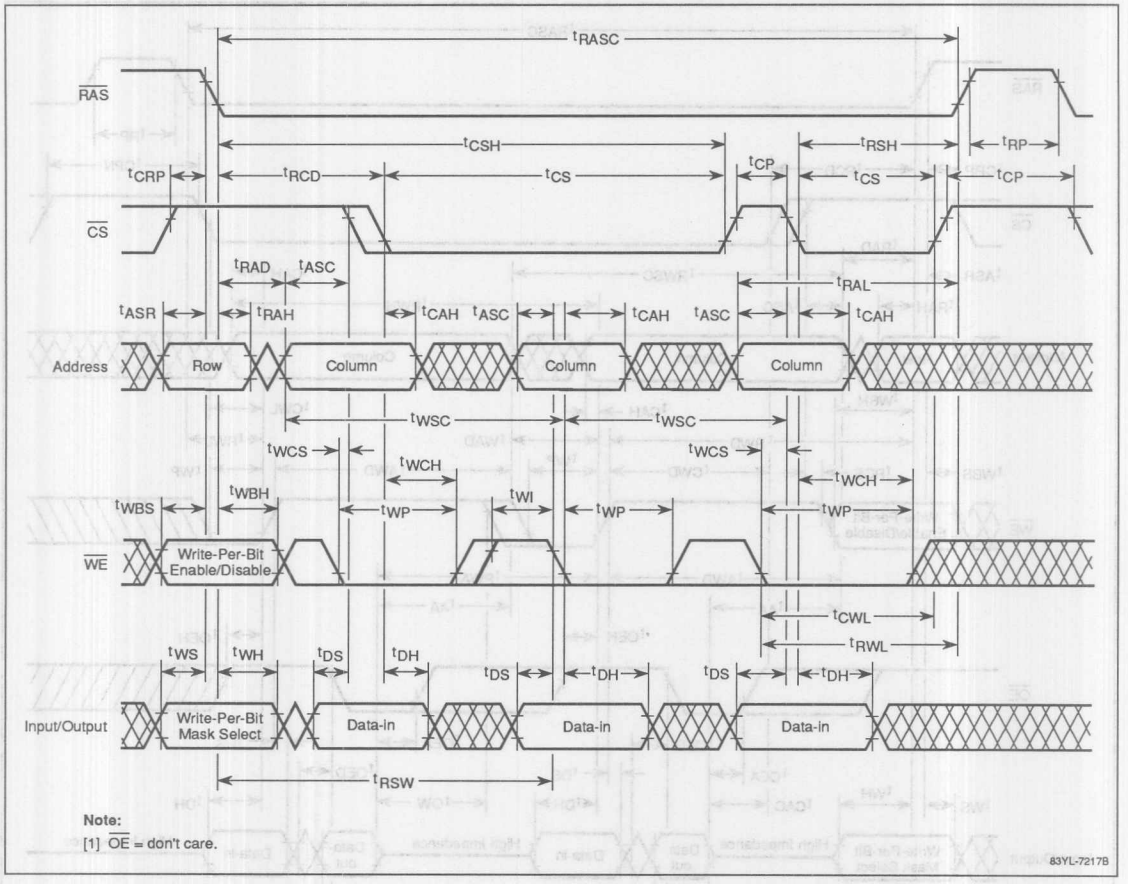
Timing Waveforms (cont)

Static-Column Read Cycle



Timing Waveforms (cont)

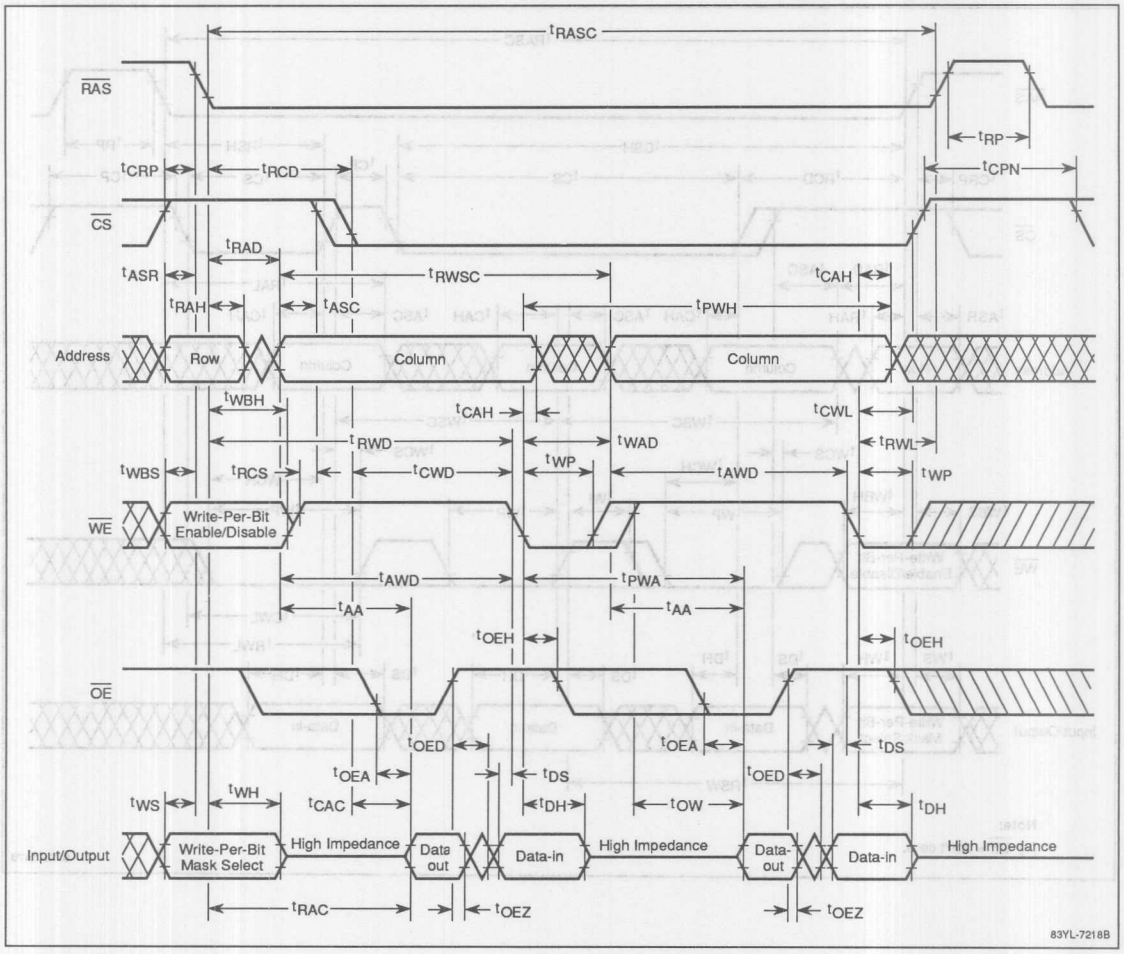
Static-Column Early Write Cycle



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Timing Waveforms (cont)

Static-Column Read-Write/Read-Modify-Write Cycle



NEC Electronics Inc.

μPD424800
524,288 x 8-Bit
Dynamic CMOS RAM

PRELIMINARY INFORMATION

Description

The μPD424800 is a fast-page dynamic RAM organized as 524,288 words by 8 bits and designed to operate from a single + 5-volt power supply. Advanced polycide technology using trench capacitors minimizes silicon area and provides high storage cell capacity, high performance, and high reliability. A single-transistor dynamic storage cell and CMOS circuitry throughout ensure minimum power dissipation, while an on-chip circuit internally generates the negative-voltage substrate bias—automatically and transparently.

The three-state I/O pins are controlled by $\overline{CAS}$ independent of $\overline{RAS}$. After a valid read or read-modify-write cycle, data is held on the outputs by maintaining $\overline{CAS}$ low. Data outputs return to high impedance when $\overline{CAS}$ goes high. Fast-page read and write cycles can be executed by cycling $\overline{CAS}$.

Refreshing may be accomplished by means of a $\overline{CAS}$ before $\overline{RAS}$ cycle that internally generates the refresh address. Refreshing may also be accomplished by means of $\overline{RAS}$-only refresh cycles or by normal read or write cycles on the 1,024 address combinations of A_0 through A_9 during a 16-ms refresh period.

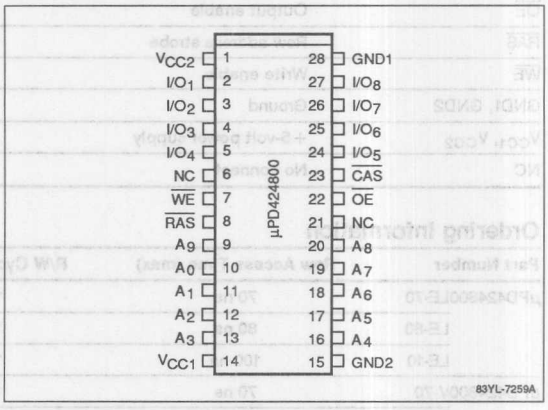
Since the μPD424800 is organized as 524,288 by eight bits wide, the addressing of the array by rows and columns is not symmetrical. Only 19 address bits are required to address the 524,288 locations. The μPD424800 uses row addresses A_0 through A_9 and column addresses A_0 through A_8. The column address bit A_9 is not used internally, but it must still meet all setup and hold times and specified voltage levels.

Features

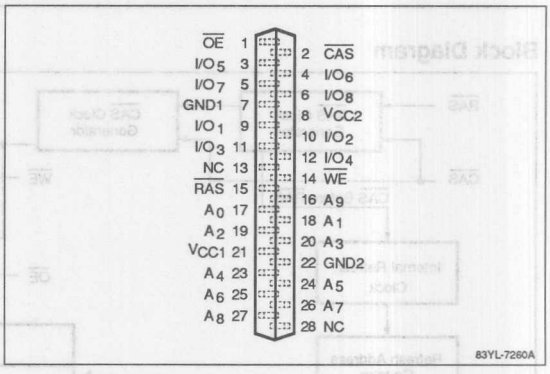
- 524,288 by 8-bit organization
- Single + 5-volt power supply
- Fast-page option (Address A_0 - A_8 only)
- Low power dissipation
- $\overline{CAS}$ before $\overline{RAS}$ refreshing
- On-chip substrate bias generator
- TTL-compatible inputs and outputs
- Nonlatched, three-state outputs
- Low input capacitance
- Multiplexed row (A_0 - A_9) and column (A_0 - A_8) addresses
- 1024 refresh cycles every 16 ms
- 28-pin plastic SOJ or 28-pin plastic ZIP packaging

Pin Configurations

28-Pin Plastic SOJ



28-Pin Plastic ZIP



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Pin Identification

Name	Function
A_0 - A_9	Address inputs
I/O_1 - I/O_8	Data inputs and outputs
$\overline{CAS}$	Column address strobe
$\overline{OE}$	Output enable
$\overline{RAS}$	Row address strobe
$\overline{WE}$	Write enable
GND1, GND2	Ground
V_{CC1}, V_{CC2}	+5-volt power supply
NC	No connect

Absolute Maximum Ratings

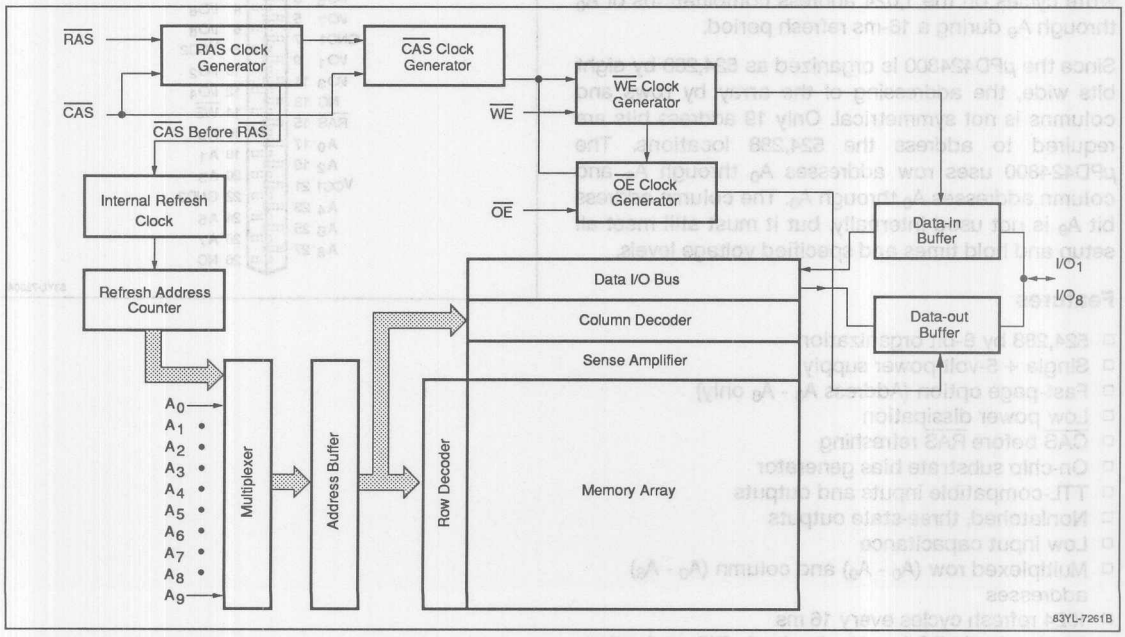
Voltage on any pin relative to GND	−1.0 to +7.0 V
Operating temperature, T_{OPR}	0 to +70°C
Storage temperature, T_{STG}	−55 to +125°C
Short-circuit output current, I_{OS}	50 mA
Power dissipation, P_D	1.0 W

Exposure to Absolute Maximum Ratings for extended periods may affect device reliability; exceeding the ratings could cause permanent damage. The device should be operated within the limits specified under DC and AC Characteristics.

Ordering Information

Part Number	Row Access Time (max)	R/W Cycle Time (min)	Fast-Page Cycle (min)	Package
μPD424800LE-70	70 ns	140 ns	45 ns	28-pin plastic SOJ
LE-80	80 ns	160 ns	50 ns	
LE-10	100 ns	190 ns	60 ns	
μPD424800V-70	70 ns	140 ns	45 ns	28-pin plastic ZIP
V-80	80 ns	160 ns	50 ns	
V-10	100 ns	190 ns	60 ns	

Block Diagram



Recommended Operating Conditions

Parameter	Symbol	Min	Typ	Max	Unit
Input voltage, high	V_{IH}	2.4		V_{CC} + 1.0	V
Input voltage, low	V_{IL}	−1.0		0.8	V
Supply voltage	V_{CC}	4.5	5.0	5.5	V
Ambient temperature	T_A	0		70	°C

Capacitance

T_A = 25°C; f = 1 MHz

Parameter	Symbol	Max	Unit	Pins Under Test
Input capacitance	C_{I1}	5	pF	Addresses
	C_{I2}	7	pF	$\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$, $\overline{OE}$
Input/output capacitance	C_O	7	pF	I/O_1 - I/O_8

DC Characteristics

T_A = 0 to +70°C; V_{CC} = +5.0 ±10%

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions
Standby current	I_{CC2}			2.0	mA	$\overline{RAS}$ = $\overline{CAS}$ ≥ V_{IH} (min); I_O = 0 mA
				1.0	mA	$\overline{RAS}$ = $\overline{CAS}$ ≥ V_{CC} − 0.2 V; I_O = 0 mA
Input leakage current	$I_{I(L)}$	−10		10	μA	V_{IN} = 0 V to V_{CC}; all other pins not under test = 0 V
Output leakage current	$I_{O(L)}$	−10		10	μA	D_{OUT} disabled; V_{OUT} = 0 V to V_{CC}
Output voltage, low	V_{OL}			0.4	V	I_{OL} = 4.2 mA
Output voltage, high	V_{OH}	2.4			V	I_{OH} = −5 mA

AC Characteristics

T_A = 0 to +70°C; V_{CC} = +5.0 V ± 10%

		-70		-80		-10			
Parameter	Symbol	Min	Max	Min	Max	Min	Max	Unit	Test Conditions
Operating current, average	I_{CC1}		120		110		100	mA	$\overline{RAS}$, $\overline{CAS}$ cycling; t_{RC} = t_{RC} min (Note 5)
Operating current, $\overline{RAS}$-only refresh cycle, average	I_{CC3}		120		110		100	mA	$\overline{RAS}$ cycling; $\overline{CAS}$ ≥ V_{IH} min; t_{RC} = t_{RC} min (Note 5)
Operating current, fast-page cycle, average	I_{CC4}		100		90		80	mA	$\overline{RAS}$ ≤ V_{IL}; $\overline{CAS}$ cycling; t_{PC} = t_{PC} min (Note 5)
Operating current, $\overline{CAS}$ before $\overline{RAS}$ refresh cycle, average	I_{CC5}		120		110		100	mA	$\overline{RAS}$ cycling; $\overline{CAS}$ ≤ V_{IL} max; t_{RC} = t_{RC} min (Note 5)
Access time from column address	t_{AA}		35		40		50	ns	(Notes 3, 4, 7, 8)
Access time from $\overline{CAS}$ precharge (rising edge)	t_{ACP}		40		45		55	ns	(Notes 3, 4, 7, 8)
Column address setup time	t_{ASC}	0		0		0		ns	
Row address setup time	t_{ASR}	0		0		0		ns	
Column address to $\overline{WE}$ delay time	t_{AWD}	55		65		80		ns	(Note 14)
Access time from $\overline{CAS}$ (falling edge)	t_{CAC}		20		20		25	ns	(Notes 3, 4, 7, 8)
Column address hold time	t_{CAH}	17		20		20		ns	

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AC Characteristics (cont)

Parameter	Symbol	-70 Min	-70 Max	-80 Min	-80 Max	-10 Min	-10 Max	Unit	Test Conditions
$\overline{CAS}$ pulse width	t_{CAS}	20	10,000	20	10,000	25	10,000	ns	
$\overline{CAS}$ hold time for $\overline{CAS}$ before $\overline{RAS}$ refreshing	t_{CHR}	15		15		20		ns	
$\overline{CAS}$ to output in low-Z	t_{CLZ}	0		0		0		ns	(Note 4, 7)
$\overline{CAS}$ precharge time, fast-page cycle	t_{CP}	10		10		10		ns	
$\overline{CAS}$ precharge time	t_{CPN}	10		10		10		ns	
$\overline{CAS}$ to $\overline{RAS}$ precharge time	t_{CRP}	10		10		10		ns	(Note 10)
$\overline{CAS}$ hold time	t_{CSH}	70		80		100		ns	
$\overline{CAS}$ setup time for $\overline{CAS}$ before $\overline{RAS}$ refresh cycle	t_{CSR}	10		10		10		ns	
$\overline{CAS}$ to $\overline{WE}$ delay	t_{CWD}	40		45		55		ns	(Note 14)
Write command referenced to $\overline{CAS}$ lead time	t_{CWL}	15		15		20		ns	
Data-in hold time	t_{DH}	15		15		20		ns	(Note 13)
Data-in setup time	t_{DS}	0		0		0		ns	(Note 13)
Access time from $\overline{OE}$	t_{OEA}		20		20		25	ns	(Notes 3, 4, 7, 8)
$\overline{OE}$ data delay time	t_{OED}	15		20		25		ns	
$\overline{OE}$ command hold time	t_{OEH}	0		0		0		ns	
$\overline{OE}$ to $\overline{RAS}$ inactive setup time	t_{OES}	0		0		0		ns	
Output turnoff delay from $\overline{OE}$	t_{OEZ}	0	15	0	20	0	25	ns	(Note 9)
Output buffer turnoff delay	t_{OFF}	0	15	0	20	0	25	ns	(Note 9)
$\overline{OE}$ to output in low-Z	t_{OLZ}	0		0		0		ns	(Note 5, 7)
Fast-page read or write cycle time	t_{PC}	45		50		60		ns	(Note 6)
Fast-page read-modify-write cycle time	t_{PRWC}	90		100		120		ns	(Note 6)
Access time from $\overline{RAS}$	t_{RAC}		70		80		100	ns	(Notes 3, 4, 7, 8)

AC Characteristics (cont)

Parameter	Symbol	-70 Min	-70 Max	-80 Min	-80 Max	-10 Min	-10 Max	Unit	Test Conditions
$\overline{RAS}$ to column address delay time	t_{RAD}	15	35	17	40	17	50	ns	(Note 8)
Row address hold time	t_{RAH}	10		12		12		ns	
Column address lead time referenced to $\overline{RAS}$ (rising edge)	t_{RAL}	35		40		50		ns	
$\overline{RAS}$ pulse width	t_{RAS}	70	10,000	80	10,000	100	10,000	ns	
$\overline{RAS}$ pulse width, fast-page cycle	t_{RASP}	70	125,000	80	125,000	100	125,000	ns	
Random read or write cycle time	t_{RC}	140		160		190		ns	(Note 6)
$\overline{RAS}$ to $\overline{CAS}$ delay time	t_{RCD}	20	50	25	60	25	75	ns	(Note 8)
Read command hold time referenced to $\overline{CAS}$	t_{RCH}	0		0		0		ns	(Note 11)
Read command setup time	t_{RCS}	0		0		0		ns	
Refresh period	t_{REF}		16		16		16	ms	Address A_0 through A_9
$\overline{RAS}$ precharge time	t_{RP}	60		70		80		ns	
$\overline{RAS}$ precharge $\overline{CAS}$ hold time	t_{RPC}	10		10		10		ns	
Read command hold time referenced to $\overline{RAS}$	t_{RRH}	10		10		10		ns	(Note 11)
$\overline{RAS}$ hold time	t_{RSH}	20		20		25		ns	
Read-modify-write cycle time	t_{RWC}	185		210		250		ns	(Note 6)
$\overline{RAS}$ to $\overline{WE}$ delay	t_{RWD}	90		105		130		ns	(Note 14)
Write command referenced to $\overline{RAS}$ lead time	t_{RWL}	20		20		25		ns	
Rise and fall transition time	t_T	3	50	3	50	3	50	ns	(Note 4)
Write command hold time	t_{WCH}	15		15		20		ns	(Note 12)
Write command setup time	t_{WCS}	0		0		0		ns	(Note 14)

6

AC Characteristics (cont)

Parameter	Symbol	-70 Min	-70 Max	-80 Min	-80 Max	-10 Min	-10 Max	Unit	Test Conditions
$\overline{WE}$ command hold time for $\overline{CAS}$ before $\overline{RAS}$ refreshing	t_{WHR}	15		15		20		ns	
Write command pulse width	t_{WP}	15		15		20		ns	(Note 12)
$\overline{WE}$ command setup time for $\overline{CAS}$ before $\overline{RAS}$ refreshing	t_{WSR}	10		10		10		ns	

Notes:

(1) All voltages are referenced to GND.

(2) An initial pause of 100 μs is required after power-up, followed by any eight $\overline{RAS}$ cycles, before proper device operation is achieved. At the end of the initial power-up sequence, it is recommended that either a $\overline{RAS}$-only refresh or a $\overline{CAS}$ before $\overline{RAS}$ refresh cycle be executed while $\overline{WE} \geq V_{IH}$ to ensure normal operation.

(3) Ac measurements assume $t_T = 5$ ns.

(4) V_{IH} (min) and V_{IL} (max) are reference levels for measuring the timing of input signals. Transition times are measured between V_{IH} and V_{IL}.

(5) I_{CC1}, I_{CC3}, I_{CC4}, and I_{CC5} depend on output loading and cycle rates. Specified values are obtained with the output open. I_{CC3} is measured assuming that all column address inputs are held at either a high level or a low level during $\overline{RAS}$-only refresh cycles. I_{CC4} is measured assuming that all column address inputs are switched only once during each fast-page cycle.

(6) The minimum specifications are used only to indicate the cycle time at which proper operation over the full temperature range (T_A = 0 to +70 °C) is assured.

(7) Load = 2 TTL (−1 mA, +4 mA) loads and 100 pF (V_{OH} = 2.0 V and V_{OL} = 0.8 V).

(8) If $t_{RCD} \leq t_{RCS}$ (max) and $t_{RAD} \leq t_{RAD}$ (max) access time is defined by t_{RAC} (max). If $t_{RCD} \geq t_{RCD}$ (max) access time is defined by t_{CAC} (max) and if $t_{RAD} \geq t_{RAD}$ (max) access time is defined by t_{AA} (max).

(9) t_{OFF} (max) and t_{OEZ} (max) define the time at which the outputs achieve the open-circuit condition and are not referenced to V_{OH} or V_{OL}.

(10) The t_{CRP} requirement should be applicable for $\overline{RAS}$/$\overline{CAS}$ cycles preceded by any cycle.

(11) Either t_{RRH} or t_{RCH} must be satisfied for a read cycle.

(12) Parameter t_{WP} is applicable for a delayed write cycle such as a read-write/read-modify-write cycle. For early write cycles, both t_{WCS} and t_{WCH} must be met.

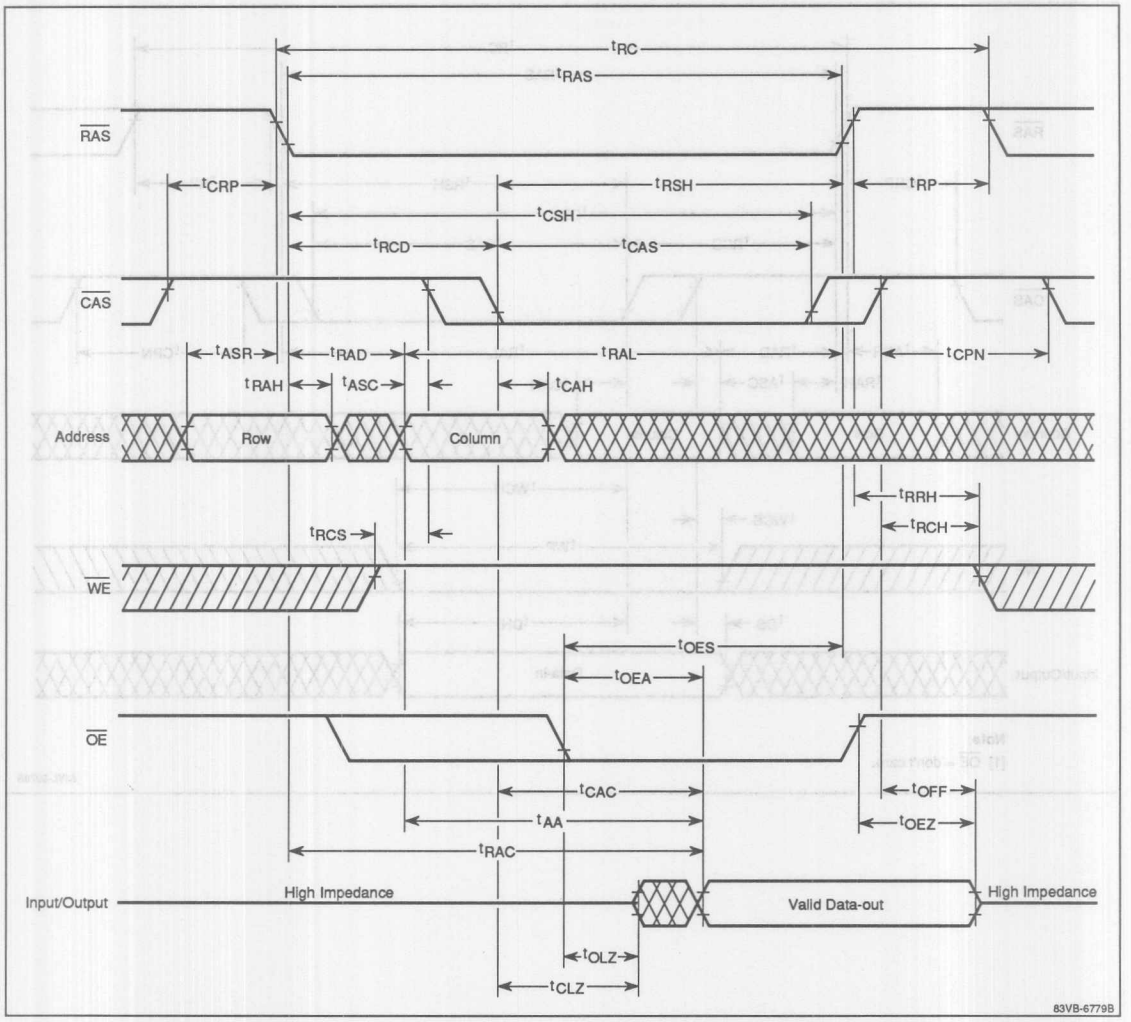
(13) These parameters are referenced to the falling edge of $\overline{CAS}$ for early write cycles and to the falling edge of $\overline{WE}$ for delayed write or read-modify-write cycles.

(14) t_{WCS}, t_{RWD}, t_{CWD}, and t_{AWD} are restrictive operating parameters in read-write/read-modify-write cycles only. If $t_{WCS} \geq t_{WCS}$ (min), the cycle is an early write cycle and the data I/O pins will remain open-circuit throughout the entire cycle. If $t_{CWD} \geq t_{CWD}$ (min), $t_{RWD} \geq t_{RWD}$ (min), and $t_{AWD} \geq t_{AWD}$ (min), then the cycle is a read-write cycle and the data I/O pins will contain data read from the selected cells. If neither of the above conditions is met, the condition of the data I/O pins (at access time and until $\overline{CAS}$ returns to V_{IH}) is indeterminate.

(15) Assumes that the test mode has been set. Contact your NEC Electronics sales representative for more details. A test mode may be initiated by executing a $\overline{CAS}$ before $\overline{RAS}$ refresh cycle with $\overline{WE}$ held at V_{IL}. This mode also may inadvertantly be initiated during power-up because external control of the signal lines is very difficult during this period. It is therefore recommended that while $\overline{WE}$ is held at V_{IH}, either a $\overline{RAS}$-only or $\overline{CAS}$ before $\overline{RAS}$ refresh cycle should be executed at any time after the end of the initial power-up sequence to ensure normal device operation.

Timing Waveforms

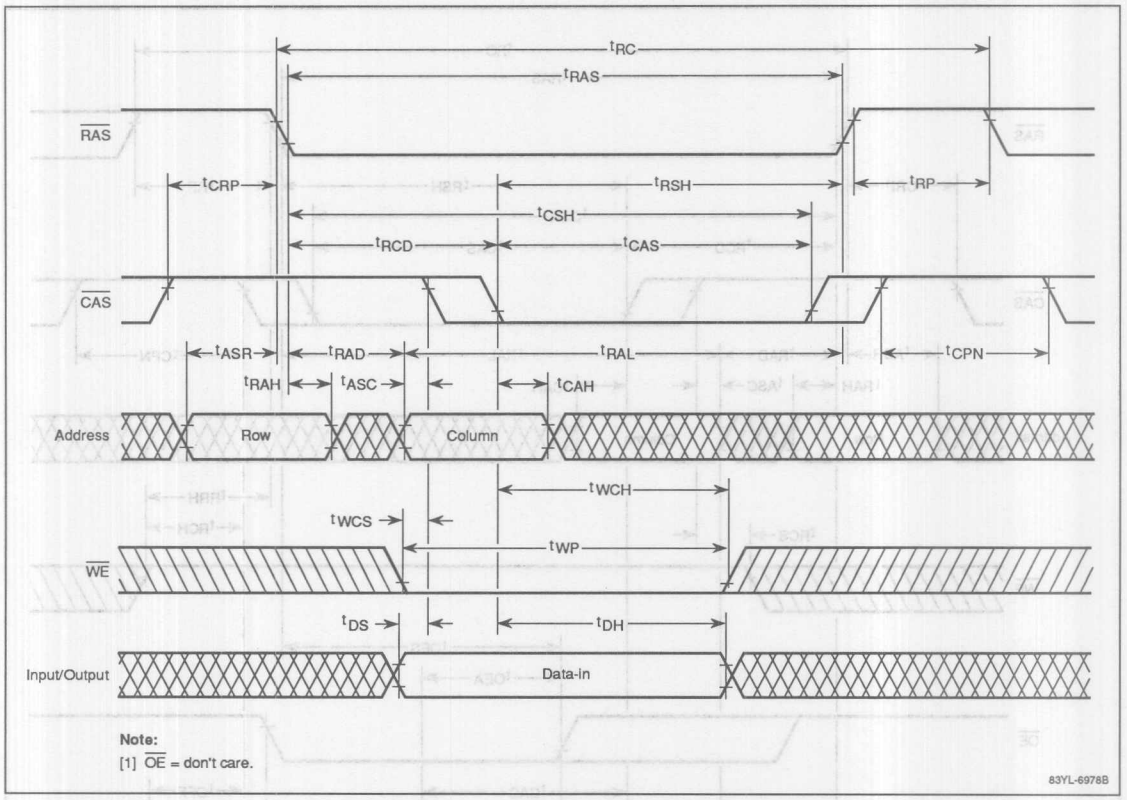
Read Cycle



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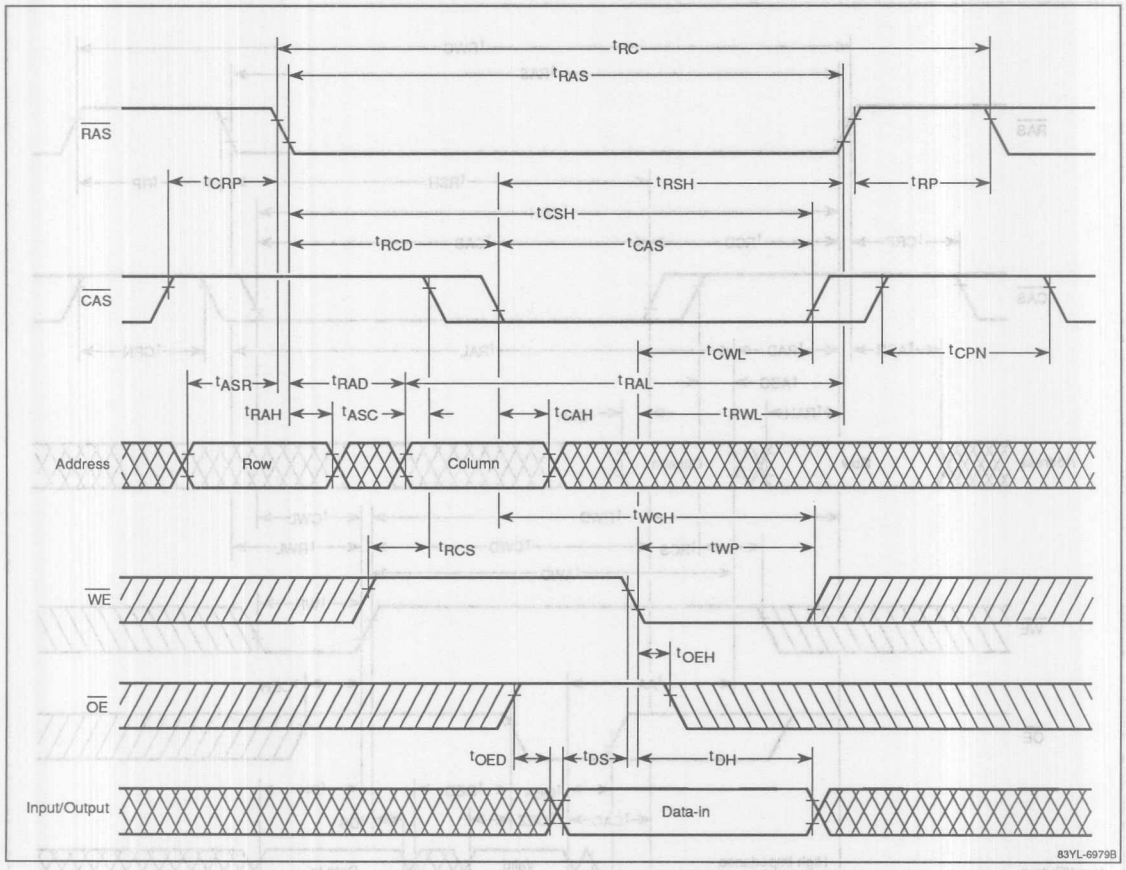
Timing Waveforms (cont)

Early Write Cycle



Timing Waveforms (cont)

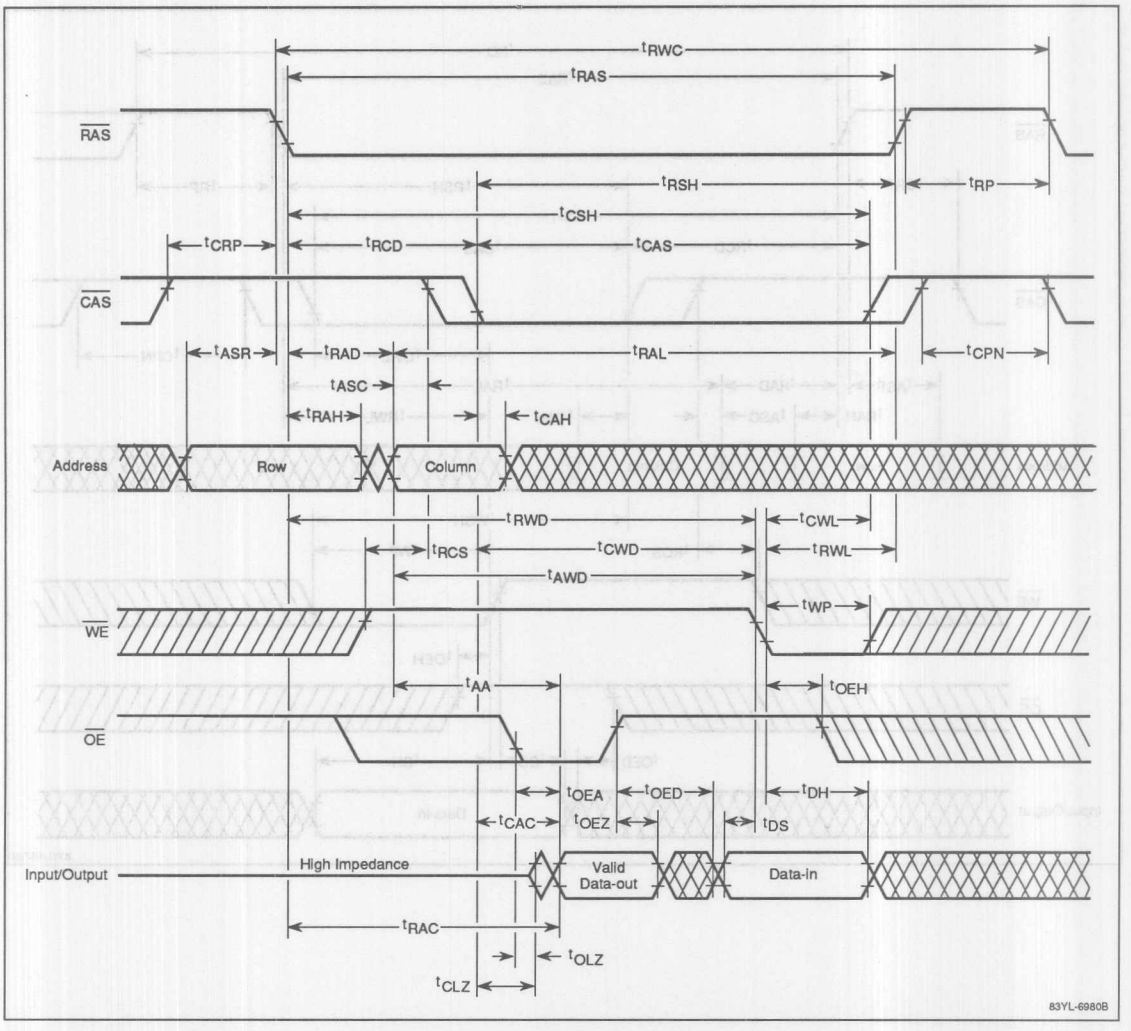
Late Write Cycle



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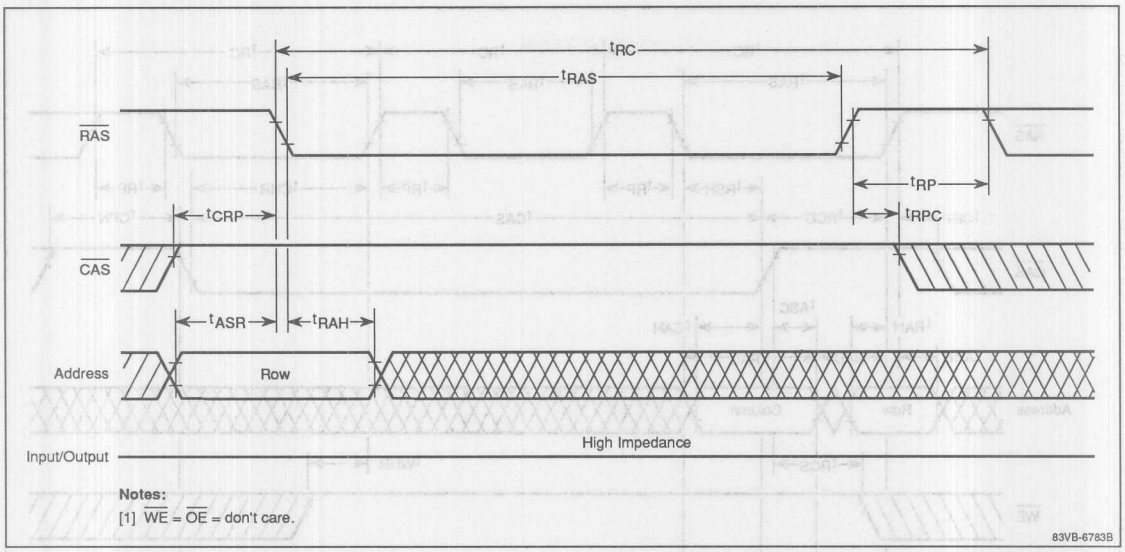
Timing Waveforms (cont)

Read-Write/Read-Modify-Write Cycle

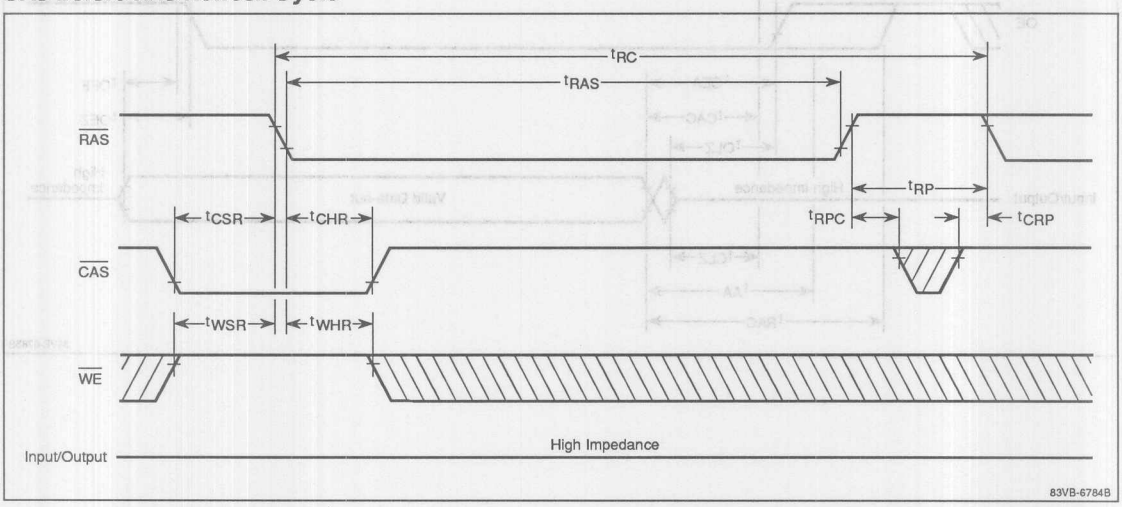


Timing Waveforms (cont)

$\overline{RAS}$-Only Refresh Cycle



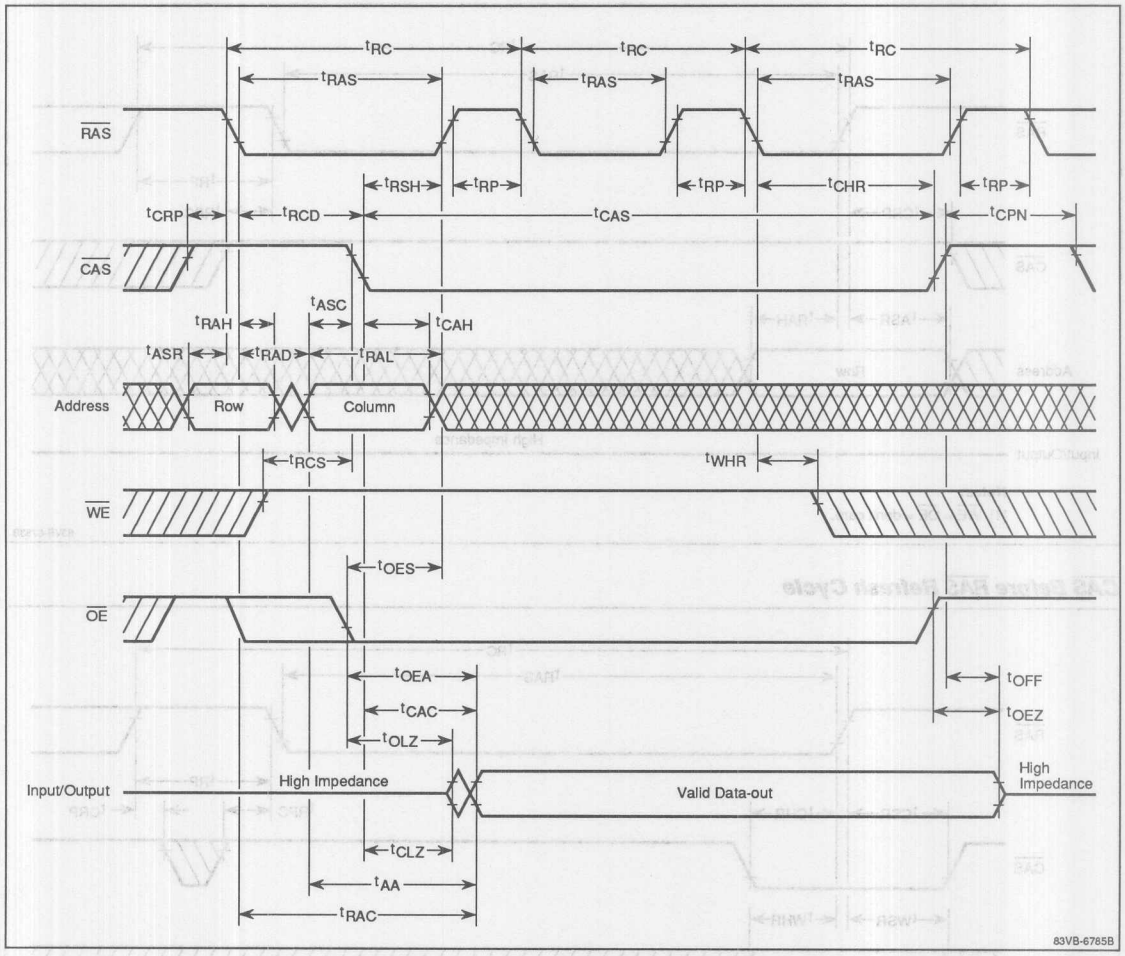
$\overline{CAS}$ Before $\overline{RAS}$ Refresh Cycle



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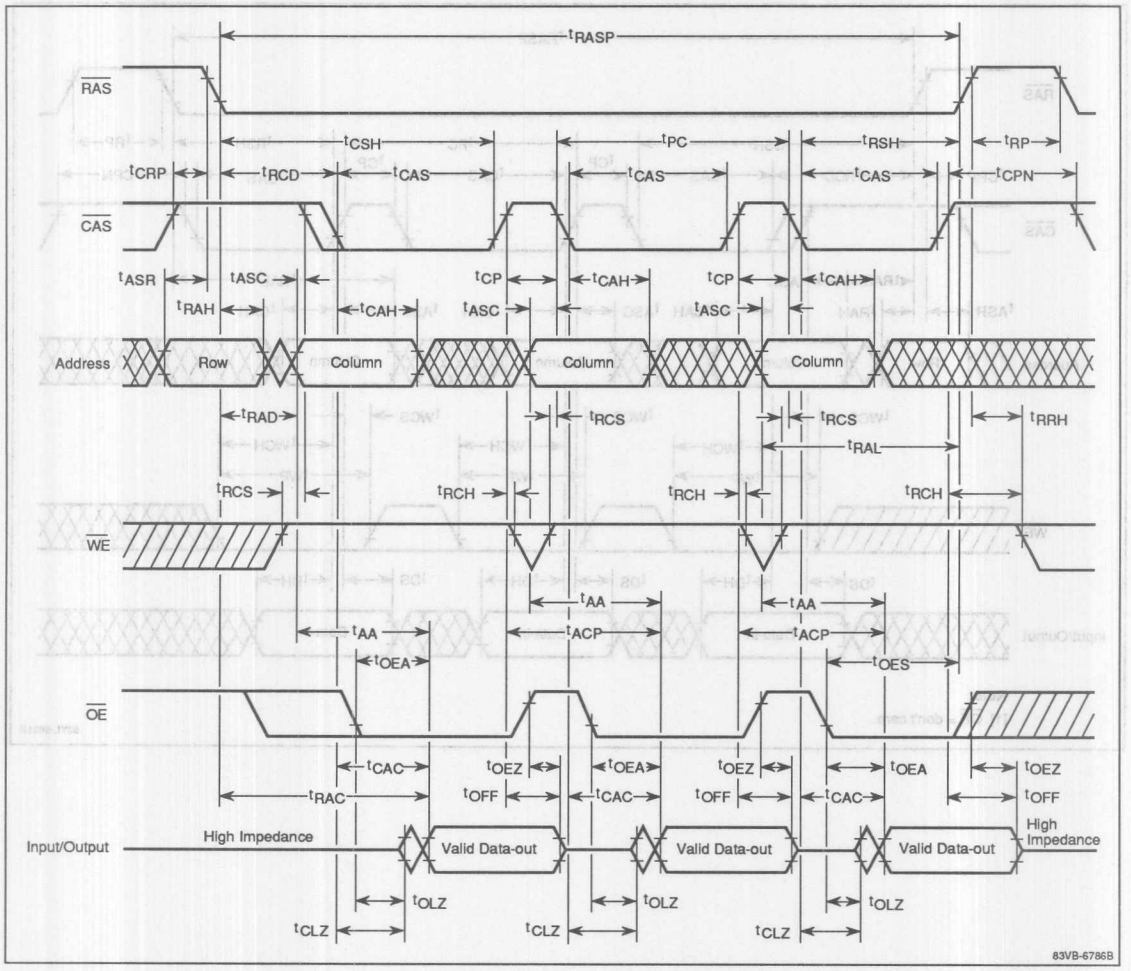
Timing Waveforms (cont)

Hidden Refresh Cycle



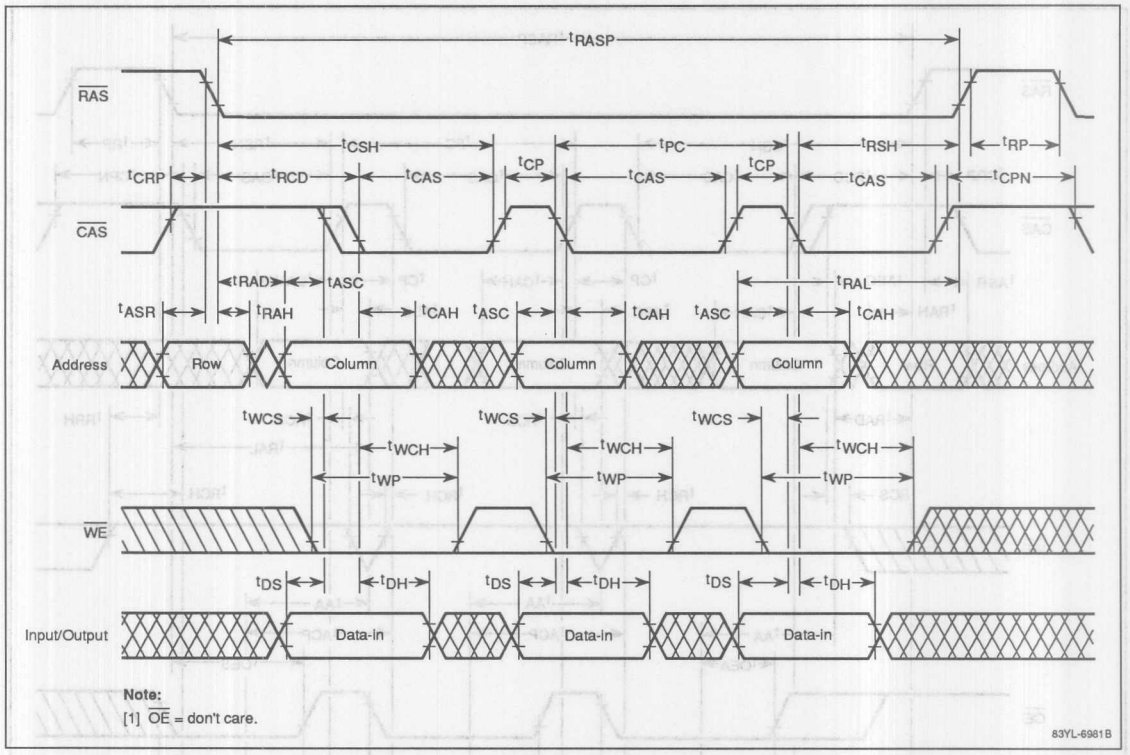
Timing Waveforms (cont)

Fast-Page Read Cycle



Timing Waveforms (cont)

Fast-Page Early Write Cycle

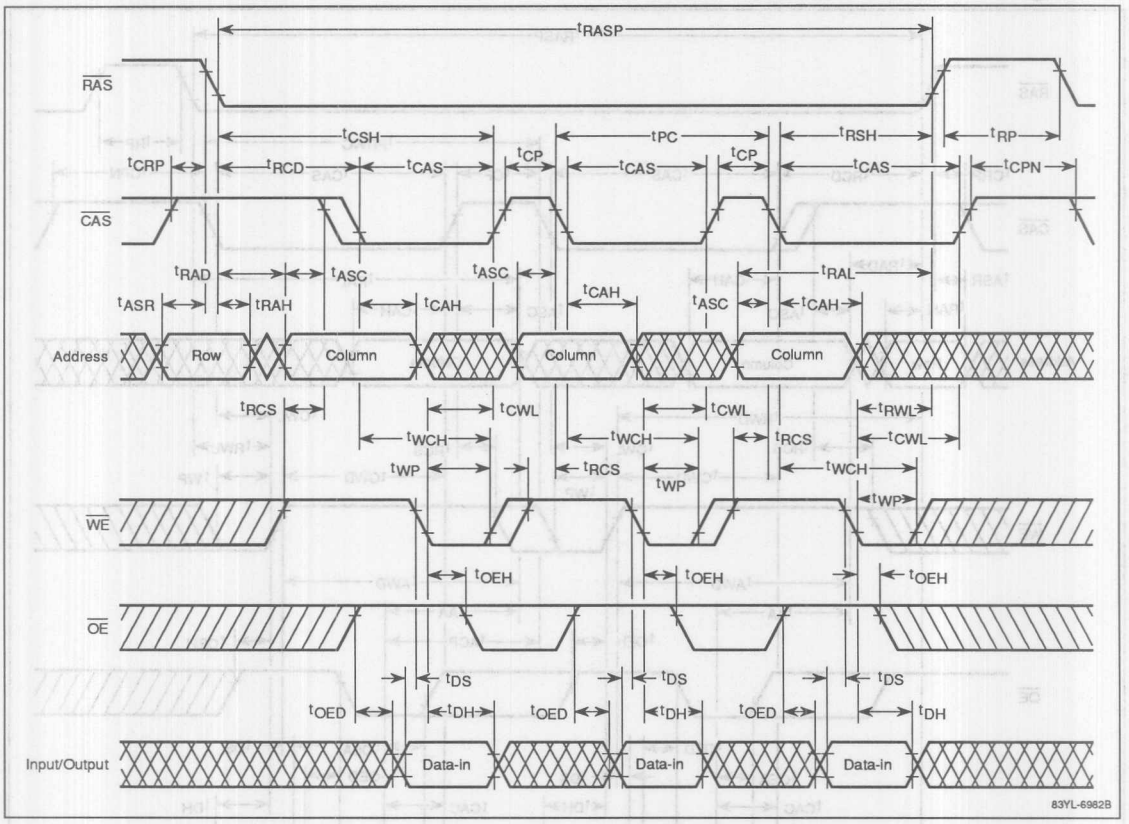


Note:
[1] $\overline{OE}$ = don't care.

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Timing Waveforms (cont)

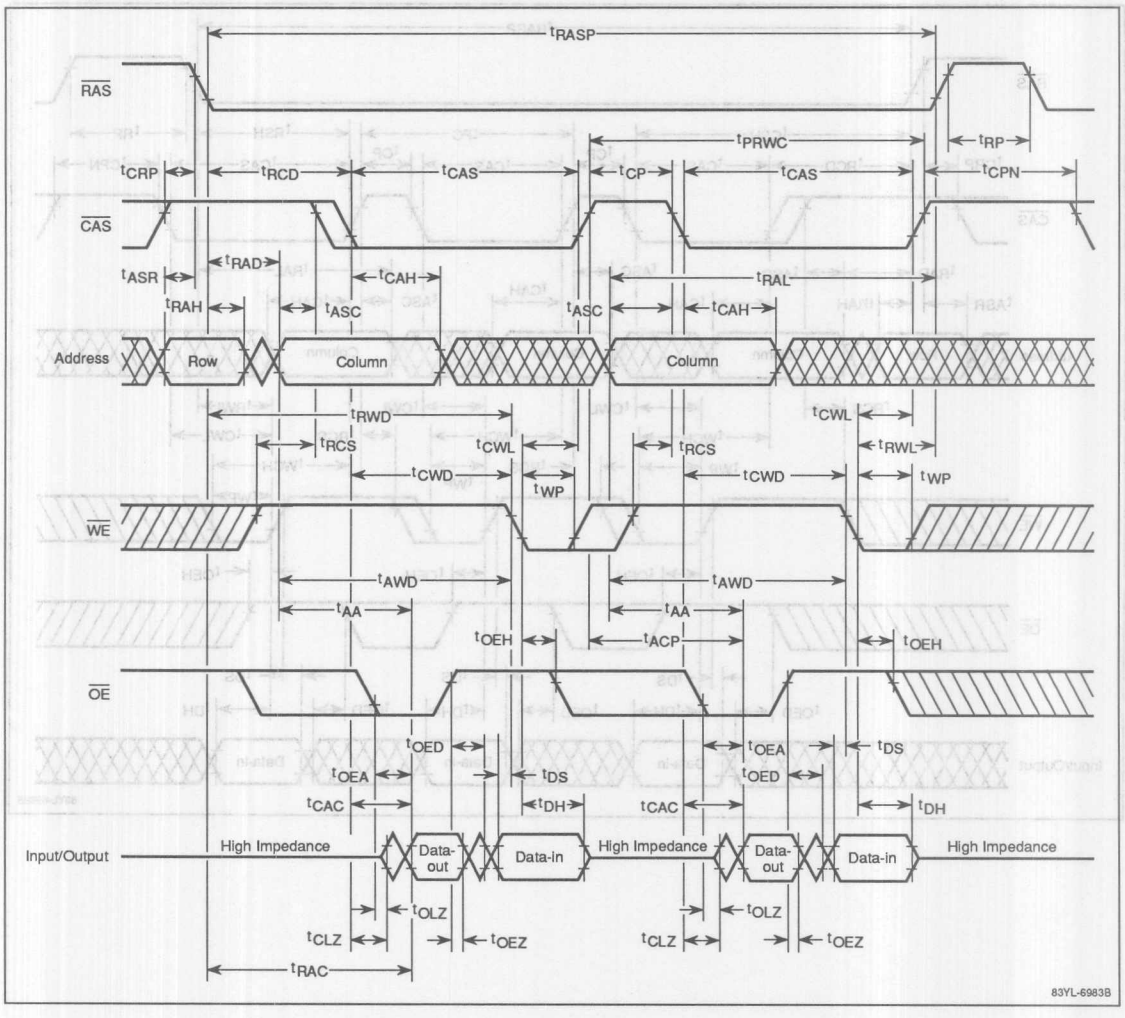
Fast-Page Late Write Cycle



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Timing Waveforms (cont)

Fast-Page Read-Write/Read-Modify-Write Cycle



Description

NEC's μPD421000, μPD421001, and μPD421002 are 1-megabit dynamic RAMs (DRAMs) manufactured with the CMOS 1-μm fine-pattern process and configured as 1,048,576 x 1 bit. As shown in table 1, this family of DRAMs has been developed in a variety of speeds and packages. The package pin layouts appear in figure 1.

Configurations

The μPD421000, μPD421001, and μPD421002 (figures 2, 3, and 4) consist of memory cell arrays, input and output buffers, clock generators, refresh address counters, and row and column decoders.

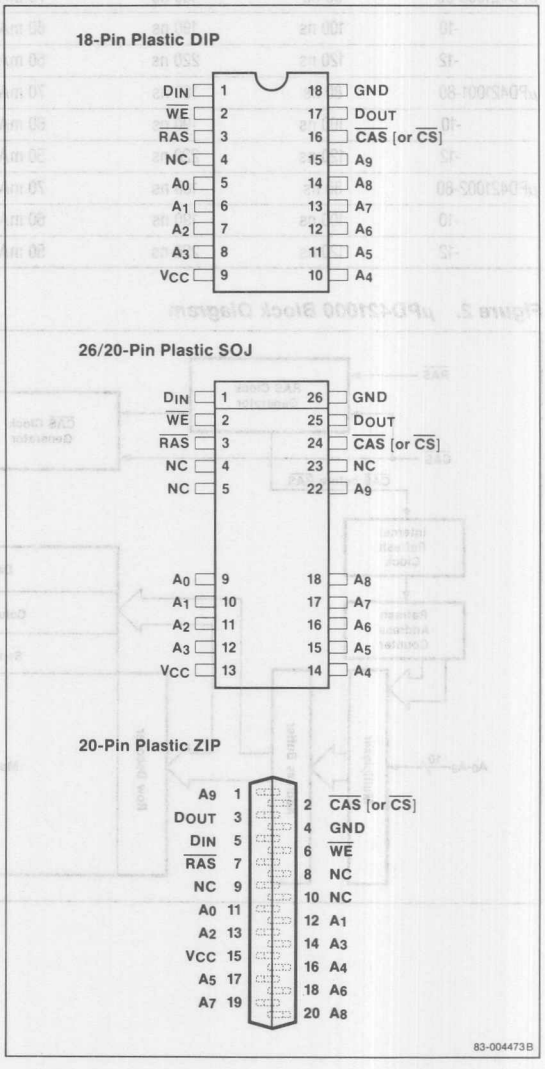
The basic layout of the chips is shown in figure 5. As can be seen from the diagram, the whole memory cell array is divided into 16 smaller 64-kilobit arrays that are accessed separately.

Memory Cell Structure

Dynamic RAMs generally feature one-transistor memory cells, which require only about one-fourth of the area used by four-transistor and six-transistor (flip-flop) memory cells in static RAMs. Although a one-transistor cell provides a big advantage in reducing chip size, data must be rewritten (refreshed) at regular intervals for proper data storage on the memory cell capacitor. A cross-sectional view of the trench-type, one-transistor memory cell used in the μPD421000-series DRAMs is shown in figure 6.

This trench design uses three-dimensional rather than planar capacitors, thereby achieving a larger capacitance in a smaller surface area than in conventional circuits. The capacitance of this type of cell is determined by total trench area, the dielectric constant, and the thickness of the insulating film. To reduce soft errors caused by α-particles, an effective capacitance in excess of 50 femtofarads (fF) is used in the μPD421000, μPD421001, and μPD421002.

Figure 1. Pin Layouts



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Table 1. 1,048,576 x 1-Bit DRAM Family

Device	$\overline{RAS}$ Access Time (max)	R/W Cycle Time (min)	Operating Current (max)	Standby Current (max)	High-Speed Mode	Packages
μPD421000-80	80 ns	160 ns	70 mA	1 mA	Fast Page	C = 18-pin plastic DIP
-10	100 ns	190 ns	60 mA	1 mA		V = 20-pin plastic ZIP
-12	120 ns	220 ns	50 mA	1 mA		LA = 26/20-pin plastic SOJ
μPD421001-80	80 ns	160 ns	70 mA	1 mA	Nibble	
-10	100 ns	190 ns	60 mA	1 mA		
-12	120 ns	220 ns	50 mA	1 mA		
μPD421002-80	80 ns	160 ns	70 mA	1 mA	Static Column	
-10	100 ns	190 ns	60 mA	1 mA		
-12	120 ns	220 ns	50 mA	1 mA		

Figure 2. μPD421000 Block Diagram

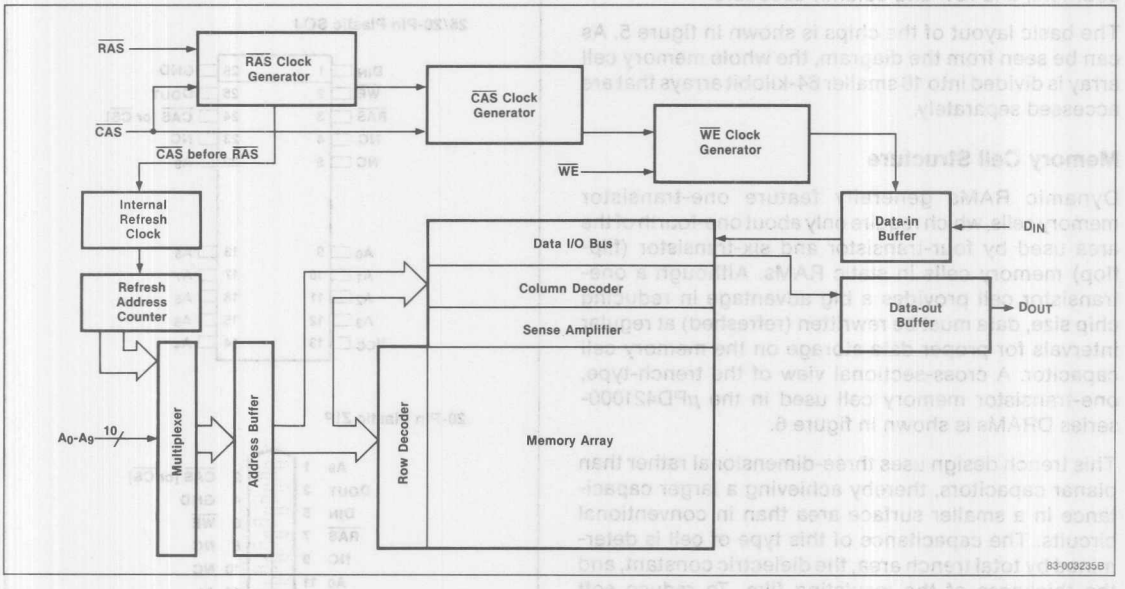


Figure 3. μPD421001 Block Diagram

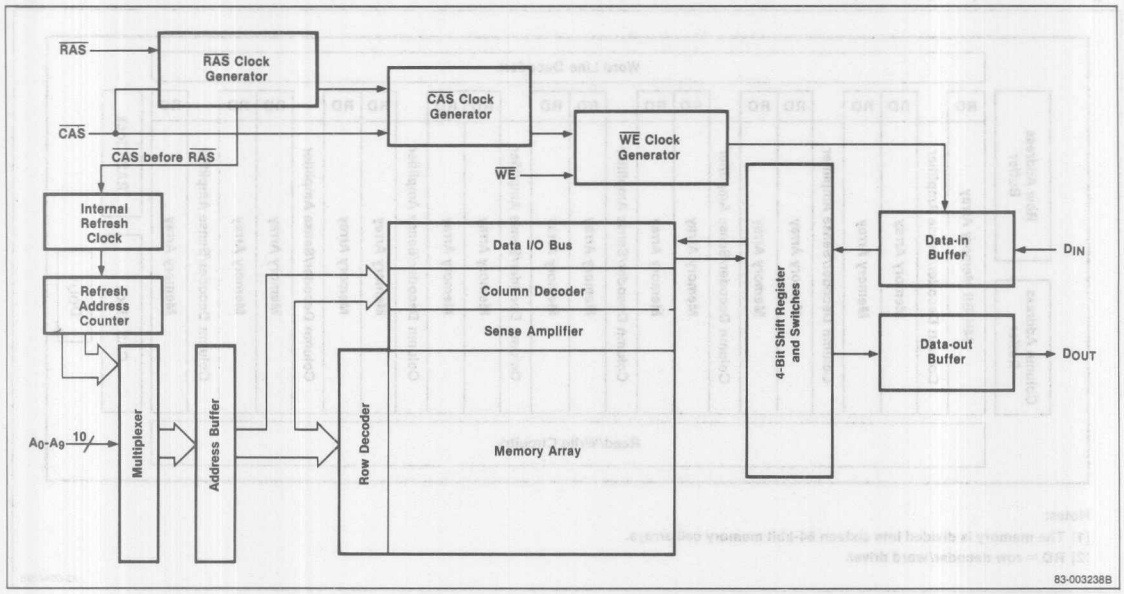
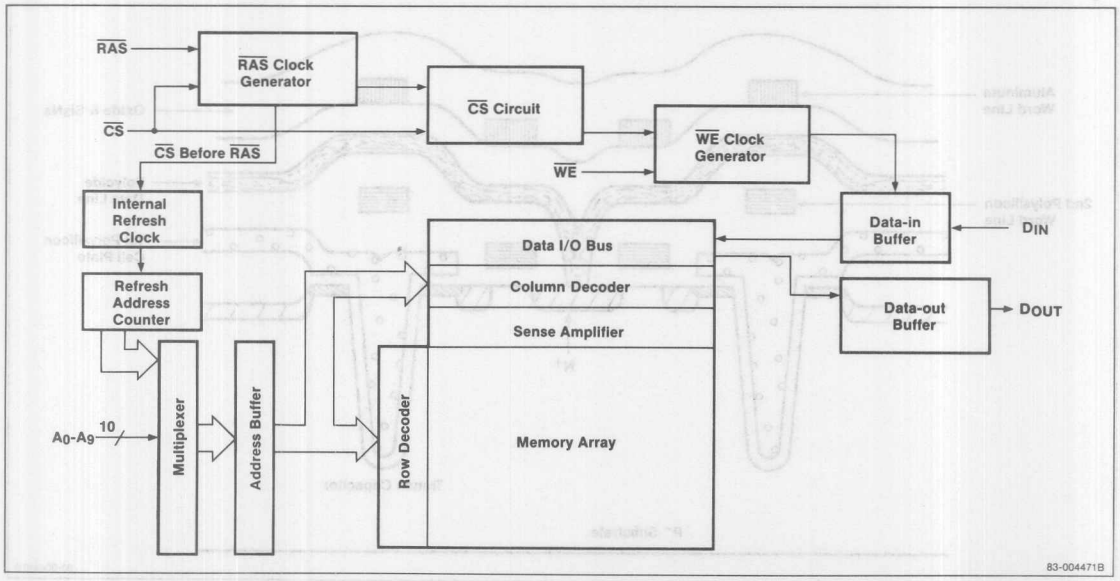
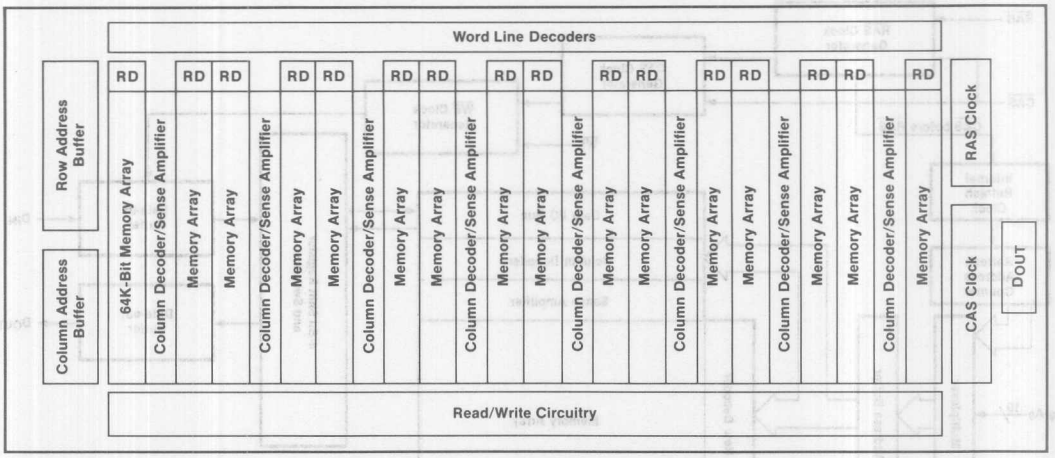


Figure 4. μPD421002 Block Diagram



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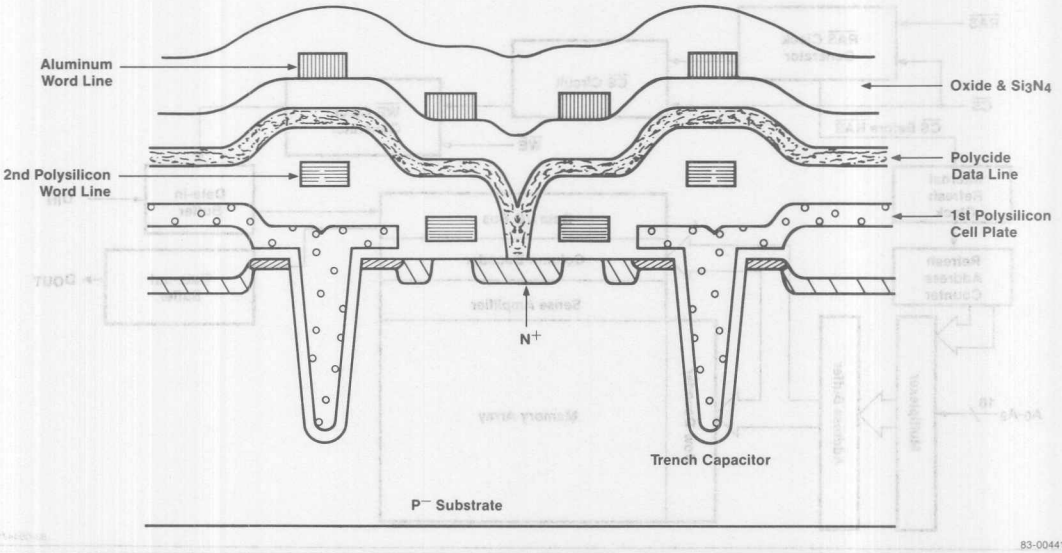
Figure 5. Chip Layout of μPD421000-Series DRAMs



Notes:
[1] The memory is divided into sixteen 64-kbit memory cell arrays.
[2] RD = row decoder/word driver.

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Figure 6. Cross Section of 1-Transistor Memory Cell



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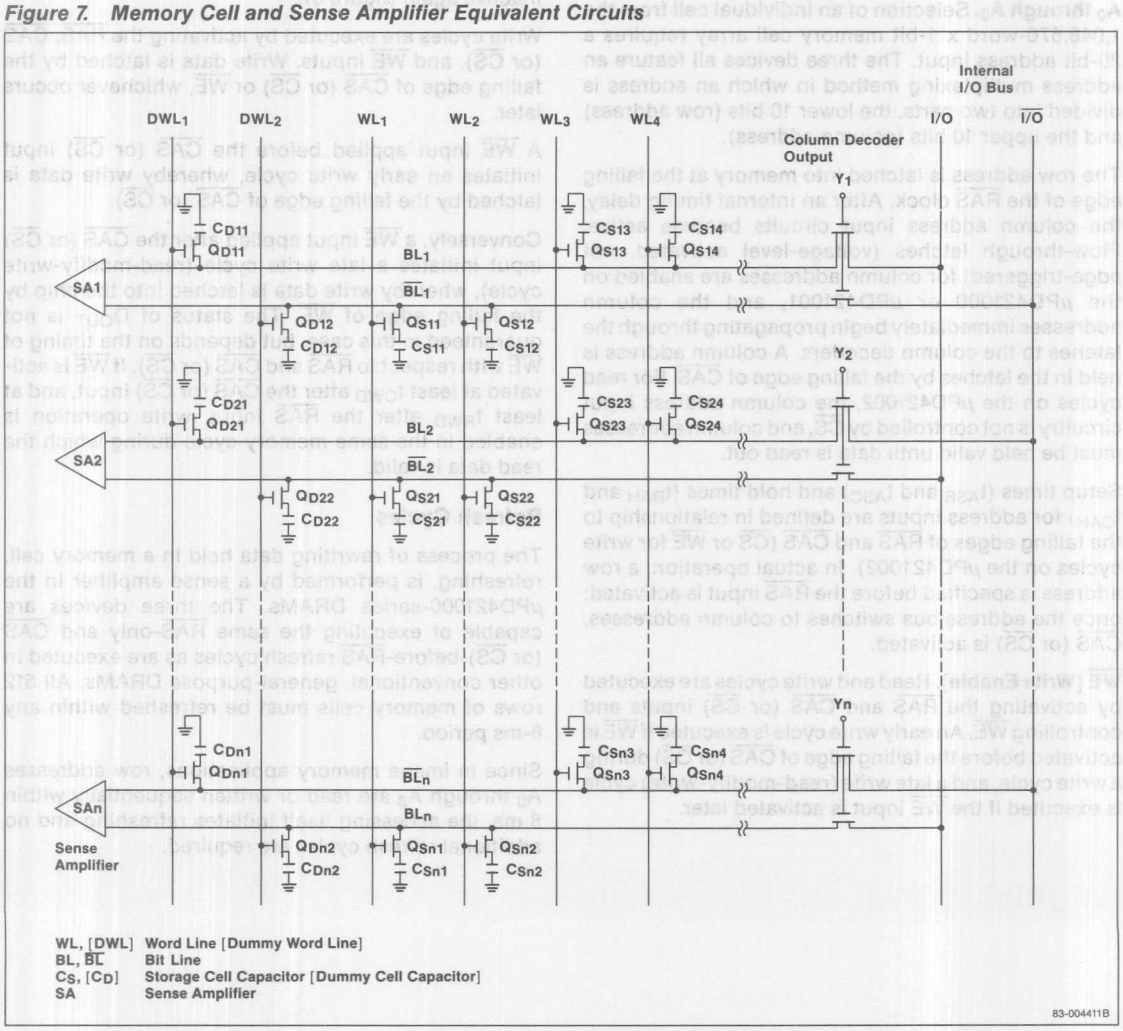
Read/Write Operation

In dynamic RAMs, changes in bit line potential caused by the minute charging and discharging of memory cells are amplified by a sense amplifier to be read as either 1 or 0. Memory cell and sense amplifier equivalent circuits are shown in figure 7.

To read the data from storage cell C_{S11}, the row address selects word line WL_1, and data from memory cells C_{S11}, C_{S21}, . . . , C_{Sn1} connected to WL_1 is passed to bit lines BL_1, BL_2, . . . , BL_n. These data signals are passed to the sense amplifiers, where they first are compared with data from dummy cells C_{D11}, C_{D21}, . . . , C_{Dn1}, connected simultaneously with the memory cells, and then amplified. At the same time, the original data is rewritten to memory cells C_{S11}, C_{S21}, . . ., C_{Sn1}. Switch Y_1 is then selected by the column address, and the C_{S11} data on the BL_1 line is passed via the I/O bus and a data amplifier to external circuits.

Write and read operations are identical, up to amplification and rewriting of memory cell data selected by a row address. After being passed to the bit line selected by the column address, write data is written into a target memory cell (such as C_{S11}). Since the number of memory cells selected by one row address in the devices is 2048, 2048 memory cells are refreshed simultaneously in each memory or refresh cycle.

Figure 7. Memory Cell and Sense Amplifier Equivalent Circuits



Pin Functions

$\overline{RAS}$ and $\overline{CAS}$ [or $\overline{CS}$]. The μPD421000-series DRAMs include two chip activator inputs: $\overline{RAS}$ and $\overline{CAS}$ (or $\overline{CS}$), row address strobe and column address strobe (or chip select). In addition to reading row addresses A_0 through A_9, selecting the relevant word line, and activating the sense amplifiers for read and write operation, the $\overline{RAS}$ input also refreshes the 2048 bits selected by row addresses A_0 through A_8. The $\overline{CAS}$ input latches in column addresses (on the μPD421000 and the μPD421001) and connects the chip's internal I/O bus to the sense amplifiers activated by the $\overline{RAS}$ clock, thereby executing data input or output operations.

A_0 through A_9. Selection of an individual cell from the 1,048,576-word x 1-bit memory cell array requires a 20-bit address input. The three devices all feature an address multiplexing method in which an address is divided into two parts, the lower 10 bits (row address) and the upper 10 bits (column address).

The row address is latched into memory at the falling edge of the $\overline{RAS}$ clock. After an internal timing delay, the column address input circuits become active. Flow-through latches (voltage-level activated, not edge-triggered) for column addresses are enabled on the μPD421000 or μPD421001, and the column addresses immediately begin propagating through the latches to the column decoders. A column address is held in the latches by the falling edge of $\overline{CAS}$. For read cycles on the μPD421002, the column address input circuitry is not controlled by $\overline{CS}$, and column addresses must be held valid until data is read out.

Setup times (t_{ASR} and t_{ASC}) and hold times (t_{RAH} and t_{CAH}) for address inputs are defined in relationship to the falling edges of $\overline{RAS}$ and $\overline{CAS}$ ($\overline{CS}$ or $\overline{WE}$ for write cycles on the μPD421002). In actual operation, a row address is specified before the $\overline{RAS}$ input is activated; once the address bus switches to column addresses, $\overline{CAS}$ (or $\overline{CS}$) is activated.

$\overline{WE}$ [Write Enable]. Read and write cycles are executed by activating the $\overline{RAS}$ and $\overline{CAS}$ (or $\overline{CS}$) inputs and controlling $\overline{WE}$. An early write cycle is executed if $\overline{WE}$ is activated before the falling edge of $\overline{CAS}$ (or $\overline{CS}$) during a write cycle, and a late write (read-modify-write) cycle is executed if the $\overline{WE}$ input is activated later.

Read and Write Cycles

Read cycles are executed by activating $\overline{RAS}$ and $\overline{CAS}$ (or $\overline{CS}$) with the $\overline{WE}$ input at a high level (inactive). The $\overline{RAS}$ access time of t_{RAC} is valid if the delay from $\overline{RAS}$ to $\overline{CAS}$ (or $\overline{CS}$) is less than t_{RCD} (max), and the delay from $\overline{RAS}$ to the column address is less than t_{RAD} (max). The $\overline{CAS}$ (or $\overline{CS}$) access time of t_{CAC} is valid if the delay from $\overline{RAS}$ to $\overline{CAS}$ (or $\overline{CS}$) is greater than t_{RCD} (max), and the delay from the column address to $\overline{CAS}$ (or $\overline{CS}$) is greater than t_{ASC} (max). The address access time of t_{AA} is valid if the delay from $\overline{RAS}$ to the column address is greater than t_{RAD} (max), and the delay from the column address to $\overline{CAS}$ (or $\overline{CS}$) is less than t_{ASC} (max). Output data is held valid until $\overline{CAS}$ (or $\overline{CS}$) becomes inactive again (figure 8).

Write cycles are executed by activating the $\overline{RAS}$, $\overline{CAS}$ (or $\overline{CS}$), and $\overline{WE}$ inputs. Write data is latched by the falling edge of $\overline{CAS}$ (or $\overline{CS}$) or $\overline{WE}$, whichever occurs later.

A $\overline{WE}$ input applied before the $\overline{CAS}$ (or $\overline{CS}$) input initiates an early write cycle, whereby write data is latched by the falling edge of $\overline{CAS}$ (or $\overline{CS}$).

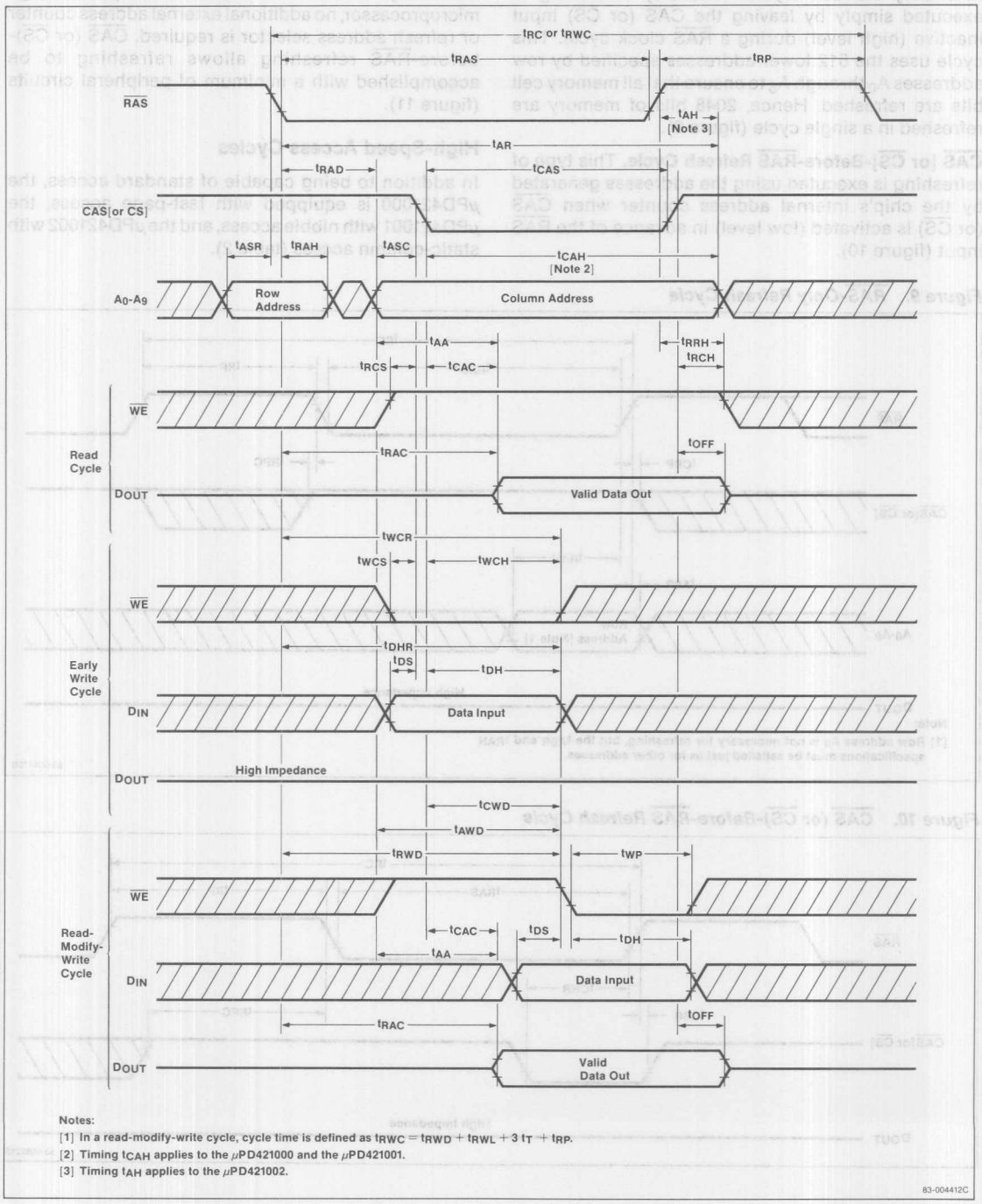
Conversely, a $\overline{WE}$ input applied after the $\overline{CAS}$ (or $\overline{CS}$) input initiates a late write cycle (read-modify-write cycle), whereby write data is latched into the chip by the falling edge of $\overline{WE}$. The status of D_{OUT} is not guaranteed in this case, but depends on the timing of $\overline{WE}$ with respect to $\overline{RAS}$ and $\overline{CAS}$ (or $\overline{CS}$). If $\overline{WE}$ is activated at least t_{CWD} after the $\overline{CAS}$ (or $\overline{CS}$) input, and at least t_{RWD} after the $\overline{RAS}$ input, write operation is enabled in the same memory cycle during which the read data is valid.

Refresh Cycles

The process of rewriting data held in a memory cell, refreshing, is performed by a sense amplifier in the μPD421000-series DRAMs. The three devices are capable of executing the same $\overline{RAS}$-only and $\overline{CAS}$ (or $\overline{CS}$)-before-$\overline{RAS}$ refresh cycles as are executed in other conventional, general-purpose DRAMs. All 512 rows of memory cells must be refreshed within any 8-ms period.

Since in image memory applications, row addresses A_0 through A_8 are read or written sequentially within 8 ms, the accessing itself initiates refreshing and no additional refresh cycles are required.

Figure 8. Access Timing



Notes:

[1] In a read-modify-write cycle, cycle time is defined as $t_{RWC} = t_{RWD} + t_{RWL} + 3\,t_T + t_{RP}$.

[2] Timing t_{CAH} applies to the μPD421000 and the μPD421001.

[3] Timing t_{AH} applies to the μPD421002.

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$\overline{RAS}$-Only Refresh Cycle. $\overline{RAS}$-only refreshing is executed simply by leaving the $\overline{CAS}$ (or $\overline{CS}$) input inactive (high level) during a $\overline{RAS}$ clock cycle. This cycle uses the 512 lower addresses specified by row addresses A_0 through A_8 to ensure that all memory cell bits are refreshed. Hence, 2048 bits of memory are refreshed in a single cycle (figure 9).

$\overline{CAS}$ [or $\overline{CS}$]-Before-$\overline{RAS}$ Refresh Cycle. This type of refreshing is executed using the addresses generated by the chip's internal address counter when $\overline{CAS}$ (or $\overline{CS}$) is activated (low level) in advance of the $\overline{RAS}$ input (figure 10).

Even in systems without an address output from the microprocessor, no additional external address counter or refresh address selector is required. $\overline{CAS}$ (or $\overline{CS}$)-before-$\overline{RAS}$ refreshing allows refreshing to be accomplished with a minimum of peripheral circuits (figure 11).

High-Speed Access Cycles

In addition to being capable of standard access, the μPD421000 is equipped with fast-page access, the μPD421001 with nibble access, and the μPD421002 with static-column access (table 2).

Figure 9. $\overline{RAS}$-Only Refresh Cycle

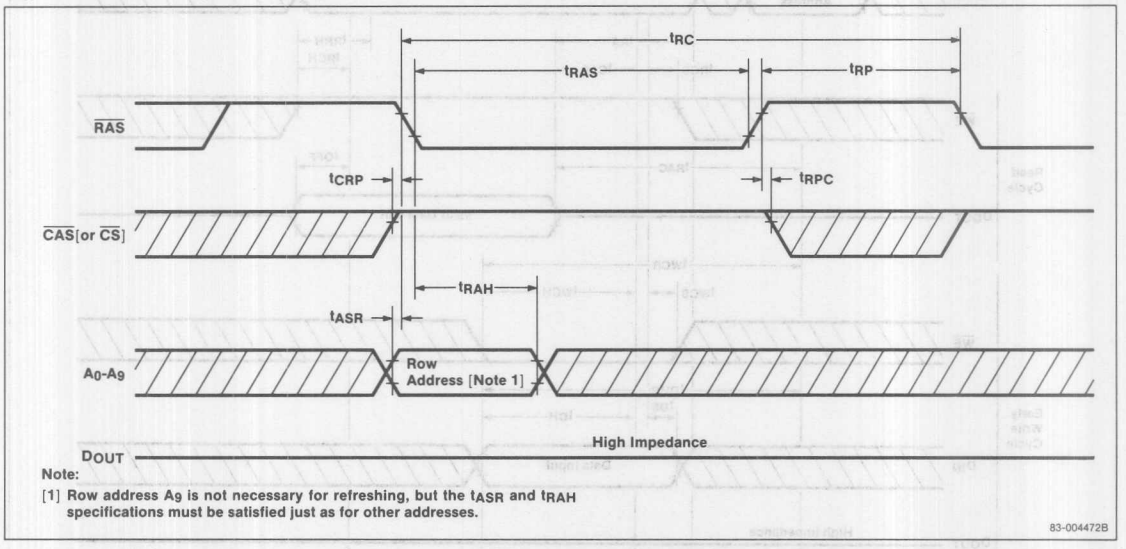


Figure 10. $\overline{CAS}$ (or $\overline{CS}$)-Before-$\overline{RAS}$ Refresh Cycle

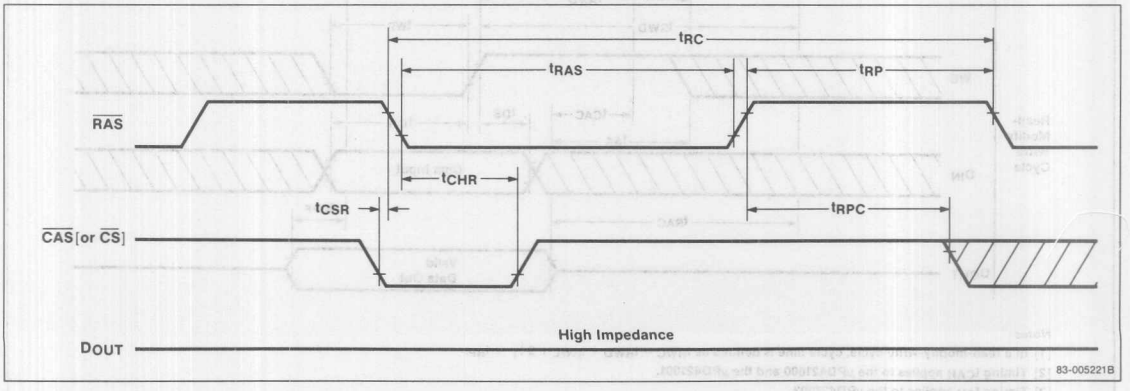


Figure 11. Address Multiplexing

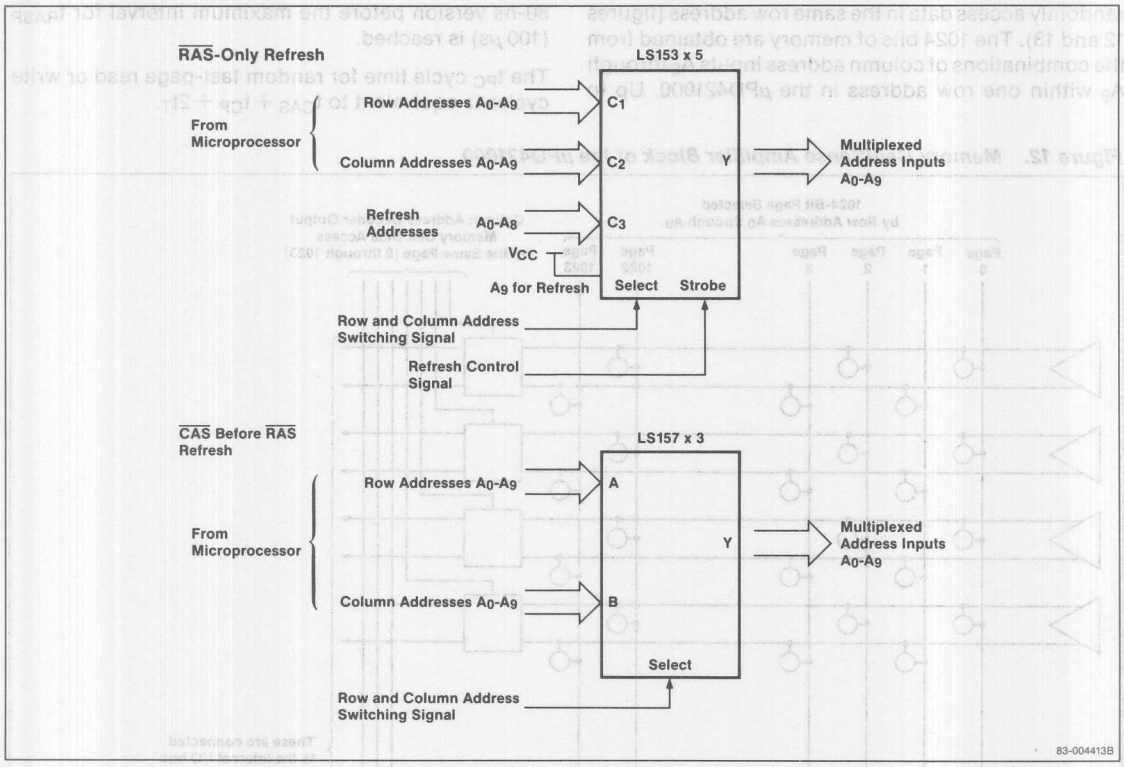


Table 2. Major Characteristics of Fast-Page, Nibble, and Static-Column Modes

Device	Access Time (max)	Cycle Time (min)	Internal Address Usage	High-Speed Access
μPD421000-80	45 ns	50 ns	Row: Page selection Column: Individual cell access on one page	Random access on one page selected by A_0 through A_9
-10	50 ns	60 ns		
-12	60 ns	70 ns		
μPD421001-80	20 ns	40 ns	Row, Column: A_9 inputs set starting location for nibble-mode access	Serial access (4 bits maximum)
-10	25 ns	45 ns		
-12	30 ns	55 ns		
μPD421002-80	45 ns	50 ns	Row: Row selection Column: Individual cell access on one row	Random access on one row selected by A_0 through A_9
-10	50 ns	60 ns		
-12	60 ns	70 ns		

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Fast-Page Mode. Fast-page mode makes it possible to randomly access data in the same row address (figures 12 and 13). The 1024 bits of memory are obtained from the combinations of column address inputs A_0 through A_9 within one row address in the μPD421000. Up to 1998 continuous accesses can be executed on the 80-ns version before the maximum interval for t_{RASP} (100 μs) is reached.

The t_{PC} cycle time for random fast-page read or write cycles is equivalent to $t_{CAS} + t_{CP} + 2t_T$.

Figure 12. Memory Cell/Sense Amplifier Block of the μPD421000

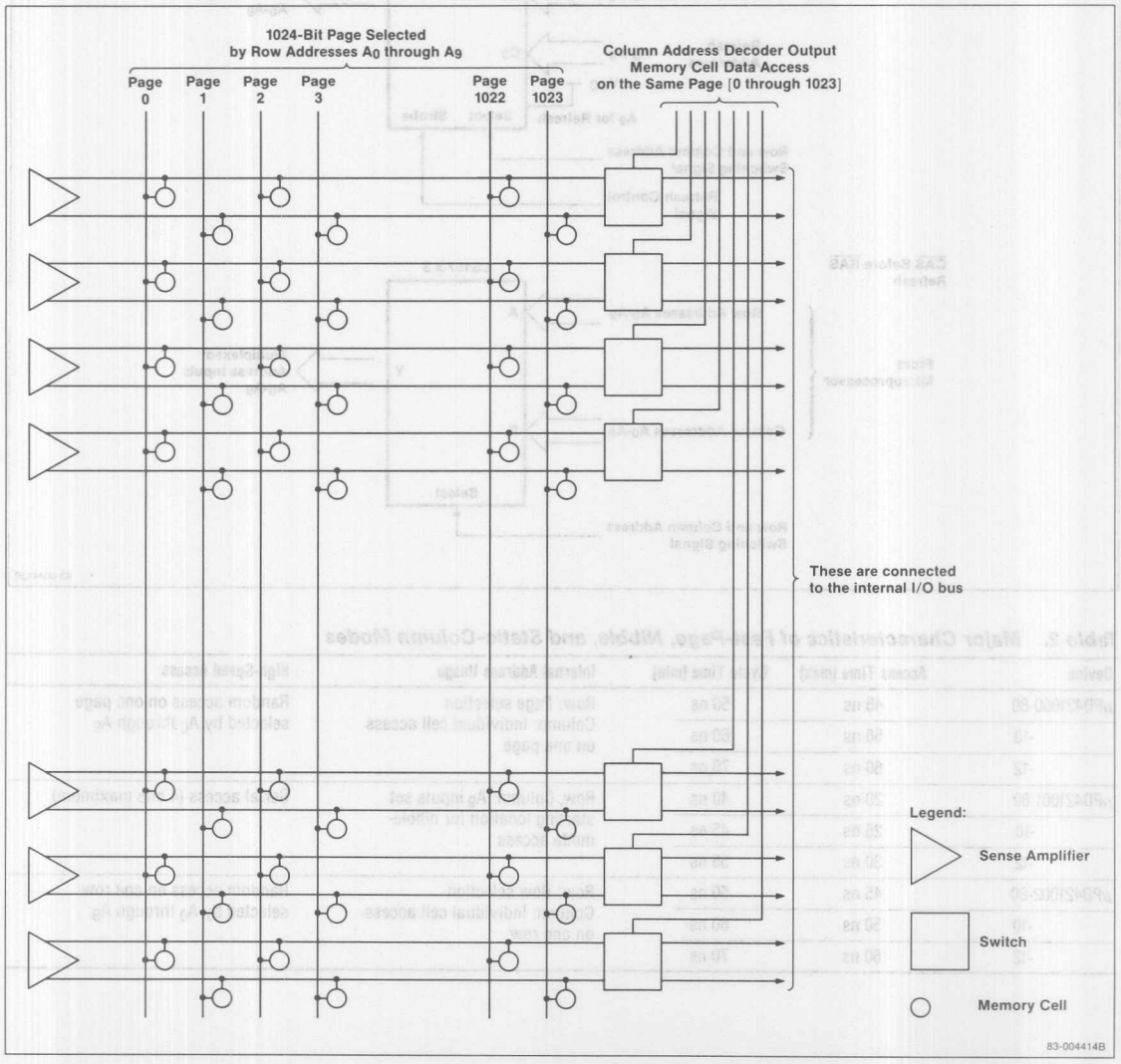
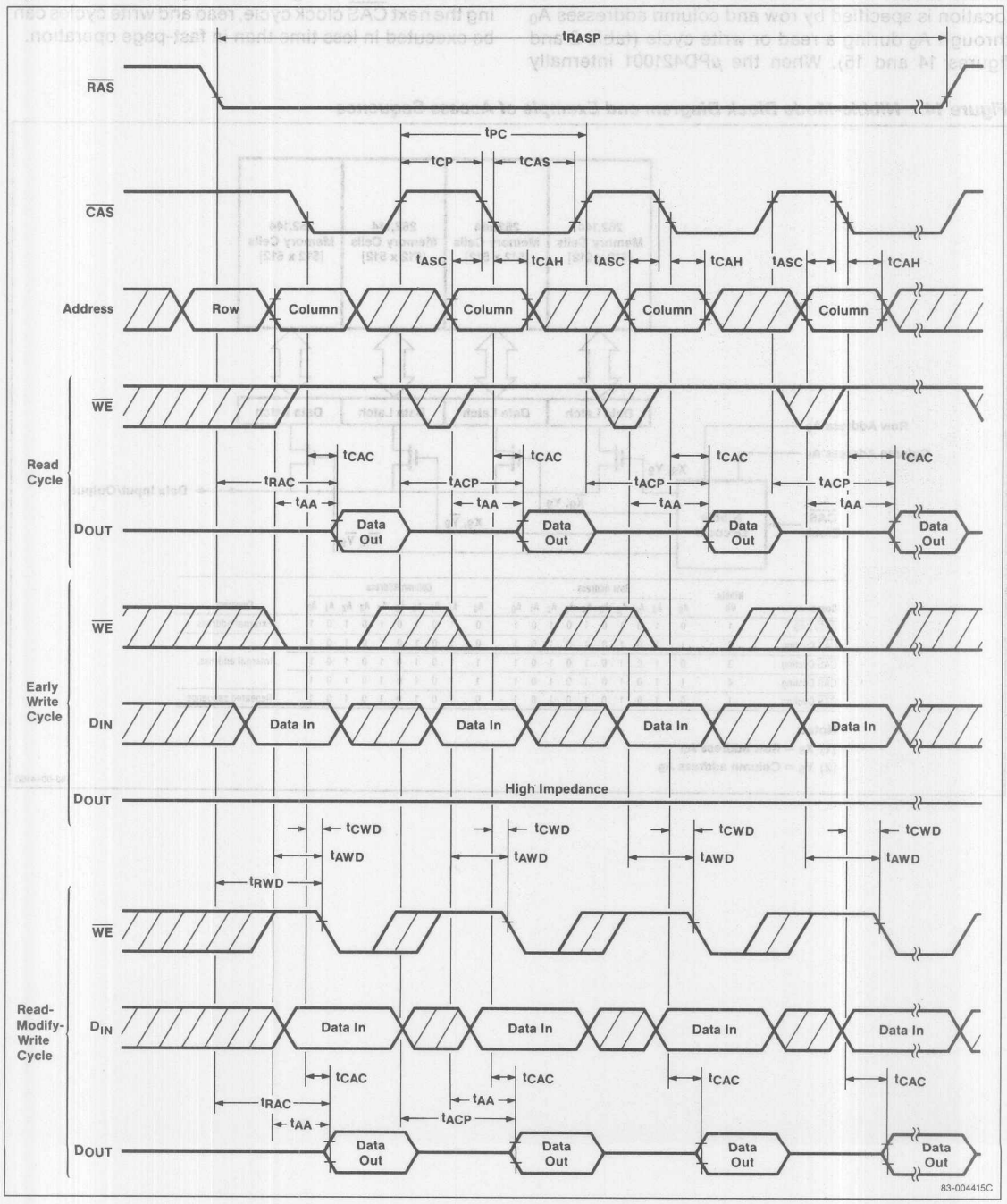
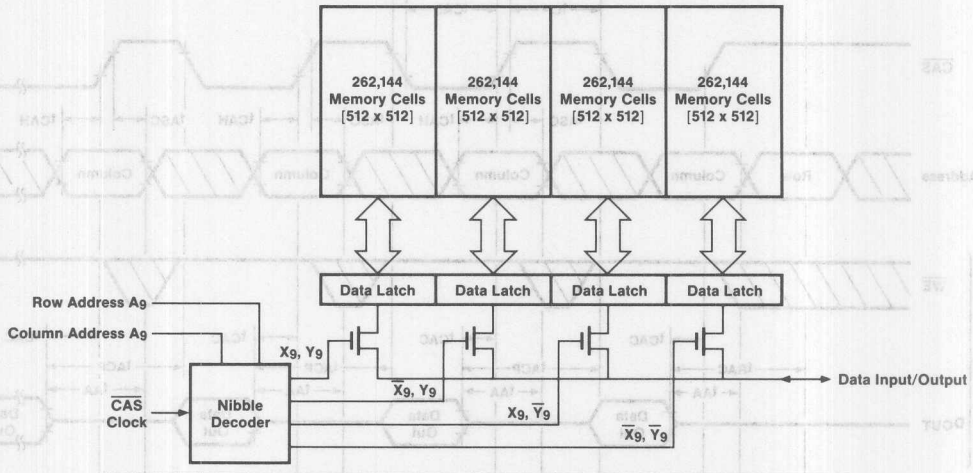


Figure 13. Fast-Page Timing



Nibble Mode. In nibble-mode cycles, the first data location is specified by row and column addresses A_0 through A_9 during a read or write cycle (table 2 and figures 14 and 15). When the μPD421001 internally sequences the two highest-order addresses (A_9) during the next $\overline{CAS}$ clock cycle, read and write cycles can be executed in less time than in fast-page operation.

Figure 14. Nibble-Mode Block Diagram and Example of Access Sequence

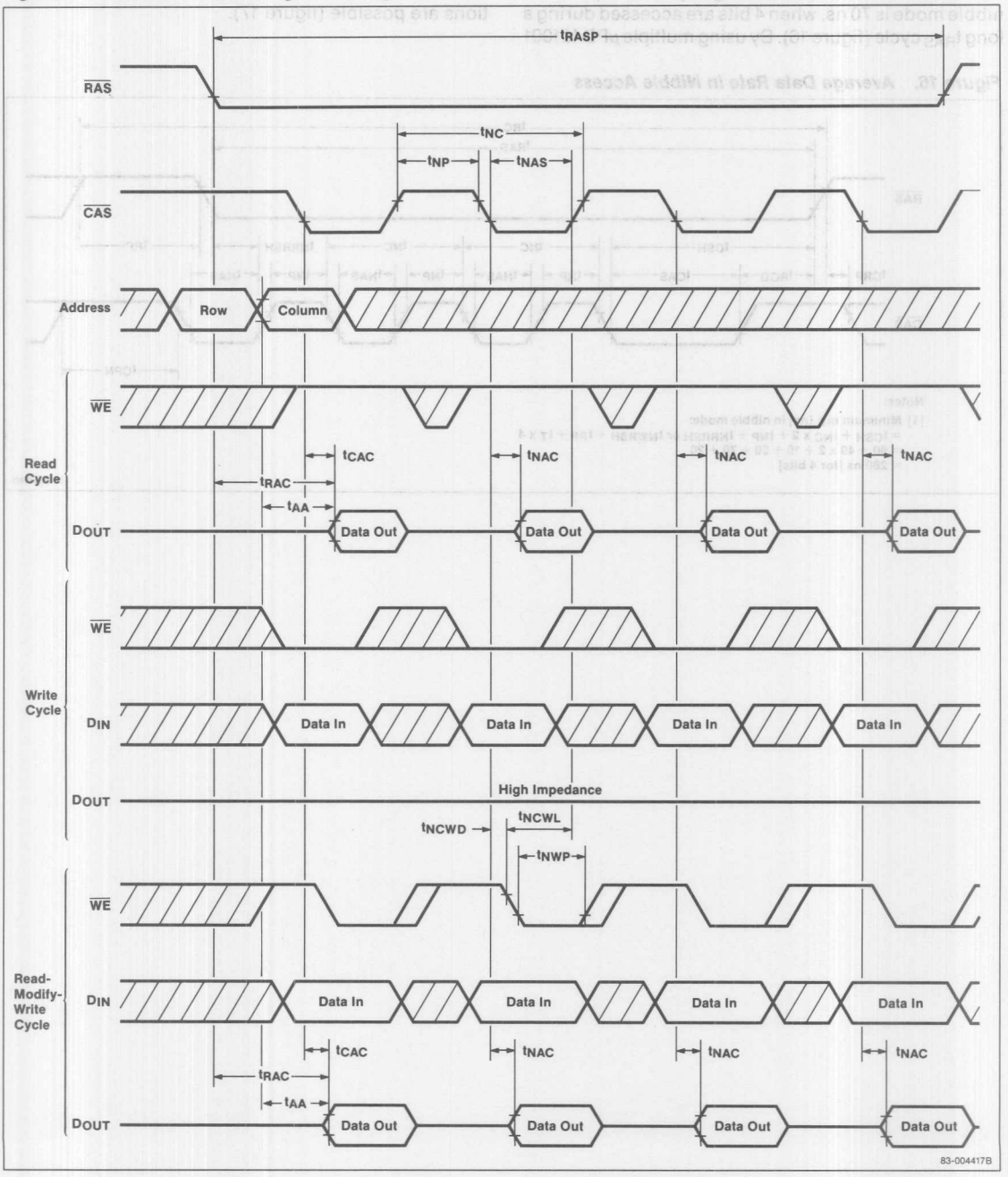


Sequence	Nibble Bit	Row Address A_9	A_8	A_7	A_6	A_5	A_4	A_3	A_2	A_1	A_0	Column Address A_9	A_8	A_7	A_6	A_5	A_4	A_3	A_2	A_1	A_0	Comment
$\overline{RAS}/\overline{CAS}$	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	External address
$\overline{CAS}$ Cycling	2	1	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	
$\overline{CAS}$ Cycling	3	0	1	0	1	0	1	0	1	0	1	1	1	0	1	0	1	0	1	0	1	Internal address
$\overline{CAS}$ Cycling	4	1	1	0	1	0	1	0	1	0	1	1	1	0	1	0	1	0	1	0	1	
$\overline{CAS}$ Cycling	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	Repeated sequence

Notes:
[1] X_9 = Row address A_9
[2] Y_9 = Column address A_9

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Figure 15. Nibble-Mode Timing



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For the 80-ns version, the average cycle time per bit in nibble mode is 70 ns, when 4 bits are accessed during a long t_{RAS} cycle (figure 16). By using multiple μPD421001 devices, high-speed cache and frame buffer applications are possible (figure 17).

Figure 16. Average Data Rate in Nibble Access

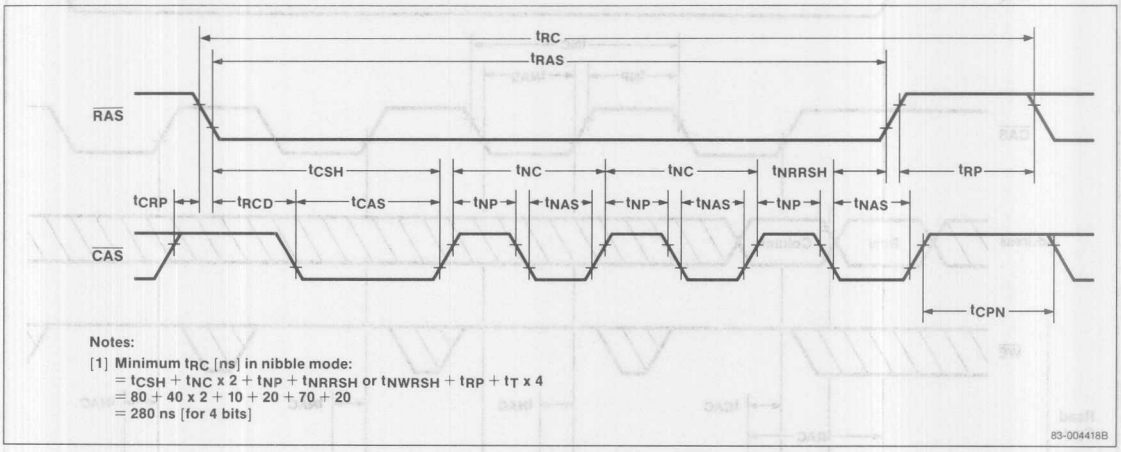
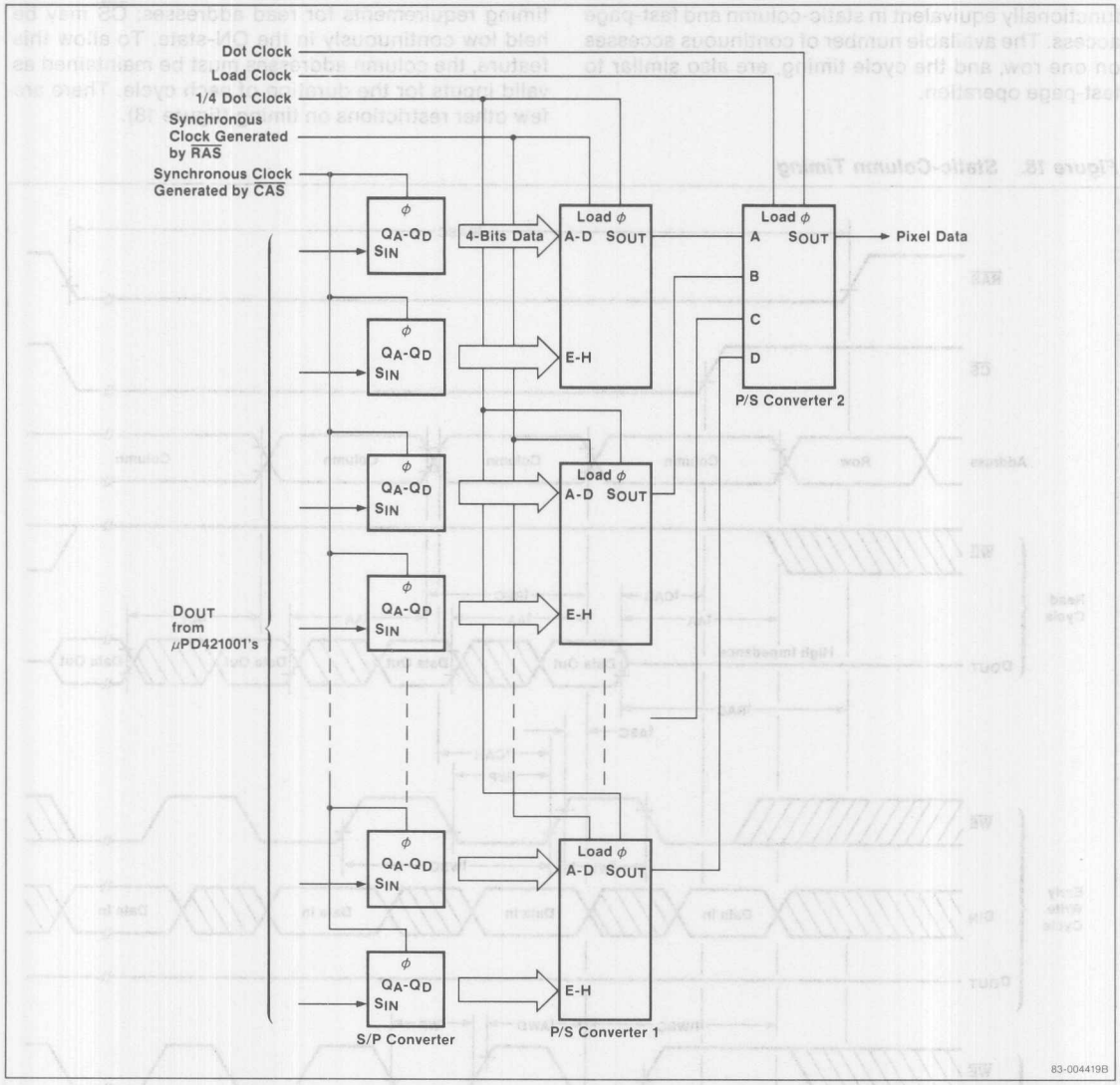


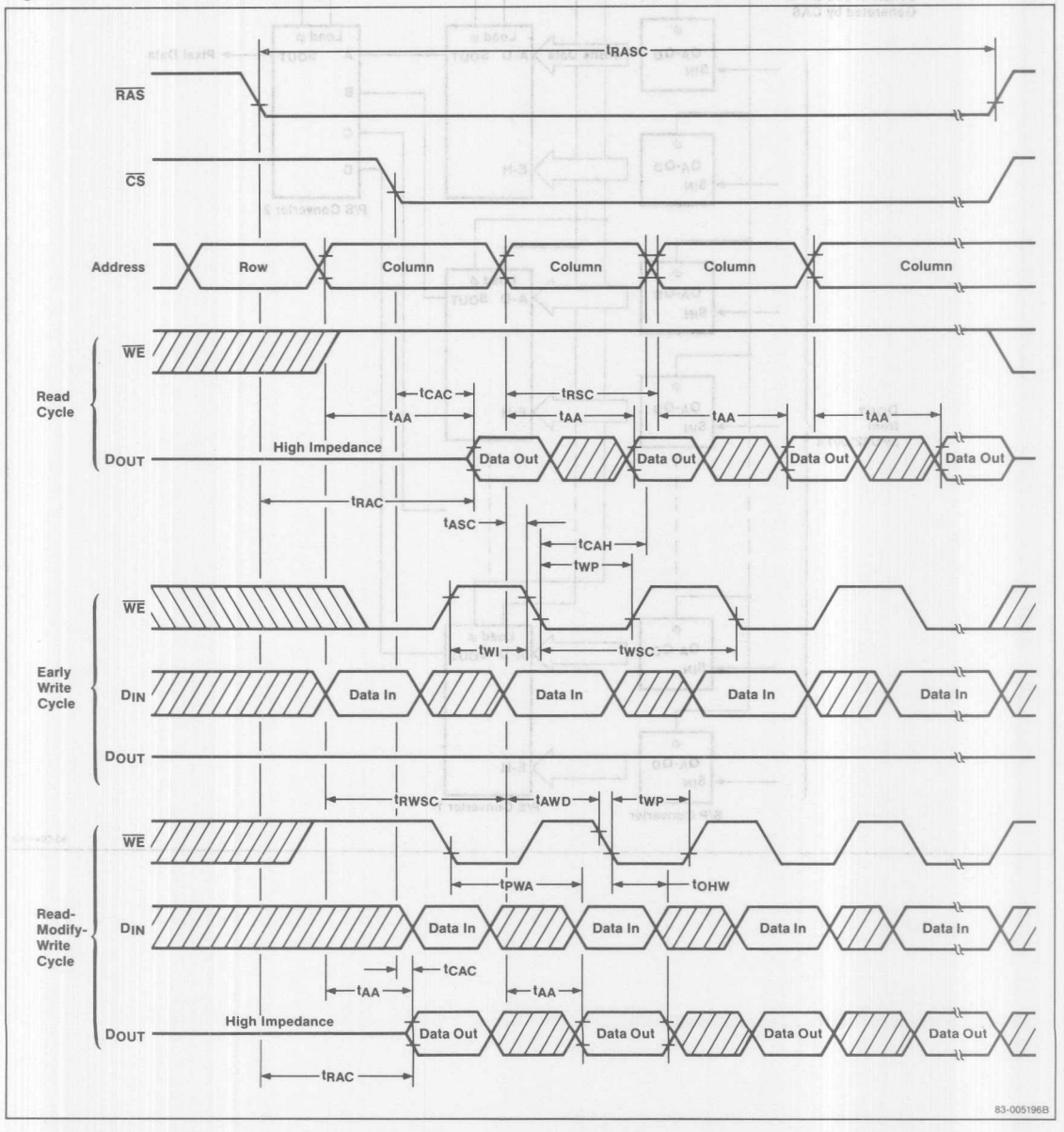
Figure 17. High-Speed Data Access Using Nibble Mode



Static-Column Mode. Row and column addresses are functionally equivalent in static-column and fast-page access. The available number of continuous accesses on one row, and the cycle timing, are also similar to fast-page operation.

In a static-column device, there are no setup or hold timing requirements for read addresses; $\overline{CS}$ may be held low continuously in the ON-state. To allow this feature, the column addresses must be maintained as valid inputs for the duration of each cycle. There are few other restrictions on timing (figure 18).

Figure 18. Static-Column Timing



Precautions

Precautions when using the μPD421000, μPD421001, μPD421002, and other DRAMs should be carefully observed in the areas listed below:

- Power-on and initialization
- Supply voltage fluctuations caused by peak currents
- Relationships between address/data inputs and drivers
- $\overline{RAS}$ and $\overline{CAS}$ (or $\overline{CS}$) generation

Power-On and Initialization. Dynamic RAMs operate by the charging and discharging of gate and internal circuit capacitances. Therefore, dummy $\overline{RAS}$ clock cycles must be executed to charge internal potentials to the prescribed levels when power is applied. Dummy $\overline{RAS}$ cycles are also necessary when there has been no accessing (reading, writing, or refreshing) for periods longer than the refresh interval (figure 19).

To control transistor threshold voltages and decrease internal stray capacitance, DRAMs are usually equipped with a substrate voltage generator circuit to supply the chip's interior with negative voltage. Approximately 100 μs is required to generate an adequate negative voltage level after power is applied and $V_{CC} \geq 4.5$ V.

When the power is switched on, a peak current dependent on the levels of $\overline{RAS}$, $\overline{CAS}$ (or $\overline{CS}$), and $\overline{WE}$ is reached during the rising of V_{CC}. This peak current—maximum when $\overline{RAS}$ and $\overline{CAS}$ (or $\overline{CS}$) are active and $\overline{WE}$ is inactive—can be minimized by using clock input pullups on $\overline{RAS}$ and $\overline{CAS}$ (or $\overline{CS}$) so that their rise times correspond to the rise time of the power supply.

Supply Voltage Fluctuations. Since 1 and 0 logic (storage) operations are executed by the charging and discharging of capacitances, including the memory cells, the peak current generated is dependent on charge and discharge timing.

This peak current is concentrated just after $\overline{RAS}$ and $\overline{CAS}$ (or $\overline{CS}$) transition intervals (figure 20) with a peak value of about 120 mA. Since this current is a source of noise (voltage drop) in the memory system supply voltage, decoupling by multilayer ceramic capacitors with excellent frequency response is necessary. If the average of the 120-mA peak current pulse lasts about 100 ns, the capacitance required to keep the drop in the supply voltage line at about 0.1 V will be calculated as follows:

$$C = \frac{120\ (\text{mA}) \times 100\ (\text{ns})}{0.1\ (\text{V})}$$

$$= 120 \times 10^3\ \text{pF}$$

$$= 0.12\ \mu\text{F}$$

Therefore, when designing the memory board, keep the power and ground leads as short as possible for low inductance. Decoupling capacitors of about 0.2 μF must be inserted between the power supply lines for each memory device. With careful board layout, the use of fewer but larger capacitors is possible. Capacitors used in one of every two memory device locations, with a value of perhaps 0.33 μF, can provide satisfactory decoupling in many cases.

Figure 19. Dummy Cycles after Power is Applied

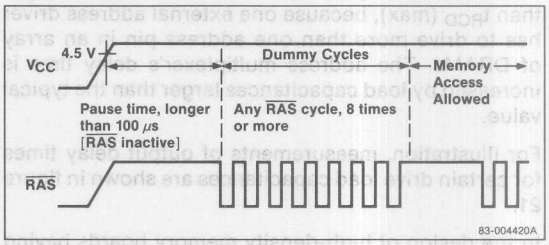
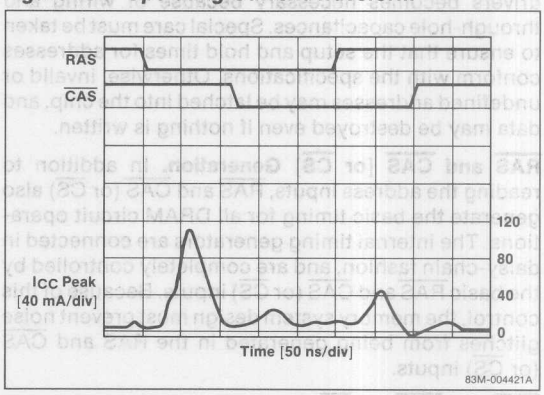


Figure 20. Operating Current Waveform



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Address/Data Inputs and Drivers. Probably the most important consideration in DRAM timing is the relationship between address/data inputs and the external drivers. In address-multiplexed DRAMs such as the μPD421000, μPD421001, and μPD421002 (where row and column addresses are supplied as two sets of inputs), addresses supplied externally have to be switched by a multiplexer.

The sequence of this timing must be designed very carefully. A timing sequence starts with the setting of row addresses. Next, $\overline{RAS}$ falls. After the specified hold time for row addresses is met, the addresses are switched to set up column address input. Once $\overline{CAS}$ (or $\overline{CS}$) falls, the specified hold time for column addresses must be satisfied.

When $\overline{CAS}$ (or $\overline{CS}$) is activated within the time specified for t_{RCD} (max), the setup time for column addresses is more difficult to guarantee than when t_{RCD} is longer than t_{RCD} (max), because one external address driver has to drive more than one address pin in an array of DRAMs. The address multiplexer's delay time is increased by load capacitances larger than the typical value.

For illustration, measurements of output delay times for certain drive load capacitances are shown in figure 21.

In the design of high-density memory boards having a large number of memory devices, partitioning of drivers becomes necessary because of wiring and through-hole capacitances. Special care must be taken to ensure that the setup and hold times for addresses conform with the specifications. Otherwise, invalid or undefined addresses may be latched into the chip, and data may be destroyed even if nothing is written.

$\overline{RAS}$ and $\overline{CAS}$ [or $\overline{CS}$] Generation. In addition to reading the address inputs, $\overline{RAS}$ and $\overline{CAS}$ (or $\overline{CS}$) also generate the basic timing for all DRAM circuit operations. The internal timing generators are connected in daisy-chain fashion, and are completely controlled by the basic $\overline{RAS}$ and $\overline{CAS}$ (or $\overline{CS}$) inputs. Because of this control, the memory system design must prevent noise glitches from being generated in the $\overline{RAS}$ and $\overline{CAS}$ (or $\overline{CS}$) inputs.

$\overline{RAS}$ and $\overline{CAS}$ (or $\overline{CS}$) timing is specified in terms of minimum values. High- or low-level pulses that do not satisfy these minimum values can result in incorrect output data (because there is insufficient time for sense amplifier operation), and can also lead to destruction of write data. Therefore, the prevention of noise glitches must be carefully considered in logic and circuit design.

Figure 21. Effect of Load Capacitance on TTL (7404) Output

Delay and Transition Times

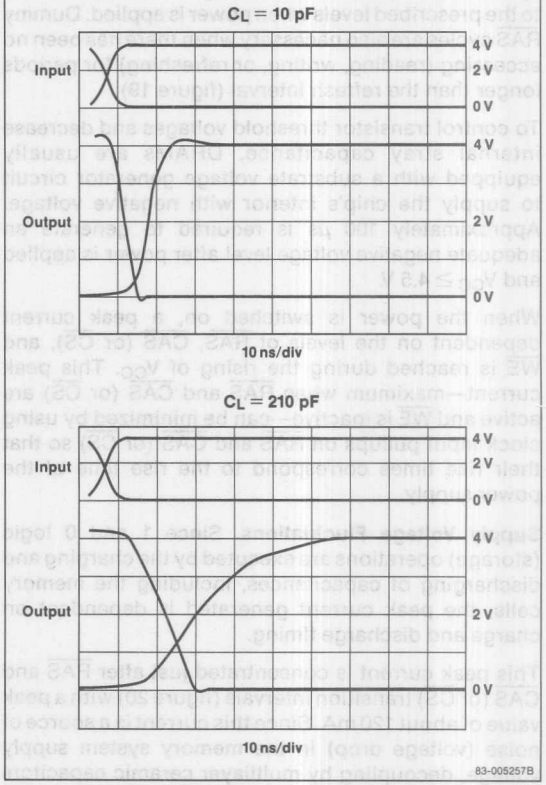
Parameter	Time [ns] C_L = 10 pF	C_L = 110 pF	C_L = 210 pF
t_{PLH}	9	16.5	26
t_{PHL}	5.5	12.5	17
t_R	3.2	7.8	15
t_F	1.5	3.8	5.5

Notes:

[1] t_{PLH}, t_{PHL} are defined as the delay time from V_{IN} = 1.5 V to V_{OUT} = 2.4 V or 0.8 V.

[2] t_R and t_F are defined as the transition time between V_{OH} [min] and V_{OL} [max].

[3] Load capacitance C_L includes the oscilloscope input capacitance.



V40™ MICROPROCESSOR APPLICATION

Features

The μPD70208 (also known as V40) is a high-performance 8-bit CMOS microprocessor featuring 16-bit architecture in the CPU, and including a number of other peripheral devices within the same chip. The CPU is equipped with a powerful set of instructions that cover bit processing and multiple-length, packed-BCD operations, high-speed multiplications and divisions, and variable-length bit and field manipulations.

This device combines high-speed processing with flexibility in a variety of applications. The on-chip peripherals include a clock generator with a timer/counter and programmable wait control, refresh control, serial control, interrupt control, and DMA control units. In addition to allowing more compact microcomputer systems, the V40 has a simplified system design.

When connected to the μPD421000-series DRAMs, the V40 does not require an external refresh timer or other peripherals, which means a big reduction in the number of external devices required.

Memory Mapping

In the V40, memories of up to 1 megaword can be accessed using address information (A_{19} through A_0) output from the 20-bit address bus (figure 22).

The first 1024 bytes, 0 through 3FFH, are allocated to interrupt vectors (although areas that cannot be used by the system can be used elsewhere). Addresses FFFF0H through FFFFBH are used for starting and resetting purposes; FFFFCH through FFFFFH are reserved for future use and cannot be used here. The remaining address space, 400H through FFFEFH, is not allocated and may be used as desired.

As shown in figure 23, with a data bus width of 8 bits in the V40, CPU connections to the memory require only that the 20-bit address output from the CPU be accepted in the 1-megabyte address space. Byte data is accessed in one bus cycle, and word data is accessed in two bus cycles.

V40 is a trademark of NEC Corporation.

Because of this simple connection requirement, it is only necessary to allocate the system control ROM to addresses of at least FFFF0H and disable the ROM-area RAM (since 1 megabyte is already taken up by eight 1-megabit DRAMs). The method used may involve either deselecting the ROM-area RAM by a decoder, or executing bank switching to use the entire area as RAM area. The example included for this application shows the former method because it is simpler.

Figure 22. V40 Memory Mapping

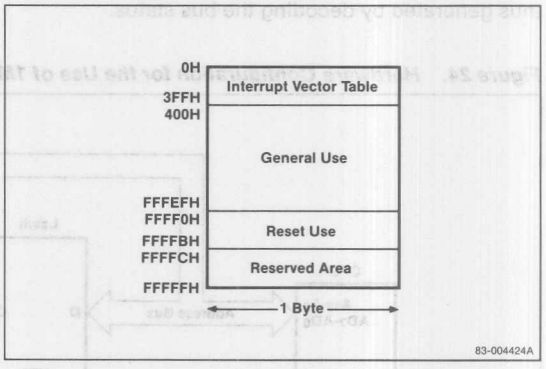
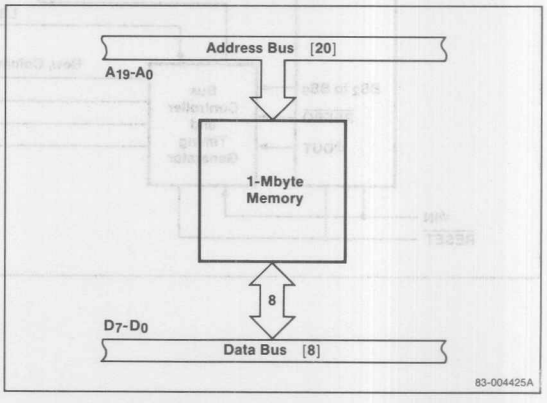


Figure 23. V40 Memory Interface



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Hardware Configuration

Since refresh addresses and the timing control outputs can be supported by programming on-chip circuits, the generation of $\overline{RAS}$ and $\overline{CAS}$ (or $\overline{CS}$) timing is the only major DRAM support not provided directly by the V40 (figure 24).

Memory Access Timing Generation

Although V40 memory access timing can be generated from either the bus status or MWR/$\overline{MRD}$, the μPD71088 system bus controller is used in this application example to enable connections to slightly slower-speed memories. The $\overline{RAS}$ and $\overline{CAS}$ (or $\overline{CS}$) signals are thus generated by decoding the bus status.

The $\overline{RAS}$ and $\overline{CAS}$ (or $\overline{CS}$) generator is shown in figure 25, and the operation timing in figure 26. To generate the control timing with this system controller, bus status signal BS_2 is sampled by the CPU clock output (ϕ_{OUT}) at the rising edge of the T_1 cycle, and $\overline{RAS}$ is generated from FF2 at the falling edge of ϕ_{OUT} at the end of T1. The multiplex control signal (MPX) used in address switching during memory cycles is generated by $\overline{RAS}$. After $\overline{RAS}$ is generated, it is delayed by the rising edge of the external 16-MHz clock to create MPX, which is then passed to the data selector input.

As can be seen from figure 26, memory access time is equal to $2/f(\phi_{OUT}) - (t_{SDK} + \text{TTL delay time})$. Even if an external clock of 16 MHz is used, a -12 device is sufficient ($\overline{RAS}$ access time in the -12 device is 120 ns).

Figure 24. Hardware Configuration for the Use of 1M DRAMs

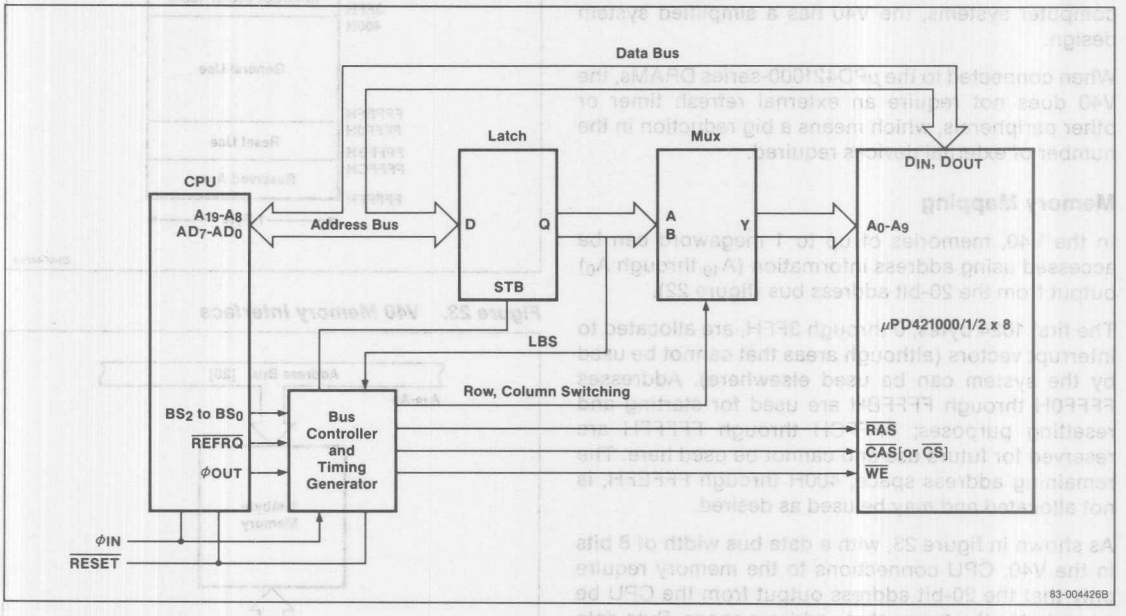
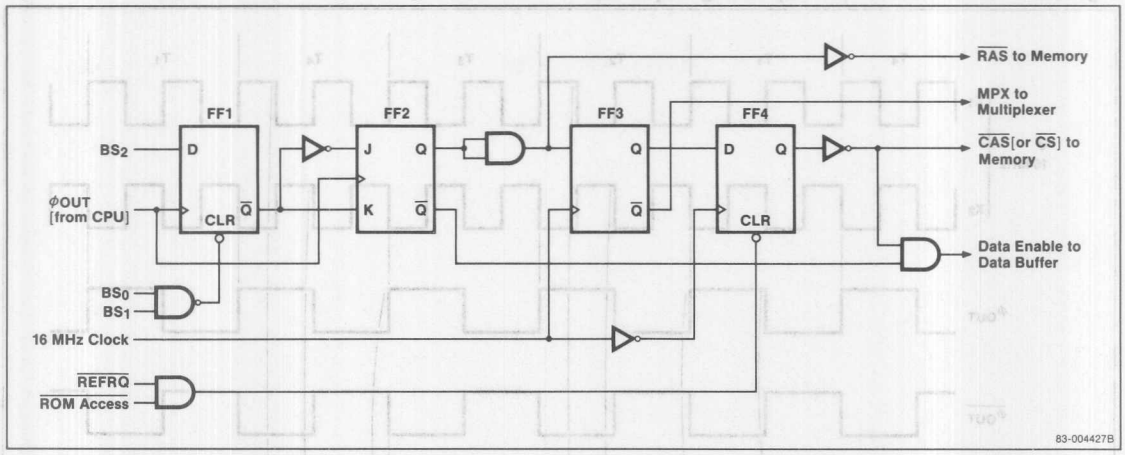
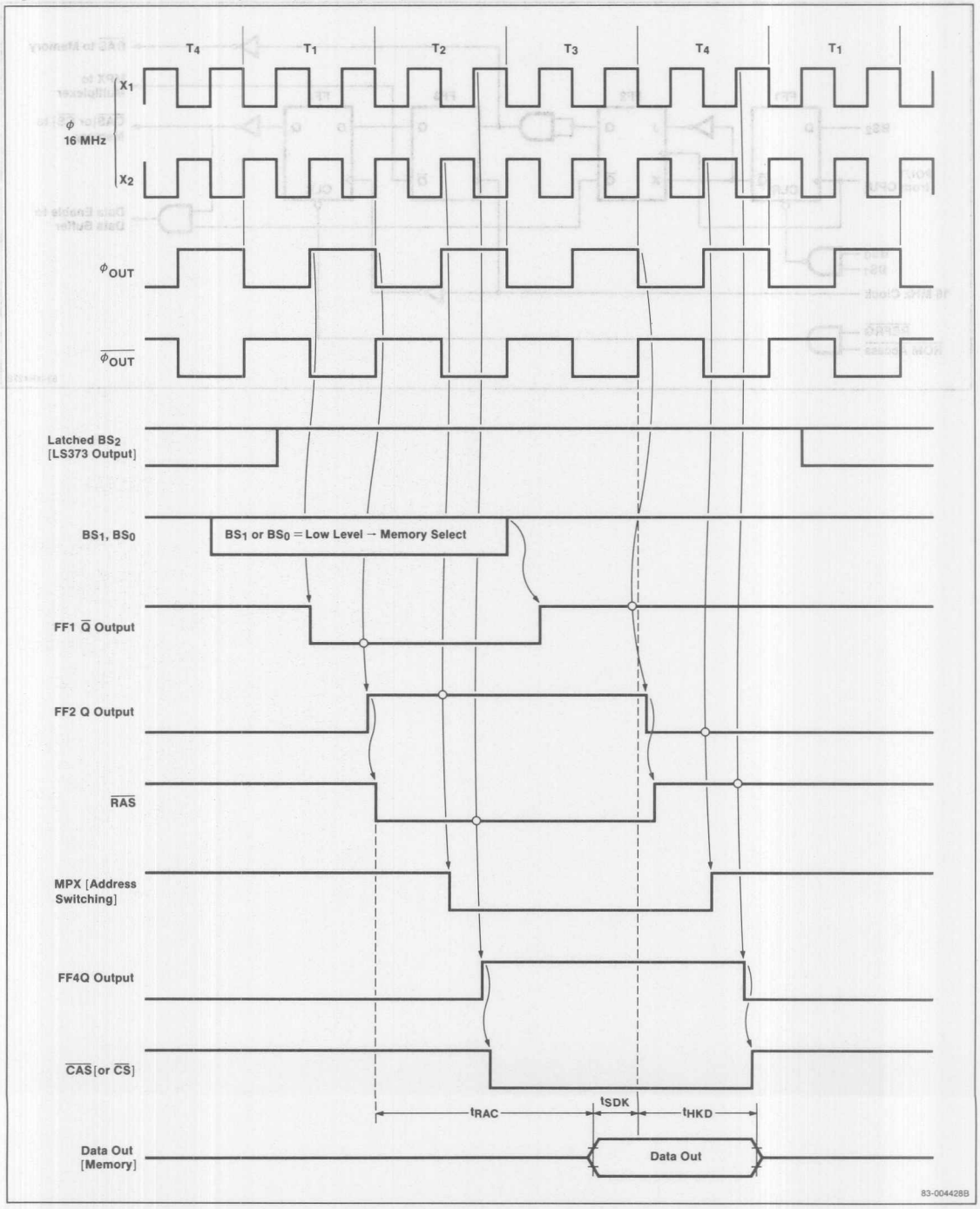


Figure 25. $\overline{RAS}$ and $\overline{CAS}$ (or $\overline{CS}$) Timing Generator



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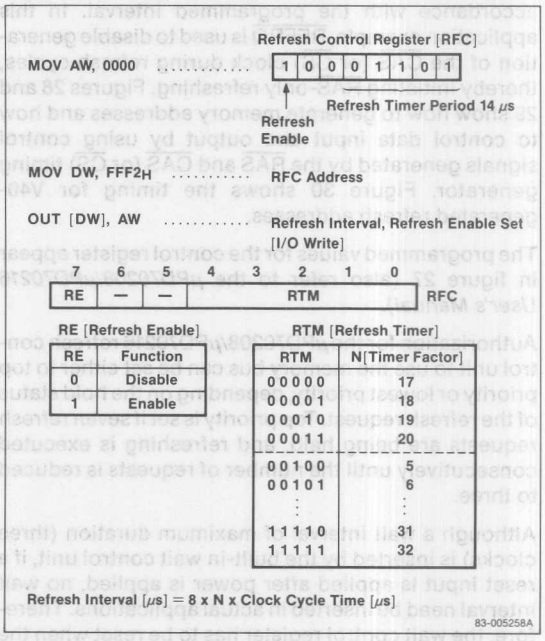
Figure 26. $\overline{RAS}$ and $\overline{CAS}$ (or $\overline{CS}$) Timing Sequence



Refresh Timing Generation

Refreshing for the μPD421000, μPD421001, and μPD421002 is executed by selecting 512 lines in 8 ms. In the V40, memory refreshing can be handled easily by outputting the $\overline{\text{REFRQ}}$ control signal and the A_0 through A_8 refresh addresses. These signals are controlled by programming the refresh control register (RFC), allocated to I/O address FFF2H (figure 27).

Figure 27. Programming of Refresh Control Register



This function generates the $\overline{\text{REFRQ}}$ control signal in accordance with the programmed interval. In this application example, $\overline{\text{REFRQ}}$ is used to disable generation of the $\overline{\text{CAS}}$ (or $\overline{\text{CS}}$) clock during refresh cycles, thereby initiating $\overline{\text{RAS}}$-only refreshing. Figures 28 and 29 show how to generate memory addresses and how to control data input and output by using control signals generated by the $\overline{\text{RAS}}$ and $\overline{\text{CAS}}$ (or $\overline{\text{CS}}$) timing generator. Figure 30 shows the timing for V40-generated refresh addresses.

The programmed values for the control register appear in figure 27 (also refer to the *μPD70208/μPD70216 User's Manual).*

Authorization for the μPD70208/μPD70216 refresh control unit to use the memory bus can be set either to top priority or lowest priority, depending on the hold status of the refresh request. Top priority is set if seven refresh requests are being held, and refreshing is executed consecutively until the number of requests is reduced to three.

Although a wait interval of maximum duration (three clocks) is inserted by the built-in wait control unit, if a reset input is applied after power is applied, no wait interval need be inserted in actual applications. Therefore, the wait control register has to be reset when the V40 is used at 8 MHz.

Wait control registers WCY2 (FFF6H), WCY1 (FFF5H), and WMB (FFF4H) write program data at these I/O addresses using an I/O write instruction (figure 31).

Figure 28. Memory Access Generation

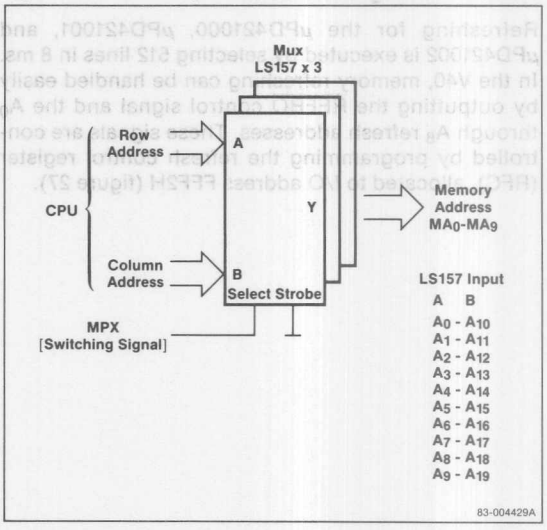


Figure 29. Data Input and Output Control

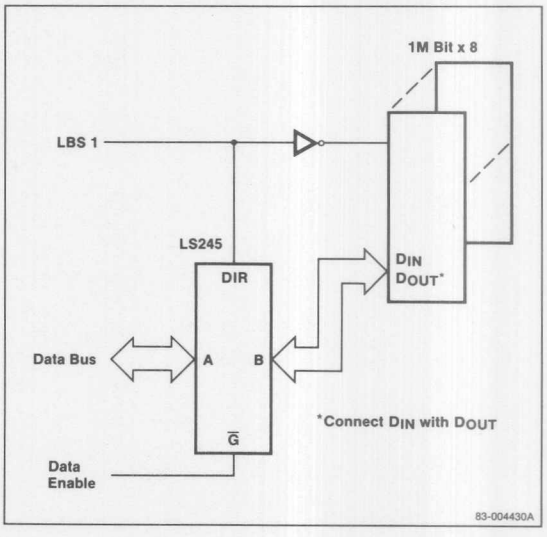
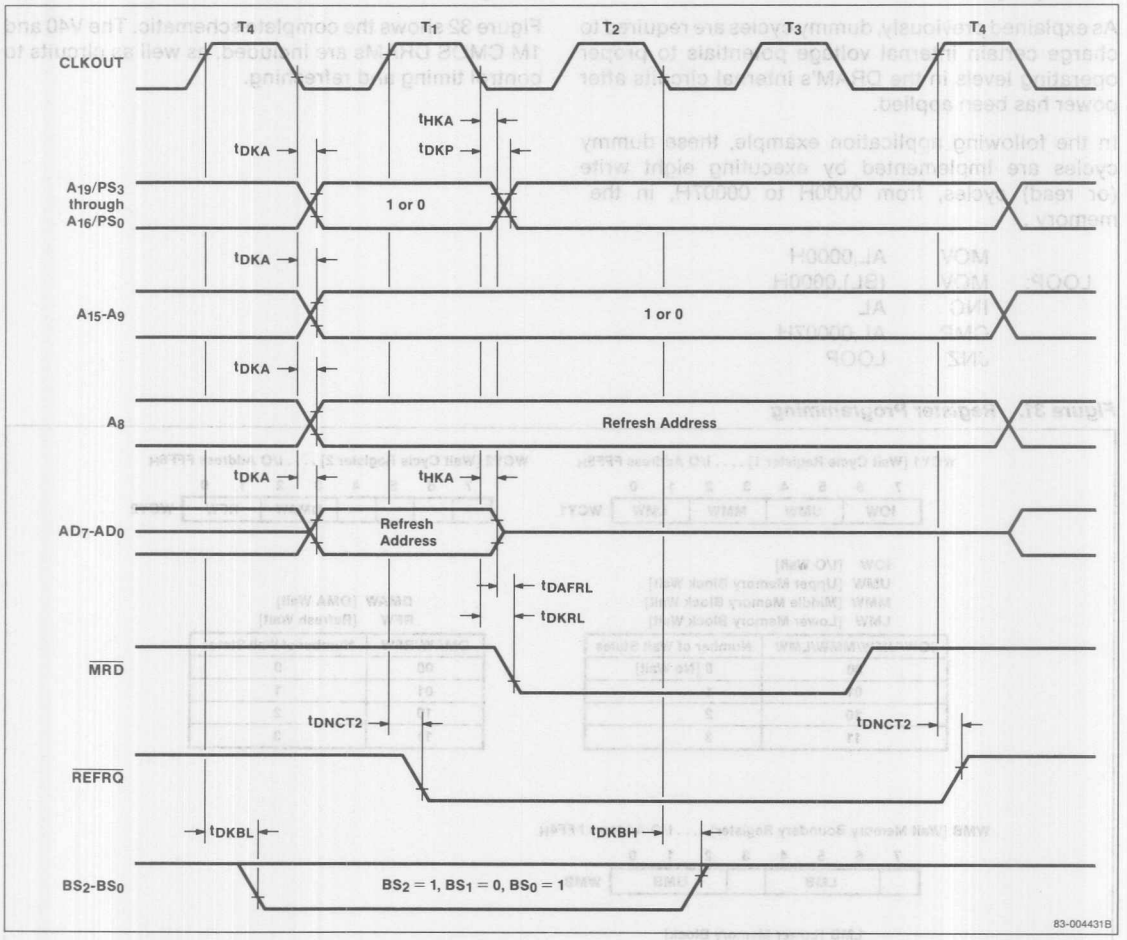


Figure 30. Refresh Timing Cycle



Dummy Cycles

As explained previously, dummy cycles are required to charge certain internal voltage potentials to proper operating levels in the DRAM's internal circuits after power has been applied.

In the following application example, these dummy cycles are implemented by executing eight write (or read) cycles, from 0000H to 00007H, in the memory .

```
        MOV     AL,0000H
LOOP:   MOV     (BL),0000H
        INC     AL
        CMP     AL,00007H
        JNZ     LOOP
```

Composite Schematic

Figure 32 shows the complete schematic. The V40 and 1M CMOS DRAMs are included, as well as circuits to control timing and refreshing.

Figure 31. Register Programming

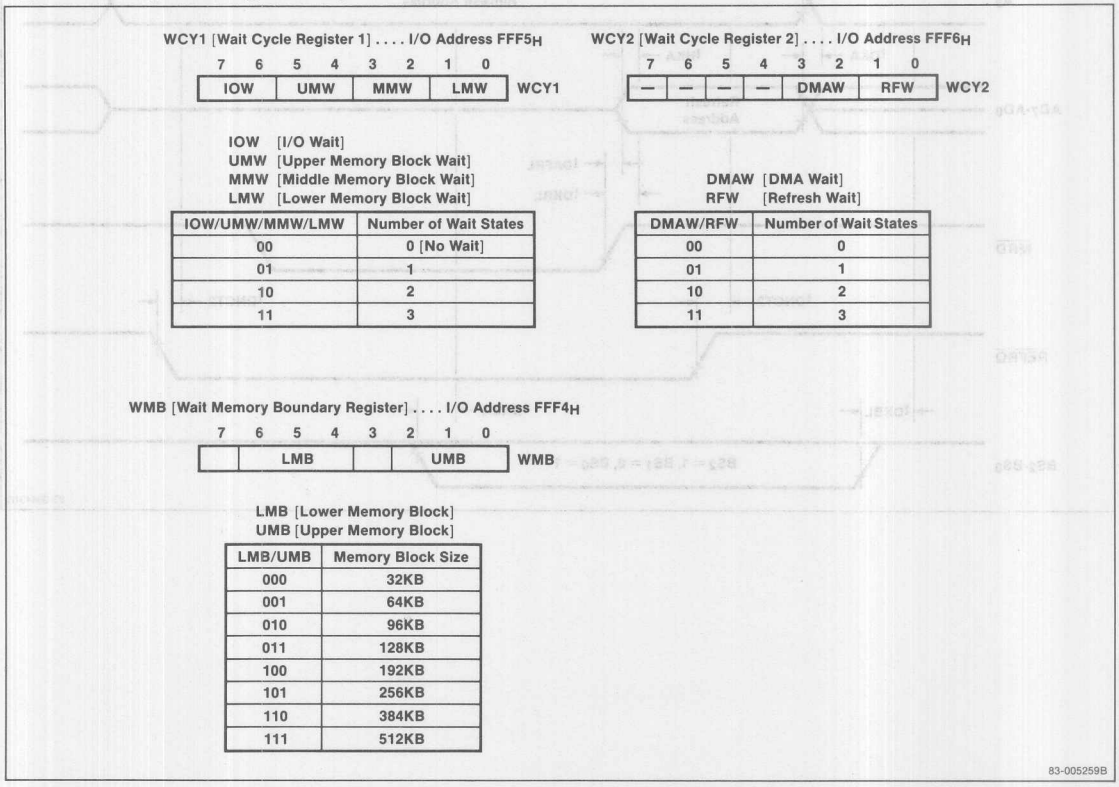
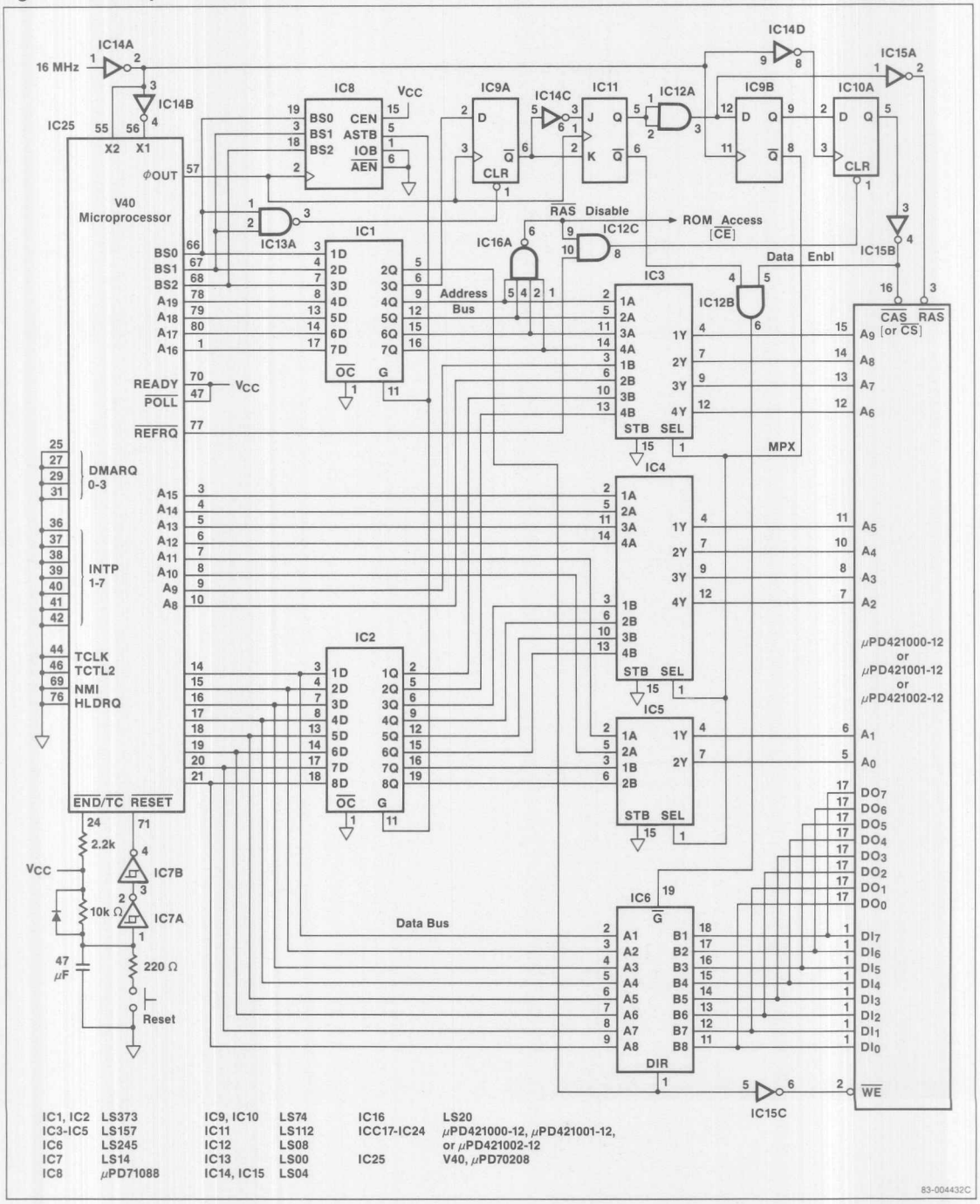
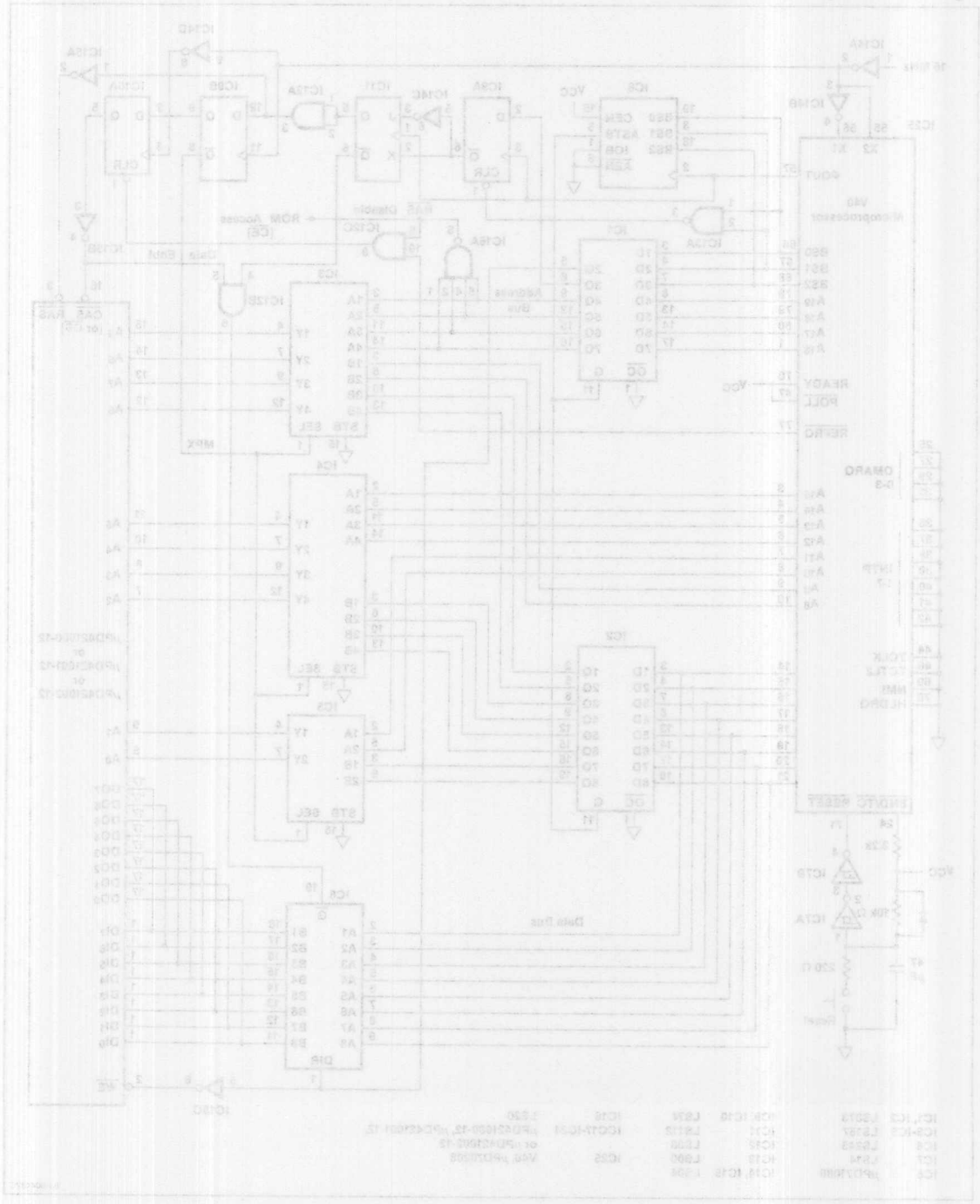


Figure 32. Composite Schematic





Section 7
Static RAMs

μPD46710 7-1
16,384 x 10-Bit x 2 Static BiCMOS RAM

μPD46741 7-3
8,192 x 20-Bit x 2 Static BiCMOS RAM

μPD4361 7-5
65,536 x 1-Bit Static CMOS RAM

μPD4362 7-13
16,384 x 4-Bit Static CMOS RAM

μPD4363 7-21
16,384 x 4-Bit Static CMOS RAM

μPD43251 7-29
262,144 x 1-Bit Static CMOS RAM

μPD46251 7-37
262,144 x 1-Bit Static BiCMOS RAM

μPD43254 7-45
65,536 x 4-Bit Static CMOS RAM

μPD43256A 7-53
32,768 x 8-Bit Static CMOS RAM

μPD43256B 7-65
32,768 x 8-Bit Static CMOS RAM

μPD43258 7-75
32,768 x 8-Bit Static CMOS RAM

μPD431000 7-83
131,072 x 8-Bit Static CMOS RAM

μPD431000A 7-93
131,072 x 8-Bit Static CMOS RAM

μPD431001 7-105
1,048,576 x 1-Bit Static CMOS RAM

μPD431004 7-113
262,144 x 4-Bit Static CMOS RAM

Application Note 50 7-121
Battery Backup Circuits for SRAMs

Application Note 90-04 7-133
Battery Backup Using NEC's Supercaps

Additional New Product Information

Device Number	Description	Comments
Static RAMs		
μPD4361	64K x 1-bit	New speeds to 12 ns
μPD4362	16K x 4 bits	New speeds to 12 ns
μPD4363	16K x 4 bits, with $\overline{OE}$	New speeds to 12 ns
μPD4368	8K x 8 bits	New device, with speeds to 15 ns
μPD4369	8K x 9 bits	New device, with speeds to 15 ns
μPD43251	256K x 1 bit	New speeds to 15 ns
μPD43253	64K x 4 bits, with $\overline{OE}$	New device, with speeds to 15 ns
μPD43254	64K x 4 bits	New speeds to 15 ns
μPD43258	32K x 8 bits	New speeds to 20 ns
μPD43259	32K x 9 bits	New device

NEC Electronics Inc.

μPD46710
16,384 x 10-Bit x 2
Static BiCMOS RAM

PRELIMINARY INFORMATION

Description

The μPD46710 is a high performance static BiCMOS RAM organized as 16,384 x 10 bits x 2 instructions and designed for use as a high-speed cache memory. The μPD46710 integrates two 16,384 x 10-bit SRAM cores with associated address latches and control signals that can be used to implement an instruction/data cache for a MIPS R3000 RISC system.

Features

- Fast access times of 15 ns and 20 ns
- 16,384 x 10-bit x 2 organization
- On-chip address latches
- On-chip instruction/data caches
- Fully static read/write operation
- 52-pin PLCC packaging

Ordering Information

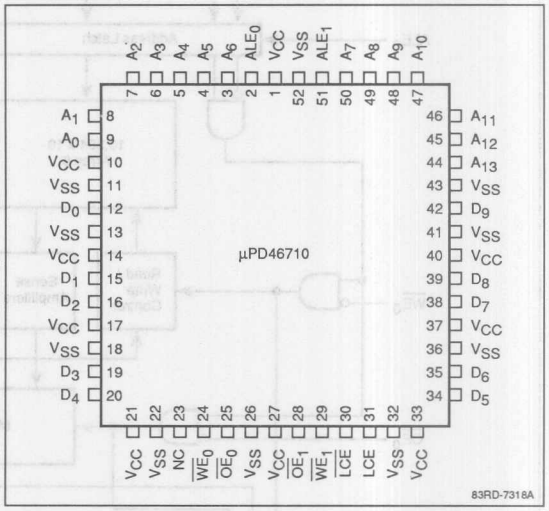
Part Number	Access Time	Package
μPD46710LN-15	15 ns	52-pin PLCC
LN-20	20 ns	

Pin Identification

Symbol	Function
A_0 - A_{13}	Addresses
ALE_0 - ALE_1	Address latch enable
D_0 - D_9	Data inputs/outputs
$\overline{LCE}$, LCE	Latch chip enable
$\overline{OE}_0$ - $\overline{OE}_1$	Output enable
$\overline{WE}_0$ - $\overline{WE}_1$	Write enable
V_{CC}	5-volt power supply
V_{SS}	Ground
NC	No connection

Pin Configuration

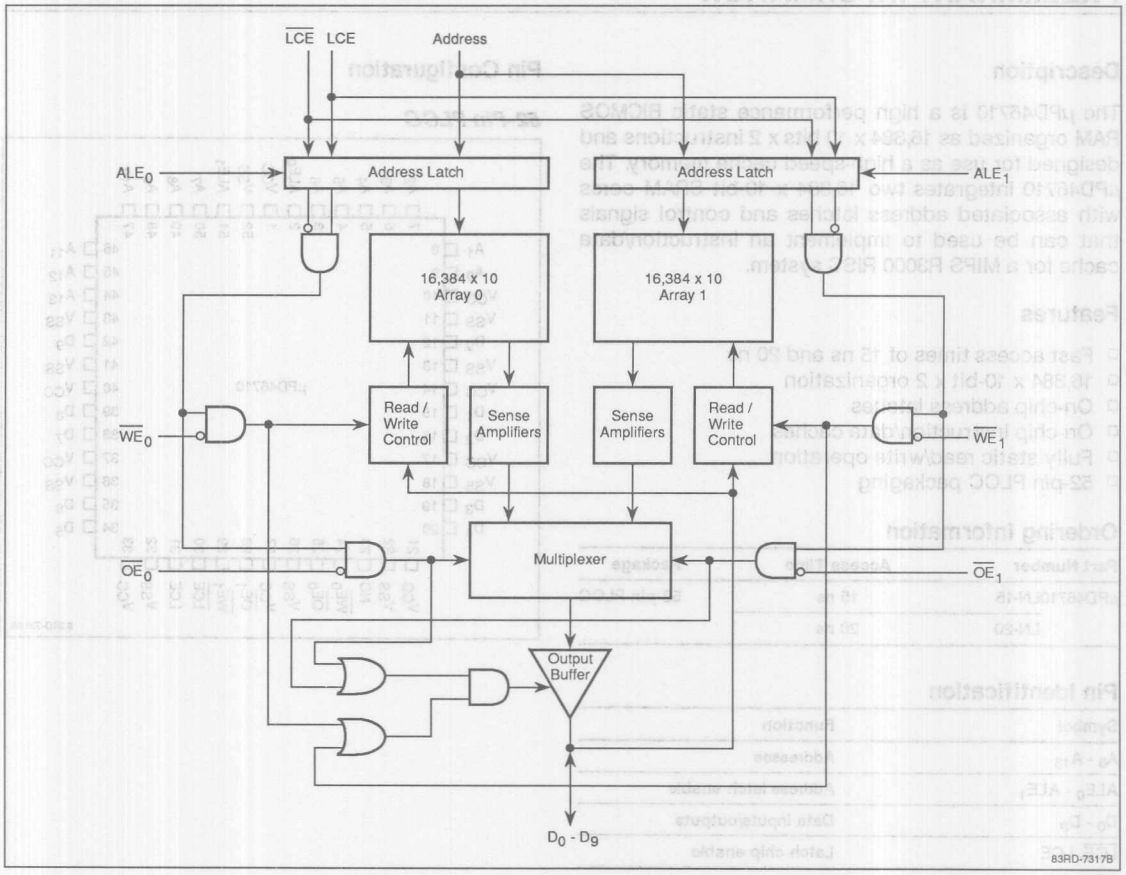
52-Pin PLCC



7

Please contact your NECEL representative for a copy of the complete data sheet.

Block Diagram



NEC Electronics Inc.

μPD46741
8,192 x 20-Bit x 2 Static BiCMOS RAM

PRELIMINARY INFORMATION

Description

The μPD46741 is a high performance BiCMOS static RAM organized as 8,192 x 20 bits x 2 instructions and designed to be used as a high-speed cache memory. The μPD46741 integrates two 8,192 x 20-bit SRAM cores with associated address latches and control signals that can be used to implement an instruction/data cache for a MIPS R3000 RISC system.

Features

- Fast access times of 15 ns and 20 ns
- 8,192 x 20-bit x 2 organization
- On-chip address latches
- On-chip instruction/data caches
- Fully static read/write operation
- 68-pin PLCC packaging

Ordering Information

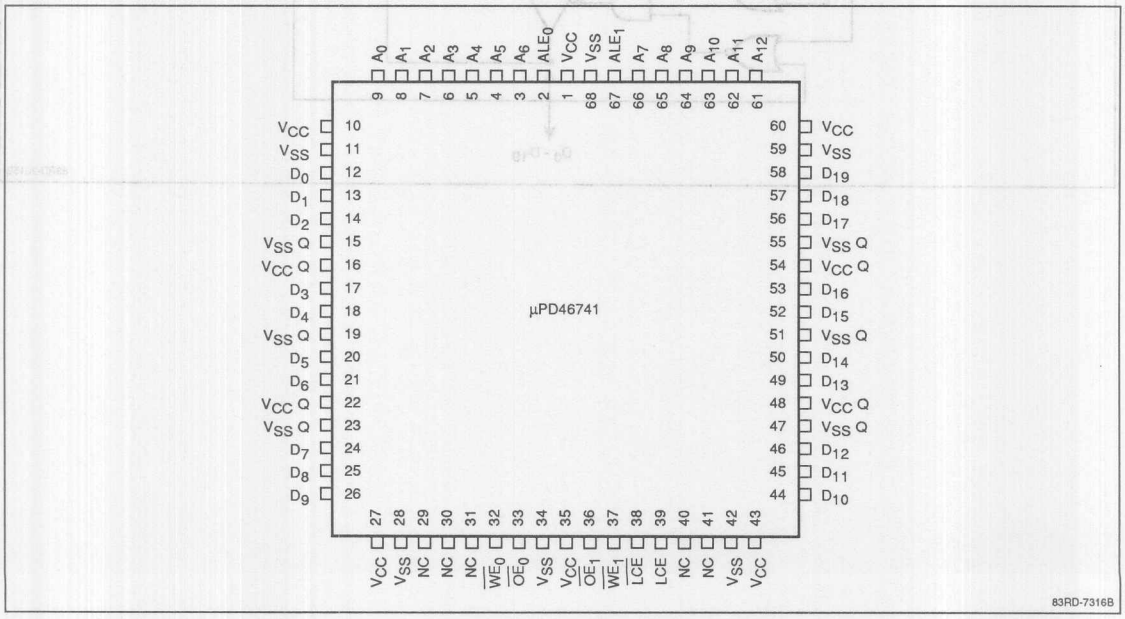
Part Number	Access Time	Package
μPD46741LP-15	15 ns	68-pin PLCC
LP-20	20 ns	

Pin Identification

Symbol	Function
A_0 - A_{12}	Addresses
ALE_0 - ALE_1	Address latch enable
D_0 - D_{19}	Data inputs/outputs
LCE, $\overline{LCE}$	Latch chip enable
$\overline{OE}_0$ - $\overline{OE}_1$	Output enable
$\overline{WE}_0$ - $\overline{WE}_1$	Write enable
V_{CC}	+5-volt power supply
V_{CCQ}	+5-volt power supply
V_{SS}	Ground
V_{SSQ}	Ground
NC	No connection

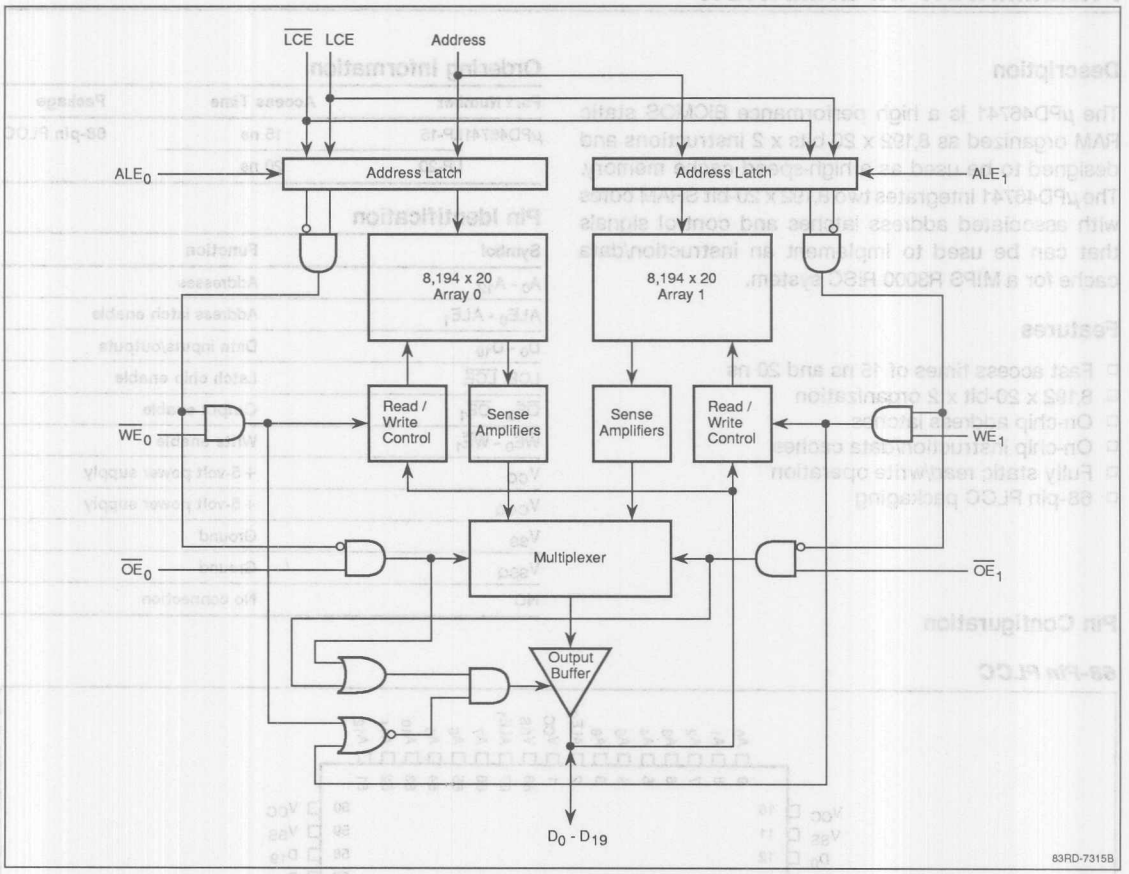
Pin Configuration

68-Pin PLCC



Please contact your NECEL representative for a copy of the complete data sheet.

Block Diagram



μPD4361
65,536 x 1-Bit
Static CMOS RAM

Description

The μPD4361 is a 65,536-word by 1-bit static RAM fabricated with advanced silicon-gate technology. CMOS peripheral circuits and N-channel memory cells with polysilicon resistors make the μPD4361 a high-speed device that requires very low power and no clock or refreshing.

The device is packaged in a 22-pin plastic DIP and 22-pin ceramic leadless chip carrier and has two types of access times, address and chip select. In addition, the μPD4361C-L features low-power data retention.

Features

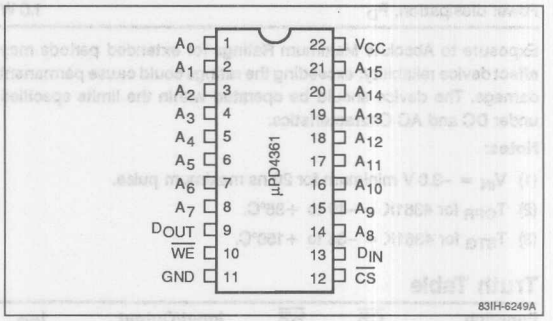
- 65, 536 x 1-bit organization
- Single +5-volt power supply
- Fully static operation—no clock or refreshing
- TTL-compatible inputs and outputs
- Separated data input and output
- Three-state outputs
- Data retention current of 50 μA max available from -L versions only
- Standard 22-pin plastic DIP and ceramic LCC
- Standard JEDEC pin configurations

Ordering Information

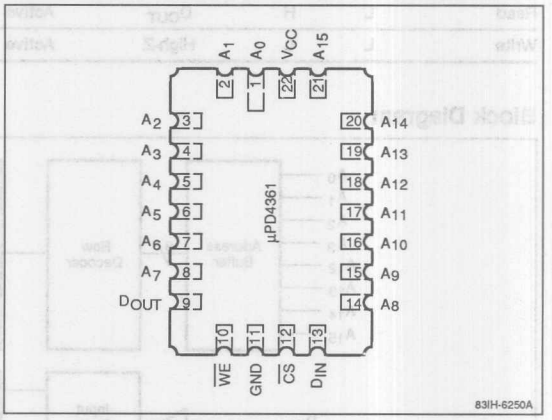
Part Number	Access Time (max)	Package
μPD4361C-45	45 ns	22-pin plastic DIP
C-55	55 ns	
C-70	70 ns	
μPD4361C-45L	45 ns	
C-55L	55 ns	
C-70L	70 ns	
μPD4361K-40	40 ns	22-pin ceramic LCC
K-45	45 ns	
K-55	55 ns	

Pin Configurations

22-Pin Plastic DIP



22-Pin Ceramic LCC



Pin Identification

Symbol	Function
A_0 - A_{15}	Address inputs
D_{IN}	Data input
D_{OUT}	Data output
$\overline{CS}$	Chip select
$\overline{WE}$	Write enable
GND	Ground
V_{CC}	+5-volt power supply

7

Absolute Maximum Ratings

Supply voltage, V_{CC}	−0.5 to +7.0 V
Input voltage, V_{IN} (Note 1)	−0.5 to +7.0 V
Operating temperature, T_{OPR} (Note 2)	0 to +70°C
Storage temperature, T_{STG} (Note 3)	−55 to +125°C
Power dissipation, P_D	1.0 W

Exposure to Absolute Maximum Ratings for extended periods may affect device reliability; exceeding the ratings could cause permanent damage. The device should be operated within the limits specified under DC and AC Characteristics.

Notes:

(1) V_{IN} = −3.0 V minimum for 20 ns maximum pulse.

(2) T_{OPR} for 4361K = −10 to +85°C.

(3) T_{STG} for 4361K = −65 to +150°C.

Truth Table

Function	$\overline{CS}$	$\overline{WE}$	Input/Output	I_{CC}
Not selected	H	X	High-Z	Standby
Read	L	H	D_{OUT}	Active
Write	L	L	High-Z	Active

Recommended Operating Conditions

Parameter	Symbol	Min	Typ	Max	Unit
Supply voltage	V_{CC}	4.5	5.0	5.5	V
Input voltage, high	V_{IH}	2.2		V_{CC} + 0.5	V
Input voltage, low	V_{IL}	−0.5		0.8	V
Operating temperature	T_A	0		70	°C

Notes:

(1) V_{IL} = −3.0 V minimum for 20 ns maximum pulse.

Capacitance

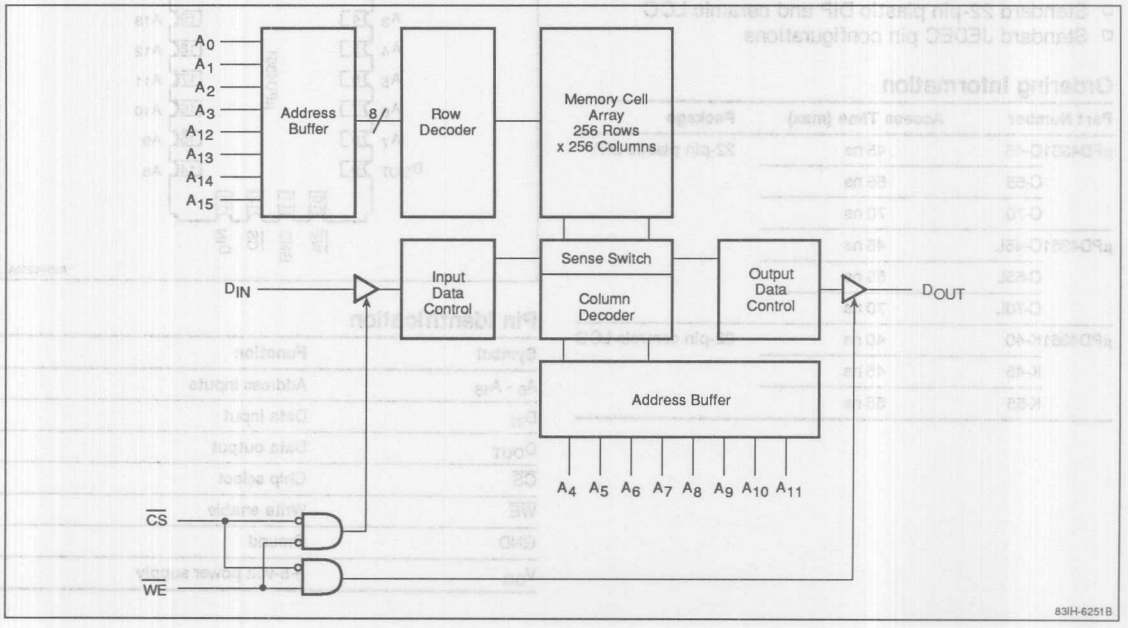
T_A = 25°C; f = 1 MHz; V_{IN} and V_{OUT} = 0 V (Note 1)

Parameter	Symbol	Min	Typ	Max	Unit
Input capacitance	C_{IN}			5	pF
Output capacitance	C_{DOUT}			7	pF

Notes:

(1) This parameter is sampled and not 100% tested.

Block Diagram



DC Characteristics

T_A = 0 to +70°C; V_{CC} = +5.0 V ± 10%

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions
Input leakage current	I_{LI}	−2		2	μA	V_{IN} = 0 V to V_{CC}
Output leakage current	I_{LO}	−2		2	μA	V_{OUT} = 0 V to V_{CC}; $\overline{CS}$ = V_{IH}
Operating supply current	I_{CC}			120	mA	$\overline{CS}$ = V_{IL}; I_{DOUT} = 0 mA
Standby supply current	I_{SB}			20	mA	$\overline{CS}$ = V_{IH}
	I_{SB1}			2	mA	$\overline{CS}$ ≥ V_{CC} − 0.2 V; V_{IN} ≤ 0.2 V or ≥ V_{CC} − 0.2 V
Output voltage, low	V_{OL}			0.4	V	I_{OL} = 8.0 mA
Output voltage, high	V_{OH}	2.4			V	I_{OH} = −4.0 mA

AC Characteristics

T_A = 0 to +70°C; V_{CC} = +5.0 V ± 10%

		μPD4361-40		μPD4361-45		μPD4361-55		μPD4361-70			
Parameter	Symbol	Min	Max	Min	Max	Min	Max	Min	Max	Unit	Test Conditions
Read Operation											
Read cycle time	t_{RC}	40		45		55		70		ns	(Note 2)
Address access time	t_{AA}		40		45		55		70	ns	
Chip select access time	t_{ACS}		40		45		55		70	ns	
Output hold from address change	t_{OH}	5		5		5		5		ns	
Chip select to output in low-Z	t_{LZ}	5		5		5		5		ns	(Note 3)
Chip deselect to output in high-Z	t_{HZ}	0	22	0	25	0	30	0	30	ns	(Note 4)
Chip select to power-up time	t_{PU}	0		0		0		0		ns	
Chip deselect to power-down time	t_{PD}	0	27	0	30	0	40	0	40	ns	
Write Operation											
Write cycle time	t_{WC}	40		45		55		70		ns	(Note 2)
Chip select to end of write	t_{CW}	37		40		50		60		ns	
Address valid to end of write	t_{AW}	37		40		50		60		ns	
Address setup time	t_{AS}	0		0		0		0		ns	
Write pulse width	t_{WP}	23		25		30		40		ns	
Write recovery time	t_{WR}	0		0		0		0		ns	
Data valid to end of write	t_{DW}	23		25		25		30		ns	
Data hold time	t_{DH}	0		0		0		0		ns	
Write enable to output in high-Z	t_{WZ}	0	22	0	25	0	25	0	30	ns	(Note 4)
Output active from end of write	t_{OW}	0		0		0		0		ns	(Note 3)

Notes:

(1) Input pulse levels = GND to 3.0 V; input pulse rise and fall times = 5 ns; timing reference levels = 1.5 V; see figures 1 and 2 for output load.

(2) All read cycle timings are referenced from the last valid address to the first transitioning address.

(3) Transition is measured at ±200 mV from steady-state voltage with the loading shown in figure 2.

(4) Transition is measured at V_{OL} + 200 mV and V_{OH} − 200 mV with the loading shown in figure 2.

Low V_{CC} Data Retention Characteristics (for -L Version Only)

T_A = 0 to 70°C

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions
Data retention supply voltage	V_{CCDR}	2.0		5.5	V	$\overline{CS} \geq V_{CC} - 0.2$ V; $V_{IN} \geq V_{CC} - 0.2$ V or $0 \text{ V} \leq V_{IN} \leq 0.2$ V
Data retention supply current	I_{CCDR}		1	50	µA	V_{CC} = 3.0 V; $\overline{CS} \geq V_{CC} - 0.2$ V; $V_{IN} \geq V_{CC} - 0.2$ V or $0 \text{ V} \leq V_{IN} \leq 0.2$ V
Chip deselect to data retention	t_{CDR}	0			ns	
Operation recovery time	t_R	t_{RC}			ns	

Data Retention Timing

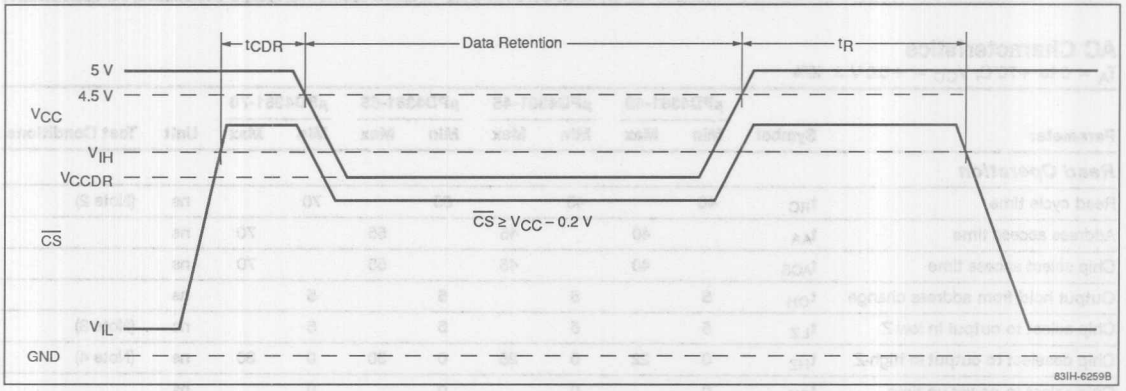


Figure 1. Output Load

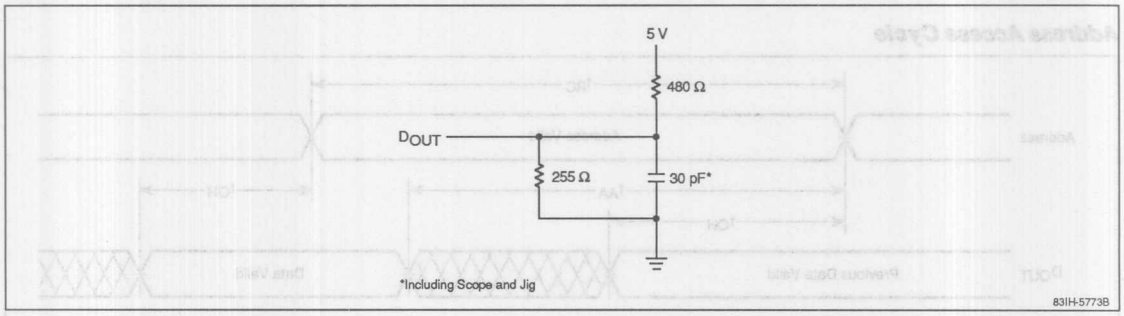
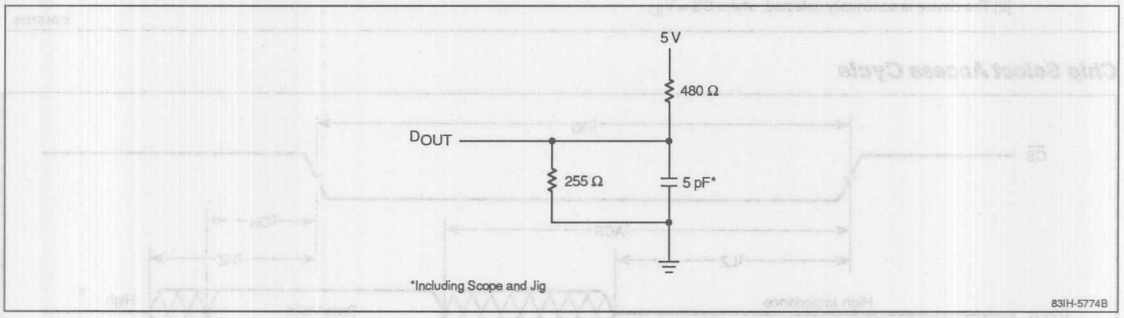


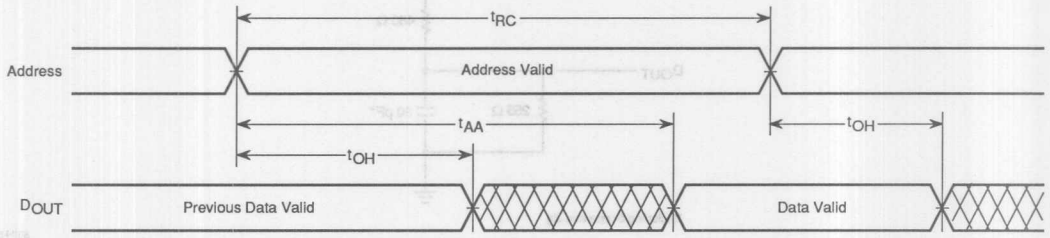
Figure 2. Output Load for t_{HZ}, t_{LZ}, t_{WZ}, and t_{OW}



7

Timing Waveforms

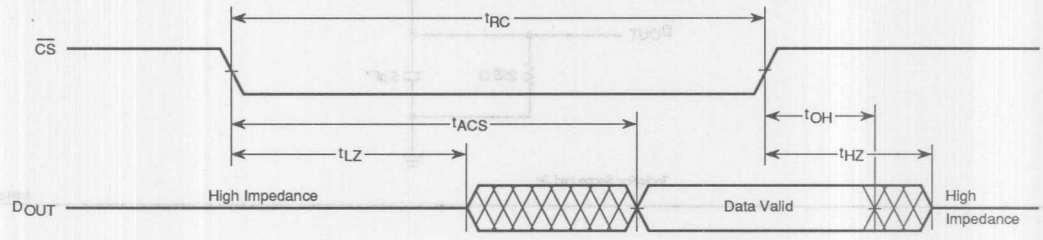
Address Access Cycle



Notes:
[1] $\overline{WE}$ is held high for a read cycle.
[2] The device is continually selected, where $\overline{CS} = V_{IL}$.

83IH-5775B

Chip Select Access Cycle

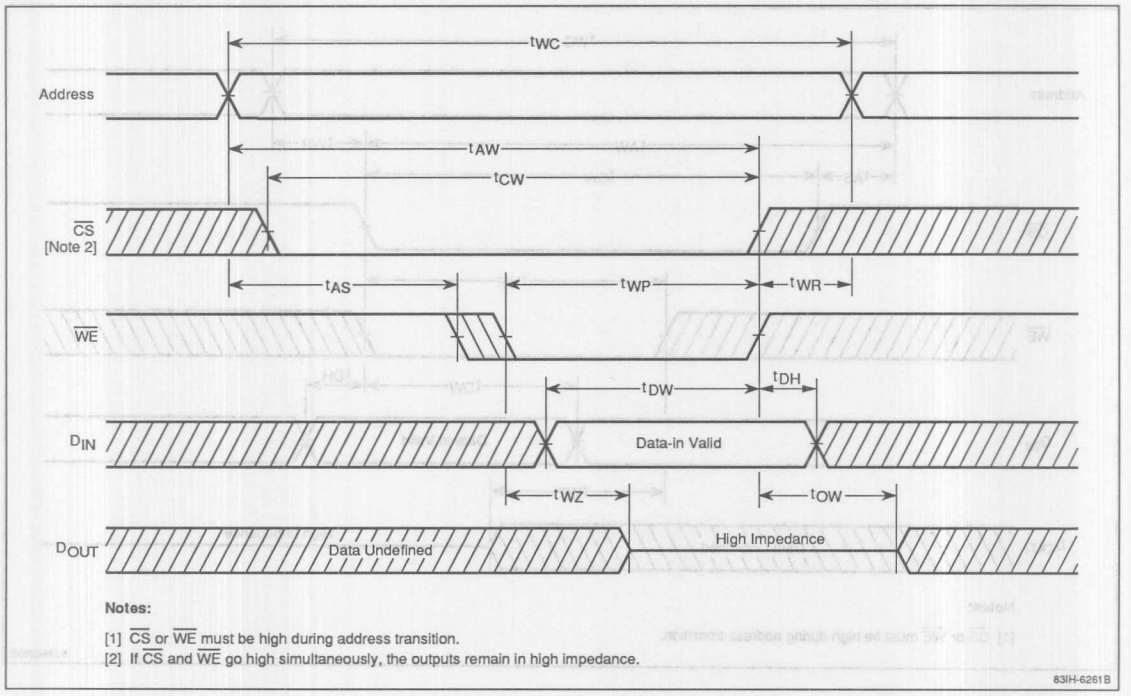


Notes:
[1] $\overline{WE}$ is held high for a read cycle.
[2] Address valid prior to or coincident with the low transition of $\overline{CS}$.

83IH-6252B

Timing Waveforms (cont)

$\overline{WE}$-Controlled Write Cycle



Notes:

[1] $\overline{CS}$ or $\overline{WE}$ must be high during address transition.

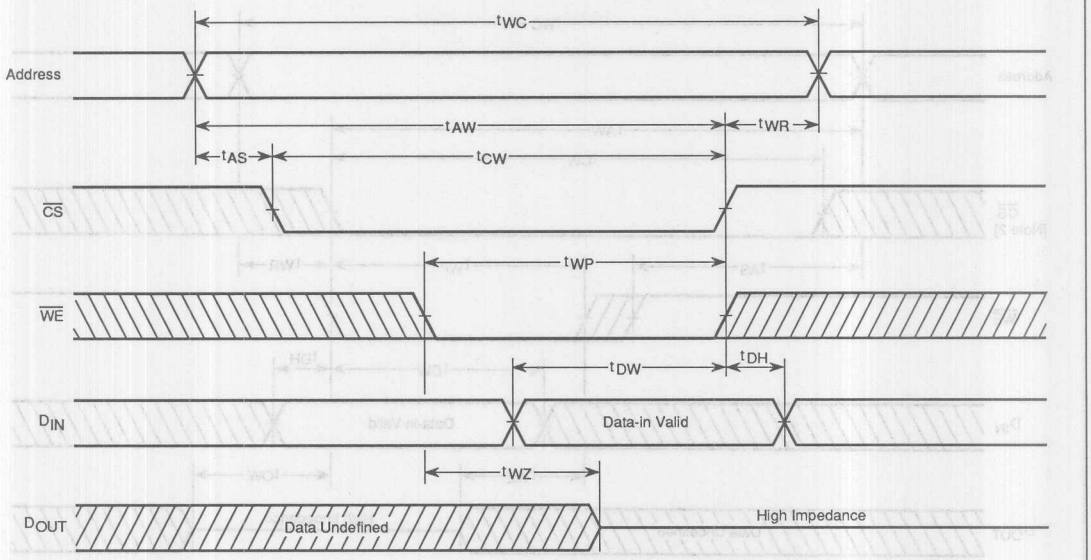
[2] If $\overline{CS}$ and $\overline{WE}$ go high simultaneously, the outputs remain in high impedance.

83IH-6261B

7

Timing Waveforms (cont)

$\overline{CS}$-Controlled Write Cycle



Notes:

[1] $\overline{CS}$ or $\overline{WE}$ must be high during address transition.

83IH-6262B

μPD4362
16,362 x 4-Bit
Static CMOS RAM

Description

The μPD4362 is a 16,384-word by 4-bit static RAM fabricated with advanced silicon-gate technology. A unique design using CMOS peripheral circuits and N-channel memory cells with polysilicon resistors makes the μPD4362 a high-speed device that requires very low power and no clock or refreshing.

The μPD4362 is packaged in a standard 22-pin plastic DIP.

Features

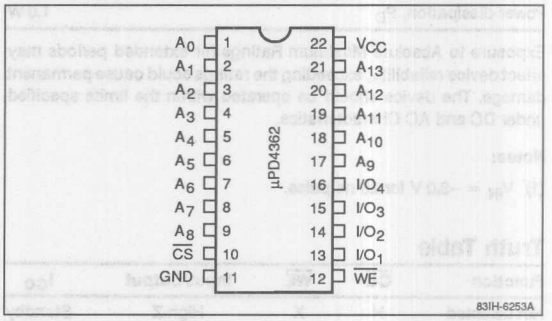
- Single +5-volt power supply
- Fully static operation—no clock or refreshing
- TTL-compatible inputs and outputs
- Common I/O capability
- Standard 300-mil, 22-pin plastic DIP packaging

Ordering Information

Part Number	Access Time (max)	Package
μPD4362C-45	45 ns	22-pin plastic DIP
C-55	55 ns	
C-70	70 ns	

Pin Configuration

22-Pin Plastic DIP



Pin Identification

Symbol	Function
A_0 - A_{13}	Address inputs
I/O_1 - I/O_4	Data inputs and outputs
$\overline{CS}$	Chip select
$\overline{WE}$	Write enable
GND	Ground
V_{CC}	+5-volt power supply

7

Absolute Maximum Ratings

Supply voltage, V_{CC}	−0.5 to +7.0 V
Input and output voltages, V_{IN} (Note 1)	−0.5 to +7.0 V
Operating temperature, T_{OPR}	0 to +70°C
Storage temperature, T_{STG}	−55 to +125°C
Power dissipation, P_D	1.0 W

Exposure to Absolute Maximum Ratings for extended periods may affect device reliability; exceeding the ratings could cause permanent damage. The device should be operated within the limits specified under DC and AC Characteristics.

Notes:

(1) V_{IN} = −3.0 V for 20 ns pulse.

Truth Table

Function	$\overline{CE}$	$\overline{WE}$	Input/Output	I_{CC}
Not selected	H	X	High-Z	Standby
Read	L	H	D_{OUT}	Active
Write	L	L	D_{IN}	Active

Notes:

(1) X = don't care.

Capacitance

T_A = 25°C; f = 1 MHz (Note 1); V_{IN} and V_{DOUT} = 0 V

Parameter	Symbol	Min	Typ	Max	Unit
Input capacitance	C_{IN}			5	pF
Output capacitance	C_{DOUT}			7	pF

Notes:

(1) This parameter is sampled and not 100% tested.

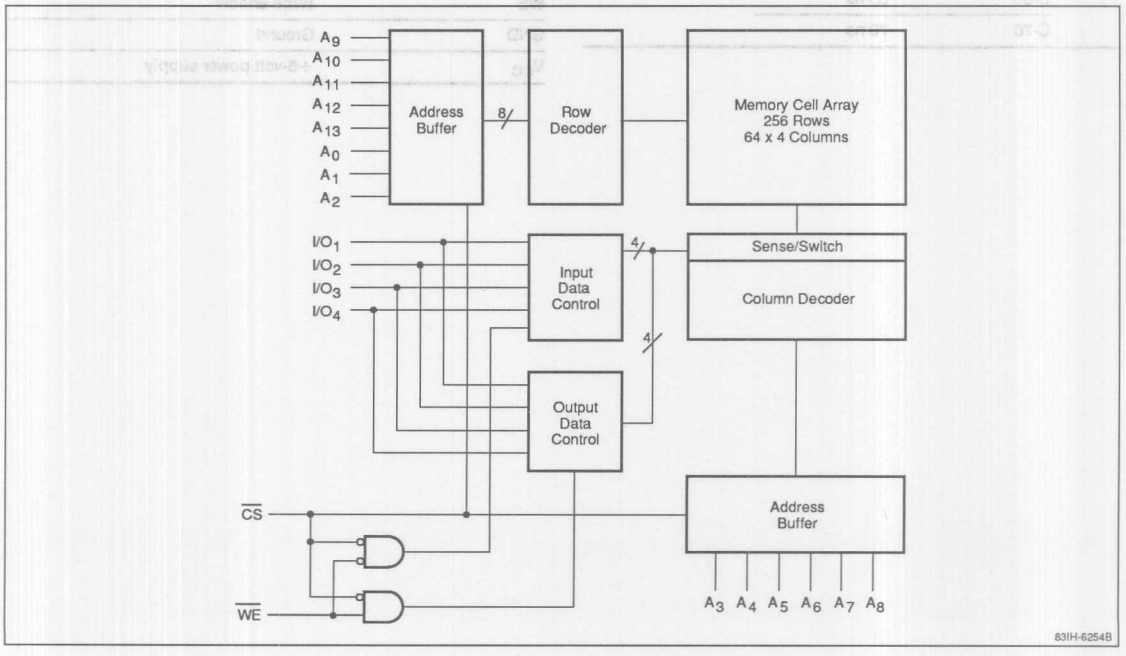
Recommended Operating Conditions

Parameter	Symbol	Min	Typ	Max	Unit
Supply voltage	V_{CC}	4.5	5.0	5.5	V
Input voltage, high	V_{IH}	2.2		V_{CC} + 0.3	V
Input voltage, low	V_{IL}	−0.5		0.8	V
Operating temperature	T_A	0		70	°C

Notes:

(1) V_{IL} = −3.0 V for 20 ns pulse.

Block Diagram



DC Characteristics

T_A = 0 to +70°C; V_{CC} = +5.0 V ± 10%

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions
Input leakage current	I_{LI}	−2		2	μA	V_{IN} = 0 V to V_{CC}; V_{CC} = max
Output leakage current	I_{LO}	−2		2	μA	V_{OUT} = 0 V to V_{CC}; $\overline{CS}$ = V_{IH}; V_{CC} = max
Operating supply current	I_{CC}			90	mA	$\overline{CS}$ = V_{IL}; I_{DOUT} = 0 mA
Standby supply current	I_{SB}			20	mA	$\overline{CS}$ = V_{IH}
	I_{SB1}			2	mA	$\overline{CS}$ ≥ V_{CC} − 0.2 V; V_{IN} ≤ 0.2 V or ≥ V_{CC} − 0.2 V
Output voltage, low	V_{OL}			0.4	V	I_{OL} = 8.0 mA
Output voltage, high	V_{OH}	2.4			V	I_{OH} = −4.0 mA

AC Characteristics

T_A = 0 to +70°C; V_{CC} = +5.0 V ± 10%

		μPD4362-45		μPD4362-55		μPD4362-70			
Parameter	Symbol	Min	Max	Min	Max	Min	Max	Unit	Test Conditions
Read Operation									
Read cycle time	t_{RC}	45		55		70		ns	(Note 2)
Address access time	t_{AA}		45		55		70	ns	
Chip selection access time	t_{ACS}		45		55		70	ns	
Output hold from address change	t_{OH}	5		5		5		ns	
Chip selection to output to low-Z	t_{LZ}	5		5		5		ns	(Note 3)
Chip deselection to output to high-Z	t_{HZ}	0	25	0	25	0	30	ns	(Note 4)
Chip selection to power-up time	t_{PU}	0		0		0		ns	
Chip deselection to power-down time	t_{PD}	0	45	0	55	0	55	ns	
Write Operation									
Write cycle time	t_{WC}	45		55		70		ns	(Note 2)
Chip selection to end of write	t_{CW}	40		50		60		ns	
Address valid to end of write	t_{AW}	40		50		60		ns	
Address setup time	t_{AS}	0		0		0		ns	
Write pulse width	t_{WP}	40		50		60		ns	
Write recovery time	t_{WR}	0		0		0		ns	
Data valid to end of write	t_{DW}	20		25		30		ns	
Data hold time	t_{DH}	0		0		0		ns	
Write enable to output in high-Z	t_{WZ}	0	20	0	25	0	30	ns	(Note 4)
Output active from end of write	t_{OW}	0		0		0		ns	(Note 3)

Notes:

(1) Input pulse levels = GND to 3.0 V; input pulse rise and fall times = 5 ns; timing reference levels = 1.5 V; see figures 1 and 2 for output load.

(2) All read cycle timings are referenced from the last valid address to the first transitioning address.

(3) Transition is measured at ±200 mV from steady-state voltage with the loading shown in figure 2.

(4) Transition is measured at V_{OL} + 200 mV and V_{OH} − 200 mV with the loading shown in figure 2.

7

Figure 1. Output Load

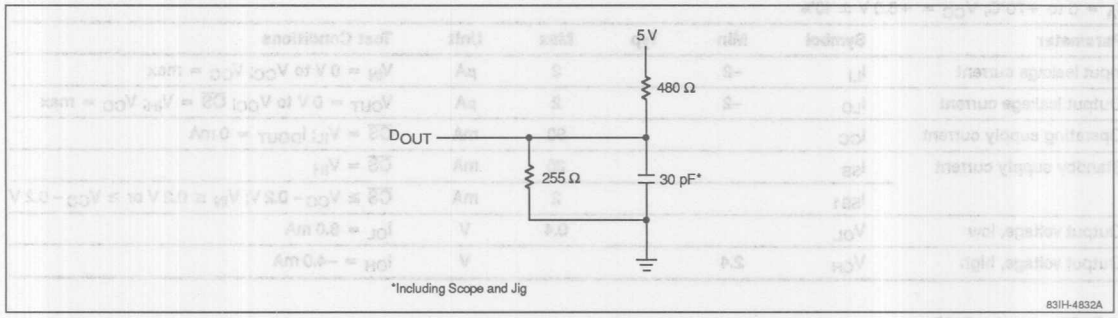
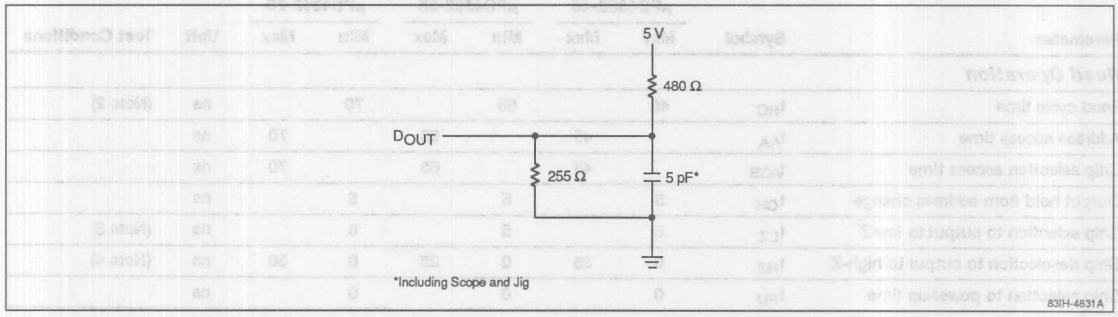
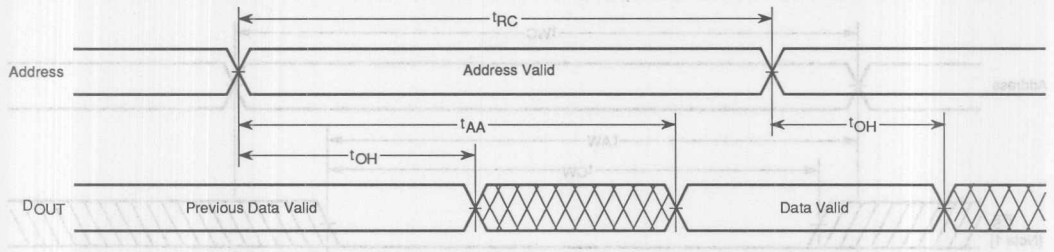


Figure 2. Output Load for t_{HZ}, t_{LZ}, t_{WZ}, and t_{OW}



Timing Waveforms

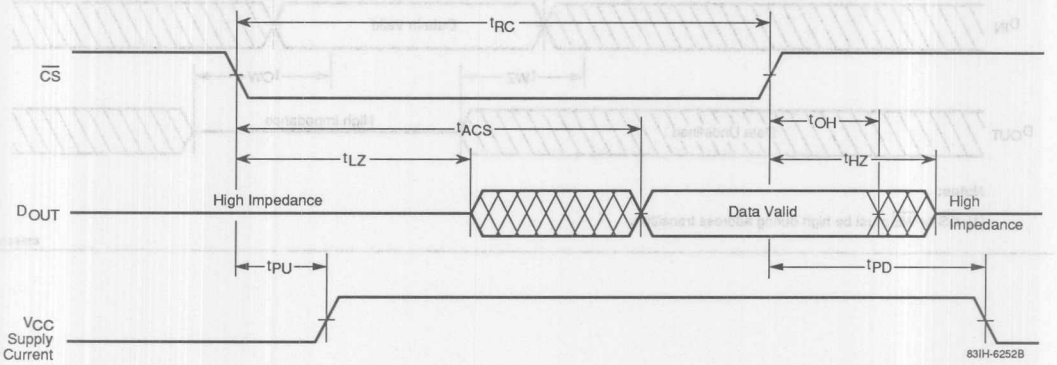
Address Access Cycle



Notes:
[1] $\overline{WE}$ is held high for a read cycle.
[2] The device is continually selected, where $\overline{CS} = V_{IL}$.

83IH-5775B

Chip Select Access Cycle



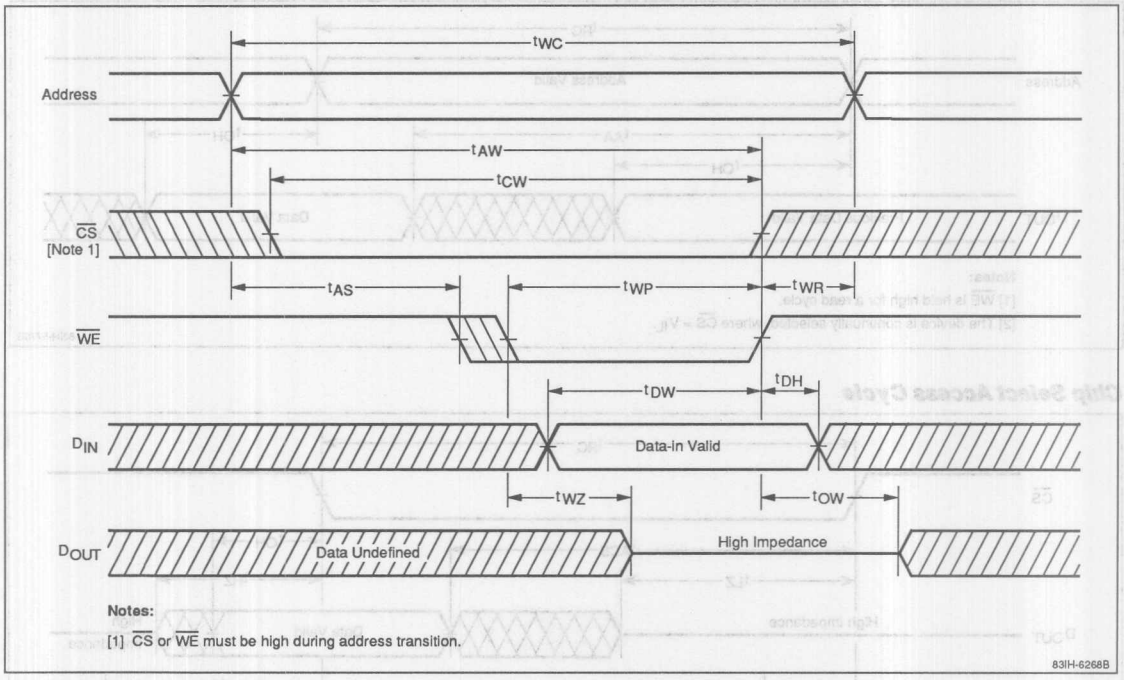
83IH-6252B

Notes:
[1] $\overline{WE}$ is held high for a read cycle.
[2] Address is valid prior to or coincident with the low transition of $\overline{CS}$.

7

Timing Waveforms (cont)

$\overline{WE}$-Controlled Write Cycle



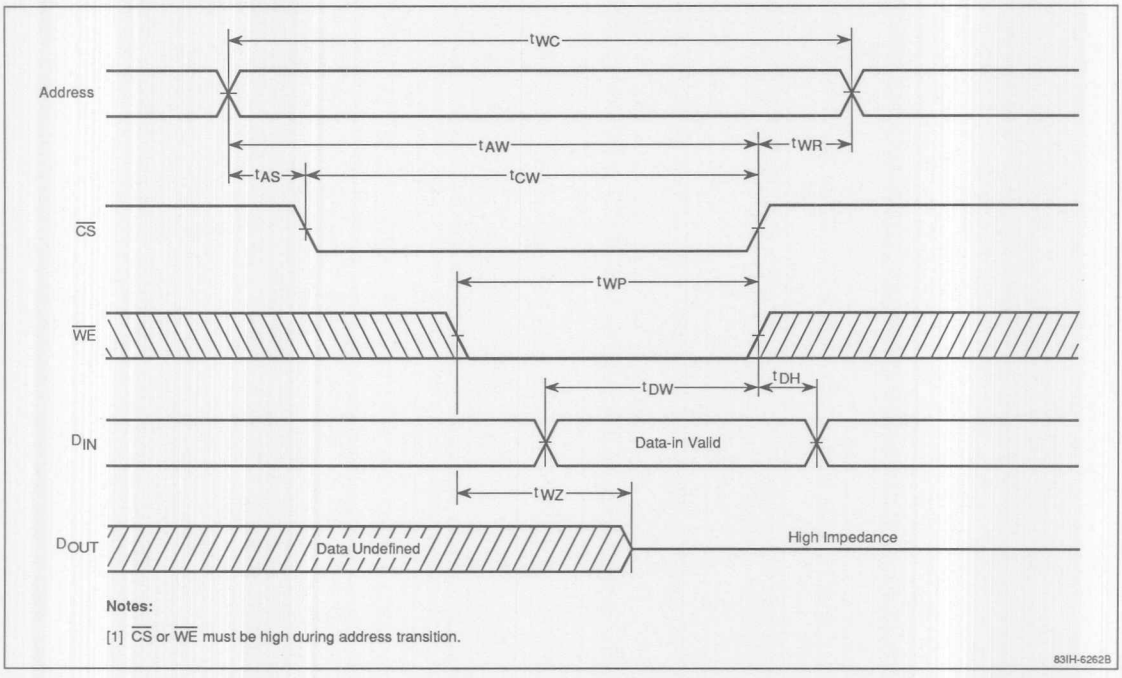
Notes:

[1] $\overline{CS}$ or $\overline{WE}$ must be high during address transition.

83IH-6268B

Timing Waveforms (cont)

$\overline{CS}$-Controlled Write Cycle

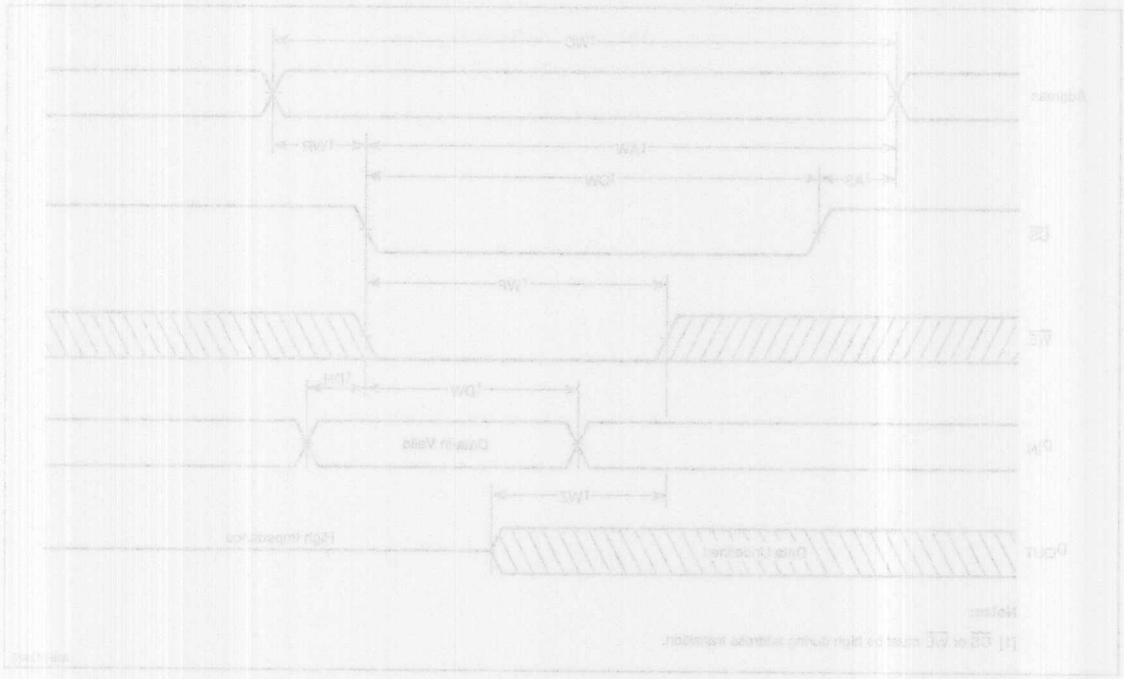


Notes:

[1] $\overline{CS}$ or $\overline{WE}$ must be high during address transition.

83IH-6262B

7



μPD4363
16,364 x 4-Bit Static CMOS RAM

Description

The μPD4363 is a 16,384-word by 4-bit static RAM fabricated with advanced silicon-gate technology. A unique design using CMOS peripheral circuits and N-channel memory cells with polysilicon resistors makes the μPD4363 a high-speed device that requires very low power and no clock or refreshing.

The μPD4363 is packaged in a standard 300-mil, 24-pin plastic DIP.

Features

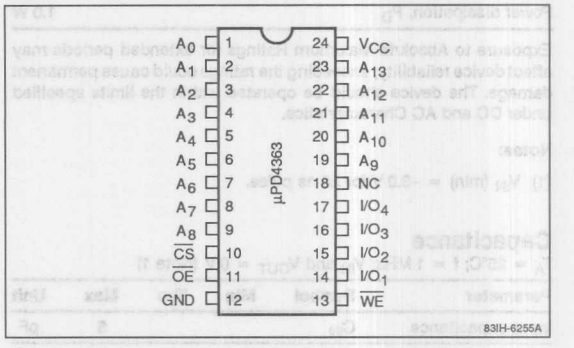
- Single +5-volt power supply
- Fully static operation—no clock or refreshing
- TTL-compatible inputs and outputs
- Common I/O capability
- $\overline{OE}$ eliminates the need for external bus buffers
- Three-state outputs
- Low power dissipation
  - 90 mA max (active)
  - 2 mA max (standby)
- Standard 300-mil, 24-pin plastic DIP packaging

Ordering Information

Part Number	Access Time (max)	Package
μPD4363C-45	45 ns	24-pin plastic DIP
C-55	55 ns	
C-70	70 ns	

Pin Configuration

24-Pin Plastic DIP



Pin Identification

Symbol	Function
A_0 - A_{13}	Address inputs
I/O_1 - I/O_4	Data inputs and outputs
$\overline{CS}$	Chip select
$\overline{OE}$	Output enable
$\overline{WE}$	Write enable
GND	Ground
V_{CC}	+5-volt power supply
NC	No connection

7

Absolute Maximum Ratings

Supply voltage, V_{CC}	−0.5 to +7.0 V
Input and output voltages, V_{IN} (Note 1)	−0.5 to +7.0 V
Operating temperature, T_{OPR}	0 to +70°C
Storage temperature, T_{STG}	−55 to +125°C
Power dissipation, P_D	1.0 W

Exposure to Absolute Maximum Ratings for extended periods may affect device reliability; exceeding the ratings could cause permanent damage. The device should be operated within the limits specified under DC and AC Characteristics.

Notes:

(1) V_{IN} (min) = −3.0 V for 20 ns pulse.

Capacitance

T_A = 25°C; f = 1 MHz; V_{IN} and V_{OUT} = 0 V (Note 1)

Parameter	Symbol	Min	Typ	Max	Unit
Input capacitance	C_{IN}			5	pF
Output capacitance	C_{DOUT}			7	pF

Notes:

(1) This parameter is sampled and not 100% tested.

Recommended Operating Conditions

Parameter	Symbol	Min	Typ	Max	Unit
Supply voltage	V_{CC}	4.5	5.0	5.5	V
Input voltage, high	V_{IH}	2.2		V_{CC} + 0.3	V
Input voltage, low	V_{IL}	−0.5		0.8	V
Operating temperature	T_A	0		70	°C

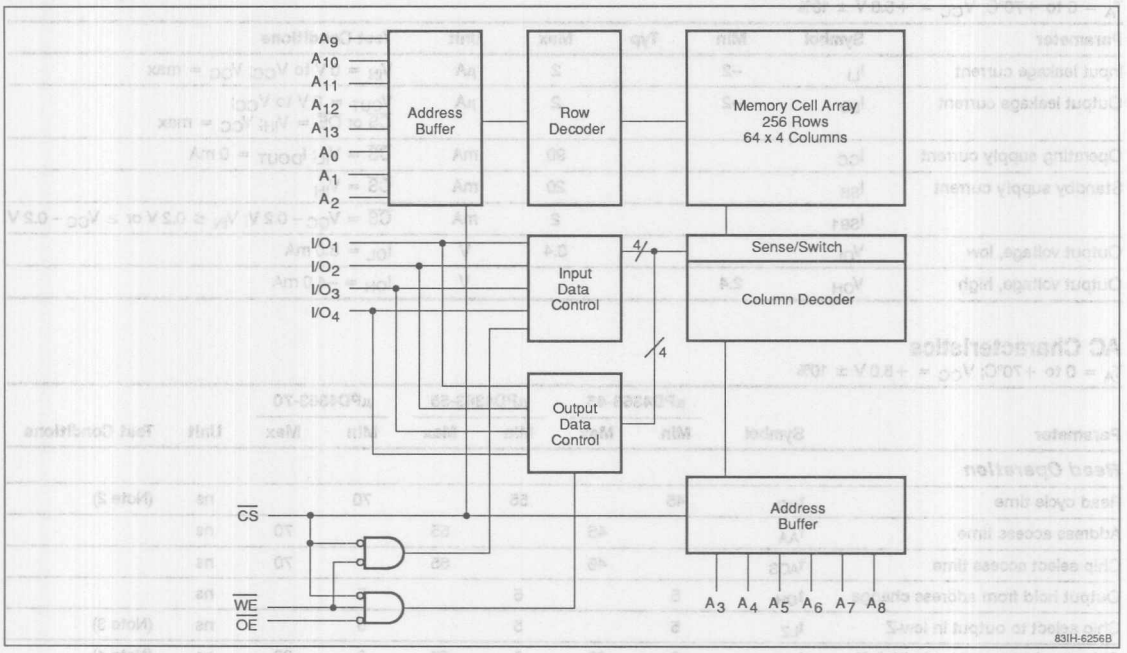
Notes:

(1) V_{IL} = −3.0 V for 20 ns pulse.

Truth Table

Function	$\overline{CS}$	$\overline{WE}$	$\overline{OE}$	Input/Output	I_{CC}
Not selected	H	X	X	High-Z	Standby
Read	L	H	L	D_{OUT}	Active
D_{OUT} disabled	L	H	H	High-Z	Active
Write	L	L	X	D_{IN}	Active

Block Diagram



7

DC Characteristics

T_A = 0 to +70°C; V_{CC} = +5.0 V ± 10%

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions
Input leakage current	I_{LI}	−2		2	µA	V_{IN} = 0 V to V_{CC}; V_{CC} = max
Output leakage current	I_{LO}	−2		2	µA	V_{OUT} = 0 V to V_{CC}; $\overline{CS}$ or $\overline{OE}$ = V_{IH}; V_{CC} = max
Operating supply current	I_{CC}			90	mA	$\overline{CS}$ = V_{IL}; I_{DOUT} = 0 mA
Standby supply current	I_{SB}			20	mA	$\overline{CS}$ = V_{IH}
	I_{SB1}			2	mA	$\overline{CS}$ = V_{CC} − 0.2 V; V_{IN} ≤ 0.2 V or ≥ V_{CC} − 0.2 V
Output voltage, low	V_{OL}			0.4	V	I_{OL} = 8.0 mA
Output voltage, high	V_{OH}	2.4			V	I_{OH} = −4.0 mA

AC Characteristics

T_A = 0 to +70°C; V_{CC} = +5.0 V ± 10%

		µPD4363-45		µPD4363-55		µPD4363-70			
Parameter	Symbol	Min	Max	Min	Max	Min	Max	Unit	Test Conditions
Read Operation									
Read cycle time	t_{RC}	45		55		70		ns	(Note 2)
Address access time	t_{AA}		45		55		70	ns	
Chip select access time	t_{ACS}		45		55		70	ns	
Output hold from address change	t_{OH}	5		5		5		ns	
Chip select to output in low-Z	t_{LZ}	5		5		5		ns	(Note 3)
Chip deselect to output in high-Z	t_{HZ}	0	20	0	25	0	30	ns	(Note 4)
Output enable access time	t_{OE}		20		25		30	ns	
Output enable to output in low-Z	t_{OLZ}	5		5		5		ns	(Note 3)
Output disable to output in high-Z	t_{OHZ}	0	25	0	30	0	35	ns	(Note 4)
Chip select to power-up time	t_{PU}	0		0		0		ns	
Chip deselect to power-down time	t_{PD}	0	30	0	40	0	40	ns	
Write Operation									
Write cycle time	t_{WC}	45		55		70		ns	(Note 2)
Chip select to end of write	t_{CW}	40		50		60		ns	
Address valid to end of write	t_{AW}	40		50		60		ns	
Address setup time	t_{AS}	0		0		0		ns	
Write pulse width	t_{WP}	40		50		60		ns	
Write recovery time	t_{WR}	0		0		0		ns	
Data valid to end of write	t_{DW}	20		25		30		ns	
Data hold time	t_{DH}	0		0		0		ns	
Write enable to output in high-Z	t_{WZ}	0	20	0	25	0	30	ns	(Note 4)
Output active from end of write	t_{OW}	0		0		0		ns	(Note 3)

Notes:

(1) Input pulse levels = GND to 3.0 V; input pulse rise and fall times = 5 ns; timing reference levels = 1.5 V; see figures 1 and 2 for output load.

(2) All read and write cycle timings are referenced from the last valid address to the first transitioning address.

(3) Transition is measured at ±200 mV from steady-state voltage with the loading shown in figure 2.

(4) Transition is measured at V_{OL} + 200 mV and V_{OH} − 200 mV with the loading shown in figure 2.

Figure 1. Output Load

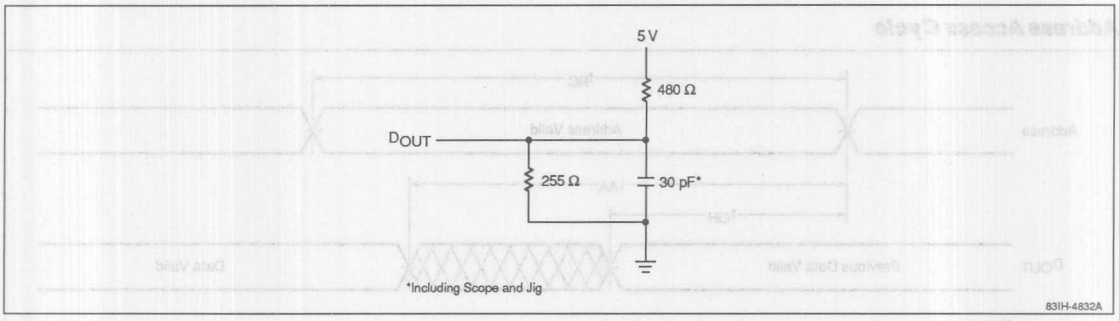
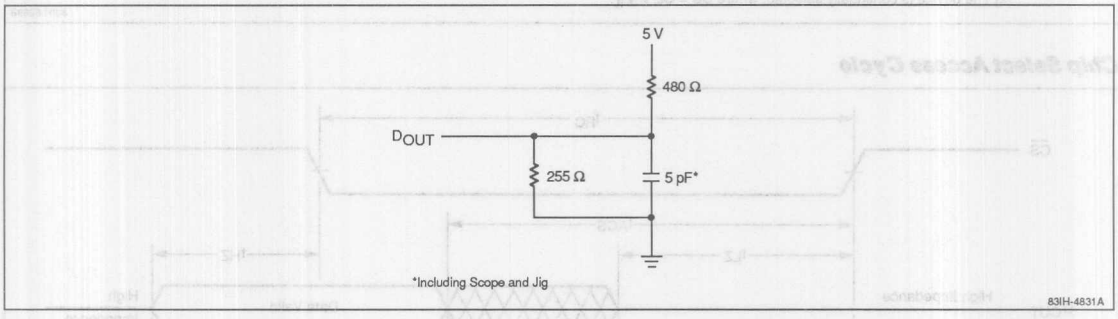


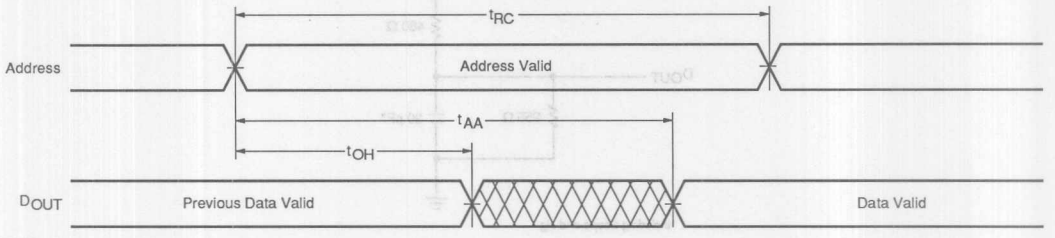
Figure 2. Output Load for t_{HZ}, t_{LZ}, t_{OHZ}, t_{OLZ}, t_{WZ}, and t_{OW}



7

Timing Waveforms (cont)

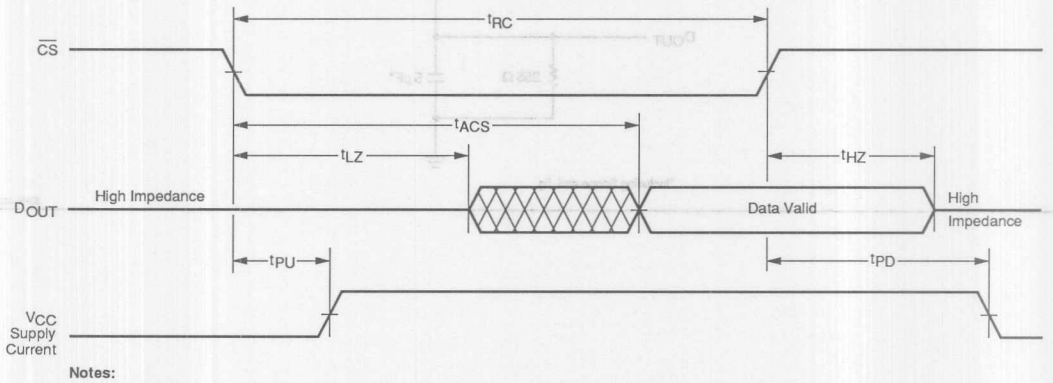
Address Access Cycle



Notes:
[1] $\overline{WE}$ is held high for a read cycle.
[2] The device is continually selected, where $\overline{CS} = \overline{OE} = V_{IL}$.

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Chip Select Access Cycle

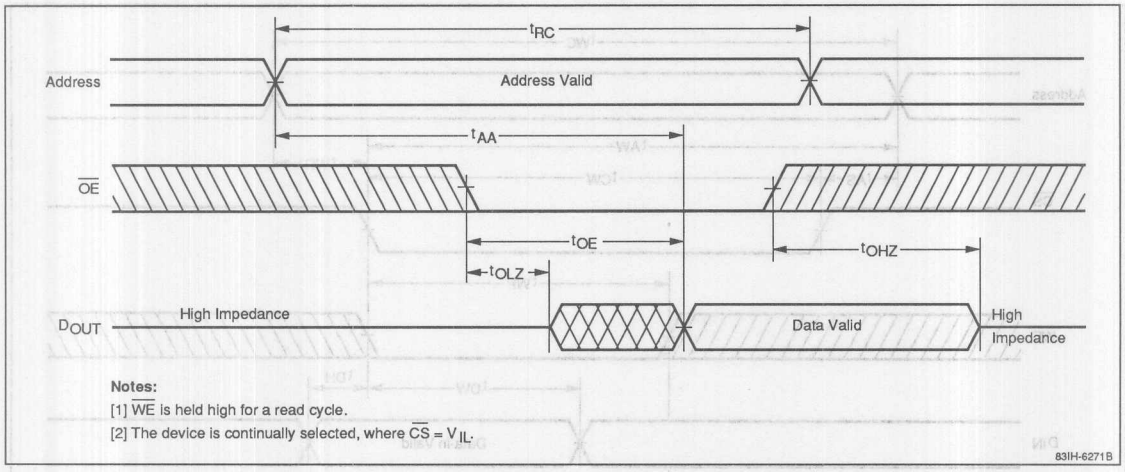


Notes:
[1] $\overline{WE}$ is held high for a read cycle.
[2] Address valid prior to or coincident with the low transition of $\overline{CS}$.
[3] $\overline{OE} = V_{IL}$.

83IH-6270B

Timing Waveforms (cont)

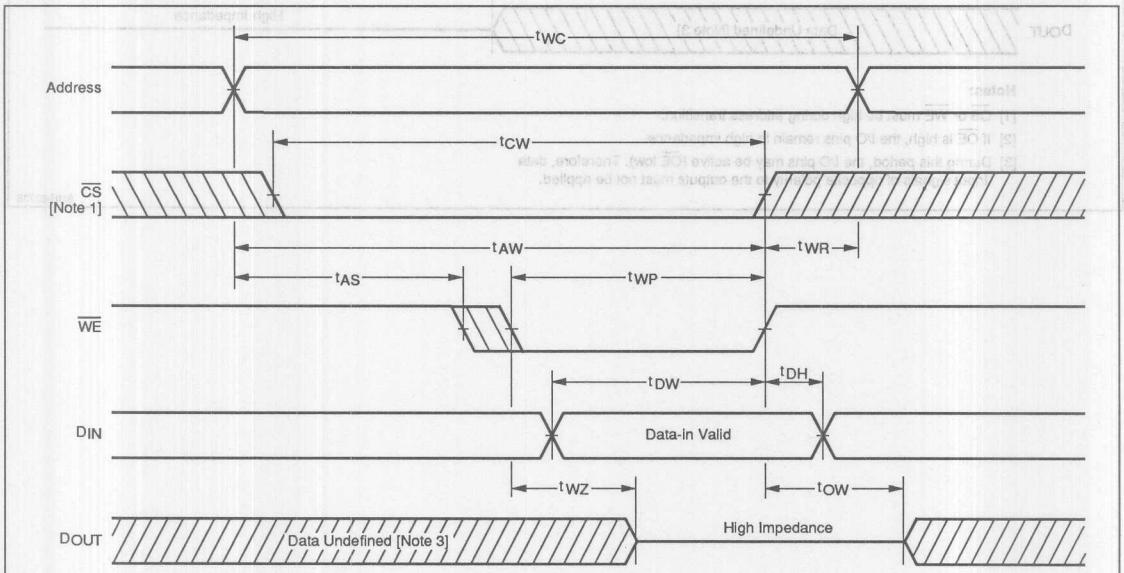
$\overline{OE}$-Controlled Access Cycle



Notes:
[1] $\overline{WE}$ is held high for a read cycle.
[2] The device is continually selected, where $\overline{CS} = V_{IL}$.

83IH-6271B

$\overline{WE}$-Controlled Write Cycle



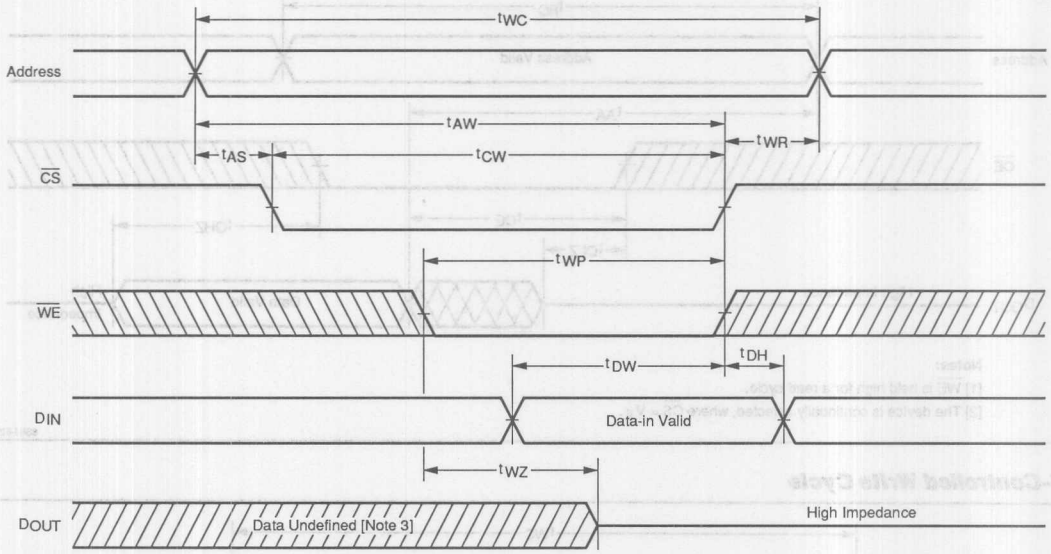
Notes:
[1] $\overline{CS}$ or $\overline{WE}$ must be high during address transition.
[2] If $\overline{OE}$ is high, the I/O pins remain in high impedance.
[3] During this period, the I/O pins may be active ($\overline{OE}$ low). Therefore, data input signals of opposite polarity to the outputs must not be applied.

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Timing Waveforms (cont)

$\overline{CS}$-Controlled Write Cycle



Notes:

[1] $\overline{CS}$ or $\overline{WE}$ must be high during address transition.

[2] If $\overline{OE}$ is high, the I/O pins remain in high impedance.

[3] During this period, the I/O pins may be active ($\overline{OE}$ low). Therefore, data input signals of opposite polarity to the outputs must not be applied.

83IH-6273B

μPD43251
262,144 x 1-Bit
Static CMOS RAM

Description

The μPD43251 is a 262,144-word by 1-bit static RAM fabricated with advanced silicon-gate technology. A unique design that uses CMOS peripheral circuits and N-channel memory cells with polysilicon resistors makes the μPD43251 a high-speed device that requires no clock or refreshing. The μPD43251 is available in 24-pin plastic DIP or 24-pin plastic SOJ packaging.

Features

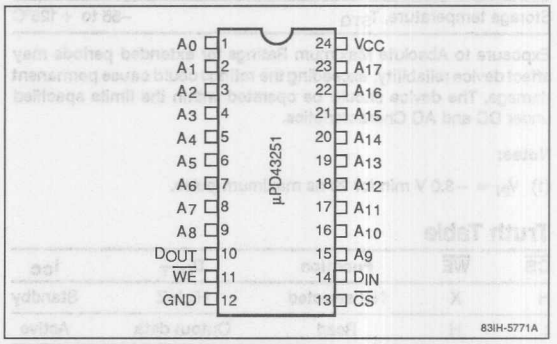
- 262,144-word x 1-bit organization
- Single +5-volt power supply
- Fully static operation—no clock or refreshing required
- TTL-compatible inputs and outputs
- Separated data input and output
- Three-state outputs
- Power dissipation
  - 100 mA max (active)
  - 2 mA max (standby)
- Standard 300-mil, 24-pin plastic DIP or plastic SOJ packaging

Ordering Information

Part Number	Access Time (max)	Package
μPD43251C-35	35 ns	24-pin plastic DIP
C-45	45 ns	
C-55	55 ns	
μPD43251LA-35	35 ns	24-pin plastic SOJ
LA-45	45 ns	
LA-55	55 ns	

Pin Configuration

24-Pin Plastic DIP or SOJ



Pin Identification

Symbol	Function
A_0 - A_{17}	Address inputs
D_{IN}	Data input
D_{OUT}	Data output
$\overline{CS}$	Chip select
$\overline{WE}$	Write enable
GND	Ground
V_{CC}	+5-volt power supply

7

New speeds to 15 ns will be available in 1991.

Absolute Maximum Ratings

Power supply voltage, V_{CC}	−0.5 to +7.0 V
Input voltage, V_{IN} (Note 1)	−0.5 to +7.0 V
Output voltage, V_{OUT}	−0.5 to +7.0 V
Operating temperature, T_{OPR}	0 to +70°C
Storage temperature, T_{STG}	−55 to +125°C

Exposure to Absolute Maximum Ratings for extended periods may affect device reliability; exceeding the ratings could cause permanent damage. The device should be operated within the limits specified under DC and AC Characteristics.

Notes:

(1) V_{IN} = −3.0 V min for 20 ns maximum pulse.

Truth Table

$\overline{CS}$	$\overline{WE}$	Function	D_{OUT}	I_{CC}
H	X	Not selected	High-Z	Standby
L	H	Read	Output data	Active
L	L	Write	High-Z	Active

Capacitance

T_A = +25°C; f = 1 MHz (Note 1); V_{IN} and V_{OUT} = 0 V

Parameter	Symbol	Min	Typ	Max	Unit
Input capacitance	C_I			6	pF
Output capacitance	C_O			8	pF

Notes:

(1) This parameter is sampled and not 100% tested.

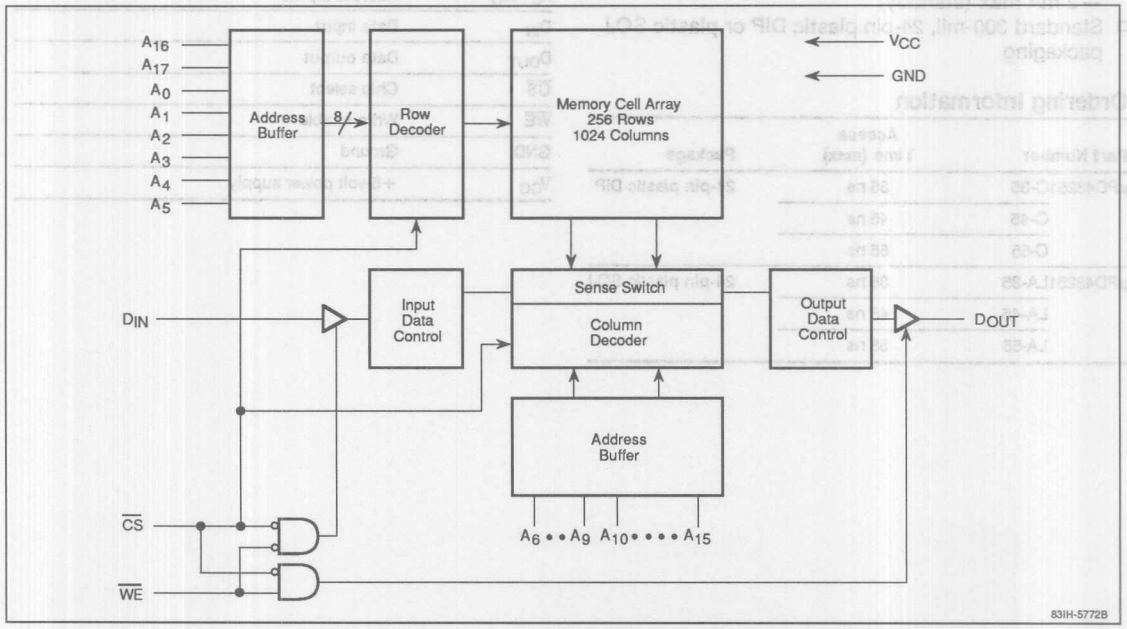
Recommended Operating Conditions

Parameter	Symbol	Min	Typ	Max	Unit
Supply voltage	V_{CC}	4.5	5.0	5.5	V
Input voltage, low (Note 1)	V_{IL}	−0.5		0.8	V
Input voltage, high	V_{IH}	2.2		V_{CC} + 0.3	V
Ambient temperature	T_A	0		70	°C

Notes:

(1) V_{IL} = −3.0 V min for 20 ns maximum pulse.

Block Diagram



DC Characteristics

T_A = 0 to +70°C; V_{CC} = +5.0 V ± 10%

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions
Input leakage current	I_{LI}	−2		2	μA	V_{IN} = 0 V to V_{CC}
Output leakage current	I_{LO}	−2		2	μA	V_{OUT} = 0 V to V_{CC}; $\overline{CS}$ = V_{IH}
Operating supply current	I_{CC}			100	mA	$\overline{CS}$ = V_{IL}; I_{OUT} = 0 mA
Standby supply current	I_{SB}			30	mA	$\overline{CS}$ = V_{IH}; V_{IN} = V_{IH} or V_{IL}
	I_{SB1}			2	mA	$\overline{CS}$ ≥ V_{CC} − 0.2 V; V_{IN} ≤ 0.2 V or ≥ V_{CC} − 0.2 V
Output voltage, low	V_{OL}			0.4	V	I_{OL} = 8.0 mA
Output voltage, high	V_{OH}	2.4			V	I_{OH} = −4.0 mA

AC Characteristics

T_A = 0 to +70°C; V_{CC} = +5.0 V ± 10%

		μPD43251-35		μPD43251-45		μPD43251-55			
Parameter	Symbol	Min	Max	Min	Max	Min	Max	Unit	Test Conditions (Note 1)
Read Operation									
Read cycle time	t_{RC}	35		45		55		ns	(Note 2)
Read access time	t_{AA}		35		45		55	ns	
Chip select access time	t_{ACS}		35		45		55	ns	
Output hold from address change	t_{OH}	5		5		5		ns	
Chip select to output in low-Z	t_{CLZ}	5		5		5		ns	(Note 3)
Chip deselect to output in high-Z	t_{CHZ}	0	15	0	20	0	25	ns	(Note 4)
Write Operation									
Write cycle time	t_{WC}	35		45		55		ns	(Note 2)
Chip select to end of write	t_{CW}	30		40		50		ns	
Address valid to end of write	t_{AW}	30		40		50		ns	
Address setup time	t_{AS}	0		0		0		ns	
Write pulse width	t_{WP}	25		35		45		ns	
Write recovery time	t_{WR}	0		0		0		ns	
Data valid to end of write	t_{DW}	15		20		25		ns	
Data hold time	t_{DH}	0		0		0		ns	
Write enable to output in high-Z	t_{WHZ}	0	15	0	20	0	25	ns	(Note 4)
Output active from end of write	t_{OW}	0		0		0		ns	(Note 3)

Notes:

(1) Input pulse levels = GND to 3.0 V; input pulse rise and fall time = 5 ns; timing reference levels = 1.5 V; see figures 1 and 2 for the output load.

(2) All read and write cycle timings are referenced from the last valid address to the first transitioning address.

(3) The transition is measured ±200 mV from steady-state voltage with the loading shown in figure 2.

(4) The transition is measured at V_{OL} + 200 mV and V_{OH} − 200 mV with the loading shown in figure 2.

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Figure 1. Output Load

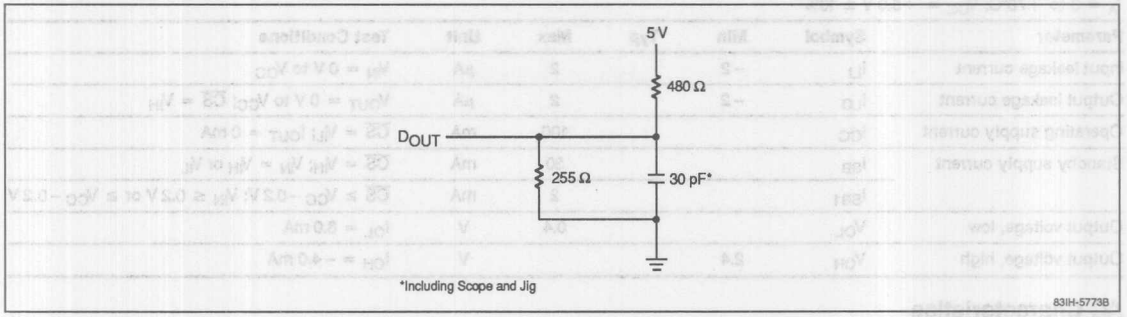
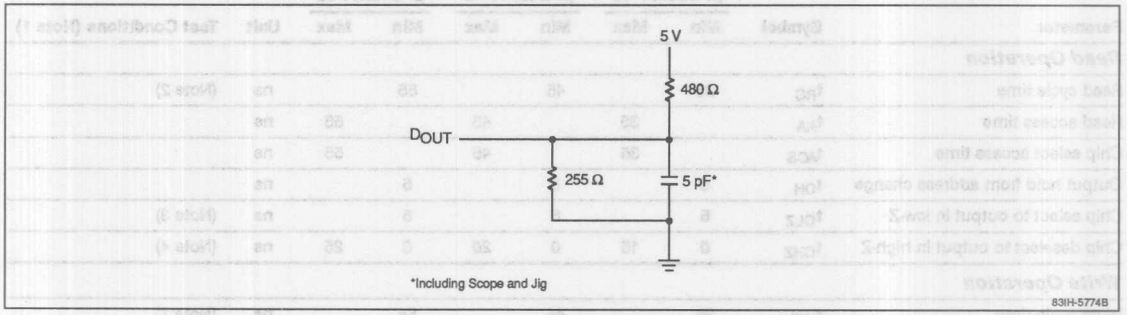
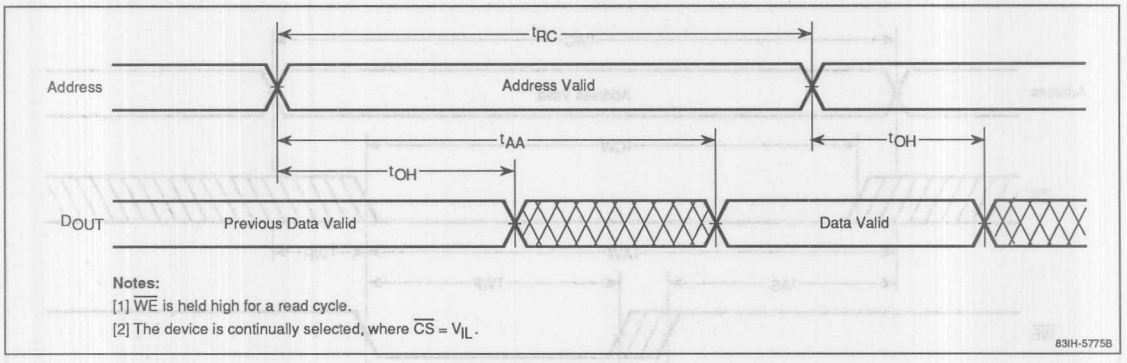


Figure 2. Output Load for t_{CHZ}, t_{CLZ}, t_{OW}, and t_{WHZ}



Timing Waveforms

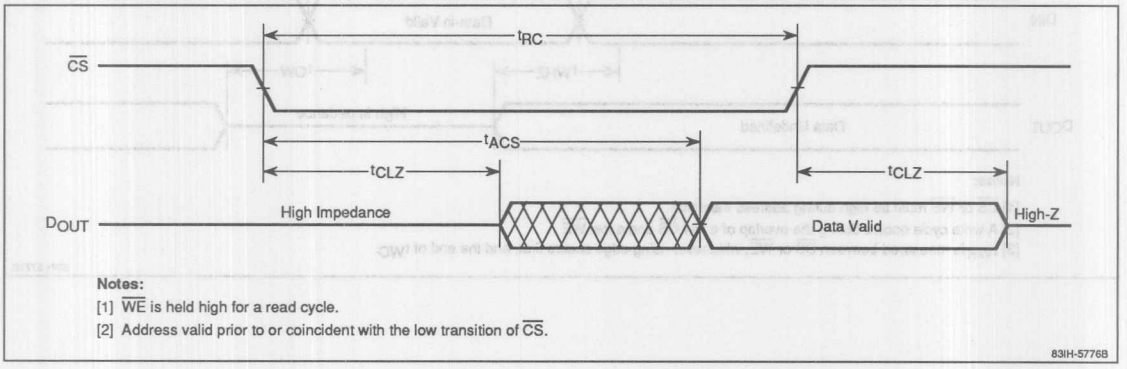
Address Access Cycle



Notes:
[1] $\overline{WE}$ is held high for a read cycle.
[2] The device is continually selected, where $\overline{CS} = V_{IL}$.

83IH-5775B

Chip Select Access Cycle



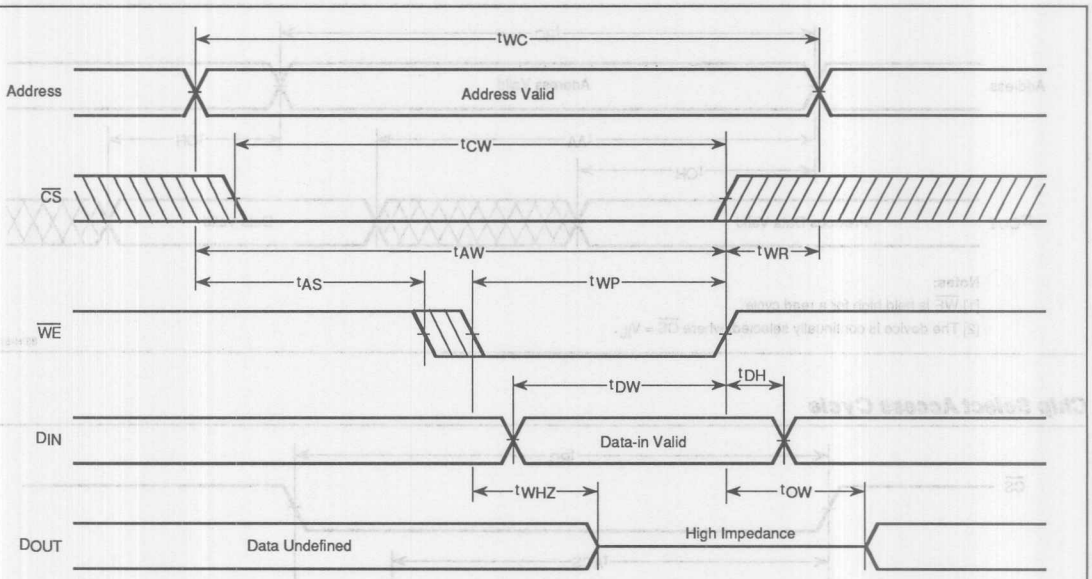
Notes:
[1] $\overline{WE}$ is held high for a read cycle.
[2] Address valid prior to or coincident with the low transition of $\overline{CS}$.

83IH-5776B

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Timing Waveforms (cont)

$\overline{WE}$-Controlled Write Cycle



Notes:

[1] $\overline{CS}$ or $\overline{WE}$ must be high during address transition.

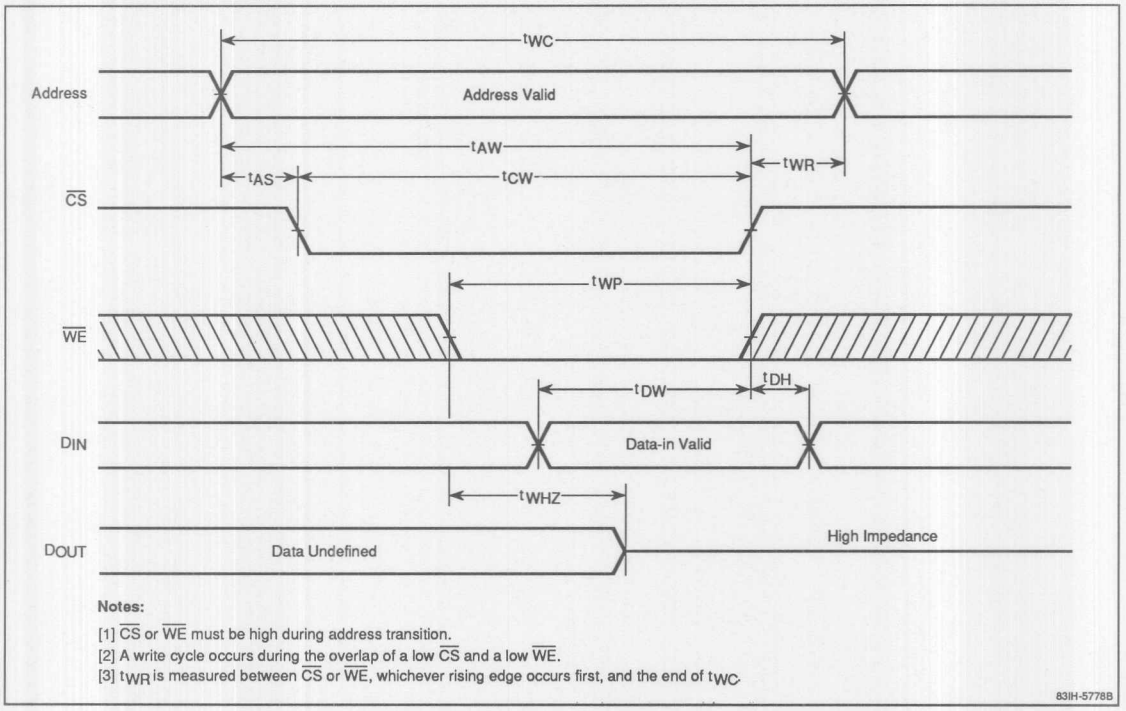
[2] A write cycle occurs during the overlap of a low $\overline{CS}$ and a low $\overline{WE}$.

[3] t_{WR} is measured between $\overline{CS}$ or $\overline{WE}$, whichever rising edge occurs first, and the end of t_{WC}.

83IH-5777B

Timing Waveforms (cont)

$\overline{CS}$-Controlled Write Cycle



Notes:

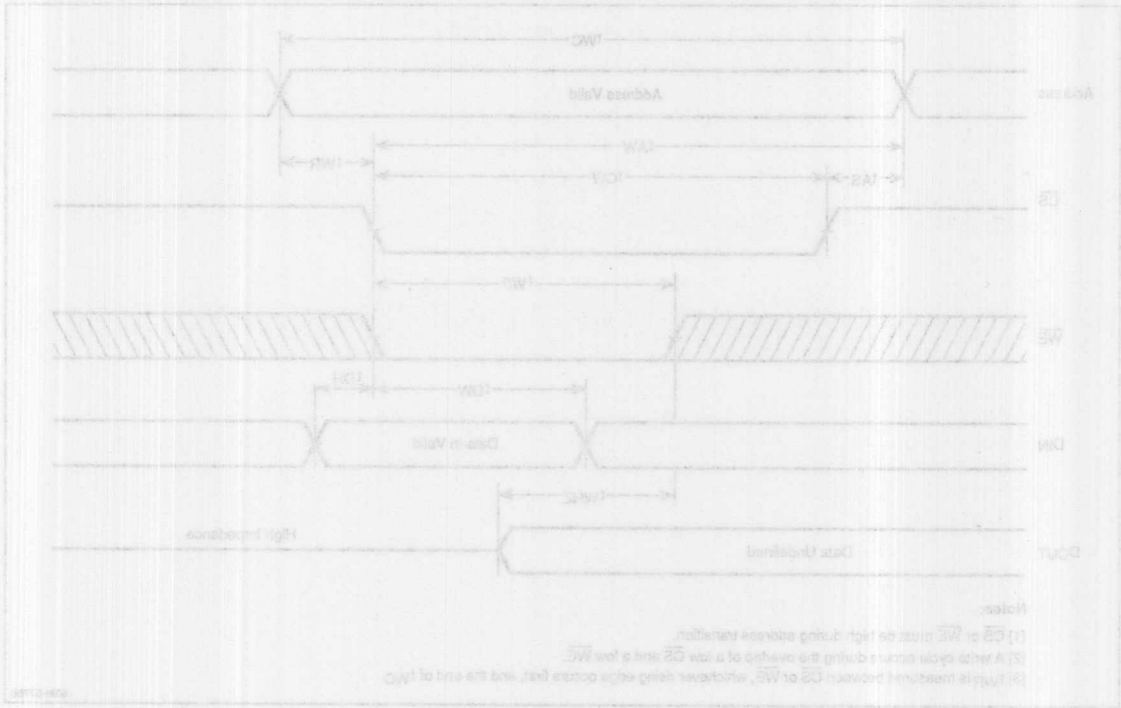
[1] $\overline{CS}$ or $\overline{WE}$ must be high during address transition.

[2] A write cycle occurs during the overlap of a low $\overline{CS}$ and a low $\overline{WE}$.

[3] t_{WR} is measured between $\overline{CS}$ or $\overline{WE}$, whichever rising edge occurs first, and the end of t_{WC}.

83IH-5778B

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μPD46251
262,144 x 1-Bit
Static BiCMOS RAM

Description

The μPD46251 is a 262,144 x 1-bit static RAM featuring a fast access time made possible by ultra-high-speed BiCMOS technology. Fully static operation requires no external clock or refreshing. A chip select ($\overline{CS}$) power down function guarantees low power consumption of 10 mA while the device is in standby.

The μPD46251 is packaged in a 24-pin plastic SOJ.

Features

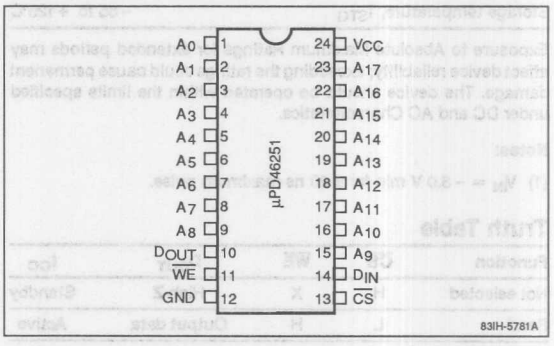
- Fast access times of 20 and 25 ns maximum
- Single +5-volt power supply
- Fully static operation—no clock or refreshing
- TTL-compatible inputs and outputs
- Separated data input and output
- Three-state outputs
- Low power dissipation
  - 140 mA max (active)
  - 10 mA max (standby)
- Standard 24-pin plastic SOJ packaging

Ordering Information

Part Number	Access Time (max)	Package
μPD46251LA-20	20 ns	24-pin plastic SOJ
LA-25	25 ns	

Pin Configuration

24-Pin Plastic SOJ



Pin Identification

Symbol	Function
A_0 - A_{17}	Address inputs
D_{IN}	Data input
D_{OUT}	Data output
$\overline{CS}$	Chip select
$\overline{WE}$	Write enable
GND	Ground
V_{CC}	+5-volt power supply

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Absolute Maximum Ratings

Power supply voltage, V_{CC}	−0.5 to +7.0 V
Input voltage, V_{IN} (Note 1)	−0.5 to +7.0 V
Output voltage, V_{OUT}	−0.5 to +7.0 V
Operating temperature, T_{OPR}	0 to +70°C
Storage temperature, T_{STG}	−55 to +125°C

Exposure to Absolute Maximum Ratings for extended periods may affect device reliability; exceeding the ratings could cause permanent damage. The device should be operated within the limits specified under DC and AC Characteristics.

Notes:

(1) V_{IN} = −3.0 V min for a 20 ns maximum pulse.

Truth Table

Function	$\overline{CS}$	$\overline{WE}$	D_{OUT}	I_{CC}
Not selected	H	X	High-Z	Standby
Read	L	H	Output data	Active
Write	L	L	High-Z	Active

Capacitance

T_A = +25°C; f = 1 MHz (Note 1); V_{IN} and V_{OUT} = 0 V

Parameter	Symbol	Min	Typ	Max	Unit
Input capacitance	C_{IN}			6	pF
Output capacitance	C_{OUT}			8	pF

Notes:

(1) This parameter is sampled and not 100% tested.

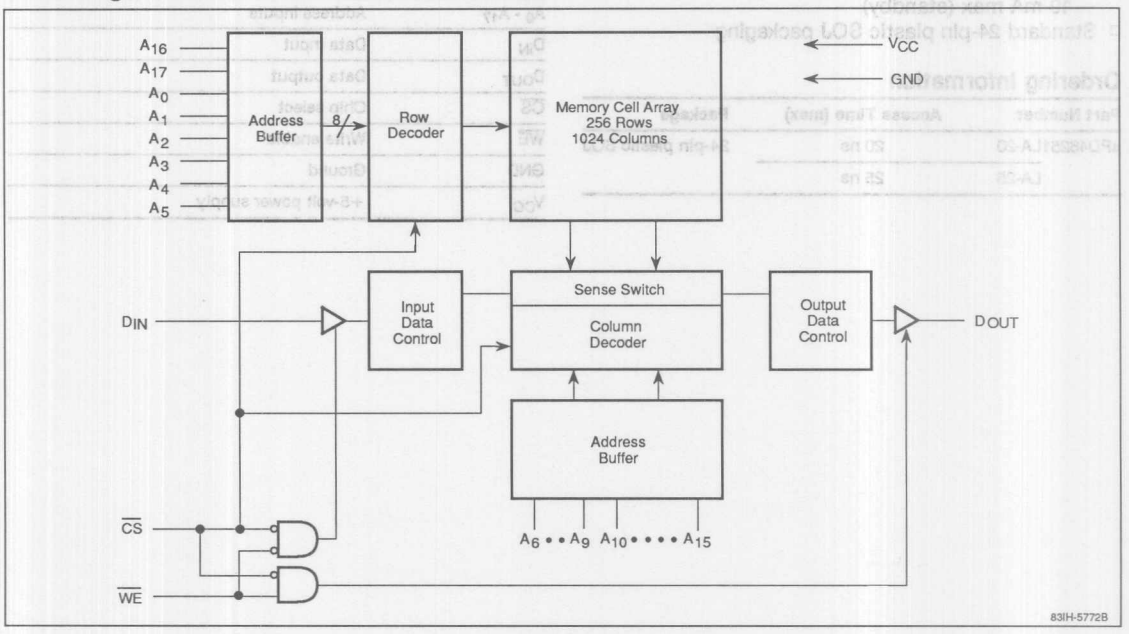
Recommended Operating Conditions

Parameter	Symbol	Min	Typ	Max	Unit
Supply voltage	V_{CC}	4.5	5.0	5.5	V
Input voltage, low	V_{IL}	−0.5		0.8	V
Input voltage, high	V_{IH}	2.2		V_{CC} + 0.3	V
Operating temperatue	T_A	0		70	°C

Notes:

(1) V_{IL} = −3.0 V min for 20 ns maximum pulse.

Block Diagram



DC Characteristics

T_A = 0 to +70°C; V_{CC} = +5.0 V ± 10%

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions
Input leakage current	I_{LI}	−2		2	μA	V_{IN} = 0 V to V_{CC}; V_{CC} = V_{CC} (max)
Output leakage current	I_{LO}	−20		20	μA	V_{OUT} = 0 V to V_{CC}; $\overline{CS}$ = V_{IH}; V_{CC} = V_{CC} (max)
Operating supply current	I_{CC}			140	mA	$\overline{CS}$ = V_{IL}; I_{OUT} = 0 mA
Standby supply current	I_{SB}			40	mA	$\overline{CS}$ = V_{IH}; V_{IN} = V_{IH} or V_{IL}
	I_{SB1}			10	mA	$\overline{CS}$ = V_{CC} − 0.2 V; V_{IN} ≤ 0.2 V or ≥ V_{CC} − 0.2 V
Output voltage, low	V_{OL}			0.4	V	I_{OL} = 8.0 mA
Output voltage, high	V_{OH}	2.4			V	I_{OH} = −4.0 mA

AC Characteristics

T_A = 0 to +70°C; V_{CC} = +5.0 V ± 10%

		μPD46251-20		μPD46251-25			
Parameter	Symbol	Min	Max	Min	Max	Unit	Test Conditions (Note 1)
Read Operation							
Read cycle time	t_{RC}	20		25		ns	(Note 2)
Address access time	t_{AA}		20		25	ns	
Chip select access time	t_{ACS}		20		25	ns	
Output hold from address change	t_{OH}	3		3		ns	
Chip select to output in low-Z	t_{CLZ}	3		3		ns	(Note 3)
Chip deselect to output in high-Z	t_{CHZ}	0	10	0	13	ns	(Note 4)
Write Operation							
Write cycle time	t_{WC}	20		25		ns	(Note 2)
Chip select to end of write	t_{CW}	17		20		ns	
Address valid to end of write	t_{AW}	17		20		ns	
Address setup time	t_{AS}	0		0		ns	
Write pulse width	t_{WP}	17		20		ns	
Write recovery time	t_{WR}	3		3		ns	
Data valid to end of write	t_{DW}	12		15		ns	
Data hold time	t_{DH}	0		0		ns	
Write enable to output in high-Z	t_{WHZ}	0	10	0	13	ns	(Note 4)
Output active from end of write	t_{OW}	0		0		ns	(Note 3)

Notes:

(1) Input pulse levels = GND to 3.0 V; input pulse rise and fall time = 3 ns; timing reference levels = 1.5 V; see figures 1 and 2 for the output load.

(2) All read and write cycle timings are referenced from the last valid address to the first transitioning address.

(3) The transition is measured ±200 mV from steady-state voltage with the loading shown in figure 2.

(4) The transition is measured at V_{OL} + 200 mV and V_{OH} − 200 mV with the loading shown in figure 2.

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Figure 1. Output Load

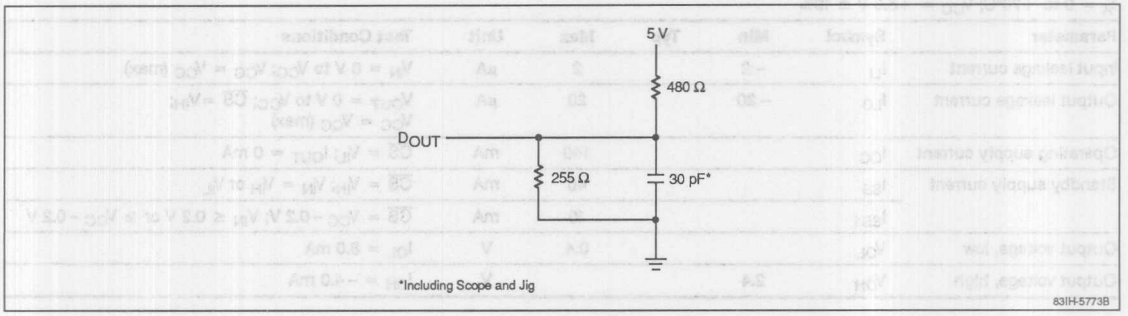
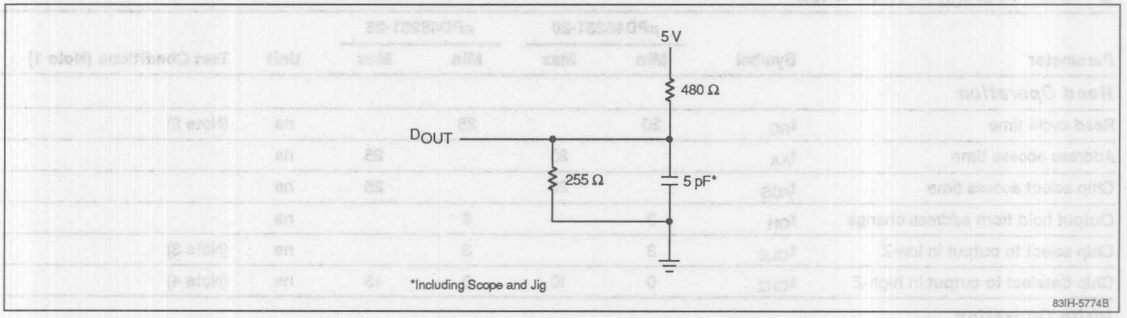
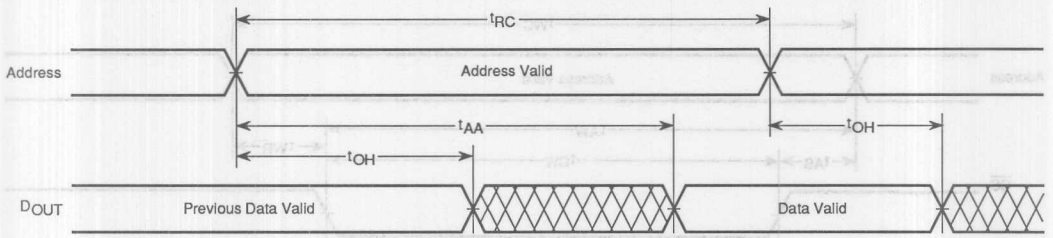


Figure 2. Output Load for t_{CHZ}, t_{CLZ}, t_{OW}, and t_{WHZ}



Timing Waveforms

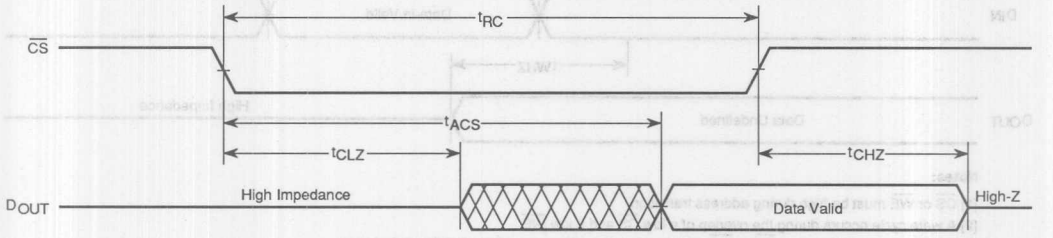
Address Access Cycle



Notes:
[1] $\overline{WE}$ is held high for a read cycle.
[2] The device is continually selected, where $\overline{CS} = V_{IL}$.

83IH-5775B

Chip Select Access Cycle



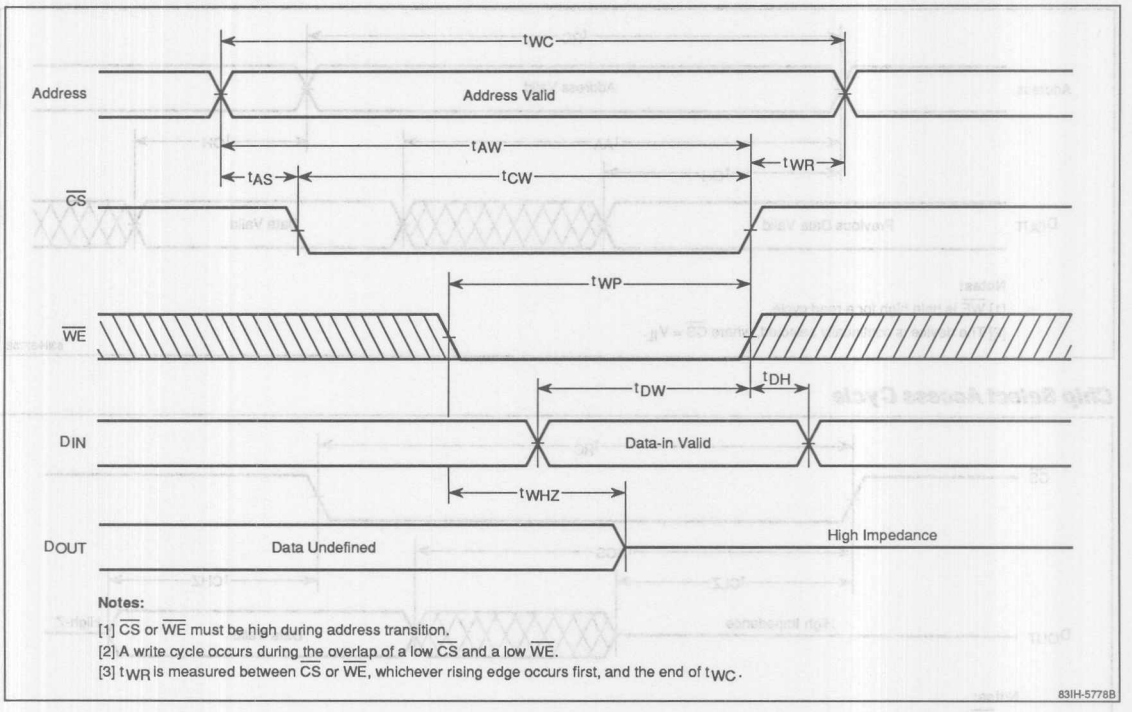
Notes:
[1] $\overline{WE}$ is held high for a read cycle.
[2] Address valid prior to or coincident with the low transition of $\overline{CS}$.

83IH-5776B

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Timing Waveforms (cont)

$\overline{WE}$-Controlled Write Cycle



Notes:

[1] $\overline{CS}$ or $\overline{WE}$ must be high during address transition.

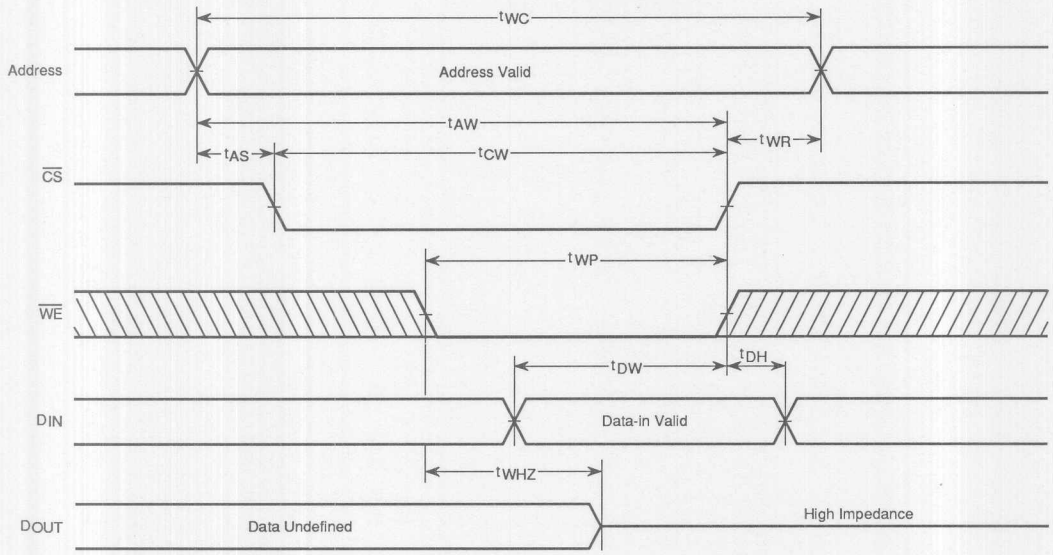
[2] A write cycle occurs during the overlap of a low $\overline{CS}$ and a low $\overline{WE}$.

[3] t_{WR} is measured between $\overline{CS}$ or $\overline{WE}$, whichever rising edge occurs first, and the end of t_{WC}.

83IH-5778B

Timing Waveforms (cont)

$\overline{CS}$-Controlled Write Cycle



Notes:

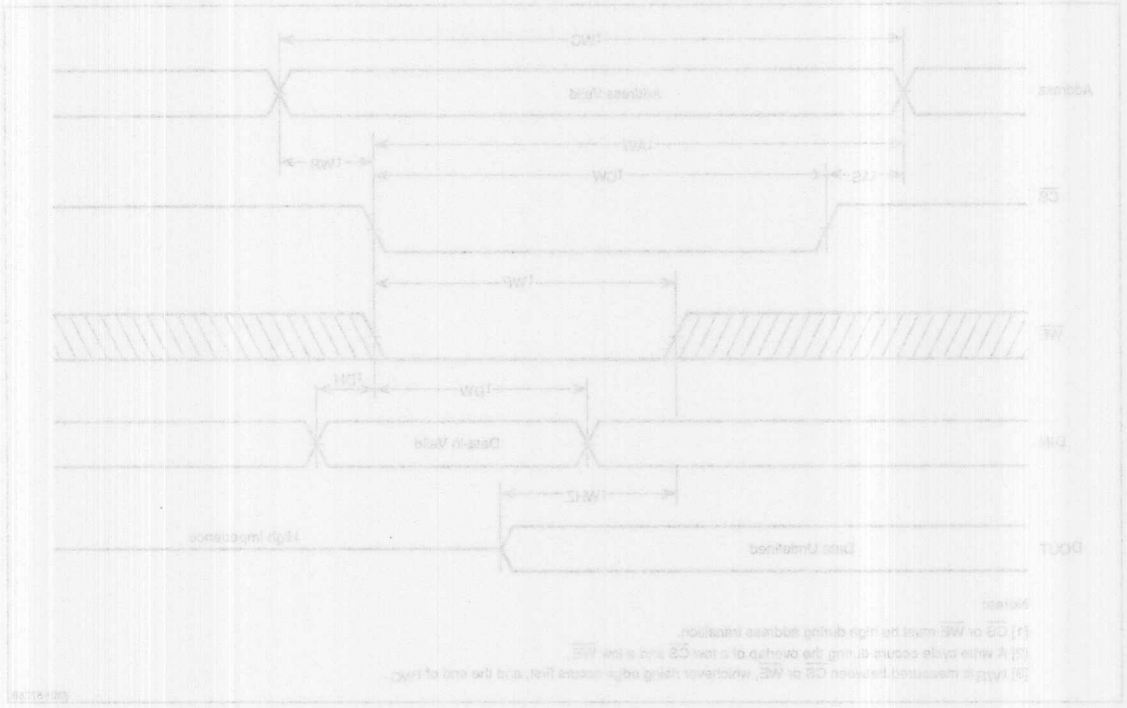
[1] $\overline{CS}$ or $\overline{WE}$ must be high during address transition.

[2] A write cycle occurs during the overlap of a low $\overline{CS}$ and a low $\overline{WE}$.

[3] t_{WR} is measured between $\overline{CS}$ or $\overline{WE}$, whichever rising edge occurs first, and the end of t_{WC}.

83IH-5778B

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Description

The μPD43254 is a 65,536-word by 4-bit static RAM fabricated with advanced silicon-gate technology. CMOS peripheral circuits and N-channel memory cells with polysilicon resistors make the μPD43254 a high-speed device that requires very low power and no clock or refreshing.

The μPD43254 is available in standard 24-pin plastic DIP and SOJ packaging.

Features

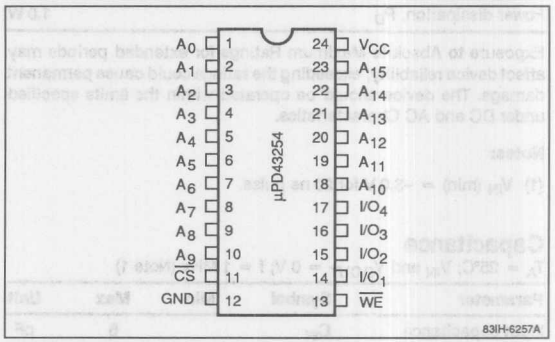
- 65,536-word x 4-bit organization
- Single + 5-volt power supply
- Fully static operation—no clock or refreshing
- TTL-compatible inputs and outputs
- Common I/O capability
- Low power dissipation
  - —120 mA max (active)
  - —2 mA max (standby)
- Standard 24-pin plastic DIP and SOJ packaging

Ordering Information

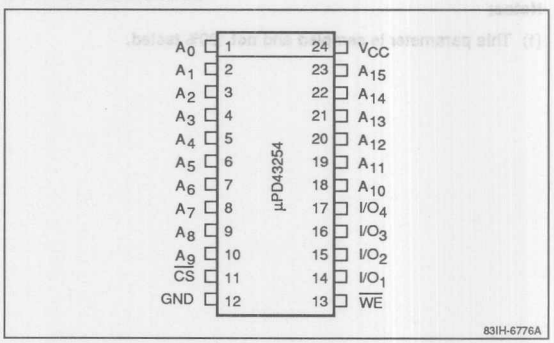
Part Number	Access Time (max)	Package
μPD43254C-35	35 ns	24-pin plastic DIP
C-45	45 ns	
C-55	55 ns	
μPD43254LA-35	35 ns	24-pin plastic SOJ
LA-45	45 ns	
LA-55	55 ns	

Pin Configurations

24-Pin Plastic DIP



24-Pin Plastic SOJ



Pin Identification

Symbol	Function
A_0 - A_{15}	Address inputs
I/O_1 - I/O_4	Data inputs and outputs
$\overline{CS}$	Chip select
$\overline{WE}$	Write enable
GND	Ground
V_{CC}	+5-volt power supply

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Absolute Maximum Ratings

Supply voltage, V_{CC}	−0.5 to +7.0 V
Input and output voltages, V_{IN} (Note 1)	−0.5 to +7.0 V
Operating temperature, T_{OPR}	0 to +70°C
Storage temperature, T_{STG}	−55 to +125°C
Power dissipation, P_D	1.0 W

Exposure to Absolute Maximum Ratings for extended periods may affect device reliability; exceeding the ratings could cause permanent damage. The device should be operated within the limits specified under DC and AC Characteristics.

Notes:

(1) V_{IN} (min) = −3.0 V for 20 ns pulse.

Capacitance

T_A = 25°C; V_{IN} and V_{DOUT} = 0 V; f = 1 MHz (Note 1)

Parameter	Symbol	Min	Max	Unit
Input capacitance	C_{IN}		6	pF
Output capacitance	C_{DOUT}		8	pF

Notes:

(1) This parameter is sampled and not 100% tested.

Recommended Operating Conditions

Parameter	Symbol	Min	Typ	Max	Unit
Supply voltage	V_{CC}	4.5	5.0	5.5	V
Input voltage, high	V_{IH}	2.2		V_{CC} + 0.3	V
Input voltage, low	V_{IL}	−0.5		0.8	V
Operating temperature	T_A	0		70	°C

Notes:

(1) V_{IL} = −3.0 V for 20 ns pulse.

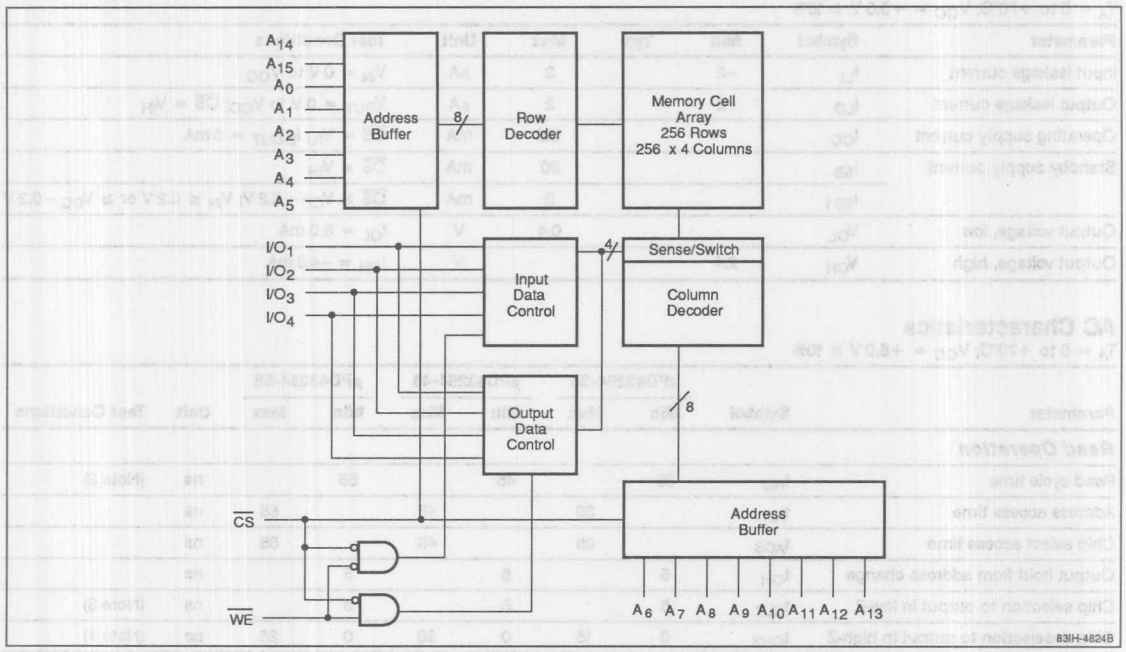
Truth Table

Function	$\overline{CS}$	$\overline{WE}$	Input/Output	I_{CC}
Not selected	H	X	High-Z	Standby
Read	L	H	D_{OUT}	Active
Write	L	L	D_{IN}	Active

Notes:

(1) X = don't care.

Block Diagram



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DC Characteristics

T_A = 0 to +70°C; V_{CC} = +5.0 V ± 10%

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions
Input leakage current	I_{LI}	−2		2	μA	V_{IN} = 0 V to V_{CC}
Output leakage current	I_{LO}	−2		2	μA	V_{OUT} = 0 V to V_{CC}; $\overline{CS}$ = V_{IH}
Operating supply current	I_{CC}			120	mA	$\overline{CS}$ = V_{IL}; I_{DOUT} = 0 mA
Standby supply current	I_{SB}			30	mA	$\overline{CS}$ = V_{IH}
	I_{SB1}			2	mA	$\overline{CS}$ ≥ V_{CC} − 0.2 V; V_{IN} ≤ 0.2 V or ≥ V_{CC} − 0.2 V
Output voltage, low	V_{OL}			0.4	V	I_{OL} = 8.0 mA
Output voltage, high	V_{OH}	2.4			V	I_{OH} = −4.0 mA

AC Characteristics

T_A = 0 to +70°C; V_{CC} = +5.0 V ± 10%

		μPD43254-35		μPD43254-45		μPD43254-55			
Parameter	Symbol	Min	Max	Min	Max	Min	Max	Unit	Test Conditions
Read Operation									
Read cycle time	t_{RC}	35		45		55		ns	(Note 2)
Address access time	t_{AA}		35		45		55	ns	
Chip select access time	t_{ACS}		35		45		55	ns	
Output hold from address change	t_{OH}	5		5		5		ns	
Chip selection to output in low-Z	t_{CLZ}	5		5		5		ns	(Note 3)
Chip deselection to output in high-Z	t_{CHZ}	0	15	0	20	0	25	ns	(Note 4)
Write Operation									
Write cycle time	t_{WC}	35		45		55		ns	(Note 2)
Chip select to end of write	t_{CW}	30		40		50		ns	
Address valid to end of write	t_{AW}	30		40		50		ns	
Address setup time	t_{AS}	0		0		0		ns	
Write pulse width	t_{WP}	30		40		50		ns	
Write recovery time	t_{WR}	0		0		0		ns	
Data valid to end of write	t_{DW}	15		20		25		ns	
Data hold time	t_{DH}	0		0		0		ns	
Write enable to output in high-Z	t_{WHZ}	0	15	0	20	0	25	ns	(Note 4)
Output active from end of write	t_{OW}	0		0		0		ns	(Note 3)

Notes:

(1) Input pulse levels = GND to 3.0 V; input pulse rise and fall times = 5 ns; timing reference levels = 1.5 V; see figures 1 and 2 for output load.

(2) All read cycle timings are referenced from the last valid address to the first transitioning address.

(3) Transition is measured at ±200 mV from steady-state voltage with the load shown in figure 2.

(4) Transition is measured at V_{OL} + 200 mV and V_{OH} − 200 mV with the load shown in figure 2.

Figure 1. Output Load

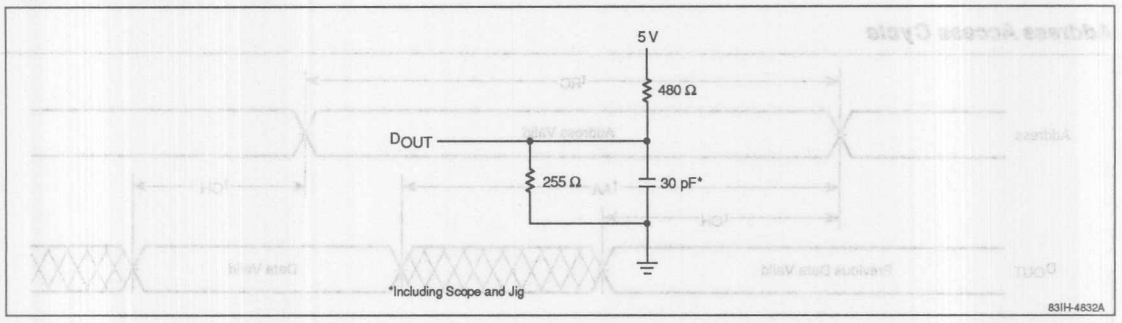
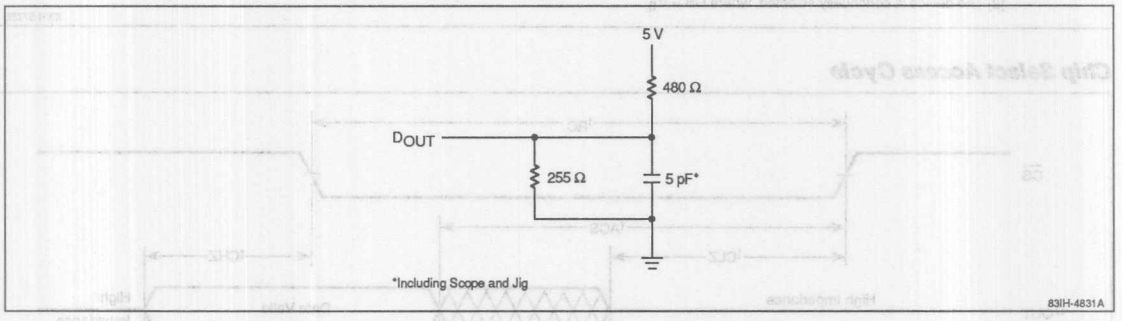


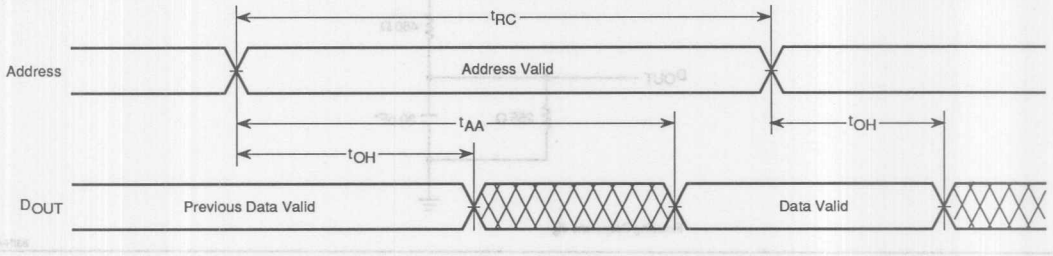
Figure 2. Output Load for t_{CHZ}, t_{CLZ}, t_{WHZ}, and t_{OW}



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Timing Waveforms

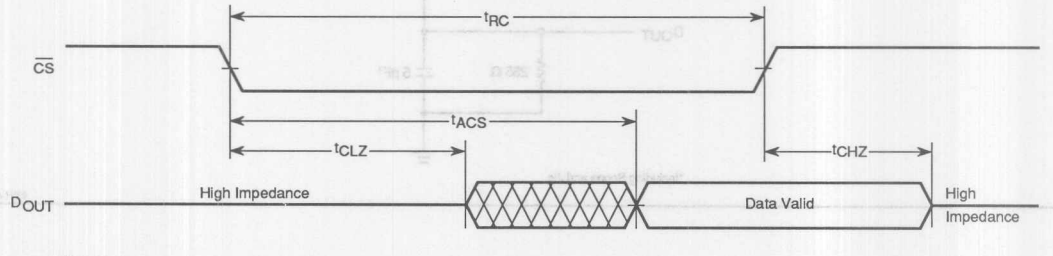
Address Access Cycle



Notes:
[1] $\overline{WE}$ is held high for a read cycle.
[2] The device is continually selected, where $\overline{CS} = V_{IL}$.

83IH-5775B

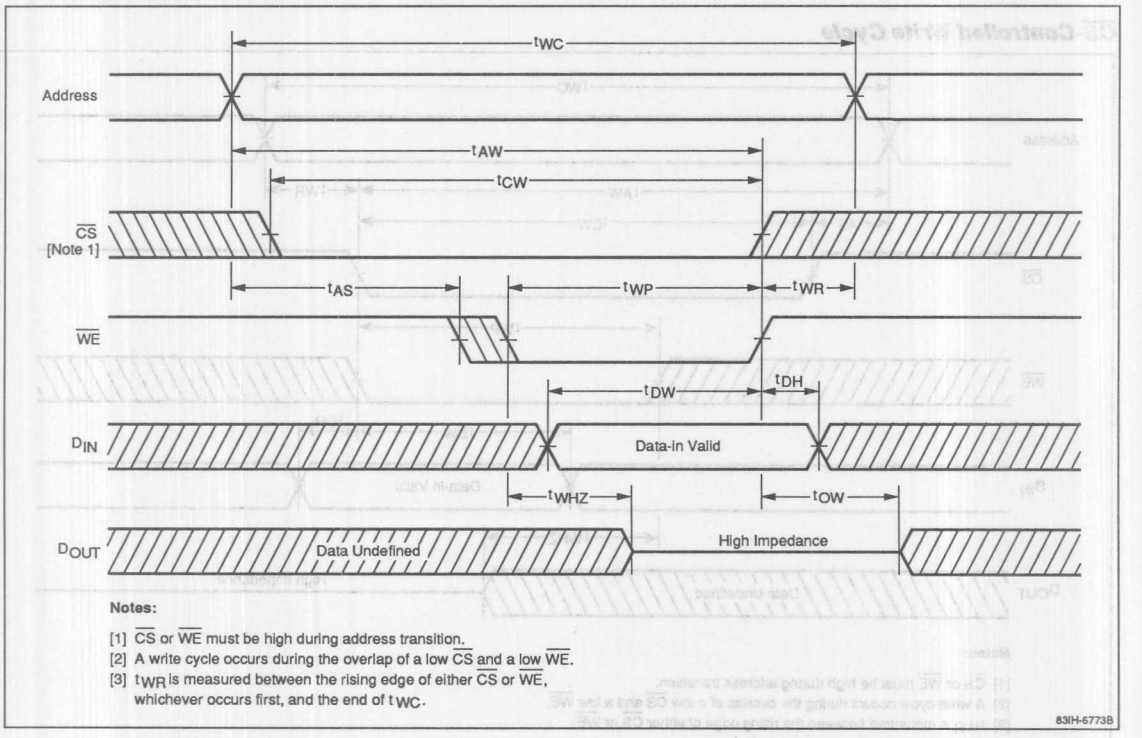
Chip Select Access Cycle



Notes:
[1] $\overline{WE}$ is held high for a read cycle.
[2] Address valid prior to or coincident with the low transition of $\overline{CS}$.

83IH-6772B

$\overline{WE}$-Controlled Write Cycle



Notes:

[1] $\overline{CS}$ or $\overline{WE}$ must be high during address transition.

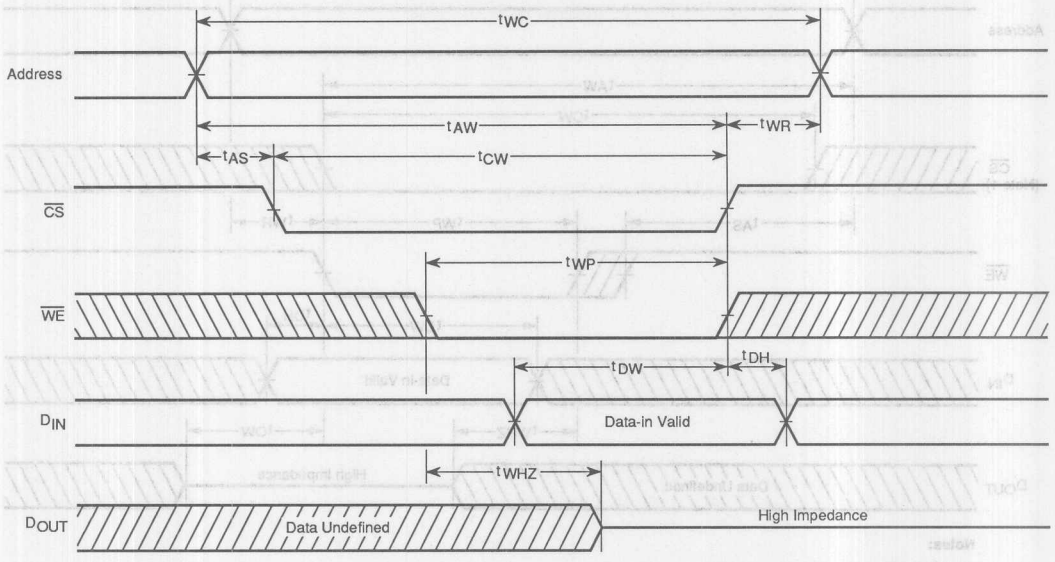
[2] A write cycle occurs during the overlap of a low $\overline{CS}$ and a low $\overline{WE}$.

[3] t_{WR} is measured between the rising edge of either $\overline{CS}$ or $\overline{WE}$, whichever occurs first, and the end of t_{WC}.

7

Timing Waveforms (cont)

$\overline{CS}$-Controlled Write Cycle



Notes:

[1] $\overline{CS}$ or $\overline{WE}$ must be high during address transition.
[2] A write cycle occurs during the overlap of a low $\overline{CS}$ and a low $\overline{WE}$.
[3] t_{WR} is measured between the rising edge of either $\overline{CS}$ or $\overline{WE}$, whichever occurs first, and the end of t_{WC}.

83IH-6774B

μPD43256A
32,768 x 8-Bit
Static CMOS RAM

Description

The μPD43256A is a 32,768-word by 8-bit static RAM fabricated with advanced silicon-gate technology. Its unique design uses CMOS peripheral circuits and N-channel memory cells with polysilicon resistors to make the μPD43256A a high-speed device that requires very low power and no clock or refreshing.

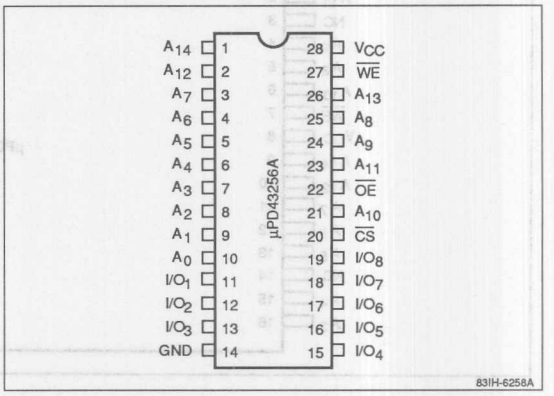
Minimum standby power is drawn when $\overline{CS}$ is high, independent of the other inputs' levels. Data retention is guaranteed at a power supply voltage as low as 2 V. The μPD43256A is available in standard 28-pin plastic DIP, 28-pin plastic miniflat, or 32-pin plastic TSOP packaging.

Features

- Single +5-volt power supply
- Fully static operation—no clock or refreshing required
- TTL-compatible inputs and outputs
- Common I/O using three-state outputs
- One $\overline{CS}$ pin and one $\overline{OE}$ pin for easy application
- Data retention of 2 V minimum
- Standard 28-pin plastic DIP and miniflat packaging
- Standard 32-pin plastic TSOP packaging (with either normal or reverse bent leads)

Pin Configurations

28-Pin Plastic DIP or Miniflat



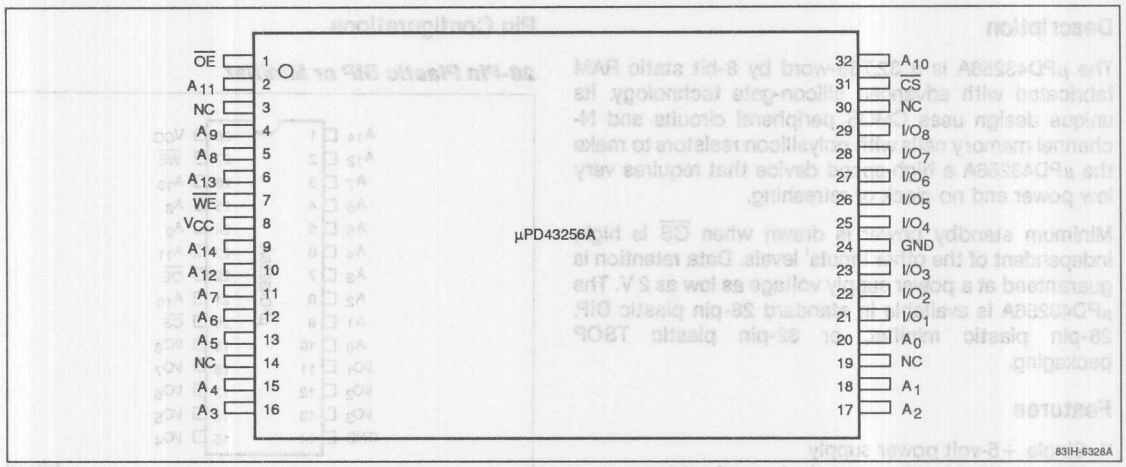
Pin Identification

Symbol	Function
A_0 - A_{14}	Address inputs
I/O_1 - I/O_8	Data inputs and outputs
$\overline{CS}$	Chip select
$\overline{OE}$	Output enable
$\overline{WE}$	Write enable
GND	Ground
V_{CC}	+5-volt power supply
NC	No connection

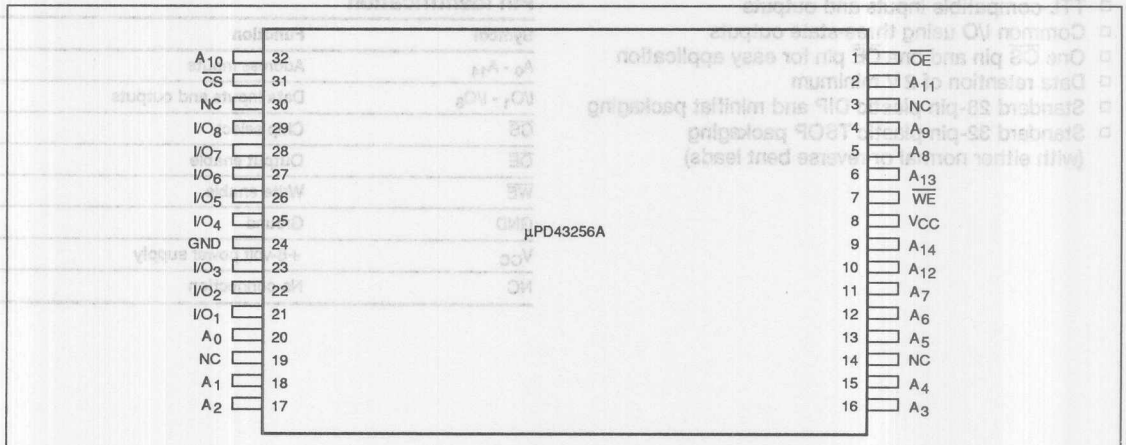
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Pin Configurations (cont)

32-Pin Plastic TSOP (normal leads, top view)



32-Pin Plastic TSOP (reverse bent leads, bottom view)



Notes:

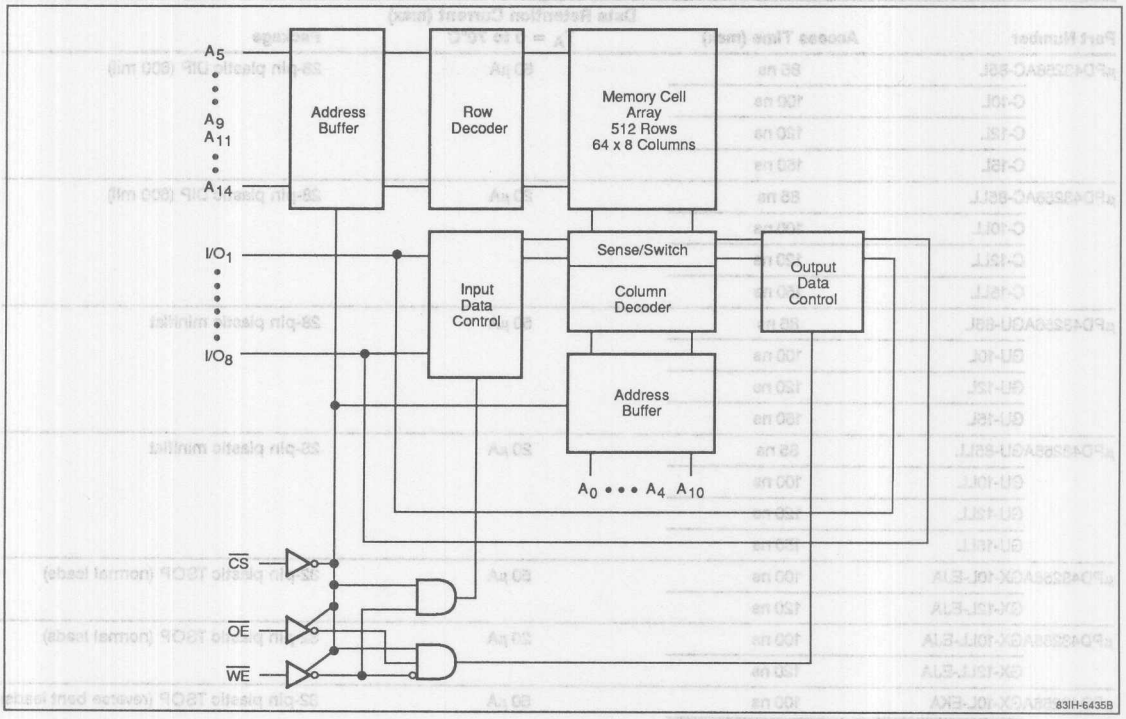
[1] This package is designed to be mounted with the top of the package closest to the mounting surface. In this position, the exposed side will be the bottom of the package.

Ordering Information

Part Number	Access Time (max)	Data Retention Current (max) T_A = 0 to 70°C	Package
μPD43256AC-85L	85 ns	50 μA	28-pin plastic DIP (600 mil)
C-10L	100 ns		
C-12L	120 ns		
C-15L	150 ns		
μPD43256AC-85LL	85 ns	20 μA	28-pin plastic DIP (600 mil)
C-10LL	100 ns		
C-12LL	120 ns		
C-15LL	150 ns		
μPD43256AGU-85L	85 ns	50 μA	28-pin plastic miniflat
GU-10L	100 ns		
GU-12L	120 ns		
GU-15L	150 ns		
μPD43256AGU-85LL	85 ns	20 μA	28-pin plastic miniflat
GU-10LL	100 ns		
GU-12LL	120 ns		
GU-15LL	150 ns		
μPD43256AGX-10L-EJA	100 ns	50 μA	32-pin plastic TSOP (normal leads)
GX-12L-EJA	120 ns		
μPD43256AGX-10LL-EJA	100 ns	20 μA	32-pin plastic TSOP (normal leads)
GX-12LL-EJA	120 ns		
μPD43256AGX-10L-EKA	100 ns	50 μA	32-pin plastic TSOP (reverse bent leads)
GX-12L-EKA	120 ns		
μPD43256AGX-10LL-EKA	100 ns	20 μA	32-pin plastic TSOP (reverse bent leads)
GX-12LL-EKA	120 ns		

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Block Diagram



Absolute Maximum Ratings

Supply voltage, V_{CC} (Note 1)	−0.5 to +7.0 V
Input voltage, V_{IN} (Note 1)	−0.5 to V_{CC} + 0.5 V
Output voltage, $V_{I/O}$ (Note 1)	−0.5 to V_{CC} + 0.5 V
Operating temperature, T_{OPR}	0 to +70°C
Storage temperature, T_{STG}	−55 to +125°C
Power dissipation, P_D	1.0 W

Exposure to Absolute Maximum Ratings for extended periods may affect device reliability; exceeding the ratings could cause permanent damage. The device should be operated within the limits specified under DC and AC Characteristics.

Notes:

(1) −3.0 V minimum (pulse width = 50 ns).

Capacitance

T_A = +25°C; f = 1 MHz; V_{IN} and V_{OUT} = 0 V

Parameter	Symbol	Min	Max	Unit
Input capacitance	C_I		5	pF
Input/output capacitance	$C_{I/O}$		8	pF

Notes:

(1) This parameter is sampled and not 100% tested.

Truth Table

$\overline{CS}$	$\overline{OE}$	$\overline{WE}$	Function	I/O	I_{CC}
H	X	X	Not selected	High-Z	Standby
L	H	H	Not selected	High-Z	Active
L	L	H	Read	D_{OUT}	Active
L	X	L	Write	D_{IN}	Active

Notes:

(1) X = don't care.

Recommended Operating Conditions

Parameter	Symbol	Min	Typ	Max	Unit
Supply voltage	V_{CC}	4.5	5.0	5.5	V
Input voltage, low (Note 1)	V_{IL}	−0.3		0.8	V
Input voltage, high	V_{IH}	2.2		V_{CC} + 0.5	V
Ambient temperature	T_A	0		70	°C

Notes:

(1) −3.0 V minimum (pulse width = 50 ns).

DC Characteristics

T_A = 0 to +70°C; V_{CC} = +5.0 V ± 10%

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions
Input leakage current	I_{LI}	−1		1	μA	V_{IN} = 0 V to V_{CC}
I/O leakage current	I_{LO}	−1		1	μA	$V_{I/O}$ = 0 V to V_{CC}; $\overline{CS} \geq V_{IH}$ or $\overline{OE} \geq V_{IH}$ or $\overline{WE} \leq V_{IL}$
Operating supply current	I_{CCA1}			45	mA	$\overline{CS} \leq V_{IL}$ (min cycle); $I_{I/O}$ = 0 V (Note 1)
	I_{CCA2}			10	mA	$\overline{CS}$ = V_{IL}; $I_{I/O}$ = 0 V
	I_{CCA3}			10	mA	$\overline{CS} \leq 0.2$ V; f = 1 MHz; $I_{I/O}$ = 0 V; $V_{IL} \leq 0.2$ V; $V_{IH} \geq V_{CC} - 0.2$ V
Standby supply current	I_{SB}			3	ma	$\overline{CS} \geq V_{IH}$
	I_{SB1}		0.002	0.1	mA	$\overline{CS} \geq V_{CC} - 0.2$ V (Note 2)
Output voltage, low	V_{OL}			0.4	V	I_{OL} = 2.1 mA
Output voltage, high	V_{OH1}	2.4			V	I_{OH} = −1.0 mA
	V_{OH2}	V_{CC} − 0.5			V	I_{OH} = −0.1 mA

Notes:

(1) μPD43256A-10L/-10LL/-12L/-12LL = 40 mA (max).
μPD43256A-15L/-15LL = 35 mA (max).

(2) μPD43256AGX-10LL/-12LL = 50 μA (max).

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AC Characteristics (for L and LL Versions)

T_A = 0 to +70°C; V_{CC} = +5.0 V ± 10%

Parameter	Symbol	μPD43256A-85		μPD43256A-10		μPD43256A-12		μPD43256A-15		Unit	Test Conditions
		Min	Max	Min	Max	Min	Max	Min	Max		
Read Operation											
Read cycle time	t_{RC}	85		100		120		150		ns	
Address access time	t_{AA}		85		100		120		150	ns	(Note 2)
Chip select access time	t_{ACS}		85		100		120		150	ns	(Note 2)
Output enable to output valid	t_{OE}		40		50		60		70	ns	(Note 2)
Output hold from address change	t_{OH}	10		10		10		10		ns	
Chip select to output in low-Z	t_{CLZ}	10		10		10		10		ns	(Note 3)
Output enable to output in low-Z	t_{OLZ}	5		5		5		5		ns	(Note 3)
Chip select to output in high-Z	t_{CHZ}		30		35		40		50	ns	(Note 3)
Output enable to output in high-Z	t_{OHZ}		30		35		40		50	ns	(Note 3)
Write Operation											
Write cycle time	t_{WC}	85		100		120		150		ns	
Chip select to end of write	t_{CW}	70		80		85		100		ns	
Address valid to end of write	t_{AW}	70		80		85		100		ns	
Address setup time	t_{AS}	0		0		0		0		ns	
Write pulse width	t_{WP}	65		70		70		90		ns	
Write recovery time	t_{WR}	5		5		5		5		ns	
Data valid to end of write	t_{DW}	35		40		50		60		ns	
Data hold time	t_{DH}	0		0		0		0		ns	
Write enable to output in high-Z	t_{WHZ}		30		35		40		50	ns	(Note 3)
Output active from end of write	t_{OW}	10		10		10		10		ns	(Note 3)

Notes:

(1) Input pulse levels = 0.8 to 2.2 V; input pulse rise and fall times = 5 ns; timing reference levels = 1.5 V.

(2) See figure 1 for output load.

(3) See figure 2 for output load.

Low V_{CC} Data Retention Characteristics

T_A = 0 to 70°C

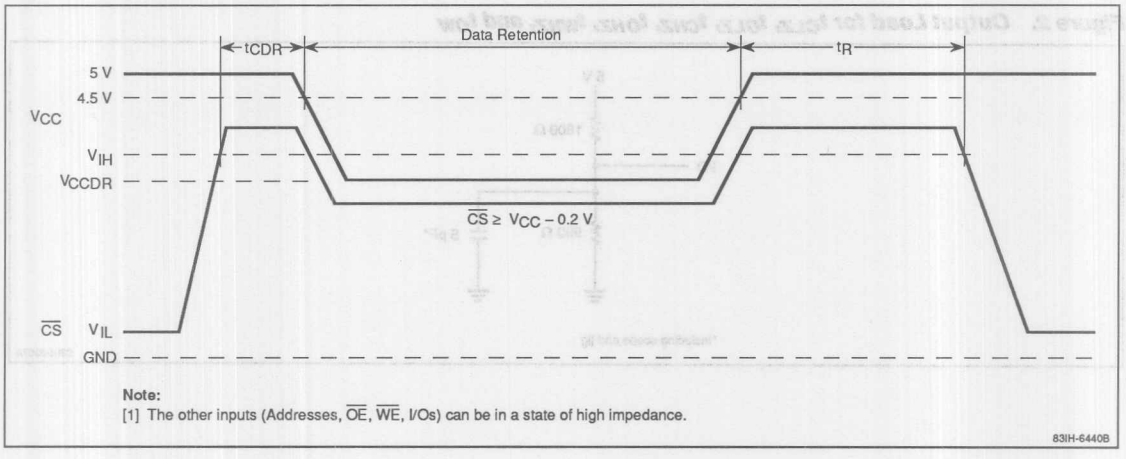
Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions
Data retention supply voltage	V_{CCDR}	2.0		5.5	V	$\overline{CS} \geq V_{CC} - 0.2$ V
Data retention supply current	I_{CCDR}		1	50	μA	V_{CC} = 3.0 V; $\overline{CS} \geq V_{CC} - 0.2$ V (Notes 1, 2)
Chip deselection to data retention	t_{CDR}	0			ns	
Operation recovery time	t_R	t_{RC}			ns	

Notes:

(1) For μPD43256A-LL, I_{CCDR} = 20 μA (max) at T_A = 0 to 70°C and 3 μA (max) at T_A = 0 to 40°C.

(2) For μPD43256A-L, I_{CCDR} = 15 μA (max) at T_A = 0 to 40°C.

Data Retention Timing



Note:
[1] The other inputs (Addresses, $\overline{OE}$, $\overline{WE}$, I/Os) can be in a state of high impedance.

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Figure 1. Output Load

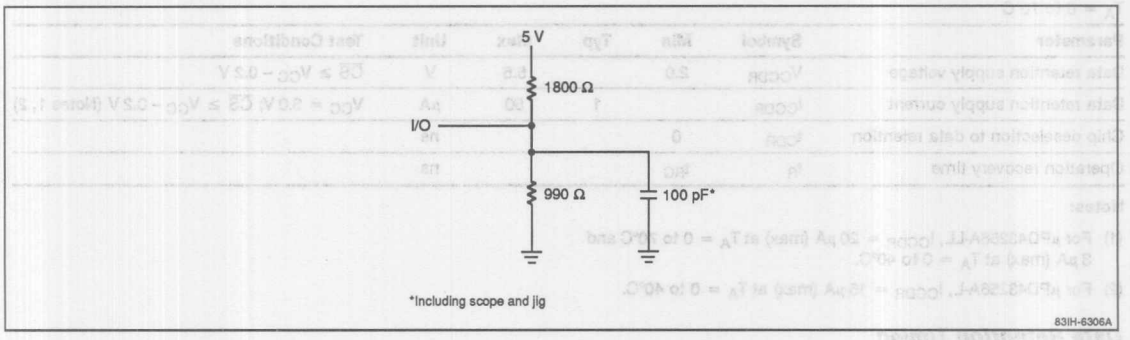
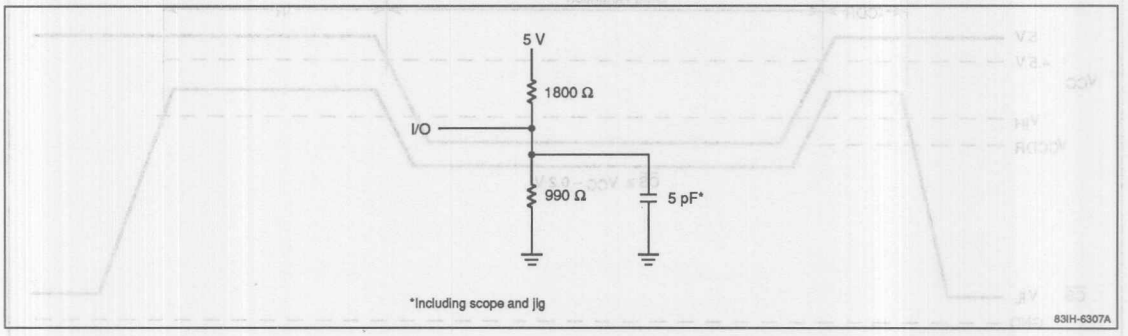
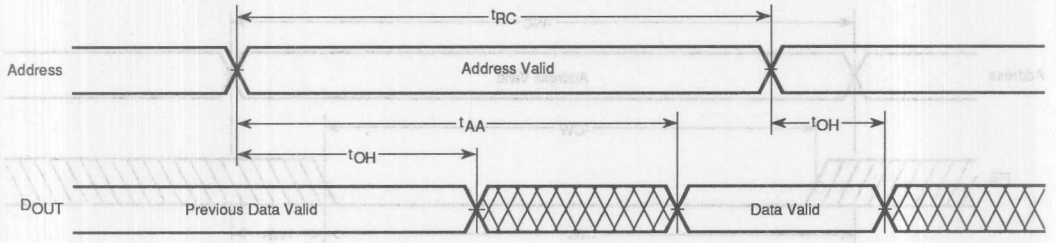


Figure 2. Output Load for t_{CLZ}, t_{OLZ}, t_{CHZ}, t_{OHZ}, t_{WHZ}, and t_{OW}



Timing Waveforms

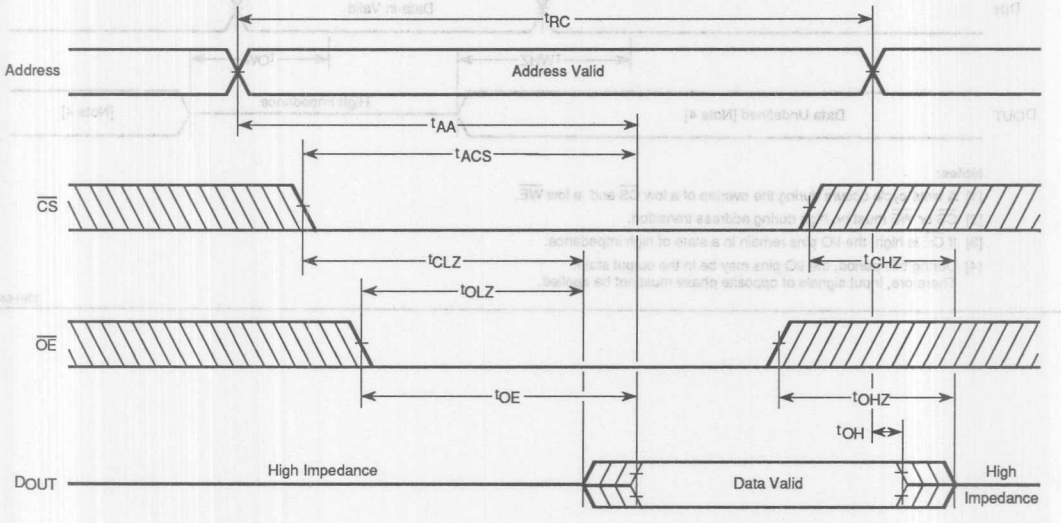
Address Access Cycle



Notes:
[1] $\overline{WE}$ is held high for a read cycle.
[2] The device is continually selected, where $\overline{CS} = \overline{OE} = V_{IL}$.

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Chip Select Access Cycle



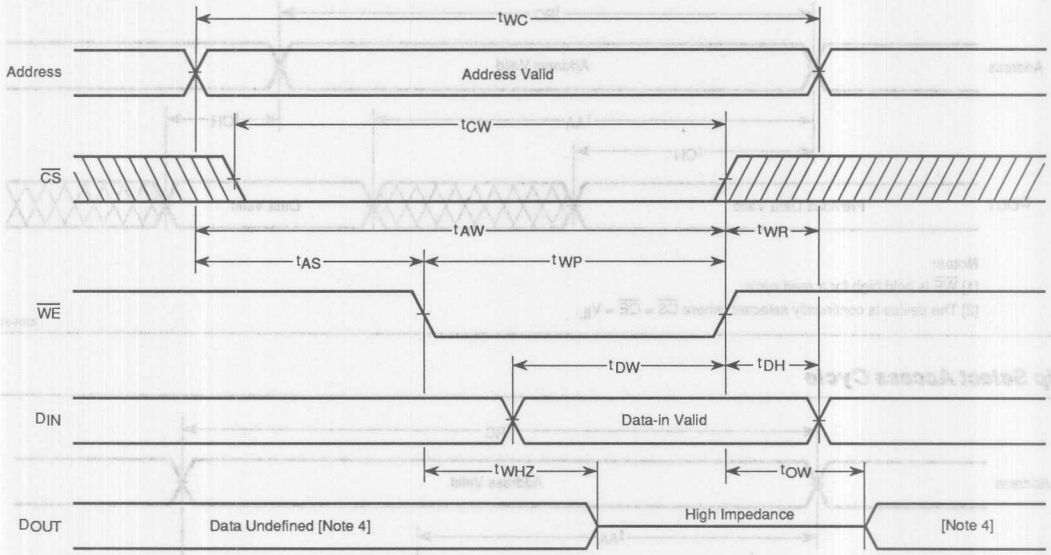
Notes:
[1] $\overline{WE}$ is high for a read cycle.
[2] Address valid prior to or coincident with the low transition of $\overline{CS}$.

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Timing Waveforms (cont)

$\overline{WE}$-Controlled Write Cycle



Notes:

[1] A write cycle occurs during the overlap of a low $\overline{CS}$ and a low $\overline{WE}$.

[2] $\overline{CS}$ or $\overline{WE}$ must be high during address transition.

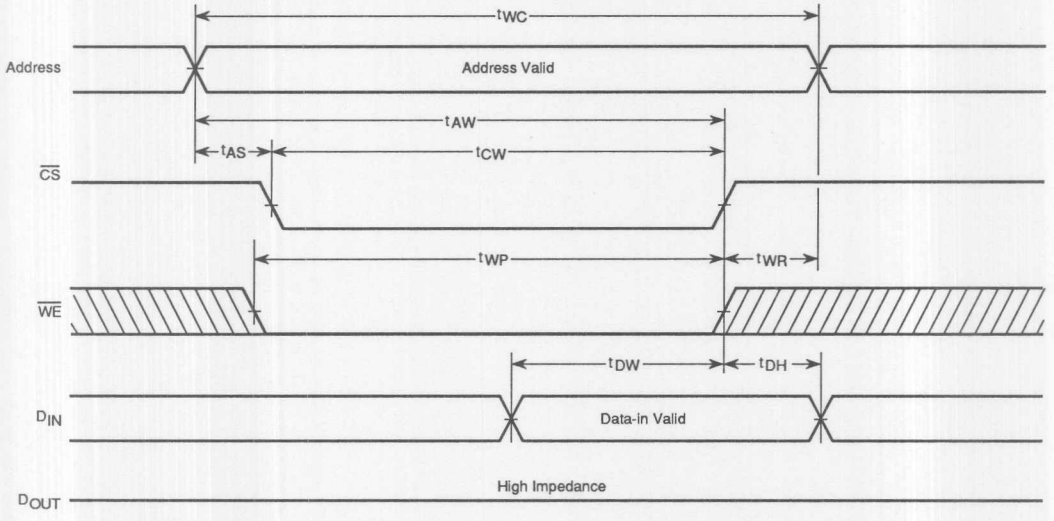
[3] If $\overline{OE}$ is high, the I/O pins remain in a state of high impedance.

[4] During this period, the I/O pins may be in the output state. Therefore, input signals of opposite phase must not be applied.

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Timing Waveforms (cont)

$\overline{CS}$-Controlled Write Cycle



Notes:

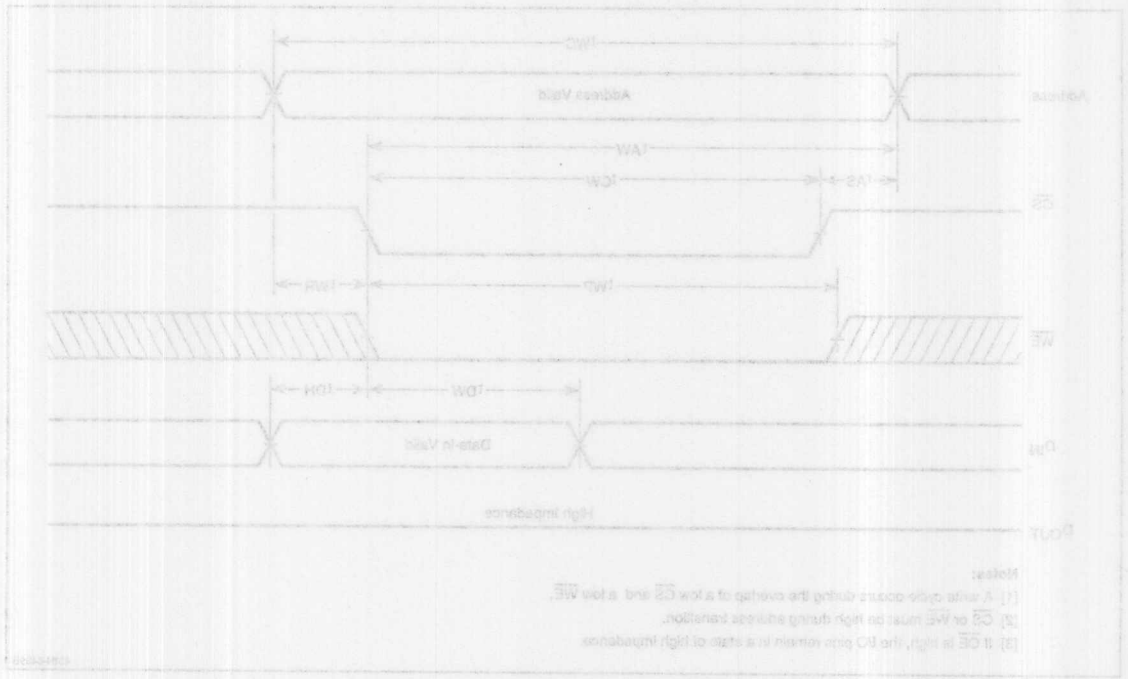
[1] A write cycle occurs during the overlap of a low $\overline{CS}$ and a low $\overline{WE}$.

[2] $\overline{CS}$ or $\overline{WE}$ must be high during address transition.

[3] If $\overline{OE}$ is high, the I/O pins remain in a state of high impedance.

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μPD43256B
32,768 x 8-Bit
Static CMOS RAM

Description

The μPD43256B is a 32,768-word by 8-bit static RAM fabricated with advanced silicon-gate technology. Its unique design uses CMOS peripheral circuits and N-channel memory cells with polysilicon resistors to make the μPD43256B a high-speed device that requires very low power and no clock or refreshing.

Minimum standby power is drawn when $\overline{CS}$ is high, independent of the other inputs' levels. Data retention is guaranteed at a power supply voltage as low as 2 V. The μPD43256B is available in standard 28-pin plastic DIP, 28-pin plastic miniflat, or 32-pin plastic TSOP packaging.

Features

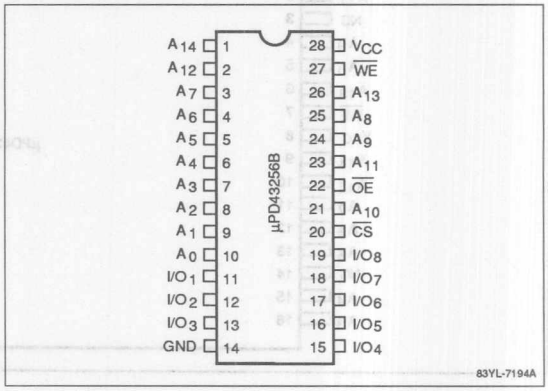
- Single + 5-volt power supply
- Fully static operation—no clock or refreshing
- TTL-compatible inputs and outputs
- Common I/O using three-state outputs
- One $\overline{CS}$ pin and one $\overline{OE}$ pin for easy application
- Data retention of 2 V minimum
- Standard 28-pin plastic DIP and miniflat packaging
- Standard 32-pin plastic TSOP packaging (with either normal or reverse bent leads)
- Fast access time of 55 ns

Ordering Information

Part Number	Access Time (max)	Package
μPD43256BC-55L	55 ns	28-pin plastic DIP
C-70L	70 ns	
C-85L	85 ns	
μPD43256BGU-55L	55 ns	28-pin plastic miniflat
GU-70L	70 ns	
GU-85L	85 ns	
μPD43256BGX55L-EJA	55 ns	32-pin plastic TSOP (normal leads)
GX70L-EJA	70 ns	
GX85L-EJA	85 ns	
μPD43256BGX55L-EKA	55 ns	32-pin plastic TSOP (reverse bent leads)
GX70L-EKA	70 ns	
GX85L-EKA	85 ns	

Pin Configurations

28-Pin Plastic DIP or Miniflat



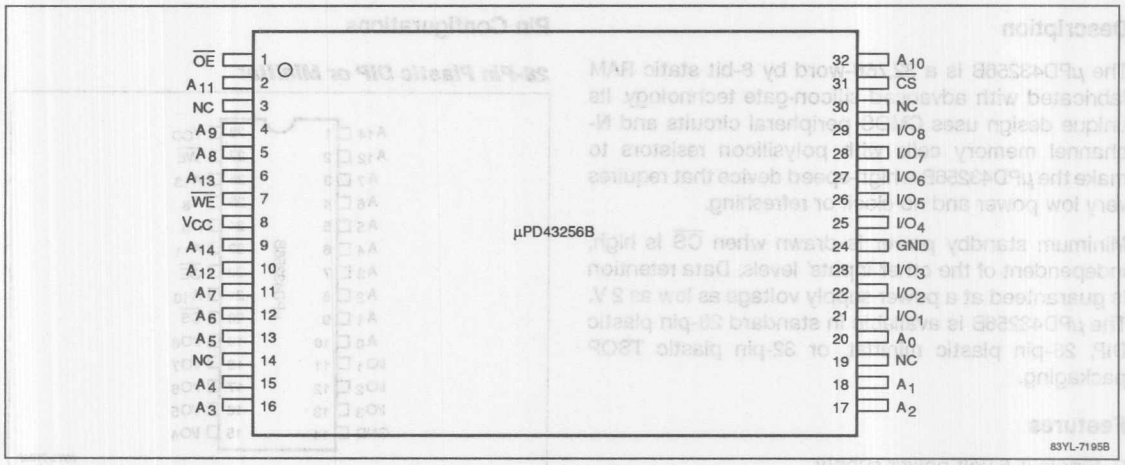
Pin Identification

Symbol	Function
A_0 - A_{14}	Address inputs
I/O_1 - I/O_8	Data inputs and outputs
$\overline{CS}$	Chip select
$\overline{OE}$	Output enable
$\overline{WE}$	Write enable
GND	Ground
V_{CC}	+5-volt power supply
NC	No connection

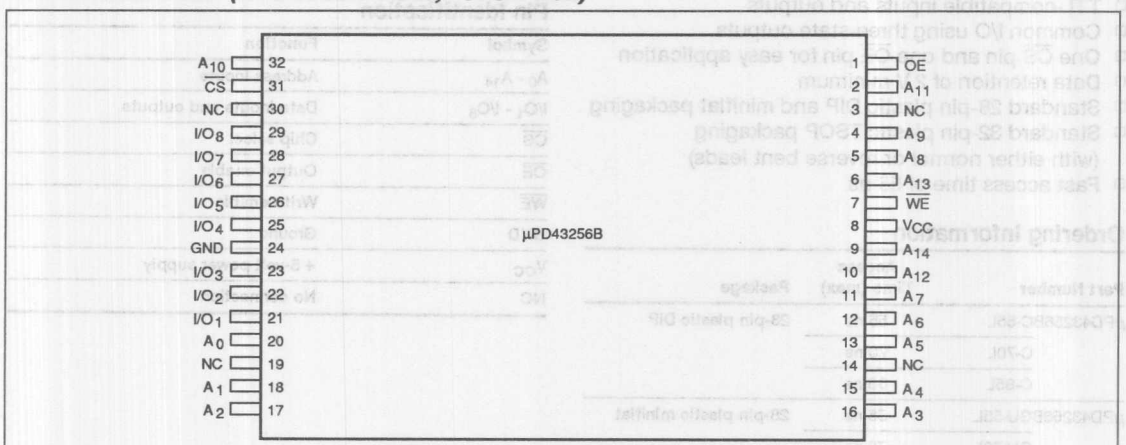
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Pin Configurations (cont)

32-Pin Plastic TSOP (normal leads, top view)



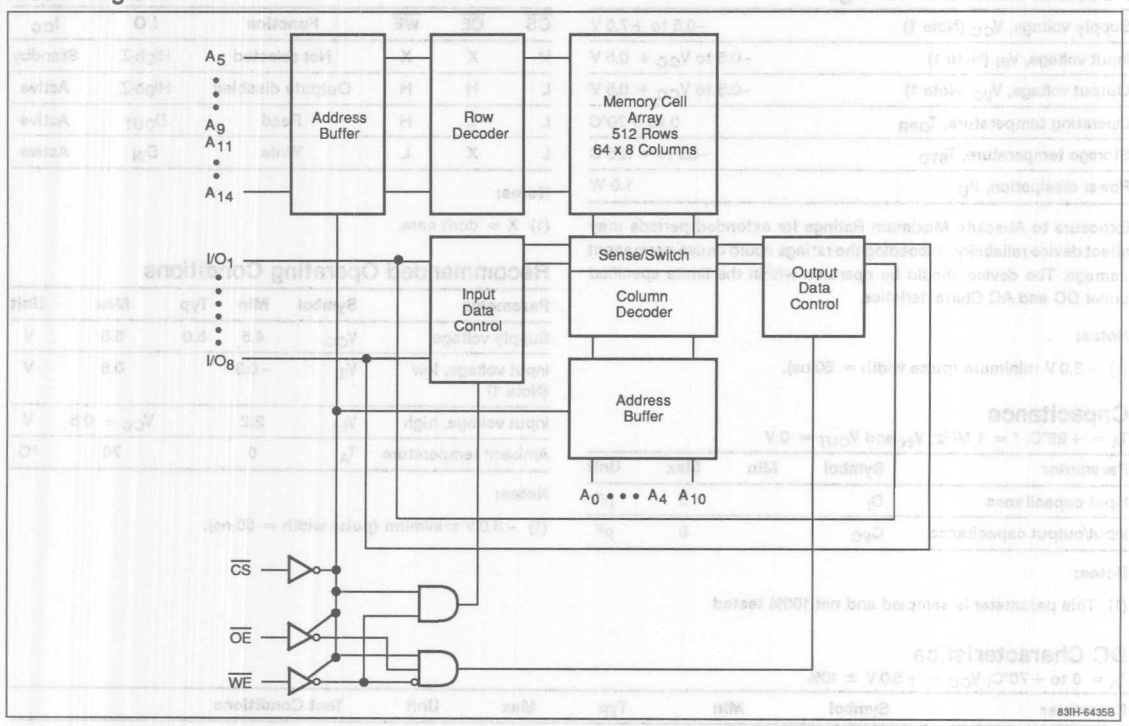
32-Pin Plastic TSOP (reverse bent leads, bottom view)



Notes:

[1] This package is designed to be mounted with the top of the package closest to the mounting surface. In this position, the exposed side will be the bottom of the package.

Block Diagram



Absolute Maximum Ratings

Supply voltage, V_{CC} (Note 1)	−0.5 to +7.0 V
Input voltage, V_{IN} (Note 1)	−0.5 to V_{CC} + 0.5 V
Output voltage, $V_{I/O}$ (Note 1)	−0.5 to V_{CC} + 0.5 V
Operating temperature, T_{OPR}	0 to +70°C
Storage temperature, T_{STG}	−55 to +125°C
Power dissipation, P_D	1.0 W

Exposure to Absolute Maximum Ratings for extended periods may affect device reliability; exceeding the ratings could cause permanent damage. The device should be operated within the limits specified under DC and AC Characteristics.

Notes:

(1) −3.0 V minimum (pulse width = 50 ns).

Capacitance

T_A = +25°C; f = 1 MHz; V_{IN} and V_{OUT} = 0 V

Parameter	Symbol	Min	Max	Unit
Input capacitance	C_I		5	pF
Input/output capacitance	$C_{I/O}$		8	pF

Notes:

(1) This parameter is sampled and not 100% tested.

Truth Table

$\overline{CS}$	$\overline{OE}$	$\overline{WE}$	Function	I/O	I_{CC}
H	X	X	Not selected	High-Z	Standby
L	H	H	Outputs disabled	High-Z	Active
L	L	H	Read	D_{OUT}	Active
L	X	L	Write	D_{IN}	Active

Notes:

(1) X = don't care.

Recommended Operating Conditions

Parameter	Symbol	Min	Typ	Max	Unit
Supply voltage	V_{CC}	4.5	5.0	5.5	V
Input voltage, low (Note 1)	V_{IL}	−0.3		0.8	V
Input voltage, high	V_{IH}	2.2		V_{CC} + 0.5	V
Ambient temperature	T_A	0		70	°C

Notes:

(1) −3.0 V minimum (pulse width = 50 ns).

DC Characteristics

T_A = 0 to +70°C; V_{CC} = +5.0 V ± 10%

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions
Input leakage current	I_{LI}	−1		1	μA	V_{IN} = 0 V to V_{CC}
I/O leakage current	I_{LO}	−1		1	μA	$V_{I/O}$ = 0 V to V_{CC}; $\overline{CS} \geq V_{IH}$ or $\overline{OE} \geq V_{IH}$ or $\overline{WE} \leq V_{IL}$
Operating supply current	I_{CCA1}			50	mA	$\overline{CS} \leq V_{IL}$ (min cycle); $I_{I/O}$ = 0 V (Note 1)
	I_{CCA2}			10	mA	$\overline{CS}$ = V_{IL}; $I_{I/O}$ = 0 V
	I_{CCA3}			10	mA	$\overline{CS} \leq$ 0.2 V; f = 1 MHz; $I_{I/O}$ = 0 V; $V_{IL} \leq$ 0.2 V; $V_{IH} \geq V_{CC}$ − 0.2 V
Standby supply current	I_{SB}			3	mA	$\overline{CS} \geq V_{IH}$
	I_{SB1}		2	100	μA	$\overline{CS} \geq V_{CC}$ − 0.2 V
Output voltage, low	V_{OL}			0.4	V	I_{OL} = 2.1 mA
Output voltage, high	V_{OH1}	2.4			V	I_{OH} = −1.0 mA
	V_{OH2}	V_{CC} − 0.5			V	I_{OH} = −0.1 mA

Notes:

(1) μPD43256B-55L = 50 mA (max).
μPD43256B-70L/-85L = 45 mA (max).

AC Characteristics (All Versions)

T_A = 0 to +70°C; V_{CC} = +5.0 V ± 10%

		μPD43256B-55		μPD43256B-70		μPD43256B-85			
Parameter	**Symbol**	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**	**Unit**	**Test Conditions**
Read Operation									
Read cycle time	t_{RC}	55		70		85		ns	(Note 2)
Address access time	t_{AA}		55		70		85	ns	(Note 2)
Chip select access time	t_{ACS}		55		70		85	ns	(Note 2)
Output enable to output valid	t_{OE}		30		35		40	ns	(Note 2)
Output hold from address change	t_{OH}	10		10		10		ns	(Note 2)
Chip select to output in low-Z	t_{CLZ}	10		10		10		ns	(Note 3)
Output enable to output in low-Z	t_{OLZ}	5		5		5		ns	(Note 3)
Chip select to output in high-Z	t_{CHZ}		30		30		30	ns	(Note 3)
Output enable to output in high-Z	t_{OHZ}		30		30		30	ns	(Note 3)
Write Operation									
Write cycle time	t_{WC}	55		70		85		ns	
Chip select to end of write	t_{CW}	50		60		70		ns	
Address valid to end of write	t_{AW}	50		60		70		ns	
Address setup time	t_{AS}	0		0		0		ns	
Write pulse width	t_{WP}	45		55		65		ns	
Write recovery time	t_{WR}	5		5		5		ns	
Data valid to end of write	t_{DW}	30		30		35		ns	
Data hold time	t_{DH}	0		0		0		ns	
Write enable to output in high-Z	t_{WHZ}		30		30		30	ns	(Note 3)
Output active from end of write	t_{OW}	10		10		10		ns	(Note 3)

Notes:

(1) Input pulse levels = 0.8 to 2.2 V; input pulse rise and fall times = 5 ns; timing reference levels = 1.5 V.

(2) See figure 1 for output load.

(3) See figure 2 for output load.

7

Low V_{CC} Data Retention Characteristics

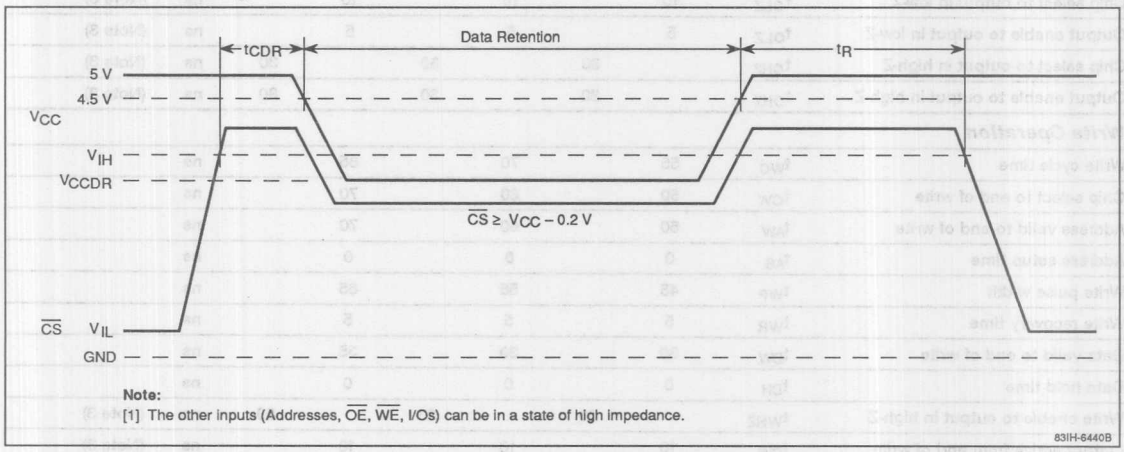
T_A = 0 to 70°C

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions
Data retention supply voltage	V_{CCDR}	2.0		5.5	V	$\overline{CS} \geq V_{CC} - 0.2$ V
Data retention supply current	I_{CCDR}		1	50	μA	V_{CC} = 3.0 V; $\overline{CS} \geq V_{CC} - 0.2$ V (Note 1)
Chip deselection to data retention	t_{CDR}	0			ns	
Operation recovery time	t_R	t_{RC}			ns	

Notes:

(1) I_{CCDR} = 15 μA (max) at T_A = 0 to 40°C.

Data Retention Timing



Note:

[1] The other inputs (Addresses, $\overline{OE}$, $\overline{WE}$, I/Os) can be in a state of high impedance.

83IH-6440B

Figure 1. Output Load

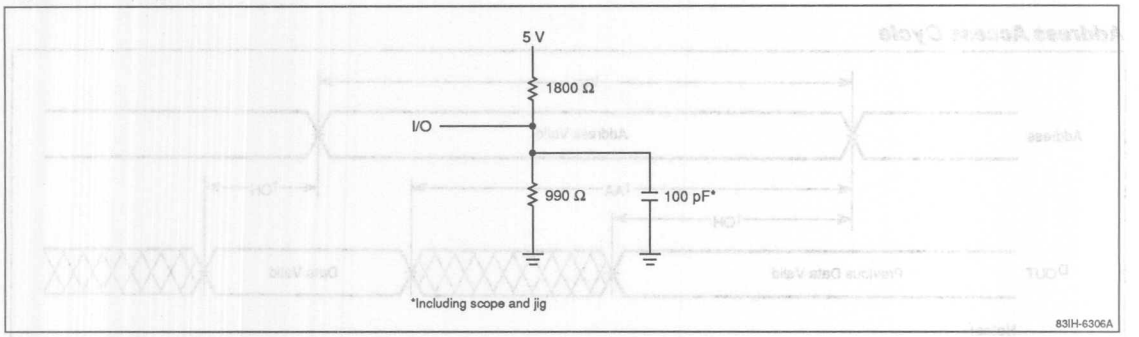
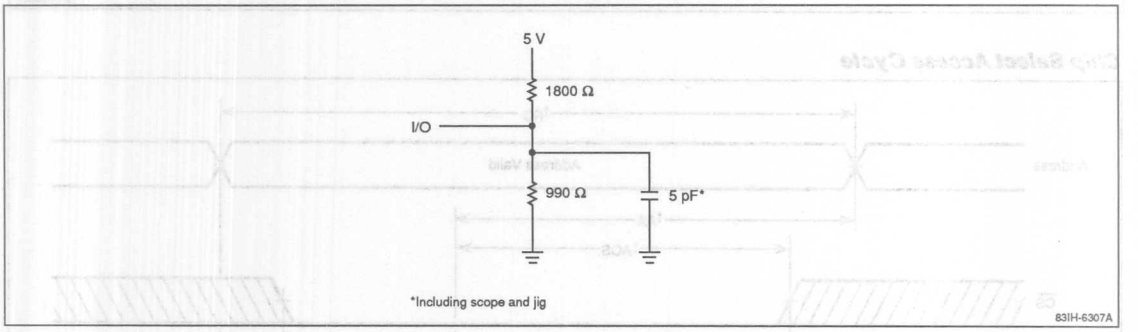


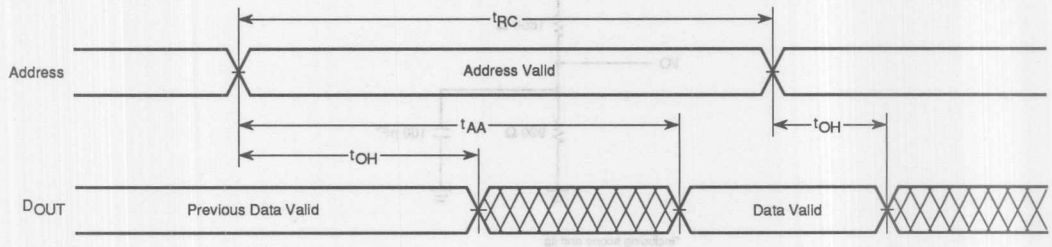
Figure 2. Output Load for t_{CLZ}, t_{OLZ}, t_{CHZ}, t_{OHZ}, t_{WHZ}, and t_{OW}



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Timing Waveforms

Address Access Cycle



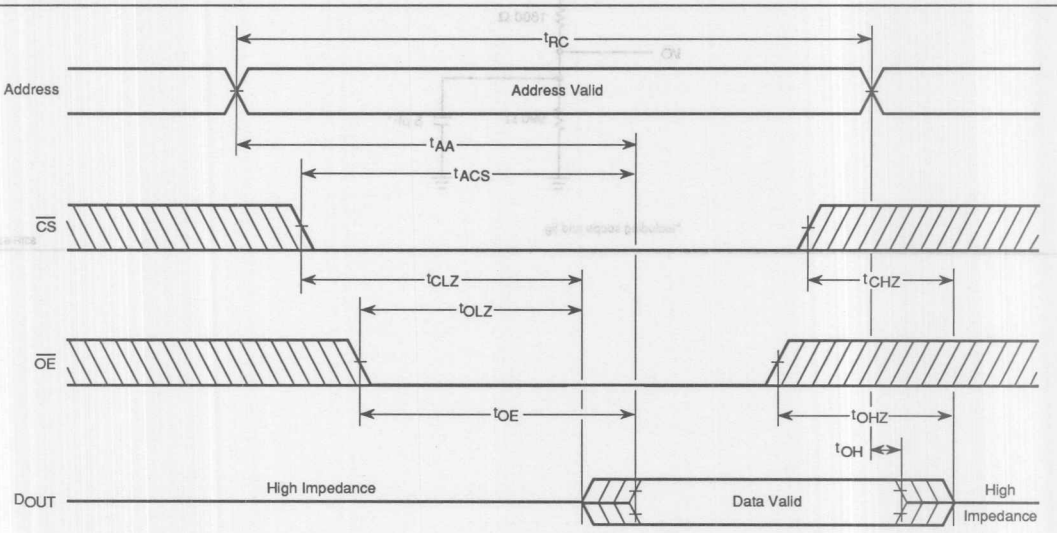
Notes:

[1] $\overline{WE}$ is held high for a read cycle.

[2] The device is continually selected, where $\overline{CS} = \overline{OE} = V_{IL}$.

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Chip Select Access Cycle



Notes:

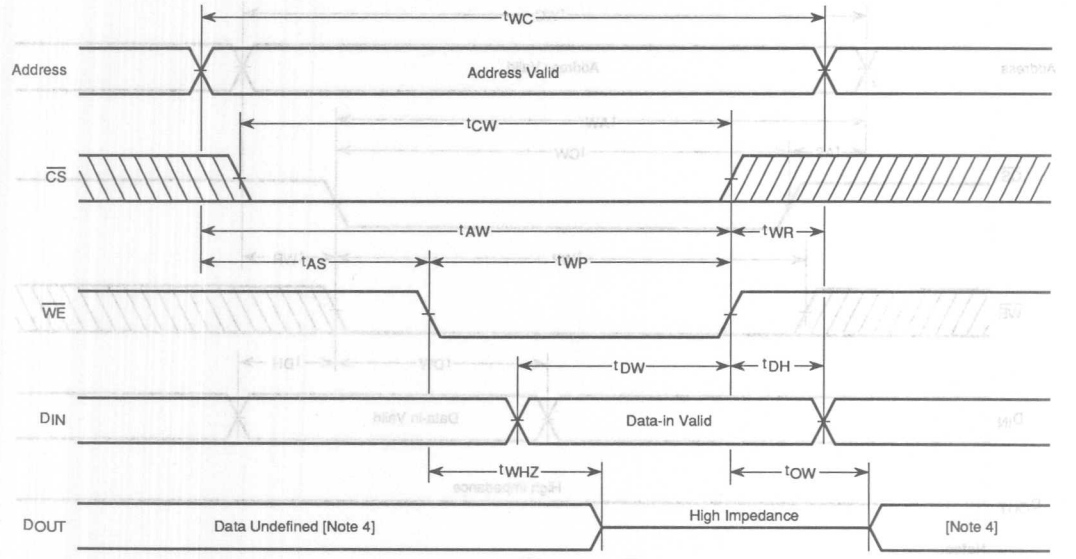
[1] $\overline{WE}$ is high for a read cycle.

[2] Address valid prior to or coincident with the low transition of $\overline{CS}$.

83IH-6437B

Timing Waveforms (cont)

$\overline{WE}$-Controlled Write Cycle



Notes:

[1] A write cycle occurs during the overlap of a low $\overline{CS}$ and a low $\overline{WE}$.

[2] $\overline{CS}$ or $\overline{WE}$ must be high during address transition.

[3] If $\overline{OE}$ is high, the I/O pins remain in a state of high impedance.

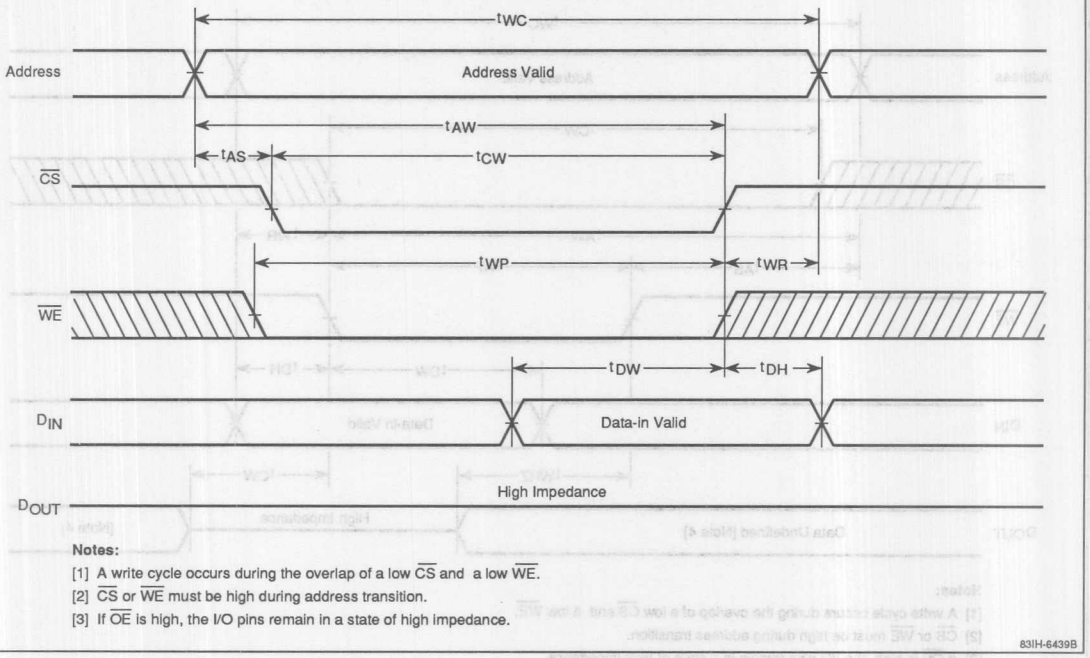
[4] During this period, the I/O pins may be in the output state. Therefore, input signals of opposite phase must not be applied.

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Timing Waveforms (cont)

$\overline{CS}$-Controlled Write Cycle



Notes:

[1] A write cycle occurs during the overlap of a low $\overline{CS}$ and a low $\overline{WE}$.

[2] $\overline{CS}$ or $\overline{WE}$ must be high during address transition.

[3] If $\overline{OE}$ is high, the I/O pins remain in a state of high impedance.

NEC Electronics Inc.

μPD43258
32,768 x 8-Bit
Static CMOS RAM

PRELIMINARY INFORMATION

Description

The μPD43258 is a 32,768-word by 8-bit static RAM fabricated with advanced silicon-gate technology. Its unique design uses CMOS peripheral circuits and N-channel memory cells with polysilicon resistors to make the μPD43258 a high-speed device that requires very low power and no clock or refreshing.

Minimum standby power is drawn when $\overline{CS}$ is high, independent of the other inputs' levels. The μPD43258 is available in standard 28-pin plastic DIP or SOJ packaging.

Features

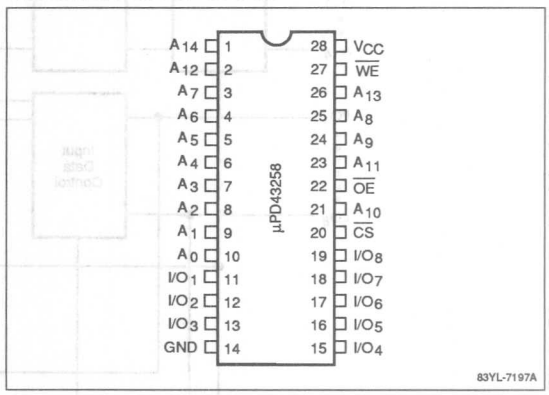
- Single +5-volt power supply
- Fully static operation—no clock or refreshing
- TTL-compatible inputs and outputs
- Common I/O using three-state outputs
- One $\overline{CS}$ pin and one $\overline{OE}$ pin for easy application
- Standard 28-pin plastic DIP and SOJ packaging
- Fast access time of 35 ns (max)

Ordering Information

Part Number	Access Time (max)	Package
μPD43258CR-35	35 ns	28-pin plastic DIP
CR-45	45 ns	
μPD43258LA-35	35 ns	28-pin plastic SOJ
LA-45	45 ns	

Pin Configurations

28-Pin Plastic DIP or SOJ

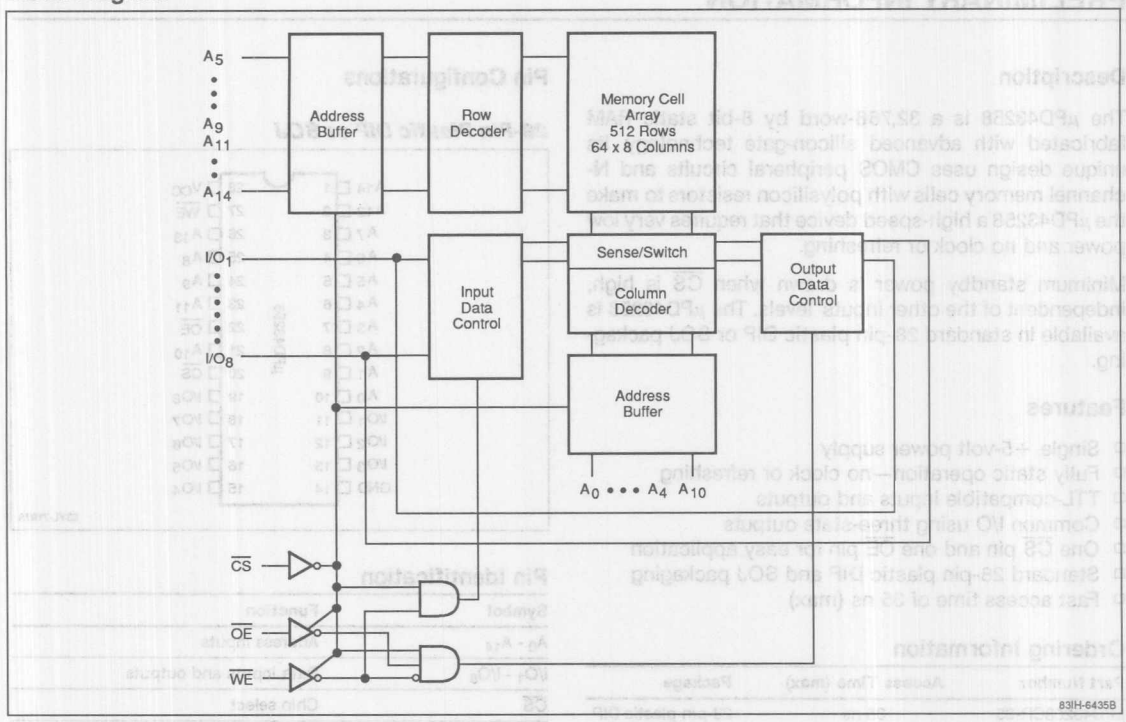


Pin Identification

Symbol	Function
A_0 - A_{14}	Address inputs
I/O_1 - I/O_8	Data inputs and outputs
$\overline{CS}$	Chip select
$\overline{OE}$	Output enable
$\overline{WE}$	Write enable
GND	Ground
V_{CC}	+5-volt power supply

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Block Diagram



Truth Table

$\overline{CS}$	$\overline{OE}$	$\overline{WE}$	Function	I/O	I_{CC}
H	X	X	Not selected	High-Z	Standby
L	H	H	Outputs disabled	High-Z	Active
L	L	H	Read	D_{OUT}	Active
L	X	L	Write	D_{IN}	Active

Notes:

(1) X = don't care.

Recommended Operating Conditions

Parameter	Symbol	Min	Typ	Max	Unit
Supply voltage	V_{CC}	4.5	5.0	5.5	V
Input voltage, low (Note 1)	V_{IL}	−0.3		0.8	V
Input voltage, high	V_{IH}	2.2		V_{CC} + 0.5	V
Ambient temperature	T_A	0		70	°C

Notes:

(1) −3.0 V minimum (pulse width = 20 ns).

DC Characteristics

T_A = 0 to +70°C; V_{CC} = +5.0 V ± 10%

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions
Input leakage current	I_{LI}	−2		2	μA	V_{IN} = 0 V to V_{CC}
I/O leakage current	I_{LO}	−2		2	μA	$V_{I/O}$ = 0 V to V_{CC}; $\overline{CS} \geq V_{IH}$ or $\overline{OE} \geq V_{IH}$ or $\overline{WE} \leq V_{IL}$
Operating supply current	I_{CC}			130	mA	$\overline{CS} \leq V_{IL}$ (min cycle); $I_{I/O}$ = 0 V
Standby supply current	I_{SB}			30	ma	$\overline{CS} \geq V_{IH}$; $V_{IN} = V_{IH}$ or V_{IL}
	I_{SB1}			2	mA	$\overline{CS} \geq V_{CC} - 0.2$ V; $V_{IN} \leq 0.2$ V or $\geq V_{CC} - 0.2$ V
Output voltage, low	V_{OL}			0.4	V	I_{OL} = 8 mA
Output voltage, high	V_{OH}	2.4			V	I_{OH} = −4.0 mA

Absolute Maximum Ratings

Supply voltage, V_{CC} (Note 1)	−0.5 to +7.0 V
Input voltage, V_{IN} (Note 1)	−0.5 to V_{CC} + 0.5 V
Output voltage, $V_{I/O}$ (Note 1)	−0.5 to V_{CC} + 0.5 V
Operating temperature, T_{OPR}	0 to +70°C
Storage temperature, T_{STG}	−55 to +125°C

Exposure to Absolute Maximum Ratings for extended periods may affect device reliability; exceeding the ratings could cause permanent damage. The device should be operated within the limits specified under DC and AC Characteristics.

Notes:

(1) −3.0 V minimum (pulse width = 20 ns).

Capacitance

T_A = +25°C; f = 1 MHz; V_{IN} and V_{OUT} = 0 V

Parameter	Symbol	Min	Max	Unit
Input capacitance	C_I		6	pF
Input/output capacitance	$C_{I/O}$		8	pF

Notes:

(1) This parameter is sampled and not 100% tested.

AC Characteristics

T_A = 0 to +70°C; V_{CC} = +5.0 V ± 10%

		μPD43258-35		μPD43258-45			
Parameter	**Symbol**	**Min**	**Max**	**Min**	**Max**	**Unit**	**Test Conditions**
Read Operation							
Read cycle time	t_{RC}	35		45		ns	(Note 2)
Address access time	t_{AA}		35		45	ns	(Note 2)
Chip select access time	t_{ACS}		35		45	ns	(Note 2)
Output enable to output valid	t_{OE}		17		20	ns	(Note 2)
Output hold from address change	t_{OH}	5		5		ns	(Note 2)
Chip select to output in low-Z	t_{CLZ}	5		5		ns	(Note 3)
Output enable to output in low-Z	t_{OLZ}	0		0		ns	(Note 3)
Chip select to output in high-Z	t_{CHZ}		15		20	ns	(Note 3)
Output enable to output in high-Z	t_{OHZ}		15		20	ns	(Note 3)
Write Operation							
Write cycle time	t_{WC}	35		45		ns	
Chip select to end of write	t_{CW}	30		40		ns	
Address valid to end of write	t_{AW}	30		40		ns	
Address setup time	t_{AS}	0		0		ns	
Write pulse width	t_{WP}	30		40		ns	
Write recovery time	t_{WR}	0		0		ns	
Data valid to end of write	t_{DW}	15		20		ns	
Data hold time	t_{DH}	0		0		ns	
Write enable to output in high-Z	t_{WHZ}		15		20	ns	(Note 3)
Output active from end of write	t_{OW}	0		0		ns	(Note 3)

Notes:

(1) Input pulse levels = 0 to 3 V; input pulse rise and fall times = 5 ns; timing reference levels = 1.5 V.

(2) See figure 1 for output load.

(3) See figure 2 for output load.

7

Figure 1. Output Load

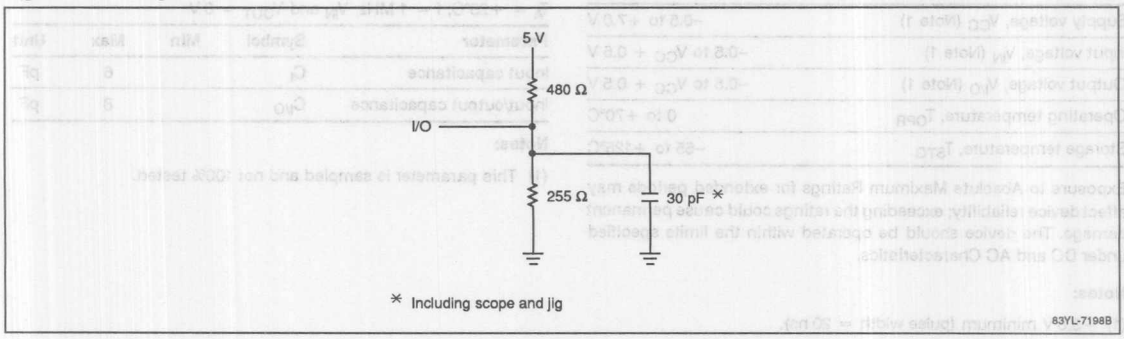
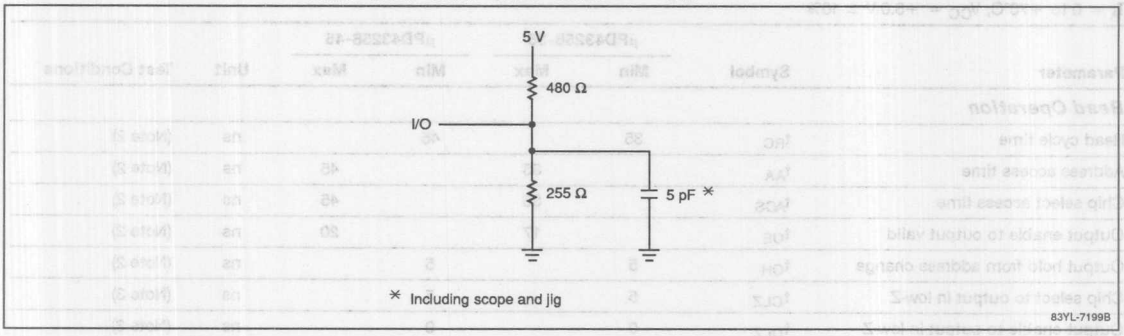
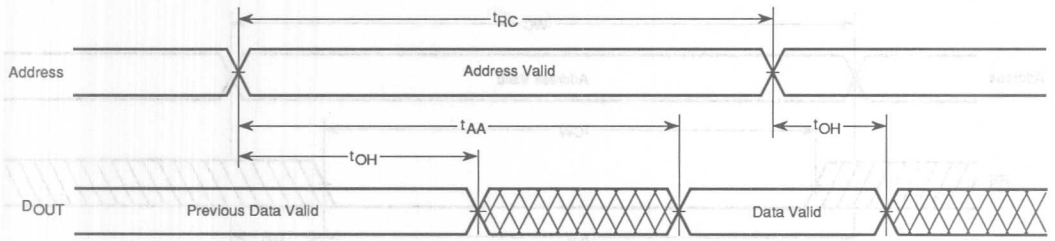


Figure 2. Output Load for t_{CLZ}, t_{OLZ}, t_{CHZ}, t_{OHZ}, t_{WHZ}, and t_{OW}



Timing Waveforms

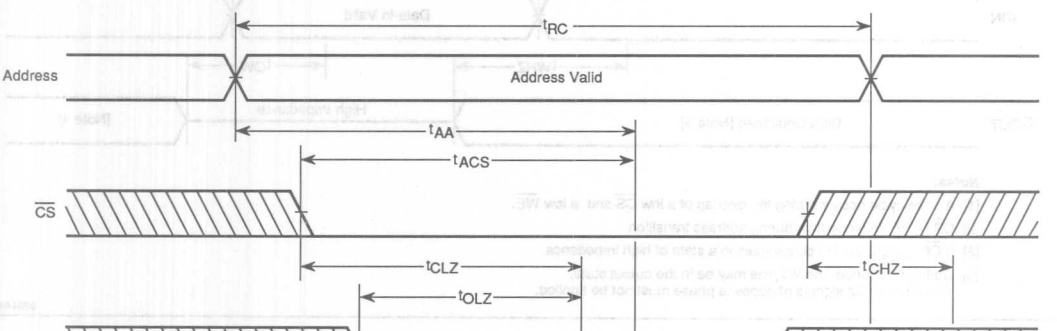
Address Access Cycle



Notes:
[1] $\overline{WE}$ is held high for a read cycle.
[2] The device is continually selected, where $\overline{CS} = \overline{OE} = V_{IL}$.

83IH-6436B

Chip Select Access Cycle



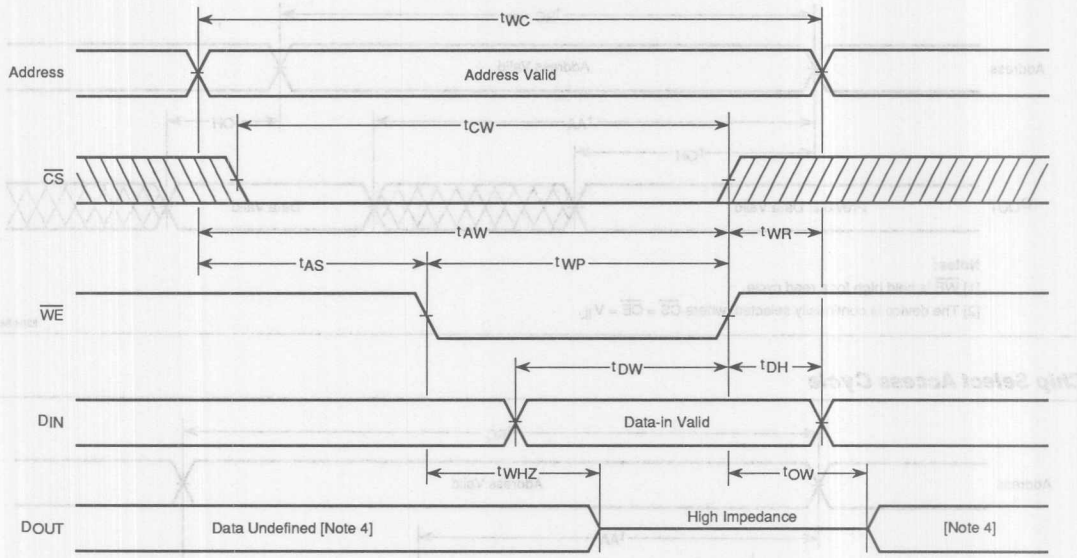
Notes:
[1] $\overline{WE}$ is high for a read cycle.
[2] Address valid prior to or coincident with the low transition of $\overline{CS}$.

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Timing Waveforms (cont)

$\overline{WE}$-Controlled Write Cycle



Notes:

[1] A write cycle occurs during the overlap of a low $\overline{CS}$ and a low $\overline{WE}$.

[2] $\overline{CS}$ or $\overline{WE}$ must be high during address transition.

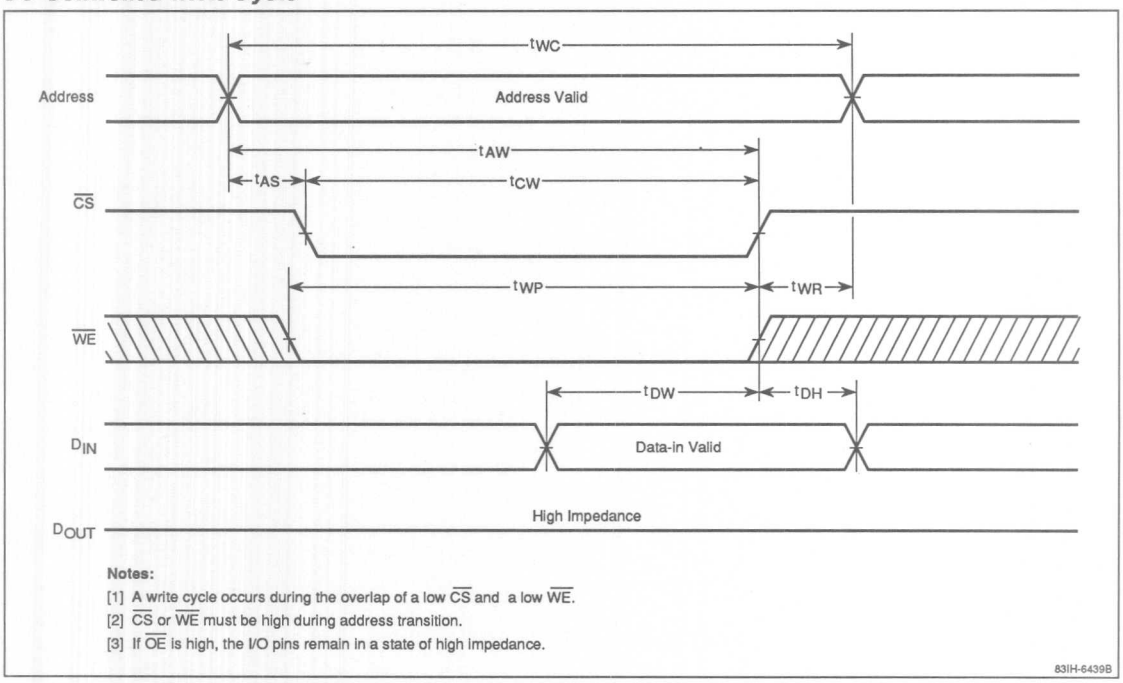
[3] If $\overline{OE}$ is high, the I/O pins remain in a state of high impedance.

[4] During this period, the I/O pins may be in the output state. Therefore, input signals of opposite phase must not be applied.

83IH-6438B

Timing Waveforms (cont)

$\overline{CS}$-Controlled Write Cycle



Notes:

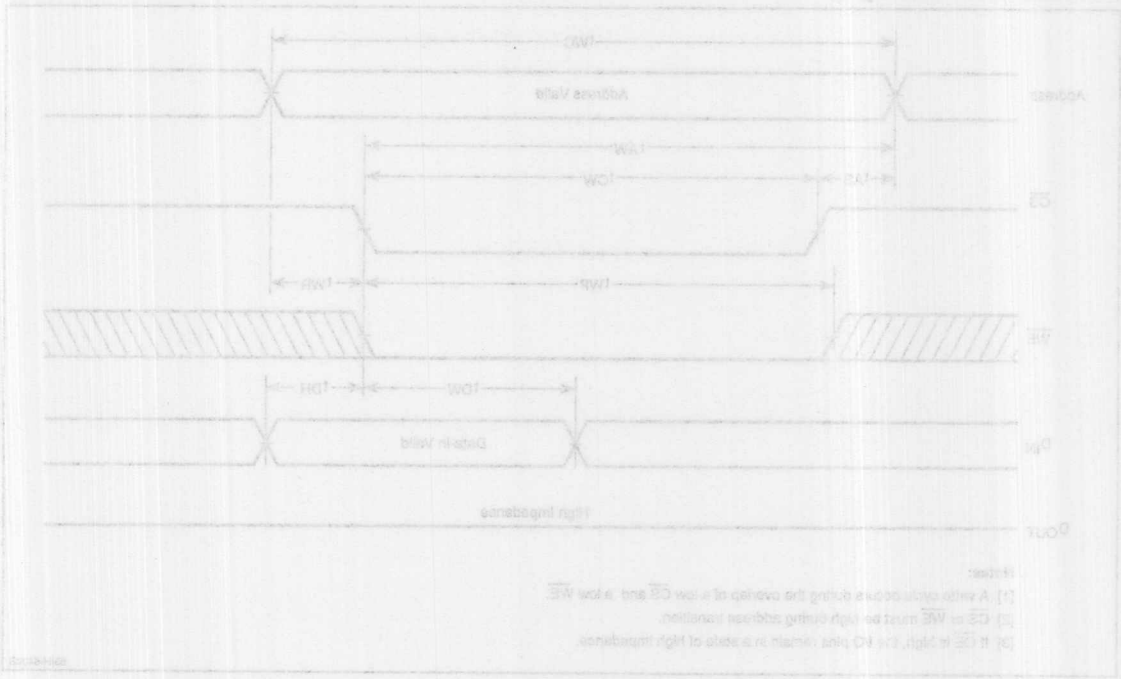
[1] A write cycle occurs during the overlap of a low $\overline{CS}$ and a low $\overline{WE}$.

[2] $\overline{CS}$ or $\overline{WE}$ must be high during address transition.

[3] If $\overline{OE}$ is high, the I/O pins remain in a state of high impedance.

83IH-6439B

7



μPD431000
131,072 x 8-Bit
Static CMOS RAM

Description

The μPD431000 is a 131,072-word by 8-bit static RAM fabricated with advanced silicon-gate technology. CMOS peripheral circuits and N-channel memory cells with polysilicon resistors make the μPD431000 a high-speed device that requires very low power and no clock or refreshing.

Minimum standby power is drawn when CE_2 is low, independent of the other inputs' levels. Data retention is guaranteed at a power supply voltage as low as 2 volts. The μPD431000 is available in standard 32-pin plastic DIP and miniflat packaging.

Features

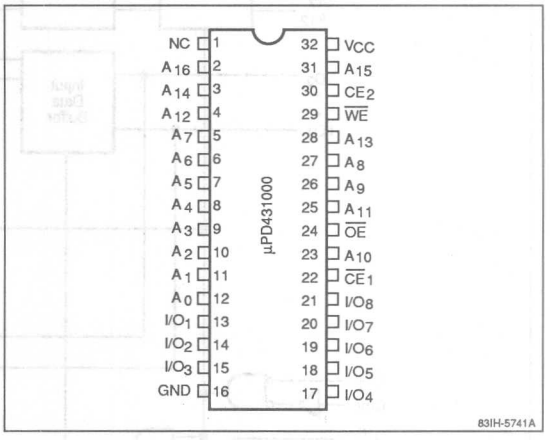
- 131,072-word by 8-bit organization
- Single +5-volt power supply
- Fully static operation—no clock or refreshing
- TTL-compatible inputs and outputs
- Common I/O using three-state outputs
- Two CE pins and one $\overline{OE}$ pin for easy application
- Data retention current of 1 μA typical
- Data retention voltage of 2 V minimum
- Standard 32-pin plastic DIP and miniflat packaging

Ordering Information

Part Number		Access Time (max)	I_{SB1} (max)	Package
μPD431000	CZ-85	85 ns	2 mA	32-pin plastic DIP
	CZ-10	100 ns		
	CZ-12	120 ns		
μPD431000	CZ-85L	85 ns	0.1 mA	
	CZ-10L	100 ns		
	CZ-12L	120 ns		
μPD431000	CZ-85LL	85 ns	0.05 mA	
	CZ-10LL	100 ns		
	CZ-12LL	120 ns		
μPD431000	GW-85L	85 ns	0.1 mA	32-pin plastic miniflat
	GW-10L	100 ns		
	GW-12L	120 ns		
μPD431000	GW-85LL	85 ns	0.05 mA	
	GW-10LL	100 ns		
	GW-12LL	120 ns		

Pin Configuration

32-Pin Plastic DIP or Miniflat

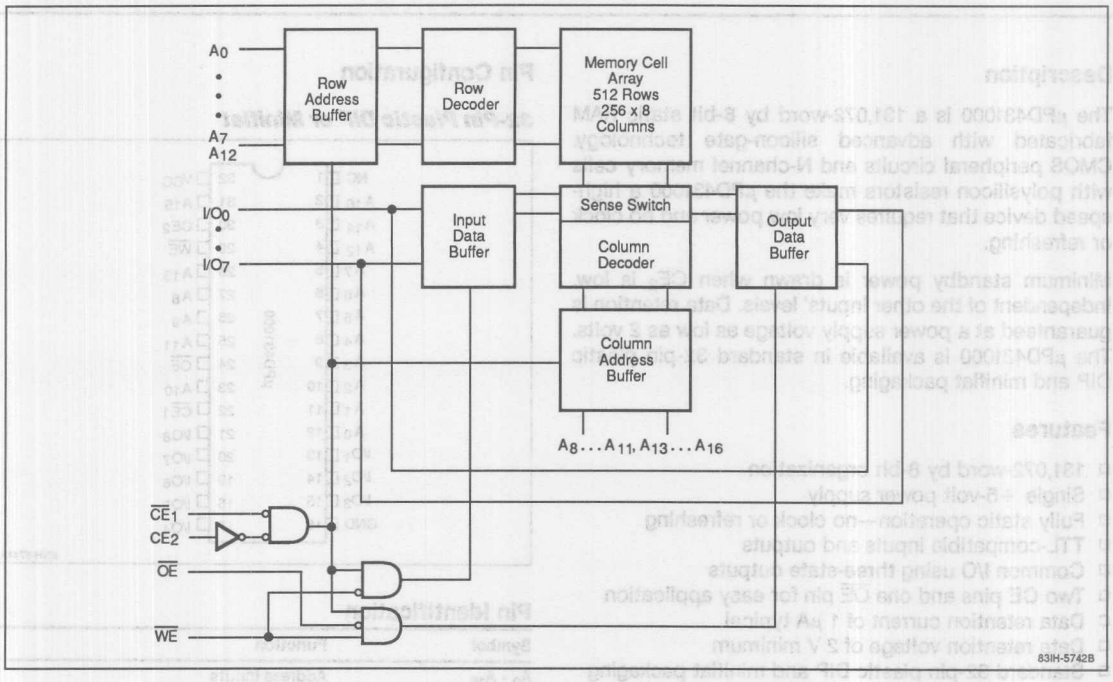


Pin Identification

Symbol	Function
A_0 - A_{16}	Address inputs
I/O_0 - I/O_7	Data inputs and outputs
$\overline{CE}_1$, CE_2	Chip enables 1 and 2
$\overline{OE}$	Output enable
$\overline{WE}$	Write enable
GND	Ground
V_{CC}	+5-volt power supply
NC	No connection

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Block Diagram



Absolute Maximum Ratings

Supply voltage, V_{CC} (Note 1)	−0.5 to +7.0 V
Input voltage, V_{IN} (Note 1)	−0.5 to V_{CC} + 0.5 V
Output voltage, $V_{I/O}$ (Note 1)	−0.5 to V_{CC} + 0.5 V
Operating temperature, T_{OPR}	0 to +70°C
Storage temperature, T_{STG}	−55 to +125°C
Power dissipation, P_D	1.0 W

Exposure to Absolute Maximum Ratings for extended periods may affect device reliability; exceeding the ratings could cause permanent damage. The device should be operated within the limits specified under DC and AC Characteristics.

Notes:

(1) −3.0 V minimum (pulse width = 50 ns).

Capacitance

T_A = +25°C; f = 1 MHz; V_{IN} and V_{OUT} = 0 V

Parameter	Symbol	Min	Typ	Max	Unit
Input capacitance	C_I			6	pF
Input/output capacitance	$C_{I/O}$			10	pF

Notes:

(1) This parameter is sampled and not 100% tested.

Truth Table

Function	$\overline{CE_1}$	CE_2	$\overline{OE}$	$\overline{WE}$	I/O	I_{CC}
Not selected	H	X	X	X	High-Z	Standby
Not selected	X	L	X	X	High-Z	Standby
Selected	L	H	H	H	High-Z	Active
Read	L	H	L	H	D_{OUT}	Active
Write	L	H	X	L	D_{IN}	Active

Notes:

(1) X = don't care.

Recommended Operating Conditions

Parameter	Symbol	Min	Typ	Max	Unit
Supply voltage	V_{CC}	4.5	5.0	5.5	V
Input voltage, low	V_{IL}	−0.3		0.8	V
Input voltage, high	V_{IH}	2.2		V_{CC} + 0.5	V
Ambient temperature	T_A	0		70	°C

Notes:

(1) −3.0 V minimum (pulse width = 50 ns).

DC Characteristics

T_A = 0 to +70°C; V_{CC} = +5.0 V ± 10%

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions
Input leakage current	I_{LI}	−1		1	μA	V_{IN} = 0 V to V_{CC}
I/O leakage current	I_{LO}	−1		1	μA	$V_{I/O}$ = 0 V to V_{CC}; $\overline{CE_1}$ = V_{IH}, or CE_2 = V_{IL}, or $\overline{OE}$ = V_{IH}, or $\overline{WE}$ = V_{IL}
Operating supply current	I_{CCA1}			70	mA	$\overline{CE_1}$ = V_{IL}; CE_2 = V_{IH}; t_{RC} = t_{RC} (min); $I_{I/O}$ = 0 mA
	I_{CCA2}		15	35	mA	$\overline{CE_1}$ = V_{IL}; CE_2 = V_{IH}; $I_{I/O}$ = 0 mA
Standby supply current	I_{SB}			3	mA	$\overline{CE_1}$ = V_{IH} or CE_2 = V_{IL} (Note 1)
	I_{SB1}		0.02	2	mA	$\overline{CE_1}$ and CE_2 ≥ V_{CC} − 0.2 V (Note 2)
	I_{SB2}		0.02	2	mA	CE_2 ≤ 0.2 V (Note 2)
Output voltage, low	V_{OL}			0.4	V	I_{OL} = 2.1 mA
Output voltage, high	V_{OH}	2.4			V	I_{OH} = −1.0 mA

Notes:

(1) I_{SB} = 5 mA (max) for non-L versions.

(2) I_{SB1} and I_{SB2} = 0.02 mA (typ) and 0.1 mA (max) for -L versions and 0.002 mA (typ) and 0.05 mA (max) for -LL versions.

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AC Characteristics

T_A = 0 to +70°C; V_{CC} = +5.0 V ± 10%

Parameter	Symbol	μPD431000-85 Min	μPD431000-85 Max	μPD431000-10 Min	μPD431000-10 Max	μPD431000-12 Min	μPD431000-12 Max	Unit	Test Conditions
Read Operation									
Read cycle time	t_{RC}	85		100		120		ns	
Address access time	t_{AA}		85		100		120	ns	(Note 2)
$\overline{CE}_1$ access time	t_{CO1}		85		100		120	ns	(Note 2)
CE_2 access time	t_{CO2}		85		100		120	ns	(Note 2)
Output enable to output valid	t_{OE}		45		50		60	ns	(Note 2)
Output hold from address change	t_{OH}	10		10		10		ns	
$\overline{CE}_1$ to output in low-Z	t_{LZ1}	10		10		10		ns	(Note 3)
CE_2 to output in low-Z	t_{LZ2}	10		10		10		ns	(Note 3)
Output enable to output in low-Z	t_{OLZ}	5		5		5		ns	(Note 3)
$\overline{CE}_1$ to output in high-Z	t_{HZ1}		30		35		45	ns	(Note 3)
CE_2 to output in high-Z	t_{HZ2}		30		35		45	ns	(Note 3)
Output enable to output in high-Z	t_{OHZ}		30		35		45	ns	(Note 3)
Write Operation									
Write cycle time	t_{WC}	85		100		120		ns	
$\overline{CE}_1$ to end of write	t_{CW1}	75		90		100		ns	
CE_2 to end of write	t_{CW2}	75		90		100		ns	
Address valid to end of write	t_{AW}	75		90		100		ns	
Address setup time	t_{AS}	0		0		0		ns	
Write pulse width	t_{WP}	65		75		85		ns	
Write recovery time	t_{WR}	5		5		5		ns	
Data valid to end of write	t_{DW}	35		40		45		ns	
Data hold time	t_{DH}	0		0		0		ns	
Write enable to output in high-Z	t_{WHZ}		30		35		40	ns	(Note 3)
Output active from end of write	t_{OW}	5		5		5		ns	(Note 3)

Notes:

(1) Input pulse levels = 0.8 to 2.2 V; input rise and fall times = 5 ns; timing reference levels = 1.5 V.

(2) See figure 1 for output loading.

(3) See figure 2 for output loading.

Low V_{CC} Data Retention Characteristics (-L and -LL Versions Only)

T_A = 0 to +70°C

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions
Data retention supply voltage	V_{CCDR1}	2		5.5	V	$\overline{CE_1} \geq V_{CC} - 0.2$ V; $CE_2 \geq V_{CC} - 0.2$ V or $CE_2 \leq 0.2$ V
	V_{CCDR2}	2		5.5	V	$CE_2 \leq 0.2$ V
Data retention supply current	I_{CCDR1}		1	50	μA	V_{CC} = 3.0 V; $\overline{CE_1} \geq V_{CC} - 0.2$ V; $CE_2 \geq V_{CC} - 0.2$ V or $CE_2 \leq 0.2$ V (Note 1)
	I_{CCDR2}		1	50	μA	V_{CC} = 3.0 V; $CE_2 \leq 0.2$ V (Note 1)
Chip deselection to data retention	t_{CDR}	0			ns	
Operation recovery time	t_R	t_{RC}			ns	

Notes:

(1) At 0 to 40°C, the maximum for I_{CCDR1} and I_{CCDR2} is 15 μA for the -L version and 5μA for the -LL version.

Figure 1. Output Loading

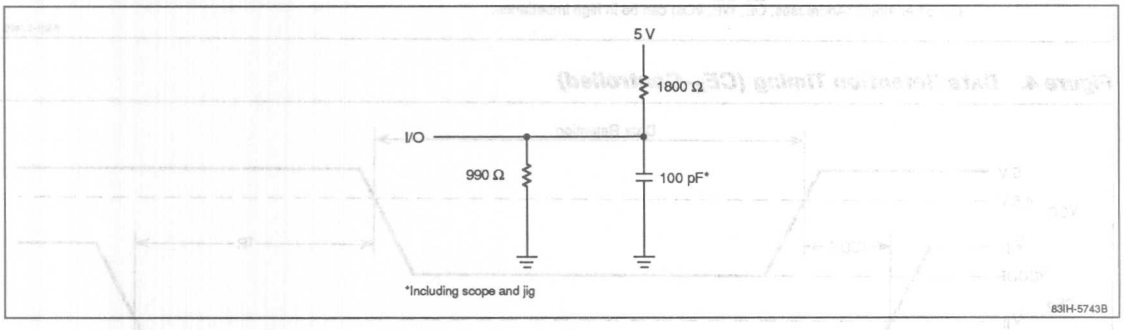
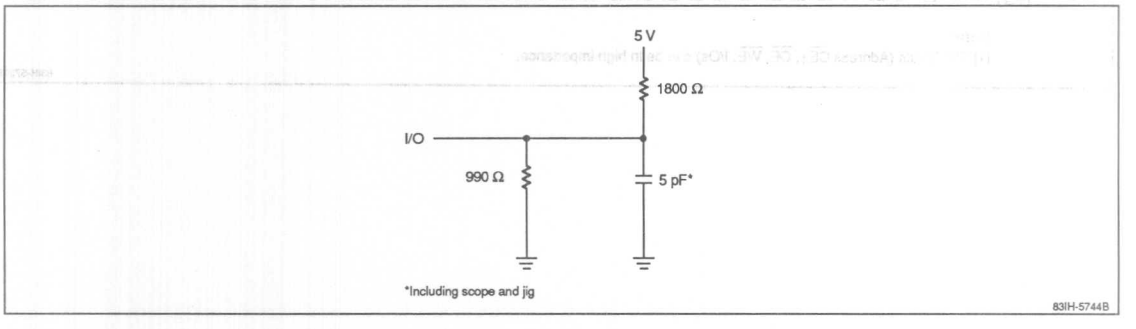
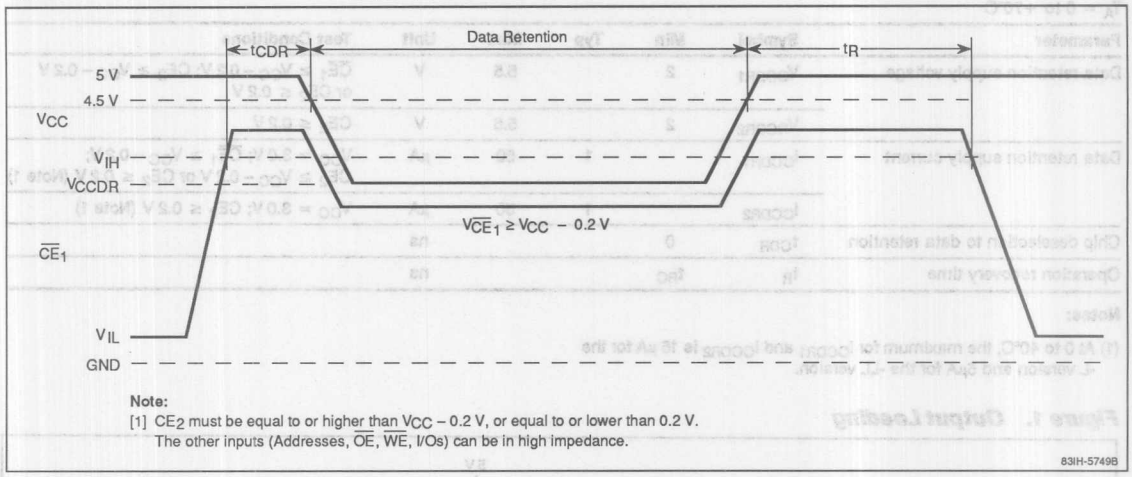


Figure 2. Output Loading for t_{HZ1}, t_{HZ2}, t_{LZ1}, t_{LZ2}, t_{OLZ}, t_{OHZ}, t_{OW}, and t_{WHZ}



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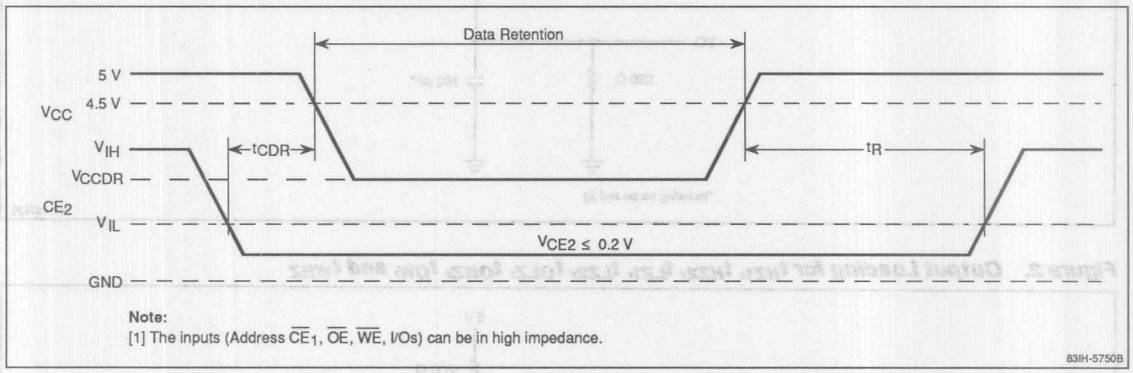
Figure 3. Data Retention Timing ($\overline{CE_1}$-Controlled)



Note:
[1] CE_2 must be equal to or higher than V_{CC} – 0.2 V, or equal to or lower than 0.2 V.
The other inputs (Addresses, $\overline{OE}$, $\overline{WE}$, I/Os) can be in high impedance.

83IH-5749B

Figure 4. Data Retention Timing (CE_2-Controlled)

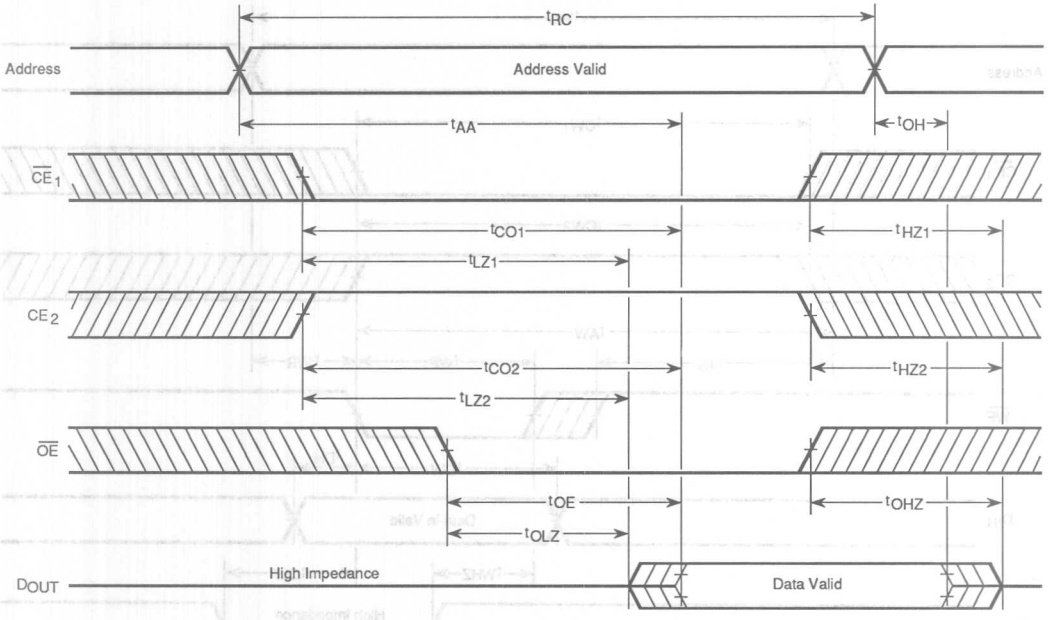


Note:
[1] The inputs (Address $\overline{CE_1}$, $\overline{OE}$, $\overline{WE}$, I/Os) can be in high impedance.

83IH-5750B

Timing Waveforms

Read Cycle



Notes:

[1] $\overline{WE}$ is high for a read cycle.

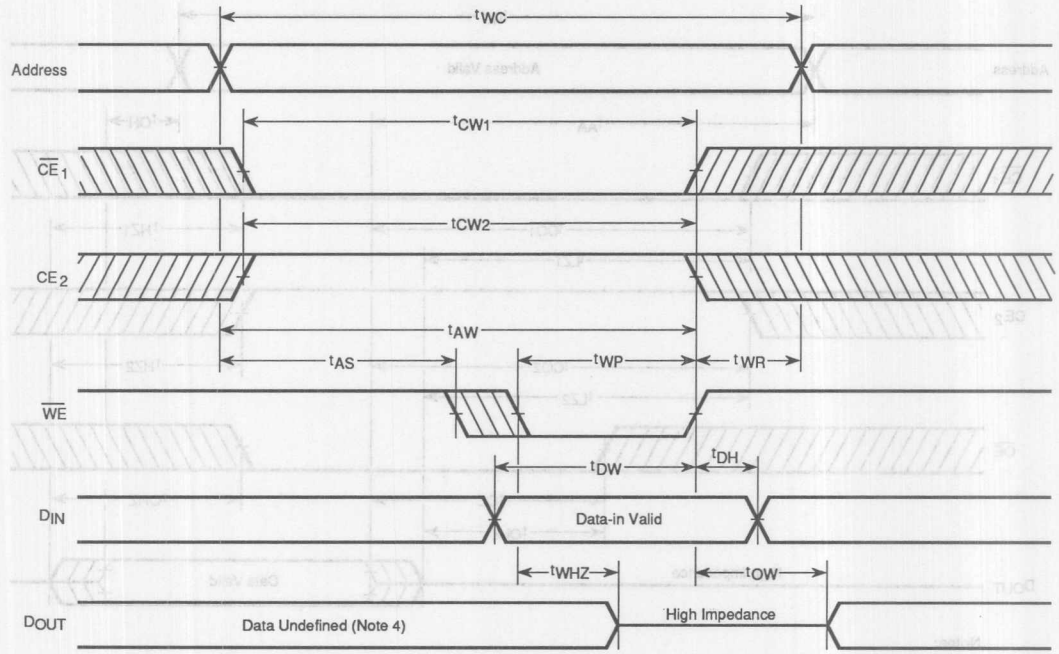
[2] Address valid prior to or coincident with the latter of the low transition of $\overline{CE}_1$ or the high transition of CE_2.

83IH-5745B

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Timing Waveforms (cont)

$\overline{WE}$-Controlled Write Cycle



Notes:

[1] A write cycle occurs during the overlap of a low $\overline{CE}_1$ and $\overline{WE}$ and a high CE_2.

[2] $\overline{CE}_1$ or $\overline{WE}$ must be high or CE_2 must be low during address transition.

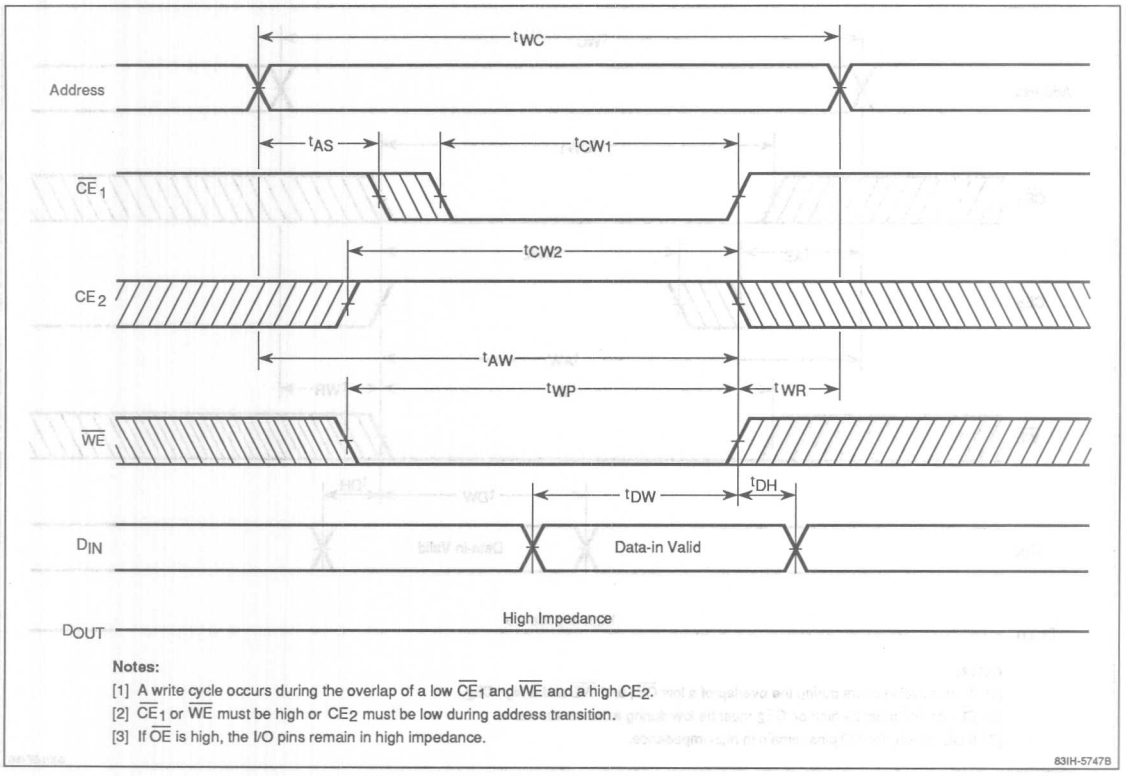
[3] If $\overline{OE}$ is high, the I/O pins remain in high impedance.

[4] During this period, the I/O pins may be in the output state; therefore, input signals of opposite phase to the output must not be applied.

83IH-5746B

Timing Waveforms (cont)

$\overline{CE}_1$-Controlled Write Cycle



Notes:

[1] A write cycle occurs during the overlap of a low $\overline{CE}_1$ and $\overline{WE}$ and a high CE_2.

[2] $\overline{CE}_1$ or $\overline{WE}$ must be high or CE_2 must be low during address transition.

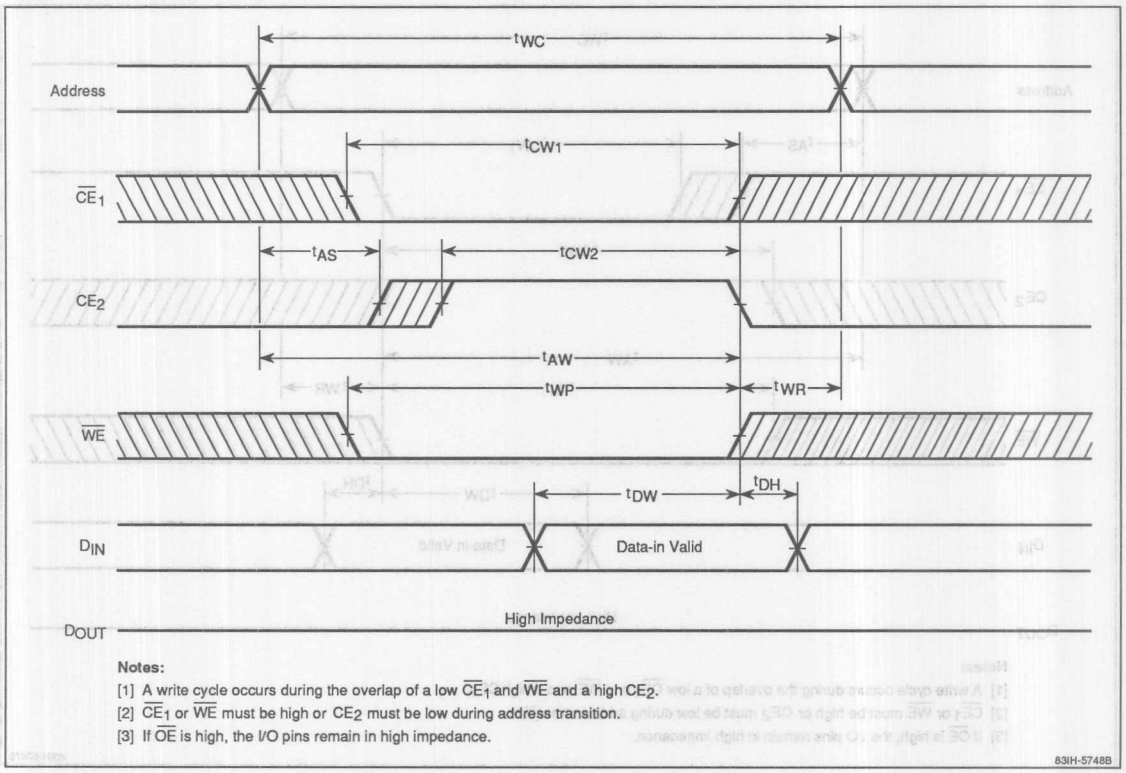
[3] If $\overline{OE}$ is high, the I/O pins remain in high impedance.

83IH-5747B

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Timing Waveforms (cont)

CE_2-Controlled Write Cycle



Notes:

[1] A write cycle occurs during the overlap of a low $\overline{CE}_1$ and $\overline{WE}$ and a high CE_2.

[2] $\overline{CE}_1$ or $\overline{WE}$ must be high or CE_2 must be low during address transition.

[3] If $\overline{OE}$ is high, the I/O pins remain in high impedance.

83IH-5748B

μPD431000A
131,072 x 8-Bit
Static CMOS RAM

Description

The μPD431000A is a 131,072-word by 8-bit static RAM fabricated with advanced silicon-gate technology. CMOS peripheral circuits and N-channel memory cells with polysilicon resistors make the μPD431000A a high-speed device that requires very low power and no clock or refreshing.

Minimum standby power is drawn when CE_2 is low, independent of the other inputs' levels. Data retention is guaranteed at a power supply voltage as low as 2 volts. The μPD431000A is available in standard 32-pin plastic DIP, 32-pin plastic miniflat, and 32-pin plastic TSOP packaging.

Features

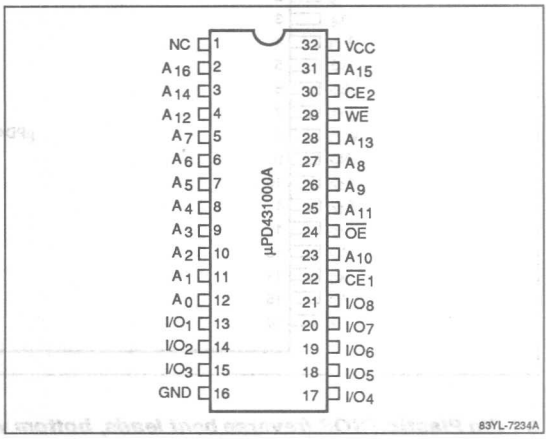
- 131,072-word by 8-bit organization
- Single + 5-volt power supply
- Fully static operation—no clock or refreshing
- TTL-compatible inputs and outputs
- Common I/O using three-state outputs
- Two CE pins and one $\overline{OE}$ pin for easy application
- Data retention current of 1 μA typical
- Data retention voltage of 2 V minimum
- Standard 32-pin plastic DIP, miniflat and TSOP packaging

Pin Identification

Symbol	Function
A_0 - A_{16}	Address inputs
I/O_0 - I/O_7	Data inputs/outputs
$\overline{CE}_1$, CE_2	Chip enables 1 and 2
$\overline{OE}$	Output enable
$\overline{WE}$	Write enable
GND	Ground
V_{CC}	+5-volt power supply
NC	No connection

Pin Configurations

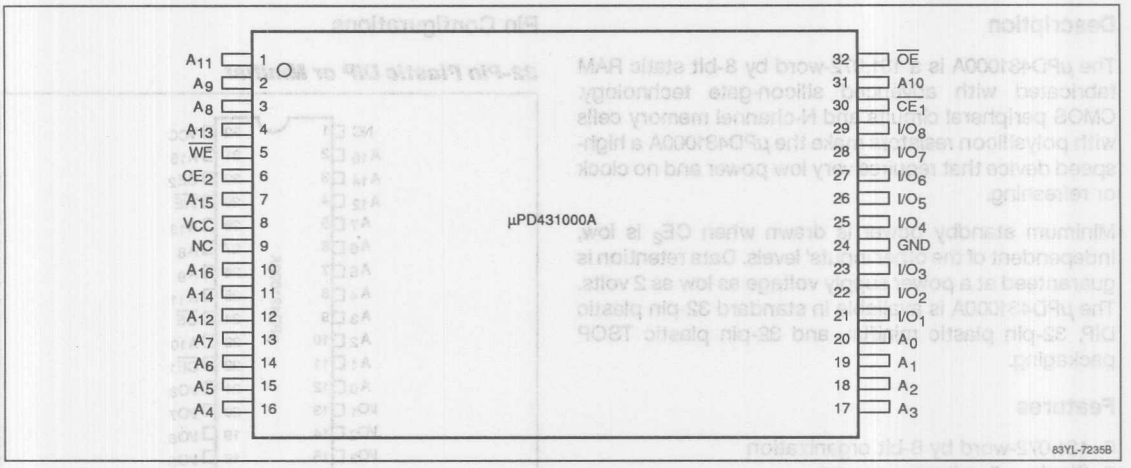
32-Pin Plastic DIP or Miniflat



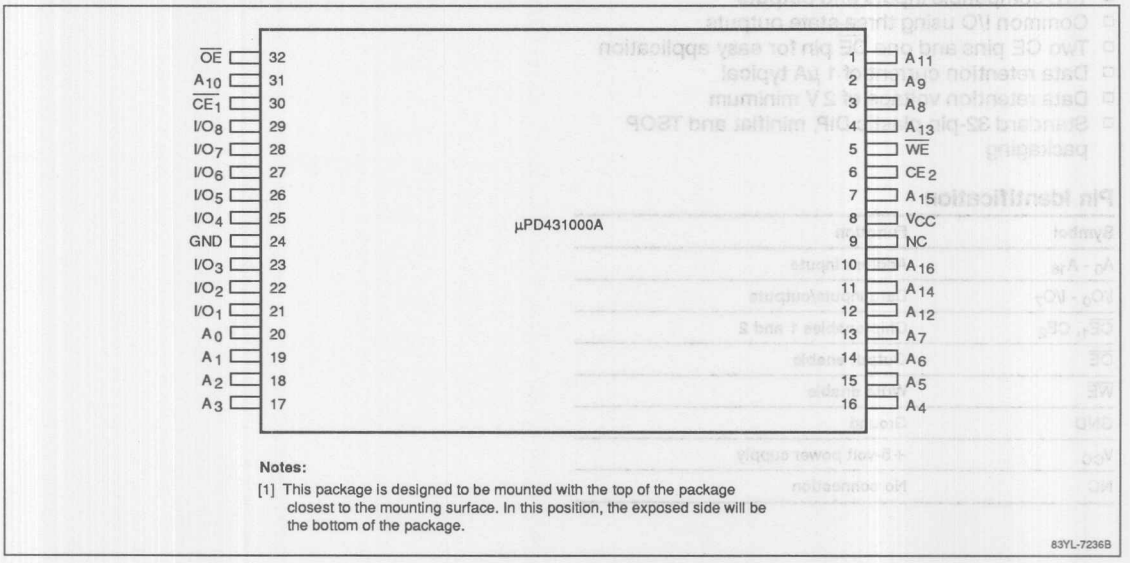
7

Pin Configurations (cont)

32-Pin Plastic TSOP (normal leads, top view)



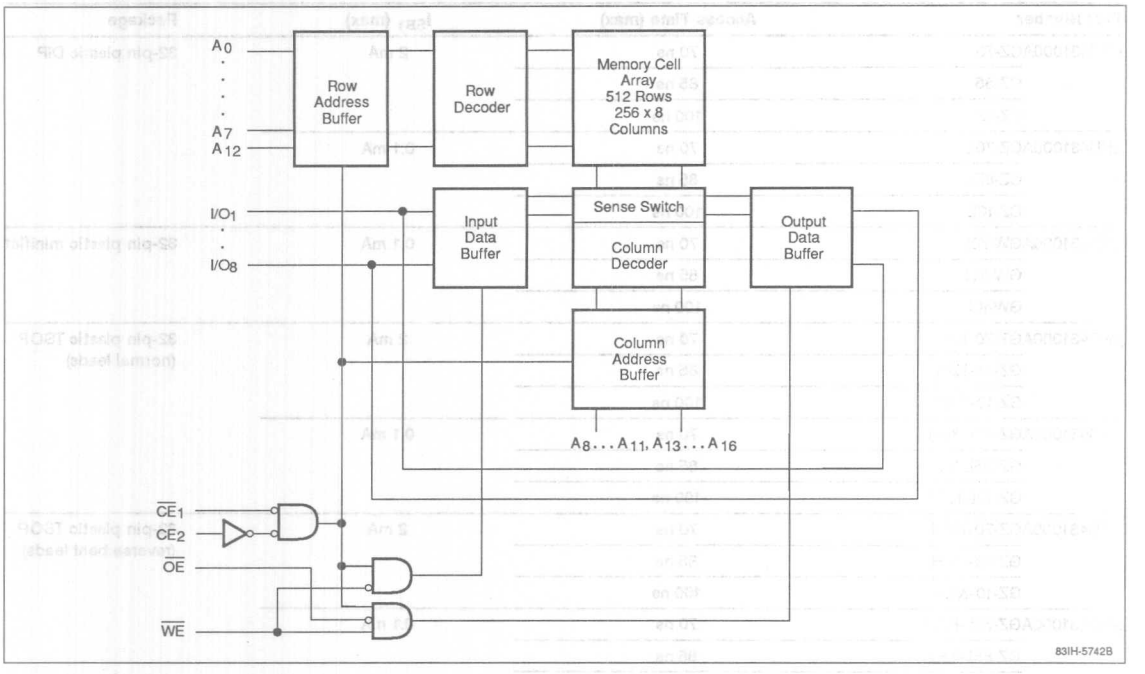
32-Pin Plastic TSOP (reverse bent leads, bottom view)



Notes:

[1] This package is designed to be mounted with the top of the package closest to the mounting surface. In this position, the exposed side will be the bottom of the package.

Block Diagram



Absolute Maximum Ratings

Supply voltage, V_{CC} (Note 1)	−0.5 to +7.0 V
Input voltage, V_{IN} (Note 1)	−0.5 to V_{CC} + 0.5 V
Output voltage, $V_{I/O}$ (Note 1)	−0.5 to V_{CC} + 0.5 V
Operating temperature, T_{OPR}	0 to +70°C
Storage temperature, T_{STG}	−55 to +125°C
Power dissipation, P_D	1.0 W

Exposure to Absolute Maximum Ratings for extended periods may affect device reliability; exceeding the ratings could cause permanent damage. The device should be operated within the limits specified under DC and AC Characteristics.

Notes:

(1) −3.0 V minimum (pulse width = 50 ns).

Capacitance

T_A = +25°C; f = 1 MHz; V_{IN} and V_{OUT} = 0 V

Parameter	Symbol	Min	Typ	Max	Unit
Input capacitance	C_I			6	pF
Input/output capacitance	$C_{I/O}$			10	pF

Notes:

(1) This parameter is sampled and not 100% tested.

Recommended Operating Conditions

Parameter	Symbol	Min	Typ	Max	Unit
Supply voltage	V_{CC}	4.5	5.0	5.5	V
Input voltage, low	V_{IL}	−0.3		0.8	V
Input voltage, high	V_{IH}	2.2		V_{CC} + 0.5	V
Ambient temperature	T_A	0		70	°C

Notes:

(1) −3.0 V minimum (pulse width = 50 ns).

Truth Table

Function	$\overline{CE}_1$	CE_2	$\overline{OE}$	$\overline{WE}$	I/O	I_{CC}
Not selected	H	X	X	X	High-Z	Standby
Not selected	X	L	X	X	High-Z	Standby
Selected	L	H	H	H	High-Z	Active
Read	L	H	L	H	D_{OUT}	Active
Write	L	H	X	L	D_{IN}	Active

Notes:

(1) X = don't care.

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Ordering Information

Part Number	Access Time (max)	I_{SB1} (max)	Package
μPD431000ACZ-70	70 ns	2 mA	32-pin plastic DIP
CZ-85	85 ns		
CZ-10	100 ns		
μPD431000ACZ-70L	70 ns	0.1 mA	
CZ-85L	85 ns		
CZ-10L	100 ns		
μPD431000AGW-70L	70 ns	0.1 mA	32-pin plastic miniflat
GW-85L	85 ns		
GW-10L	100 ns		
μPD431000AGZ-70-KJH	70 ns	2 mA	32-pin plastic TSOP (normal leads)
GZ-85-KJH	85 ns		
GZ-10-KJH	100 ns		
μPD431000AGZ-70L-KJH	70 ns	0.1 mA	
GZ-85L-KJH	85 ns		
GZ-10L-KJH	100 ns		
μPD431000AGZ-70-KKH	70 ns	2 mA	32-pin plastic TSOP (reverse bent leads)
GZ-85-KKH	85 ns		
GZ-10-KKH	100 ns		
μPD431000AGZ-70L-KKH	70 ns	0.1 mA	
GZ-85L-KKH	85 ns		
GZ-10L-KKH	100 ns		

Notes:

(1) Contact your NEC sales representative for data sheet and product availability for the -LL version of the μPD431000A.

DC Characteristics

T_A = 0 to +70°C; V_{CC} = +5.0 V ± 10%

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions
Input leakage current	I_{LI}	−1		1	μA	V_{IN} = 0 V to V_{CC}
I/O leakage current	I_{LO}	−1		1	μA	$V_{I/O}$ = 0 V to V_{CC}; $\overline{CE}_1$ = V_{IH}, or CE_2 = V_{IL}, or $\overline{OE}$ = V_{IH}, or $\overline{WE}$ = V_{IL}
Operating supply current	I_{CCA1}		40	70	mA	$\overline{CE}_1$ = V_{IL}; CE_2 = V_{IH}; t_{RC} = t_{RC} (min); $I_{I/O}$ = 0 mA
	I_{CCA2}			15	mA	$\overline{CE}_1$ = V_{IL}; CE_2 = V_{IH}; $I_{I/O}$ = 0 mA
	I_{CCA3}			10	mA	V_{CE1} ≤ 0.2 V; V_{CE2} ≥ V_{CC} − 0.2 V; t_{RC} or t_{WC} = 1 MHz; V_{IN} ≤ 0.2 V or V_{IN} ≥ V_{CC} − 0.2 V
Standby supply current	I_{SB}			5	mA	$\overline{CE}_1$ = V_{IH} or CE_2 = V_{IL} (Note 1)
	I_{SB1}		0.02	2	mA	$\overline{CE}_1$ and CE_2 ≥ V_{CC} − 0.2 V (Note 2)
	I_{SB2}		0.02	2	mA	CE_2 ≤ 0.2 V (Note 2)
Output voltage, low	V_{OL}			0.4	V	I_{OL} = 2.1 mA
Output voltage, high	V_{OH}	2.4			V	I_{OH} = −1.0 mA

Notes:

(1) I_{SB} = 3 mA (max) for -L versions.

(2) I_{SB1} and I_{SB2} = 0.02 mA (typ) and 0.1 mA (max) for -L versions.

AC Characteristics

T_A = 0 to +70°C; V_{CC} = +5.0 V ± 10%

Parameter	Symbol	μPD431000A-70 Min	μPD431000A-70 Max	μPD431000A-85 Min	μPD431000A-85 Max	μPD431000A-10 Min	μPD431000A-10 Max	Unit	Test Conditions
Read Operation									
Read cycle time	t_{RC}	70		85		100		ns	
Address access time	t_{AA}		70		85		100	ns	(Note 2)
$\overline{CE}_1$ access time	t_{CO1}		70		85		100	ns	(Note 2)
CE_2 access time	t_{CO2}		70		85		100	ns	(Note 2)
Output enable to output valid	t_{OE}		35		45		50	ns	(Note 2)
Output hold from address change	t_{OH}	10		10		10		ns	
$\overline{CE}_1$ to output in low-Z	t_{LZ1}	10		10		10		ns	(Note 3)
CE_2 to output in low-Z	t_{LZ2}	10		10		10		ns	(Note 3)
Output enable to output in low-Z	t_{OLZ}	5		5		5		ns	(Note 3)
$\overline{CE}_1$ to output in high-Z	t_{HZ1}		25		30		35	ns	(Note 3)
CE_2 to output in high-Z	t_{HZ2}		25		30		35	ns	(Note 3)
Output enable to output in high-Z	t_{OHZ}		25		30		35	ns	(Note 3)
Write Operation									
Write cycle time	t_{WC}	70		85		100		ns	
$\overline{CE}_1$ to end of write	t_{CW1}	60		75		90		ns	
CE_2 to end of write	t_{CW2}	60		75		90		ns	
Address valid to end of write	t_{AW}	60		75		90		ns	
Address setup time	t_{AS}	0		0		0		ns	
Write pulse width	t_{WP}	55		65		75		ns	
Write recovery time	t_{WR}	5		5		5		ns	
Data valid to end of write	t_{DW}	35		35		40		ns	
Data hold time	t_{DH}	0		0		0		ns	
Write enable to output in high-Z	t_{WHZ}		25		30		35	ns	(Note 3)
Output active from end of write	t_{OW}	5		5		5		ns	(Note 3)

Notes:

(1) Input pulse levels = 0.8 to 2.2 V; input rise and fall times = 5 ns; timing reference levels = 1.5 V.

(2) See figure 1 for output loading.

(3) See figure 2 for output loading.

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Figure 1. Output Loading

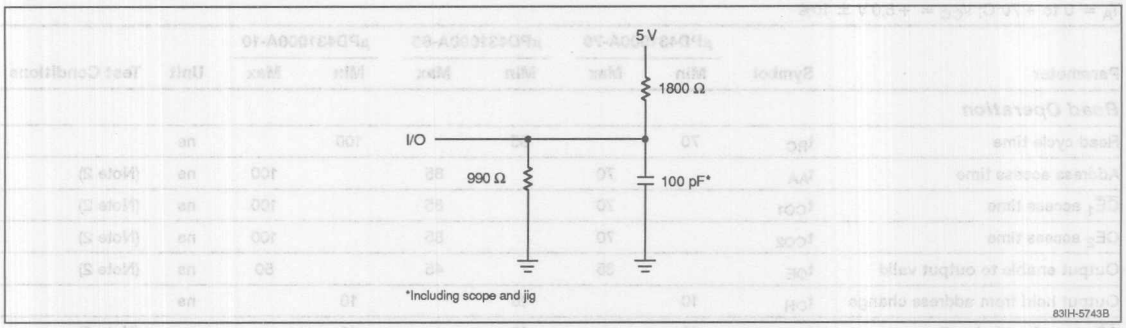
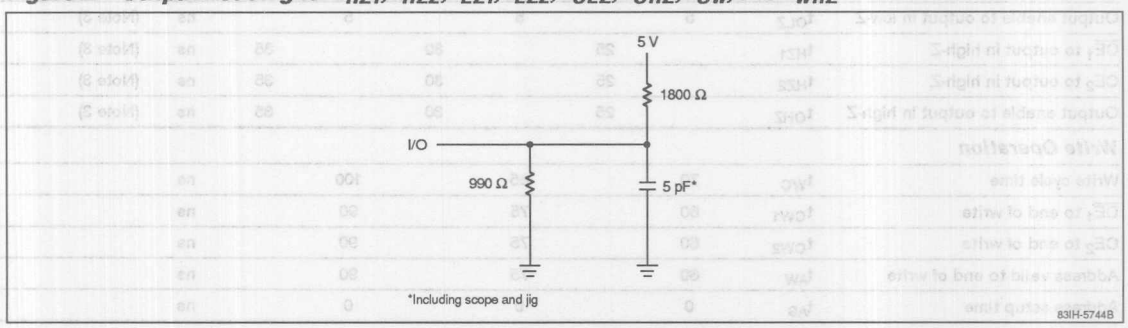


Figure 2. Output Loading for t_{HZ1}, t_{HZ2}, t_{LZ1}, t_{LZ2}, t_{OLZ}, t_{OHZ}, t_{OW}, and t_{WHZ}



Low V_{CC} Data Retention Characteristics (-L Version Only)

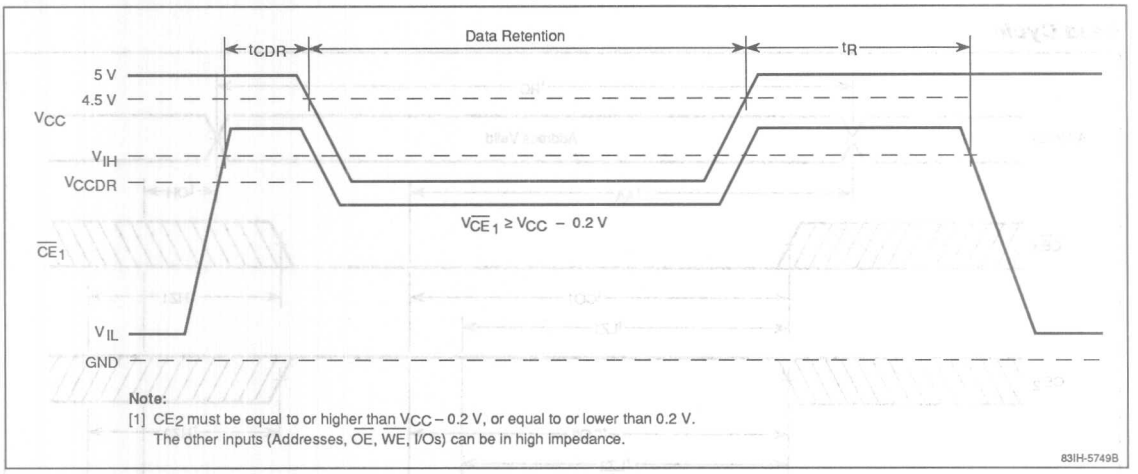
T_A = 0 to +70°C

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions
Data retention supply voltage	V_{CCDR1}	2		5.5	V	$\overline{CE_1} \geq V_{CC} - 0.2$ V; $CE_2 \geq V_{CC} - 0.2$ V or $CE_2 \leq 0.2$ V
	V_{CCDR2}	2		5.5	V	$CE_2 \leq 0.2$ V
Data retention supply current	I_{CCDR1}		1	50	μA	V_{CC} = 3.0 V; $\overline{CE_1} \geq V_{CC} - 0.2$ V; $CE_2 \geq V_{CC} - 0.2$ V or $CE_2 \leq 0.2$ V (Note 1)
	I_{CCDR2}		1	50	μA	V_{CC} = 3.0 V; $CE_2 \leq 0.2$ V (Note 1)
Chip deselection to data retention	t_{CDR}	0			ns	
Operation recovery time	t_R	5			ms	

Notes:

(1) At 0 to 40°C, the maximum for I_{CCDR1} and I_{CCDR2} is 15 μA.

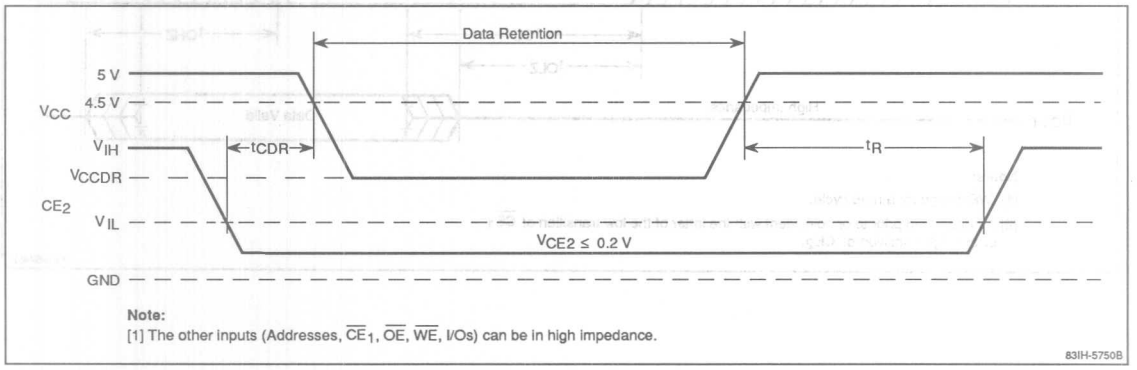
Figure 3. $\overline{CE_1}$-Controlled Data Retention Timing



Note:
[1] CE_2 must be equal to or higher than V_{CC} − 0.2 V, or equal to or lower than 0.2 V.
The other inputs (Addresses, $\overline{OE}$, $\overline{WE}$, I/Os) can be in high impedance.

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Figure 4. CE_2-Controlled Data Retention Timing



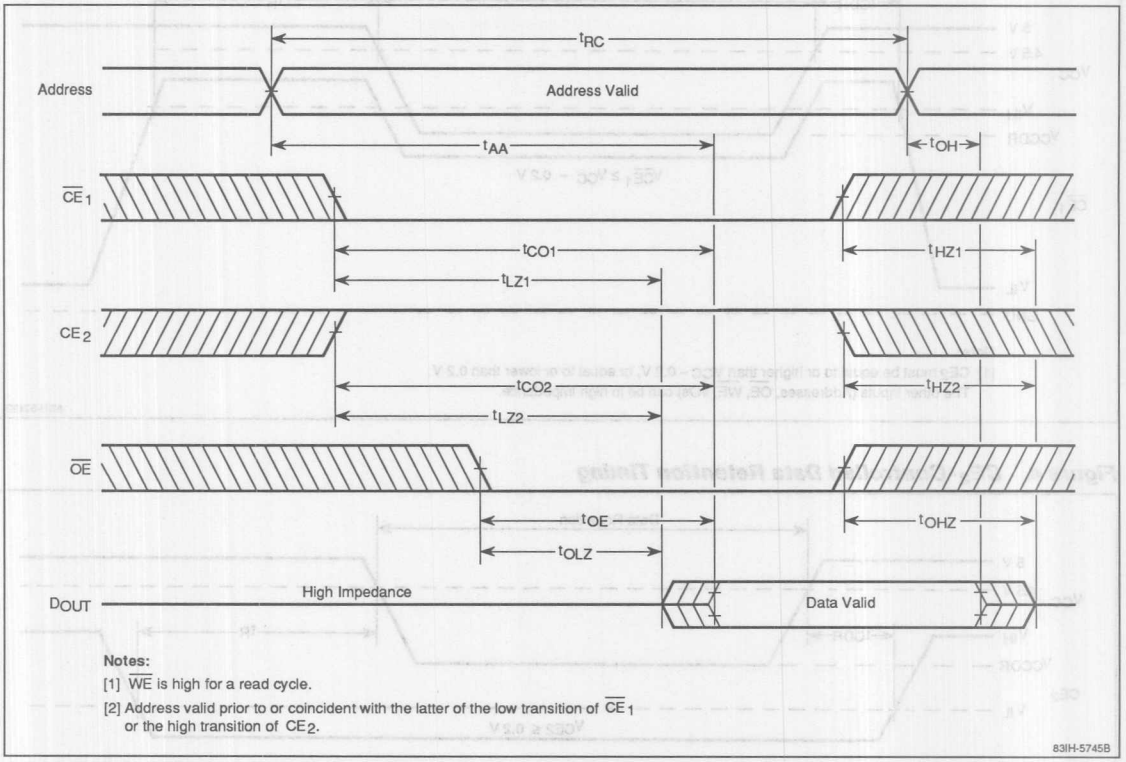
Note:
[1] The other inputs (Addresses, $\overline{CE_1}$, $\overline{OE}$, $\overline{WE}$, I/Os) can be in high impedance.

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Timing Waveforms

Read Cycle



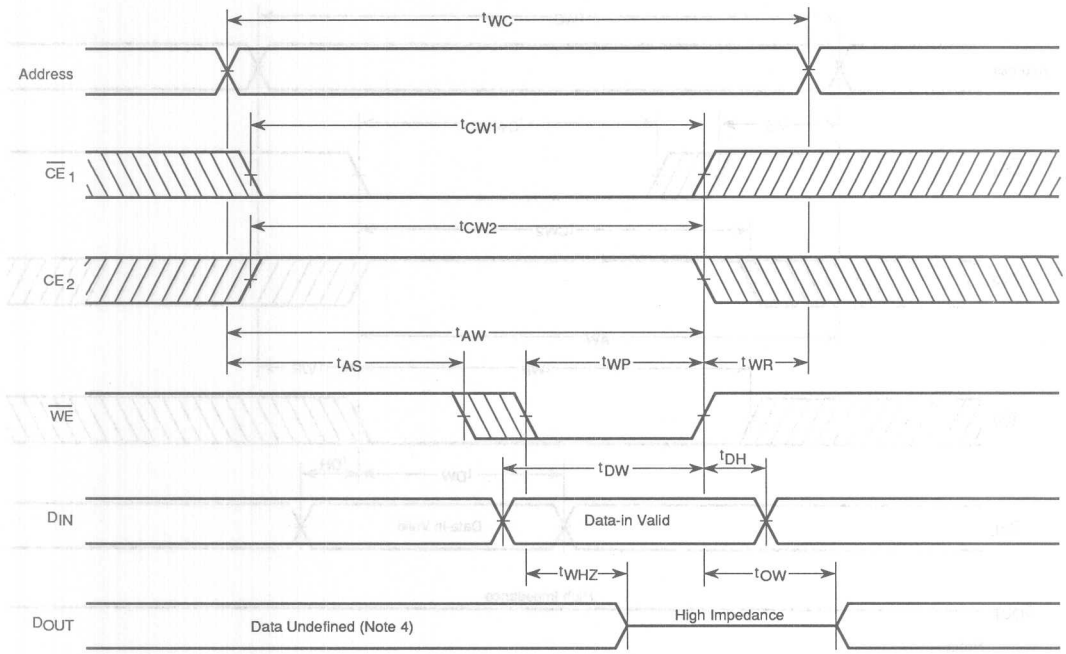
Notes:

[1] $\overline{WE}$ is high for a read cycle.

[2] Address valid prior to or coincident with the latter of the low transition of $\overline{CE}_1$ or the high transition of CE_2.

Timing Waveforms (cont)

$\overline{WE}$-Controlled Write Cycle



Notes:

[1] A write cycle occurs during the overlap of a low $\overline{CE}_1$ and $\overline{WE}$ and a high CE_2.

[2] $\overline{CE}_1$ or $\overline{WE}$ must be high or CE_2 must be low during address transition.

[3] If $\overline{OE}$ is high, the I/O pins remain in high impedance.

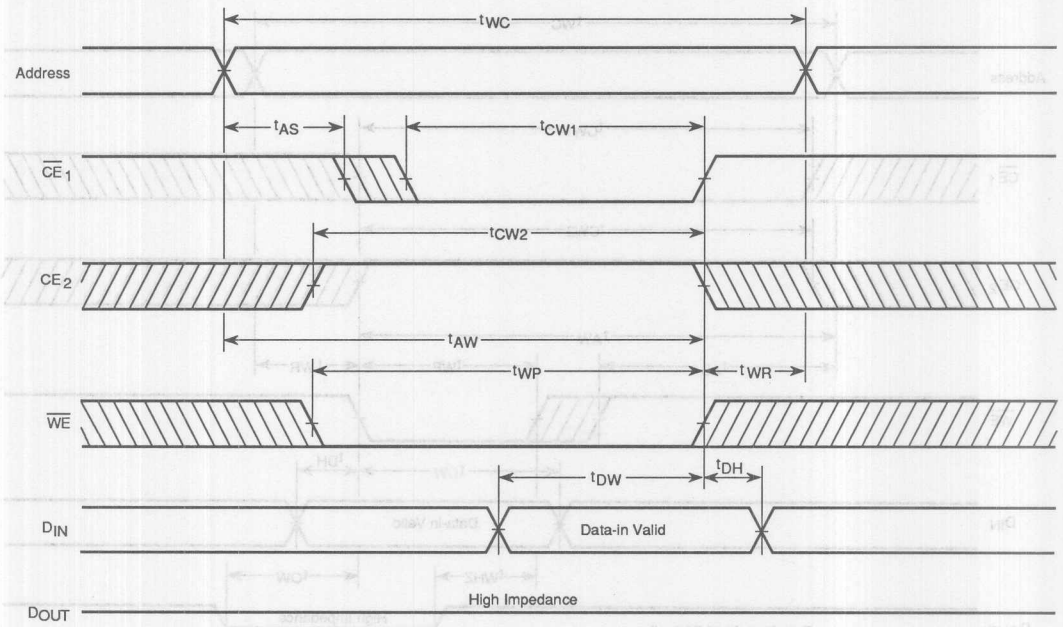
[4] During this period, the I/O pins may be in the output state; therefore, input signals of opposite phase to the output must not be applied.

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Timing Waveforms (cont)

$\overline{CE}_1$-Controlled Write Cycle



Notes:

[1] A write cycle occurs during the overlap of a low $\overline{CE}_1$ and $\overline{WE}$ and a high CE_2.

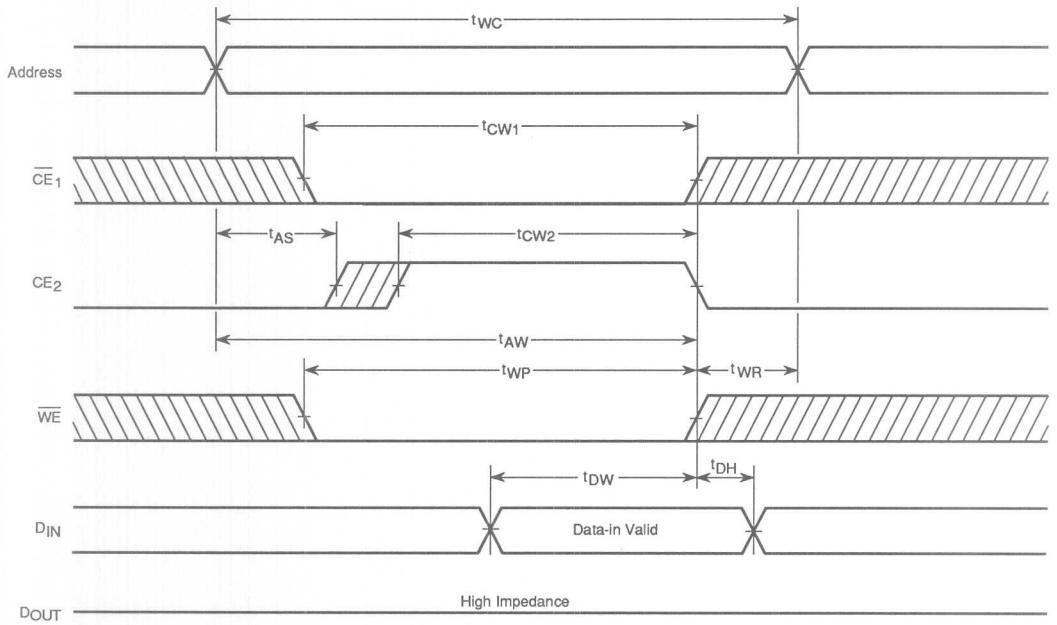
[2] $\overline{CE}_1$ or $\overline{WE}$ must be high or CE_2 must be low during address transition.

[3] If $\overline{OE}$ is high, the I/O pins remain in high impedance.

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Timing Waveforms (cont)

CE_2-Controlled Write Cycle



Notes:

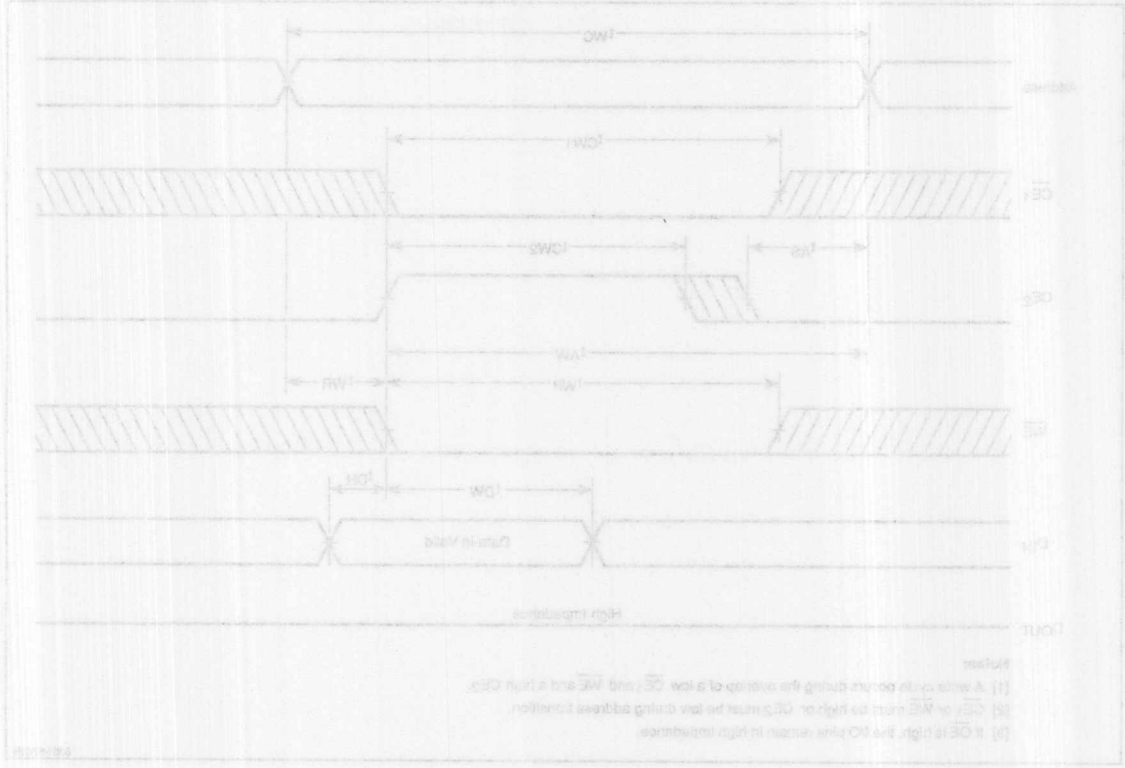
[1] A write cycle occurs during the overlap of a low $\overline{CE}_1$ and $\overline{WE}$ and a high CE_2.

[2] $\overline{CE}_1$ or $\overline{WE}$ must be high or CE_2 must be low during address transition.

[3] If $\overline{OE}$ is high, the I/O pins remain in high impedance.

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PRELIMINARY INFORMATION

Description

The μPD431001 is a 1,084,576-word by 1-bit static RAM fabricated with advanced silicon-gate technology. A unique design that uses CMOS peripheral circuits and N-channel memory cells with polysilicon resistors makes the μPD431001 a high-speed device that requires no clock or refreshing. The μPD431001 is available in 28-pin plastic SOJ packaging.

Features

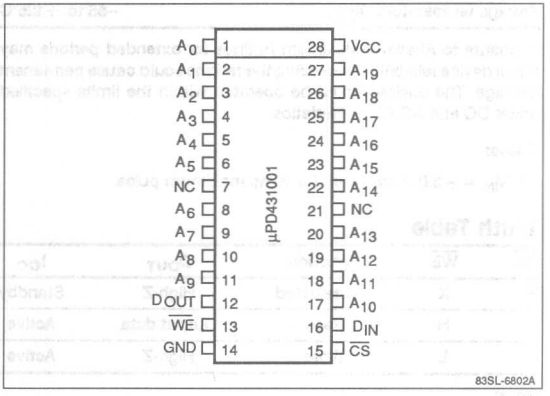
- 1,048,576-word x 1-bit organization
- Single +5-volt power supply
- Fully static operation—no clock or refreshing
- TTL-compatible inputs and outputs
- Separated data input and output
- Three-state outputs
- Power dissipation
  - — 120 mA max (active)
  - — 2 mA max (standby)
- Standard 400-mil, 28-pin plastic SOJ packaging

Ordering Information

Part Number	Access Time (max)	Package
μPD431001LE-25	25 ns	28-pin plastic SOJ
LE-35	35 ns	

Pin Configuration

28-Pin Plastic SOJ



Pin Identification

Symbol	Function
A_0 - A_{19}	Address inputs
D_{IN}	Data input
D_{OUT}	Data output
$\overline{CS}$	Chip select
$\overline{WE}$	Write enable
GND	Ground
V_{CC}	+5-volt power supply
NC	No connection

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Absolute Maximum Ratings

Power supply voltage, V_{CC}	−0.5 to +7.0 V
Input voltage, V_{IN} (Note 1)	−0.5 to V_{CC} + 0.3 V
Output voltage, V_{OUT}	−0.5 to V_{CC} + 0.3 V
Operating temperature, T_{OPR}	0 to +70°C
Storage temperature, T_{STG}	−55 to +125°C

Exposure to Absolute Maximum Ratings for extended periods may affect device reliability; exceeding the ratings could cause permanent damage. The device should be operated within the limits specified under DC and AC Characteristics.

Notes:

(1) V_{IN} = −3.0 V minimum for 10 ns maximum pulse.

Truth Table

$\overline{CS}$	$\overline{WE}$	Function	D_{OUT}	I_{CC}
H	X	Not selected	High-Z	Standby
L	H	Read	Output data	Active
L	L	Write	High-Z	Active

Note:

(1) X = don't care

Capacitance

T_A = +25°C; f = 1 MHz (Note 1); V_{IN} and V_{OUT} = 0 V

Parameter	Symbol	Min	Typ	Max	Unit
Input capacitance	C_I			6	pF
Output capacitance	C_O			10	pF

Notes:

(1) This parameter is sampled and not 100% tested.

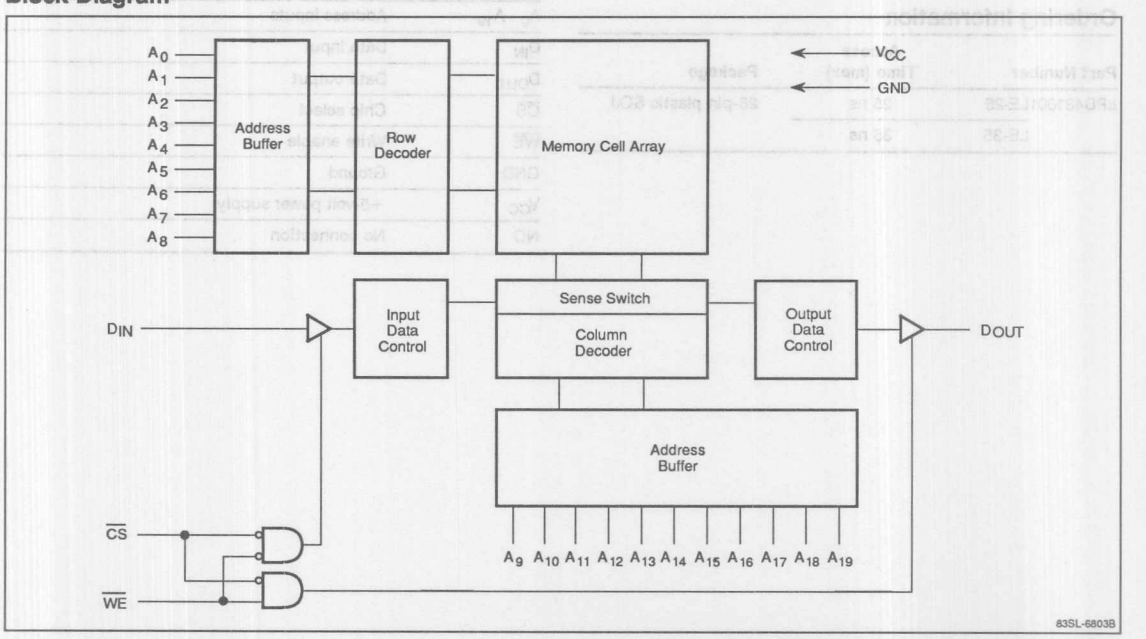
Recommended Operating Conditions

Parameter	Symbol	Min	Typ	Max	Unit
Supply voltage	V_{CC}	4.5	5.0	5.5	V
Input voltage, low	V_{IL}	−0.5		0.8	V
Input voltage, high	V_{IH}	2.2		V_{CC} + 0.3	V
Ambient temperature	T_A	0		70	°C

Note:

(1) V_{IL} = −3.0 V minimum for 10 ns maximum pulse.

Block Diagram



DC Characteristics

T_A = 0 to +70°C; V_{CC} = +5.0 V ± 10%

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions
Input leakage current	I_{LI}	−2		2	μA	V_{IN} = 0 V to V_{CC}
Output leakage current	I_{LO}	−2		2	μA	V_{OUT} = 0 V to V_{CC}; $\overline{CS}$ = V_{IH} or $\overline{WE}$ = V_{IL}
Operating supply current	I_{CC}			120	mA	$\overline{CS}$ = V_{IL}; t_{RC} = t_{RC} (min); I_{OUT} = 0 mA (Note 1)
Standby supply current	I_{SB}			30	mA	$\overline{CS}$ = V_{IH}; V_{IN} = V_{IH} or V_{IL}
	I_{SB1}			2	mA	$\overline{CS}$ ≥ V_{CC} − 0.2 V; V_{IN} ≤ 0.2 V or ≥ V_{CC} − 0.2 V
Output voltage, low	V_{OL}			0.4	V	I_{OL} = 8.0 mA
Output voltage, high	V_{OH}	2.4			V	I_{OH} = −4.0 mA

Note:

(1) I_{CC} = 100 mA (max) for the μPD431001-35.

AC Characteristics

T_A = 0 to +70°C; V_{CC} = +5.0 V ± 10%

		μPD431001-25		μPD431001-35			
Parameter	Symbol	Min	Max	Min	Max	Unit	Test Conditions (Note 1)
Read Operation							
Read cycle time	t_{RC}	25		35		ns	(Note 2)
Read access time	t_{AA}		25		35	ns	
Chip select access time	t_{ACS}		25		35	ns	
Output hold from address change	t_{OH}	5		5		ns	
Chip select to output in low-Z	t_{CLZ}	5		5		ns	(Note 3)
Chip deselect to output in high-Z	t_{CHZ}	0	10	0	15	ns	(Note 4)
Write Operation							
Write cycle time	t_{WC}	25		35		ns	(Note 2)
Chip select to end of write	t_{CW}	20		30		ns	
Address valid to end of write	t_{AW}	20		30		ns	
Address setup time	t_{AS}	0		0		ns	
Write pulse width	t_{WP}	20		25		ns	
Write recovery time	t_{WR}	0		0		ns	
Data valid to end of write	t_{DW}	15		20		ns	
Data hold time	t_{DH}	0		0		ns	
Write enable to output in high-Z	t_{WHZ}	0	10	0	15	ns	(Note 4)
Output active from end of write	t_{OW}	0		0		ns	(Note 3)

Notes:

(1) Input pulse levels = GND to 3.0 V; input pulse rise and fall time = 5 ns; timing reference levels = 1.5 V; see figures 1 and 2 for the output load.

(2) All read and write cycle timings are referenced from the last valid address to the first transitioning address.

(3) The transition is measured ±200 mV from steady-state voltage with the load shown in figure 2.

(4) The transition is measured at V_{OL} + 200 mV and V_{OH} − 200 mV with the load shown in figure 2.

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Figure 1. Output Load

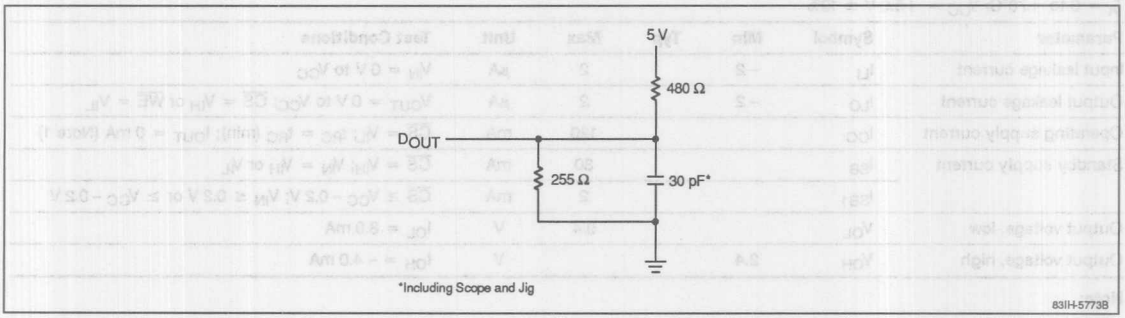
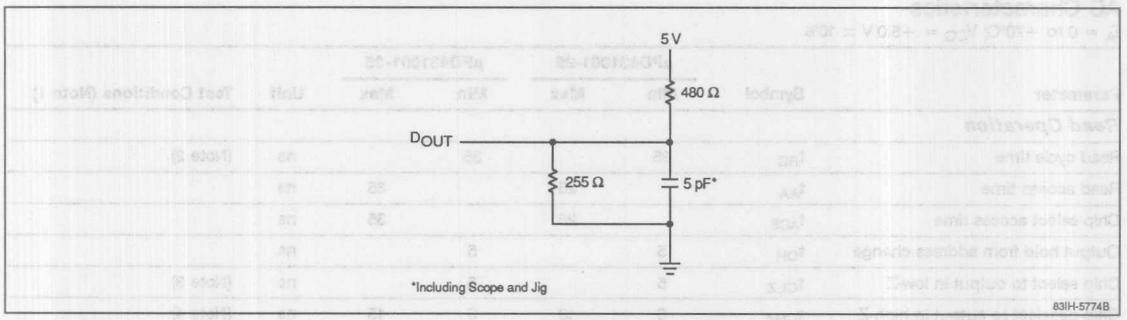
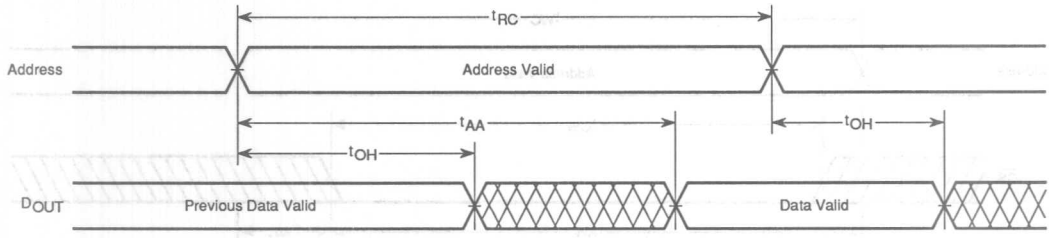


Figure 2. Output Load for t_{CHZ}, t_{CLZ}, t_{OW}, and t_{WHZ}



Timing Waveforms

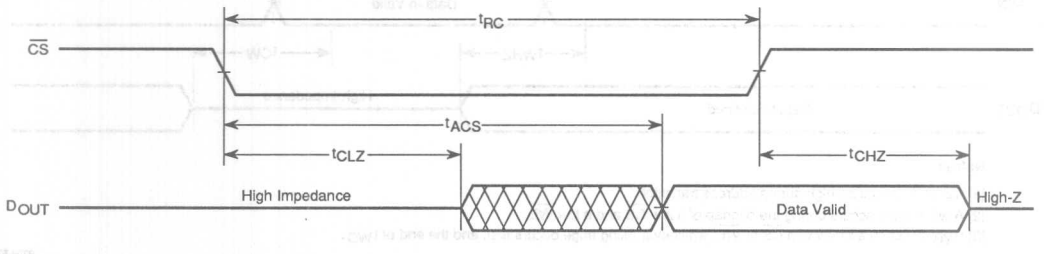
Address Access Cycle



Notes:
[1] $\overline{WE}$ is held high for a read cycle.
[2] The device is continually selected, where $\overline{CS} = V_{IL}$.

83IH-5775B

Chip Select Access Cycle



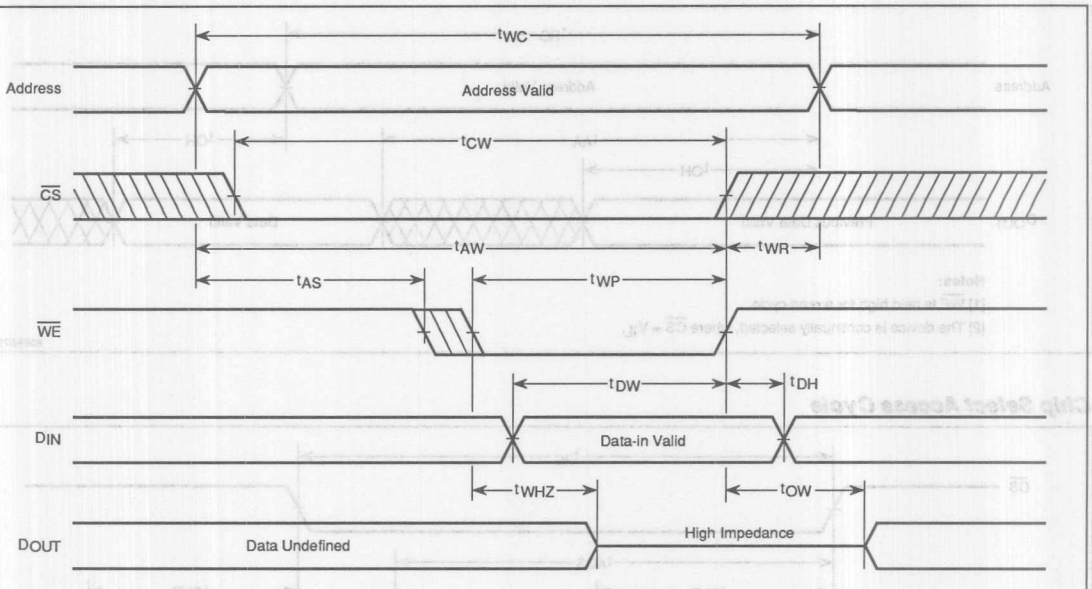
Notes:
[1] $\overline{WE}$ is held high for a read cycle.
[2] Address valid prior to or coincident with the low transition of $\overline{CS}$.

83IH-5776B

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Timing Waveforms (cont)

WE-Controlled Write Cycle



Notes:

[1] $\overline{CS}$ or $\overline{WE}$ must be high during address transition.

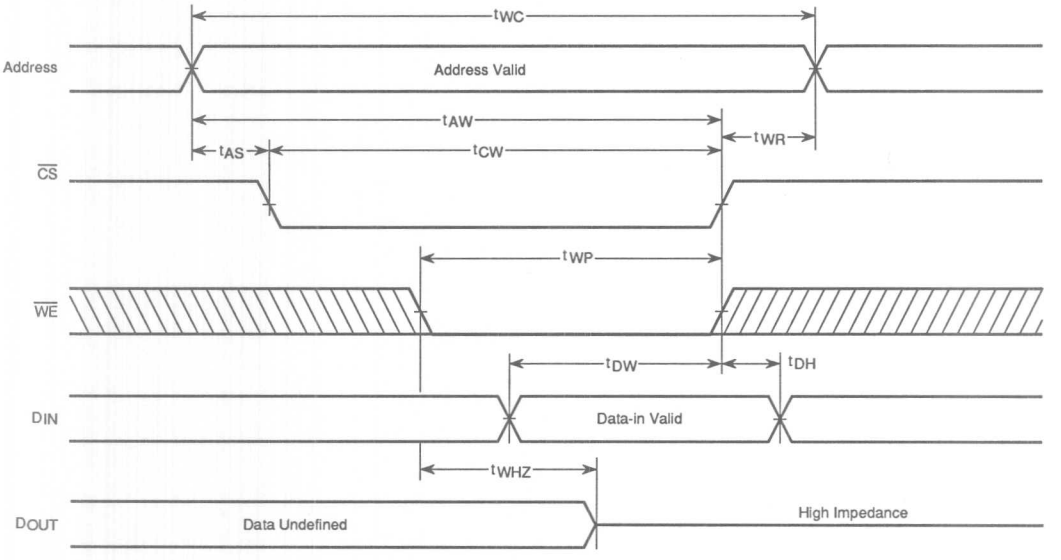
[2] A write cycle occurs during the overlap of a low $\overline{CS}$ and a low $\overline{WE}$.

[3] t_{WR} is measured between $\overline{CS}$ or $\overline{WE}$, whichever rising edge occurs first, and the end of t_{WC}.

83IH-5777B

Timing Waveforms (cont)

$\overline{CS}$-Controlled Write Cycle



Notes:

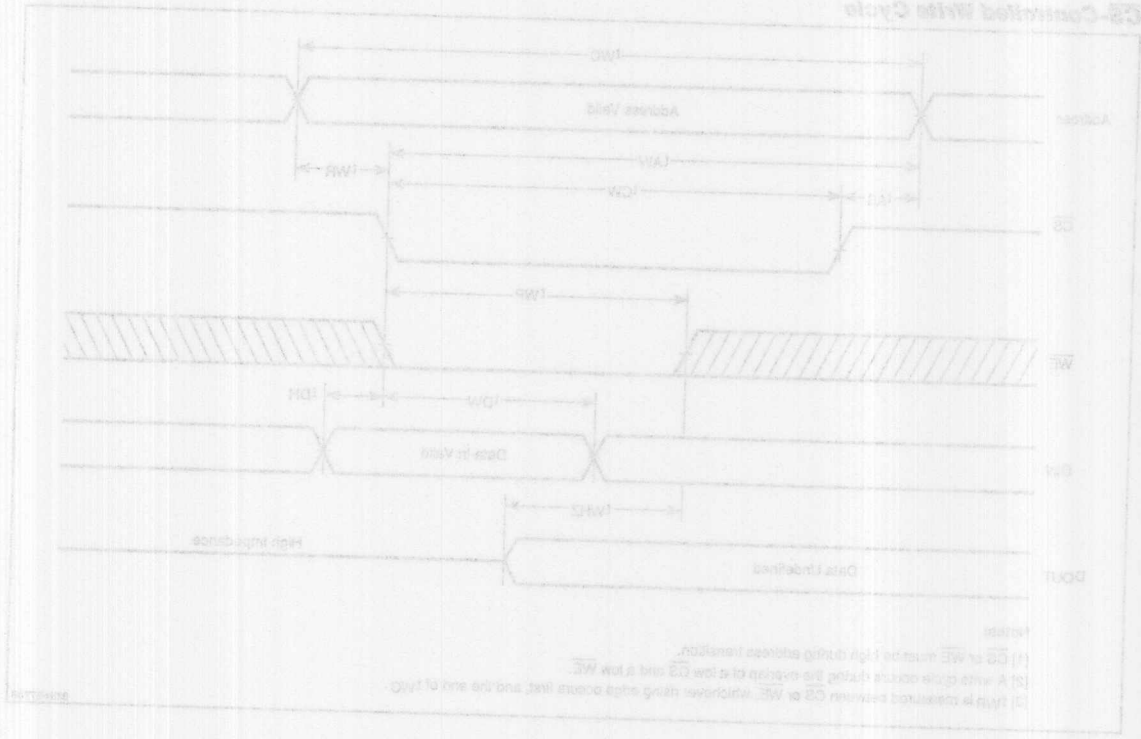
[1] $\overline{CS}$ or $\overline{WE}$ must be high during address transition.

[2] A write cycle occurs during the overlap of a low $\overline{CS}$ and a low $\overline{WE}$.

[3] t_{WR} is measured between $\overline{CS}$ or $\overline{WE}$, whichever rising edge occurs first, and the end of t_{WC}.

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Description

The μPD431004 is a 262,144-word by 4-bit static RAM fabricated with advanced silicon-gate technology. CMOS peripheral circuits and N-channel memory cells with polysilicon resistors make the μPD431004 a high-speed device that requires very low power and no clock or refreshing.

The μPD431004 is available in standard 28-pin plastic SOJ packaging.

Features

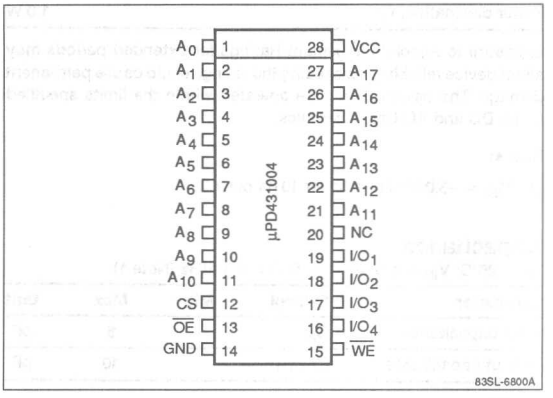
- 262,144-word x 4-bit organization
- Single +5-volt power supply
- Fully static operation—no clock or refreshing
- TTL-compatible inputs and outputs
- Common I/O capability
- Low power dissipation
  - 140 mA max (active)
  - 2 mA max (standby)
- Standard 28-pin plastic SOJ packaging

Ordering Information

Part Number	Access Time (max)	Package
μPD431004LE-25	25 ns	28-pin plastic SOJ
LE-35	35 ns	

Pin Configuration

28-Pin Plastic SOJ



Pin Identification

Symbol	Function
A_0 - A_{17}	Address inputs
I/O_1 - I/O_4	Data inputs and outputs
$\overline{CS}$	Chip select
$\overline{WE}$	Write enable
GND	Ground
V_{CC}	+5-volt power supply
NC	No connection

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Absolute Maximum Ratings

Supply voltage, V_{CC}	−0.5 to +7.0 V
Input and output voltages, V_{IN} (Note 1)	−0.5 to V_{CC} + 0.3
Operating temperature, T_{OPR}	0 to +70°C
Storage temperature, T_{STG}	−55 to +125°C
Power dissipation, P_D	1.0 W

Exposure to Absolute Maximum Ratings for extended periods may affect device reliability; exceeding the ratings could cause permanent damage. The device should be operated within the limits specified under DC and AC Characteristics.

Notes:

(1) V_{IN} = −3.0 V minimum for 10 ns pulse.

Capacitance

T_A = 25°C; V_{IN} and V_{DOUT} = 0 V; f = 1 MHz (Note 1)

Parameter	Symbol	Min	Max	Unit
Input capacitance	C_{IN}		6	pF
Output capacitance	C_{DOUT}		10	pF

Notes:

(1) This parameter is sampled and not 100% tested.

Truth Table

Function	$\overline{CS}$	$\overline{WE}$	$\overline{OE}$	Input/Output	I_{CC}
Not selected	H	X	X	High-Z	Standby
Output disable	L	H	H	High-Z	Active
Read	L	H	L	D_{OUT}	Active
Write	L	L	X	D_{IN}	Active

Notes:

(1) X = don't care.

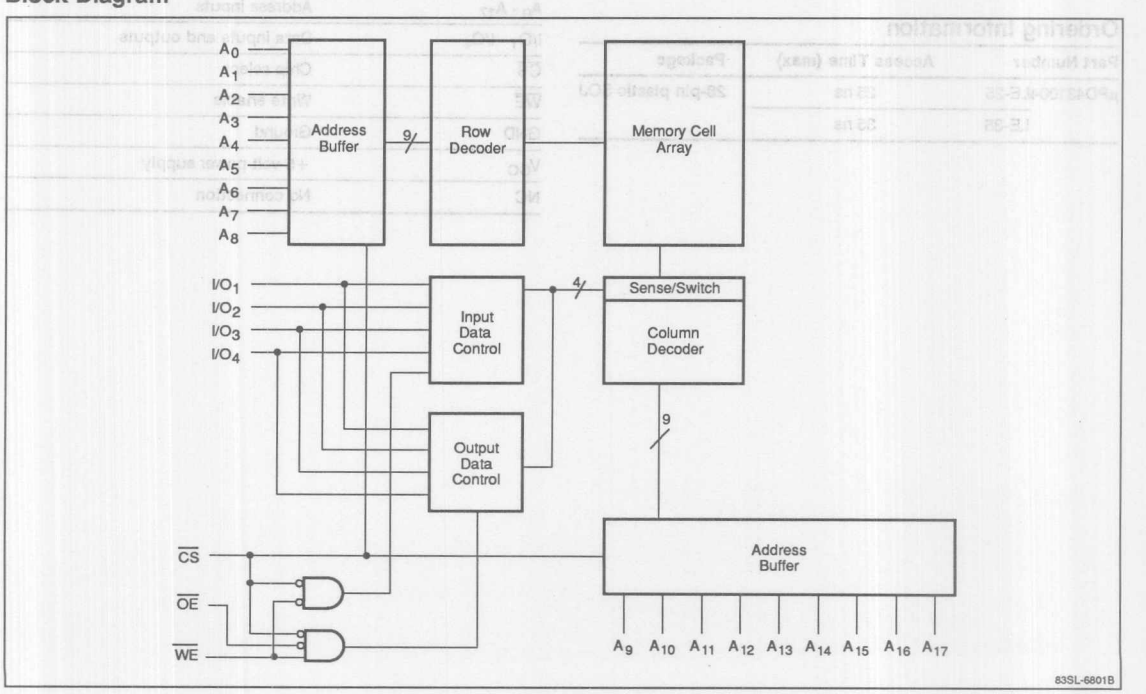
Recommended Operating Conditions

Parameter	Symbol	Min	Typ	Max	Unit
Supply voltage	V_{CC}	4.5	5.0	5.5	V
Input voltage, high	V_{IH}	2.2		V_{CC} + 0.3	V
Input voltage, low	V_{IL}	−0.5		0.8	V
Operating temperature	T_A	0		70	°C

Notes:

(1) V_{IL} = −3.0 V minimum for 10 ns pulse.

Block Diagram



DC Characteristics

T_A = 0 to +70°C; V_{CC} = +5.0 V ± 10%

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions
Input leakage current	I_{LI}	−2		2	μA	V_{IN} = 0 V to V_{CC}
Output leakage current	I_{LO}	−2		2	μA	V_{OUT} = 0 V to V_{CC}; $\overline{CS}$ = V_{IH} or $\overline{WE}$ = V_{IL} or $\overline{OE}$ = V_{IH}
Operating supply current	I_{CC}			140	mA	$\overline{CS}$ = V_{IL}; t_{RC} = t_{RC} (min); I_{DOUT} = 0 mA (Note 1)
Standby supply current	I_{SB}			30	mA	$\overline{CS}$ = V_{IH}
	I_{SB1}			2	mA	$\overline{CS}$ ≥ V_{CC} − 0.2 V; V_{IN} ≤ 0.2 V or ≥ V_{CC} − 0.2 V
Output voltage, low	V_{OL}			0.4	V	I_{OL} = 8.0 mA
Output voltage, high	V_{OH}	2.4			V	I_{OH} = −4.0 mA

Notes:

(1) I_{CC} = 120 mA (max) for the μPD431004-35.

AC Characteristics

T_A = 0 to +70°C; V_{CC} = +5.0 V ± 10%

		μPD431004-25		μPD431004-35			
Parameter	Symbol	Min	Max	Min	Max	Unit	Test Conditions
Read Operation							
Read cycle time	t_{RC}	25		35		ns	(Note 2)
Address access time	t_{AA}		25		35	ns	
Chip select access time	t_{ACS}		25		35	ns	
Output hold from address change	t_{OH}	5		5		ns	
Output enable access time	t_{OE}		10		15	ns	
Output enable to output in low-Z	t_{OLZ}	0		0		ns	(Note 3)
Output disable to output in high-Z	t_{OHZ}	0	10	0	15	ns	(Note 4)
Chip selection to output in low-Z	t_{CLZ}	5		5		ns	(Note 3)
Chip selection to output in high-Z	t_{CHZ}	0	10	0	15	ns	(Note 4)
Write Operation							
Write cycle time	t_{WC}	25		35		ns	(Note 2)
Chip select to end of write	t_{CW}	20		30		ns	
Address valid to end of write	t_{AW}	20		30		ns	
Address setup time	t_{AS}	0		0		ns	
Write pulse width	t_{WP}	20		30		ns	
Write recovery time	t_{WR}	3		3		ns	
Data valid to end of write	t_{DW}	12		20		ns	
Data hold time	t_{DH}	0		0		ns	
Write enable to output in high-Z	t_{WHZ}	0	8	0	10	ns	(Note 4)
Output active from end of write	t_{OW}	0		0		ns	(Note 3)

Notes:

(1) Input pulse levels = GND to 3.0 V; input pulse rise and fall times = 3 ns; timing reference levels = 1.5 V; see figures 1 and 2 for output load.

(2) All read cycle timings are referenced from the last valid address to the first transitioning address.

(3) Transition is measured at ±200 mV from steady-state voltage with the load shown in figure 2.

(4) Transition is measured at V_{OL} + 200 mV and V_{OH} − 200 mV with the load shown in figure 2.

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Figure 1. Output Load

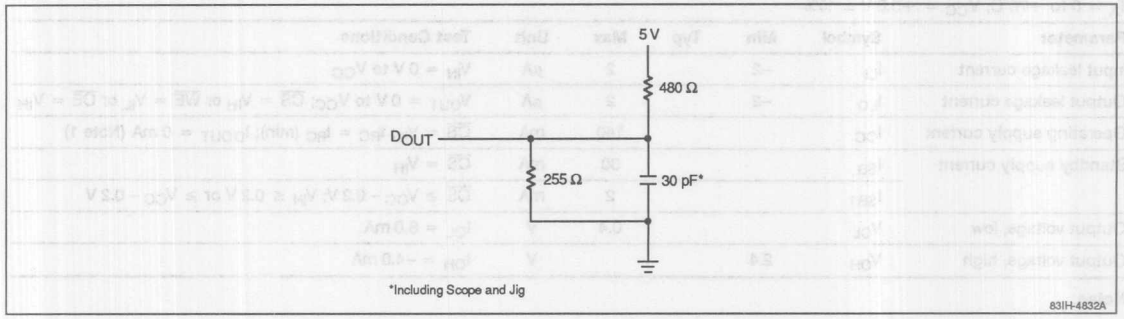
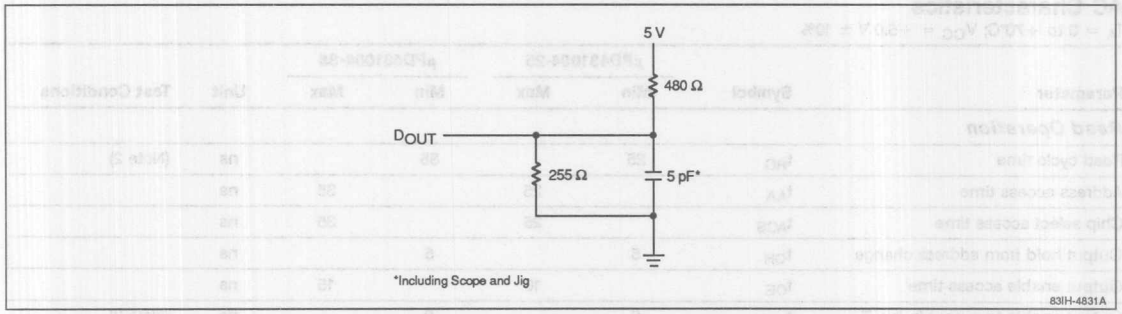
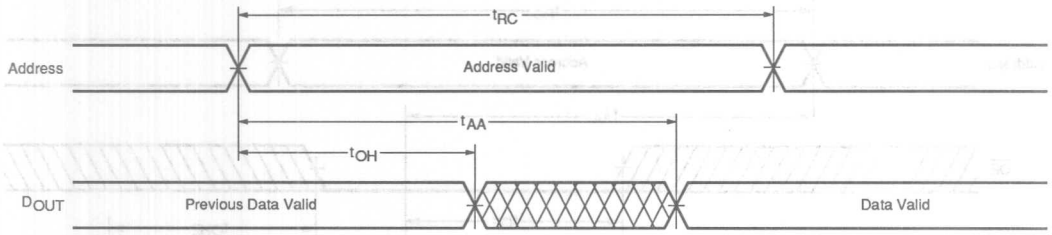


Figure 2. Output Load for t_{CHZ}, t_{CLZ}, t_{OHZ}, t_{OLZ}, t_{WHZ}, and t_{OW}



Timing Waveforms

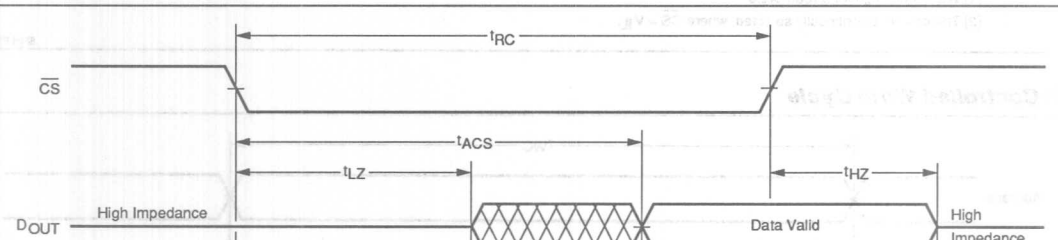
Address Access Cycle



Notes:
[1] $\overline{WE}$ is held high for a read cycle.
[2] The device is continually selected, where $\overline{CS} = \overline{OE} = V_{IL}$.

83IH-6269B

Chip Select Access Cycle



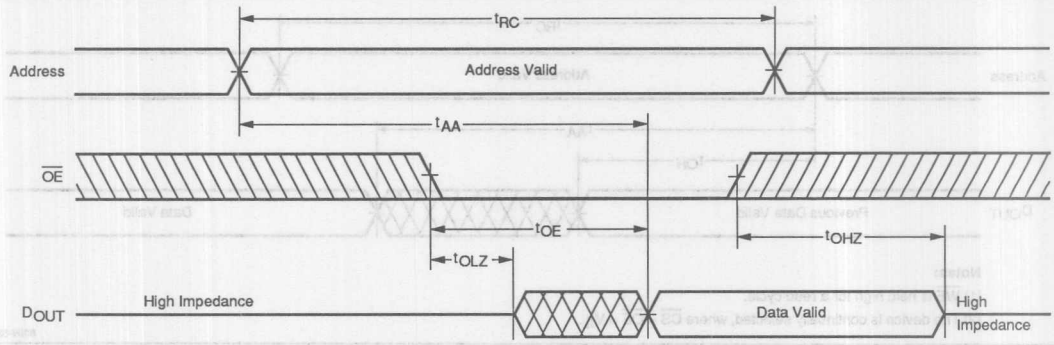
Notes:
[1] $\overline{WE}$ is held high for a read cycle.
[2] Address valid prior to or coincident with the low transition of $\overline{CS}$.
[3] $\overline{OE} = V_{IL}$.

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Timing Waveforms (cont)

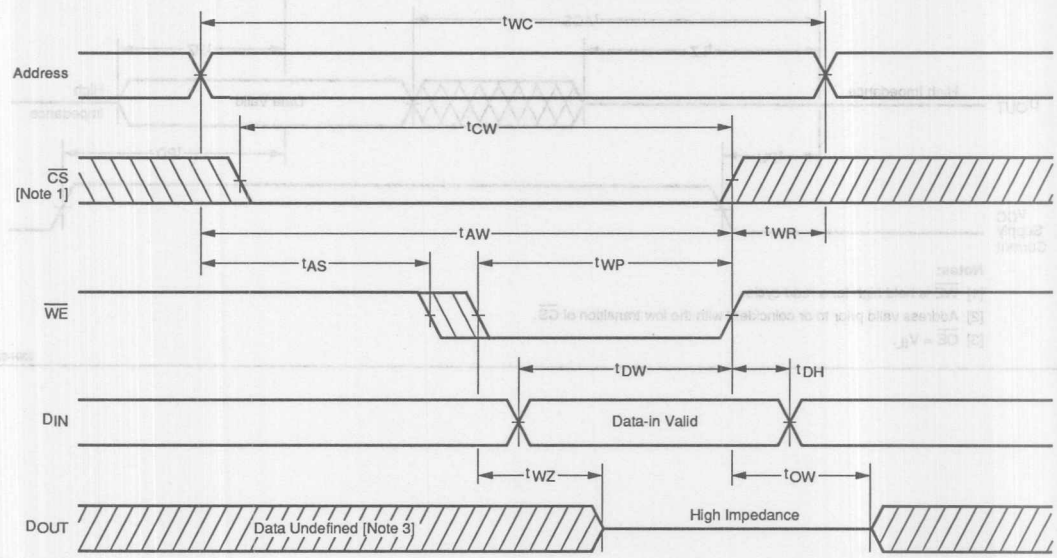
Output Enable Access Cycle



Notes:
[1] $\overline{WE}$ is held high for a read cycle.
[2] The device is continually selected, where $\overline{CS} = V_{IL}$.

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$\overline{WE}$-Controlled Write Cycle

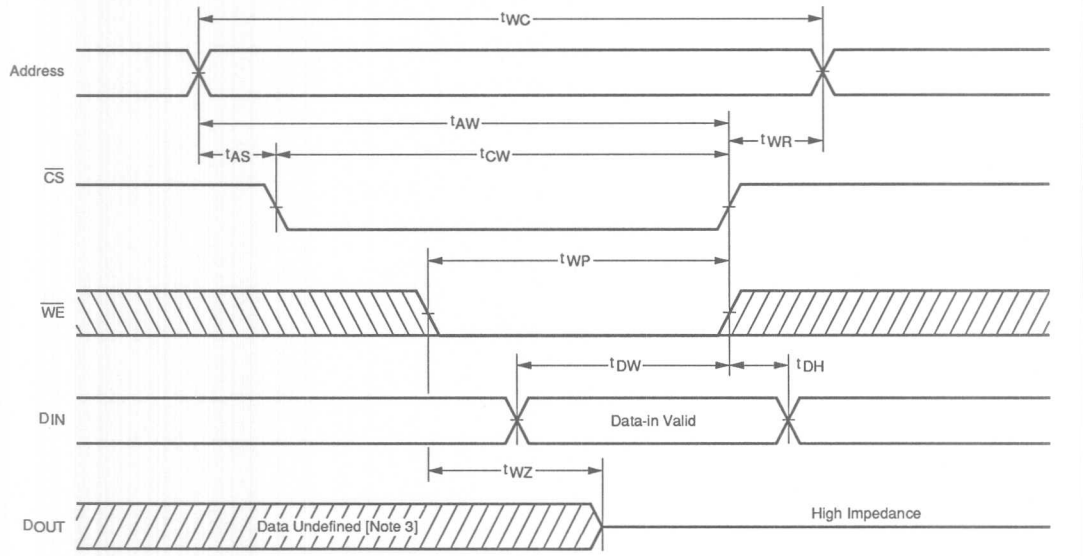


Notes:
[1] $\overline{CS}$ or $\overline{WE}$ must be high during address transition.
[2] If $\overline{OE}$ is high, the I/O pins remain in high impedance.
[3] During this period, the I/O pins may be active ($\overline{OE}$ low). Therefore, data input signals of opposite polarity to the outputs must not be applied.

83IH-6272B

Timing Waveforms (cont)

$\overline{CS}$-Controlled Write Cycle



Notes:

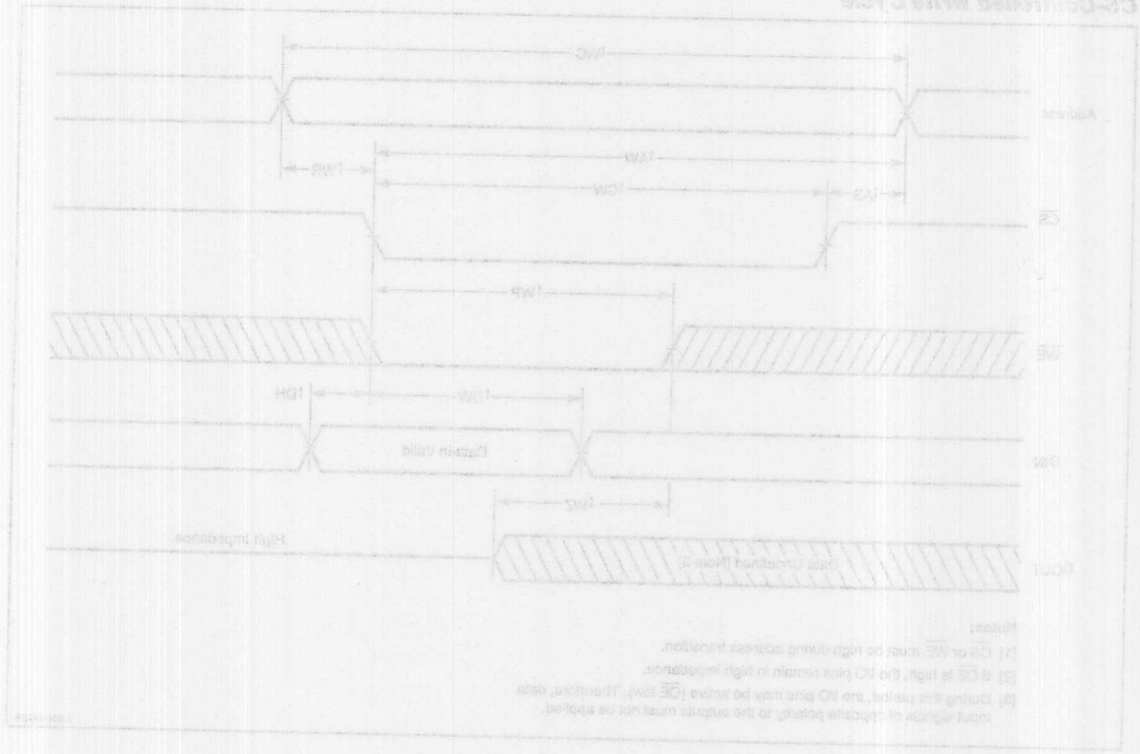
[1] $\overline{CS}$ or $\overline{WE}$ must be high during address transition.

[2] If $\overline{OE}$ is high, the I/O pins remain in high impedance.

[3] During this period, the I/O pins may be active ($\overline{OE}$ low). Therefore, data input signals of opposite polarity to the outputs must not be applied.

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APPLICATION NOTE 50
BATTERY BACKUP CIRCUITS FOR SRAMs

Introduction

The evolution of low-power, high-capacity, high-speed memory technologies has led the system designer to novel and highly portable computer designs. As technology has advanced to low-power devices, it has become possible to make an entire system nonvolatile for the life of the product.

To provide this nonvolatile function, secondary power sources are mounted on a printed circuit board controlled by a backup circuit that switches from the primary power to secondary power during power failures. The backup issue is considered as part of the overall system design, and the choice of a secondary power source and backup circuit are based on the unique characteristics of each application.

This application note deals with the issues of providing a nonvolatile memory system. A review of the evolution of static RAMs (SRAMs) with regard to state-of-the-art, low-power SRAM technology is followed by an example of secondary power sources, as well as several sample backup circuit designs.

SRAM Technology

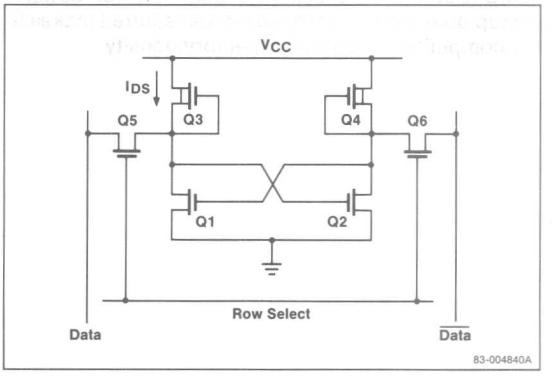
The SRAM historically has been used by system designers to provide a high-speed, low-power data storage function for a variety of computer architectures. The higher cost-per-bit compared to dynamic memories is offset by a simpler circuit design that features a nonmultiplexed address structure, simple timing signals, and no refresh requirement.

Six-Transistor Cell

The development of the SRAM memory cell has followed the trail of bipolar, NMOS, and CMOS technologies in that large-capacity memory devices require minimal cell size, not only to reduce power requirements, but also to be able to fit the die into the package.

The static memory cell is basically a cross-coupled flip-flop circuit requiring no clocks or refreshing. Early six-transistor NMOS static memory cell designs employed the use of enhancement or depletion mode FETs as load devices. Figure 1 shows an example using depletion loads. Q3 and Q4 are depletion-type devices fabricated such that they are always conductive when their respective gate and source nodes are shorted together. If the gate of enhancement device Q2 is written to a low level using Q5 and the data line, Q2 turns off. This allows load device Q4 to pull its source node high and turn on Q1; the write operation using Q6 also helps this action. The cell is designed so that Q1 has much lower "on" resistance than its load Q3. After the write operation ends, and Q5 and Q6 are off, Q1 keeps its drain node at a low level to maintain Q2 in the off state, while the drain node of Q2 is maintained high by Q4. The stored voltages are stable.

Figure 1. Six-Transistor Cell—Depletion



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Four-Transistor Cell

As NMOS technology evolved, the active device for the load was replaced with polysilicon resistors (see figure 2). With the polysilicon load resistor, current levels of less than 1 nA are achievable. Because of these low-current levels, the cell can be used in advanced SRAMs with very high memory density and low standby current. NEC uses this technology in its low-power family of SRAMs to facilitate their use in battery backup applications. This type of core cell is used in both NMOS and CMOS SRAMs from NEC.

CMOS Cell

CMOS technology, with its high-speed, low-power characteristics, makes an attractive choice for memory backup systems.

In figure 3, Q1-Q3 and Q2-Q4 form two CMOS inverters that are cross-coupled to form the conventional flip-flop of the SRAM cell. Unlike the enhancement or polysilicon resistor cells, the CMOS cell does not have a dc current path (other than leakage) in either of its quiescent logic states. While the potentially lower-leakage and wider-voltage operating range makes the six-transistor CMOS cell very desirable for battery backup operation, the large die area required makes it less competitive in cost and memory density.

Figure 2. Four-Transistor Cell—Polysilicon Resistor

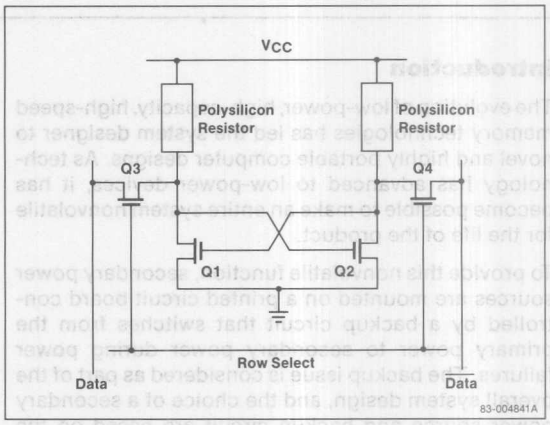
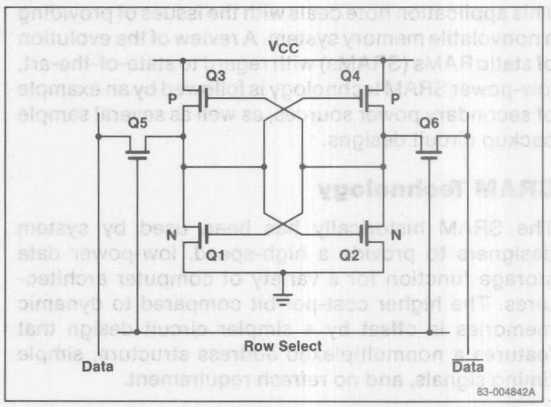


Figure 3. CMOS Cell



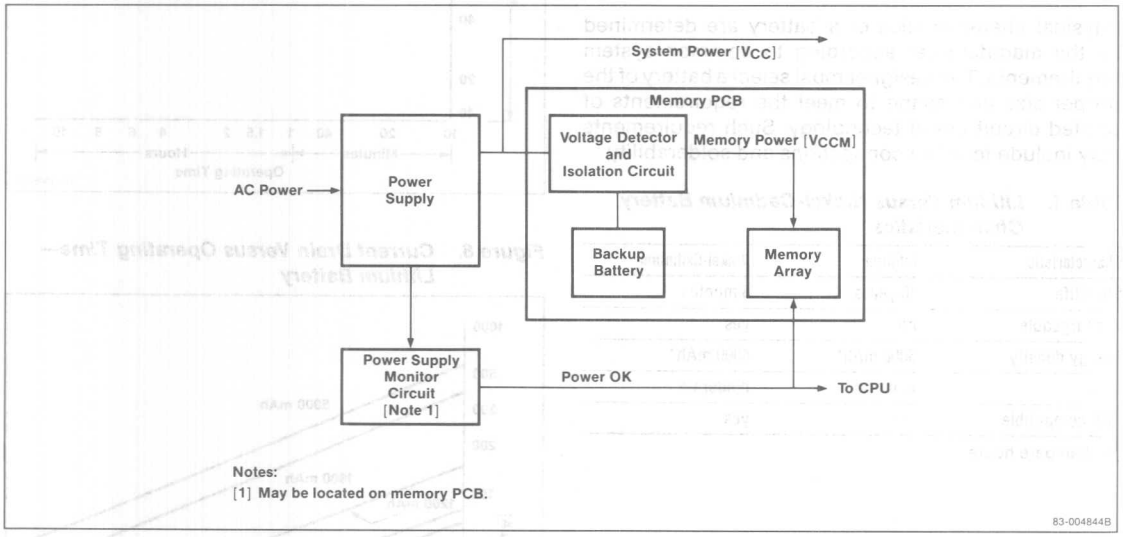
Battery Backup Concept

The goal of a memory backup system design is to guarantee memory data retention for days, months, or years. In the past, these memory backup circuits were implemented as part of the computer's power supply circuit. Today, the memory backup function is designed as part of the individual memory circuit, where each provides a constant secondary (backup) power source and the necessary circuitry to detect power failures and isolate the main power supply from the backup power source (battery). The battery backup circuit must be an integral part of printed circuit board layout. Furthermore, SRAM technology must be able to guarantee the requirements of the memory battery backup function. The following sections discuss in detail the aspects of memory battery backup circuit design using NEC's low-power SRAM technology.

A typical functional block diagram for a memory battery backup system is illustrated in figure 4. The power supply converts ac voltage into a regulated dc voltage, which powers all of the system components (V_{CC}). The power supply monitor circuit detects a power failure and generates an interrupt to the CPU. This circuit also signals the memory circuit to deselect the memory array, thus protecting the memory from false CPU commands. The power supply monitor circuit may be centralized to the power supply or decentralized to each memory circuit.

On the memory circuit, power failure is sensed by a voltage-detector circuit, which isolates the system power from the memory power, allowing the backup battery to become active.

Figure 4. Battery Backup System Block Diagram



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Backup Battery Selection

Battery Type

Nickel-cadmium batteries and lithium batteries were compared for use in a memory battery backup application. Although nickel-cadmium batteries have been a popular choice for this application, recent years have seen the development of lithium batteries. Some characteristics of these two types of batteries are contrasted in table 1. For additional comparison, the characteristics of current drain versus operating time for nickel-cadmium and lithium batteries are shown in figures 5 and 6, respectively.

Since lithium batteries provide a constant current for up to 10 years in this type of low-power application, they were chosen over nickel-cadmium for this design example. A single 3-volt lithium battery is adequate for most CMOS SRAM applications. If higher voltage is required, batteries may be connected in series.

Physical characteristics of a battery are determined by the manufacturer according to common system requirements. The designer must select a battery of the proper size and shape to meet the requirements of printed circuit board technology. Such requirements may include terminal connections and solderability.

Table 1. Lithium Versus Nickel-Cadmium Battery Characteristics

Characteristic	Lithium	Nickel-Cadmium
Shelf life	10 years	6 months
Rechargeable	no	yes
Energy density	5000 mAh*	4000 mAh*
Cost	moderate	moderate
PCB-compatible	yes	yes

*milliampere hours

Figure 5. Current Drain Versus Operating Time—Nickel Cadmium Battery

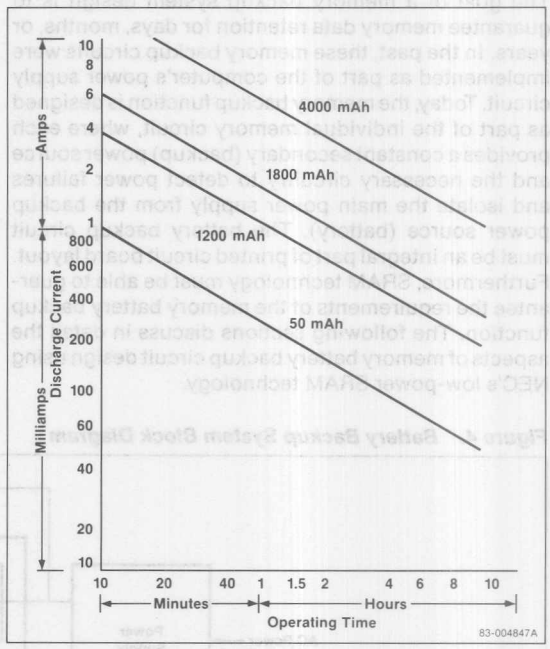
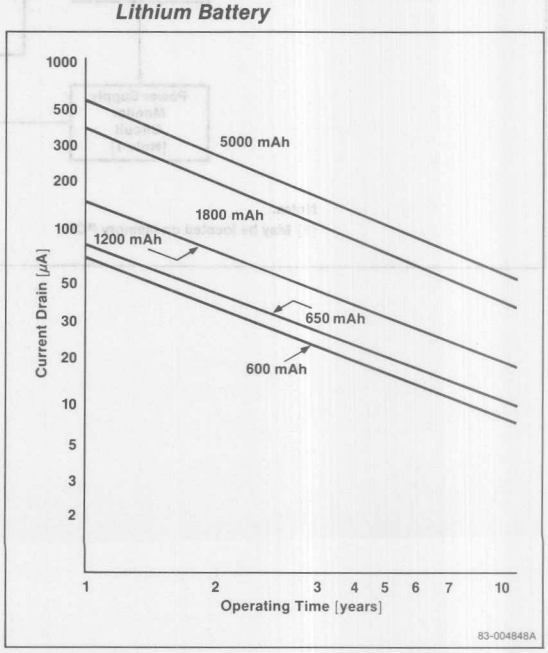


Figure 6. Current Drain Versus Operating Time—Lithium Battery



Battery Capacity

Battery capacity defines the current drive of the battery over a period of time, measured in milliampere hours (mAh). Required capacity of the battery selected for the memory backup circuit can be determined from the following formula:

Current required (mA) x time in backup mode (hours/day) x 365 days/year x number of years

Battery capacity is affected by temperature, humidity, and load conditions. The designer must ensure that these conditions do not degrade the operating life (discharge characteristics) of the battery. Figures 7 and 8 show the effects of temperature and load current variations on lithium battery discharge characteristics.

Figure 7. Lithium Discharge Characteristics— ≃ 20 μA Load

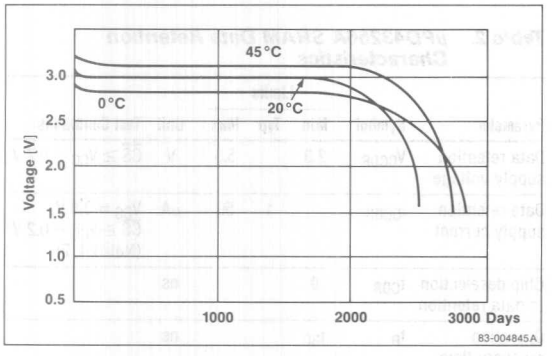
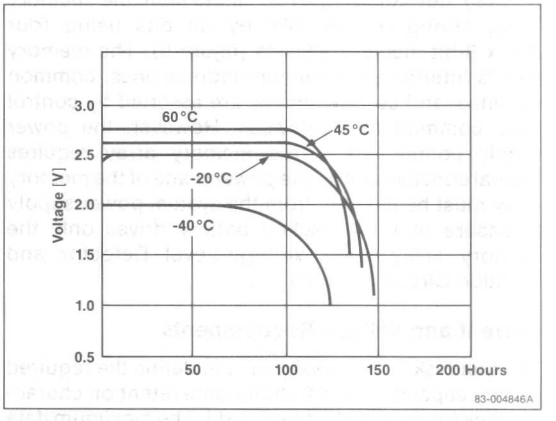


Figure 8. Lithium Discharge Characteristics— ≃ 8.5 mA Load



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Design Example

This section presents and documents a detailed battery backup design example. The discussion encompasses SRAM memory array design, current and voltage requirements, voltage-detector and isolation circuitry, and memory protection design considerations.

SRAM Memory Array

For the battery backup design example, NEC's μPD43256A-15LL (a CMOS-fabricated, 150-ns SRAM memory device) is used to implement the memory array, configured as 32K by 32 bits using four 32K x 8-bit memory devices (figure 9). The memory array's interface of common address lines, common I/O lines, and control signals are asserted by control logic common to all devices. However, the power supply connection to the memory array requires special consideration. The power plane of the memory array must be isolated from the system power supply to ensure that the backup battery drives only the memory array (see "Voltage-Level Detector and Isolation Circuit Design").

Current and Voltage Requirements

The first task for the designer is to define the required battery capacity. Table 2 shows data retention characteristics for the μPD43256A SRAM. The maximum data retention current for this device is 20 μA at 0 to 70°C. For a circuit with four memory devices, total memory array current is 4 x 20 μA = 80 μA.

The battery's operating period is assumed to be 10 years at 12 hours-per-day. Using the formula shown under "Battery Capacity," the required capacity of the battery can be derived from this calculation.

80 μA x 12 hours/day x 365 days/year x 10 years = 3504 mAh

Requirements for the data retention voltage of the μPD43256A SRAM are defined in table 2, while figure 10 shows timing requirements for data retention with respect to the $\overline{CS}$ chip select signal.

Table 2. μPD43256A SRAM Data Retention Characteristics

Parameter	Symbol	Limits Min	Typ	Max	Unit	Test Conditions
Data retention supply voltage	V_{CCDR}	2.0		5.5	V	$\overline{CS} \geq V_{CC} - 0.2$ V
Data retention supply current	I_{CCDR}		1	50	μA	$V_{CC} = 3.0$ V; $\overline{CS} \geq V_{CC} - 0.2$ V (Notes 1, 2)
Chip deselection to data retention	t_{CDR}	0			ns	
Operation recovery time	t_R	t_{RC}			ns	

Notes:

(1) μPD43256A-LL: I_{CCDR} = 20 μA (max) for T_A = 0 to 70°C and 3 μA (max) for T_A = 0 to 40°C.

(2) μPD43256A-L: I_{CCDR} = 15 μA (max) for T_A = 0 to 40°C.

Figure 9. SRAM Memory Array

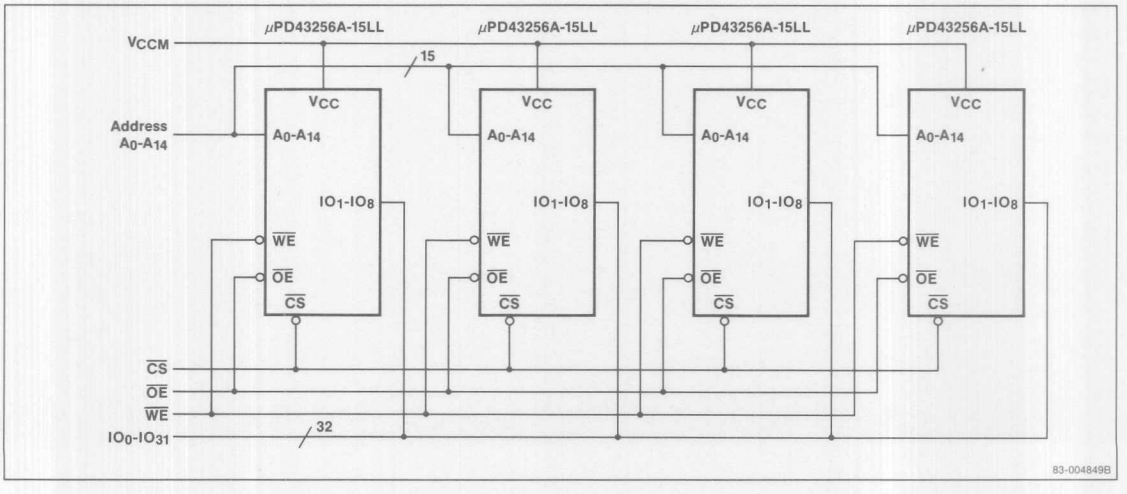
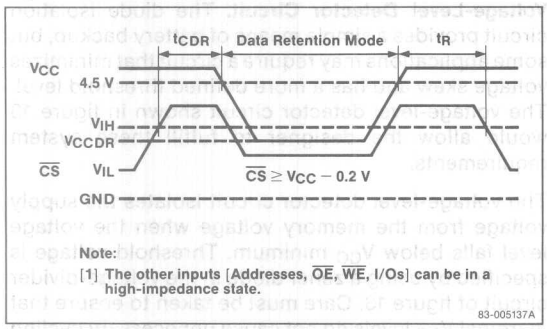


Figure 10. Data Retention Timing Waveforms



Battery Protection. Figure 11 shows the battery portion of the memory battery backup circuit. This portion of the circuit must be designed to provide the required data retention voltage and energy capacity for the memory backup function, yet protect the battery from reverse (charging) current. The diode and resistor shown in figure 11 were selected to protect the battery according to UL standards.

Since lithium batteries are not rechargeable, current-limiting protection must be provided to control the amount of current from the main power supply. For this purpose, the designer must select a diode that protects against charging current, yet provides sufficient voltage for memory battery backup.

The UL-allowable charging current for a lithium battery is specified as 1% of the battery capacity, calculated as follows:

1% x capacity of battery (mAh) ÷ (amount of time charging may occur (hours/day) x 365 days/year x number of years)

In this design example, a minimum capacity of 3504 mAh is required. The closest standard-size lithium battery has a capacity of 5000 mAh. The allowed charging current of this battery for a 10-year period is calculated in this way:

1% x 5000 mAh ÷ (12 hours/day x 365 days/year x 10 years) = 1.1 μA

Therefore, the diode selected to protect the battery must have a maximum reverse leakage current rating of 1.1 μA. To maintain the required data retention voltage at the memory device, a diode with a small forward-voltage drop must be selected. A Schottky diode, with a forward-voltage drop of 0.2 volt, provides a 2.7-volt battery backup voltage and also meets the reverse leakage current specification for this circuit.

According to UL standards, the battery must also be protected against charging current in case the protection diode is damaged. The designer must select a current-limiting resistor for this purpose. Resistor value is determined according to this formula:

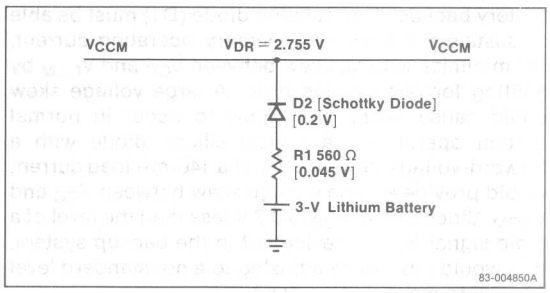
(V_{CC} − $V_{Battery}$) ÷ maximum charging current

UL standards specify a maximum charging current of 5 mA. Therefore, for the circuit in this design example, the minimum resistor value is specified as follows:

(5.5 − 3 V) ÷ 5 mA = 500 Ω

Selecting the aforementioned Schottky diode and a standard 10% resistor value of 560 Ω would guarantee minimum data retention voltage for the battery backup circuit. Total voltage drop across the protection diode and current-limiting resistor is equal to 0.245 volt, which provides a memory backup voltage of 2.755 volts—well above the minimum data retention voltage of 2 volts.

Figure 11. Backup Energy Source Circuit



7

Voltage-Level Detector and Isolation Circuit Design

The designer must also determine the best method for detecting power failures and isolating the main power supply from the backup battery. The circuit designed for these functions must fulfill two requirements: 1) sustain maximum operating current for the memory array, and 2) provide isolation protection during battery backup operation. Several design alternatives for voltage-level detector and isolation circuits are discussed in this section. The standards of comparison between these circuits are relative simplicity of design and voltage drop of the isolation element.

Note: In applications that are subjected to brownouts or extreme temperatures, these voltage-level detector and isolation circuits will minimize unnecessary cycling of the backup battery. However, considerations must be made to protect the memory devices from unstable circuit conditions, especially during power failure. For a discussion of memory protection under these circumstances, refer to "System Power Failure Design Considerations," following this section.

The designer must first determine maximum operating current of the memory array. Since maximum operating current for the μPD43256A SRAM is specified as 35 mA, total operating current is calculated as 4 x 35 mA = 140 mA for the memory array in this design example.

Diode Isolation Circuit. The diode isolation circuit in figure 12 provides a simple approach to memory battery backup. The isolation diode (D1) must be able to sustain the maximum memory operating current, yet minimize voltage skew between V_{CC} and V_{CCM} by limiting forward-voltage drop. A large voltage skew could cause illegal conditions to occur in normal system operations. A typical silicon diode with a forward-voltage drop of 0.7 V at a 140-mA load current would provide a large voltage skew between V_{CC} and V_{CCM}. Since SRAM V_{CC} is 0.7 V less than the level of a logic signal from a device not in the backup system, V_{CC} would have to be adjusted to a nonstandard level of 5.7 V to maintain V_{CC} at 5 V.

In contrast, a Schottky diode typically provides a forward-voltage drop of 0.2 V at a 3-A load current. This low voltage drop minimizes voltage skew and maintains logic input levels to within 0.2 V of V_{CC}, which makes the Schottky diode an ideal choice for the diode isolation circuit.

Voltage-Level Detector Circuit. The diode isolation circuit provides a simple means of battery backup, but some applications may require a circuit that minimizes voltage skew and has a more defined threshold level. The voltage-level detector circuit shown in figure 13 would allow the designer to fulfill these system requirements.

The voltage-level detector circuit isolates the supply voltage from the memory voltage when the voltage level falls below V_{CC} minimum. Threshold voltage is specified by using a zener diode in the voltage-divider circuit of figure 13. Care must be taken to ensure that marginal V_{CC} levels do not cause unnecessary cycling of the backup battery.

Figure 12. Diode Isolation Circuit

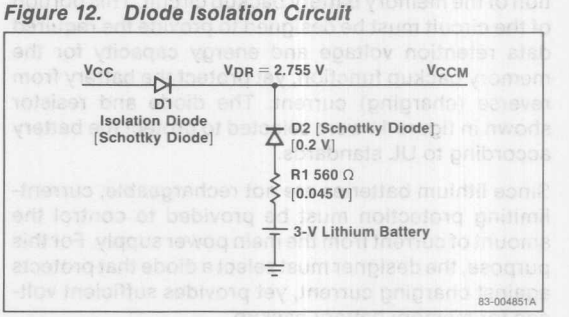
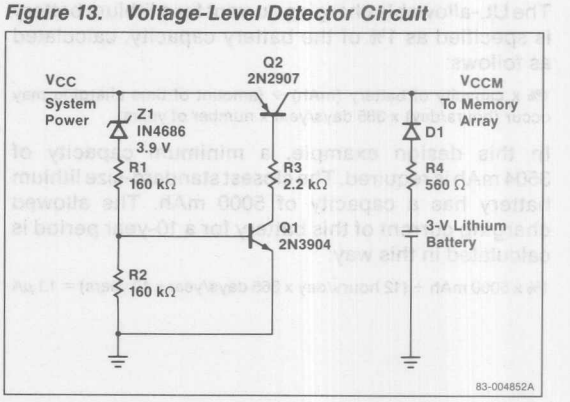


Figure 13. Voltage-Level Detector Circuit



The voltage-level detector circuit consists of zener diode Z1, switching transistor Q1, and the R1 and R2 voltage-divider network. The collector of Q1 is connected to the base of PNP isolation transistor Q2, isolating V_{CC} from V_{CCM} when the V_{CC} voltage level falls below threshold. Threshold voltage (V_{TH}) is determined by $V_{TH} = V_Z + V_{BE1}$, where V_Z is zener voltage and V_{BE1} is the base-to-emitter voltage drop of Q1. The threshold voltage in figure 13 is 3.9 + 0.6 V = 4.5 V, which is the specification for minimum V_{CC}. When V_{CC} drops below minimum specification, the zener diode operates in its forward-voltage region, and no base current flows into Q1. Q1 is then forced into cutoff. With Q1 in cutoff, no base current flows into Q2, consequently forcing Q2 into cutoff and isolating V_{CC} from V_{CCM}.

Isolation transistor Q2 must be capable of supplying a maximum memory operating current of 140 mA and also must provide a minimum V_{SAT} to reduce voltage skew. The PNP 2N2907 medium-power transistor chosen for this application can drive up to 150 mA with a dc gain range of 100 to 300. The maximum base current needed to turn on Q2 is calculated as follows:

$I_{BQ2} = I_{CQ2} \div h_{fe} = 140\ mA \div 100 = 1.4\ mA$

Since the base of Q2 is connected to the collector of Q1, and $I_{BQ2} = I_{CQ1}$, Q1 must be capable of driving a collector current of 1.4 mA or greater. The choice for Q1 is an NPN 2N3904, a general-purpose transistor with an I_C maximum of 10 mA and an h_{fe} of 100. The base current needed to turn on Q1 is calculated at 3 mA ÷ 100 = 30 μA, which is much less than the maximum I_{BQ1} provided by the R1-R2 network. The voltage divider R1-R2 must also forward-bias the base-emitter junction of Q1 to allow the transistor to operate in its active region. The voltage at the Q1 base node is 4.1 volts, which keeps Q1 turned on until threshold voltage is reached.

The circuit in figure 13 was characterized, and the relationship between the input and output voltage for two output loads is shown in figure 14. At an input voltage level of 4.5 V, the output voltage maintains a voltage level higher than the minimum data retention voltage of 2 V.

Schmitt Trigger Voltage-Level Detector. The voltage-level detector circuit is an improvement over the diode isolation circuit. However, the threshold point is sensitive to variations in Q1 gain, and could cause oscillations around the trigger point, draining the backup battery. The circuit shown in figure 15 reduces threshold sensitivity by adding an operational amplifier, thereby improving threshold margin by introducing hysteresis into the threshold region. This comparator circuit is commonly referred to as a Schmitt trigger.

Figure 14. Voltage-Level Detector/Transfer Function

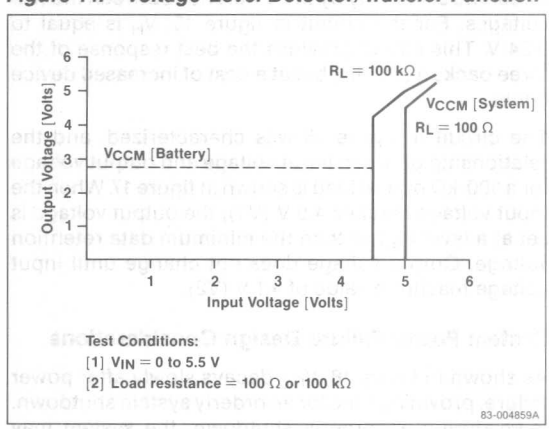
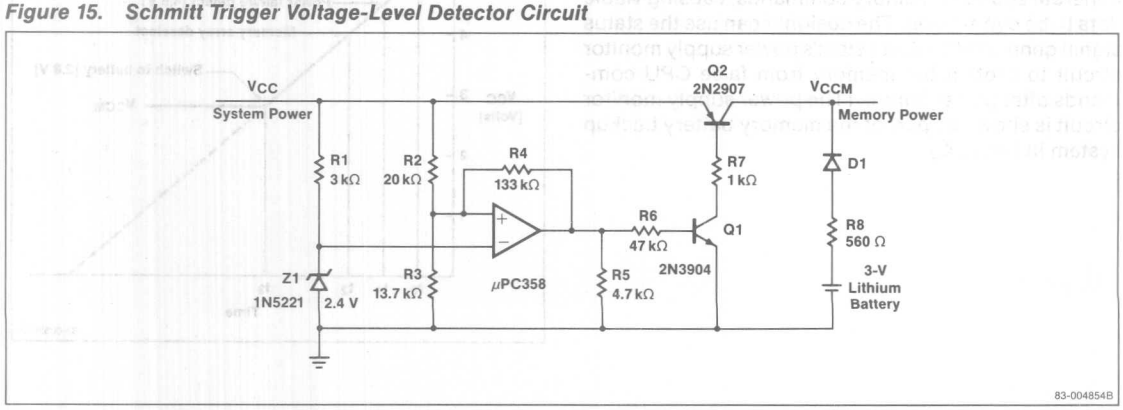


Figure 15. Schmitt Trigger Voltage-Level Detector Circuit



The noninverting input of the μPC358 is connected to a reference-voltage network consisting of R4 and R5. This reference voltage, when compared to the input voltage on the inverting input, determines when the output of the operational amplifier will transition. If a loop gain in excess of unity is chosen, the output waveform continues to be virtually discontinuous at the comparison voltage. However, at this point, the circuit would exhibit a phenomenom called hysteresis. Hysteresis voltage is determined by the resistor network of R4 and R5.

Figure 16 illustrates the response of the Schmitt trigger voltage-level detector circuit to the input signals connected to the noninverting input of the μPC358. When the input voltage reaches the value V1, the output goes high, and when the input is at V2, the output transitions to the low state. The difference between the input signals (V1 − V2) is called the hysteresis voltage (V_H). Therefore, the threshold voltage is dependent upon two input values, increasing the threshold sensitivity by the difference between the two voltages. For the circuit in figure 15, V_H is equal to 0.34 V. This circuit provides the best response of the three backup circuits, but at a cost of increased device count.

The circuit in figure 15 was characterized, and the relationship between input voltage and output voltage for a 100-kΩ output load is shown in figure 17. When the input voltage reaches 4.5 V (V1), the output voltage is set at a level higher than the minimum data retention voltage. Output voltage does not change until input voltage reaches a value of 4.1 V (V2).

System Power Failure Design Considerations

As shown in figure 18, V_{CC} decays slowly after power failure, providing time for an orderly system shutdown. Even during an orderly shutdown, the system may generate spurious memory commands, causing viable data to be overwritten. The designer can use the status signal generated by the system's power supply monitor circuit to protect the memory from false CPU commands after power failure. (The power supply monitor circuit is shown as part of the memory battery backup system in figure 4.)

Figure 16. Response of the Schmitt Trigger to an Arbitrary Signal

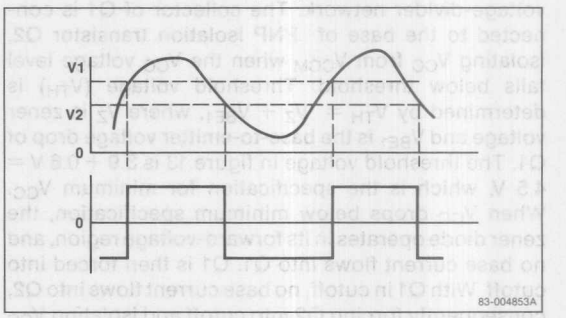


Figure 17. Schmitt Trigger Detector/Transfer Function

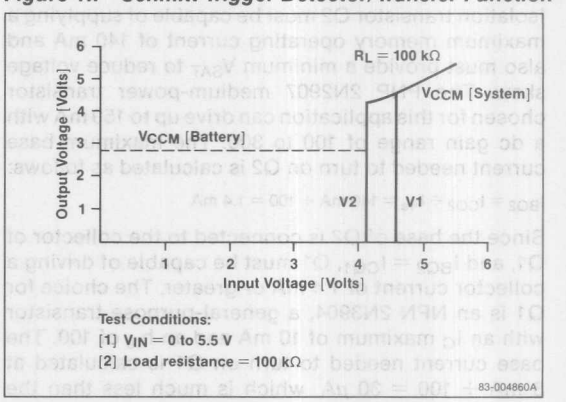
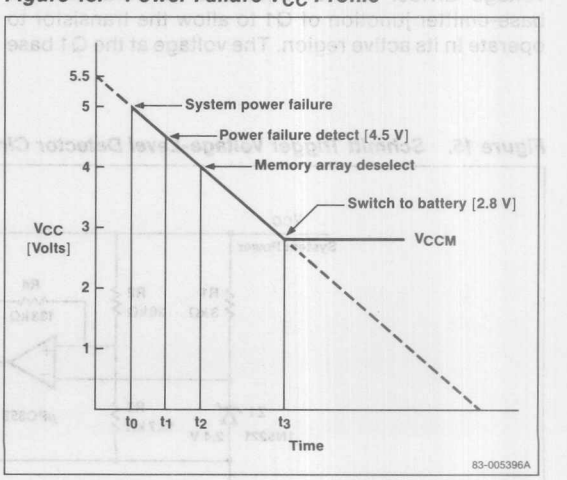


Figure 18. Power Failure V_{CC} Profile



The power supply status signal (Power OK) remains inactive during the entire time V_{CC} is off to force the output of the NAND gate to remain inactive (high). This status signal also is sent to the NAND gate of the memory circuit ("Power OK" in figure 19). The memory circuit "ands" this status signal with the other control signals and deselects the memory array before any false commands are generated.

Once the backup circuit has taken over and the memory array has been deselected, $\overline{CS}$ must be maintained at $V_{CC} - 0.2$ V. The 10 kΩ resistor ensures that the requirement for $\overline{CS} \geq V_{CCM} - 0.2$ V is met.

If a power supply monitor circuit is not provided, the designer may design one. The circuit shown in figure 20 uses a voltage-level detector design to detect when V_{CC} falls below 4.5 V. This circuit is similar to the voltage-level detector circuit used in the battery backup design example. Rather than control an isolation transistor, this power supply monitor circuit generates a power supply status signal (Power OK) to the memory select logic.

The circuit shown in figure 20 is subject to oscillations due to variations in Q1 gain and limited threshold margins. The addition of a Schmitt trigger to the power supply monitor circuit (figure 21) increases threshold margins by introducing hysteresis into the threshold region. The amount of hysteresis is determined by the values of R4 and R5. When input voltage falls below 4.5 V, the circuit generates a low signal (Power OK) to the memory select logic, and the memory array is deselected. Power OK remains low, because R5 pulls it down as long as V_{CC} is off.

Figure 19. Memory Array Deselect Circuit

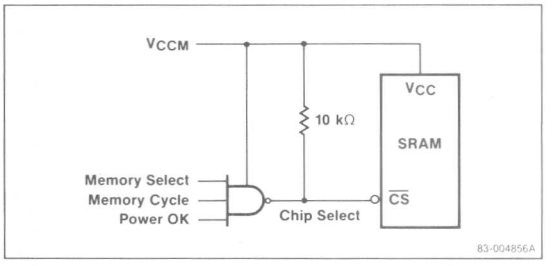


Figure 20. Power Supply Monitor Circuit

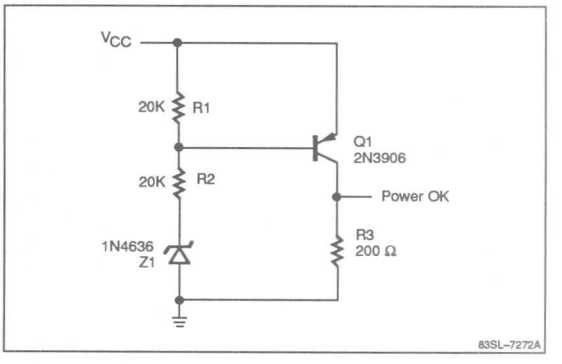
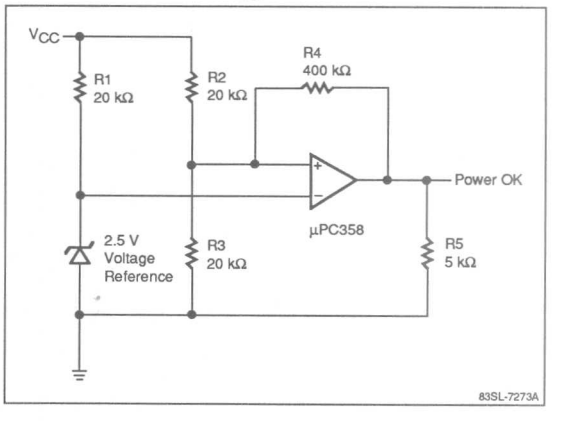


Figure 21. Power Supply Monitor Circuit With Schmitt Trigger



7

NEC Electronics Inc.

Battery Backup Using NEC's Supercaps™ Application Note 90-04

Introduction

Supercaps are an innovative type of capacitor providing a volumetric efficiency (i.e., capacitance per unit volume for a given voltage) of 10 to 50 times that of conventional aluminum electrolytic capacitors. High capacitance (2.2 million μF) and low leakage current make the supercap an efficient, reliable and cost-effective energy storage device.

In 1879, the theory of electric double-layer capacitance was introduced by Helmholtz, but the first electric double-layer capacitor using solid electrolyte wasn't developed until 90 years later, a gap caused in part by a lack of proper materials. In 1979, NEC introduced its electric double-layer supercapacitor, nicknamed *supercap*, and with it a new manufacturing technology and newly developed construction materials.

Today NEC manufactures an extensive line of supercaps to meet a variety of demands. For example, large current backup is provided by our FA- and FE-series, small current backup by our FY-series, moderate current backup by the FS-series, and wide operating margins by the FR-series.

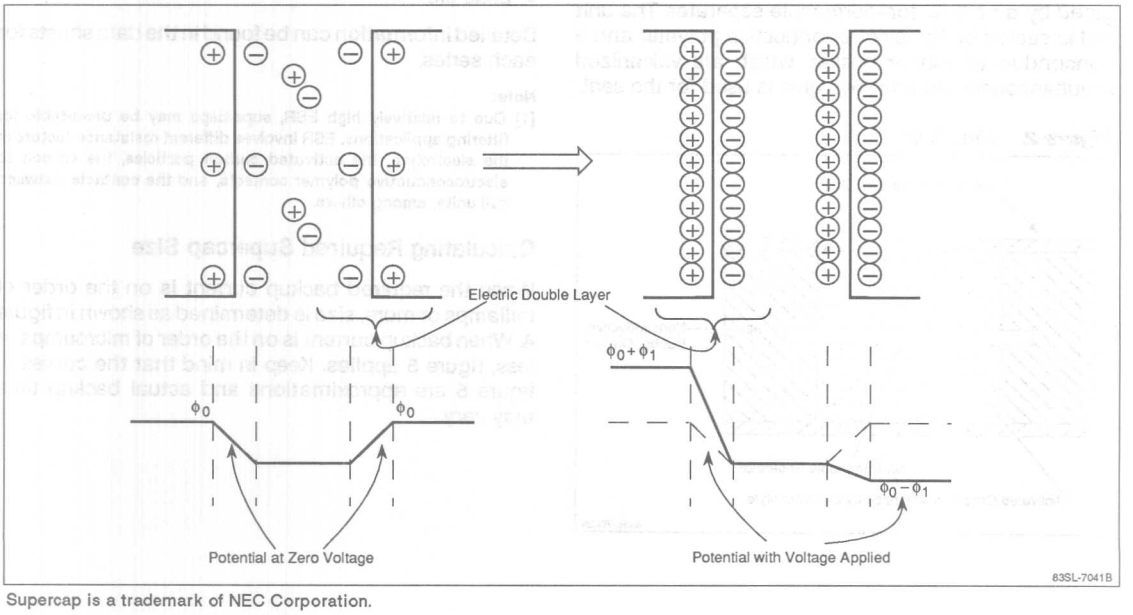
Theory of Operation

At each interface (figure 1), an array of charged particles and induced charges is thought to exist. This array is known as an electric double layer. The large capacitance of an electric double-layer capacitor arises from the charge stored at the interface as the electric field changes across two available phases. In a supercap, one phase consists of activated carbon particles and the other of sulfuric acid solution as an ionically conducting electrolyte. In general, the relationship of the charge per unit area (η) and the double-layer potential (ϕ) is reflected by the following equation:

$$\eta = [d / (4\pi\delta)] \times \phi$$

where d is the dielectric constant of the interface media and δ is the mean distance between the solid surface (polarizable electrode) and the ionic center. The value of δ is a few angstroms. In the Helmholtz model, the potential gradient exists only in the area of the electric double layer. As a result, the potential curve is as shown in figure 1.

Figure 1. Basic Model of a Supercap



Supercap is a trademark of NEC Corporation.

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If ϕ_0 represents ϕ when no external bias is applied, then the calculation is expressed this way:

$$\eta_0 = [d / (4\pi\delta)] \times \phi_0$$

Conversely, some charges are accumulated at the interface if an external electric field is applied to the system shown in figure 1. In this case, the potential rises to ϕ_1 and the charge of η_1 can be accumulated as shown by this equation:

$$\eta_1 = [d / (4\pi\delta)] \times (2\phi_1 - \phi_0)$$

The charge equivalent to η_1 can be accumulated by changing the external electric field, as follows:

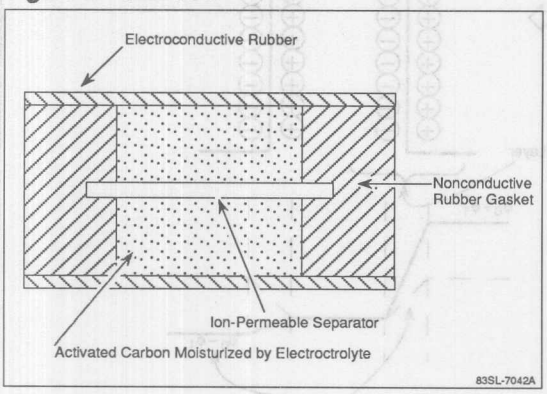
$$\eta_1 \cong 2\eta_0 (\phi_1 / \phi_0), \text{ where } (\phi_1 \gg \phi_0)$$

The experimental result, using mercury as a polarizable electrode, shows a 20 to 40 μF/cm^2 value. Therefore, if the activated carbon behavior is the same as that of mercury, the capacitance for a capacitor consisting of activated carbon with a 1,000 m^2/g surface area is calculated to be 200 to 400 F/g, a very large value. In this way, a device with large capacitance and small size can be easily manufactured.

Structure

The cross section of a unit cell is shown in figure 2. The activated carbon particles moisturized (semi-liquid state) by diluted sulfuric acid electrolyte are segregated by a porous, ion-permeable separator. The unit cell is sealed by the electroconductive polymer and a nonconductive rubber gasket, which are vulcanized simultaneously. No adhesive glue is used for the seal.

Figure 2. Unit Cell



The breakdown voltage of the unit cell can be as low as 1.2 volts (thermodynamically), which is the decomposition voltage of aqueous electrolyte solution. Therefore, several unit cells are stacked in series to get the required rated voltage (figure 3).

Performance

Supercaps have no standard specifications from groups such as the EIA and, accordingly, are specified by individual manufacturers. For example, NEC has specifications to cover the following:

- Operating temperature
- Maximum working voltage
- Capacitance
- Capacitance tolerance
- Equivalent series resistance[1] (ESR)
- Charging (leakage) current at 30 minutes
- Voltage holding characteristics
- Temperature characteristics
- Lead terminal strength
- Vibration
- Solderability
- Resistance to soldering heat
- Temperature cycling
- Humidity
- Load life

Detailed information can be found in the data sheets for each series.

Note:

[1] Due to relatively high ESR, supercaps may be unsuitable for filtering applications. ESR involves different resistance factors in the electrolyte, the activated carbon particles, the carbon to electroconductive polymer contacts, and the contacts between cell units, among others.

Calculating Required Supercap Size

When the required backup current is on the order of miliamps or more, size is determined as shown in figure 4. When backup current is on the order of microamps or less, figure 5 applies. Keep in mind that the curves in figure 5 are approximations and actual backup time may vary.

Figure 3. Cross Section

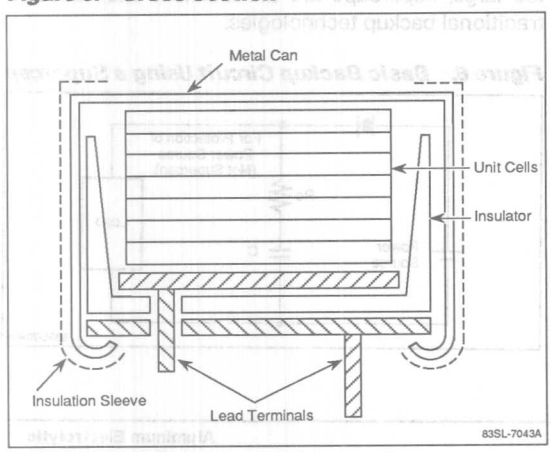


Figure 4. Relationship Between Voltage and Time While the Supercap is Charging and Discharging

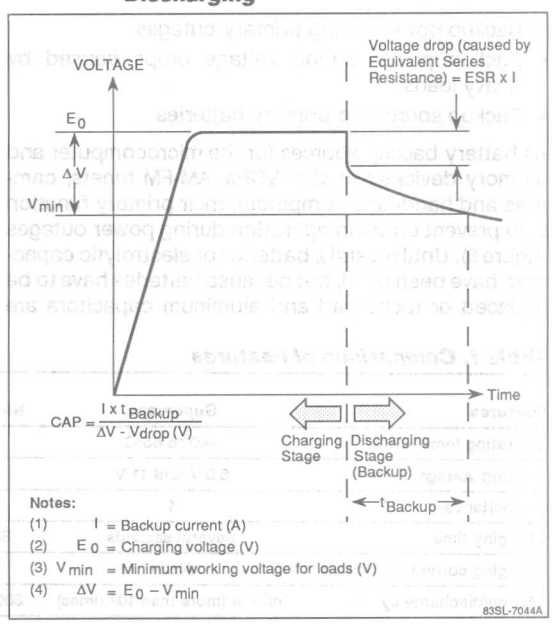
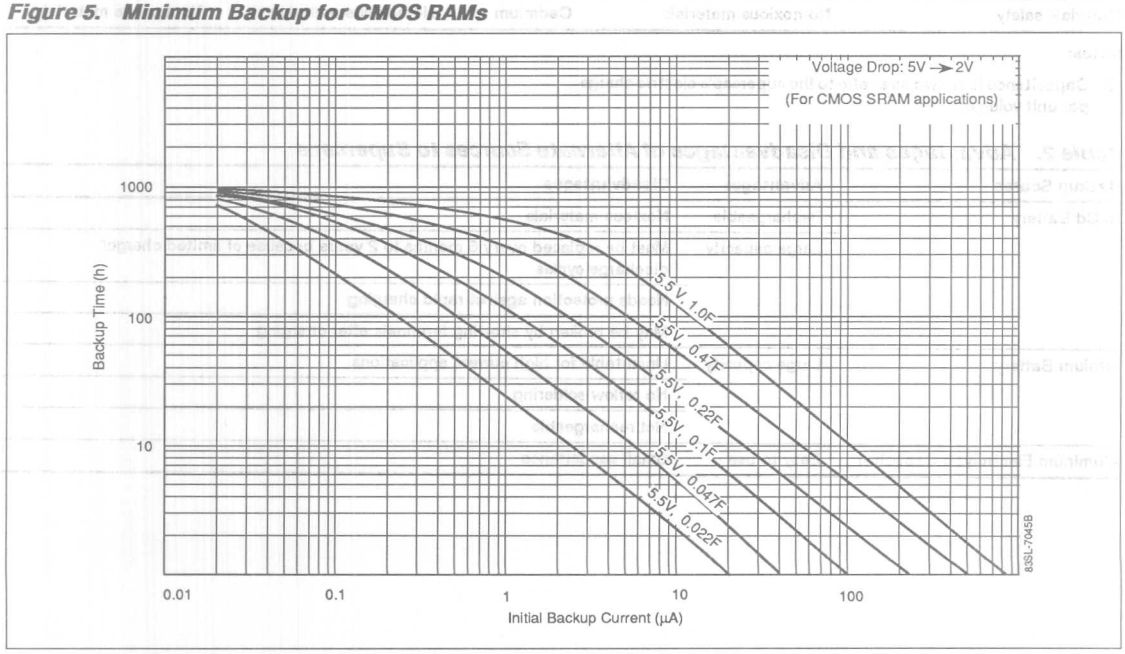


Figure 5. Minimum Backup for CMOS RAMs



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Applications

Supercaps typically are used as

- Backup power during primary outages
- Backup power during voltage drops caused by heavy loads
- Backup sources to primary batteries

As battery backup sources for the microcomputer and memory devices found in VCRs, AM-FM tuners, cameras and hand-held computers, their primary function is to prevent errors in operation during power outages (figure 6). Until recently, batteries or electrolytic capacitors have been used, but because batteries have to be replaced or recharged and aluminum capacitors are too large, supercaps are an excellent alternative to traditional backup technologies.

Figure 6. Basic Backup Circuit Using a Supercap

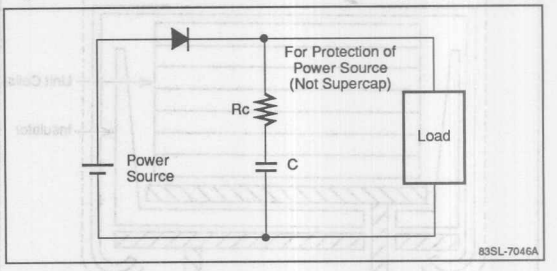


Table 1. Comparison of Features

Features	Supercaps	Ni-Cd Batteries	Lithium Batteries	Aluminum Electrolytic Capacitors
Operating temperature	−40 to 85°C	−20 to 65°C	−20 to 60°C	−40 to 85°C
Working voltage	5.5 V and 11 V	1.2 V	3 V	Over 6.3 V
Capacitance	1	210	360	0.01
Charging time	Several seconds	Several hours	—	Several seconds
Charging current limitations	None	Limited	—	None
Charge/discharge cycles	Infinite (more than 10^5 times)	300 to 500 times	—	Infinite (more than 10^5 times)
Reflow soldering	Applicable	Not applicable	Not applicable	Applicable
Materials safety	No noxious materials	Cadmium	No noxious materials	No noxious materials

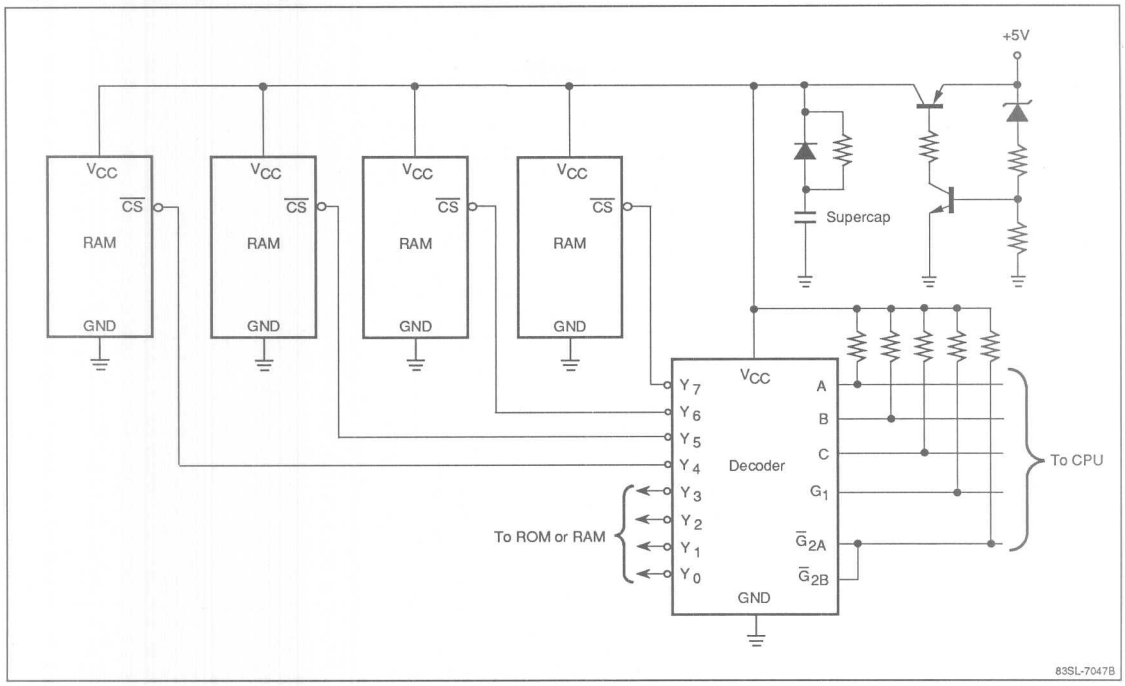
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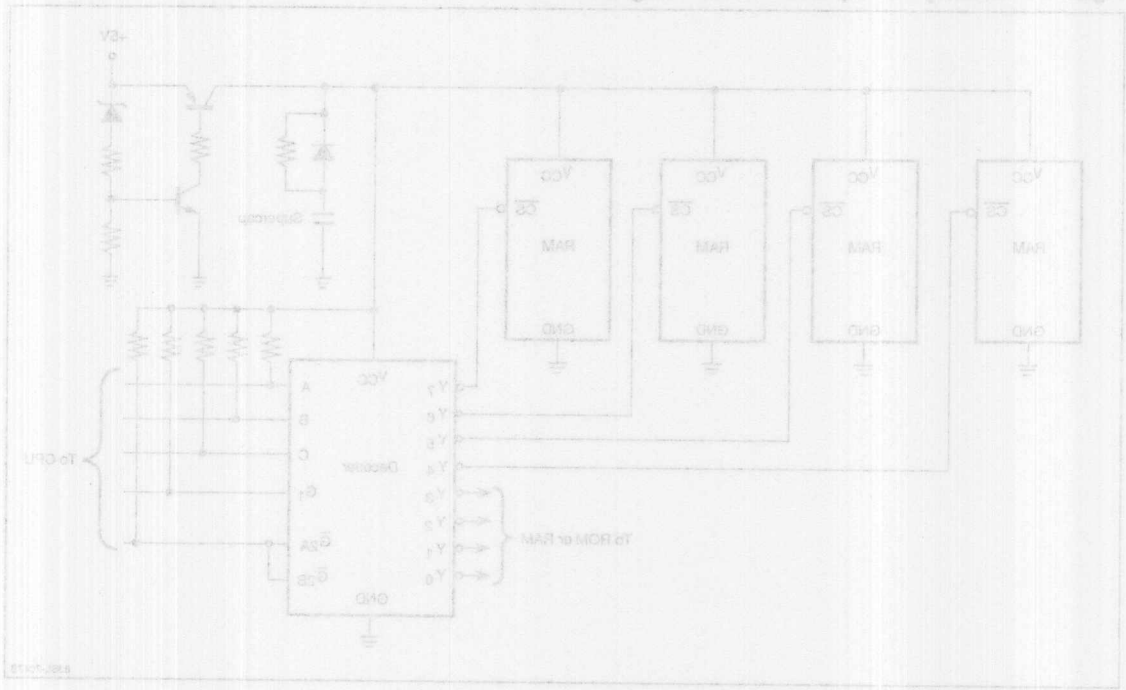
(1) Capacitance is shown as a ratio to the supercap's electric charge per unit volume.

Table 2. Advantages and Disadvantages of Alternate Sources to Supercaps

Backup Source	Advantages	Disadvantages
Ni-Cd Battery	Rechargeable	Noxious materials
	Large capacity	Must be replaced every 6 months to 2 years because of limited charge/discharge cycles
		Needs protection against rapid charging
		May be broken by shorting terminals after charging
Lithium Battery	Large capacity	Unsuitable for high current applications
		No reflow soldering
		Not rechargeable
Aluminum Electrolytic Capacitor	Easy to use	Small capacitance

Figure 7. Memory Backup Circuit Block Diagram





Section 8
ECL RAMs

μPB10422 8-1
256 x 4-Bit 10K ECL RAM

μPB10470 8-7
4,096 x 1-Bit 10K ECL RAM

μPB10474 8-13
1,024 x 4-Bit 10K ECL RAM

μPB10474A 8-19
1,024 x 4-Bit 10K ECL RAM

μPB10474E 8-25
1,024 x 4-Bit 10K ECL RAM

μPB10480 8-33
16,384 x 1-Bit 10K ECL RAM

μPB10484 8-39
4,096 x 4-Bit 10K ECL RAM

μPB10484A 8-45
4,096 x 4-Bit 10K ECL RAM

μPB10A484 8-51
4,096 x 4-Bit 10K ECL RAM

μPD10500 8-57
262,144 x 1-Bit 10K BiCMOS ECL RAM

μPD10504 8-63
65,536 x 4-Bit 10K BiCMOS ECL RAM

μPB100422 8-69
256 x 4-Bit 100K ECL RAM

μPB100470 8-75
4,096 x 1-Bit 100K ECL RAM

μPB100474 8-81
1,024 x 4-Bit 100K ECL RAM

μPB100474A 8-87
1,024 x 4-Bit 100K ECL RAM

μPB100474E 8-93
1,024 x 4-Bit 100K ECL RAM

μPB100480 8-99
16,384 x 1-Bit 100K ECL RAM

μPB100484 8-105
4,096 x 4-Bit 100K ECL RAM

μPB100484A 8-111
4,096 x 4-Bit 100K ECL RAM

μPB100A484 8-117
4,096 x 4-Bit 100K ECL RAM

μPD100500 8-123
262,144 x 1-Bit 100K BiCMOS ECL RAM

μPD100504 8-129
65,536 x 4-Bit 100K BiCMOS ECL RAM

Description

The μPB10422 is a very high-speed 10K interface ECL RAM organized as 256 words by 4 bits and designed with noninverted, open-emitter outputs and low power consumption. Two versions with fast access times of 7 and 10 ns maximum are available in 24-pin ceramic DIP packaging.

Features

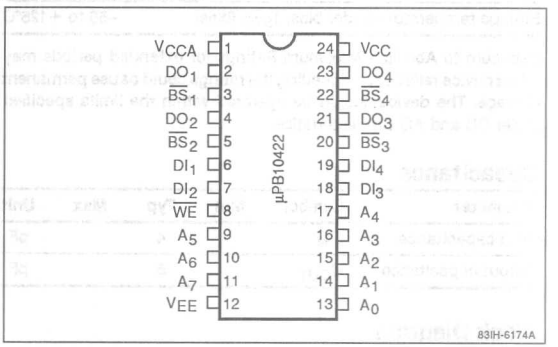
- 256-word x 4-bit organization
- 10K ECL interface
- Noninverted, open-emitter outputs
- Fast access times
- Low power consumption
- 24-pin ceramic DIP packaging

Ordering Information

Part Number	Access Time (max)	Supply Current (min)	Package
μPB10422D-7	7 ns	–220 mA	24-pin ceramic DIP
D-10	10 ns		

Pin Configurations

24-Pin Ceramic DIP



Pin Identification

Symbol	Function
A_0 - A_7	Address inputs
DI_1 - DI_4	Data inputs
DO_1 - DO_4	Data outputs
$\overline{BS}_1$ - $\overline{BS}_4$	Block select inputs
$\overline{WE}$	Write enable
V_{CC}	Power supply (current switches and bias driver)
V_{CCA}	Power supply (output devices)
V_{EE}	Power supply

8

Absolute Maximum Ratings

Supply voltage, V_{EE} to V_{CC}	−7.0 to +0.5 V
Input voltage, V_{IN}	V_{EE} to +0.5 V
Output current, I_{OUT}	−30 to +0.1 mA
Storage temperature, T_{STG}	−65 to +150°C
Storage temperature under bias, T_{STG} (bias)	−55 to +125°C

Exposure to Absolute Maximum Ratings for extended periods may affect device reliability; exceeding the ratings could cause permanent damage. The device should be operated within the limits specified under DC and AC Characteristics.

Capacitance

Parameter	Symbol	Min	Typ	Max	Unit
Input capacitance	C_{IN}		4		pF
Output capacitance	C_{OUT}		5		pF

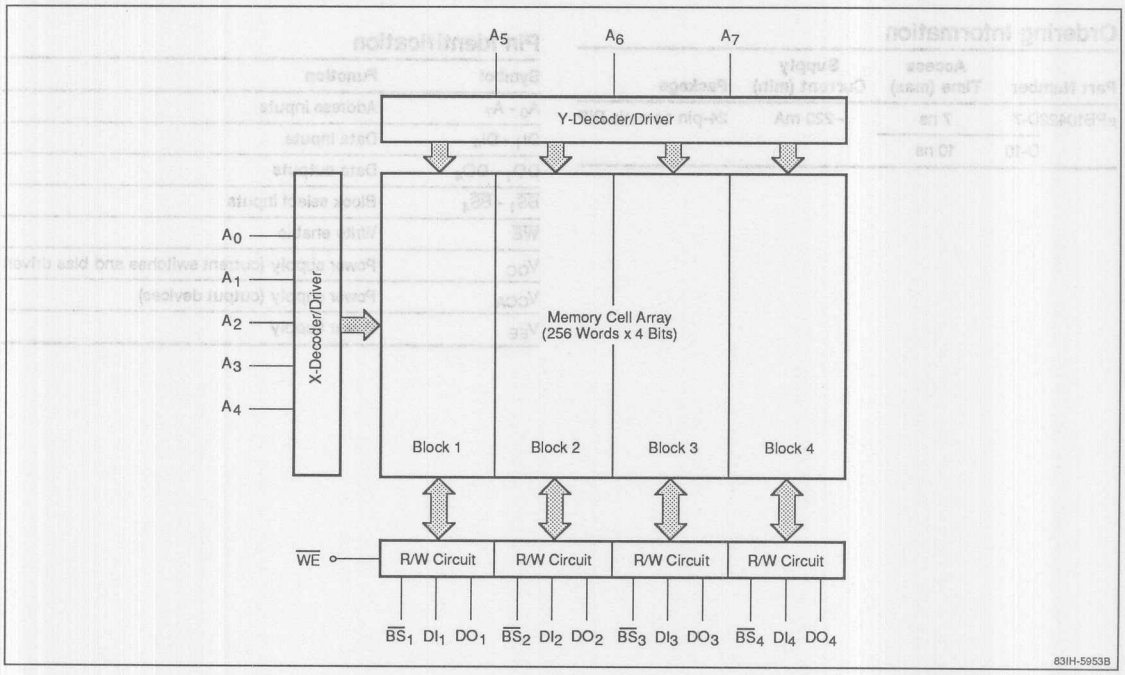
Truth Table

$\overline{BS}$	$\overline{WE}$	DI	DO	Function
H	X	X	L	Not selected
L	L	L	L	Write 0
L	L	H	L	Write 1
L	H	X	Data Valid	Read

Notes:

(1) The Block Select input for each of the four memory blocks is used independently as shown in the block diagram.

Block Diagram



DC Characteristics

T_A = 0 to +75°C; V_{EE} = −5.2 V; output load = 50 Ω to −2.0 V

Parameter	Symbol	Min	Max	Unit	Test Conditions
Output voltage, high	V_{OH}	−1000	−840	mV	V_{IN} = V_{IH} max or V_{IL} min; T_A = 0°C
		−960	−810	mV	V_{IN} = V_{IH} max or V_{IL} min; T_A = 25°C
		−900	−720	mV	V_{IN} = V_{IH} max or V_{IL} min; T_A = 75°C
Output voltage, low	V_{OL}	−1870	−1665	mV	V_{IN} = V_{IH} max or V_{IL} min; T_A = 0°C
		−1850	−1650	mV	V_{IN} = V_{IH} max or V_{IL} min; T_A = 25°C
		−1830	−1625	mV	V_{IN} = V_{IH} max or V_{IL} min; T_A = 75°C
Output threshold voltage, high	V_{OHC}	−1020		mV	V_{IN} = V_{IH} min or V_{IL} max; T_A = 0°C
		−980		mV	V_{IN} = V_{IH} min or V_{IL} max; T_A = 25°C
		−920		mV	V_{IN} = V_{IH} min or V_{IL} max; T_A = 75°C
Output threshold voltage, low	V_{OLC}		−1645	mV	V_{IN} = V_{IH} min or V_{IL} max; T_A = 0°C
			−1630	mV	V_{IN} = V_{IH} min or V_{IL} max; T_A = 25°C
			−1605	mV	V_{IN} = V_{IH} min or V_{IL} max; T_A = 75°C
Input voltage, high	V_{IH}	−1145	−840	mV	For all inputs: T_A = 0°C
		−1105	−810	mV	For all inputs: T_A = 25°C
		−1045	−720	mV	For all inputs: T_A = 75°C
Input voltage, low	V_{IL}	−1870	−1490	mV	For all inputs: T_A = 0°C
		−1850	−1475	mV	For all inputs: T_A = 25°C
		−1830	−1450	mV	For all inputs: T_A = 75°C
Input current, high	I_{IH}		220	μA	V_{IN} = V_{IH} max
Input current, low	I_{IL}	0.5	170	μA	$\overline{BS_1}$ - $\overline{BS_4}$; V_{IN} = V_{IL} min
		−50		μA	For all others: V_{IN} = V_{IL} min
Supply current	I_{EE}	−220		mA	For all inputs and outputs open

Notes:

(1) The device under test is mounted in a test socket and measured at a thermal equilibrium established with a transverse air flow maintained at greater than 2.0 m/s.

8

AC Characteristics

T_A = 0 to +75°C; V_{EE} = −5.2 V ± 5%; output load = 50 Ω to −2.0 V

		μPB10422-7			μPB10422-10				
Parameter	**Symbol**	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**	**Unit**	**Test Conditions**
Read Operation									
Block select access time	t_{ABS}			5			5	ns	
Block select recovery time	t_{RBS}			5			5	ns	
Address access time	t_{AA}			7			10	ns	
Write Operation									
Write pulse width	t_W	5			6			ns	
Data setup time	t_{WSD}	1			2			ns	
Data hold time	t_{WHD}	1			2			ns	
Address setup time	t_{WSA}	1			2			ns	
Address hold time	t_{WHA}	1			2			ns	
Block select setup time	t_{WSBS}	1			2			ns	
Block select hold time	t_{WHBS}	1			2			ns	
Write disable time	t_{WS}			5			5	ns	
Write recovery time	t_{WR}			6			9	ns	
Output Rise and Fall Times									
Output rise time	t_R		2			2		ns	
Output fall time	t_F		2			2		ns	

Notes:

(1) The device under test is mounted in a test socket and measured at a thermal equilibrium established with a transverse air flow maintained at greater than 2.0 m/s.

(2) All timing measurements are referenced to 50% input levels.

(3) See figures 1 and 2.

Figure 1. Loading Conditions Test Circuit

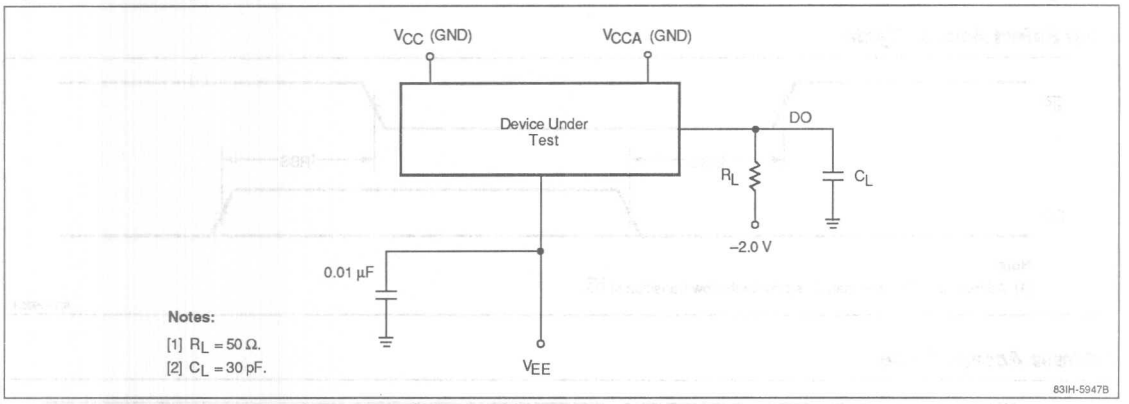
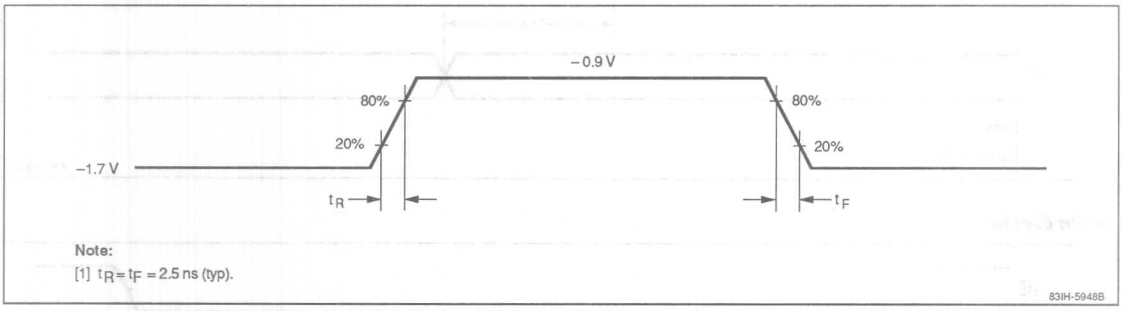


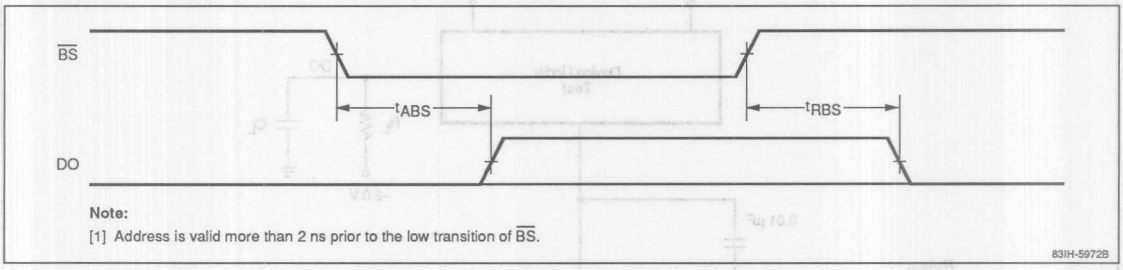
Figure 2. Input Pulse



8

Timing Waveforms

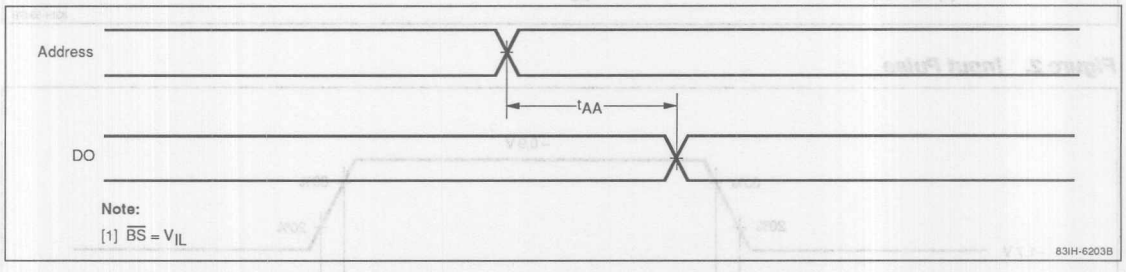
Chip Select Access Cycle



Note:
[1] Address is valid more than 2 ns prior to the low transition of $\overline{BS}$.

83IH-5972B

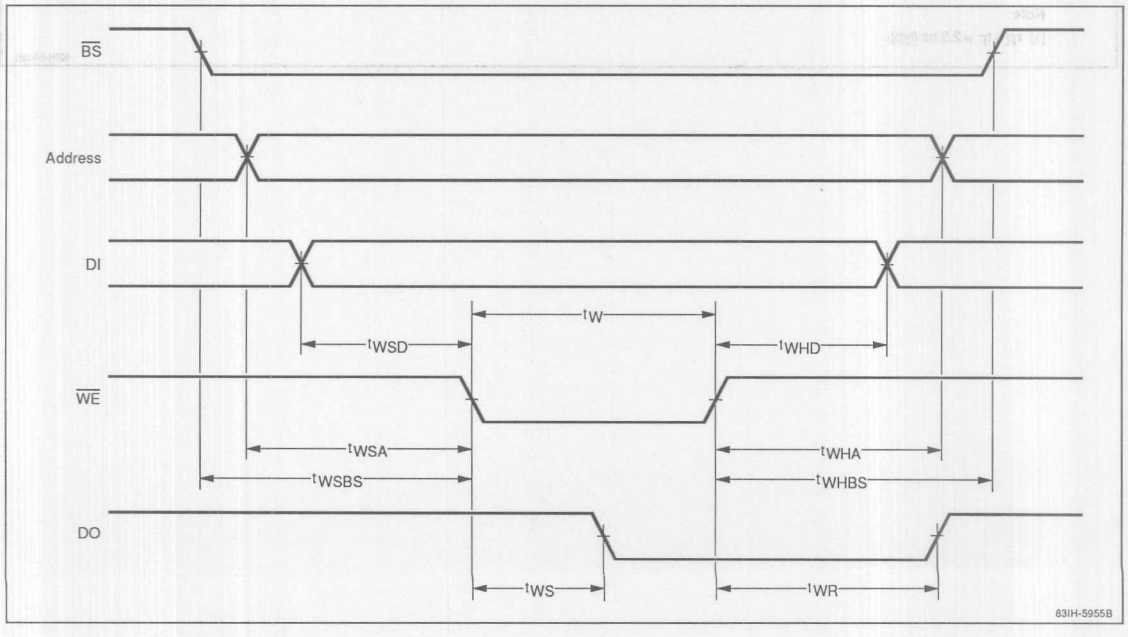
Address Access Cycle



Note:
[1] $\overline{BS} = V_{IL}$

83IH-6203B

Write Cycle



83IH-5955B

μPB10470
4,096 x 1-BIT
10K ECL RAM

Description

The μPB10470 is a very high-speed 10K interface ECL RAM organized as 4K words by 1 bit and designed with an open emitter output (noninverted) for low power consumption. Two fast access time versions are available: 10 ns maximum and 15 ns maximum. The μPB10470 is available in a hermetic, 300-mil, 18-pin cerdip.

Features

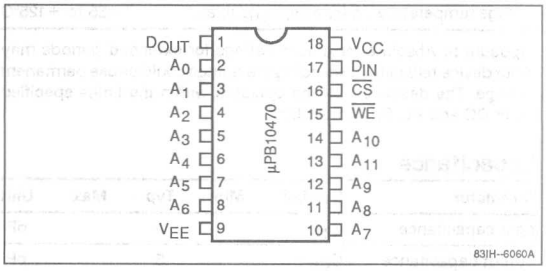
- 4096-word x 1-bit organization
- 10K ECL interface
- Open emitter output (noninverted)
- Fast access times
- Low power consumption
- 300-mil, 18-pin cerdip packaging

Ordering Information

Part Number	Access Time (max)	Package
μPB10470D-10	10 ns	18-pin cerdip
D-15	15 ns	

Pin Configuration

18-Pin Cerdip



Pin Identification

Symbol	Function
A_0 - A_{11}	Address inputs
D_{IN}	Data input
D_{OUT}	Data output
$\overline{CS}$	Chip select
$\overline{WE}$	Write enable
V_{CC}	Ground
V_{EE}	–5.2-volt power supply

8

Absolute Maximum Ratings

Supply voltage, V_{EE} to V_{CC}	−7.0 to +0.5 V
Input voltage, V_{IN}	V_{EE} to +0.5 V
Output current, I_{OUT}	−30 to +0.1 mA
Storage temperature, T_{STG}	−65 to +150°C
Storage temperature under bias, T_{STG} (bias)	−55 to +125°C

Exposure to Absolute Maximum Ratings for extended periods may affect device reliability; exceeding the ratings could cause permanent damage. The device should be operated within the limits specified under DC and AC Characteristics.

Capacitance

Parameter	Symbol	Min	Typ	Max	Unit
Input capacitance	C_{IN}		4		pF
Output capacitance	C_{OUT}		5		pF

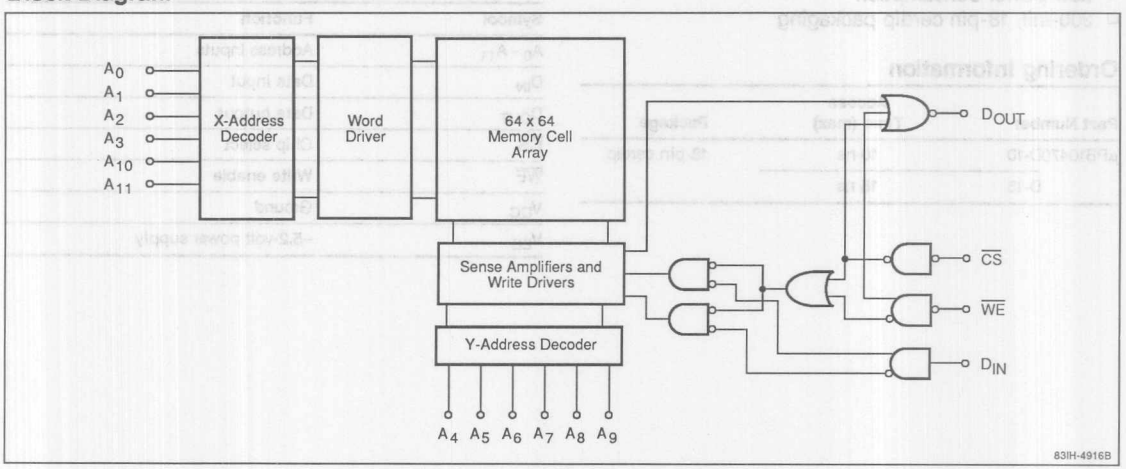
Truth Table

$\overline{CS}$	$\overline{WE}$	D_{IN}	Function	Output
H	X	X	Not selected	L
L	L	L	Write 0	L
L	L	H	Write 1	L
L	H	X	Read	D_{OUT}

Notes:

(1) X = don't care.

Block Diagram



DC Characteristics

T_A = 0 to +75°C; V_{EE} = −5.2 V; output load = 50 Ω to −2.0 V

Parameter	Symbol	T_A (°C)	Min	Max	Unit	Test Conditions
Output voltage, high	V_{OH}	0	−1000	−840	mV	V_{IN} = V_{IH} (max) or V_{IL} (min)
		+25	−960	−810	mV	
		+75	−900	−720	mV	
Output voltage, low	V_{OL}	0	−1870	−1665	mV	V_{IN} = V_{IH} (max) or V_{IL} (min)
		+25	−1850	−1650	mV	
		+75	−1830	−1625	mV	
Output threshold voltage, high	V_{OHC}	0	−1020		mV	V_{IN} = V_{IH} (min) or V_{IL} (max)
		+25	−980		mV	
		+75	−920		mV	
Output threshold voltage, low	V_{OLC}	0		−1645	mV	V_{IN} = V_{IH} (min) or V_{IL} (max)
		+25		−1630	mV	
		+75		−1605	mV	
Input voltage, high	V_{IH}	0	−1145	−840	mV	Guaranteed input voltage high for all inputs
		+25	−1105	−810	mV	
		+75	−1045	−720	mV	
Input voltage, low	V_{IL}	0	−1870	−1490	mV	Guaranteed input voltage low for all inputs
		+25	−1850	−1475	mV	
		+75	−1830	−1450	mV	
Input current, high	I_{IH}	0 to +75		220	μA	V_{IN} = V_{IH} (max)
Input current, low	I_{IL}	0 to +75	0.5	170	μA	For $\overline{CS}$: V_{IN} = V_{IL} (min)
		0 to +75	−50		μA	For all others: V_{IN} = V_{IL} (min)
Supply current	I_{EE}	0 to +75	−220		mA	All inputs and outputs open

Notes:

(1) The device under test (DUT) is mounted in a test socket and is measured at a thermal equilibrium established with a transverse air flow maintained at greater than 2.0 m/s.

AC Characteristics

T_A = 0 to +75°C; V_{EE} = −5.2 V ± 5%

Parameter	Symbol	μPB10470-10 Min	μPB10470-10 Typ	μPB10470-10 Max	μPB10470-15 Min	μPB10470-15 Typ	μPB10470-15 Max	Unit	Test Conditions
Read Operation									
Address access time	t_{AA}			10			15	ns	
Chip select access time	t_{ACS}			6			8	ns	
Chip select recovery time	t_{RCS}			6			8	ns	
Write Operation									
Write pulse width	t_W	10			15			ns	
Data setup time	t_{WSD}	2			2			ns	
Data hold time	t_{WHD}	2			2			ns	
Address setup time	t_{WSA}	3			3			ns	
Address hold time	t_{WHA}	2			2			ns	
Chip select setup time	t_{WSCS}	2			2			ns	
Chip select hold time	t_{WHCS}	2			2			ns	
Write disable time	t_{WS}			6			8	ns	
Write recovery time	t_{WR}			10			10	ns	
Output Rise and Fall Times									
Rise time	t_R		2			2		ns	
Fall time	t_F		2			2		ns	

Notes:

(1) The device under test (DUT) is mounted in a test socket and is measured at a thermal equilibrium established with a transverse air flow maintained at greater than 2.0 m/s.

Figure 1. Loading Conditions Test Circuit

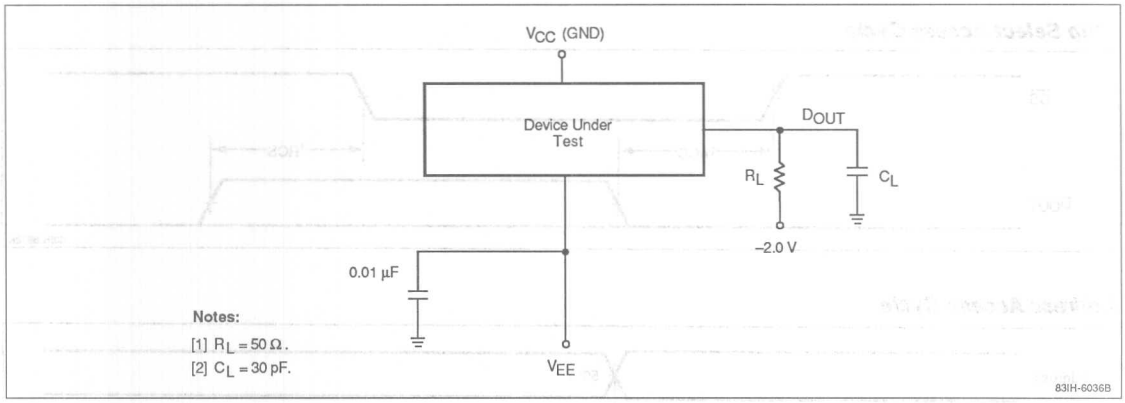
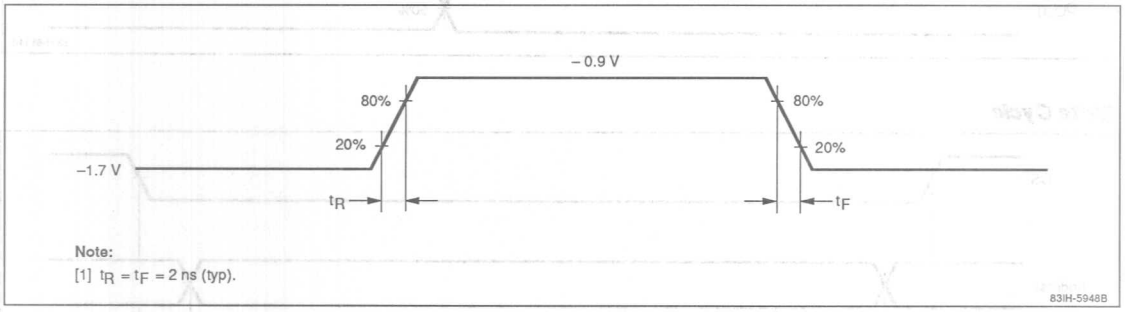


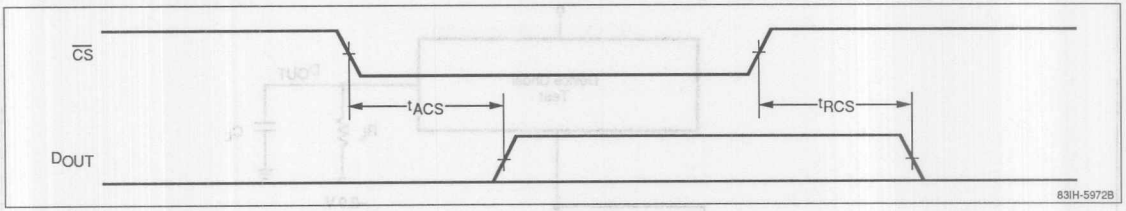
Figure 2. Input Pulse



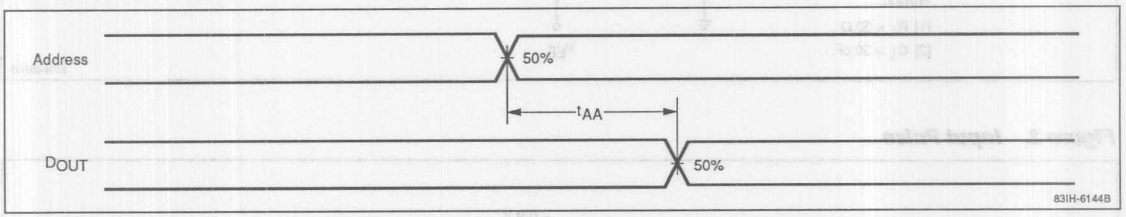
8

Timing Waveforms

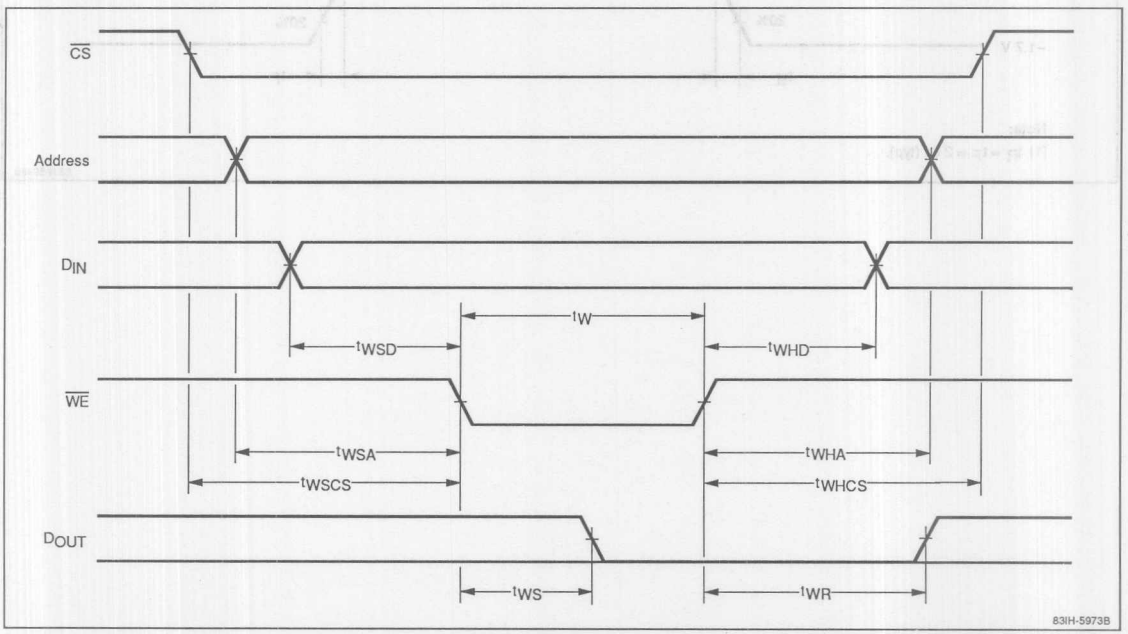
Chip Select Access Cycle



Address Access Cycle



Write Cycle



μPB10474
1,024 x 4-Bit
10K ECL RAM

Description

The μPB10474 is a very high-speed 10K interface ECL RAM organized as 1,024 words by 4 bits and designed with noninverted, open-emitter outputs and low power consumption. Three versions with access times of 8 ns, 10 ns and 15 ns maximum are available in hermetic, 400-mil, 24-pin cerdip packaging.

Features

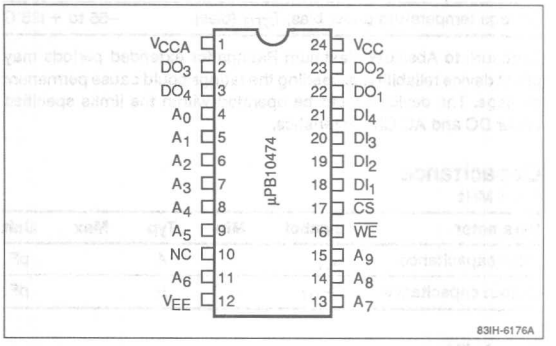
- 1,024-word x 4-bit organization
- 10K ECL interface
- Noninverted, open-emitter outputs
- Fast access times
- Low power consumption
- 400-mil, 24-pin cerdip packaging

Ordering Information

Part Number	Access Time (max)	Package
μPB10474D-8	8 ns	24-pin cerdip
D-10	10 ns	
D-15	15 ns	

Pin Configuration

24-Pin Cerdip



Pin Identification

Symbol	Function
A_0 - A_9	Address inputs
DI_1 - DI_4	Data inputs
DO_1 - DO_4	Data outputs
$\overline{WE}$	Write enable
$\overline{CS}$	Chip select
V_{CC}	Power supply (current switches and bias driver)
V_{CCA}	Power supply (output devices)
V_{EE}	Power supply
NC	No connection

8

Absolute Maximum Ratings

Supply voltage, V_{EE} to V_{CC}	−7.0 to +0.5 V
Input voltage, V_{IN}	V_{EE} to +0.5 V
Output current, I_{OUT}	−30 to +0.1 mA
Storage temperature, T_{STG}	−65 to +150°C
Storage temperature under bias, T_{STG} (bias)	−55 to +125°C

Exposure to Absolute Maximum Ratings for extended periods may affect device reliability; exceeding the ratings could cause permanent damage. The device should be operated within the limits specified under DC and AC Characteristics.

Capacitance

f = 1 MHz

Parameter	Symbol	Min	Typ	Max	Unit
Input capacitance	C_{IN}		4		pF
Output capacitance	C_{OUT}		5		pF

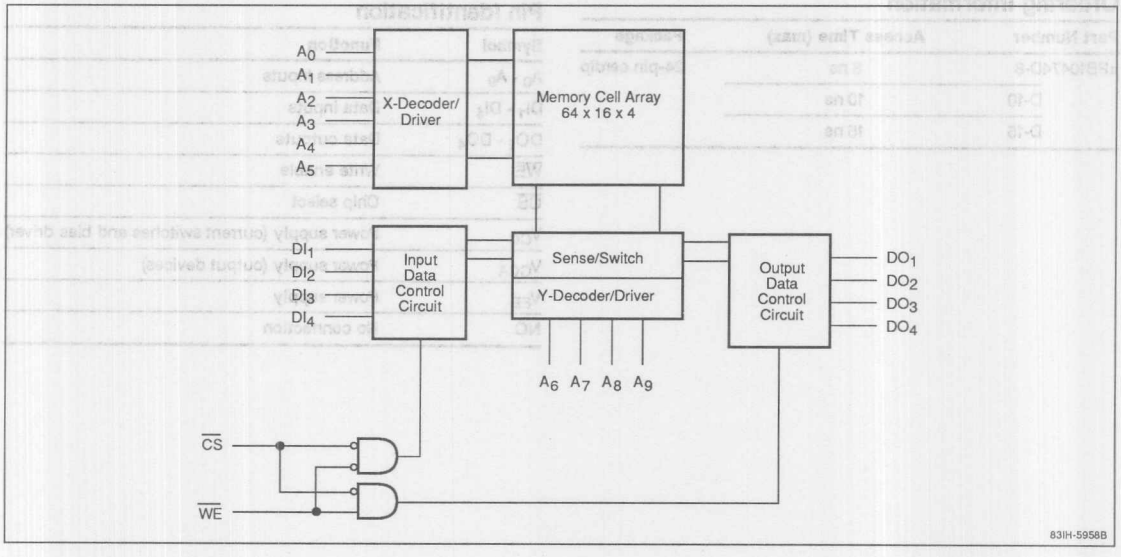
Truth Table

$\overline{CS}$	$\overline{WE}$	D_{IN}	Output	Mode
H	X	X	L	Not selected
L	L	L	L	Write 0
L	L	H	L	Write 1
L	H	X	D_{OUT}	Read

Notes:

(1) X = don't care.

Block Diagram



DC Characteristics

T_A = 0 to +75°C; V_{EE} = −5.2 V; output load = 50 Ω to −2.0 V

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions
Output voltage, high	V_{OH}	−1000		−840	mV	V_{IN} = V_{IH} max or V_{IL} min; T_A = 0°C
		−960		−810	mV	V_{IN} = V_{IH} max or V_{IL} min; T_A = 25°C
		−900		−720	mV	V_{IN} = V_{IH} max or V_{IL} min; T_A = 75°C
Output voltage, low	V_{OL}	−1870		−1665	mV	V_{IN} = V_{IH} max or V_{IL} min; T_A = 0°C
		−1850		−1650	mV	V_{IN} = V_{IH} max or V_{IL} min; T_A = 25°C
		−1830		−1625	mV	V_{IN} = V_{IH} max or V_{IL} min; T_A = 75°C
Output threshold voltage, high	V_{OHC}	−1020			mV	V_{IN} = V_{IH} min or V_{IL} max; T_A = 0°C
		−980			mV	V_{IN} = V_{IH} min or V_{IL} max; T_A = 25°C
		−920			mV	V_{IN} = V_{IH} min or V_{IL} max; T_A = 75°C
Output threshold voltage, low	V_{OLC}			−1645	mV	V_{IN} = V_{IH} min or V_{IL} max; T_A = 0°C
				−1630	mV	V_{IN} = V_{IH} min or V_{IL} max; T_A = 25°C
				−1605	mV	V_{IN} = V_{IH} min or V_{IL} max; T_A = 75°C
Input voltage, high	V_{IH}	−1145		−840	mV	For all inputs: T_A = 0°C
		−1105		−810	mV	For all inputs: T_A = 25°C
		−1045		−720	mV	For all inputs: T_A = 75°C
Input voltage, low	V_{IL}	−1870		−1490	mV	For all inputs: T_A = 0°C
		−1850		−1475	mV	For all inputs: T_A = 25°C
		−1830		−1450	mV	For all inputs: T_A = 75°C
Input current, high	I_{IH}			220	μA	V_{IN} = V_{IH} max
Input current, low	I_{IL}	0.5		170	μA	For $\overline{CS}$: V_{IN} = V_{IL} min
		−50			μA	For all others: V_{IN} = V_{IL} min
Supply current	I_{EE}	−220			mA	All inputs and outputs open

Notes:

(1) The device under test is mounted in a test socket and measured at a thermal equilibrium established with a transverse air flow maintained at greater than 2.0 m/s.

8

AC Characteristics

T_A = 0 to +75°C; V_{EE} = −5.2 V ± 5%; output load = 50 Ω to −2.0 V

		μPB10474-8			μPB10474-10			μPB10474-15				
Parameter	**Symbol**	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**	**Unit**	**Test Conditions**
Read Operation												
Chip select access time	t_{ACS}			5			6			8	ns	
Chip select recovery time	t_{RCS}			5			6			8	ns	
Address access time	t_{AA}			8			10			15	ns	
Write Operation												
Write pulse width	t_W	6			10			15			ns	
Data setup time	t_{WSD}	1			2			2			ns	
Data hold time	t_{WHD}	1			2			2			ns	
Address setup time	t_{WSA}	1			3			3			ns	
Address hold time	t_{WHA}	1			2			2			ns	
Chip select setup time	t_{WSCS}	1			2			2			ns	
Chip select hold time	t_{WHCS}	1			2			2			ns	
Write disable time	t_{WS}			5			6			8	ns	
Write recovery time	t_{WR}			8			10			10	ns	
Output Rise and Fall Times												
Output rise time	t_R		2			2			2		ns	
Output fall time	t_F		2			2			2		ns	

Notes:

(1) The device under test is mounted in a test socket and measured at a thermal equilibrium established with a transverse air flow maintained at greater than 2.0 m/s.

(2) See figures 1 and 2 for loading conditions and input pulse timing. Input pulse levels = −1.7 to −0.9 V; input rise and fall times (measured between 20% and 80% or 80% and 20%) = 2 ns; input and output timing reference levels = 50%.

Figure 1. Loading Conditions Test Circuit

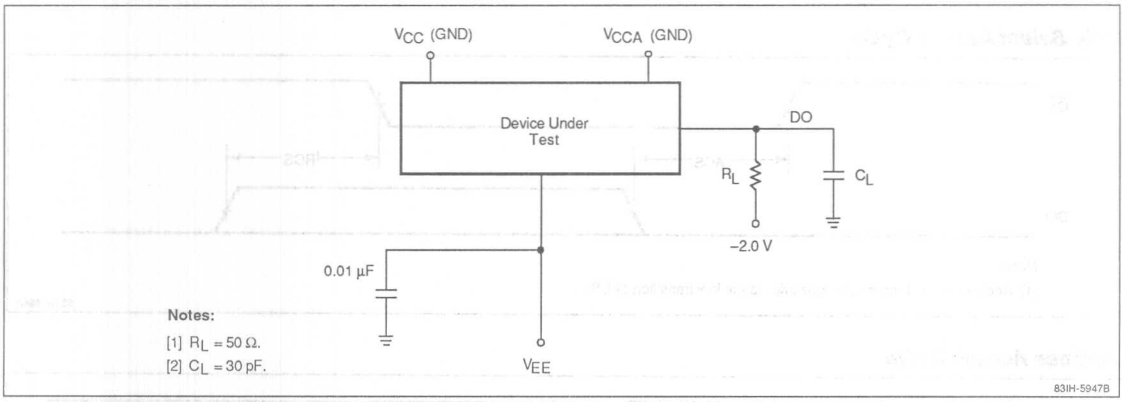
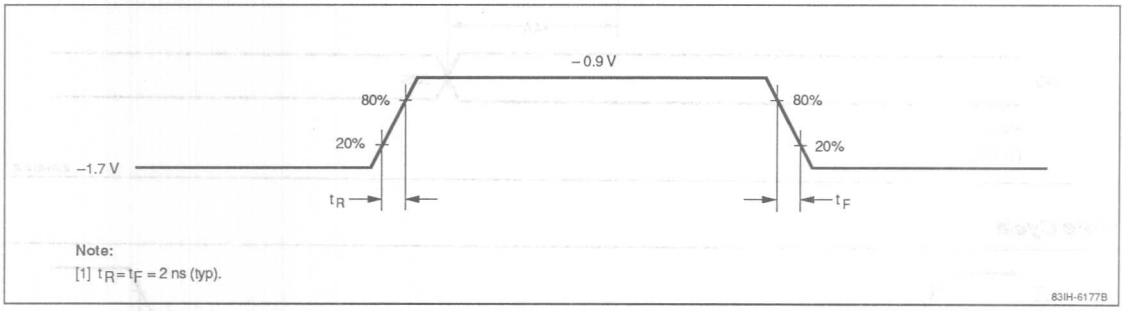


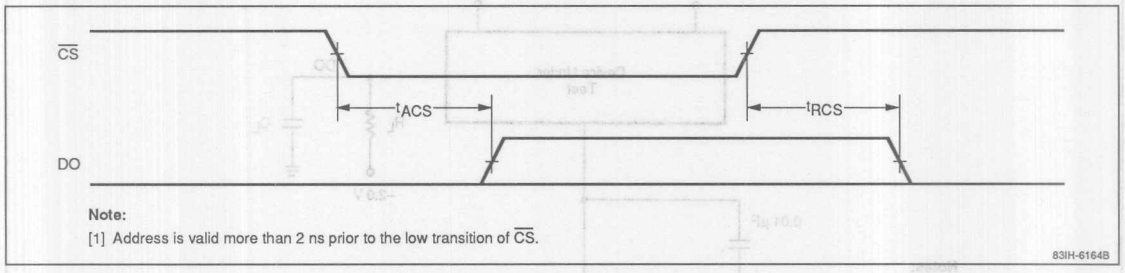
Figure 2. Input Pulse



8

Timing Waveforms

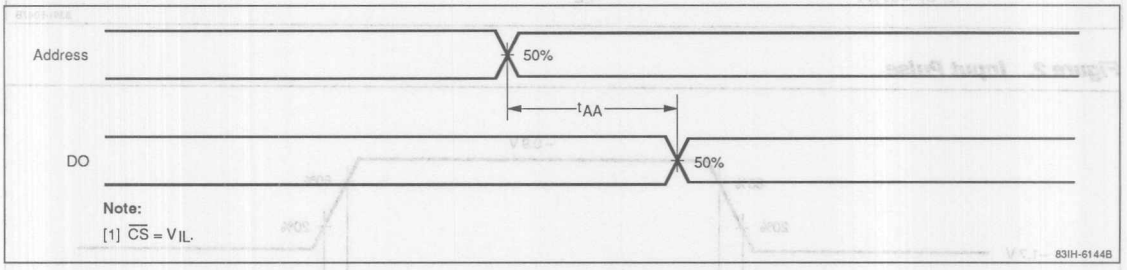
Chip Select Access Cycle



Note:
[1] Address is valid more than 2 ns prior to the low transition of $\overline{CS}$.

83IH-6164B

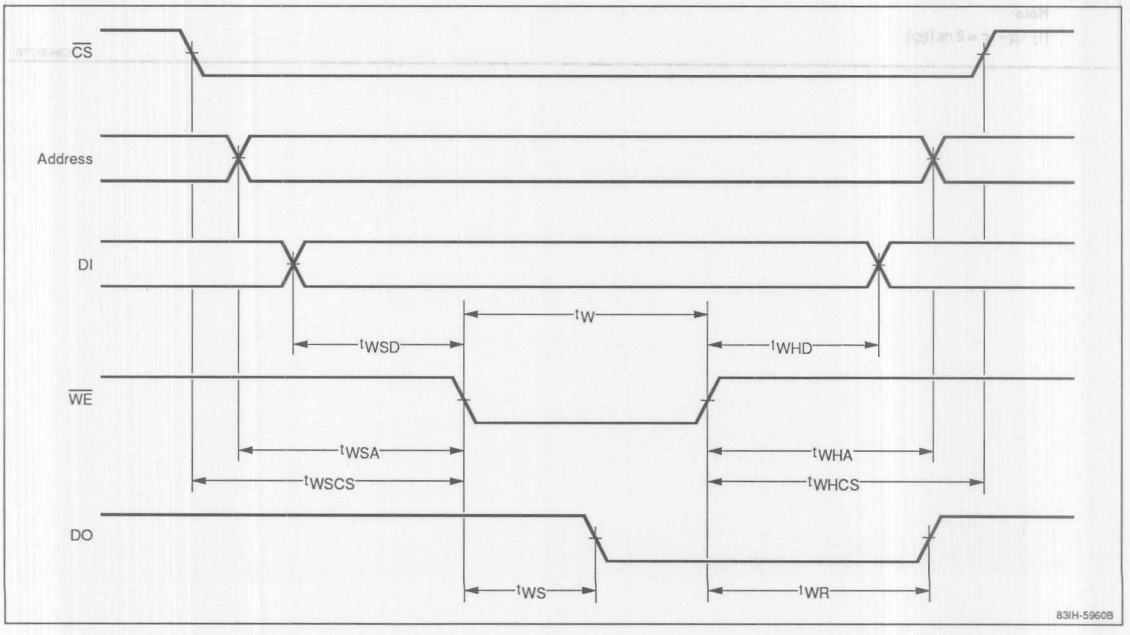
Address Access Cycle



Note:
[1] $\overline{CS} = V_{IL}$.

83IH-6144B

Write Cycle



83IH-5960B

Description

The μPB10474A is a very high-speed 10K interface ECL RAM organized as 1,024 words by 4 bits and designed with noninverted, open-emitter outputs and low power consumption. Two versions with access times of 5 and 6 ns maximum are available in hermetic, 400-mil, 24-pin cerdip packaging.

Features

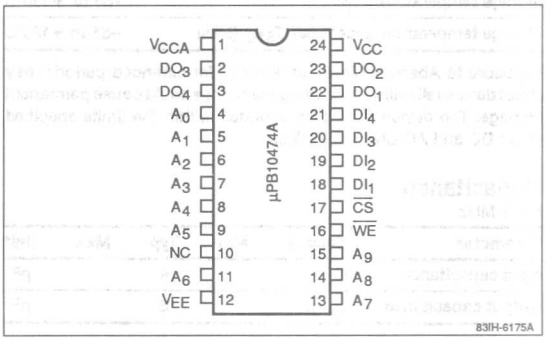
- 1,024-word x 4-bit organization
- 10K ECL interface
- Noninverted, open-emitter outputs
- Fast access times
- Low power consumption
- 400-mil, 24-pin cerdip packaging

Ordering Information

Part Number	Access Time (max)	Package
μPB10474AD-5	5 ns	24-pin cerdip
D-6	6 ns	

Pin Configurations

24-Pin Cerdip



Pin Identification

Symbol	Function
A_0 - A_9	Address inputs
DI_1 - DI_4	Data inputs
DO_1 - DO_4	Data outputs
$\overline{WE}$	Write enable (active low)
$\overline{CS}$	Chip select (active low)
V_{CC}	Power supply (current switches and bias driver)
V_{CCA}	Power supply (output devices)
V_{EE}	–5.2-volt power supply
NC	No connection

8

Absolute Maximum Ratings

$V_{CC} = V_{CCA} = 0$ V

Supply voltage, V_{EE} to V_{CC}	−7.0 to +0.5 V
Input voltage, V_{IN}	V_{EE} to +0.5 V
Output current, I_{OUT}	−30 to +0.1 mA
Storage temperature, T_{STG}	−65 to +150°C
Storage temperature under bias, T_{STG} (bias)	−55 to +125°C

Exposure to Absolute Maximum Ratings for extended periods may affect device reliability; exceeding the ratings could cause permanent damage. The device should be operated within the limits specified under DC and AC Characteristics.

Capacitance

f = 1 MHz

Parameter	Symbol	Min	Typ	Max	Unit
Input capacitance	C_{IN}		4		pF
Output capacitance	C_{OUT}		5		pF

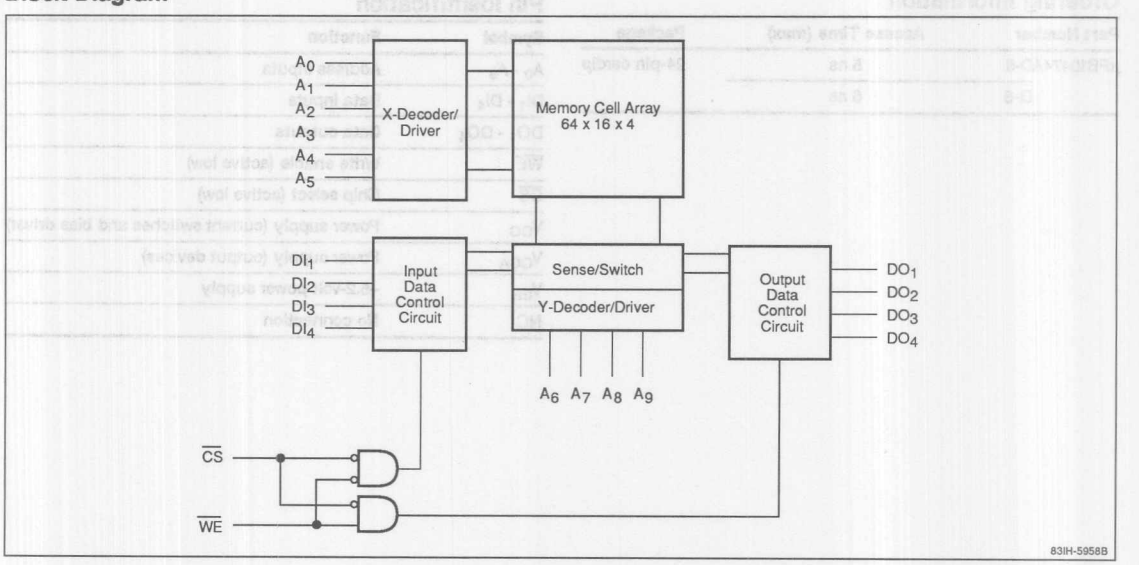
Truth Table

$\overline{CS}$	$\overline{WE}$	D_{IN}	Output	Function
H	X	X	L	Not selected
L	L	L	L	Write 0
L	L	H	L	Write 1
L	H	X	D_{OUT}	Read

Notes:

(1) X = don't care.

Block Diagram



DC Characteristics

T_A = 0 to +75°C; V_{EE} = −5.2 V; output load = 50 Ω to −2.0 V; V_{CC} = V_{CCA} = 0 V

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions
Output voltage, high	V_{OH}	−1000		−840	mV	V_{IN} = V_{IH} max or V_{IL} min; T_A = 0°C
		−960		−810	mV	V_{IN} = V_{IH} max or V_{IL} min; T_A = 25°C
		−900		−720	mV	V_{IN} = V_{IH} max or V_{IL} min; T_A = 75°C
Output voltage, low	V_{OL}	−1870		−1665	mV	V_{IN} = V_{IH} max or V_{IL} min; T_A = 0°C
		−1850		−1650	mV	V_{IN} = V_{IH} max or V_{IL} min; T_A = 25°C
		−1830		−1625	mV	V_{IN} = V_{IH} max or V_{IL} min; T_A = 75°C
Output threshold voltage, high	V_{OHC}	−1020			mV	V_{IN} = V_{IH} min or V_{IL} max; T_A = 0°C
		−980			mV	V_{IN} = V_{IH} min or V_{IL} max; T_A = 25°C
		−920			mV	V_{IN} = V_{IH} min or V_{IL} max; T_A = 75°C
Output threshold voltage, low	V_{OLC}			−1645	mV	V_{IN} = V_{IH} min or V_{IL} max; T_A = 0°C
				−1630	mV	V_{IN} = V_{IH} min or V_{IL} max; T_A = 25°C
				−1605	mV	V_{IN} = V_{IH} min or V_{IL} max; T_A = 75°C
Input voltage, high	V_{IH}	−1145		−840	mV	For all inputs: T_A = 0°C
		−1105		−810	mV	For all inputs: T_A = 25°C
		−1045		−720	mV	For all inputs: T_A = 75°C
Input voltage, low	V_{IL}	−1870		−1490	mV	For all inputs: T_A = 0°C
		−1850		−1475	mV	For all inputs: T_A = 25°C
		−1830		−1450	mV	For all inputs: T_A = 75°C
Input current, high	I_{IH}			220	μA	V_{IN} = V_{IH} max
Input current, low	I_{IL}	0.5		170	μA	For $\overline{CS}$: V_{IN} = V_{IL} min
		−50			μA	For all others: V_{IN} = V_{IL} min
Supply current	I_{EE}	−250			mA	All inputs and outputs open

Notes:

(1) The device under test is mounted in a test socket and measured at a thermal equilibrium established with a transverse air flow maintained at greater than 2.0 m/s.

8

AC Characteristics

T_A = 0 to +75°C; V_{EE} = −5.2 V ± 5%; output load = 50 Ω to −2.0 V; V_{CC} = V_{CCA} = 0 V

		μPB10474A-5			μPB10474A-6				
Parameter	**Symbol**	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**	**Unit**	**Test Conditions**
Read Operation									
Address access time	t_{AA}			5			6	ns	
Chip select recovery time	t_{RCS}			3			4	ns	
Chip select access time	t_{ACS}			3			4	ns	
Write Operation									
Write pulse width	t_W	5			6			ns	
Data setup time	t_{WSD}	1			1			ns	
Data hold time	t_{WHD}	1			1			ns	
Address setup time	t_{WSA}	1			1			ns	
Address hold time	t_{WHA}	1			1			ns	
Chip select setup time	t_{WSCS}	1			1			ns	
Chip select hold time	t_{WHCS}	1			1			ns	
Write disable time	t_{WS}			3			4	ns	
Write recovery time	t_{WR}			6			7	ns	
Output Rise and Fall Times									
Output rise time	t_R		2			2		ns	
Output fall time	t_F		2			2		ns	

Notes:

(1) The device under test is mounted in a test socket and measured at a thermal equilibrium established with a transverse air flow maintained at greater than 2.0 m/s.

(2) See figures 1 and 2 for loading conditions and input pulse timing. Input pulse levels = −1.7 to −0.9 V; input rise and fall times (measured between 20% and 80% or 80% and 20%) = 2 ns; input and output timing reference levels = 50%.

Figure 1. Loading Conditions Test Circuit

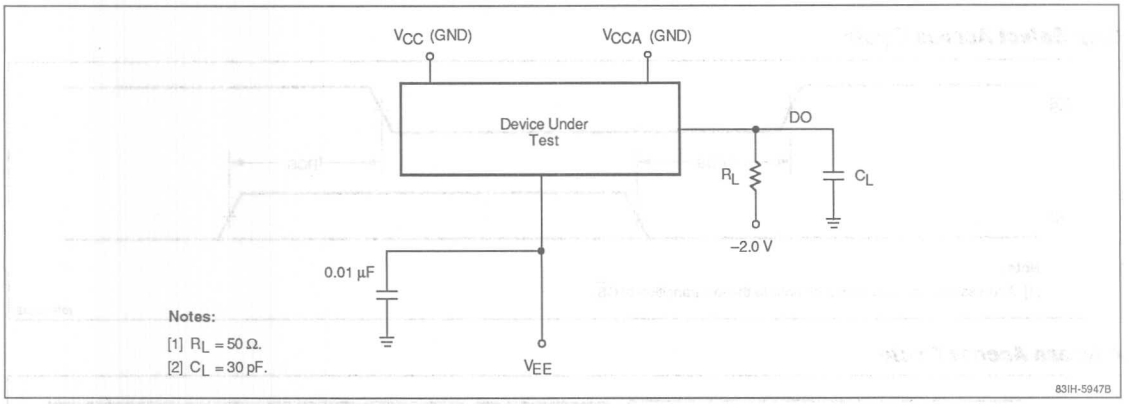
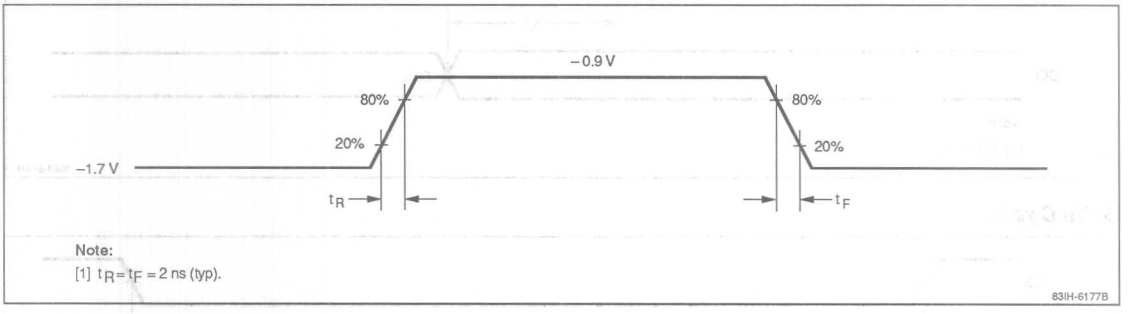


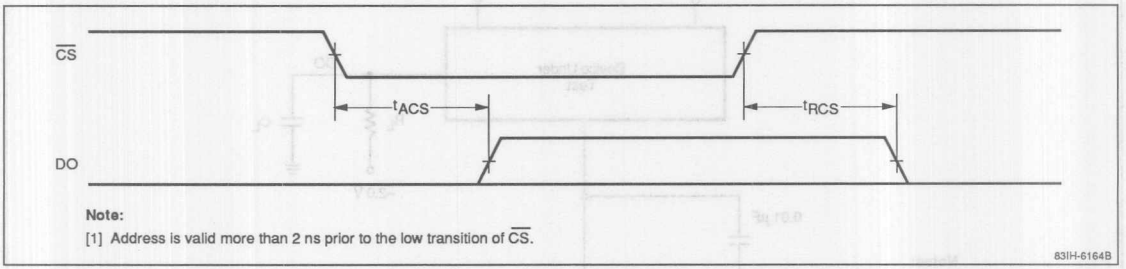
Figure 2. Input Pulse



8

Timing Waveforms

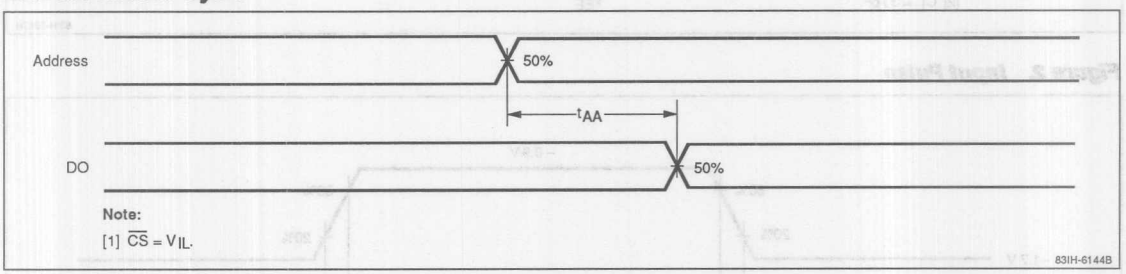
Chip Select Access Cycle



Note:
[1] Address is valid more than 2 ns prior to the low transition of $\overline{CS}$.

83IH-6164B

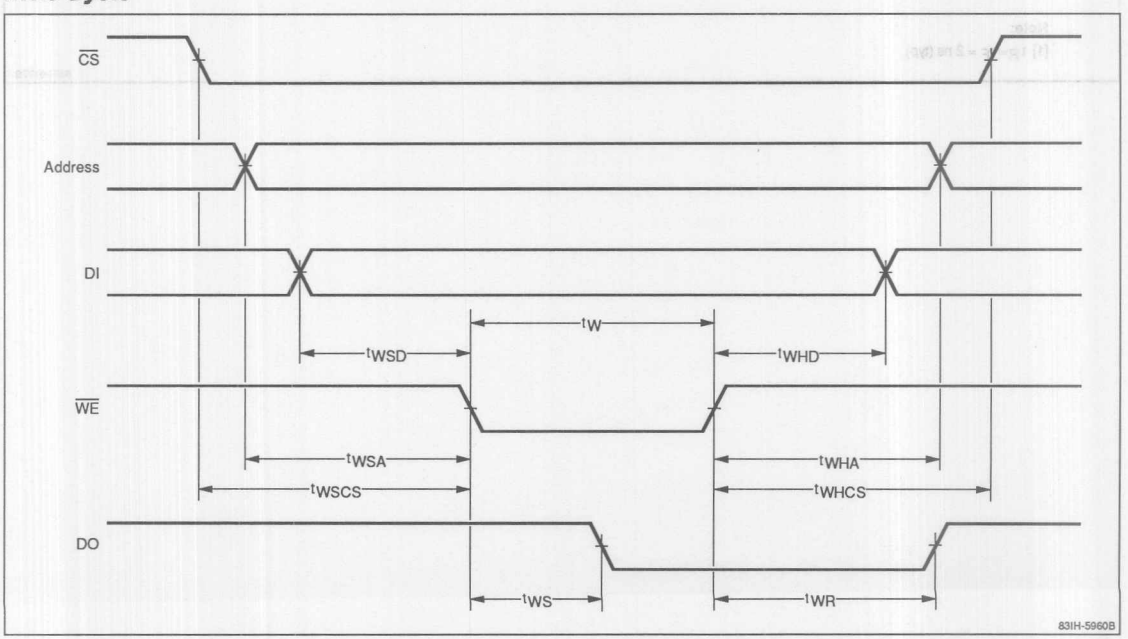
Address Access Cycle



Note:
[1] $\overline{CS} = V_{IL}$.

83IH-6144B

Write Cycle



83IH-5960B

μPB10474E
1,024 x 4-Bit
10K ECL RAM

PRELIMINARY INFORMATION

Description

The μPB10474E is a very high-speed 10K interface ECL RAM organized as 1,024 words by 4 bits and designed with noninverted, open-emitter outputs and low power consumption. Two versions with access times of 3 and 4 ns maximum are available in hermetic, 400-mil, 24-pin cerdip packaging.

Features

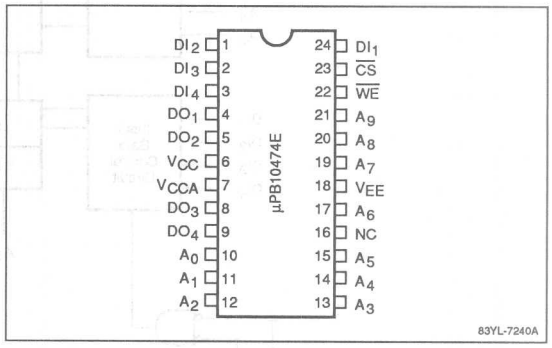
- 1,024-word x 4-bit organization
- 10K ECL interface
- Noninverted, open-emitter outputs
- Fast access times
- Low power consumption
- 400-mil, 24-pin cerdip packaging

Ordering Information

Part Number	Access Time (max)	Package
μPB10474ED-3	3 ns	24-pin cerdip
D-4	4 ns	

Pin Configuration

24-Pin Cerdip

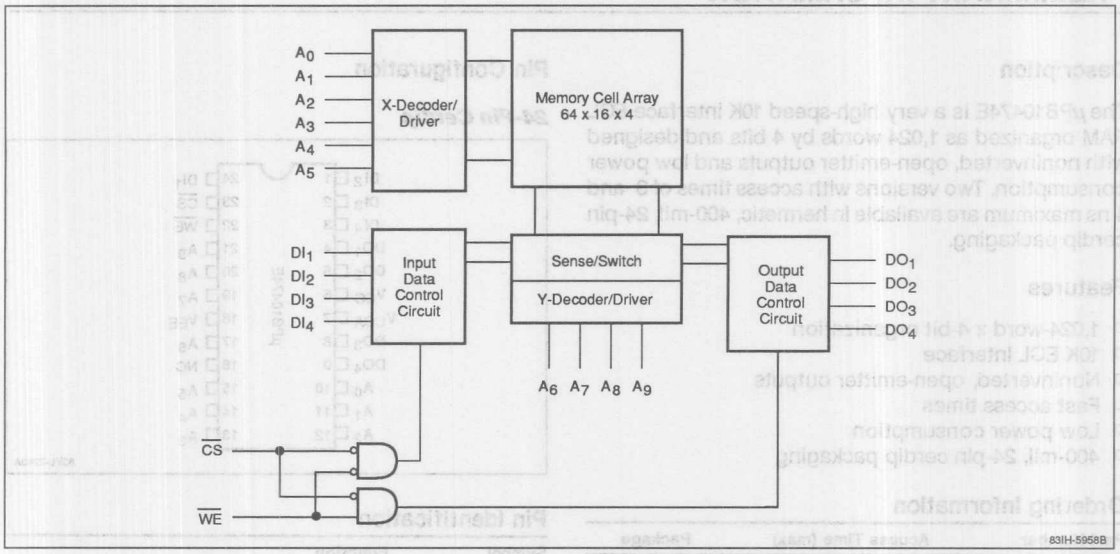


Pin Identification

Symbol	Function
A_0 - A_9	Address inputs
DI_1 - DI_4	Data inputs
DO_1 - DO_4	Data outputs
$\overline{WE}$	Write enable (active low)
$\overline{CS}$	Chip select (active low)
V_{CC}	Power supply (current switches and bias driver)
V_{CCA}	Power supply (output devices)
V_{EE}	–5.2-volt power supply
NC	No connection

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Block Diagram



Absolute Maximum Ratings

$V_{CC} = V_{CCA} = 0$ V

Supply voltage, V_{EE} to V_{CC}	−7.0 to +0.5 V
Input voltage, V_{IN}	V_{EE} to +0.5 V
Output current, I_{OUT}	−30 to +0.1 mA
Storage temperature, T_{STG}	−65 to +150°C
Storage temperature under bias, T_{STG} (bias)	−55 to +125°C

Exposure to Absolute Maximum Ratings for extended periods may affect device reliability; exceeding the ratings could cause permanent damage. The device should be operated within the limits specified under DC and AC Characteristics.

Capacitance

f = 1 MHz

Parameter	Symbol	Min	Typ	Max	Unit
Input capacitance	C_{IN}		4		pF
Output capacitance	C_{OUT}		5		pF

Truth Table

$\overline{CS}$	$\overline{WE}$	D_{IN}	Output	Function
H	X	X	L	Not selected
L	L	L	L	Write 0
L	L	H	L	Write 1
L	H	X	D_{OUT}	Read

Notes:

(1) X = don't care.

DC Characteristics

T_A = 0 to +75°C; V_{EE} = −5.2 V; output load = 50 Ω to −2.0 V; V_{CC} = V_{CCA} = 0 V

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions
Output voltage, high	V_{OH}	−1000		−840	mV	V_{IN} = V_{IH} max or V_{IL} min; T_A = 0°C
		−960		−810	mV	V_{IN} = V_{IH} max or V_{IL} min; T_A = 25°C
		−900		−720	mV	V_{IN} = V_{IH} max or V_{IL} min; T_A = 75°C
Output voltage, low	V_{OL}	−1870		−1665	mV	V_{IN} = V_{IH} max or V_{IL} min; T_A = 0°C
		−1850		−1650	mV	V_{IN} = V_{IH} max or V_{IL} min; T_A = 25°C
		−1830		−1625	mV	V_{IN} = V_{IH} max or V_{IL} min; T_A = 75°C
Output threshold voltage, high	V_{OHC}	−1020			mV	V_{IN} = V_{IH} min or V_{IL} max; T_A = 0°C
		−980			mV	V_{IN} = V_{IH} min or V_{IL} max; T_A = 25°C
		−920			mV	V_{IN} = V_{IH} min or V_{IL} max; T_A = 75°C
Output threshold voltage, low	V_{OLC}			−1645	mV	V_{IN} = V_{IH} min or V_{IL} max; T_A = 0°C
				−1630	mV	V_{IN} = V_{IH} min or V_{IL} max; T_A = 25°C
				−1605	mV	V_{IN} = V_{IH} min or V_{IL} max; T_A = 75°C
Input voltage, high	V_{IH}	−1145		−840	mV	For all inputs: T_A = 0°C
		−1105		−810	mV	For all inputs: T_A = 25°C
		−1045		−720	mV	For all inputs: T_A = 75°C
Input voltage, low	V_{IL}	−1870		−1490	mV	For all inputs: T_A = 0°C
		−1850		−1475	mV	For all inputs: T_A = 25°C
		−1830		−1450	mV	For all inputs: T_A = 75°C
Input current, high	I_{IH}			220	μA	V_{IN} = V_{IH} max
Input current, low	I_{IL}	0.5		170	μA	For $\overline{CS}$: V_{IN} = V_{IL} min
		−50			μA	For all others: V_{IN} = V_{IL} min
Supply current	I_{EE}	−330			mA	All inputs and outputs open

Notes:

(1) The device under test is mounted in a test socket and measured at a thermal equilibrium established with a transverse air flow maintained at greater than 2.0 m/s.

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AC Characteristics

T_A = 0 to +75°C; V_{EE} = −5.2 V ± 5%; output load = 50 Ω to −2.0 V; V_{CC} = V_{CCA} = 0 V

		μPB10474E-3			μPB10474E-4				
Parameter	**Symbol**	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**	**Unit**	**Test Conditions**
Read Operation									
Address access time	t_{AA}			3			4	ns	
Chip select recovery time	t_{RCS}			2			3	ns	
Chip select access time	t_{ACS}			2			3	ns	
Write Operation									
Write pulse width	t_W	5			6			ns	
Data setup time	t_{WSD}	0.5			0.5			ns	
Data hold time	t_{WHD}	0.5			0.5			ns	
Address setup time	t_{WSA}	0.5			0.5			ns	
Address hold time	t_{WHA}	0.5			0.5			ns	
Chip select setup time	t_{WSCS}	0.5			0.5			ns	
Chip select hold time	t_{WHCS}	0.5			0.5			ns	
Write disable time	t_{WS}			2			3	ns	
Write recovery time	t_{WR}			4			5	ns	
Output Rise and Fall Times									
Output rise time	t_R		2			2		ns	
Output fall time	t_F		2			2		ns	

Notes:

(1) The device under test is mounted in a test socket and measured at a thermal equilibrium established with a transverse air flow maintained at greater than 2.0 m/s.

(2) See figures 1 and 2 for loading conditions and input pulse timing. Input pulse levels = −1.7 to −0.9 V; input rise and fall times (measured between 20% and 80% or 80% and 20%) = 2 ns; input and output timing reference levels = 50%.

Figure 1. Loading Conditions Test Circuit

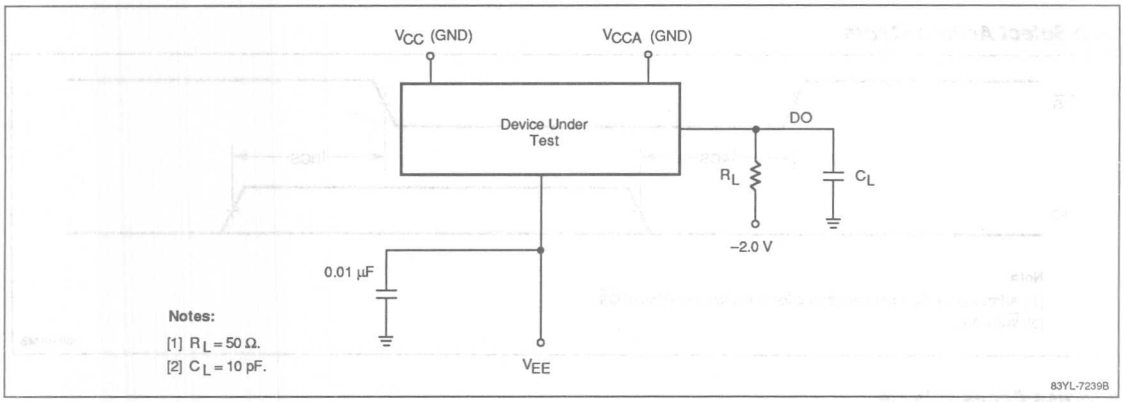
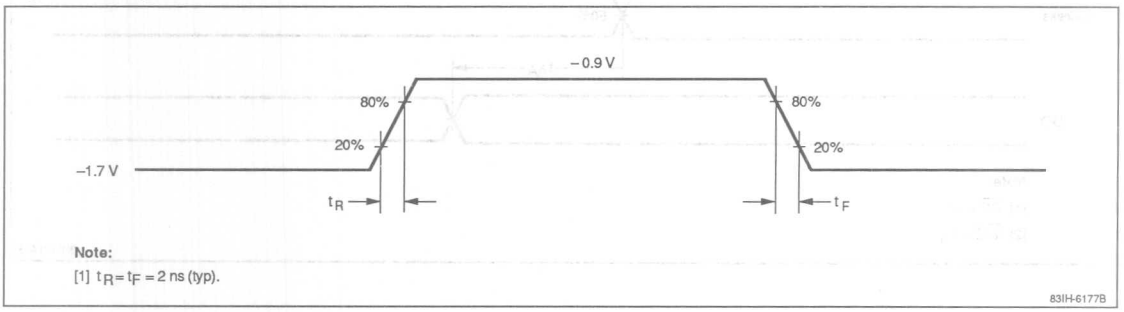


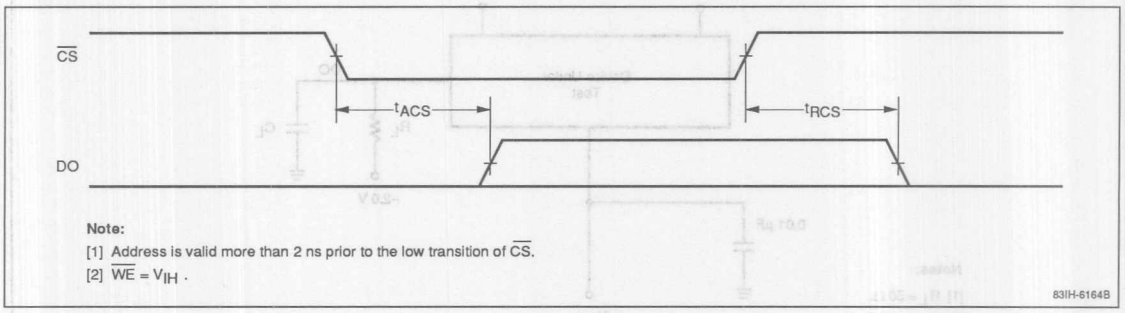
Figure 2. Input Pulse



8

Timing Waveforms

Chip Select Access Cycle

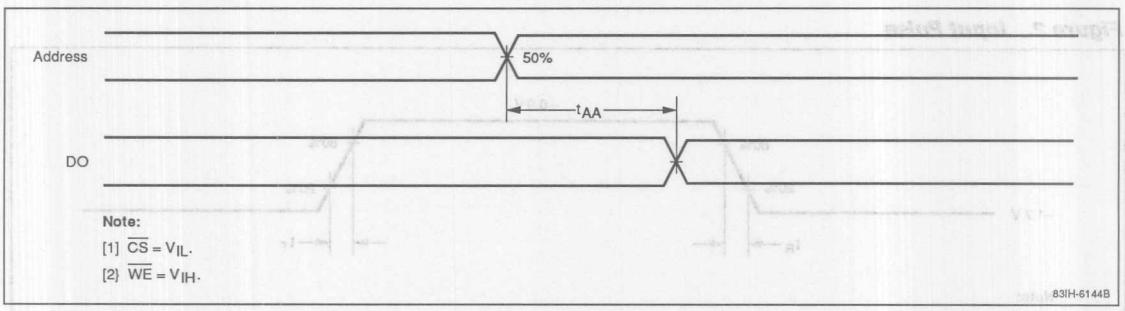


Note:

[1] Address is valid more than 2 ns prior to the low transition of $\overline{CS}$.

[2] $\overline{WE} = V_{IH}$.

Address Access Cycle



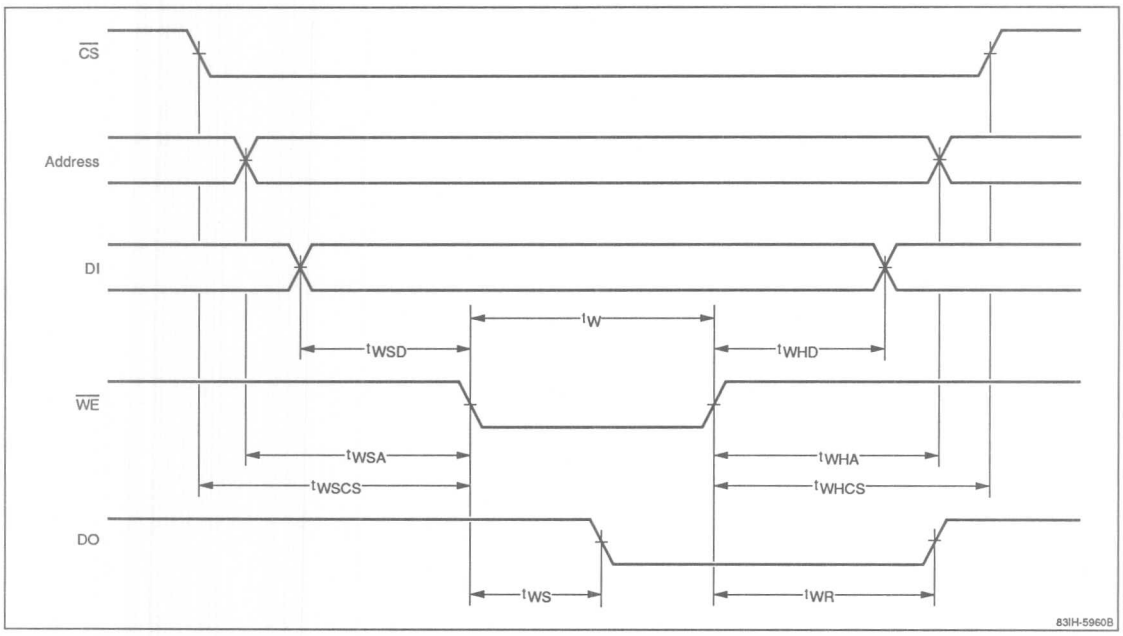
Note:

[1] $\overline{CS} = V_{IL}$.

[2] $\overline{WE} = V_{IH}$.

Timing Waveforms (cont)

Write Cycle



8

Description

The μPB10480 is a very high-speed 10K interface ECL RAM organized as 16,384 words by 1 bit and designed with noninverted, open-emitter outputs and low power consumption. Two versions with fast access times of 10 ns and 15 ns maximum are available in hermetic, 300-mil, 20-pin cerdip or 20-pin ceramic flatpack packaging.

Features

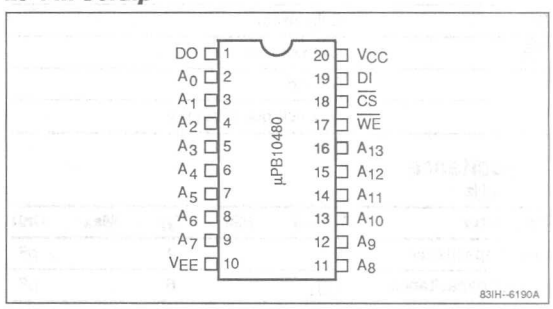
- 16,384-word x 1-bit organization
- 10K ECL interface
- Noninverted, open-emitter outputs
- Fast access times
- Low power consumption
- 300-mil, 20-pin cerdip or 20-pin ceramic flatpack packaging

Ordering Information

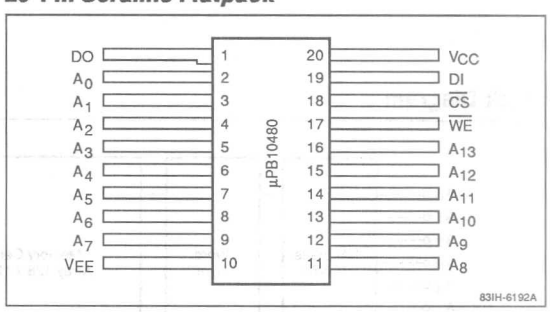
Part Number	Access Time (max)	Power Consumption (max)	Package
μPB10480D-10	10 ns	1.4 W	20-pin cerdip
D-15	15 ns	1.3 W	
μPB10480B-10	10 ns	1.4 W	20-pin ceramic flatpack
B-15	15 ns	1.3 W	

Pin Configurations

20-Pin Cerdip



20-Pin Ceramic Flatpack



8

Pin Identification

Symbol	Function
A_0 - A_{13}	Address inputs
DI	Data input
DO	Data output
$\overline{CS}$	Chip select
$\overline{WE}$	Write enable
V_{CC}	Ground
V_{EE}	–5.2-volt power supply

Capacitance

f = 1 MHz

Parameter	Symbol	Min	Typ	Max	Unit
Input capacitance	C_{IN}		4		pF
Output capacitance	C_{OUT}		6		pF

Absolute Maximum Ratings

Supply voltage, V_{EE}	–7.0 to +0.5 V
Input voltage, V_{IN}	V_{EE} to +0.5 V
Output current, I_{OUT}	–30 to +0.1 mA
Storage temperature, T_{STG}	–65 to +150°C
Storage temperature under bias, T_{STG} (bias)	–55 to +125°C

Exposure to Absolute Maximum Ratings for extended periods may affect device reliability; exceeding the ratings could cause permanent damage. The device should be operated within the limits specified under DC and AC Characteristics.

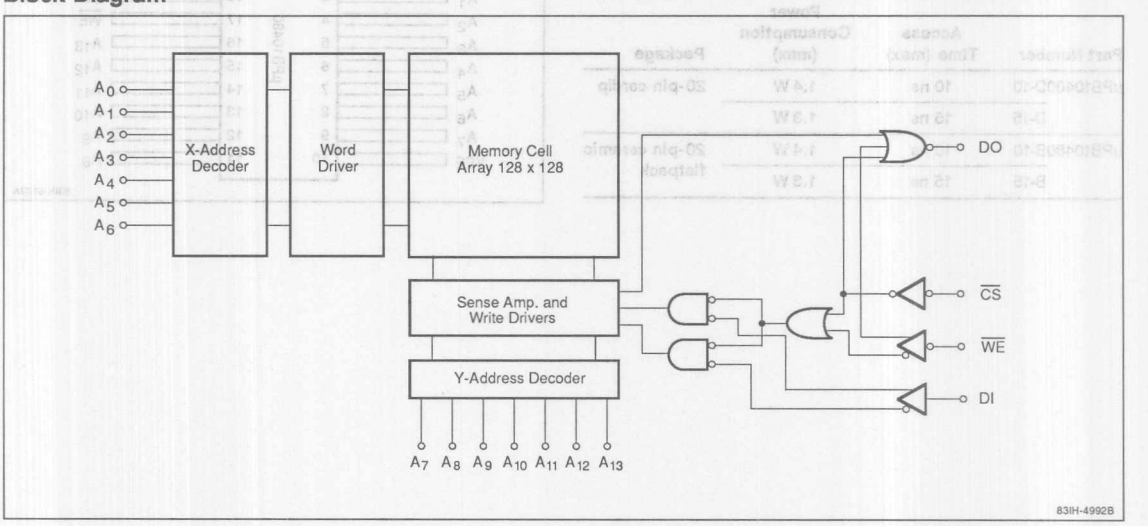
Truth Table

$\overline{CS}$	$\overline{WE}$	D_{IN}	Output	Mode
H	X	X	L	Not selected
L	L	L	L	Write 0
L	L	H	L	Write 1
L	H	X	D_{OUT}	Read

Notes:

(1) X = don't care.

Block Diagram



DC Characteristics

T_A = 0 to +75°C; V_{EE} = −5.2 V; output load = 50 Ω to −2.0 V

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions
Output voltage, high	V_{OH}	−1000		−840	mV	V_{IN} = V_{IH} max or V_{IL} min; T_A = 0°C
		−960		−810	mV	V_{IN} = V_{IH} max or V_{IL} min; T_A = 25°C
		−900		−720	mV	V_{IN} = V_{IH} max or V_{IL} min; T_A = 75°C
Output voltage, low	V_{OL}	−1870		−1665	mV	V_{IN} = V_{IH} max or V_{IL} min; T_A = 0°C
		−1850		−1650	mV	V_{IN} = V_{IH} max or V_{IL} min; T_A = 25°C
		−1830		−1625	mV	V_{IN} = V_{IH} max or V_{IL} min; T_A = 75°C
Output threshold voltage, high	V_{OHC}	−1020			mV	V_{IN} = V_{IH} min or V_{IL} max; T_A = 0°C
		−980			mV	V_{IN} = V_{IH} min or V_{IL} max; T_A = 25°C
		−920			mV	V_{IN} = V_{IH} min or V_{IL} max; T_A = 75°C
Output threshold voltage, low	V_{OLC}			−1645	mV	V_{IN} = V_{IH} min or V_{IL} max; T_A = 0°C
				−1630	mV	V_{IN} = V_{IH} min or V_{IL} max; T_A = 25°C
				−1605	mV	V_{IN} = V_{IH} min or V_{IL} max; T_A = 75°C
Input voltage, high	V_{IH}	−1145		−840	mV	For all inputs: T_A = 0°C
		−1105		−810	mV	For all inputs: T_A = 25°C
		−1045		−720	mV	For all inputs: T_A = 75°C
Input voltage, low	V_{IL}	−1870		−1490	mV	For all inputs: T_A = 0°C
		−1850		−1475	mV	For all inputs: T_A = 25°C
		−1830		−1450	mV	For all inputs: T_A = 75°C
Input current, high	I_{IH}			220	μA	V_{IN} = V_{IH} max
Input current, low	I_{IL}	0.5		170	μA	For $\overline{CS}$: V_{IN} = V_{IL} min
		−50			μA	For all others: V_{IN} = V_{IL} min
Supply current	I_{EE}	−260			mA	For μPB10480-10: all inputs and outputs open
		−240			mA	For μPB10480-15: all inputs and outputs open

Notes:

(1) The device under test is mounted in a test socket and measured at a thermal equilibrium established with a transverse air flow maintained at greater than 2.0 m/s.

8

AC Characteristics

T_A = 0 to +75°C; V_{EE} = −5.2 V ±5%

		μPB10480-10			μPB10480-15				
Parameter	Symbol	Min	Typ	Max	Min	Typ	Max	Unit	Test Conditions
Read Operation									
Address access time	t_{AA}			10			15	ns	
Chip select recovery time	t_{RCS}			5			8	ns	
Chip select access time	t_{ACS}			5			8	ns	
Write Operation									
Write pulse width	t_W	10			15			ns	
Data setup time	t_{WSD}	2			3			ns	
Data hold time	t_{WHD}	1			2			ns	
Address setup time	t_{WSA}	2			3			ns	
Address hold time	t_{WHA}	1			2			ns	
Chip select setup time	t_{WSCS}	2			3			ns	
Chip select hold time	t_{WHCS}	1			2			ns	
Write disable time	t_{WS}			5			8	ns	
Write recovery time	t_{WR}			11			17	ns	
Output Rise and Fall Times									
Output rise time	t_R		2			2		ns	
Output fall time	t_F		2			2		ns	

Notes:

(1) The device under test is mounted in a test socket and measured at a thermal equilibrium established with a transverse air flow maintained at greater than 2.0 m/s.

(2) Input pulse levels = −1.7 to −0.9 V; input rise and fall times (measured between 20% and 80% or 80% to 20%) = 2.5 ns; input and output timing reference level = 50%.

Figure 1. Loading Conditions Test Circuit

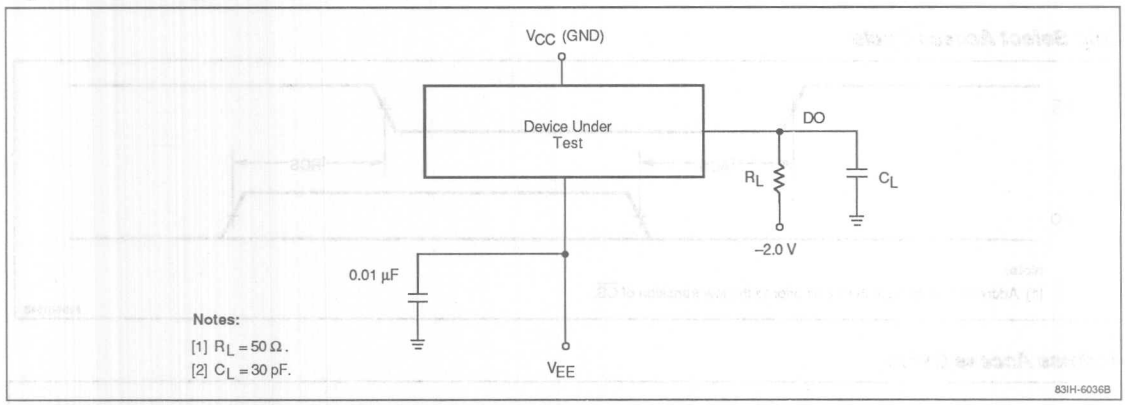
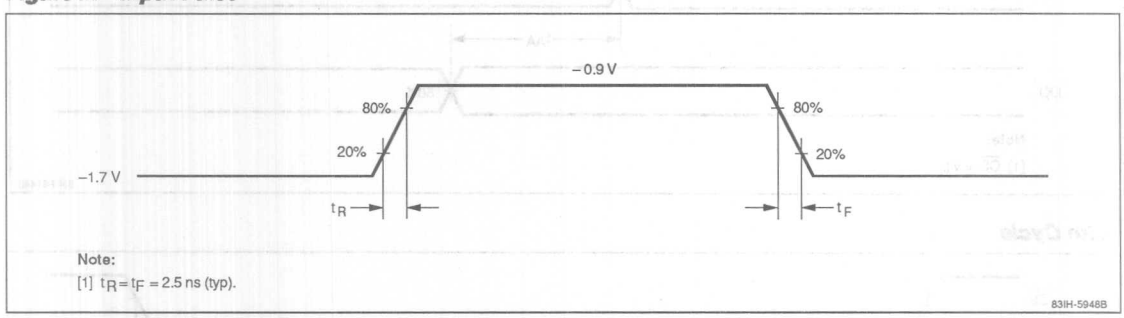


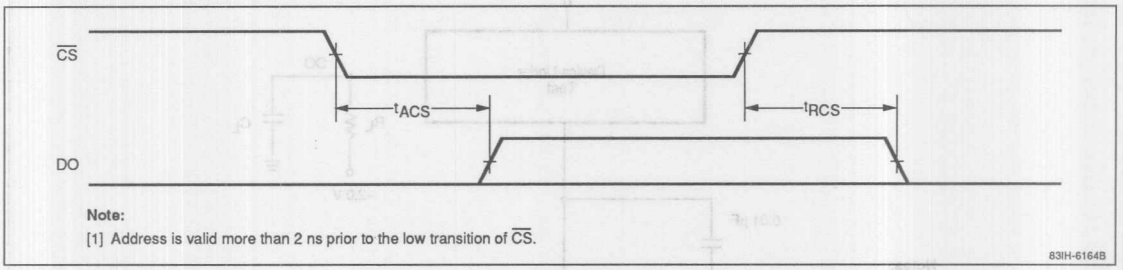
Figure 2. Input Pulse



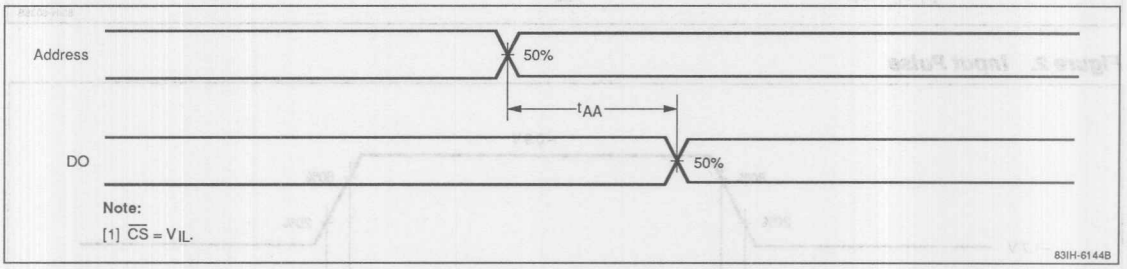
8

Timing Waveforms

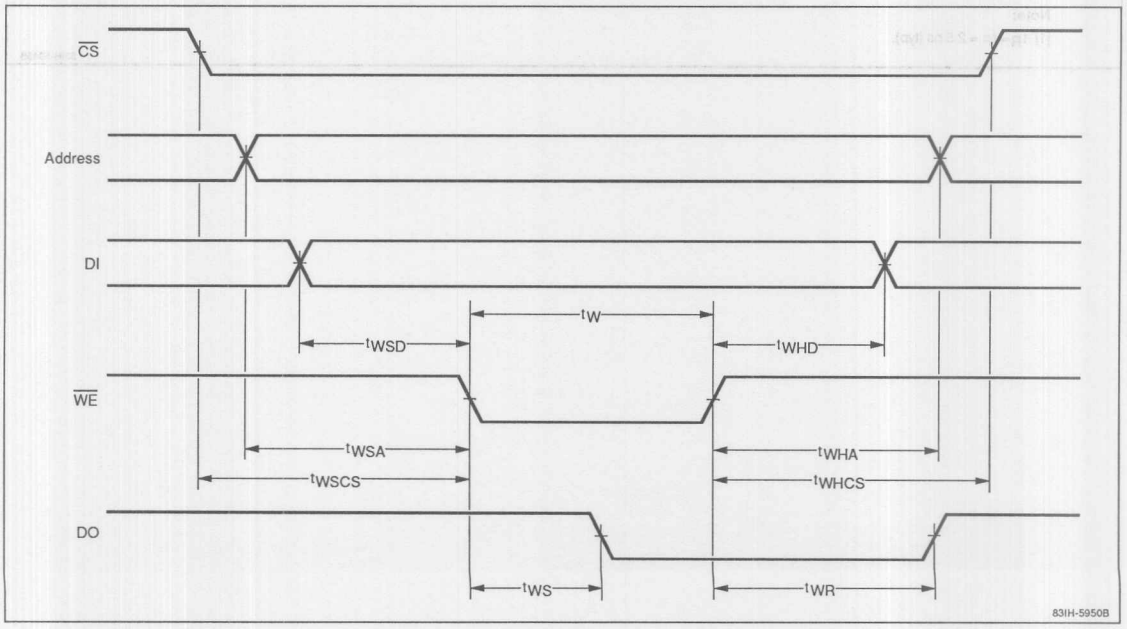
Chip Select Access Cycle



Address Access Cycle



Write Cycle



NEC Electronics Inc.

μPB10484
4,096 x 4-Bit
10K ECL RAM

Description

The μPB10484 is a very high-speed 10K interface ECL RAM organized as 4,096 words by 4 bits and designed with noninverted, open-emitter outputs and low power consumption. Two versions with access times of 10 and 15 ns maximum are available. The μPB10484 is packaged in a hermetic, 400-mil, 28-pin cerdip or 28-pin ceramic flatpack.

Features

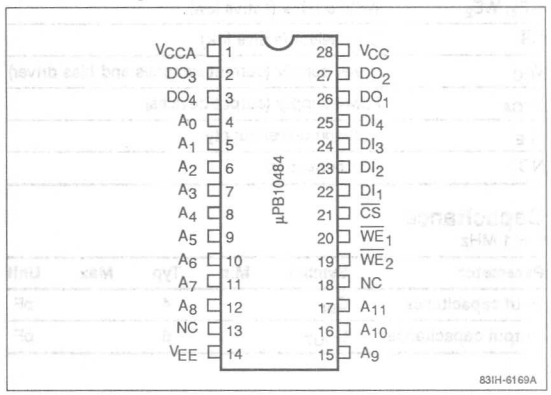
- 4,096-word x 4-bit organization
- 10K ECL interface
- Noninverted, open-emitter outputs
- Low power consumption of 1.4 W maximum
- Fast access times of 10 and 15 ns maximum
- 400-mil, 28-pin cerdip or 28-pin ceramic flatpack packaging

Ordering Information

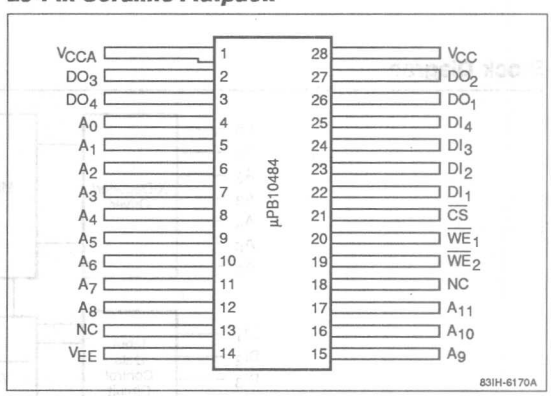
Part Number	Access Time (max)	Package
μPB10484D-10	10 ns	28-pin cerdip
D-15	15 ns	
μPB10484B-10	10 ns	28-pin ceramic flatpack
B-15	15 ns	

Pin Configurations

28-Pin Cerdip



28-Pin Ceramic Flatpack



8

Pin Identification

Symbol	Function
A_0 - A_{11}	Address inputs
DI_1 - DI_4	Data inputs
DO_1 - DO_4	Data outputs
$\overline{WE}_1$, $\overline{WE}_2$	Write enable (active low)
$\overline{CS}$	Chip select (active low)
V_{CC}	Power supply (current switches and bias driver)
V_{CCA}	Power supply (output devices)
V_{EE}	–5.2-volt power supply
NC	No connection

Capacitance

f = 1 MHz

Parameter	Symbol	Min	Typ	Max	Unit
Input capacitance	C_{IN}		4		pF
Output capacitance	C_{OUT}		6		pF

Absolute Maximum Ratings

$V_{CC} = V_{CCA} = 0$ V

Supply voltage, V_{EE}	–7.0 to +0.5 V
Input voltage, V_{IN}	V_{EE} to +0.5 V
Output current, I_{OUT}	–30 to +0.1 mA
Storage temperature, T_{STG}	–65 to +150°C
Storage temperature under bias, T_{STG} (bias)	–55 to +125°C

Exposure to Absolute Maximum Ratings for extended periods may affect device reliability; exceeding the ratings could cause permanent damage. The device should be operated within the limits specified under DC and AC Characteristics.

Truth Table

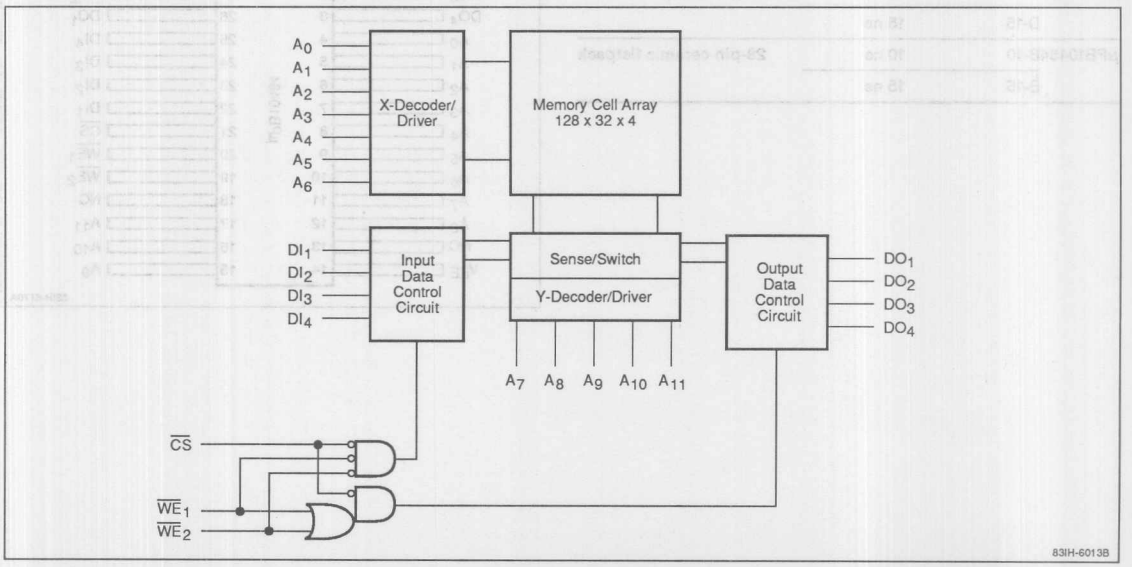
$\overline{CS}$	$\overline{WE}$	D_{IN}	Output	Mode
H	X	X	L	Not selected
L	L (Note 2)	L	L	Write 0
L	L (Note 2)	H	L	Write 1
L	H (Note 2)	X	D_{OUT}	Read

Notes:

(1) X = don't care.

(2) Both $\overline{WE}_1$ and $\overline{WE}_2$ must be low to initiate write operation. For read operation, either $\overline{WE}_1$ or $\overline{WE}_2$ or both must be high.

Block Diagram



DC Characteristics

T_A = 0 to +75°C; V_{EE} = −5.2 V; output load = 50 Ω to −2.0 V; V_{CC} = V_{CCA} = 0 V

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions
Output voltage, high	V_{OH}	−1000		−840	mV	V_{IN} = V_{IH} max or V_{IL} min; T_A = 0°C
		−960		−810	mV	V_{IN} = V_{IH} max or V_{IL} min; T_A = 25°C
		−900		−720	mV	V_{IN} = V_{IH} max or V_{IL} min; T_A = 75°C
Output voltage, low	V_{OL}	−1870		−1665	mV	V_{IN} = V_{IH} max or V_{IL} min; T_A = 0°C
		−1850		−1650	mV	V_{IN} = V_{IH} max or V_{IL} min; T_A = 25°C
		−1830		−1625	mV	V_{IN} = V_{IH} max or V_{IL} min; T_A = 75°C
Output threshold voltage, high	V_{OHC}	−1020			mV	V_{IN} = V_{IH} min or V_{IL} max; T_A = 0°C
		−980			mV	V_{IN} = V_{IH} min or V_{IL} max; T_A = 25°C
		−920			mV	V_{IN} = V_{IH} min or V_{IL} max; T_A = 75°C
Output threshold voltage, low	V_{OLC}			−1645	mV	V_{IN} = V_{IH} min or V_{IL} max; T_A = 0°C
				−1630	mV	V_{IN} = V_{IH} min or V_{IL} max; T_A = 25°C
				−1605	mV	V_{IN} = V_{IH} min or V_{IL} max; T_A = 75°C
Input voltage, high	V_{IH}	−1145		−840	mV	For all inputs: T_A = 0°C
		−1105		−810	mV	For all inputs: T_A = 25°C
		−1045		−720	mV	For all inputs: T_A = 75°C
Input voltage, low	V_{IL}	−1870		−1490	mV	For all inputs: T_A = 0°C
		−1850		−1475	mV	For all inputs: T_A = 25°C
		−1830		−1450	mV	For all inputs: T_A = 75°C
Input current, high	I_{IH}			220	μA	V_{IN} = V_{IH} max
Input current, low	I_{IL}	0.5		170	μA	For $\overline{CS}$: V_{IN} = V_{IL} min
		−50			μA	For all others: V_{IN} = V_{IL} min
Supply current	I_{EE}	−260			mA	For μPB10484-10: all inputs and outputs open
		−240			mA	For μPB10484-15: all inputs and outputs open

Notes:

(1) The device under test is mounted in a test socket and measured at a thermal equilibrium established with a transverse air flow maintained at greater than 2.0 m/s.

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AC Characteristics

T_A = 0 to +75°C; V_{EE} = −5.2 V ±5%; output load = 50 Ω to −2.0 V; V_{CC} = V_{CCA} = 0 V

		μPB10484-10			μPB10484-15				
Parameter	**Symbol**	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**	**Unit**	**Test Conditions**
Read Operation									
Address access time	t_{AA}			10			15	ns	
Chip select recovery time	t_{RCS}			5			8	ns	
Chip select access time	t_{ACS}			5			8	ns	
Write Operation									
Write pulse width	t_W	10			15			ns	
Data setup time	t_{WSD}	2			3			ns	
Data hold time	t_{WHD}	1			2			ns	
Address setup time	t_{WSA}	2			3			ns	
Address hold time	t_{WHA}	1			2			ns	
Chip select setup time	t_{WSCS}	2			3			ns	
Chip select hold time	t_{WHCS}	1			2			ns	
Write disable time	t_{WS}			5			8	ns	
Write recovery time	t_{WR}			11			17	ns	
Output Rise and Fall Times									
Output rise time	t_R		2			2		ns	
Output fall time	t_F		2			2		ns	

Notes:

(1) The device under test is mounted in a test socket and measured at a thermal equilibrium established with a transverse air flow maintained at greater than 2.0 m/s.

(2) Input pulse levels = −1.7 to −0.9 V; input rise and fall times (measured between 20% and 80% or 80% to 20%) = 2.5 ns; input and output timing reference level = 50%.

Figure 1. Loading Conditions Test Circuit

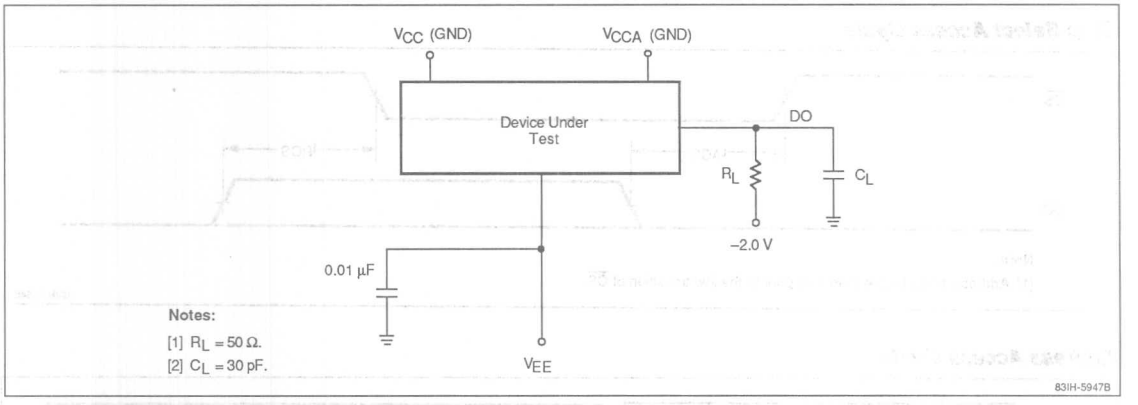
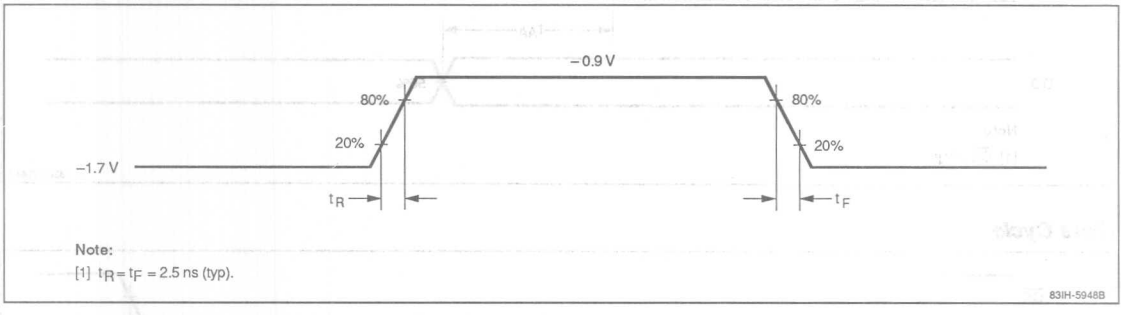


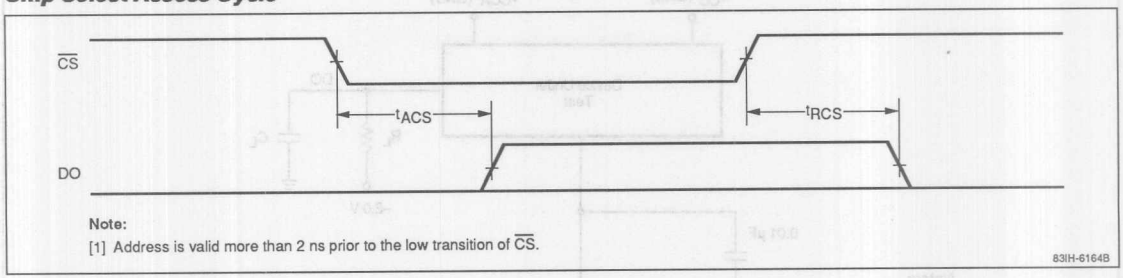
Figure 2. Input Pulse



8

Timing Waveforms

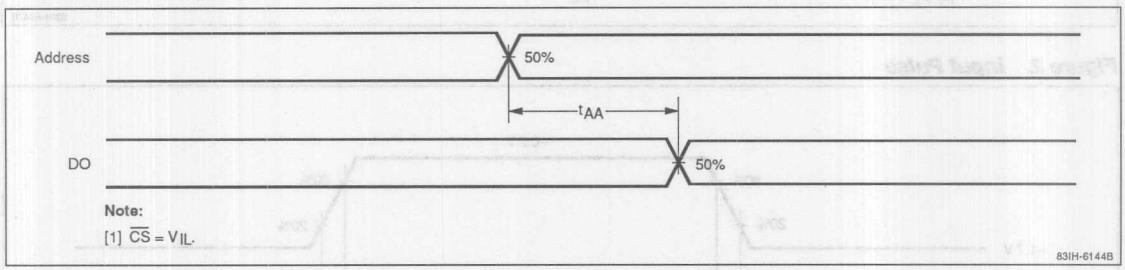
Chip Select Access Cycle



Note:
[1] Address is valid more than 2 ns prior to the low transition of $\overline{CS}$.

83IH-6164B

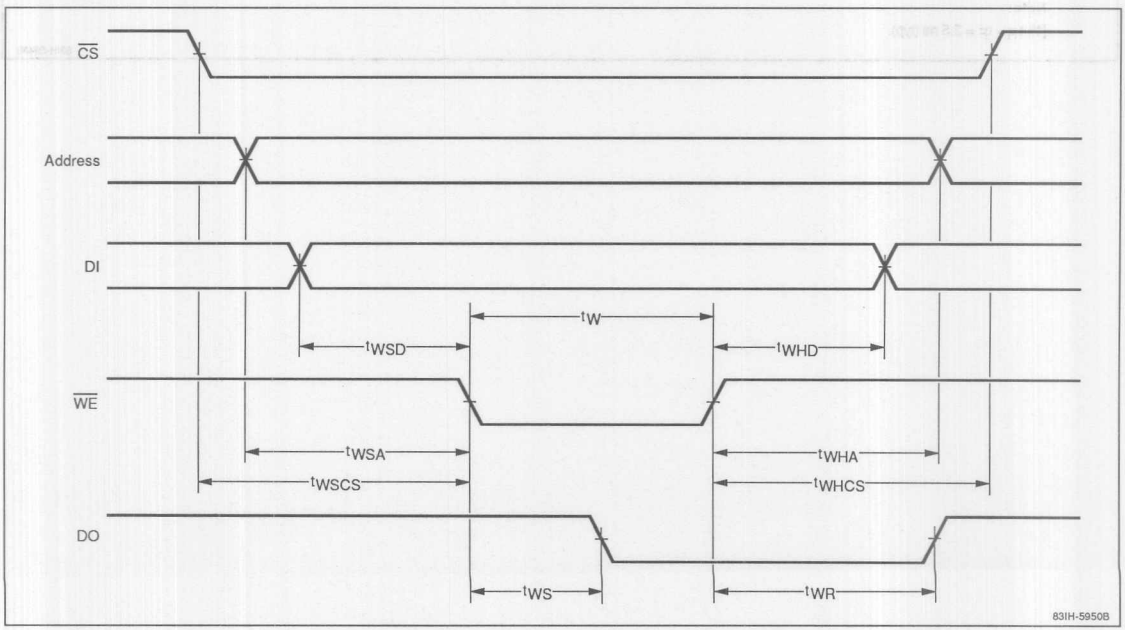
Address Access Cycle



Note:
[1] $\overline{CS} = V_{IL}$.

83IH-6144B

Write Cycle



83IH-5950B

PRELIMINARY INFORMATION

Description

The μPB10484A is a very high-speed 10K interface ECL RAM. It is organized as 4,096 words by 4 bits and designed with noninverted, open-emitter outputs and low power consumption. Two versions with access times of 5 or 7 ns maximum are available. The μPB10484A is packaged in a hermetic, 400-mil, 28-pin cerdip or 28-pin ceramic flatpack.

Features

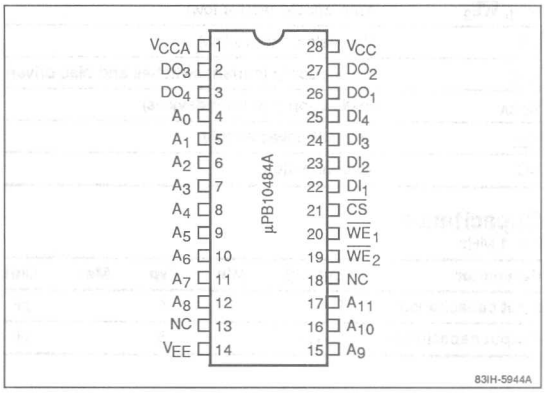
- 4,096-word x 4-bit organization
- 10K ECL interface
- Noninverted, open-emitter outputs
- Fast access times of 5 and 7 ns maximum
- Low power consumption of 1.4 W maximum
- 400-mil, 28-pin cerdip or ceramic flatpack packaging

Ordering Information

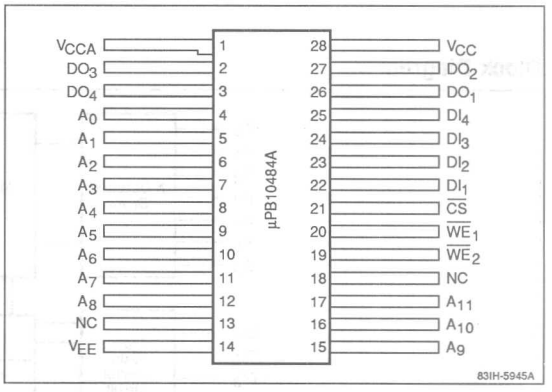
Part Number	Access Time (max)	Package
μPB10484AD-5	5 ns	28-pin cerdip
D-7	7 ns	
μPB10484AB-5	5 ns	28-pin ceramic flatpack
B-7	7 ns	

Pin Configurations

28-Pin Cerdip



28-Pin Ceramic Flatpack



8

Pin Identification

Symbol	Function
A_0 - A_{11}	Address inputs
DI_1 - DI_4	Data inputs
DO_1 - DO_4	Data outputs
$\overline{WE}_1$, $\overline{WE}_2$	Write enable (active low)
$\overline{CS}$	Chip select (active low)
V_{CC}	Power supply (current switches and bias driver)
V_{CCA}	Power supply (output devices)
V_{EE}	–5.2-volt power supply
NC	No connection

Capacitance

f = 1 MHz

Parameter	Symbol	Min	Typ	Max	Unit
Input capacitance	C_{IN}		4		pF
Output capacitance	C_{OUT}		6		pF

Absolute Maximum Ratings

$V_{CC} = V_{CCA} = 0$ V

Supply voltage, V_{EE}	–7.0 to +0.5 V
Input voltage, V_{IN}	V_{EE} to +0.5 V
Output current, I_{OUT}	–30 to +0.1 mA
Storage temperature, T_{STG}	–65 to +150 °C
Storage temperature under bias, T_{STG} (bias)	–55 to +125 °C

Exposure to Absolute Maximum Ratings for extended periods may affect device reliability; exceeding the ratings could cause permanent damage. The device should be operated within the limits specified under DC and AC Characteristics.

Truth Table

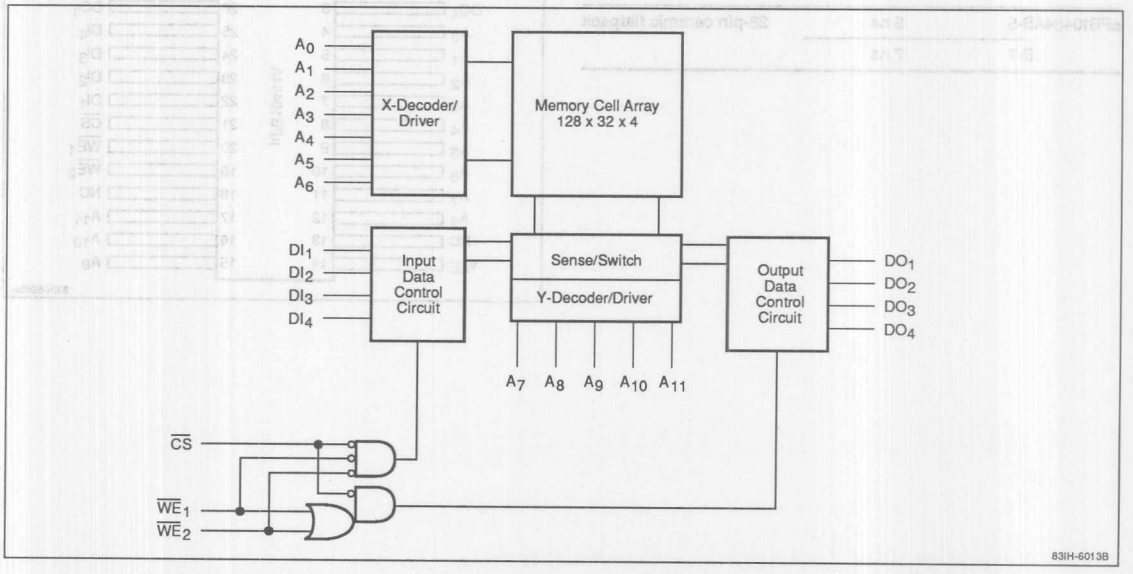
$\overline{CS}$	$\overline{WE}$	DI	Output	Function
H	X	X	L	Not selected
L	L (Note 2)	L	L	Write 0
L	L (Note 2)	H	L	Write 1
L	H (Note 2)	X	D_{OUT}	Read

Notes:

(1) X = don't care.

(2) Both $\overline{WE}_1$ and $\overline{WE}_2$ must be low to initiate write operation. For read operation, either $\overline{WE}_1$ or $\overline{WE}_2$ or both must be high.

Block Diagram



DC Characteristics

T_A = 0 to +75 °C; V_{EE} = −5.2 V; output load = 50 Ω to −2.0 V; V_{CC} = V_{CCA} = 0 V

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions
Output voltage, high	V_{OH}	−1000		−840	mV	V_{IN} = V_{IH} max or V_{IL} min; T_A = 0 °C
		−960		−810	mV	V_{IN} = V_{IH} max or V_{IL} min; T_A = 25 °C
		−900		−720	mV	V_{IN} = V_{IH} max or V_{IL} min; T_A = 75 °C
Output voltage, low	V_{OL}	−1870		−1665	mV	V_{IN} = V_{IH} max or V_{IL} min; T_A = 0 °C
		−1850		−1650	mV	V_{IN} = V_{IH} max or V_{IL} min; T_A = 25 °C
		−1830		−1625	mV	V_{IN} = V_{IH} max or V_{IL} min; T_A = 75 °C
Output threshold voltage, high	V_{OHC}	−1020			mV	V_{IN} = V_{IH} min or V_{IL} max; T_A = 0 °C
		−980			mV	V_{IN} = V_{IH} min or V_{IL} max; T_A = 25 °C
		−920			mV	V_{IN} = V_{IH} min or V_{IL} max; T_A = 75 °C
Output threshold voltage, low	V_{OLC}			−1645	mV	V_{IN} = V_{IH} min or V_{IL} max; T_A = 0 °C
				−1630	mV	V_{IN} = V_{IH} min or V_{IL} max; T_A = 25 °C
				−1605	mV	V_{IN} = V_{IH} min or V_{IL} max; T_A = 75 °C
Input voltage, high	V_{IH}	−1145		−840	mV	For all inputs: T_A = 0 °C
		−1105		−810	mV	For all inputs: T_A = 25 °C
		−1045		−720	mV	For all inputs: T_A = 75 °C
Input voltage, low	V_{IL}	−1870		−1490	mV	For all inputs: T_A = 0 °C
		−1850		−1475	mV	For all inputs: T_A = 25 °C
		−1830		−1450	mV	For all inputs: T_A = 75 °C
Input current, high	I_{IH}			220	μA	V_{IN} = V_{IH} max
Input current, low	I_{IL}	0.5		170	μA	For $\overline{CS}$: V_{IN} = V_{IL} min
		−50			μA	For all others: V_{IN} = V_{IL} min
Supply current	I_{EE}	−260			mA	For μPB10484A-5: all inputs and outputs open
		−240			mA	For μPB10484A-7: all inputs and outputs open

Notes:

(1) The device under test is mounted in a test socket and measured at a thermal equilibrium established with a transverse air flow maintained at greater than 2.0 m/s.

8

AC Characteristics

T_A = 0 to +75 °C; V_{EE} = −5.2 V ± 5%; output load = 50 Ω to −2.0 V; V_{CC} = V_{CCA} = 0 V

		μPB10484A-5			μPB10484A-7				
Parameter	**Symbol**	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**	**Unit**	**Test Conditions**
Read Operation									
Address access time	t_{AA}			5			7	ns	
Chip select recovery time	t_{RCS}			3.5			4	ns	
Chip select access time	t_{ACS}			3.5			4	ns	
Write Operation									
Write pulse width	t_W	6			8			ns	
Data setup time	t_{WSD}	1			1			ns	
Data hold time	t_{WHD}	2			2			ns	
Address setup time	t_{WSA}	1			1			ns	
Address hold time	t_{WHA}	2			2			ns	
Chip select setup time	t_{WSCS}	1			1			ns	
Chip select hold time	t_{WHCS}	2			2			ns	
Write disable time	t_{WS}			3.5			5	ns	
Write recovery time	t_{WR}			7			9	ns	
Output Rise and Fall Times									
Output rise time	t_R		2			2		ns	
Output fall time	t_F		2			2		ns	

Notes:

(1) The device under test is mounted in a test socket and measured at a thermal equilibrium established with a transverse air flow maintained at greater than 2.0 m/s.

(2) Input pulse levels = −1.7 to −0.9 V; input rise and fall times (measured between 20% and 80% or 80% and 20%) = 2.5 ns; input and output timing reference level = 50%.

Figure 1. Loading Conditions Test Circuit

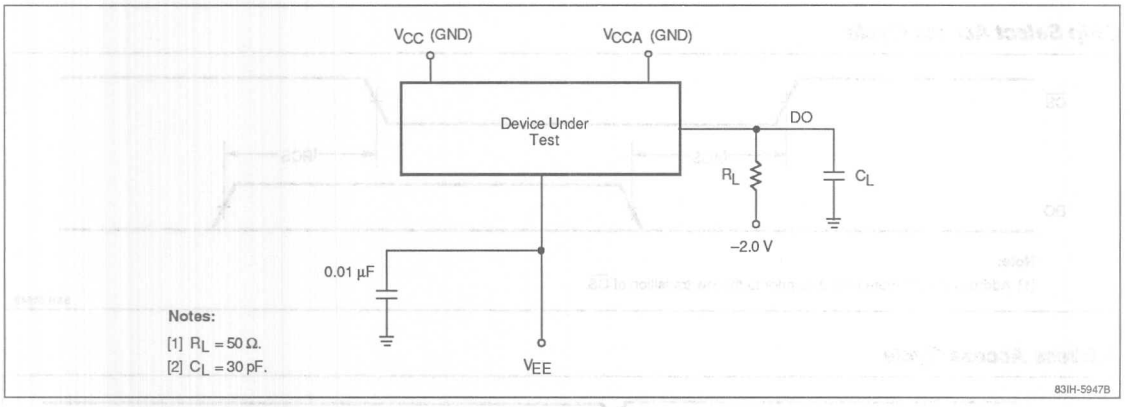
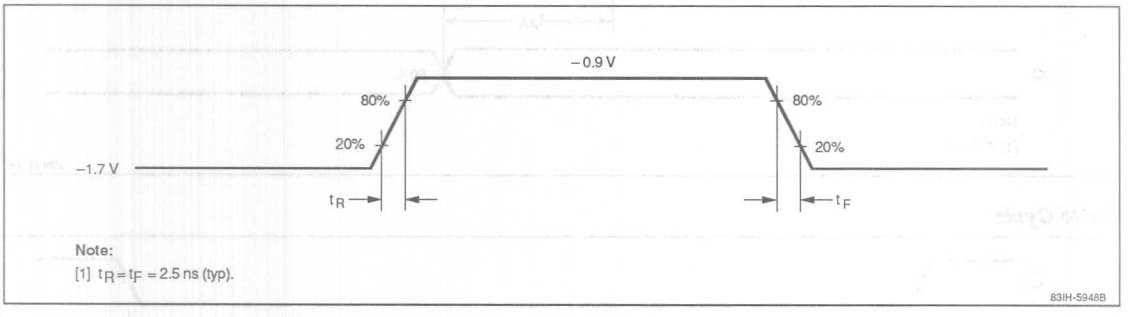


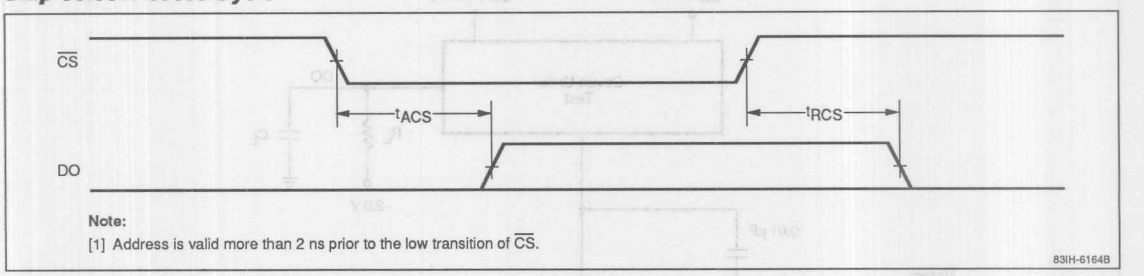
Figure 2. Input Pulse



8

Timing Waveforms

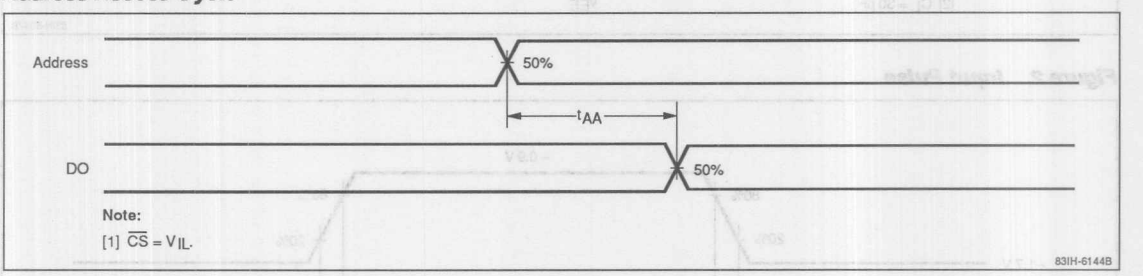
Chip Select Access Cycle



Note:
[1] Address is valid more than 2 ns prior to the low transition of $\overline{CS}$.

83IH-6164B

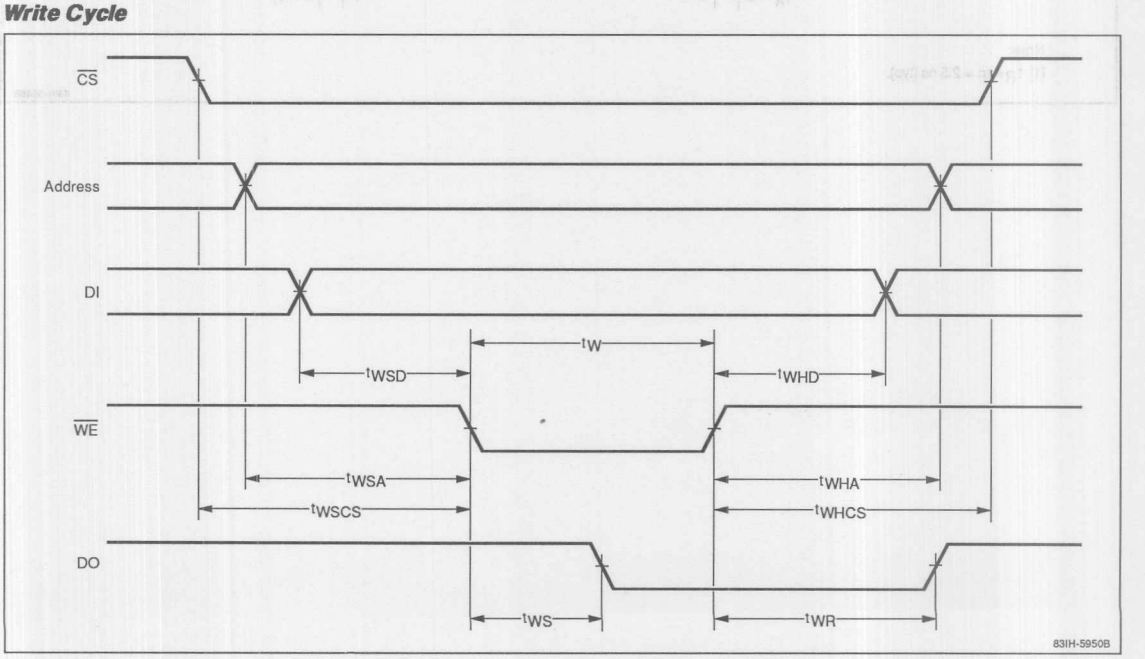
Address Access Cycle



Note:
[1] $\overline{CS} = V_{IL}$.

83IH-6144B

Write Cycle



83IH-5950B

μPB10A484
4,096 x 4-Bit
10K ECL RAM

PRELIMINARY INFORMATION

Description

The μPB10A484 is a very high-speed 10K interface ECL RAM organized as 4,096 words by 4 bits with noninverted, open-emitter outputs. Two versions with access times of 5 ns and 7 ns maximum are available. The μPB10A484 is packaged in a hermetic, 400-mil, 28-pin cerdip or 28-pin ceramic flatpack.

Features

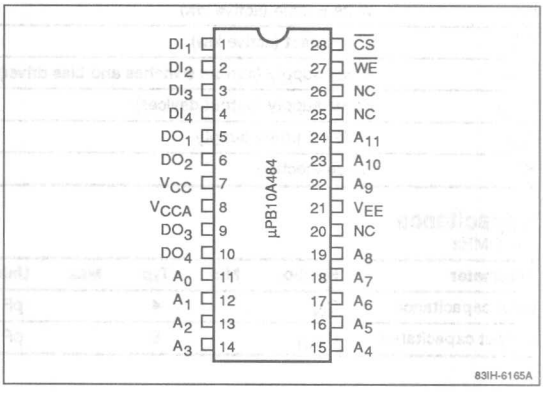
- 4,096-word x 4-bit organization
- 10K ECL interface
- Noninverted, open-emitter outputs
- Fast access times of 5 and 7 ns maximum
- 400-mil, 28-pin cerdip or ceramic flatpack packaging
- Center power pins

Ordering Information

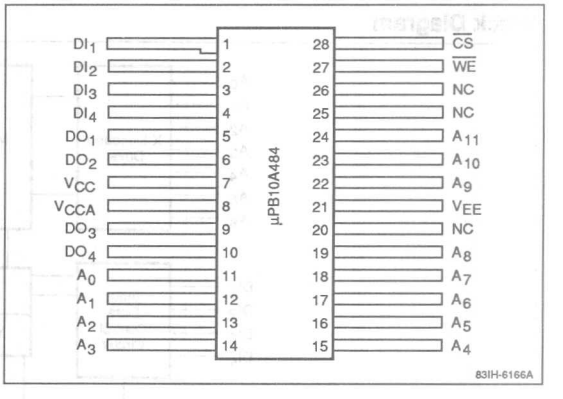
Part Number	Access Time (max)	Package
μPB10A484D-5	5 ns	28-pin cerdip
D-7	7 ns	
μPB10A484BH-5	5 ns	28-pin ceramic flatpack
BH-7	7 ns	

Pin Configurations

28-Pin Cerdip



28-Pin Ceramic Flatpack



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Pin Identification

Symbol	Function
A_0 - A_{11}	Address inputs
DI_1 - DI_4	Data inputs
DO_1 - DO_4	Data outputs
$\overline{WE}$	Write enable (active low)
$\overline{CS}$	Chip select (active low)
V_{CC}	Power supply (current switches and bias driver)
V_{CCA}	Power supply (output devices)
V_{EE}	–5.2-volt power supply
NC	No connection

Capacitance

f = 1 MHz

Parameter	Symbol	Min	Typ	Max	Unit
Input capacitance	C_{IN}		4		pF
Output capacitance	C_{OUT}		6		pF

Absolute Maximum Ratings

$V_{CC} = V_{CCA} = 0$ V

Supply voltage, V_{EE}	–7.0 to +0.5 V
Input voltage, V_{IN}	V_{EE} to +0.5 V
Output current, I_{OUT}	–30 to +0.1 mA
Storage temperature, T_{STG}	–65 to +150°C
Storage temperature under bias, T_{STG} (bias)	–55 to +125°C

Exposure to Absolute Maximum Ratings for extended periods may affect device reliability; exceeding the ratings could cause permanent damage. The device should be operated within the limits specified under DC and AC Characteristics.

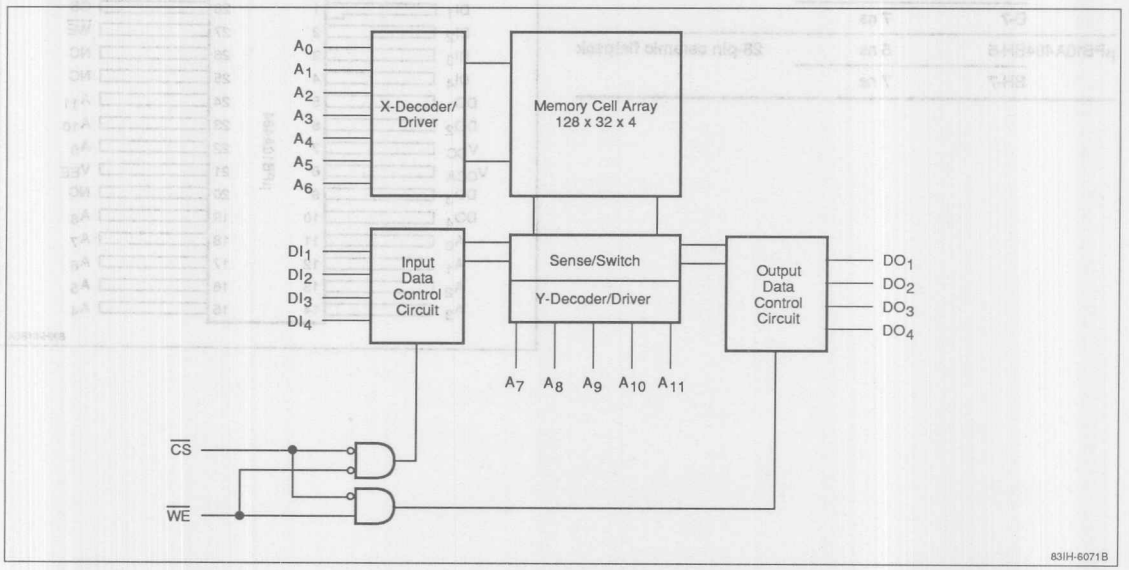
Truth Table

Function	$\overline{CS}$	$\overline{WE}$	D_{IN}	Output
Not selected	H	X	X	L
Write 0	L	L	L	L
Write 1	L	L	H	L
Read	L	H	X	D_{OUT}

Notes:

(1) X = don't care.

Block Diagram



DC Characteristics

T_A = 0 to +75°C; V_{EE} = −5.2 V; output load = 50 Ω to −2.0 V; V_{CC} = V_{CCA} = 0 V

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions
Output voltage, high	V_{OH}	−1000		−840	mV	V_{IN} = V_{IH} max or V_{IL} min; T_A = 0°C
		−960		−810	mV	V_{IN} = V_{IH} max or V_{IL} min; T_A = 25°C
		−900		−720	mV	V_{IN} = V_{IH} max or V_{IL} min; T_A = 75°C
Output voltage, low	V_{OL}	−1870		−1665	mV	V_{IN} = V_{IH} max or V_{IL} min; T_A = 0°C
		−1850		−1650	mV	V_{IN} = V_{IH} max or V_{IL} min; T_A = 25°C
		−1830		−1625	mV	V_{IN} = V_{IH} max or V_{IL} min; T_A = 75°C
Output threshold voltage, high	V_{OHC}	−1020			mV	V_{IN} = V_{IH} min or V_{IL} max; T_A = 0°C
		−980			mV	V_{IN} = V_{IH} min or V_{IL} max; T_A = 25°C
		−920			mV	V_{IN} = V_{IH} min or V_{IL} max; T_A = 75°C
Output threshold voltage, low	V_{OLC}			−1645	mV	V_{IN} = V_{IH} min or V_{IL} max; T_A = 0°C
				−1630	mV	V_{IN} = V_{IH} min or V_{IL} max; T_A = 25°C
				−1605	mV	V_{IN} = V_{IH} min or V_{IL} max; T_A = 75°C
Input voltage, high	V_{IH}	−1145		−840	mV	For all inputs: T_A = 0°C
		−1105		−810	mV	For all inputs: T_A = 25°C
		−1045		−720	mV	For all inputs: T_A = 75°C
Input voltage, low	V_{IL}	−1870		−1490	mV	For all inputs: T_A = 0°C
		−1850		−1475	mV	For all inputs: T_A = 25°C
		−1830		−1450	mV	For all inputs: T_A = 75°C
Input current, high	I_{IH}			220	μA	V_{IN} = V_{IH} max
Input current, low	I_{IL}	0.5		170	μA	For $\overline{CS}$: V_{IN} = V_{IL} min
		−50			μA	For all others: V_{IN} = V_{IL} min
Supply current	I_{EE}	320			mA	All inputs and outputs open

Notes:

(1) The device under test is mounted in a test socket and measured at a thermal equilibrium established with a transverse air flow maintained at greater than 2.0 m/s.

8

AC Characteristics

T_A = 0 to +75°C; V_{EE} = −5.2 V ± 5%; output load = 50 Ω to −2.0 V; V_{CC} = V_{CCA} = 0 V

		μPB10A484-5			μPB10A484-7				
Parameter	**Symbol**	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**	**Unit**	**Test Conditions**
Read Operation									
Address access time	t_{AA}			5			7	ns	
Chip select recovery time	t_{RCS}			3.5			4	ns	
Chip select access time	t_{ACS}			3.5			4	ns	
Write Operation									
Write pulse width	t_W	6			8			ns	
Data setup time	t_{WSD}	1			1			ns	
Data hold time	t_{WHD}	2			2			ns	
Address setup time	t_{WSA}	1			1			ns	
Address hold time	t_{WHA}	2			2			ns	
Chip select setup time	t_{WSCS}	1			1			ns	
Chip select hold time	t_{WHCS}	2			2			ns	
Write disable time	t_{WS}			3.5			5	ns	
Write recovery time	t_{WR}			7			9	ns	
Output Rise and Fall Times									
Output rise time	t_R		2			2		ns	
Output fall time	t_F		2			2		ns	

Notes:

(1) The device under test is mounted in a test socket and measured at a thermal equilibrium established with a transverse air flow maintained at greater than 2.0 m/s.

(2) Input pulse levels = −1.7 to −0.9 V; input rise and fall times (measured between 20% and 80% or 80% and 20%) = 2.5 ns; input and output timing reference level = 50%.

Figure 1. Loading Conditions Test Circuit

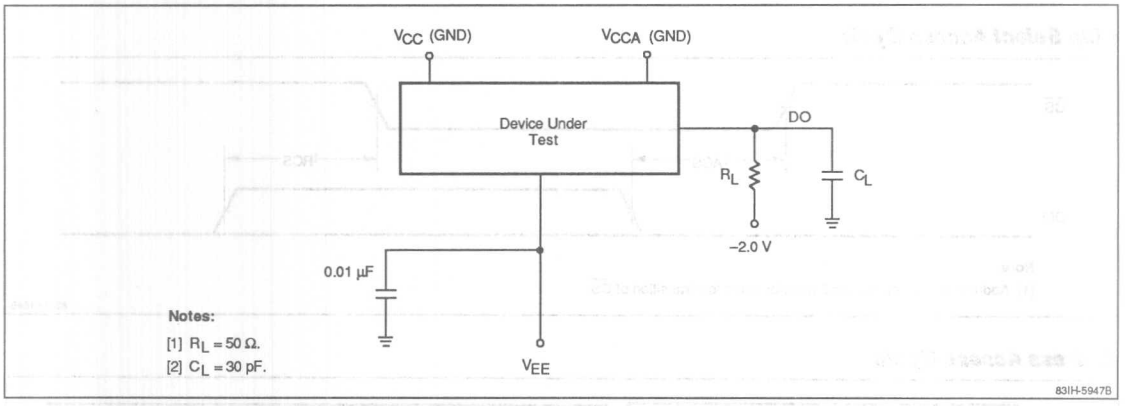
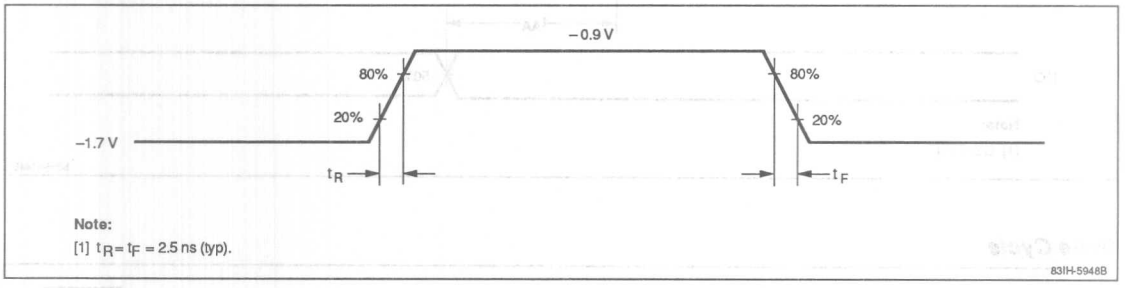


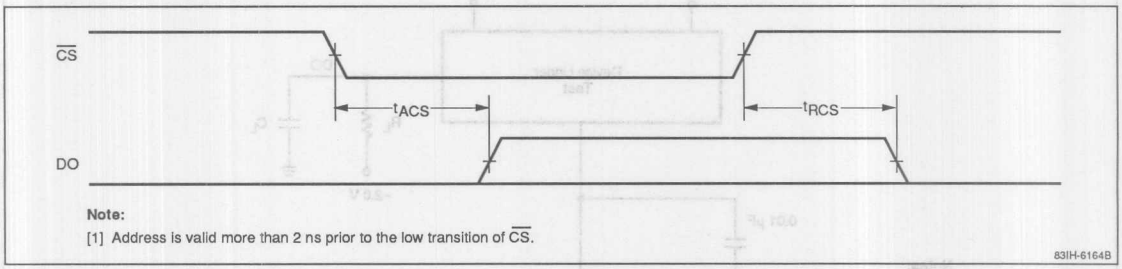
Figure 2. Input Pulse



8

Timing Waveforms

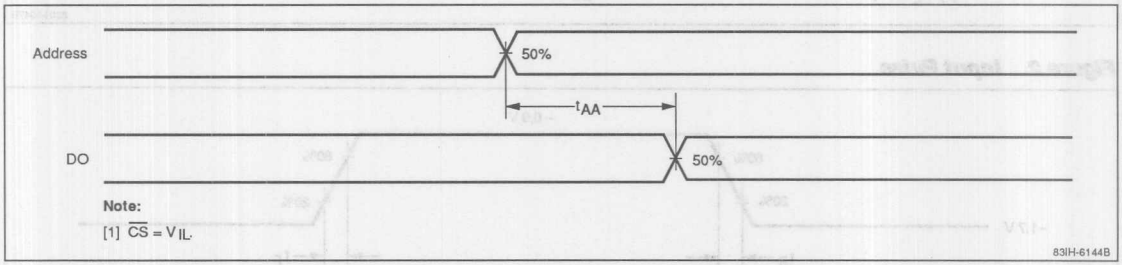
Chip Select Access Cycle



Note:
[1] Address is valid more than 2 ns prior to the low transition of $\overline{CS}$.

83IH-6164B

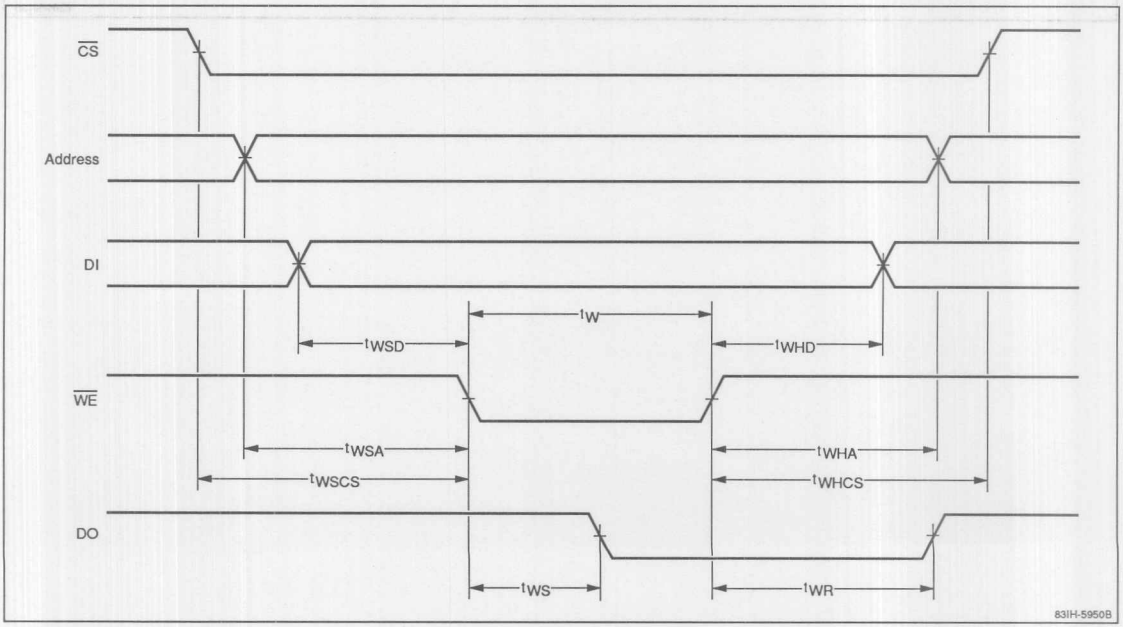
Address Access Cycle



Note:
[1] $\overline{CS} = V_{IL}$.

83IH-6144B

Write Cycle



83IH-5950B

PRELIMINARY INFORMATION

Description

The μPD10500 is a very high-speed BiCMOS RAM with a 10K ECL interface. Its unique design uses blended CMOS and bipolar peripheral circuits and N-channel MOS memory cells. The device is organized as 262,144 words by 1 bit and is designed with an open-emitter output (noninverted) and low power consumption. Two versions with fast access times of 15 and 20 ns maximum are available in hermetic, 300-mil, 24-pin cerdip packaging.

Features

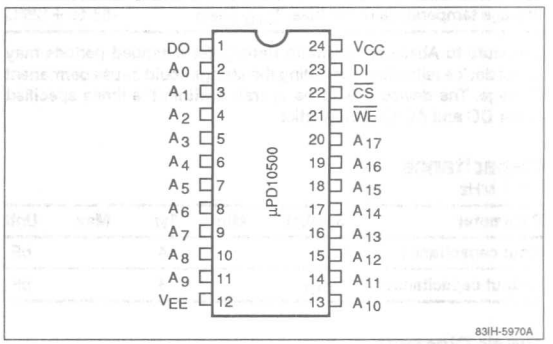
- BiCMOS technology
- 262,144-word x 1-bit organization
- 10K ECL interface
- Open-emitter output (noninverted)
- Fast access times
- Low power consumption
- 300-mil, 24-pin cerdip packaging

Ordering Information

Part Number	Access Time (max)	Power Consumption (max)	Package
μPD10500D-15	15 ns	832 mW	24-pin cerdip
D-20	20ns		

Pin Configuration

24-Pin Cerdip



Pin Identification

Symbol	Function
A_0 - A_{17}	Address inputs
DI	Data input
DO	Data output
$\overline{CS}$	Chip select
$\overline{WE}$	Write enable
V_{CC}, V_{CCA}	Ground
V_{EE}	–5.2-volt power supply

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Absolute Maximum Ratings

Supply voltage, V_{EE}	−7.0 to +0.5 V
Input voltage, V_{IN}	V_{EE} to +0.5 V
Output current, I_{OUT}	−30 to +0.1 mA
Storage temperature, T_{STG}	−65 to +150°C
Storage temperature under bias, T_{STG} (bias)	−55 to +125°C

Exposure to Absolute Maximum Ratings for extended periods may affect device reliability; exceeding the ratings could cause permanent damage. The device should be operated within the limits specified under DC and AC Characteristics.

Capacitance

f = 1 MHz

Parameter	Symbol	Min	Typ	Max	Unit
Input capacitance	C_{IN}		4		pF
Output capacitance	C_{OUT}		6		pF

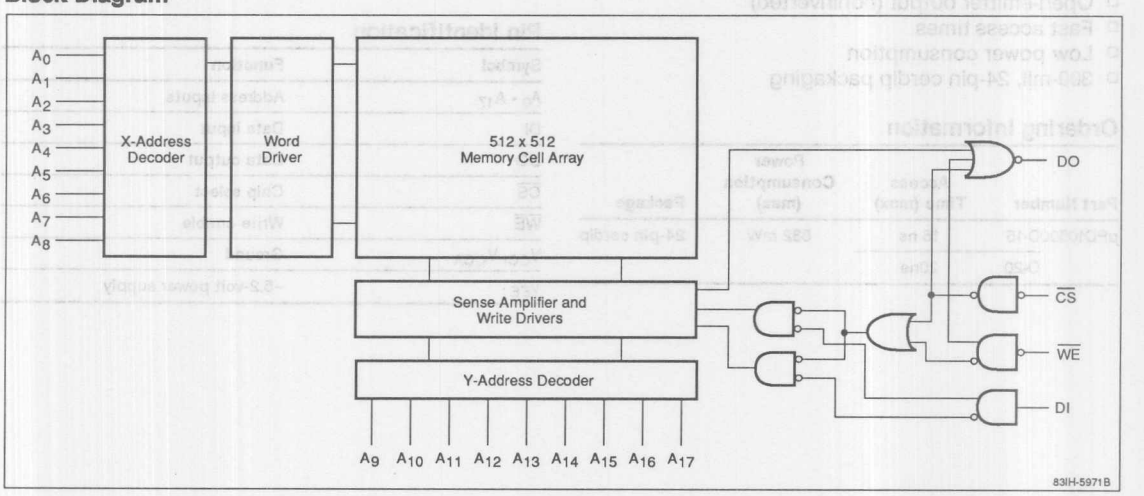
Truth Table

$\overline{CS}$	$\overline{WE}$	DI	Function	Output
H	X	X	Not selected	L
L	L	L	Write 0	L
L	L	H	Write 1	L
L	H	X	Read	D_{OUT}

Notes:

(1) X = don't care.

Block Diagram



DC Characteristics

T_A = 0 to +75°C; V_{EE} = −5.2 V ±5%; output load = 50 Ω to −2.0 V; V_{CC} = V_{CCA} = 0 V

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions
Output voltage, high	V_{OH}	−1000		−840	mV	V_{IN} = V_{IH} max or V_{IL} min; T_A = 0°C
		−960		−810	mV	V_{IN} = V_{IH} max or V_{IL} min; T_A = 25°C
		−900		−720	mV	V_{IN} = V_{IH} max or V_{IL} min; T_A = 75°C
Output voltage, low	V_{OL}	−1870		−1665	mV	V_{IN} = V_{IH} max or V_{IL} min; T_A = 0°C
		−1850		−1650	mV	V_{IN} = V_{IH} max or V_{IL} min; T_A = 25°C
		−1830		−1625	mV	V_{IN} = V_{IH} max or V_{IL} min; T_A = 75°C
Output threshold voltage, high	V_{OHC}	−1020			mV	V_{IN} = V_{IH} min or V_{IL} max; T_A = 0°C
		−980			mV	V_{IN} = V_{IH} min or V_{IL} max; T_A = 25°C
		−920			mV	V_{IN} = V_{IH} min or V_{IL} max; T_A = 75°C
Output threshold voltage, low	V_{OLC}			−1645	mV	V_{IN} = V_{IH} min or V_{IL} max; T_A = 0°C
				−1630	mV	V_{IN} = V_{IH} min or V_{IL} max; T_A = 25°C
				−1605	mV	V_{IN} = V_{IH} min or V_{IL} max; T_A = 75°C
Input voltage, high	V_{IH}	−1145		−840	mV	For all inputs: T_A = 0°C
		−1105		−810	mV	For all inputs: T_A = 25°C
		−1045		−720	mV	For all inputs: T_A = 75°C
Input voltage, low	V_{IL}	−1870		−1490	mV	For all inputs: T_A = 0°C
		−1850		−1475	mV	For all inputs: T_A = 25°C
		−1830		−1450	mV	For all inputs: T_A = 75°C
Input current, high	I_{IH}			220	μA	V_{IN} = V_{IH} max
Input current, low	I_{IL}	0.5		170	μA	For $\overline{CS}$: V_{IN} = V_{IL} min
		−50			μA	For all others: V_{IN} = V_{IL} min
Supply current	I_{EE}	−160			mA	All inputs and outputs open

Notes:

(1) The device under test is mounted in a test socket and measured at a thermal equilibrium established with a transverse air flow maintained at greater than 2.0 m/s.

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AC Characteristics

T_A = 0 to +75 °C; V_{EE} = −5.2 V ± 5%

Parameter	Symbol	μPD10500-15			μPD10500-20			Unit	Test Conditions
		Min	Typ	Max	Min	Typ	Max		
Read Operation									
Address access time	t_{AA}			15			20	ns	
Chip select access time	t_{ACS}			10			15	ns	
Chip select recovery time	t_{RCS}			10			15	ns	
Write Operation									
Write pulse width	t_W	10			15			ns	
Data setup time	t_{WSD}	2			2			ns	
Data hold time	t_{WHD}	3			3			ns	
Address setup time	t_{WSA}	2			2			ns	
Address hold time	t_{WHA}	3			3			ns	
Chip select setup time	t_{WSCS}	2			2			ns	
Chip select hold time	t_{WHCS}	3			3			ns	
Write disable time	t_{WS}			10			15	ns	
Write recovery time	t_{WR}			18			23	ns	
Output Rise and Fall Times									
Rise time	t_R		2			2		ns	
Fall time	t_F		2			2		ns	

Notes:

(1) The device under test (DUT) is mounted in a test socket and is measured at a thermal equilibrium established with a transverse air flow maintained at greater than 2.0 m/s.

(2) Input pulse levels = −1.7 to −0.9 V; input rise and fall times (measured between 20% and 80% or 80% and 20%) = 2.5 ns; input and output timing reference levels = 50%.

Figure 1. Loading Conditions Test Circuit

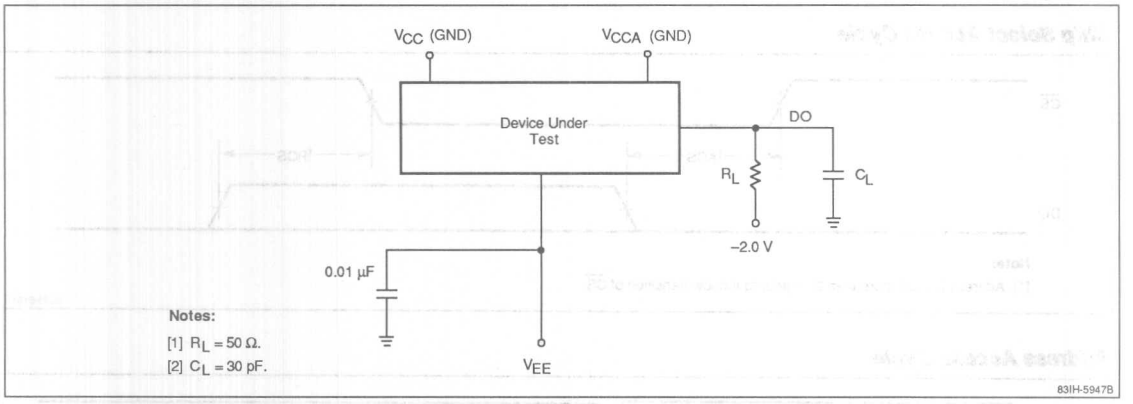
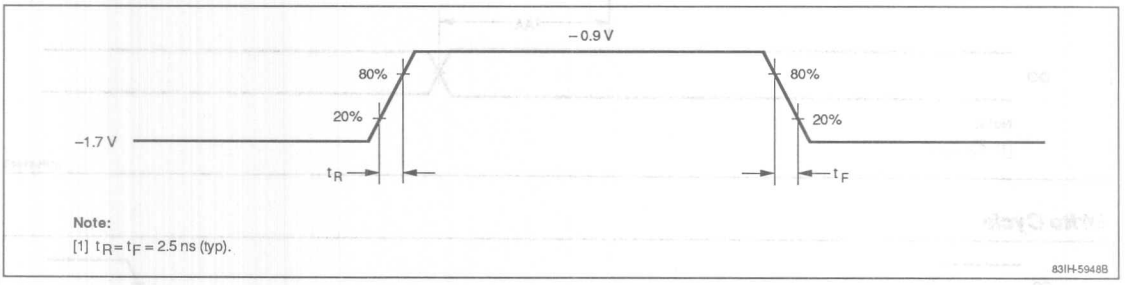


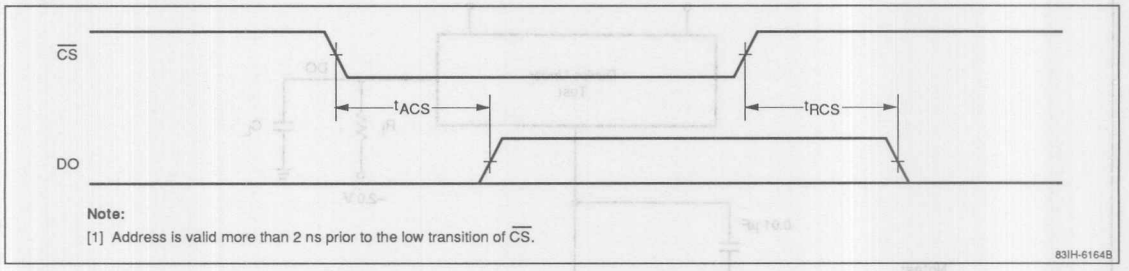
Figure 2. Input Pulse



8

Timing Waveforms

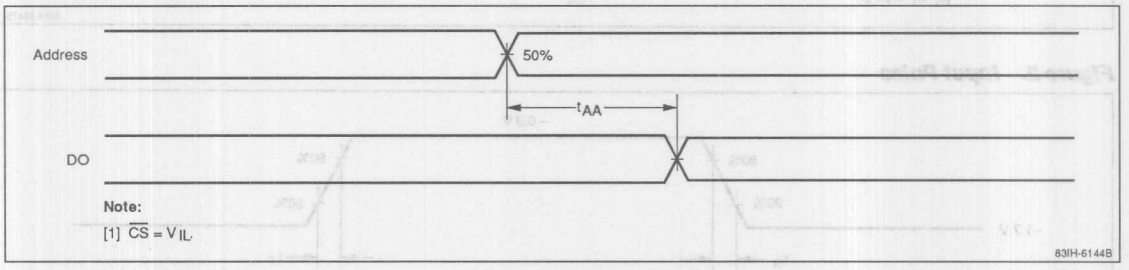
Chip Select Access Cycle



Note:
[1] Address is valid more than 2 ns prior to the low transition of $\overline{CS}$.

83IH-6164B

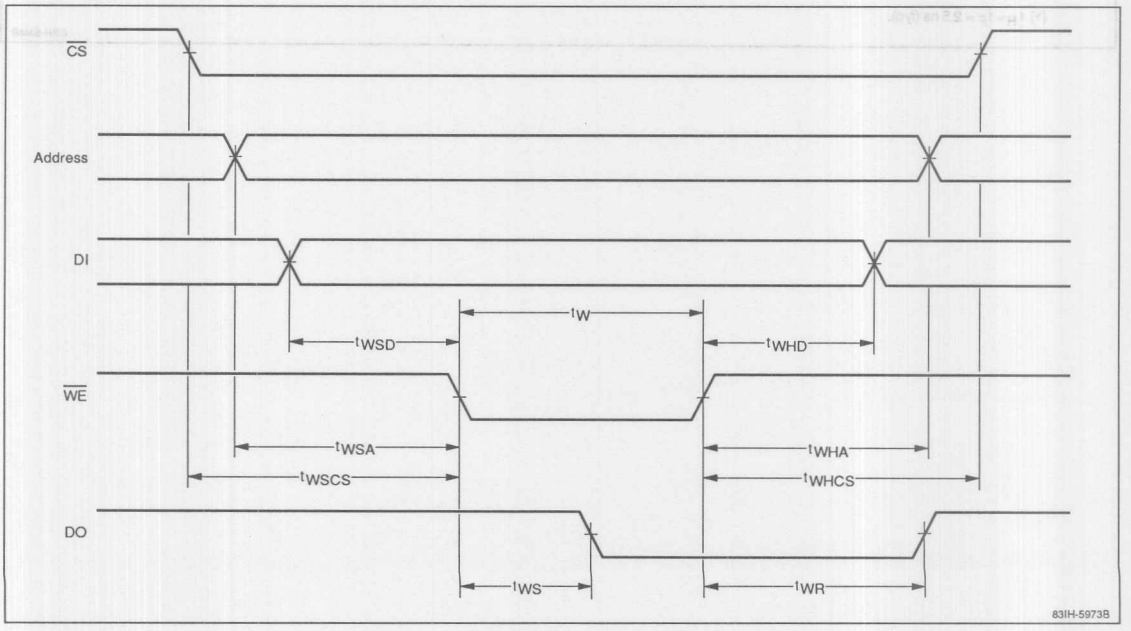
Address Access Cycle



Note:
[1] $\overline{CS} = V_{IL}$.

83IH-6144B

Write Cycle



83IH-5973B

μPD10504
65,536 x 4-Bit
10K BiCMOS ECL RAM

PRELIMINARY INFORMATION

Description

The μPD10504 is a very high-speed BiCMOS RAM with a 10K ECL interface. Its unique design uses blended CMOS and bipolar peripheral circuits and N-channel MOS memory cells. The device is organized as 65,536 words by 4 bit and designed with an open emitter output (noninverted) and low power consumption. The μPD10504 is available in hermetic, 400-mil, 32-pin cerdip packaging.

Features

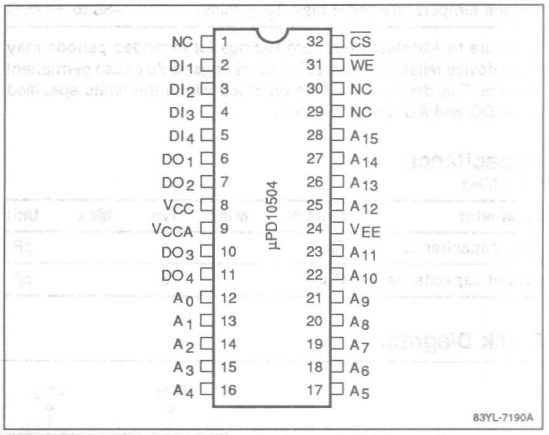
- BiCMOS technology
- 65,536-word x 4-bit organization
- 10K ECL interface
- Open emitter output (noninverted)
- Fast access times
- Low power consumption
- 400-mil, 32-pin cerdip packaging

Ordering Information

Part Number	Access Time (max)	Power Consumption (max)	Package
μPD10504D-15	15 ns	936 mW	32-pin cerdip

Pin Configuration

32-Pin Cerdip



Pin Identification

Symbol	Function
A_0 - A_{15}	Address inputs
DI_1 - DI_4	Data inputs
DO_1 - DO_4	Data outputs
$\overline{CS}$	Chip select
$\overline{WE}$	Write enable
V_{CC}, V_{CCA}	Ground
V_{EE}	–5.2-volt power supply
NC	No connection

8

Absolute Maximum Ratings

Supply voltage, V_{EE}	−7.0 to +0.5 V
Input voltage, V_{IN}	V_{EE} to +0.5 V
Output current, I_{OUT}	−30 to +0.1 mA
Storage temperature, T_{STG}	−65 to +150°C
Storage temperature under bias, T_{STG} (bias)	−55 to +125°C

Exposure to Absolute Maximum Ratings for extended periods may affect device reliability; exceeding the ratings could cause permanent damage. The device should be operated within the limits specified under DC and AC Characteristics.

Capacitance

f = 1 MHz

Parameter	Symbol	Min	Typ	Max	Unit
Input capacitance	C_{IN}		4		pF
Output capacitance	C_{OUT}		6		pF

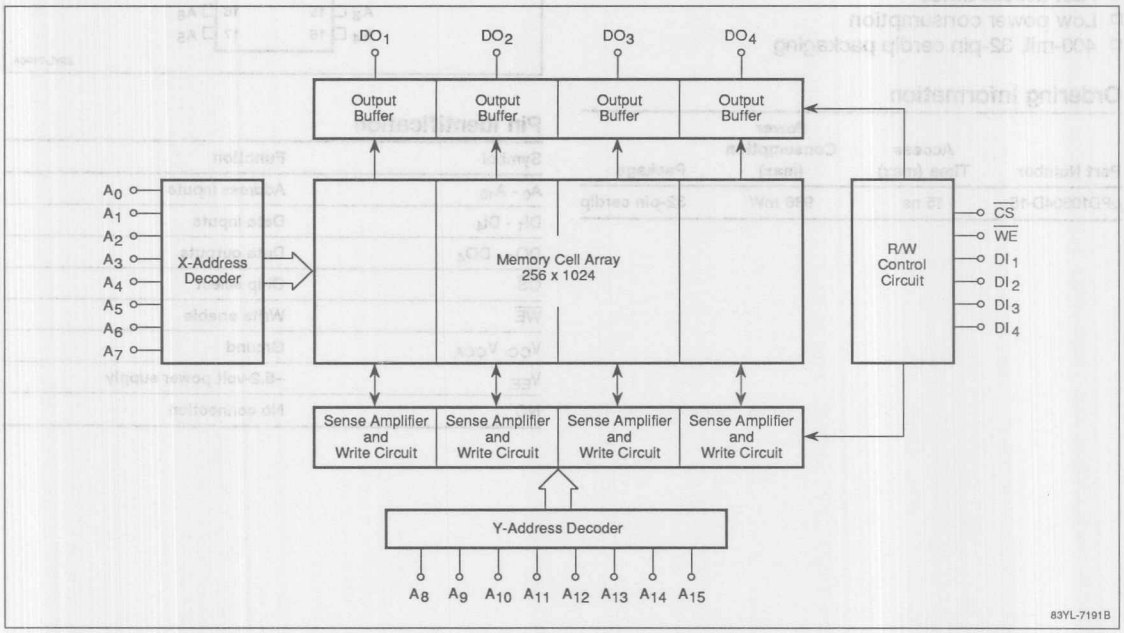
Truth Table

$\overline{CS}$	$\overline{WE}$	DI	Function	Output
H	X	X	Not selected	L
L	L	L	Write 0	L
L	L	H	Write 1	L
L	H	X	Read	D_{OUT}

Notes:

(1) X = don't care.

Block Diagram



DC Characteristics

T_A = 0 to +75°C; V_{EE} = −5.2 V ±5%; output load = 50 Ω to −2.0 V; V_{CC} = V_{CCA} = 0 V

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions
Output voltage, high	V_{OH}	−1000		−840	mV	V_{IN} = V_{IH} max or V_{IL} min; T_A = 0°C
		−950		−810	mV	V_{IN} = V_{IH} max or V_{IL} min; T_A = 25°C
		−900		−720	mV	V_{IN} = V_{IH} max or V_{IL} min; T_A = 75°C
Output voltage, low	V_{OL}	−1870		−1665	mV	V_{IN} = V_{IH} max or V_{IL} min; T_A = 0°C
		−1850		−1650	mV	V_{IN} = V_{IH} max or V_{IL} min; T_A = 25°C
		−1830		−1625	mV	V_{IN} = V_{IH} max or V_{IL} min; T_A = 75°C
Output threshold voltage, high	V_{OHC}	−1020			mV	V_{IN} = V_{IH} min or V_{IL} max; T_A = 0°C
		−980			mV	V_{IN} = V_{IH} min or V_{IL} max; T_A = 25°C
		−920			mV	V_{IN} = V_{IH} min or V_{IL} max; T_A = 75°C
Output threshold voltage, low	V_{OLC}			−1645	mV	V_{IN} = V_{IH} min or V_{IL} max; T_A = 0°C
				−1630	mV	V_{IN} = V_{IH} min or V_{IL} max; T_A = 25°C
				−1605	mV	V_{IN} = V_{IH} min or V_{IL} max; T_A = 75°C
Input voltage, high	V_{IH}	−1145		−840	mV	For all inputs: T_A = 0°C
		−1105		−810	mV	For all inputs: T_A = 25°C
		−1045		−720	mV	For all inputs: T_A = 75°C
Input voltage, low	V_{IL}	−1870		−1490	mV	For all inputs: T_A = 0°C
		−1850		−1475	mV	For all inputs: T_A = 25°C
		−1830		−1450	mV	For all inputs: T_A = 75°C
Input current, high	I_{IH}			220	μA	V_{IN} = V_{IH} max
Input current, low	I_{IL}	0.5		170	μA	For $\overline{CS}$: V_{IN} = V_{IL} min
		−50			μA	For all others: V_{IN} = V_{IL} min
Supply current	I_{EE}	−180			mA	All inputs and outputs open

Notes:

(1) The device under test is mounted in a test socket and measured at a thermal equilibrium established with a transverse air flow maintained at greater than 2.0 m/s.

8

AC Characteristics

T_A = 0 to +75°C; V_{EE} = −5.2 V ± 5%

Parameter	Symbol	μPD10504-15 Min	Typ	Max	Unit	Test Conditions
Read Operation						
Address access time	t_{AA}			15	ns	
Chip select access time	t_{ACS}			10	ns	
Chip select recovery time	t_{RCS}			10	ns	
Write Operation						
Write pulse width	t_W	10			ns	
Data setup time	t_{WSD}	2			ns	
Data hold time	t_{WHD}	3			ns	
Address setup time	t_{WSA}	2			ns	
Address hold time	t_{WHA}	3			ns	
Chip select setup time	t_{WSCS}	2			ns	
Chip select hold time	t_{WHCS}	3			ns	
Write disable time	t_{WS}			10	ns	
Write recovery time	t_{WR}			18	ns	
Output Rise and Fall Times						
Rise time	t_R		2		ns	
Fall time	t_F		2		ns	

Notes:

(1) The device under test is mounted in a test socket and is measured at a thermal equilibrium established with a transverse air flow maintained at greater than 2.0 m/s.

(2) Input pulse levels = −1.7 to −0.9 V; input rise and fall times (measured between 20% and 80% or 80% and 20%) = 2.0 ns; input and output timing reference levels = 50%.

Figure 1. Loading Conditions Test Circuit

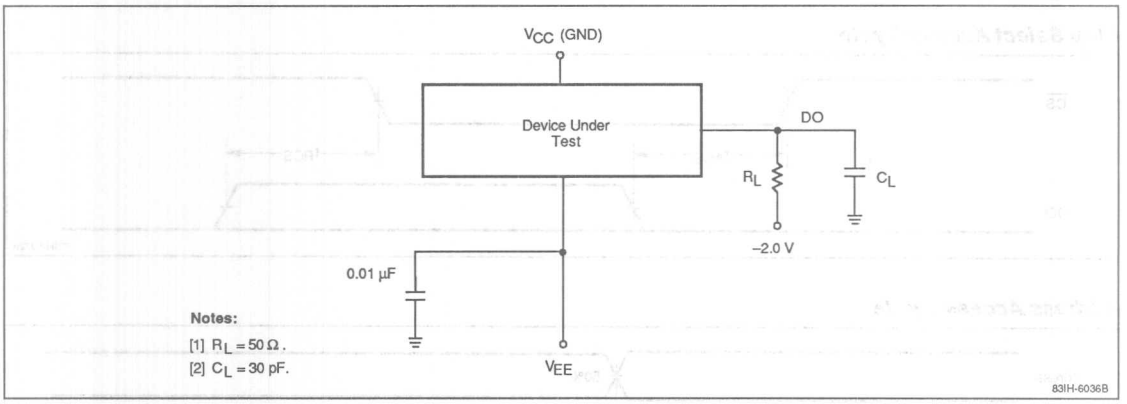
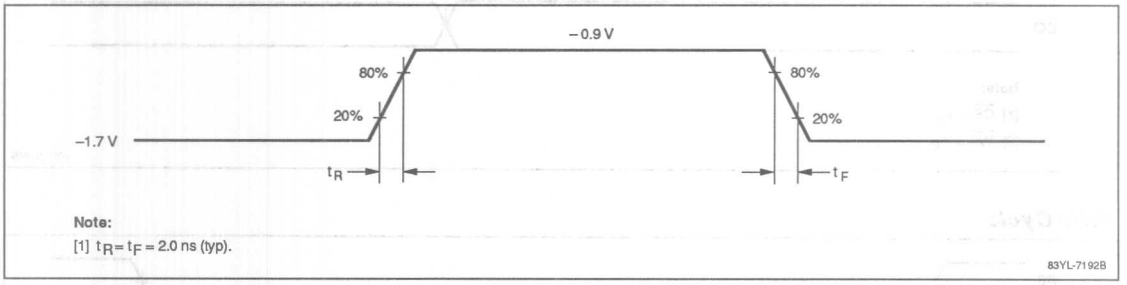


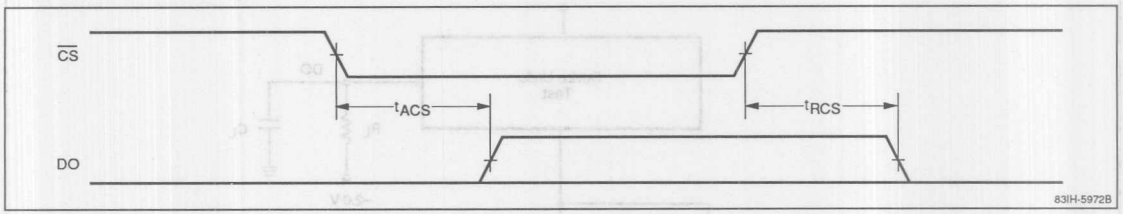
Figure 2. Input Pulse



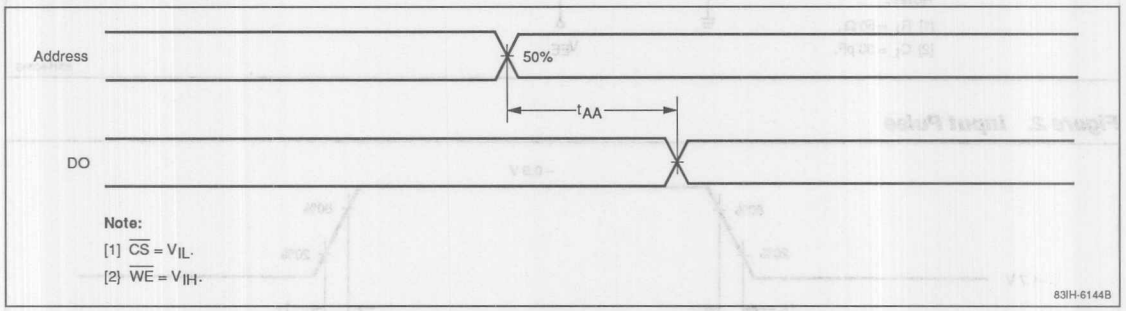
8

Timing Waveforms

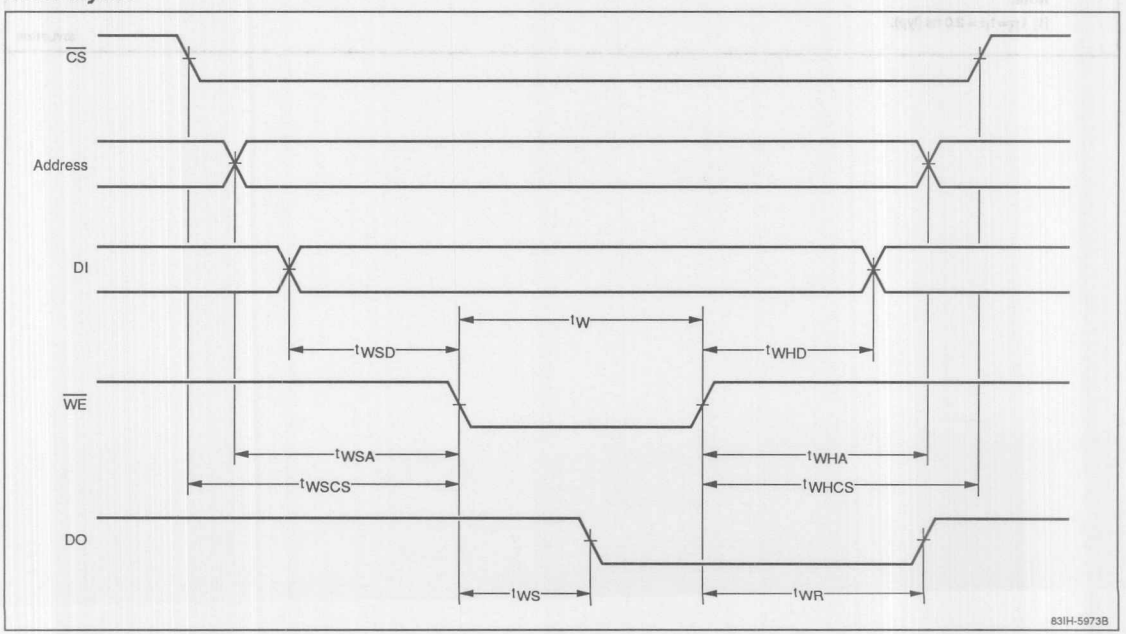
Chip Select Access Cycle



Address Access Cycle



Write Cycle



Description

The μPB100422 is a very high-speed 100K interface ECL RAM organized as 256 words by 4 bits and designed with noninverted, open-emitter outputs and low power consumption. Two versions with fast access times of 7 or 10 ns maximum are available in 24-pin ceramic DIP or ceramic flatpack packaging.

Features

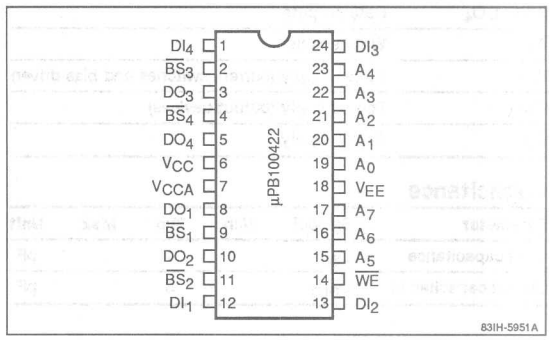
- 256-word x 4-bit organization
- 100K ECL interface
- Noninverted, open-emitter outputs
- Fast access times
- Low power consumption
- 400-mil, 24-pin ceramic DIP or 24-pin ceramic flatpack packaging

Ordering Information

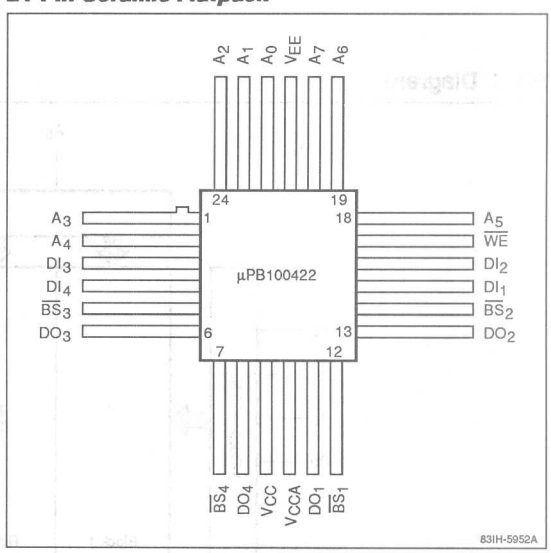
Part Number	Access Time (max)	Supply Current (min)	Package
μPB100422D-7	7 ns	–220 mA	24-pin ceramic DIP
D-10	10 ns		
μPB100422B-7	7 ns	–220 mA	24-pin ceramic flatpack
B-10	10 ns		

Pin Configurations

24-Pin Ceramic DIP



24-Pin Ceramic Flatpack



8

Pin Identification

Symbol	Function
A_0 - A_7	Addresses
$\overline{BS}_1$ - $\overline{BS}_4$	Block select inputs
DI_1 - DI_4	Data inputs
DO_1 - DO_4	Data outputs
$\overline{WE}$	Write enable
V_{CC}	Power supply (current switches and bias driver)
V_{CCA}	Power supply (output devices)
V_{EE}	Power supply

Capacitance

Parameter	Symbol	Min	Typ	Max	Unit
Input capacitance	C_{IN}		4		pF
Output capacitance	C_{OUT}		5		pF

Absolute Maximum Ratings

Supply voltage, V_{EE} to V_{CC}	−7.0 to +0.5 V
Input voltage, V_{IN}	V_{EE} to +0.5 V
Output current, I_{OUT}	−30 to +0.1 mA
Storage temperature, T_{STG}	−65 to +150°C
Storage temperature, under bias, $T_{STG\ (bias)}$	−55 to +125°C

Exposure to Absolute Maximum Ratings for extended periods may affect device reliability; exceeding the ratings could cause permanent damage. The device should be operated within the limits specified under DC and AC Characteristics.

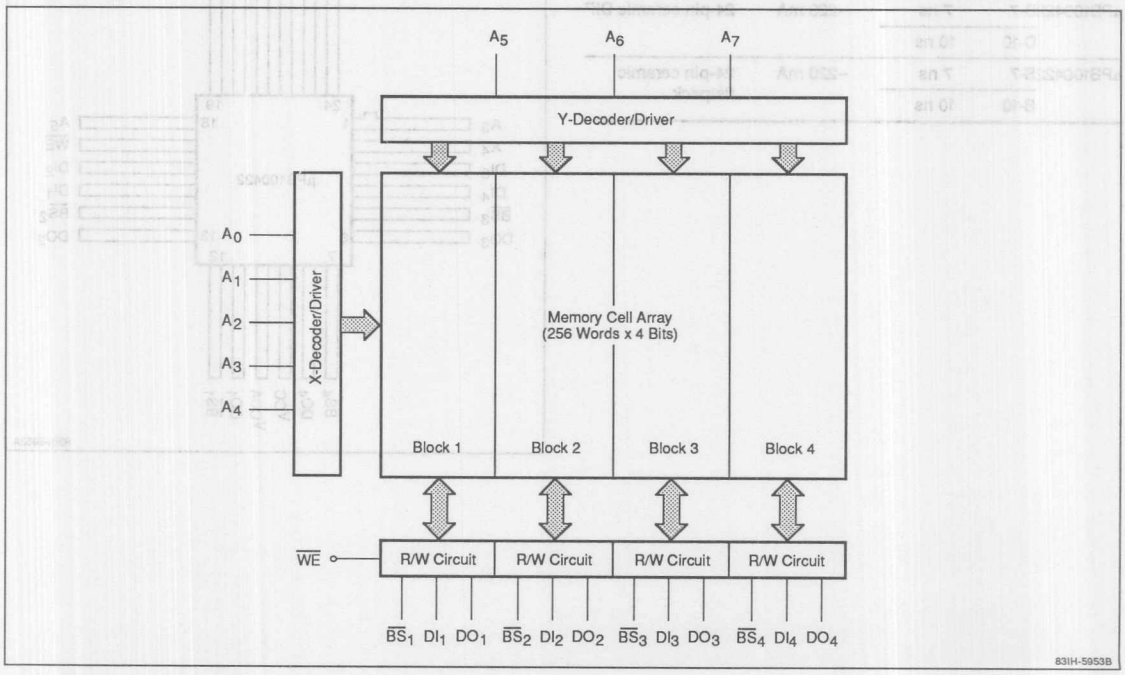
Truth Table

$\overline{BS}$	$\overline{WE}$	DI	DO	Function
H	X	X	L	Not Selected
L	L	L	L	Write "0"
L	L	H	L	Write "1"
L	H	X	Data Valid	Read

Notes:

(1) The Block Select input for each of the four memory blocks is used independently as shown in the block diagram.

Block Diagram



DC Characteristics

T_A = 0 to +85 °C; V_{EE} = −4.5 V; output load = 50 Ω to −2.0 V

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions
Output voltage, high	V_{OH}	−1025		−880	mV	V_{IN} = V_{IH} max or V_{IL} min
Output voltage, low	V_{OL}	−1810		−1620	mV	V_{IN} = V_{IH} max or V_{IL} min
Output threshold voltage, high	V_{OHC}	−1035			mV	V_{IN} = V_{IH} min or V_{IL} max
Output threshold voltage, low	V_{OLC}			−1610	mV	V_{IN} = V_{IH} min or V_{IL} max
Input voltage, high	V_{IH}	−1165		−880	mV	For all inputs
Input voltage, low	V_{IL}	−1810		−1475	mV	For all inputs
Input current, high	I_{IH}			220	μA	V_{IN} = V_{IH} max
Input current, low	I_{IL}	0.5		170	μA	For $\overline{BS}_1$-$\overline{BS}_4$: V_{IN} = V_{IL} min
		−50			μA	For all others: V_{IN} = V_{IL} min
Supply current	I_{EE}	−220			mA	All inputs and outputs open

Notes:

(1) Device under test is mounted in a test socket and measured at a thermal equilibrium established with a transverse air flow maintained at greater than 2.0 m/s.

AC Characteristics

T_A = 0 to +85 °C; V_{EE} = −4.5 V ± 5%

		μPB100422-7			μPB100422-10				
Parameter	Symbol	Min	Typ	Max	Min	Typ	Max	Unit	Test Conditions
Read Operation									
Block select access time	t_{ABS}			5			5	ns	
Block select recovery time	t_{RBS}			5			5	ns	
Address access time	t_{AA}			7			10	ns	
Write Operation									
Write pulse width	t_W	5			6			ns	
Data setup time	t_{WSD}	1			2			ns	
Data hold time	t_{WHD}	1			2			ns	
Address setup time	t_{WSA}	1			2			ns	
Address hold time	t_{WHA}	1			2			ns	
Block select setup time	t_{WSBS}	1			2			ns	
Block select hold time	t_{WHBS}	1			2			ns	
Write disable time	t_{WS}			5			5	ns	
Write recovery time	t_{WR}			6			9	ns	
Output Rise and Fall Times									
Output rise time	t_R		2			2		ns	
Output fall time	t_F		2			2		ns	

Notes:

(1) Device under test is mounted in a test socket and measured at a thermal equilibrium established with a transverse air flow maintained at greater than 2.0 m/s.

(2) All timing measurements are referenced to 50% input levels.

(3) The output load is shown in figure 1.

(4) Input transition times are shown in figure 2.

8

Figure 1. Loading Conditions Test Circuit

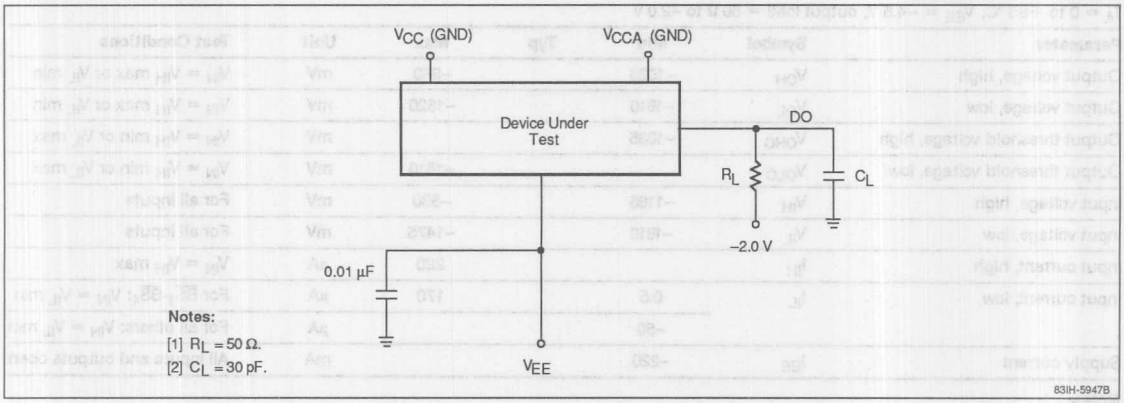
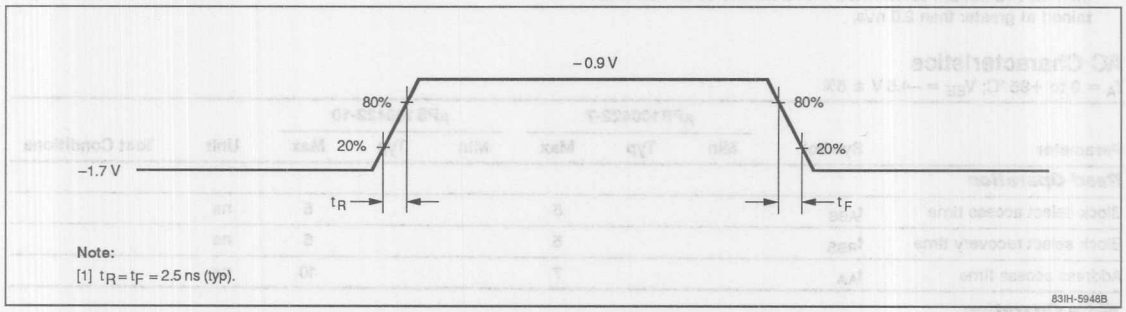
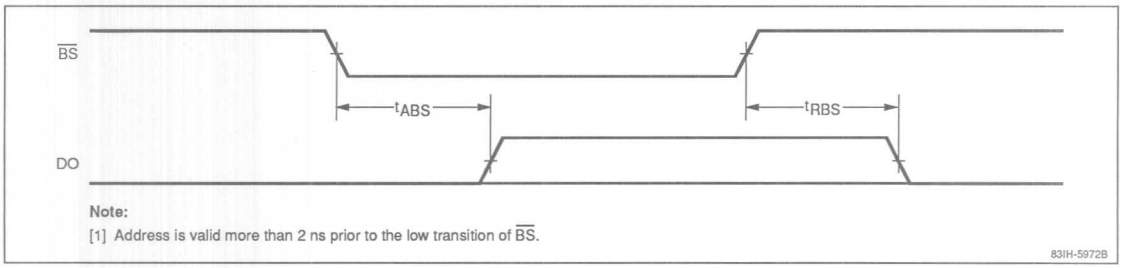


Figure 2. Input Pulse



Timing Waveforms

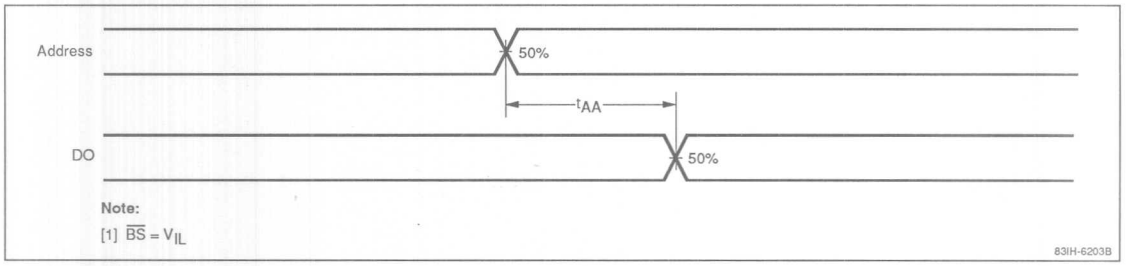
Chip Select Access



Note:
[1] Address is valid more than 2 ns prior to the low transition of $\overline{BS}$.

83IH-5972B

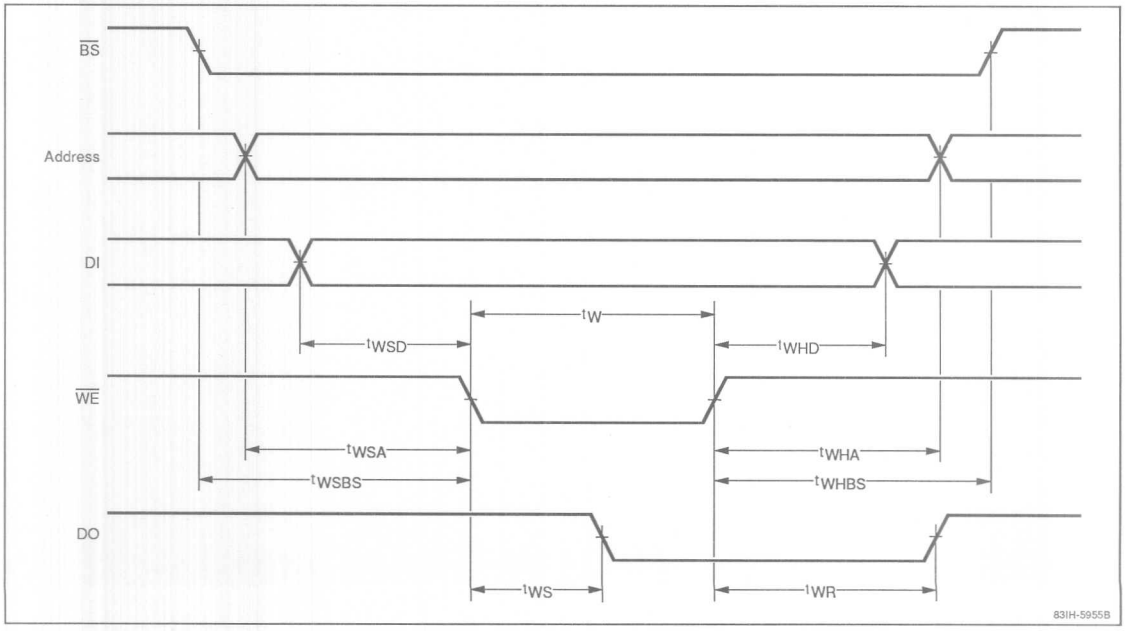
Address Access Cycle



Note:
[1] $\overline{BS} = V_{IL}$

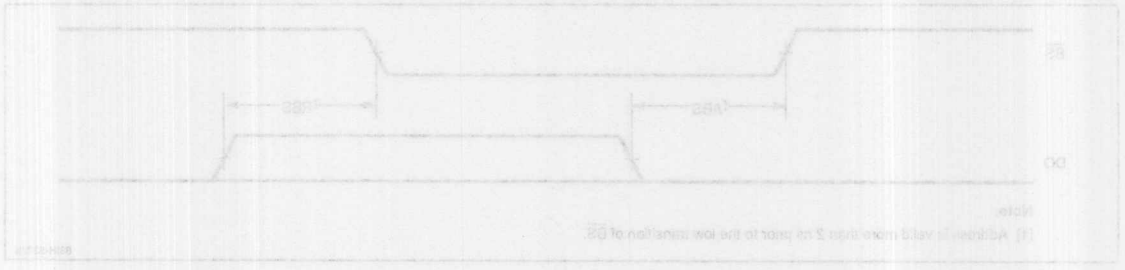
83IH-6203B

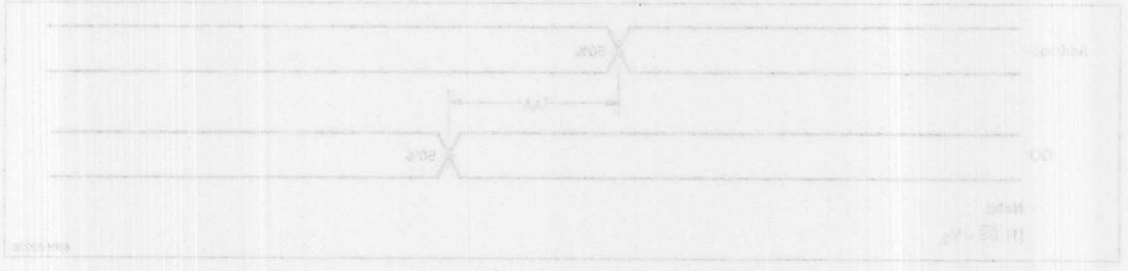
Write Cycle

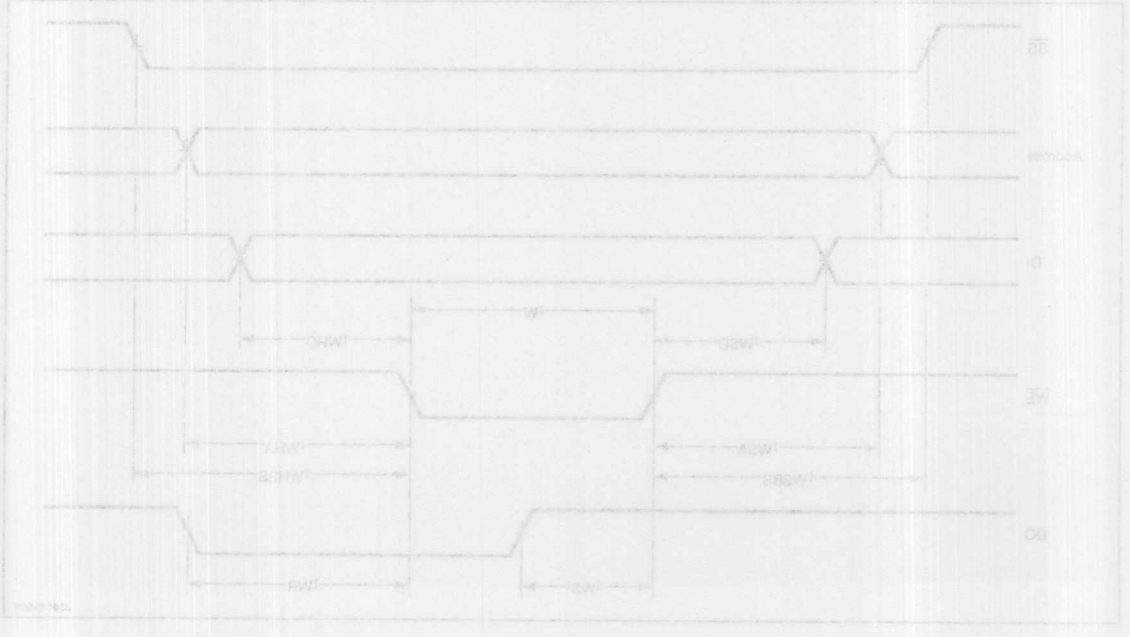


83IH-5955B

8







μPB100470
4,096 x 1-BIT
100K ECL RAM

Description

The μPB100470 is a very high-speed 100K interface ECL RAM with full voltage and temperature compensation. The device is organized as 4K words by 1 bit, and is designed with an open emitter output (noninverted) for low power consumption. Two fast access time versions are available: 10 ns maximum and 15 ns maximum. The μPB100470 is available in a hermetic, 300-mil, 18-pin cerdip.

Features

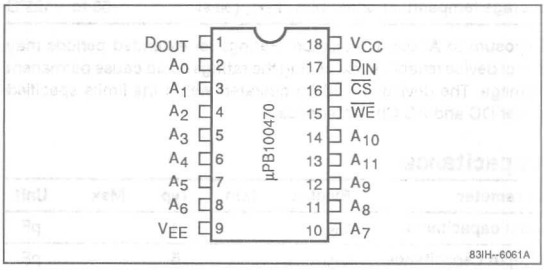
- 4,096-word x 1-bit organization
- 100K ECL interface with full voltage and temperature compensation
- Open emitter output (noninverted)
- Fast access times
- Low power consumption
- 300-mil, 18-pin cerdip packaging

Ordering Information

Part Number	Access Time (max)	Package
μPB100470D-10	10 ns	18-pin cerdip
D-15	15 ns	

Pin Configuration

18-Pin Cerdip



Pin Identification

Symbol	Function
A_0 - A_{11}	Address inputs
D_{IN}	Data input
D_{OUT}	Data output
$\overline{CS}$	Chip select
$\overline{WE}$	Write enable
V_{CC}	Ground
V_{EE}	−4.5-volt power supply

8

Absolute Maximum Ratings

Supply voltage, V_{EE} to V_{CC}	−7.0 to +0.5 V
Input voltage, V_{IN}	V_{EE} to +0.5 V
Output current, I_{OUT}	−30 to +0.1 mA
Storage temperature, T_{STG}	−65 to +150°C
Storage temperature under bias, T_{STG} (bias)	−55 to +125°C

Exposure to Absolute Maximum Ratings for extended periods may affect device reliability; exceeding the ratings could cause permanent damage. The device should be operated within the limits specified under DC and AC Characteristics.

Capacitance

Parameter	Symbol	Min	Typ	Max	Unit
Input capacitance	C_{IN}		4		pF
Output capacitance	C_{OUT}		5		pF

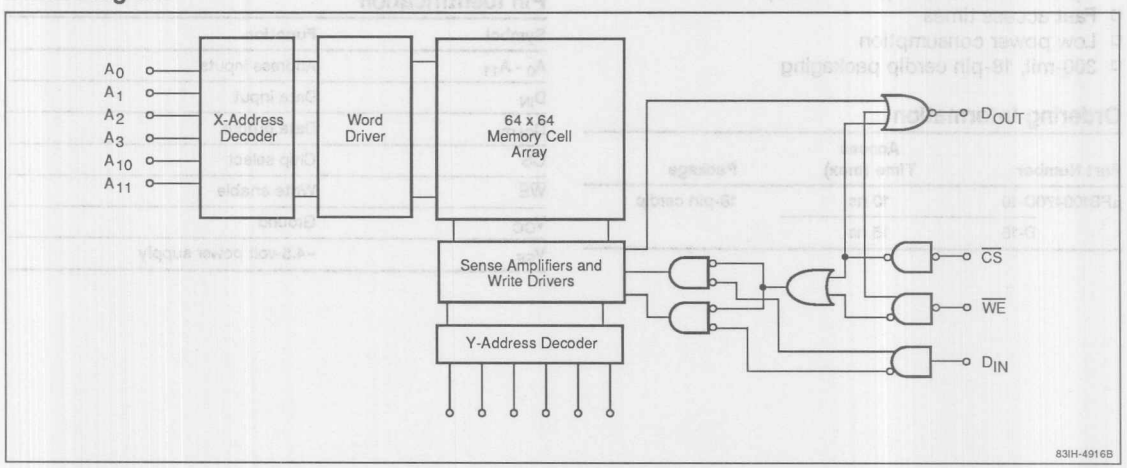
Truth Table

$\overline{CS}$	$\overline{WE}$	D_{IN}	Function	Output
H	X	X	Not selected	L
L	L	L	Write 0	L
L	L	H	Write 1	L
L	H	X	Read	D_{OUT}

Notes:

(1) X = don't care.

Block Diagram



DC Characteristics

T_A = 0 to +85°C; V_{EE} = −4.5 V; output load = 50 Ω to −2.0 V

Parameter	Symbol	Min	Max	Unit	Test Conditions
Output voltage, high	V_{OH}	−1025	−880	mV	$V_{IN} = V_{IH}$ (max) or V_{IL} (min)
Output voltage, low	V_{OL}	−1810	−1620	mV	
Output threshold voltage, high	V_{OHC}	−1035		mV	$V_{IN} = V_{IH}$ (min) or V_{IL} (max)
Output threshold voltage, low	V_{OLC}		−1610	mV	
Input voltage, high	V_{IH}	−1165	−880	mV	Guaranteed input voltage high for all inputs
Input voltage, low	V_{IL}	−1810	−1475	mV	Guaranteed input voltage low for all inputs
Input current, high	I_{IH}		220	μA	$V_{IN} = V_{IH}$ (max)
Input current, low	I_{IL}	0.5	170	μA	For $\overline{CS}$: $V_{IN} = V_{IL}$ (min)
		−50		μA	For all others: $V_{IN} = V_{IL}$ (min)
Supply current	I_{EE}	−220		mA	All inputs and outputs open

Notes:

(1) The device under test (DUT) is mounted in a test socket and is measured at a thermal equilibrium established with a transverse air flow maintained at greater than 2.0 m/s.

AC Characteristics

T_A = 0 to +85°C; V_{EE} = −4.5 V ± 5%

		μPB100470-10			μPB100470-15				
Parameter	Symbol	Min	Typ	Max	Min	Typ	Max	Unit	Test Conditions
Read Operation									
Address access time	t_{AA}			10			15	ns	
Chip select access time	t_{ACS}			6			8	ns	
Chip select recovery time	t_{RCS}			6			8	ns	
Write Operation									
Write pulse width	t_W	10			15			ns	
Data setup time	t_{WSD}	2			2			ns	
Data hold time	t_{WHD}	2			2			ns	
Address setup time	t_{WSA}	3			3			ns	
Address hold time	t_{WHA}	2			2			ns	
Chip select setup time	t_{WSCS}	2			2			ns	
Chip select hold time	t_{WHCS}	2			2			ns	
Write disable time	t_{WS}			6			8	ns	
Write recovery time	t_{WR}			10			10	ns	
Output Rise and Fall Times									
Rise time	t_R		2			2		ns	
Fall time	t_F		2			2		ns	

Notes:

(1) The device under test (DUT) is mounted in a test socket and is measured at a thermal equilibrium established with a transverse air flow maintained at greater than 2.0 m/s.

Figure 1. Loading Conditions Test Circuit

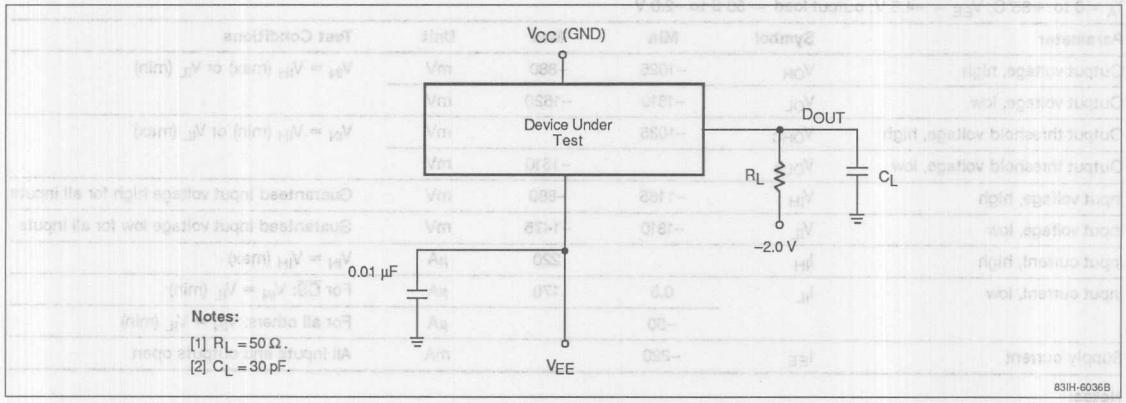
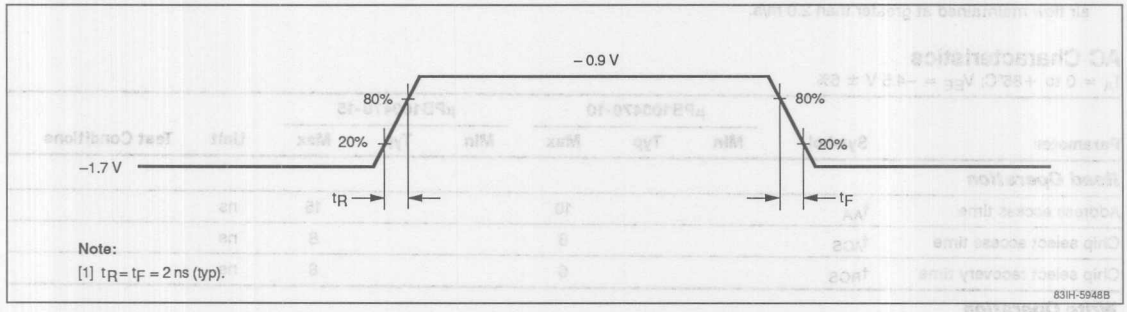
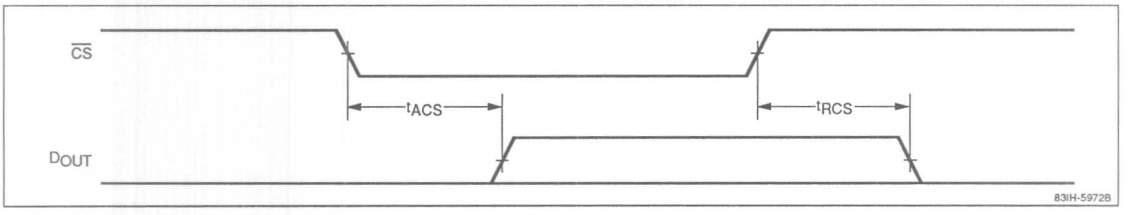


Figure 2. Input Pulse

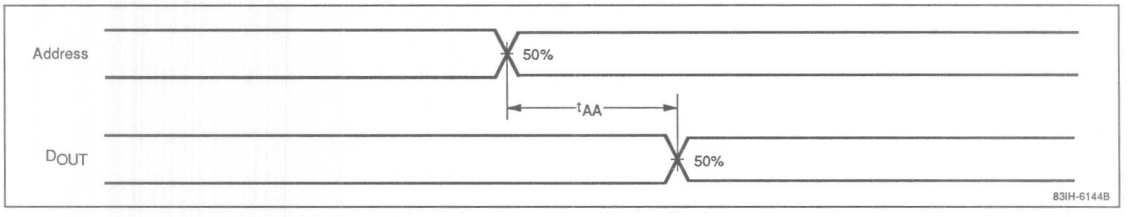


Timing Waveforms

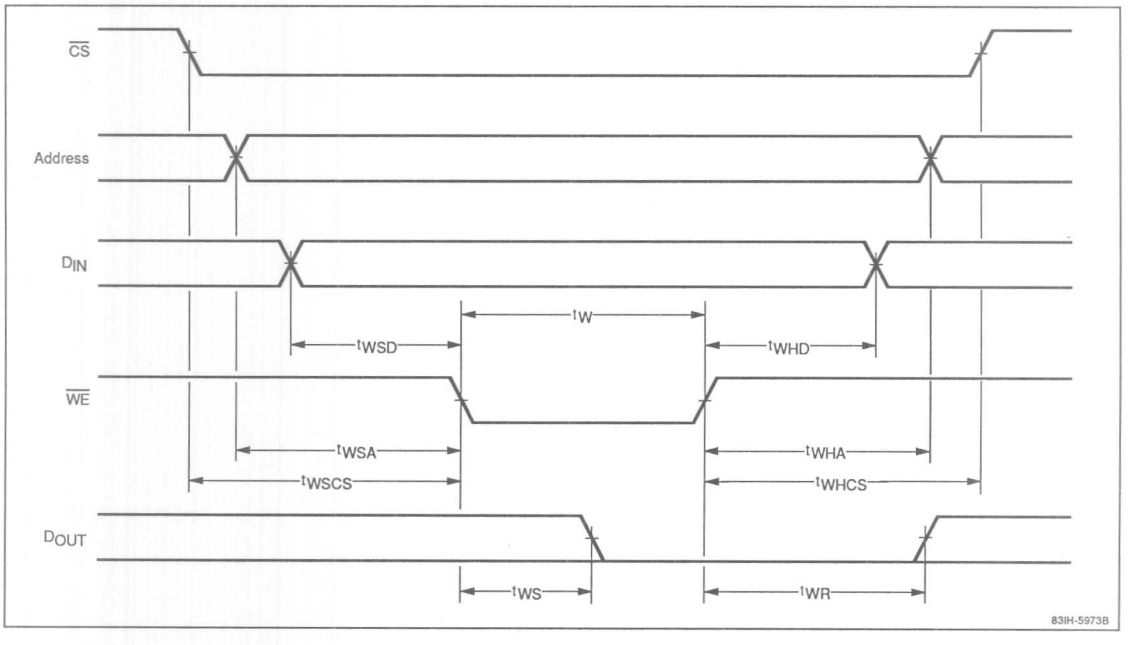
Chip Select Access Cycle



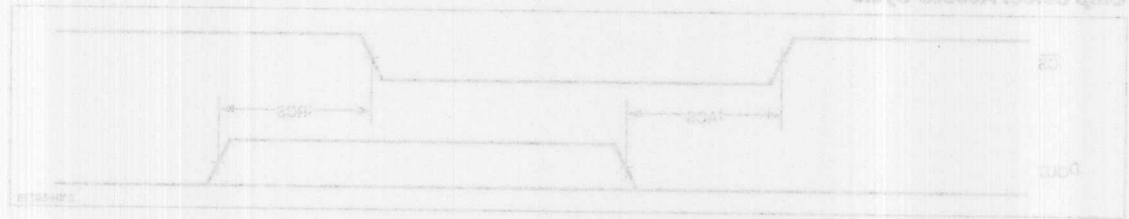
Address Access Cycle

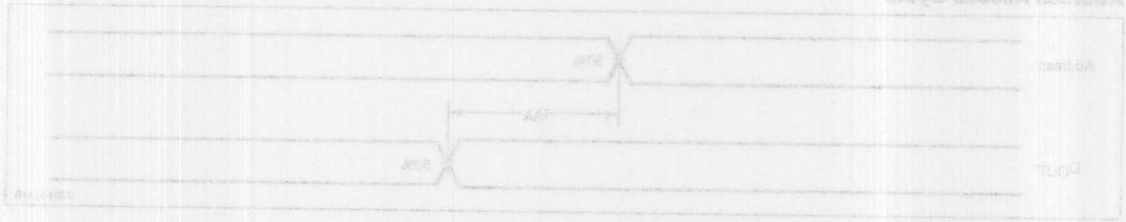


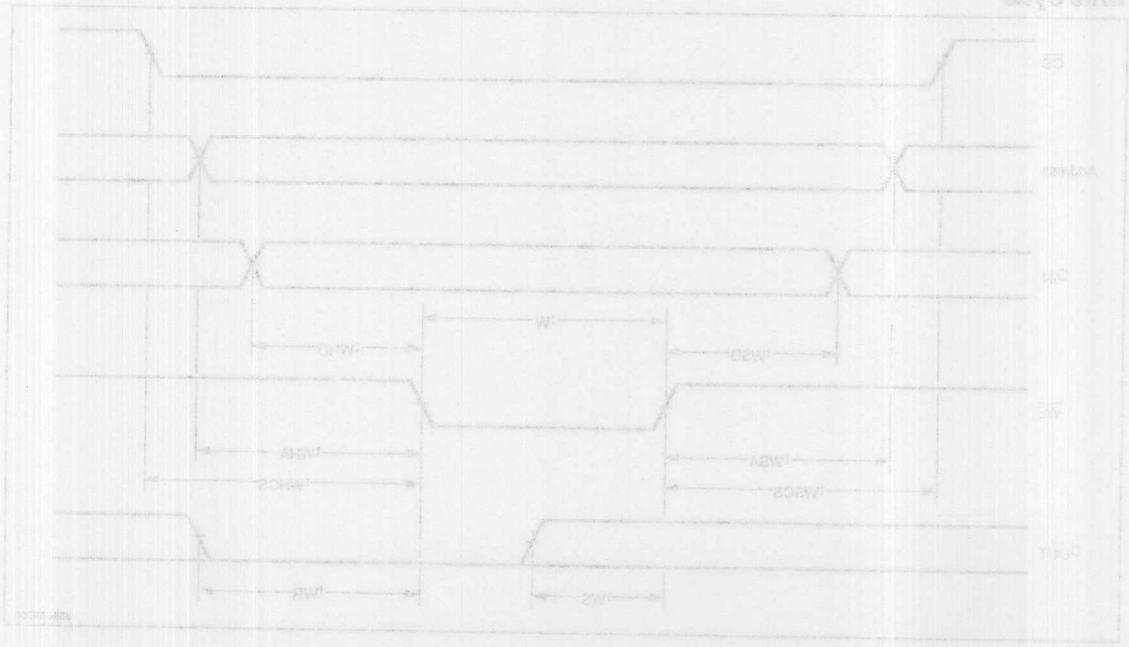
Write Cycle



8







μPB100474
1,024, x 4-Bit
100K ECL RAM

Description

NEC's μPB100474 is a very high-speed 100K interface ECL RAM organized as 1,024 words by 4 bits and designed with open-emitter, noninverted outputs. It is available in a 24-pin cerdip, 24-pin ceramic LCC, or 24-pin ceramic flatpack package.

Features

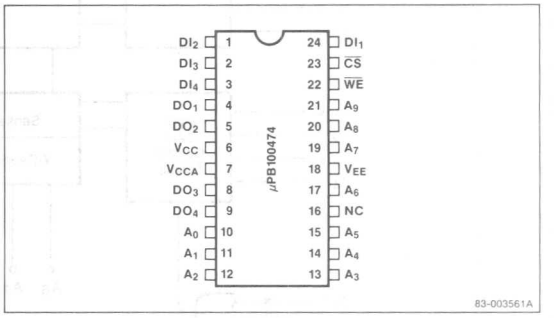
- 1024-word by 4-bit organization
- 100K interface ECL
- Full voltage and temperature compensation
- Noninverted, open emitter outputs
- Fast access times
- 24-pin cerdip, ceramic LCC, and ceramic flatpack packaging

Ordering Information

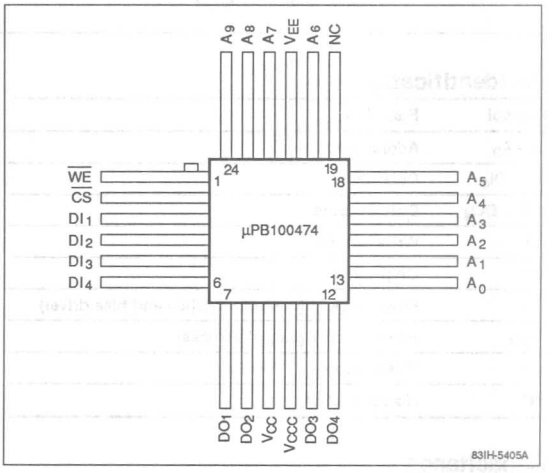
Part Number	Access Time (max)	Supply Current (min)	Package
μPB100474B-6	6 ns	−450 mA	24-pin ceramic flatpack
B-8	8 ns	−220 mA	
B-10	10 ns		
B-15	15 ns		
μPB100474D-8	8 ns	−220 mA	24-pin cerdip
D-10	10 ns		
D-15	15 ns		
μPB100474K-4.5	4.5 ns	−450 mA	24-pin ceramic LCC
K-6	6 ns		

Pin Configurations

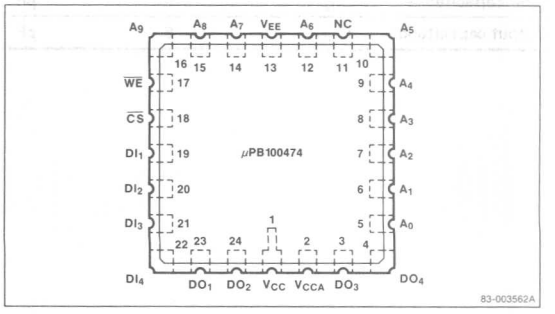
24-Pin Cerdip



24-Pin Ceramic Flatpack

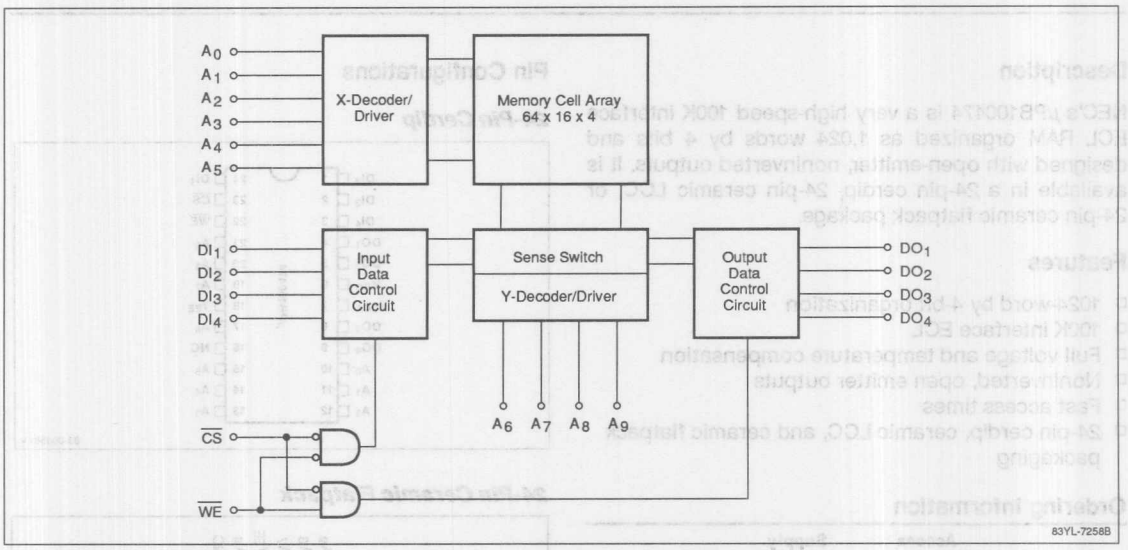


24-Pin Ceramic LCC



8

Block Diagram



Pin Identification

Symbol	Function
A_0 - A_9	Addresses
DI_1 - DI_4	Data inputs
DO_1 - DO_4	Data outputs
$\overline{WE}$	Write enable
$\overline{CS}$	Chip select
V_{CC}	Power supply (current switches and bias driver)
V_{CCA}	Power supply (output devices)
V_{EE}	Power supply
NC	No connection

Capacitance

Parameter	Symbol	Min	Typ	Max	Unit
Input capacitance	C_{IN}		4		pF
Output capacitance	C_{OUT}		5		pF

Absolute Maximum Ratings

Supply voltage, V_{EE} to V_{CC}	−7.0 V to +0.5
Input voltage, V_{IN}	+0.5 V to V_{EE}
Output current, I_{OUT}	−30 mA to +0.1
Storage temperature, T_{STG}	−65 to +150 °C
Storage temperature under bias, T_{STG} (Bias)	−55 to +125 °C

Exposure to Absolute Maximum Ratings for extended periods may affect device reliability; exceeding the ratings could cause permanent damage. The device should be operated within the limits specified under DC and AC Characteristics.

Truth Table

$\overline{CS}$	$\overline{WE}$	D_{IN}	Output	Function
H	X	X	L	Not selected
L	L	L	L	Write 0
L	L	H	L	Write 1
L	H	X	D_{OUT}	Read

Notes:

(1) X = don't care.

DC Characteristics

T_A = 0 to +85°C; V_{EE} = −4.5 V; output load = 50 Ω to −2.0 V

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions
Output voltage, high	V_{OH}	−1025		−880	mV	V_{IN} = V_{IH} max or V_{IL} min
Output voltage, low	V_{OL}	−1810		−1620	mV	V_{IN} = V_{IH} max or V_{IL} min
Output threshold voltage, high	V_{OHC}	−1035			mV	V_{IN} = V_{IH} min or V_{IL} max
Output threshold voltage, low	V_{OLC}			−1610	mV	V_{IN} = V_{IH} min or V_{IL} max
Input voltage, high	V_{IH}	−1165		−880	mV	Guaranteed input voltage high for all inputs
Input voltage, low	V_{IL}	−1810		−1475	mV	Guaranteed input voltage low for all inputs
Input current, high	I_{IH}			220	μA	V_{IN} = V_{IH} max
Input current, low	I_{IL}	0.5		170	μA	For $\overline{CS}$: V_{IN} = V_{IL} min
		−50			μA	For all others: V_{IN} = V_{IL} min
Supply current	I_{EE}	−220			mA	t_{AA} = 8/10/15 ns; all inputs and outputs open
		−450			mA	t_{AA} = 4.5/6 ns; all inputs and outputs open (Note 2)

Notes:

(1) The device under test is mounted in a test socket and is measured at a thermal equilibrium established with a transverse air flow maintained at greater than 2.0 ms.

(2) For the μPB100474-4.5/-6, take measures to reduce the thermal resistance and to keep the junction temperature less than 90 °C. Forced air and appropriate fins on the substrate on which the package is mounted, or on the package itself, are recommended. The thermal resistance of the junction to the case (bottom side) of an LCC or flatpack package is less than 10°C/W.

Figure 1. Loading Conditions Test Circuit

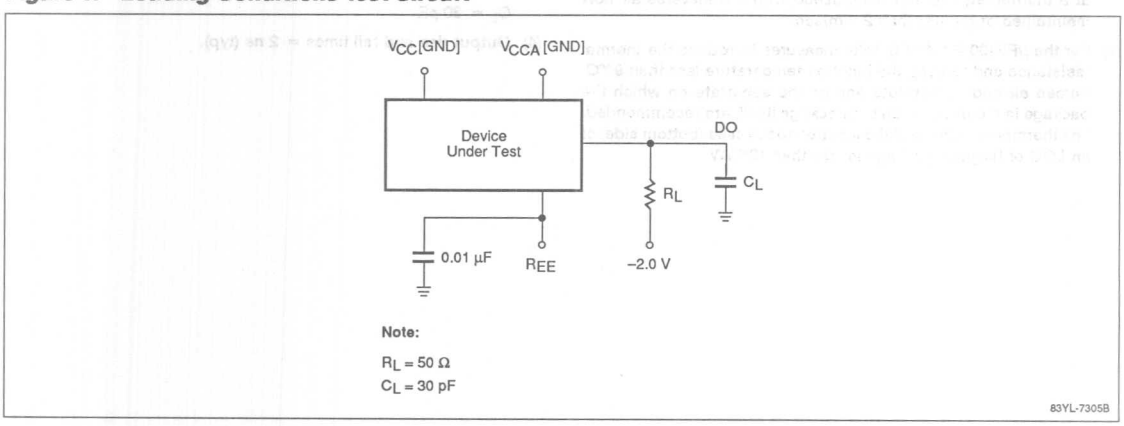
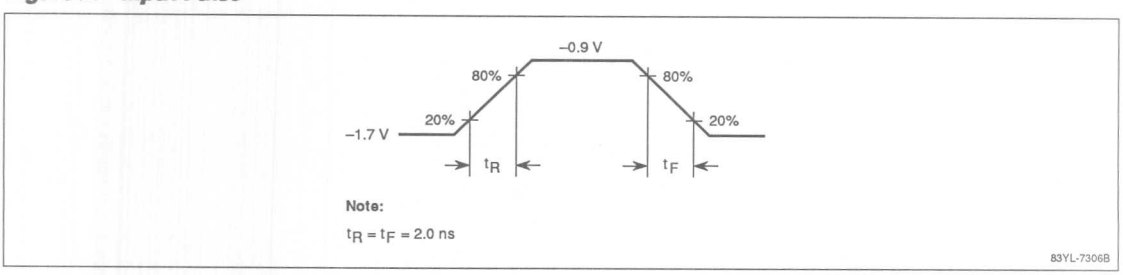


Figure 2. Input Pulse



8

AC Characteristics

T_A = 0 to +85°C; V_{EE} = −4.5 V ±5%

		μPB100474-4.5		μPB100474-6		μPB100474-8		μPB100474-10		μPB100474-15		
Parameter	Symbol	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Unit
Read Operation												
Chip select access time	t_{ACS}		4		4		5		6		8	ns
Chip select recovery time	t_{RCS}		4		4		5		6		8	ns
Address access time	t_{AA}		4.5		6		8		10		15	ns
Write Operation												
Write pulse width	t_W	4.5		6		6		10		15		ns
Data setup time	t_{WSD}	1		1		1		2		2		ns
Data hold time	t_{WHD}	1		1		1		2		2		ns
Address setup time	t_{WSA}	1		1		1		3		3		ns
Address hold time	t_{WHA}	2		2		1		2		2		ns
Chip select setup time	t_{WSCS}	1		1		1		2		2		ns
Chip select hold time	t_{WHCS}	1		1		1		2		2		ns
Write disable time	t_{WS}		4		4		5		6		8	ns
Write recovery time	t_{WR}		4.5		6		8		10		10	ns

Notes:

(1) The device under test is mounted in a test socket and is measured at a thermal equilibrium established with a transverse air flow maintained at greater than 2.0 m/sec.

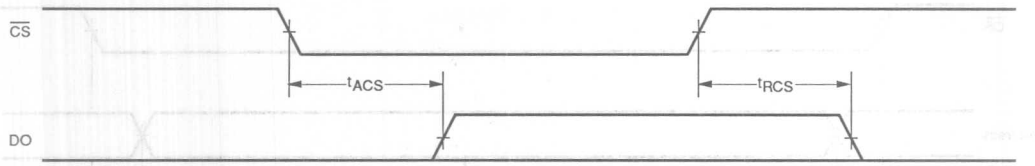
(2) For the μPB100474-4.5/-6, take measures to reduce the thermal resistance and to keep the junction temperature less than 90°C. Forced air and appropriate fins on the substrate on which the package is mounted, or on the package itself, are recommended. The thermal resistance of the junction to the case (bottom side) of an LCC or flatpack package is less than 10°C/W.

(3) See figures 1 and 2 for loading conditions and input pulse timing. For the μPB100474-4.5/-6, C_L = 5 pF. For the μPB100474-8/10/15, C_L = 30 pF.

(4) Output rise and fall times = 2 ns (typ).

Timing Waveforms

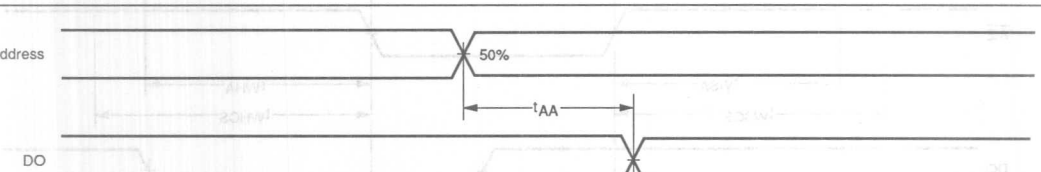
Chip Select Access Cycle



Note:
[1] Address is valid more than 2 ns prior to the low transition of $\overline{CS}$.
[2] $\overline{WE} = V_{IH}$.

83IH-6164B

Address Access Cycle



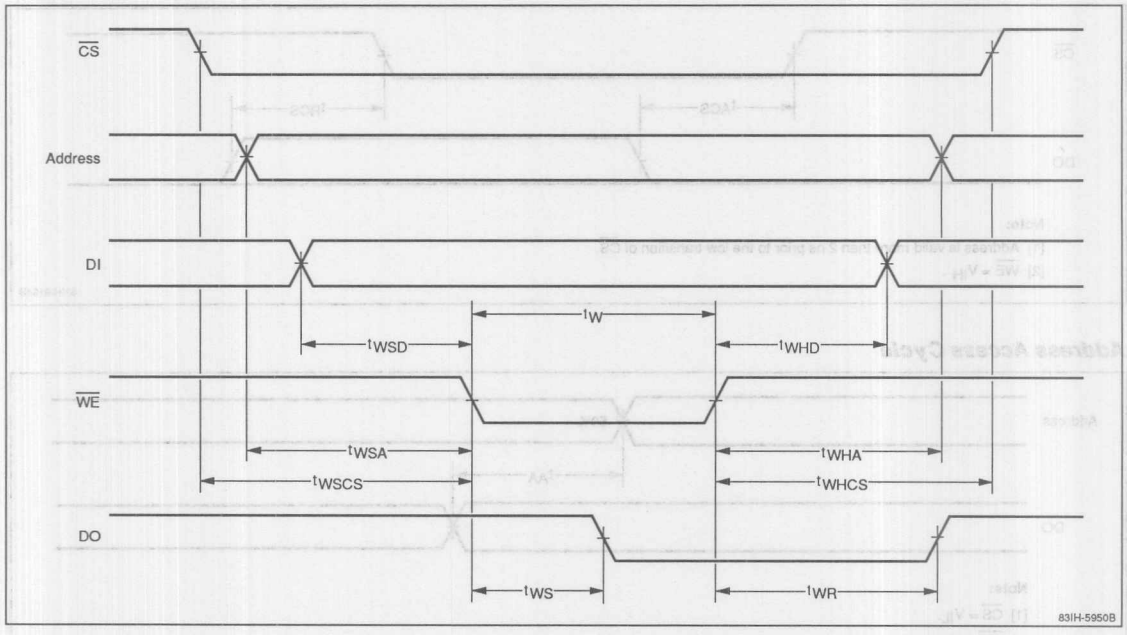
Note:
[1] $\overline{CS} = V_{IL}$.
[2] $\overline{WE} = V_{IH}$.

83IH-6144B

8

Timing Waveforms (cont)

Write Cycle



μPB100474A
1,024 x 4-Bit
100K ECL RAM

Description

The μPB100474A is a very high-speed 100K interface ECL RAM organized as 1,024 words by 4 bits and designed with noninverted, open emitter outputs and full voltage and temperature compensation. The device is packaged in a 24-pin cerdip or ceramic flatpack.

Features

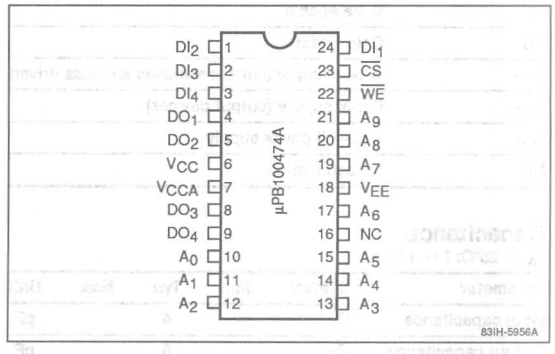
- 1,024 word by 4-bit organization
- 100K ECL interface
- Full voltage and temperature compensation
- Open emitter outputs (noninverted)
- Fast access times
- 24-pin cerdip and flatpack packaging

Ordering Information

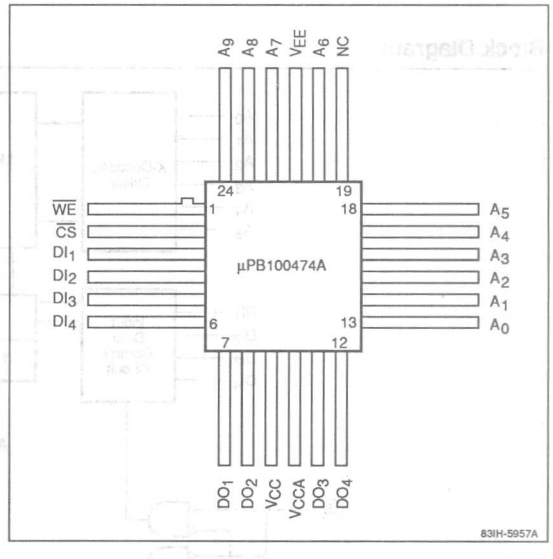
Part Number	Access Time (max)	Supply Current (min)	Package
μPB100474AD-5	5 ns	–250 mA	24-pin cerdip
AD-6	6 ns		
μPB100474ABH-5	5 ns	–250 mA	24-pin ceramic flatpack
ABH-6	6 ns		

Pin Configurations

24-Pin Cerdip



24-Pin Ceramic Flatpack



8

Pin Identification

Symbol	Function
A_0 - A_9	Address inputs
DI_1 - DI_4	Data inputs
DO_1 - DO_4	Data outputs
$\overline{WE}$	Write enable
$\overline{CS}$	Chip select
V_{CC}	Power supply (current switches and bias driver)
V_{CCA}	Power supply (output devices)
V_{EE}	–4.5-volt power supply
NC	No connection

Capacitance

T_A = 25°C; f = 1 MHz

Parameter	Symbol	Min	Typ	Max	Unit
Input capacitance	C_I		4		pF
Output capacitance	C_O		6		pF

Absolute Maximum Ratings

Supply voltage, V_{EE} to V_{CC}	–7.0 to +0.5 V
Input voltage, V_{IN}	V_{EE} to +0.5 V
Output current, I_{OUT}	–30 to +0.1 mA
Storage temperature, T_{STG}	–65 to +150°C
Storage temperature under bias, T_{STG} (Bias)	–55 to +125°C

Exposure to Absolute Maximum Ratings for extended periods may affect device reliability; exceeding the ratings could cause permanent damage. The device should be operated within the limits specified under DC and AC Characteristics.

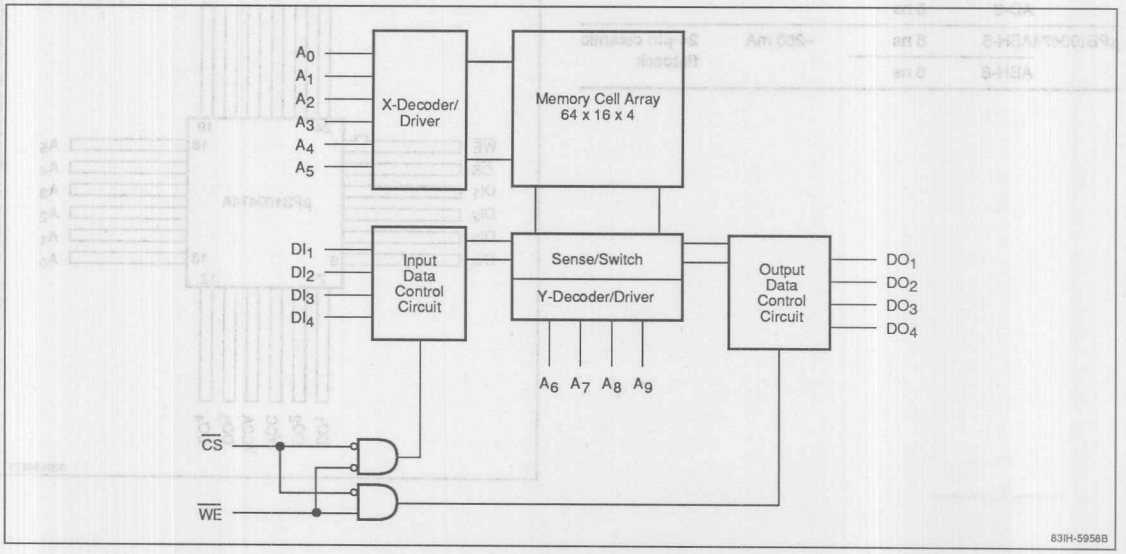
Truth Table

Function	$\overline{CS}$	$\overline{WE}$	D_{IN}	Output
Not selected	H	X	X	L
Write 0	L	L	L	L
Write 1	L	L	H	L
Read	L	H	X	D_{OUT}

Notes:

(1) X = don't care.

Block Diagram



DC Characteristics

T_A = 0 to +85°C; V_{EE} = −4.5 V; output load = 50 Ω to −2.0 V; V_{CC} = V_{CCA} = 0 V

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions
Output voltage, high	V_{OH}	−1025		−880	mV	V_{IN} = V_{IH} (max) or V_{IL} (min)
Output voltage, low	V_{OL}	−1810		−1620	mV	V_{IN} = V_{IH} (max) or V_{IL} (min)
Output threshold voltage, high	V_{OHC}	−1035			mV	V_{IN} = V_{IH} (min) or V_{IL} (max)
Output threshold voltage, low	V_{OLC}			−1610	mV	V_{IN} = V_{IH} (min) or V_{IL} (max)
Input voltage, high	V_{IH}	−1165		−880	mV	
Input voltage, low	V_{IL}	−1810		−1475	mV	
Input current, high	I_{IH}			220	μA	V_{IN} = V_{IH} (max)
Input current, low	I_{IL}	0.5		170	μA	For $\overline{CS}$: V_{IN} = V_{IL} (min)
		−50			μA	For all others: V_{IN} = V_{IL} (min)
Supply current	I_{EE}	−250			mA	All inputs and outputs open

Notes:

(1) The device under test (DUT) is mounted in a test socket and is measured at a thermal equilibrium established with a transverse air flow maintained at greater than 2.0 m/sec.

AC Characteristics

T_A = 0 to +85°C; V_{EE} = −4.5 V ±5%; output load = 50 Ω to −2.0 V; V_{CC} = V_{CCA} = 0 V

		μPB100474A-5			μPB100474A-6				
Parameter	Symbol	Min	Typ	Max	Min	Typ	Max	Unit	Test Conditions
Read Operation									
Address access time	t_{AA}			5			6	ns	
Chip select access time	t_{ACS}			3			4	ns	
Chip select recovery time	t_{RCS}			3			4	ns	
Write Operation									
Write pulse width	t_W	5			6			ns	
Data setup time	t_{WSD}	1			1			ns	
Data hold time	t_{WHD}	1			1			ns	
Address setup time	t_{WSA}	1			1			ns	
Address hold time	t_{WHA}	1			1			ns	
Chip select setup time	t_{WSCS}	1			1			ns	
Chip select hold time	t_{WHCS}	1			1			ns	
Write disable time	t_{WS}			3			4	ns	
Write recovery time	t_{WR}			6			7	ns	
Rise and Fall Times									
Output rise time	t_R		2			2		ns	
Output fall time	t_F		2			2		ns	

Notes:

(1) The device under test (DUT) is mounted in a test socket and is measured at a thermal equilibrium established with a transverse air flow maintained at greater than 2.0 m/sec.

(2) See figures 1 and 2 for loading conditions and input pulse timing. Input pulse levels = −1.7 to −0.9 V; input rise and fall times (measured between 20% and 80% or 80% and 20%) = 2 ns; input and output timing reference levels = 50%.

8

Figure 1. Loading Conditions Test Circuit

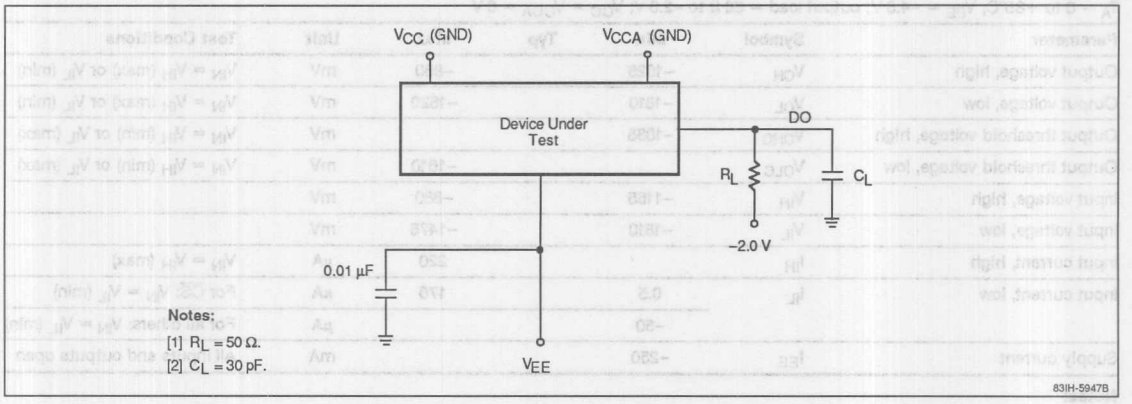
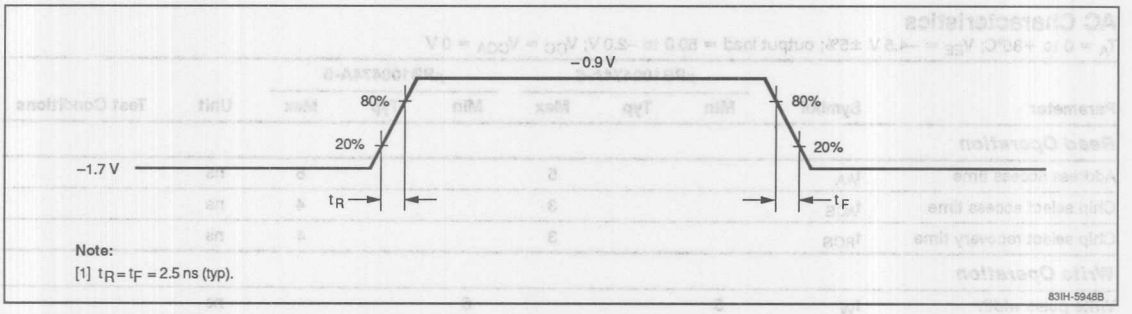
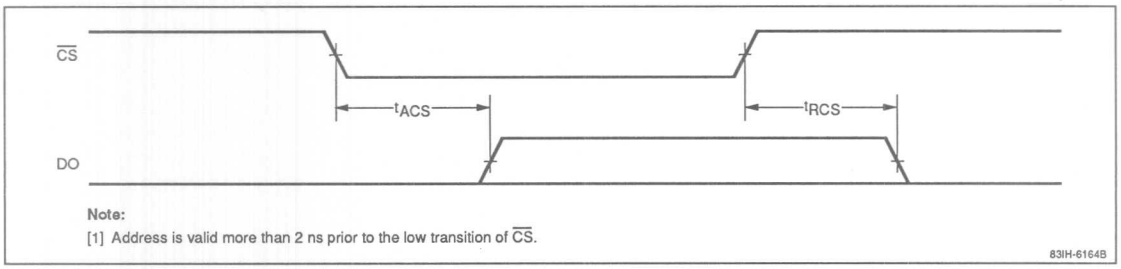


Figure 2. Input Pulse

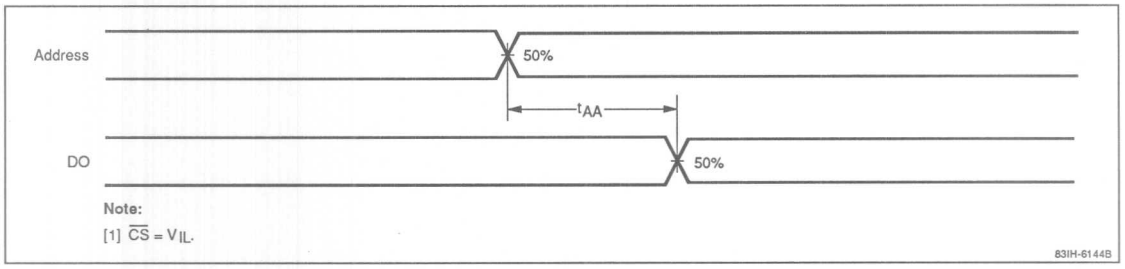


Timing Waveforms

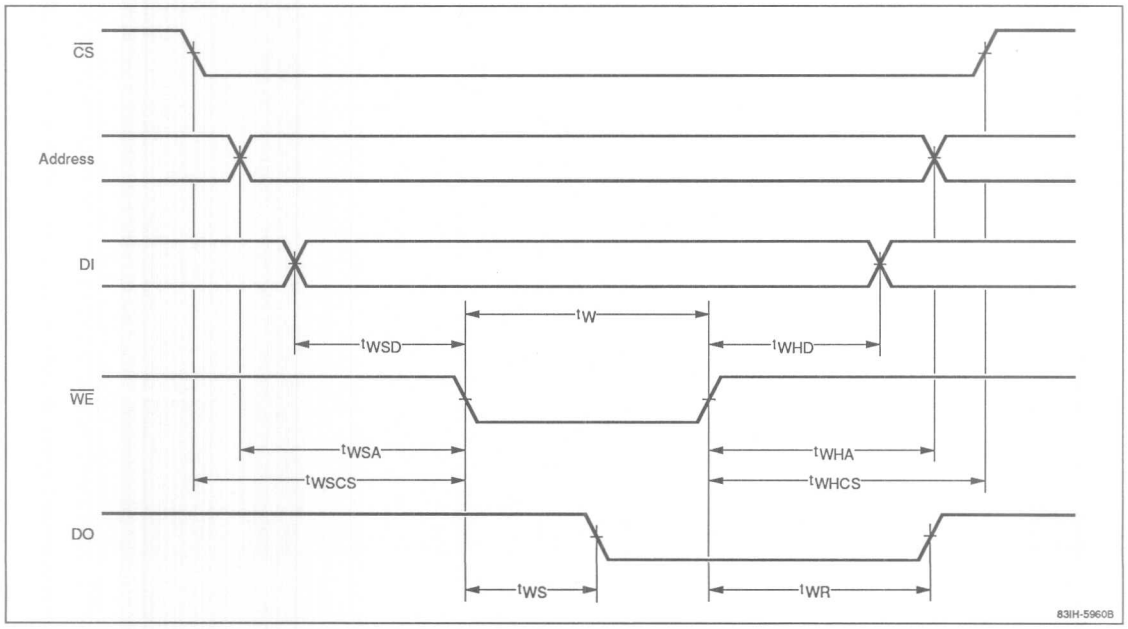
Chip Select Access Cycle



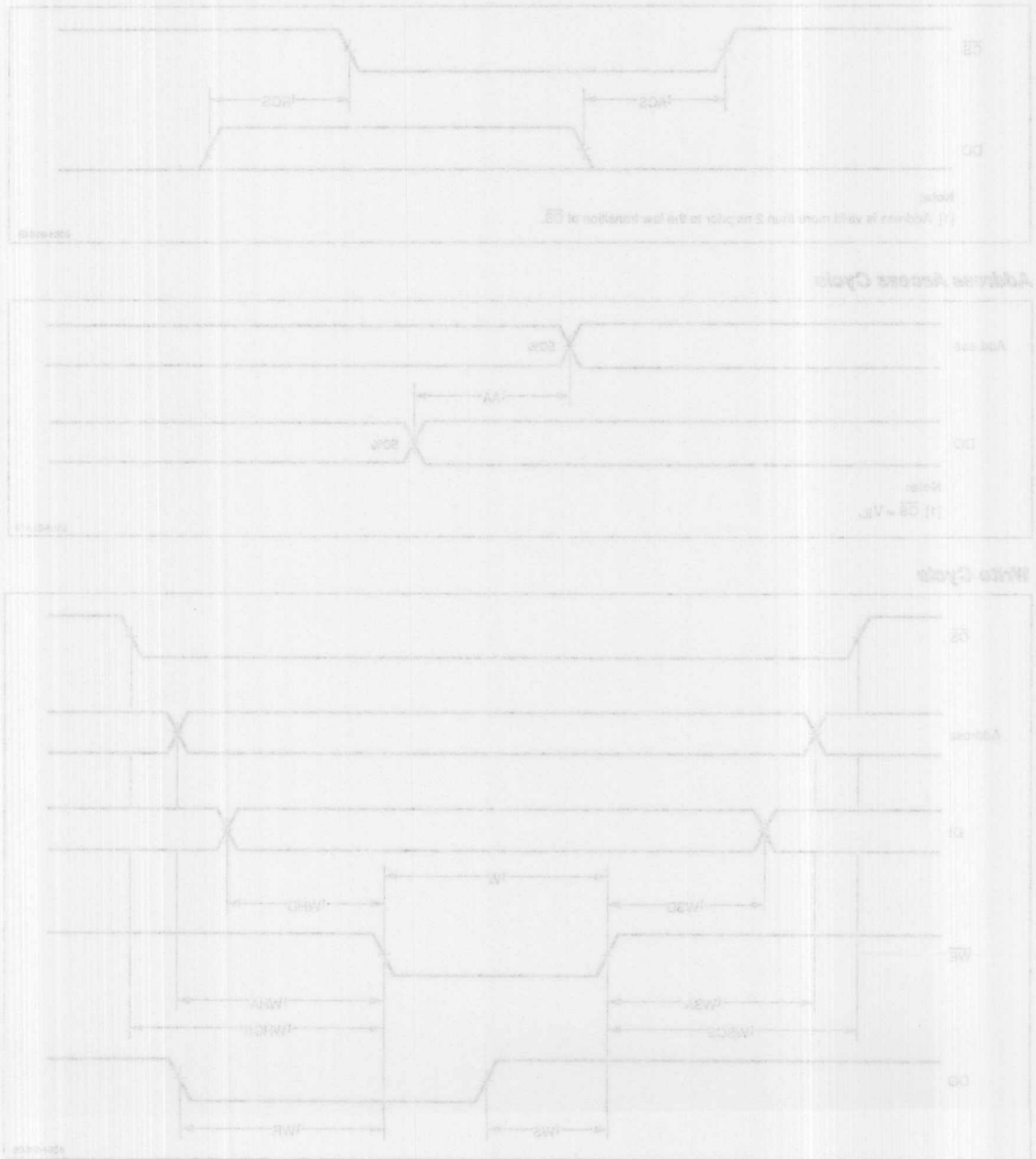
Address Access Cycle



Write Cycle



8



PRELIMINARY INFORMATION

Description

The μPB100474E is a very high-speed 100K interface ECL RAM organized as 1,024 words by 4 bits and designed with noninverted, open emitter outputs and full voltage and temperature compensation. The device is packaged in a 24-pin cerdip or ceramic flatpack.

Features

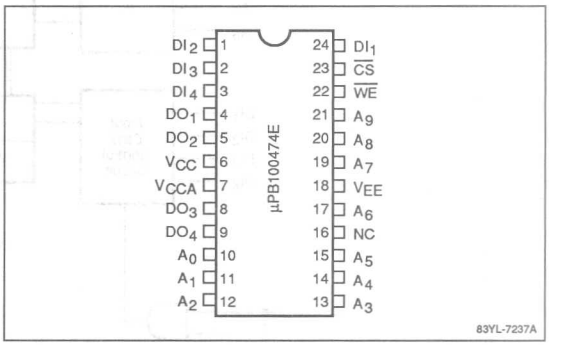
- 1,024 word by 4-bit organization
- 100K ECL interface
- Full voltage and temperature compensation
- Open emitter outputs (noninverted)
- Fast access times
- 24-pin cerdip and flatpack packaging

Ordering Information

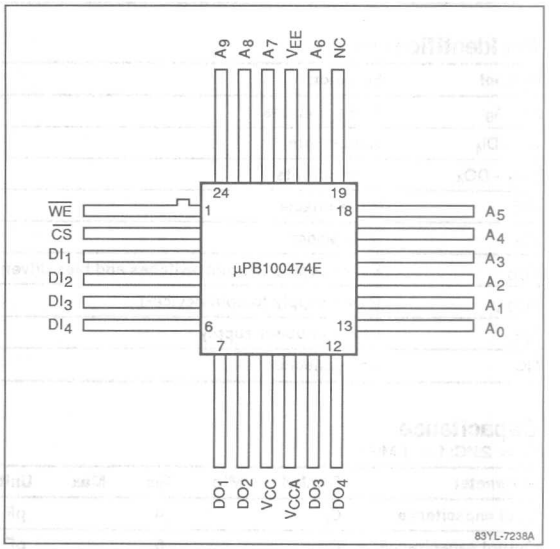
Part Number	Access Time (max)	Supply Current (min)	Package
μPB100474ED-3	3 ns	−330 mA	24-pin cerdip
ED-4	4 ns		
μPB100474EBH-3	3 ns	−330 mA	24-pin ceramic flatpack
EBH-4	4 ns		

Pin Configurations

24-Pin Cerdip

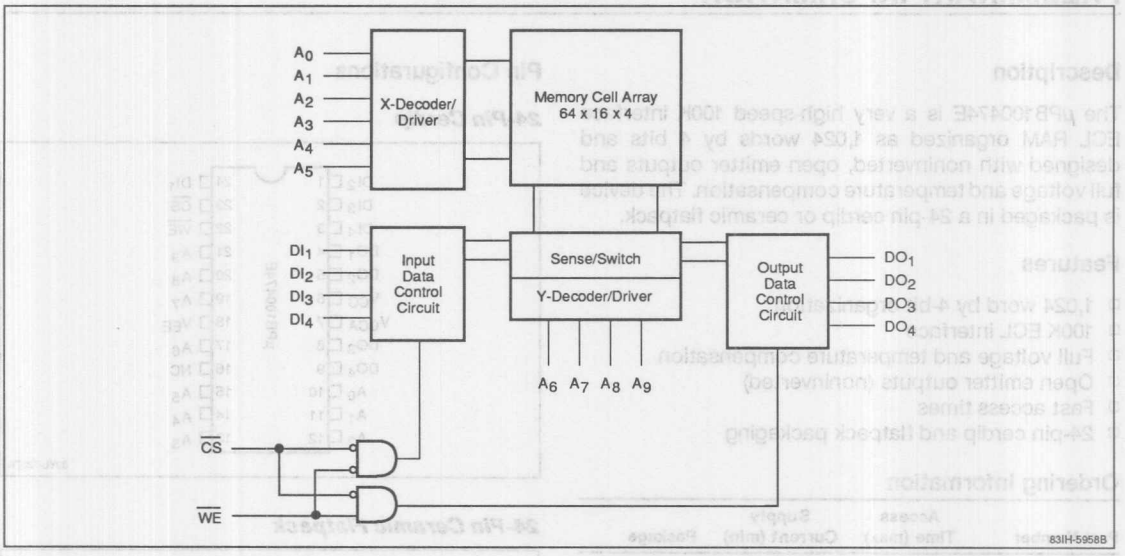


24-Pin Ceramic Flatpack



8

Block Diagram



Pin Identification

Symbol	Function
A_0 - A_9	Address inputs
DI_1 - DI_4	Data inputs
DO_1 - DO_4	Data outputs
$\overline{WE}$	Write enable
$\overline{CS}$	Chip select
V_{CC}	Power supply (current switches and bias driver)
V_{CCA}	Power supply (output devices)
V_{EE}	–4.5-volt power supply
NC	No connection

Capacitance

T_A = 25°C; f = 1 MHz

Parameter	Symbol	Min	Typ	Max	Unit
Input capacitance	C_I		4		pF
Output capacitance	C_O		5		pF

Absolute Maximum Ratings

Supply voltage, V_{EE} to V_{CC}	–7.0 to +0.5 V
Input voltage, V_{IN}	V_{EE} to +0.5 V
Output current, I_{OUT}	–30 to +0.1 mA
Storage temperature, T_{STG}	–65 to +150°C
Storage temperature under bias, T_{STG} (Bias)	–55 to +125°C

Exposure to Absolute Maximum Ratings for extended periods may affect device reliability; exceeding the ratings could cause permanent damage. The device should be operated within the limits specified under DC and AC Characteristics.

Truth Table

Function	$\overline{CS}$	$\overline{WE}$	DI	Output
Not selected	H	X	X	L
Write 0	L	L	L	L
Write 1	L	L	H	L
Read	L	H	X	DO

Notes:

(1) X = don't care.

DC Characteristics

T_A = 0 to +85°C; V_{EE} = −4.5 V; output load = 50 Ω to −2.0 V; V_{CC} = V_{CCA} = 0 V

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions
Output voltage, high	V_{OH}	−1025		−880	mV	V_{IN} = V_{IH} (max) or V_{IL} (min)
Output voltage, low	V_{OL}	−1810		−1620	mV	V_{IN} = V_{IH} (max) or V_{IL} (min)
Output threshold voltage, high	V_{OHC}	−1035			mV	V_{IN} = V_{IH} (min) or V_{IL} (max)
Output threshold voltage, low	V_{OLC}			−1610	mV	V_{IN} = V_{IH} (min) or V_{IL} (max)
Input voltage, high	V_{IH}	−1165		−880	mV	
Input voltage, low	V_{IL}	−1810		−1475	mV	
Input current, high	I_{IH}			220	μA	V_{IN} = V_{IH} (max)
Input current, low	I_{IL}	0.5		170	μA	For $\overline{CS}$: V_{IN} = V_{IL} (min)
		−50			μA	For all others: V_{IN} = V_{IL} (min)
Supply current	I_{EE}	−330			mA	All inputs and outputs open

Notes:

(1) The device under test is mounted in a test socket and is measured at a thermal equilibrium established with a transverse air flow maintained at greater than 2.0 ms.

AC Characteristics

T_A = 0 to +85°C; V_{EE} = −4.5 V ±5%; output load = 50 Ω to −2.0 V; V_{CC} = V_{CCA} = 0 V

		μPB100474E-3			μPB100474E-4				
Parameter	Symbol	Min	Typ	Max	Min	Typ	Max	Unit	Test Conditions
Read Operation									
Address access time	t_{AA}			3			4	ns	
Chip select access time	t_{ACS}			2			3	ns	
Chip select recovery time	t_{RCS}			2			3	ns	
Write Operation									
Write pulse width	t_W	5			6			ns	
Data setup time	t_{WSD}	0.5			0.5			ns	
Data hold time	t_{WHD}	0.5			0.5			ns	
Address setup time	t_{WSA}	0.5			0.5			ns	
Address hold time	t_{WHA}	0.5			0.5			ns	
Chip select setup time	t_{WSCS}	0.5			0.5			ns	
Chip select hold time	t_{WHCS}	0.5			0.5			ns	
Write disable time	t_{WS}			2			3	ns	
Write recovery time	t_{WR}			4			5	ns	
Rise and Fall Times									
Output rise time	t_R		2			2		ns	
Output fall time	t_F		2			2		ns	

Notes:

(1) The device under test is mounted in a test socket and is measured at a thermal equilibrium established with a transverse air flow maintained at greater than 2.0 ms.

(2) See figures 1 and 2 for loading conditions and input pulse timing. Input pulse levels = −1.7 to −0.9 V; input rise and fall times (measured between 20% and 80% or 80% and 20%) = 2 ns; input and output timing reference levels = 50%.

8

Figure 1. Loading Conditions Test Circuit

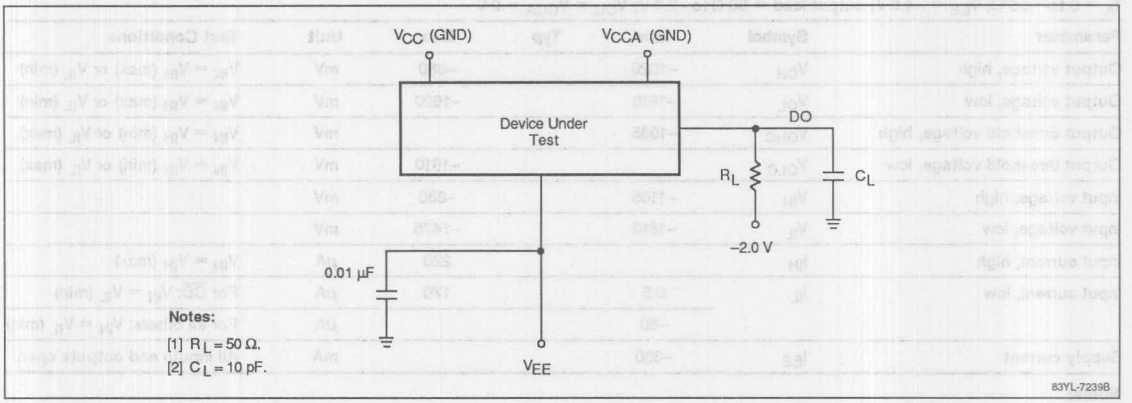
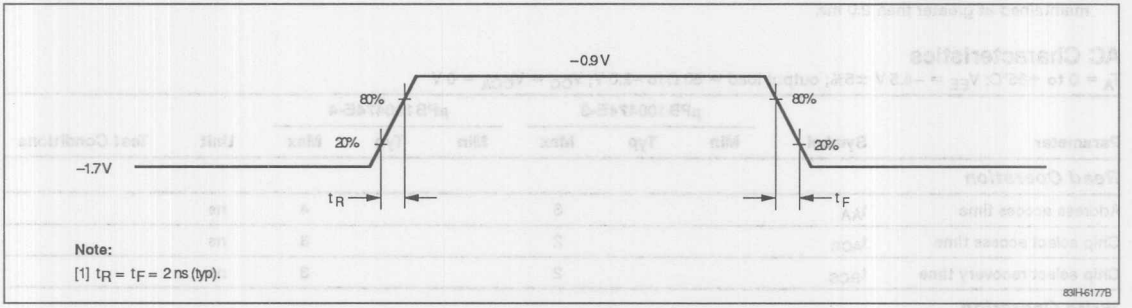
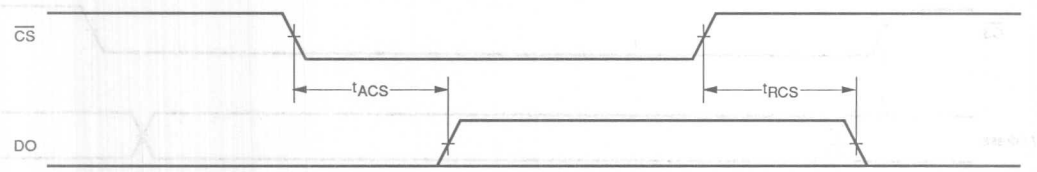


Figure 2. Input Pulse



Timing Waveforms

Chip Select Access Cycle



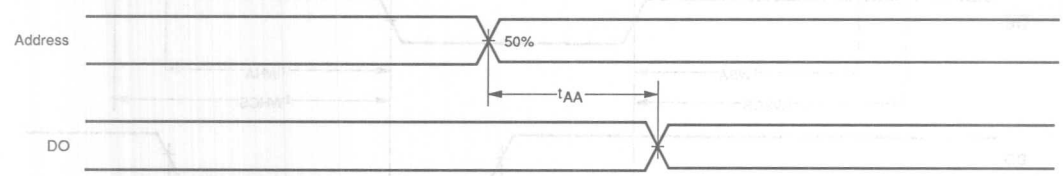
Note:

[1] Address is valid more than 2 ns prior to the low transition of $\overline{CS}$.

[2] $\overline{WE} = V_{IH}$.

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Address Access Cycle



Note:

[1] $\overline{CS} = V_{IL}$.

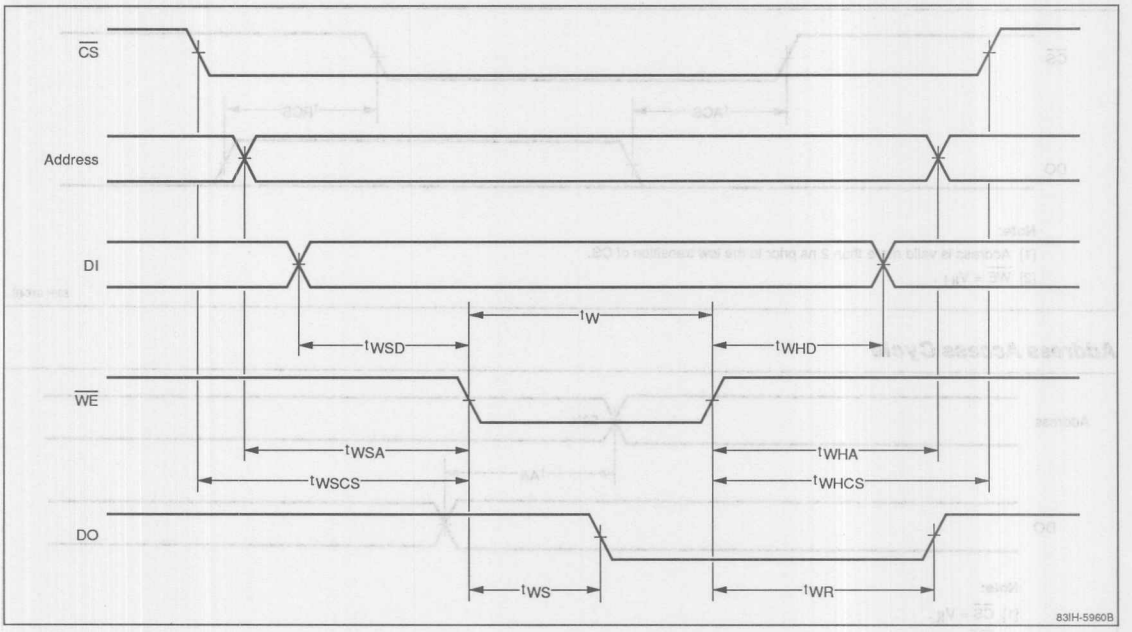
[2] $\overline{WE} = V_{IH}$.

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Timing Waveforms (cont)

Write Cycle



μPB100480
16,384 x 1-Bit
100K ECL RAM

Description

The μPB100480 is a very high-speed 100K interface ECL RAM with full voltage and temperature compensation. The device is organized as 16,384 words by 1 bit and designed with noninverted, open-emitter outputs and low power consumption. Two versions with fast access times of 10 ns and 15 ns maximum are available. The μPB100480 is packaged in a hermetic, 300-mil, 20-pin cerdip or 20-pin ceramic flatpack.

Features

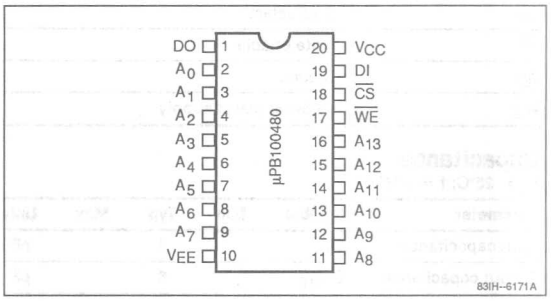
- 16,384-word x 1-bit organization
- 100K ECL interface with full voltage and temperature compensation
- Noninverted, open-emitter outputs
- Fast access times of 10 and 15 ns maximum
- Low power consumption
- 300-mil, 20-pin cerdip or 20-pin ceramic flatpack packaging

Ordering Information

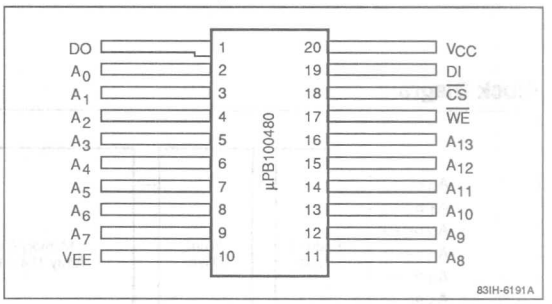
Part Number	Access Time (max)	Power Consumption (max)	Package
μPB100480D-10	10 ns	1.2 W	20-pin cerdip
D-15	15 ns	1.1 W	
μPB100480B-10	10 ns	1.2 W	20-pin ceramic flatpack
B-15	15 ns	1.1 W	

Pin Configurations

20-Pin Cerdip



20-Pin Ceramic Flatpack



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Pin Identification

Symbol	Function
A_0 - A_{13}	Address inputs
DI	Data input
DO	Data output
$\overline{CS}$	Chip select
$\overline{WE}$	Write enable
V_{CC}	Ground
V_{EE}	−4.5-volt power supply

Capacitance

T_A = 25°C; f = 1 MHz

Parameter	Symbol	Min	Typ	Max	Unit
Input capacitance	C_{IN}		4		pF
Output capacitance	C_{OUT}		6		pF

Absolute Maximum Ratings

Supply voltage, V_{EE}	−7.0 to +0.5 V
Input voltage, V_{IN}	V_{EE} to +0.5 V
Output current, I_{OUT}	−30 to +0.1 mA
Storage temperature, T_{STG}	−65 to +150°C
Storage temperature under bias, T_{STG} (bias)	−55 to +125°C

Exposure to Absolute Maximum Ratings for extended periods may affect device reliability; exceeding the ratings could cause permanent damage. The device should be operated within the limits specified under DC and AC Characteristics.

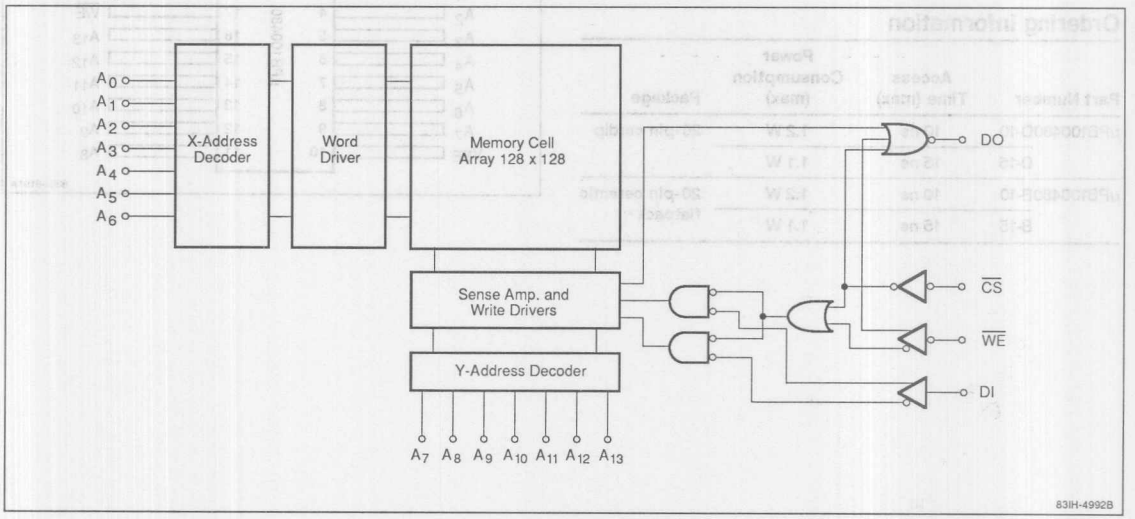
Truth Table

$\overline{CS}$	$\overline{WE}$	D_{IN}	Output	Mode
H	X	X	L	Not selected
L	L	L	L	Write 0
L	L	H	L	Write 1
L	H	X	D_{OUT}	Read

Notes:

(1) X = don't care.

Block Diagram



DC Characteristics

T_A = 0 to +85°C; V_{EE} = −4.5 V; output load = 50 Ω to −2.0 V; V_{CC} = 0 V

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions
Output voltage, high	V_{OH}	−1025		−880	mV	V_{IN} = V_{IH} max or V_{IL} min
Output voltage, low	V_{OL}	−1810		−1620	mV	V_{IN} = V_{IH} max or V_{IL} min
Output threshold voltage, high	V_{OHC}	−1035			mV	V_{IN} = V_{IH} min or V_{IL} max
Output threshold voltage, low	V_{OLC}			−1610	mV	V_{IN} = V_{IH} min or V_{IL} max
Input voltage, high	V_{IH}	−1165		−880	mV	Guaranteed input voltage high for all inputs
Input voltage, low	V_{IL}	−1810		−1475	mV	Guaranteed input voltage low for all inputs
Input current, high	I_{IH}			220	μA	V_{IN} = V_{IH} max
Input current, low	I_{IL}	0.5		170	μA	For $\overline{CS}$: V_{IN} = V_{IL} min
		−50			μA	For all others: V_{IN} = V_{IL} min
Supply current	I_{EE}	−260			mA	For μPB100480-10: all inputs and outputs open
		−240			mA	For μPB100480-15: all inputs and outputs open

Notes:

(1) The device under test is mounted in a test socket and measured at a thermal equilibrium established with a transverse air flow maintained at greater than 2.0 m/s.

AC Characteristics

T_A = 0 to +85°C; V_{EE} = −4.5 V ±5%

		μPB100480-10			μPB100480-15				
Parameter	Symbol	Min	Typ	Max	Min	Typ	Max	Unit	Test Conditions
Read Operation									
Address access time	t_{AA}			10			15	ns	
Chip select recovery time	t_{RCS}			5			8	ns	
Chip select access time	t_{ACS}			5			8	ns	
Write Operation									
Write pulse width	t_W	10			15			ns	
Data setup time	t_{WSD}	2			3			ns	
Data hold time	t_{WHD}	1			2			ns	
Address setup time	t_{WSA}	2			3			ns	
Address hold time	t_{WHA}	1			2			ns	
Chip select setup time	t_{WSCS}	2			3			ns	
Chip select hold time	t_{WHCS}	1			2			ns	
Write disable time	t_{WS}			5			8	ns	
Write recovery time	t_{WR}			11			17	ns	
Output Rise and Fall Times									
Output rise time	t_R		2			2		ns	
Output fall time	t_F		2			2		ns	

Notes:

(1) The device under test is mounted in a test socket and measured at a thermal equilibrium established with a transverse air flow maintained at greater than 2.0 m/s.

(2) Input pulse levels = −1.7 to −0.9 V; input rise and fall times (measured between 20% and 80% or 80% to 20%) = 2.5 ns; input and output timing reference level = 50%.

8

Figure 1. Loading Conditions Test Circuit

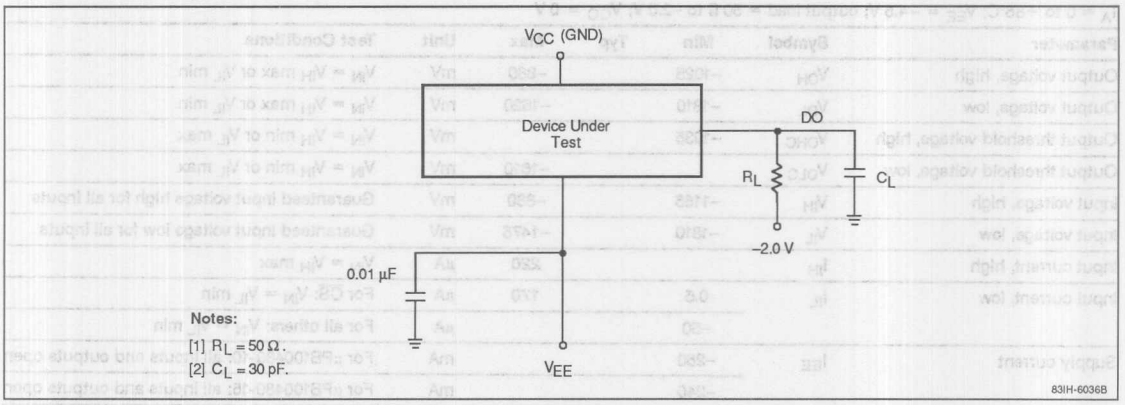
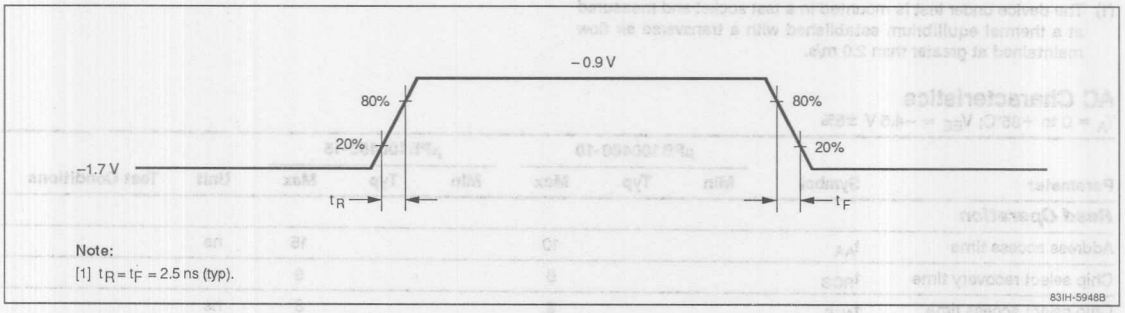
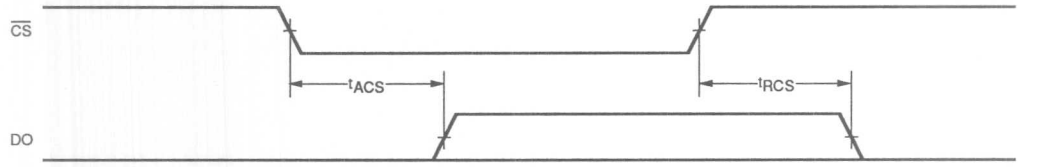


Figure 2. Input Pulse



Timing Waveforms

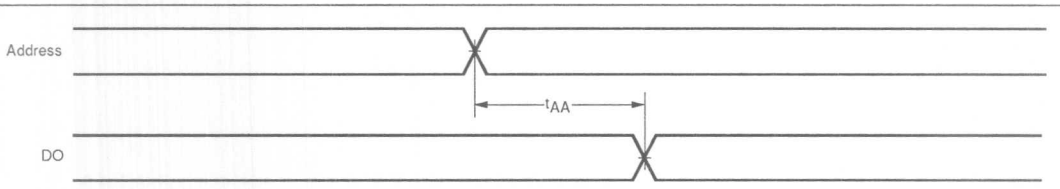
Chip Select Access Cycle



Note:
[1] Address is valid more than 2 ns prior to the low transition of $\overline{CS}$.

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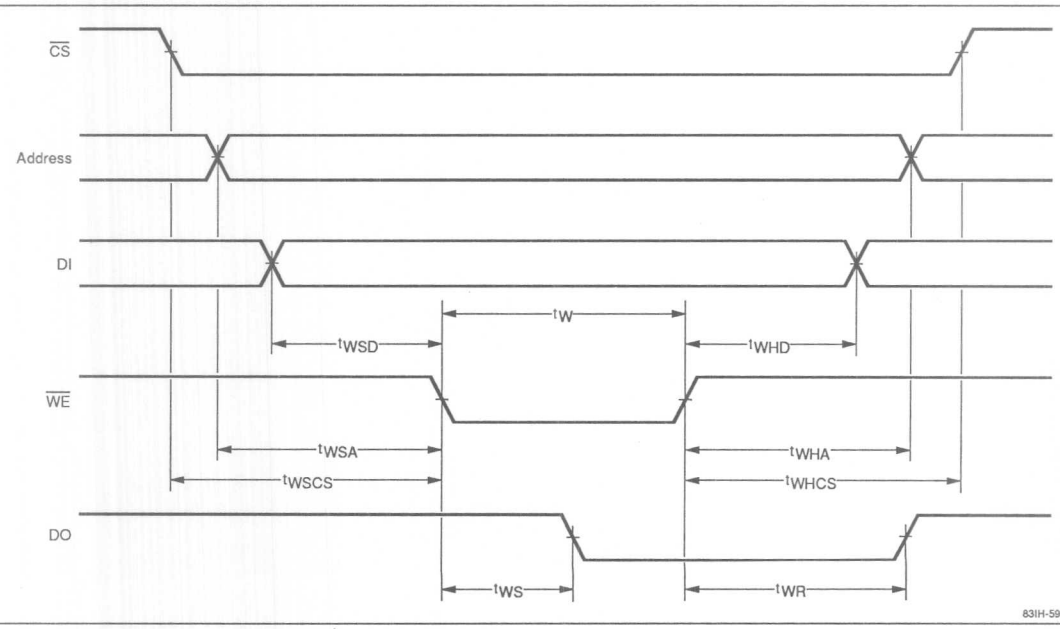
Address Access Cycle



Note:
[1] $\overline{CS} = V_{IL}$

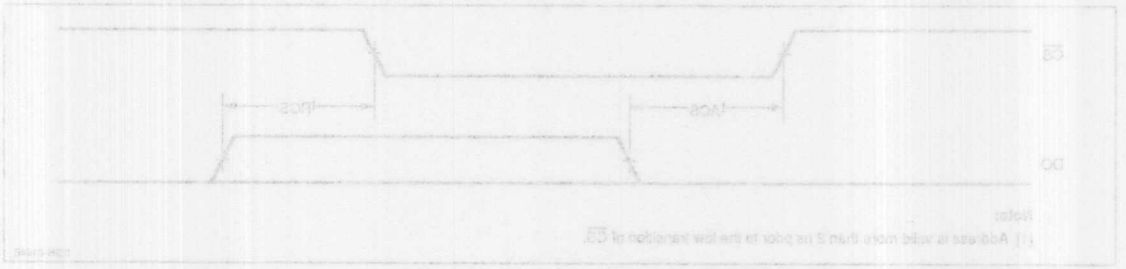
83IH-5954B

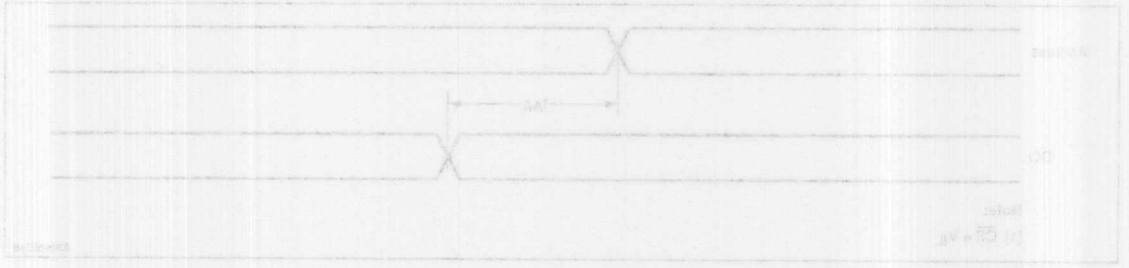
Write Cycle

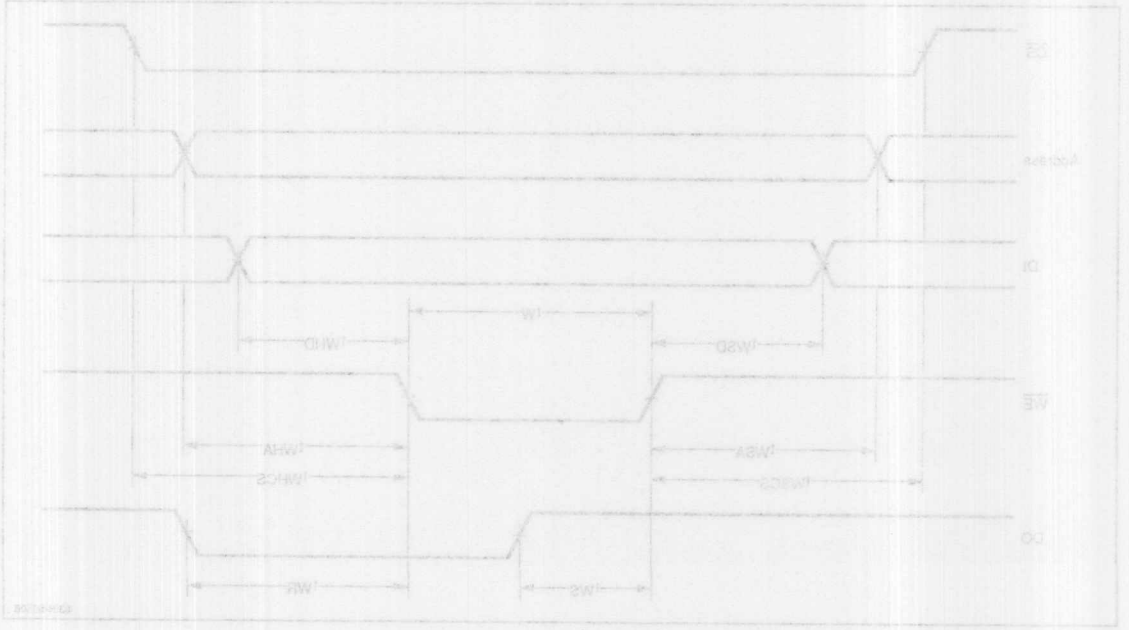


83IH-5950B

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Description

The μPB100484 is a very high-speed 100K interface ECL RAM organized as 4,096 words by 4 bits with open-emitter outputs (noninverted). It is available in 28-pin cerdip or flatpack packages.

Features

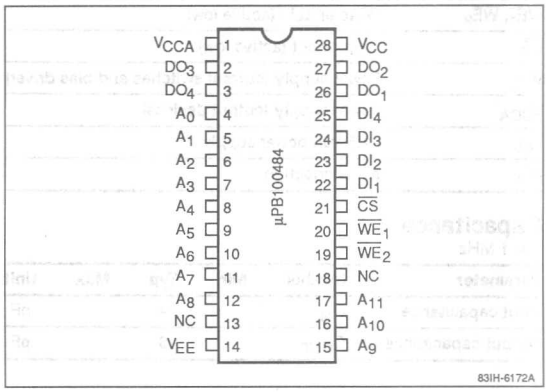
- 4,096-word x 4-bit organization
- 100K ECL interface
- Full voltage and temperature compensation
- Open-emitter outputs (noninverted)
- Fast access times and low power consumption
- 28-pin cerdip and 28-pin flatpack packaging

Ordering Information

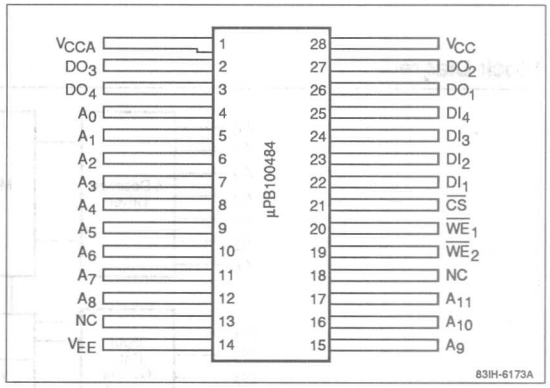
Part Number	Access Time (max)	Supply Current (min)	Package
μPB100484D-10	10 ns	–260 mA	28-pin cerdip
D-15	15 ns	–240 mA	
μPB100484B-10	10 ns	–260 mA	28-pin ceramic flatpack
B-15	15 ns	–240 mA	

Pin Configurations

28-Pin Cerdip



28-Pin Ceramic Flatpack



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Pin Identification

Symbol	Function
A_0 - A_{11}	Address inputs
DI_1 - DI_4	Data inputs
DO_1 - DO_4	Data outputs
$\overline{WE}_1$, $\overline{WE}_2$	Write enable (active low)
$\overline{CS}$	Chip select (active low)
V_{CC}	Power supply (current switches and bias driver)
V_{CCA}	Power supply (output devices)
V_{EE}	–4.5-volt power supply
NC	No connection

Capacitance

f = 1 MHz

Parameter	Symbol	Min	Typ	Max	Unit
Input capacitance	C_{IN}		4		pF
Output capacitance	C_{OUT}		6		pF

Absolute Maximum Ratings

$V_{CC} = V_{CCA} = 0$ V

Supply voltage, V_{EE}	–7.0 to +0.5 V
Input voltage, V_{IN}	V_{EE} to +0.5 V
Output current, I_{OUT}	–30 to +0.1 mA
Storage temperature, T_{STG}	–65 to +150°C
Storage temperature under bias, T_{STG} (bias)	–55 to +125°C

Exposure to Absolute Maximum Ratings for extended periods may affect device reliability; exceeding the ratings could cause permanent damage. The device should be operated within the limits specified under DC and AC Characteristics.

Truth Table

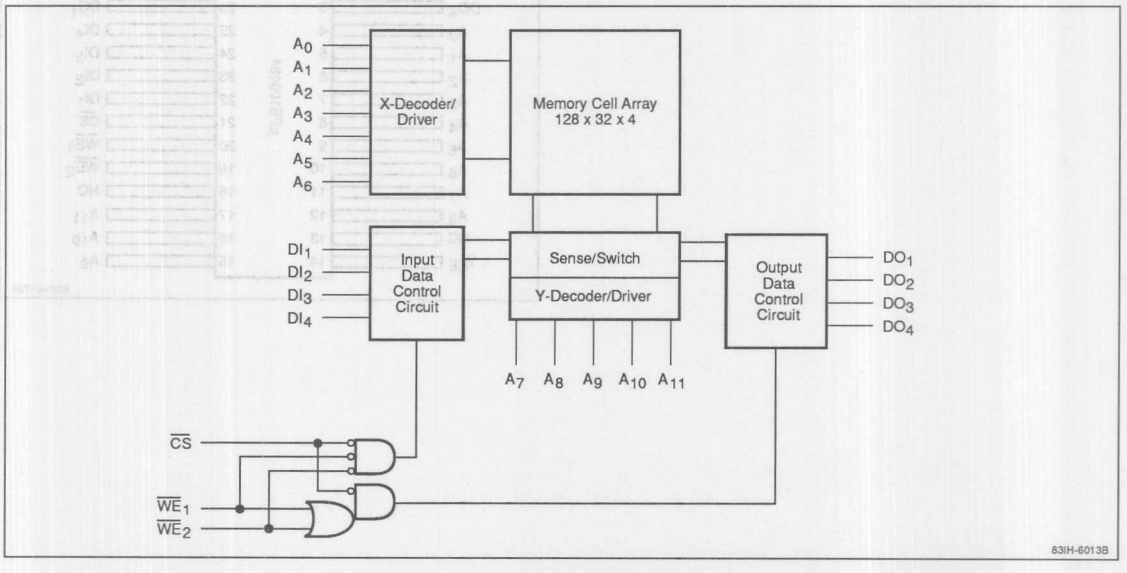
$\overline{CS}$	$\overline{WE}$	D_{IN}	Output	Mode
H	X	X	L	Not selected
L	L (Note 2)	L	L	Write 0
L	L (Note 2)	H	L	Write 1
L	H (Note 2)	X	D_{OUT}	Read

Notes:

(1) X = don't care.

(2) Both $\overline{WE}_1$ and $\overline{WE}_2$ must be low to initiate write operation. For read operation, either $\overline{WE}_1$ or $\overline{WE}_2$ or both must be high.

Block Diagram



DC Characteristics

T_A = 0 to +85°C; V_{EE} = −4.5 V; output load = 50 Ω to −2.0 V; V_{CC} = V_{CCA} = 0 V

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions
Output voltage, high	V_{OH}	−1025		−880	mV	V_{IN} = V_{IH} max or V_{IL} min
Output voltage, low	V_{OL}	−1810		−1620	mV	V_{IN} = V_{IH} max or V_{IL} min
Output threshold voltage, high	V_{OHC}	−1035			mV	V_{IN} = V_{IH} min or V_{IL} max
Output threshold voltage, low	V_{OLC}			−1610	mV	V_{IN} = V_{IH} min or V_{IL} max
Input voltage, high	V_{IH}	−1165		−880	mV	
Input voltage, low	V_{IL}	−1810		−1475	mV	
Input current, high	I_{IH}			220	μA	V_{IN} = V_{IH} max
Input current, low	I_{IL}	0.5		170	μA	For $\overline{CS}$: V_{IN} = V_{IL} min
		−50			μA	For all others: V_{IN} = V_{IL} min
Supply current	I_{EE}	−260			mA	For μPB100484-10: all inputs and outputs open
		−240			mA	For μPB100484-15: all inputs and outputs open

Notes:

(1) The device under test is mounted in a test socket and measured at a thermal equilibrium established with a transverse air flow maintained at greater than 2.0 m/s.

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AC Characteristics

T_A = 0 to +85°C; V_{EE} = −4.5 V ±5%; output load = 50 Ω to −2.0 V; V_{CC} = V_{CCA} = 0 V

		μPB100484-10			μPB100484-15				
Parameter	**Symbol**	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**	**Unit**	**Test Conditions**
Read Operation									
Address access time	t_{AA}			10			15	ns	
Chip select recovery time	t_{RCS}			5			8	ns	
Chip select access time	t_{ACS}			5			8	ns	
Write Operation									
Write pulse width	t_W	10			15			ns	
Data setup time	t_{WSD}	2			3			ns	
Data hold time	t_{WHD}	1			2			ns	
Address setup time	t_{WSA}	2			3			ns	
Address hold time	t_{WHA}	1			2			ns	
Chip select setup time	t_{WSCS}	2			3			ns	
Chip select hold time	t_{WHCS}	1			2			ns	
Write disable time	t_{WS}			5			8	ns	
Write recovery time	t_{WR}			11			17	ns	
Output Rise and Fall Times									
Output rise time	t_R		2			2		ns	
Output fall time	t_F		2			2		ns	

Notes:

(1) The device under test is mounted in a test socket and measured at a thermal equilibrium established with a transverse air flow maintained at greater than 2.0 m/s.

(2) See figure 1 and 2 for loading conditions and input pulse timing. Input pulse levels = −1.7 to −0.9 V; input rise and fall times = 2.5 ns; input and output timing reference levels = 50%.

Figure 1. Loading Conditions Test Circuit

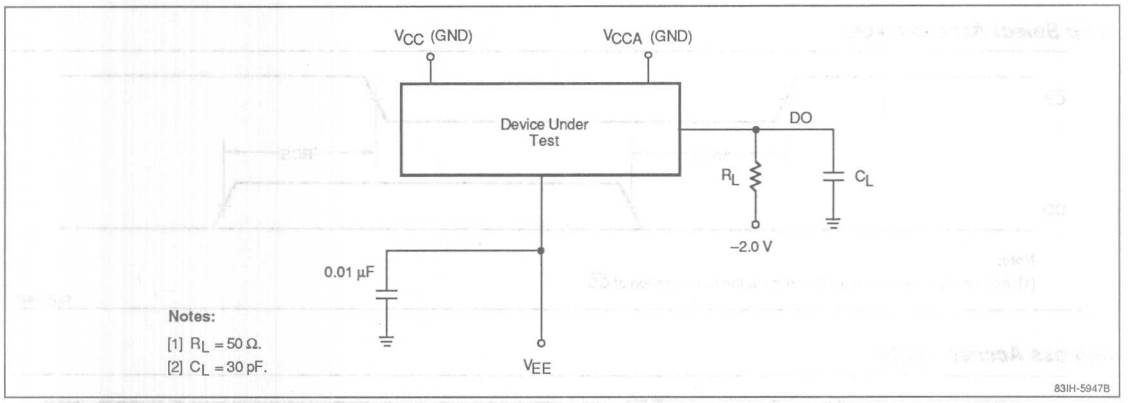
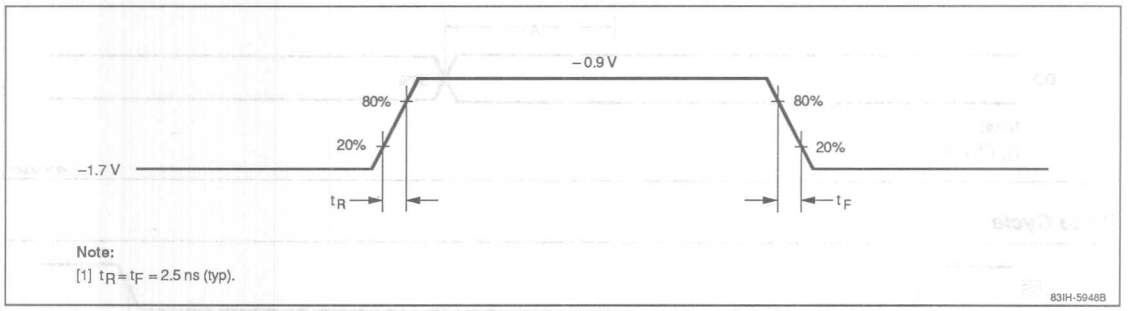


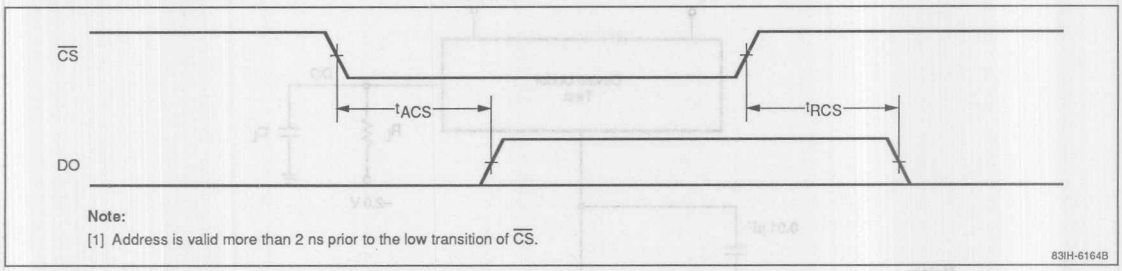
Figure 2. Input Pulse



8

Timing Waveforms

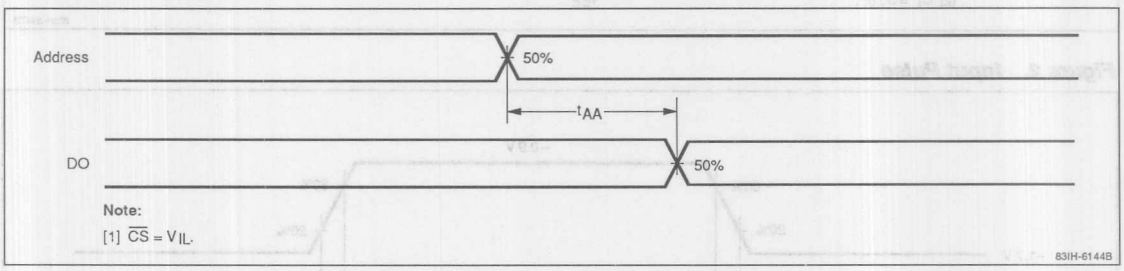
Chip Select Access Cycle



Note:
[1] Address is valid more than 2 ns prior to the low transition of $\overline{CS}$.

83IH-6164B

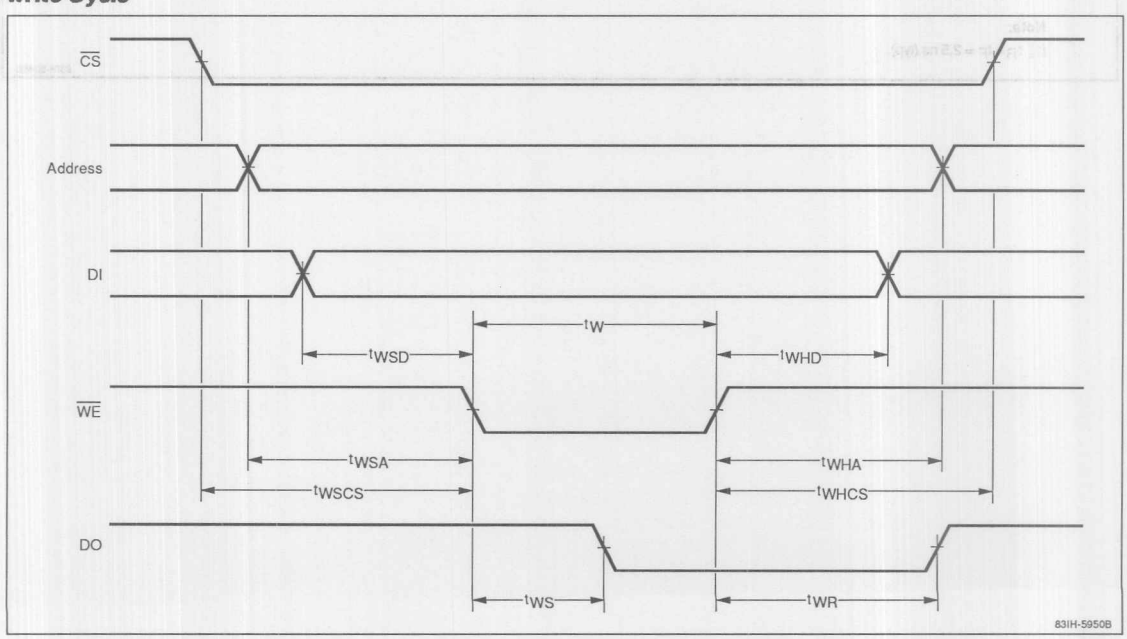
Address Access Cycle



Note:
[1] $\overline{CS} = V_{IL}$.

83IH-6144B

Write Cycle



83IH-5950B

NEC Electronics Inc.

μPB100484A
4,096 x 4-BIT
100K ECL RAM

PRELIMINARY INFORMATION

Description

The μPB100484A is a very high-speed 100K interface ECL RAM. It is organized as 4,096 words by 4 bits with noninverted, open-emitter outputs and low power consumption. Two access time versions are available: 5 ns and 7 ns maximum. The μPB100484A is available in a hermetic, 400-mil, 28-pin cerdip or 28-pin ceramic flatpack.

Features

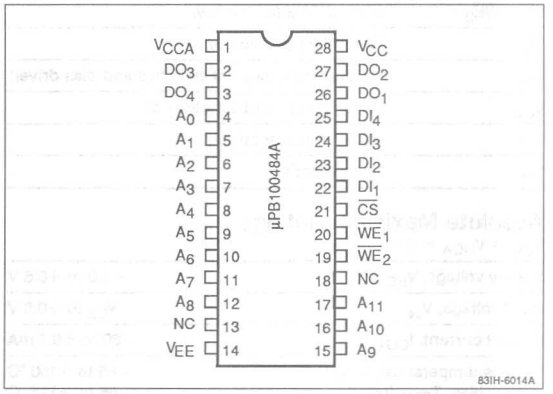
- 4,096-word x 4-bit organization
- 100K ECL interface
- Full voltage and temperature compensation
- Noninverted, open-emitter outputs
- Fast access times: 5 and 7 ns maximum
- Low power consumption
- 400-mil, 28-pin cerdip or 28-pin ceramic flatpack packaging

Ordering Information

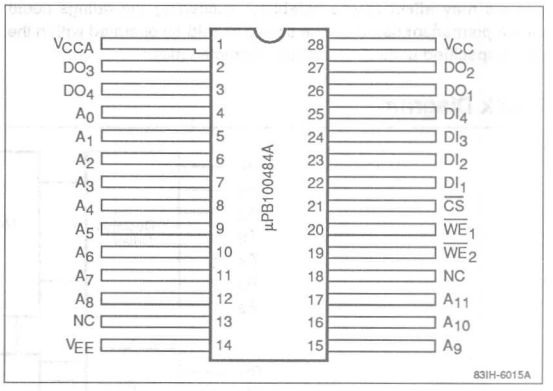
Part Number	Access Time (max)	Supply current (min)	Package
μPB100484AB-5	5 ns	−260 mA	28-pin ceramic flatpack
B-7	7 ns	−240 mA	
μPB100484AD-5	5 ns	−260 mA	28-pin cerdip
D-7	7 ns	−240 mA	

Pin Configurations

28-Pin Cerdip



28-Pin Ceramic Flatpack



8

Pin Identification

Symbol	Function
A_0 - A_{11}	Address inputs
DI_1 - DI_4	Data inputs
DO_1 - DO_4	Data outputs
$\overline{WE}_1$, $\overline{WE}_2$	Write enable (active low)
$\overline{CS}$	Chip select (active low)
V_{CC}	Power supply (current switches and bias driver)
V_{CCA}	Power supply (output devices)
V_{EE}	– 4.5-volt power supply
NC	No connection

Absolute Maximum Ratings

$V_{CC} = V_{CCA} = 0$ V

Supply voltage, V_{EE}	– 7.0 to +0.5 V
Input voltage, V_{IN}	V_{EE} to +0.5 V
Output current, I_{OUT}	– 30 to +0.1 mA
Storage temperature, T_{STG}	– 65 to +150 °C
Under bias, T_{STG} (bias)	– 55 to +125 °C

Comment: Exposure to Absolute Maximum Ratings for extended periods may affect device reliability; exceeding the ratings could cause permanent damage. The device should be operated within the limits specified under DC and AC Characteristics.

Capacitance

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions
Input capacitance	C_{IN}		4		pF	
Output capacitance	C_{OUT}		6		pF	

Truth Table

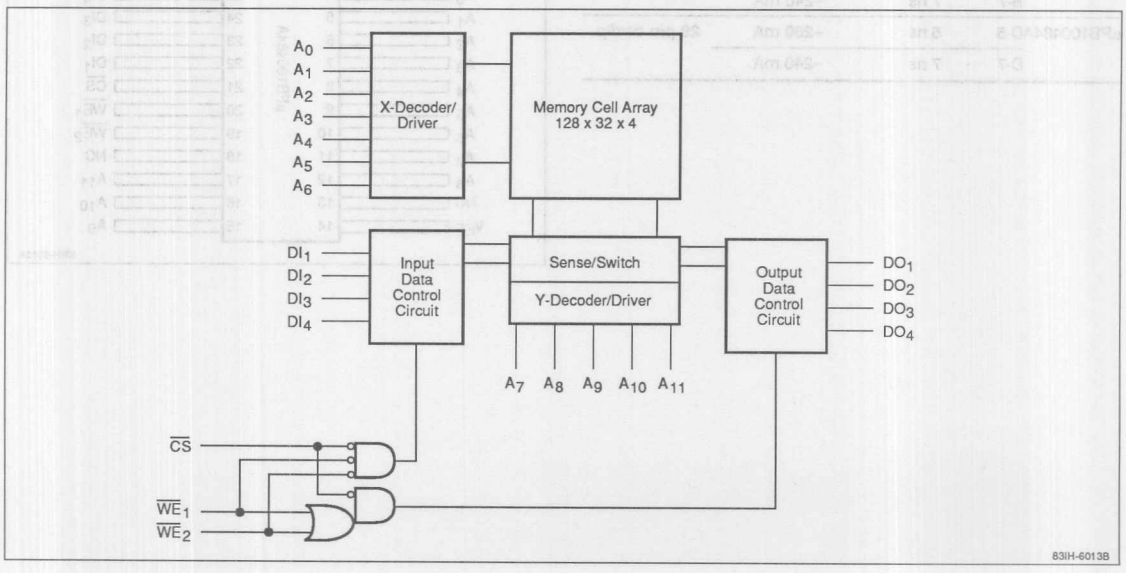
$\overline{CS}$	$\overline{WE}$	D_{IN}	Output	Function
H	X	X	L	Not selected
L	L (Note 2)	L	L	Write 0
L	L (Note 2)	H	L	Write 1
L	H (Note 2)	X	D_{OUT}	Read

Notes:

(1) X = don't care.

(2) Both $\overline{WE}_1$ and $\overline{WE}_2$ must be low to initiate write operation. For read operation, either $\overline{WE}_1$ or $\overline{WE}_2$ or both must be high.

Block Diagram



DC Characteristics

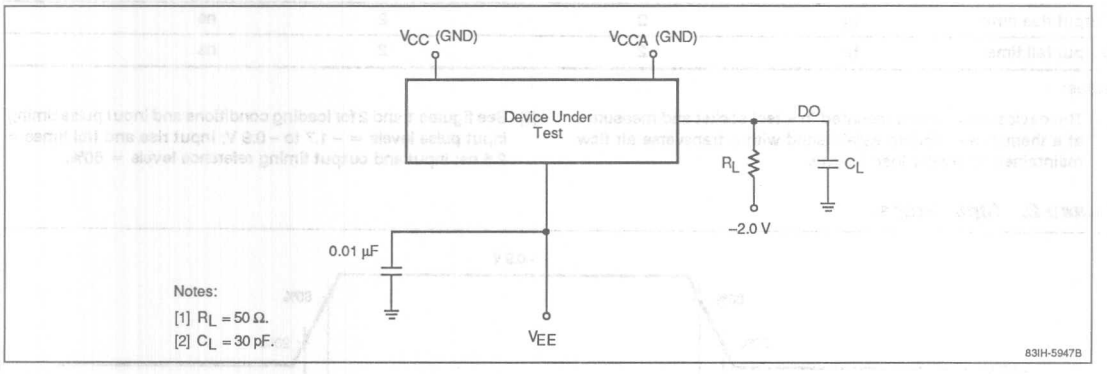
T_A = 0 to +85°C; V_{EE} = −4.5 V; output load = 50 Ω to −2.0 V; V_{CC} = V_{CCA} = 0 V

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions
Output voltage, high	V_{OH}	−1025		−880	mV	V_{IN} = V_{IH} max or V_{IL} min
Output voltage, low	V_{OL}	−1810		−1620	mV	V_{IN} = V_{IH} max or V_{IL} min
Output threshold voltage, high	V_{OHC}	−1035			mV	V_{IN} = V_{IH} min or V_{IL} max
Output threshold voltage, low	V_{OLC}			−1610	mV	V_{IN} = V_{IH} min or V_{IL} max
Input voltage, high	V_{IH}	−1165		−880	mV	
Input voltage, low	V_{IL}	−1810		−1475	mV	
Input current, high	I_{IH}			220	μA	V_{IN} = V_{IH} max
Input current, low	I_{IL}	0.5		170	μA	For $\overline{CS}$: V_{IN} = V_{IL} min
		−50			μA	For all others: V_{IN} = V_{IL} min
Supply current	I_{EE}	−260			mA	For μPB100484A-5: All inputs and outputs open
		−240			mA	For μPB100484A-7: All inputs and outputs open

Notes:

(1) The device under test is mounted in a test socket and measured at a thermal equilibrium established with a transverse air flow maintained at greater than 2.0 m/s.

Figure 1. Loading Conditions Test Circuit



8

AC Characteristics

T_A = 0 to +85°C; V_{EE} = −4.5 V ± 5%; output load = 50 Ω to −2.0 V; V_{CC} = V_{CCA} = 0 V

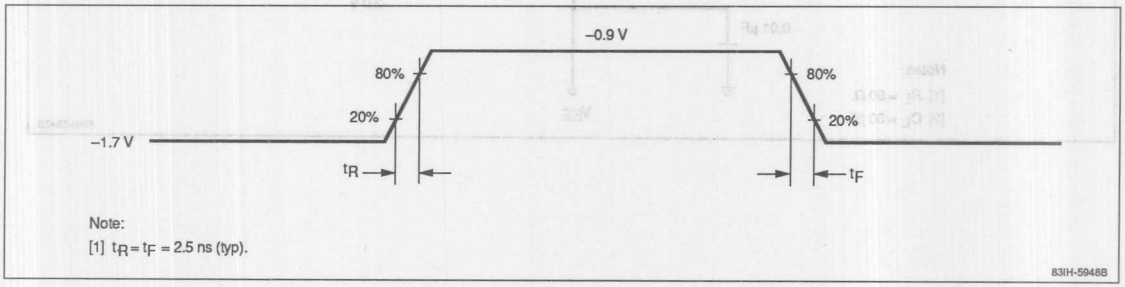
		μPB100484A-5			μPB100484A-7				
Parameter	**Symbol**	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**	**Unit**	**Test Conditions**
Read Operation									
Address access time	t_{AA}			5			7	ns	
Chip select recovery time	t_{RCS}			3.5			4	ns	
Chip select access time	t_{ACS}			3.5			4	ns	
Write Operation									
Write pulse width	t_W	6			8			ns	
Data setup time	t_{WSD}	1			1			ns	
Data hold time	t_{WHD}	2			2			ns	
Address setup time	t_{WSA}	1			1			ns	
Address hold time	t_{WHA}	2			2			ns	
Chip select setup time	t_{WSCS}	1			1			ns	
Chip select hold time	t_{WHCS}	2			2			ns	
Write disable time	t_{WS}			3.5			5	ns	
Write recovery time	t_{WR}			7			9	ns	
Output Rise and Fall Times									
Output rise time	t_R		2			2		ns	
Output fall time	t_F		2			2		ns	

Notes:

(1) The device under test is mounted in a test socket and measured at a thermal equilibrium established with a transverse air flow maintained at greater than 2.0 m/s.

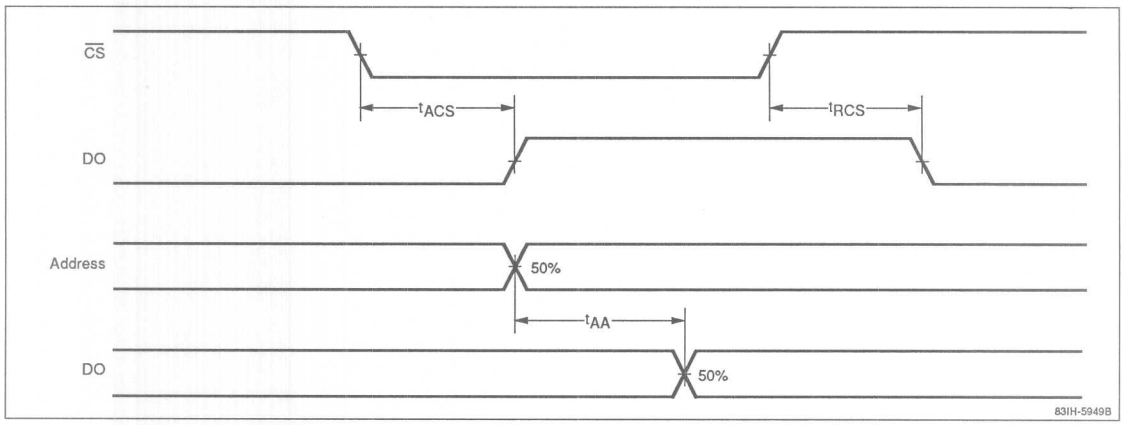
(2) See figures 1 and 2 for loading conditions and input pulse timing. Input pulse levels = −1.7 to −0.9 V; input rise and fall times = 2.5 ns; input and output timing reference levels = 50%.

Figure 2. Input Pulse

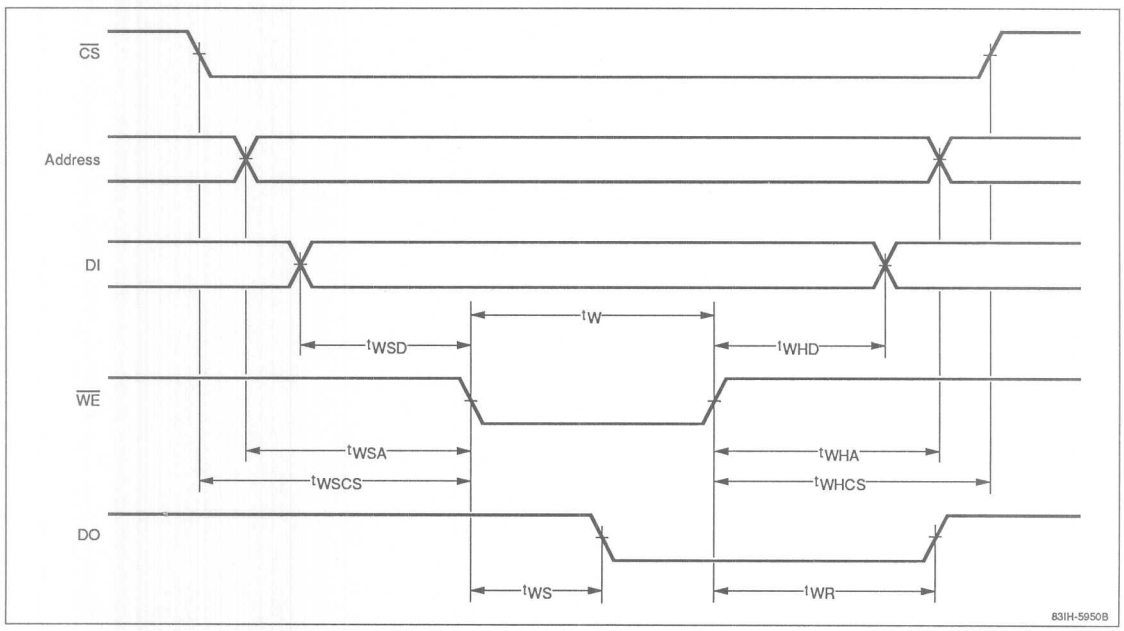


Timing Waveforms

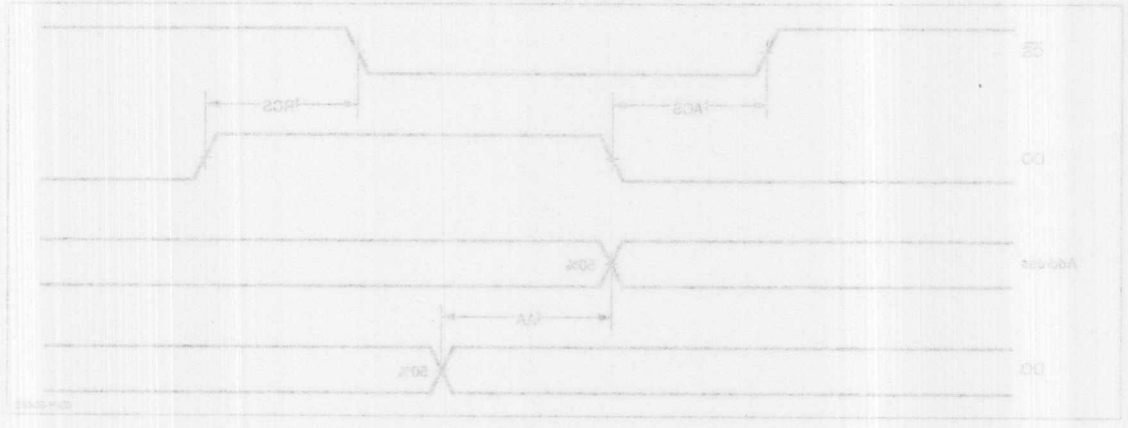
Read Cycle

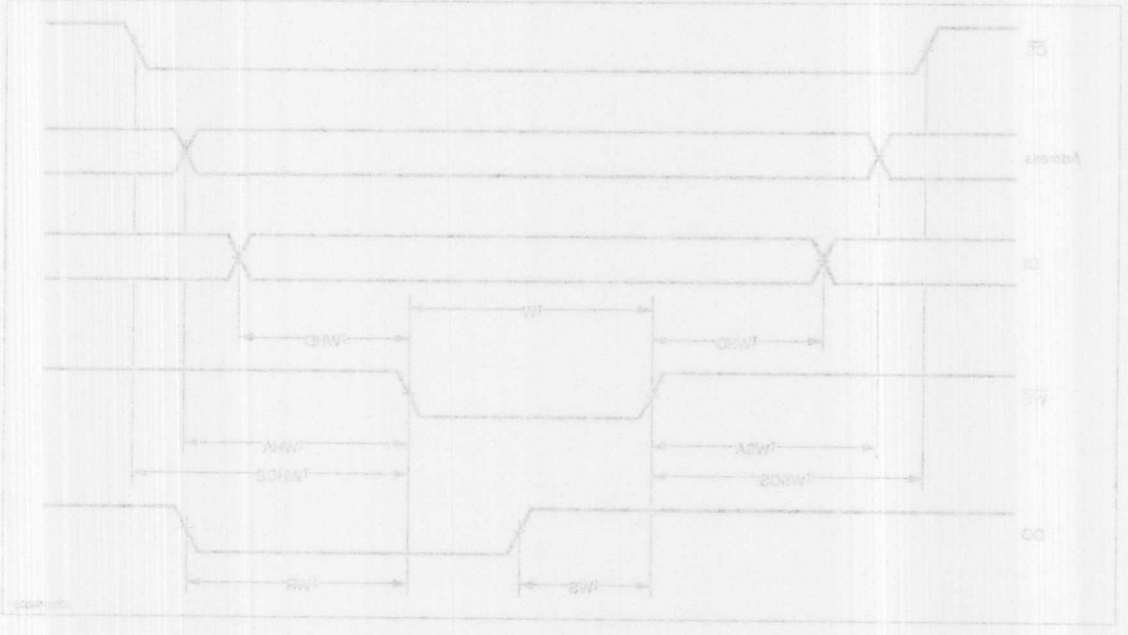


Write Cycle



8





μPB100A484
4,096 x 4-Bit
100K ECL RAM

PRELIMINARY INFORMATION

Description

The μPB100A484 is a very high-speed 100K interface ECL RAM organized as 4K words by 4 bits and designed with open emitter outputs (noninverted). It is available in 28-pin cerdip or flatpack packages.

Features

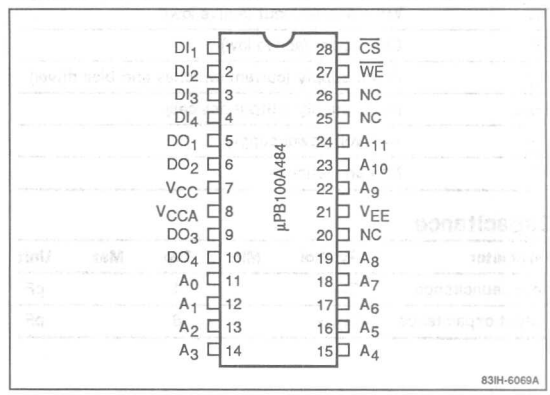
- 4096 word x 4-bit organization
- 100K ECL interface
- Full voltage and temperature compensation
- Open emitter outputs (noninverted)
- Fast access times and low power consumption
- 28-pin cerdip and flatpack packaging
- Center power pins

Ordering Information

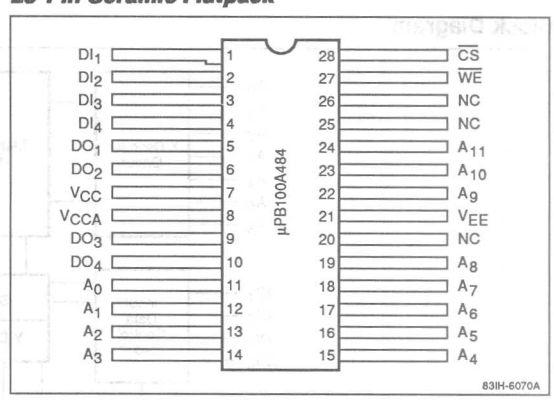
Part Number	Access Time (max)	Supply Current (min)	Package
μPB100A484B-5	5 ns	TBD	28-pin ceramic flatpack
B-7	7 ns	TBD	
μPB100A484D-5	5 ns	TBD	28-pin cerdip
D-7	7 ns	TBD	

Pin Configurations

28-Pin Cerdip



28-Pin Ceramic Flatpack



8

Pin Identification

Symbol	Function
A_0 - A_{11}	Address inputs
DI_1 - DI_4	Data inputs
DO_1 - DO_4	Data outputs
$\overline{WE}$	Write enable input (active low)
$\overline{CS}$	Chip select (active low)
V_{CC}	Power supply (current switches and bias driver)
V_{CCA}	Power supply (output devices)
V_{EE}	–4.5-volt power supply
NC	No connection

Capacitance

Parameter	Symbol	Min	Typ	Max	Unit
Input capacitance	C_{IN}		4		pF
Output capacitance	C_{OUT}		6		pF

Truth Table

$\overline{CS}$	$\overline{WE}$	D_{IN}	Output	Function
H	X	X	L	Not selected
L	L	L	L	Write 0
L	L	H	L	Write 1
L	H	X	D_{OUT}	Read

Notes:

(1) X = don't care.

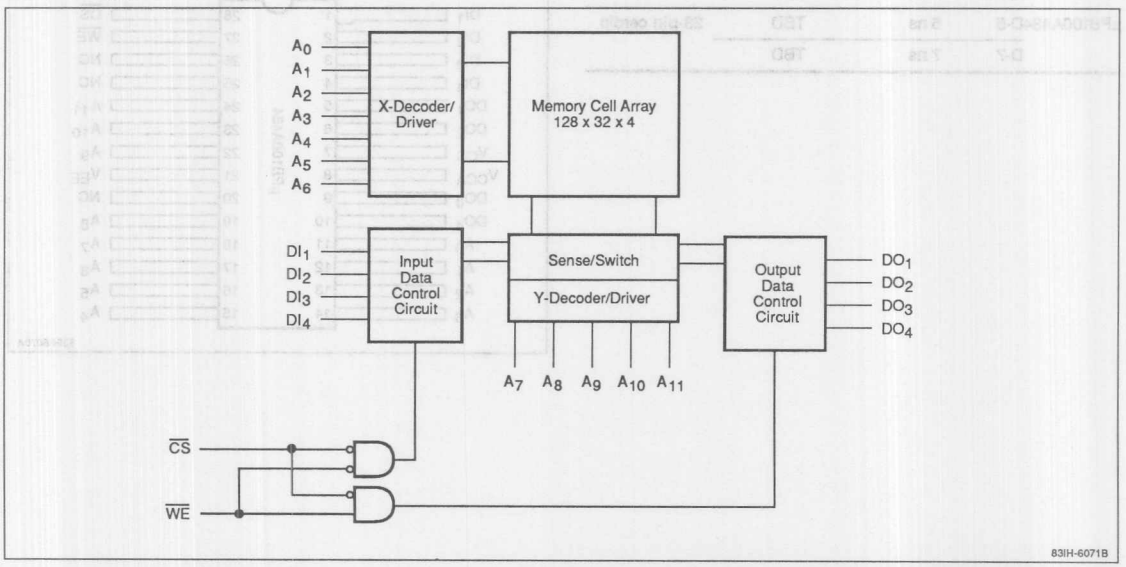
Absolute Maximum Ratings

$V_{CC} = V_{CCA} = 0$ V

Supply voltage, V_{EE}	–7.0 to +0.5 V
Input voltage, V_{IN}	V_{EE} to +0.5 V
Output current, I_{OUT}	–30 to +0.1 mA
Storage temperature, T_{STG}	–65 to +150°C
Storage temperature under bias, T_{STG} (Bias)	–55 to +125°C

Exposure to Absolute Maximum Ratings for extended periods may affect device reliability; exceeding the ratings could cause permanent damage. The device should be operated within the limits specified under DC and AC Characteristics.

Block Diagram



DC Characteristics

T_A = 0 to +85°C; V_{EE} = −4.5 V; output load = 50 Ω to −2.0 V; V_{CC} = V_{CCA} = 0 V

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions
Output voltage, high	V_{OH}	−1025		−880	mV	V_{IN} = V_{IH} (max) or V_{IL} (min)
Output voltage, low	V_{OL}	−1810		−1620	mV	V_{IN} = V_{IH} (max) or V_{IL} (min)
Output threshold voltage, high	V_{OHC}	−1035			mV	V_{IN} = V_{IH} (min) or V_{IL} (max)
Output threshold voltage, low	V_{OLC}			−1610	mV	V_{IN} = V_{IH} (min) or V_{IL} (max)
Input voltage, high	V_{IH}	−1165		−880	mV	
Input voltage, low	V_{IL}	−1810		−1475	mV	
Input current, high	I_{IH}			220	μA	V_{IN} = V_{IH} (max)
Input current, low	I_{IL}	0.5		170	μA	For $\overline{CS}$: V_{IN} = V_{IL} (min)
		−50			μA	For all others: V_{IN} = V_{IL} (min)
Supply current	I_{EE}	TBD			mA	μPB100A484-5: all inputs and outputs open
		TBD			mA	μPB100A484-7: all inputs and outputs open

Notes:

(1) The device under test is mounted in a test socket and measured at a thermal equilibrium established with a transverse air flow maintained at greater than 2.0 m/sec.

AC Characteristics

T_A = 0 to +85°C; V_{EE} = −4.5 V ±5%; output load = 50 Ω to −2.0 V; V_{CC} = V_{CCA} = 0 V

		μPB100A484-5			μPB100A484-7				
Parameter	Symbol	Min	Typ	Max	Min	Typ	Max	Unit	Test Conditions
Read Operation									
Address access time	t_{AA}			5			7	ns	
Chip select recovery time	t_{RCS}			3.5			4	ns	
Chip select access time	t_{ACS}			3.5			4	ns	
Write Operation									
Write pulse width	t_W	6			8			ns	
Data setup time	t_{WSD}	1			1			ns	
Data hold time	t_{WHD}	2			2			ns	
Address setup time	t_{WSA}	1			1			ns	
Address hold time	t_{WHA}	2			2			ns	
Chip select setup time	t_{WSCS}	1			1			ns	
Chip select hold time	t_{WHCS}	2			2			ns	
Write disable time	t_{WS}			3.5			5	ns	
Write recovery time	t_{WR}			7			9	ns	
Output Rise and Fall Times									
Output rise time	t_R		2			2		ns	
Output fall time	t_F		2			2		ns	

Notes:

(1) The device under test is mounted in a test socket and measured at a thermal equilibrium established with a transverse air flow maintained at greater than 2.0 m/s.

(2) See figures 1 and 2 for loading conditions and input pulse timing. Input pulse levels = −1.7 to −0.9 V; input rise and fall times = 2.5 ns; input and output timing reference levels = 50%.

8

Figure 1. Loading Conditions Test Circuit

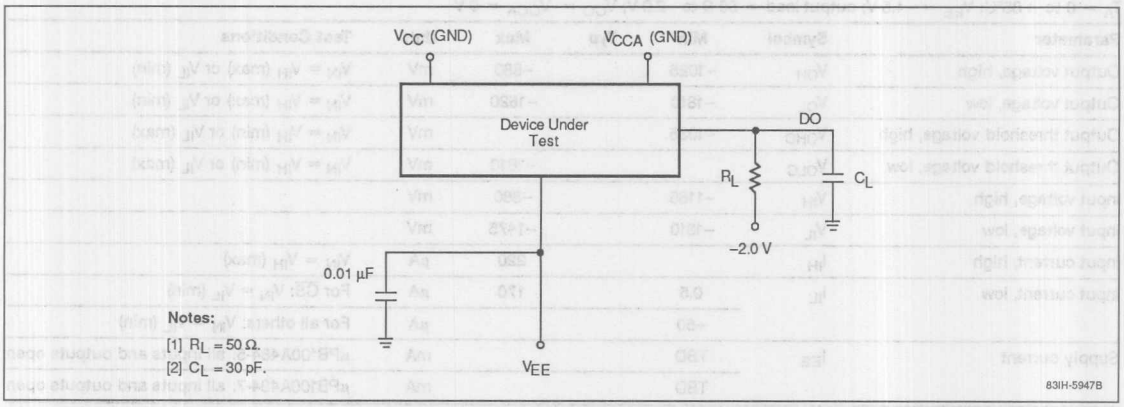
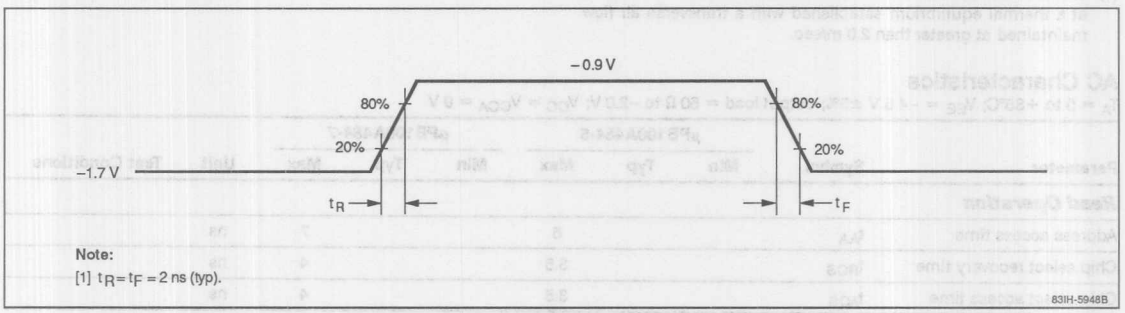
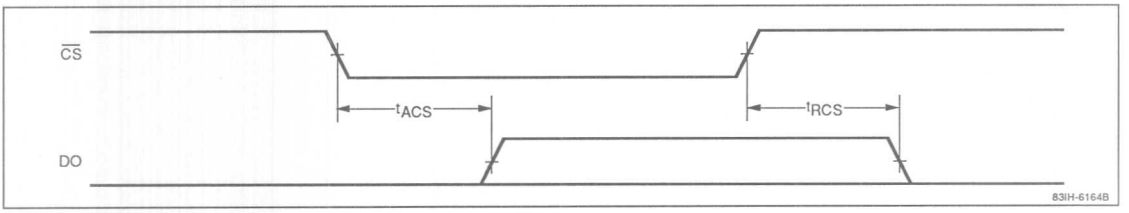


Figure 2. Input Pulse

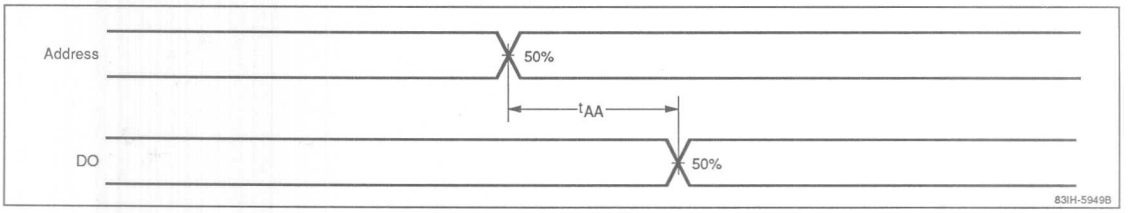


Timing Waveforms

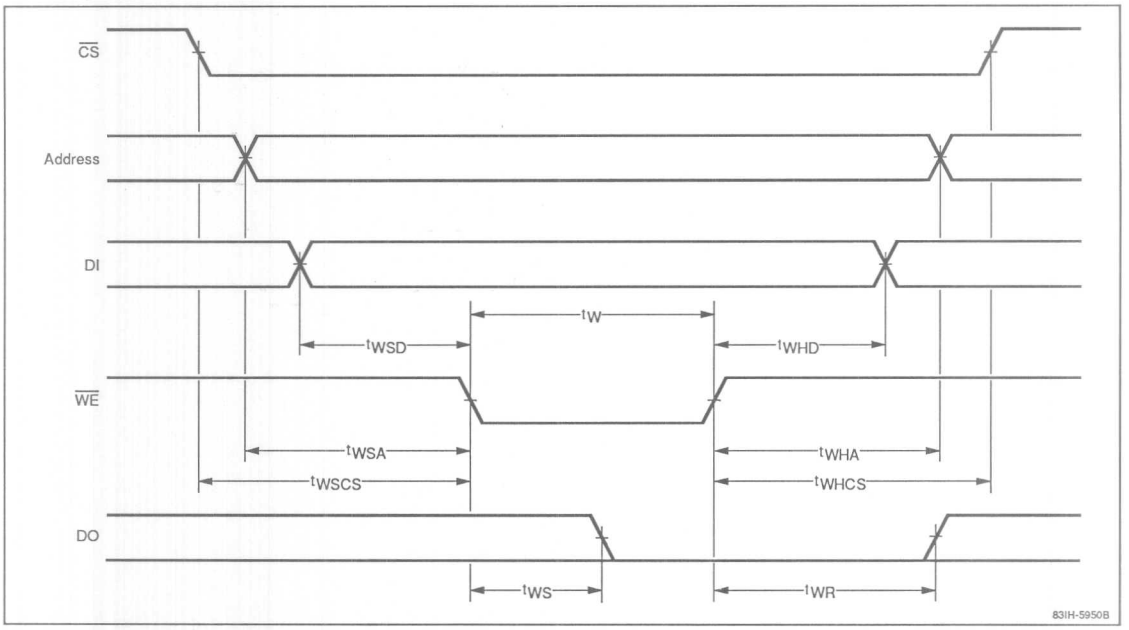
Chip Select Access Cycle



Address Access Cycle



Write Cycle



8

NEC Electronics Inc.

μPD100500
262,144 x 1-Bit
100K BiCMOS ECL RAM

PRELIMINARY INFORMATION

Description

The μPD100500 is a very high-speed BiCMOS RAM with full voltage and temperature compensation for a 100K ECL interface. Its unique design uses blended CMOS and bipolar peripheral circuits and N-channel MOS memory cells. The device is organized as 262,144 words by 1 bit and designed with an open-emitter output (noninverted) for low power consumption. Two versions with fast access times of 15 and 20 ns maximum are available in hermetic, 300-mil, 24-pin cerdip packaging.

Features

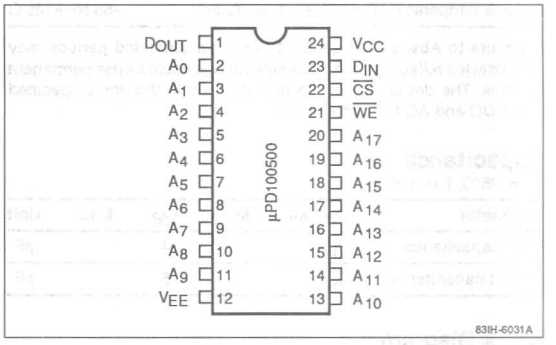
- BiCMOS technology
- 262,144-word x 1-bit organization
- 100K interface ECL with full voltage and temperature compensation
- Noninverted, open-emitter output
- Fast access times of 15 and 20 ns maximum
- Low power consumption
- 300-mil, 24-pin cerdip packaging

Ordering Information

Part Number	Access Time (max)	Power Consumption (max)	Package
μPD100500D-15	15 ns	720 mW	24-pin cerdip
D-20	20 ns		

Pin Configuration

24-Pin Cerdip



Pin Identification

Symbol	Function
A_0 - A_{17}	Address inputs
D_{IN}	Data input
D_{OUT}	Data output
$\overline{CS}$	Chip select
$\overline{WE}$	Write enable
V_{CC}	Ground
V_{EE}	−4.5-volt power supply

8

Absolute Maximum Ratings

Supply voltage, V_{EE}	−7.0 to +0.5 V
Input voltage, V_{IN}	V_{EE} to +0.5 V
Output current, I_{OUT}	−30 to +0.1 mA
Storage temperature, T_{STG}	−65 to +150°C
Storage temperature under bias, T_{STG} (bias)	−55 to +125°C

Exposure to Absolute Maximum Ratings for extended periods may affect device reliability; exceeding the ratings could cause permanent damage. The device should be operated within the limits specified under DC and AC Characteristics.

Capacitance

T_A = 25°C; f = 1 MHz

Parameter	Symbol	Min	Typ	Max	Unit
Input capacitance	C_{IN}		4		pF
Output capacitance	C_{OUT}		6		pF

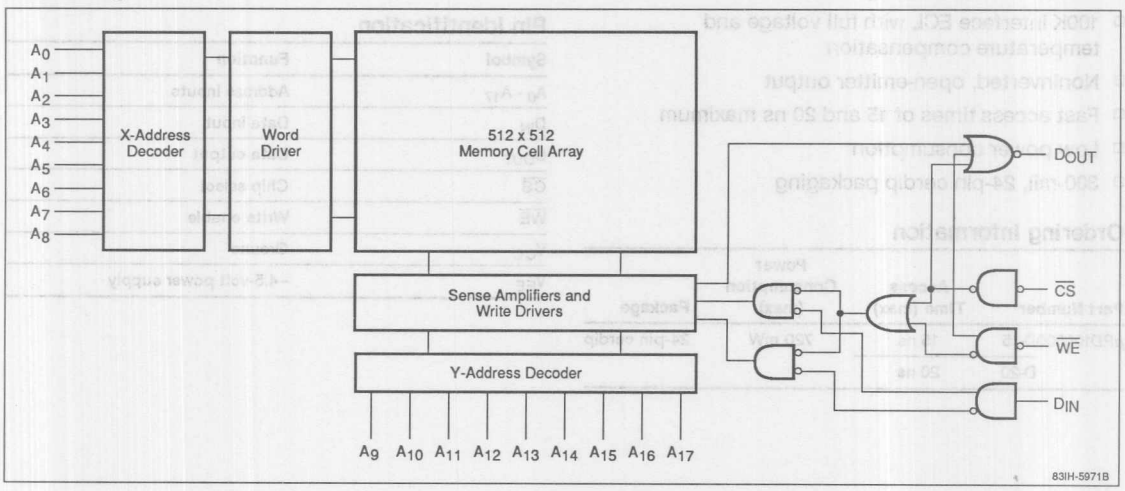
Truth Table

$\overline{CS}$	$\overline{WE}$	D_{IN}	Output	Mode
H	X	X	L	Not selected
L	L	L	L	Write 0
L	L	H	L	Write 1
L	H	X	D_{OUT}	Read

Notes:

(1) X = don't care.

Block Diagram



DC Characteristics

T_A = 0 to +85°C; V_{EE} = −4.5 V; output load = 50 Ω to −2.0 V; V_{CC} = 0 V

Parameter	Symbol	Min	Max	Unit	Test Conditions
Output voltage, high	V_{OH}	−1025	−880	mV	V_{IN} = V_{IH} max or V_{IL} min
Output voltage, low	V_{OL}	−1810	−1620	mV	V_{IN} = V_{IH} max or V_{IL} min
Output threshold voltage, high	V_{OHC}	−1035		mV	V_{IN} = V_{IH} min or V_{IL} max
Output threshold voltage, low	V_{OLC}		−1610	mV	V_{IN} = V_{IH} min or V_{IL} max
Input voltage, high	V_{IH}	−1165	−880	mV	Guaranteed input voltage high for all inputs
Input voltage, low	V_{IL}	−1810	−1475	mV	Guaranteed input voltage low for all inputs
Input current, high	I_{IH}		220	μA	V_{IN} = V_{IH} max
Input current, low	I_{IL}	0.5	170	μA	For $\overline{CS}$: V_{IN} = V_{IL} min
		−50		μA	For all others: V_{IN} = V_{IL} min
Supply current	I_{EE}	−160		mA	All inputs and outputs open

Notes:

(1) The device under test is mounted in a test socket and is measured at a thermal equilibrium established with a transverse air flow maintained at greater than 2.0 m/s.

AC Characteristics

T_A = 0 to +85 °C; V_{EE} = −4.5 V ± 5%

		μPD100500-15			μPD100500-20				
Parameter	Symbol	Min	Typ	Max	Min	Typ	Max	Unit	Test Conditions
Read Operation									
Address access time	t_{AA}			15			20	ns	
Chip select access time	t_{ACS}			10			15	ns	
Chip select recovery time	t_{RCS}			10			15	ns	
Write Operation									
Write pulse width	t_W	10			15			ns	
Data setup time	t_{WSD}	2			3			ns	
Data hold time	t_{WHD}	3			3			ns	
Address setup time	t_{WSA}	2			2			ns	
Address hold time	t_{WHA}	3			3			ns	
Chip select setup time	t_{WSCS}	2			2			ns	
Chip select hold time	t_{WHCS}	3			3			ns	
Write disable time	t_{WS}			10			15	ns	
Write recovery time	t_{WR}			18			23	ns	
Output Rise and Fall Times									
Rise time	t_R		2			2		ns	
Fall time	t_F		2			2		ns	

Notes:

(1) The device under test is mounted in a test socket and is measured at a thermal equilibrium established with a transverse air flow maintained at greater than 2.0 m/s.

(2) Input pulse levels = −1.7 to −0.9 V; input rise and fall times (measured between 20% and 80% or 80% and 20%) = 2.5 ns; input and output timing reference levels = 50%.

8

Figure 1. Loading Conditions Test Circuit

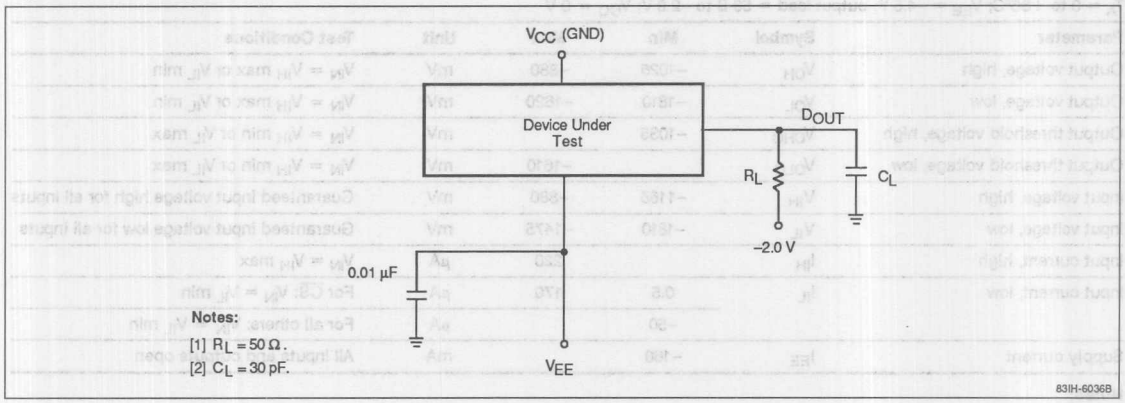
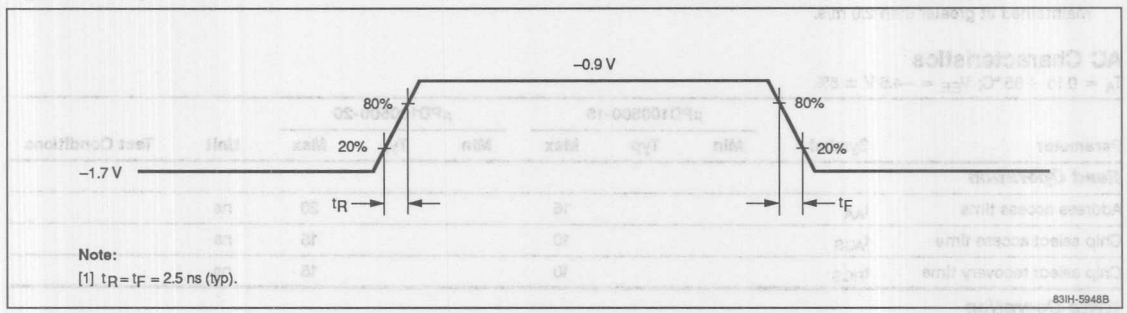
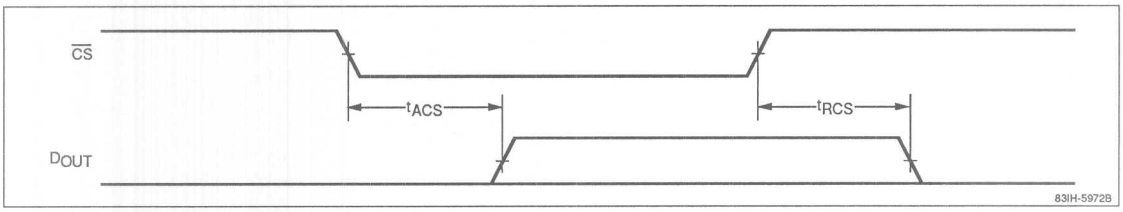


Figure 2. Input Pulse

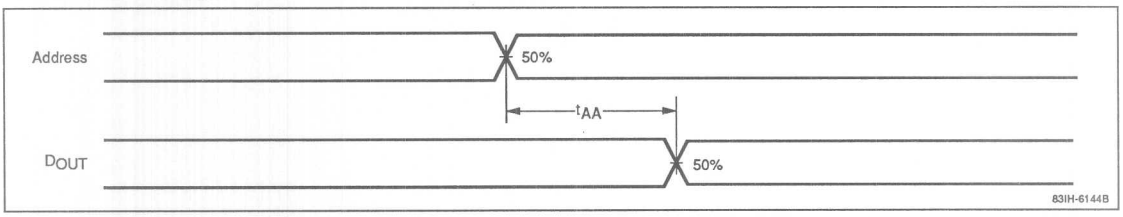


Timing Waveforms

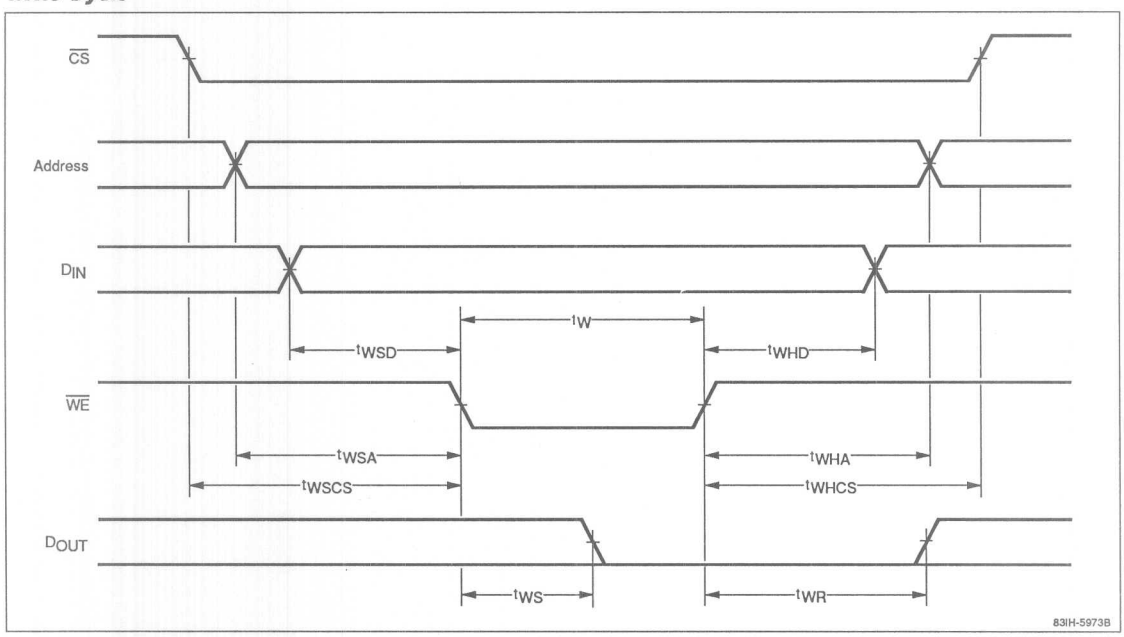
Chip Select Access Cycle



Address Access Cycle

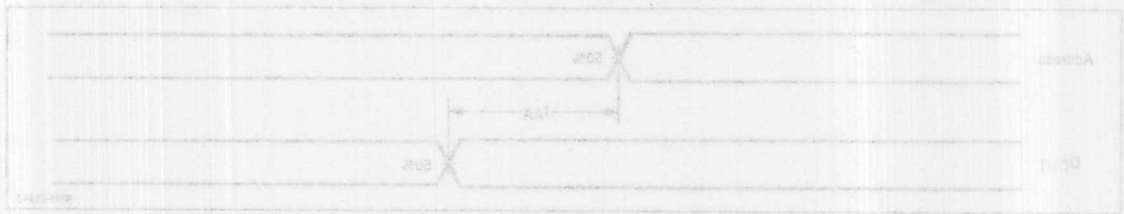


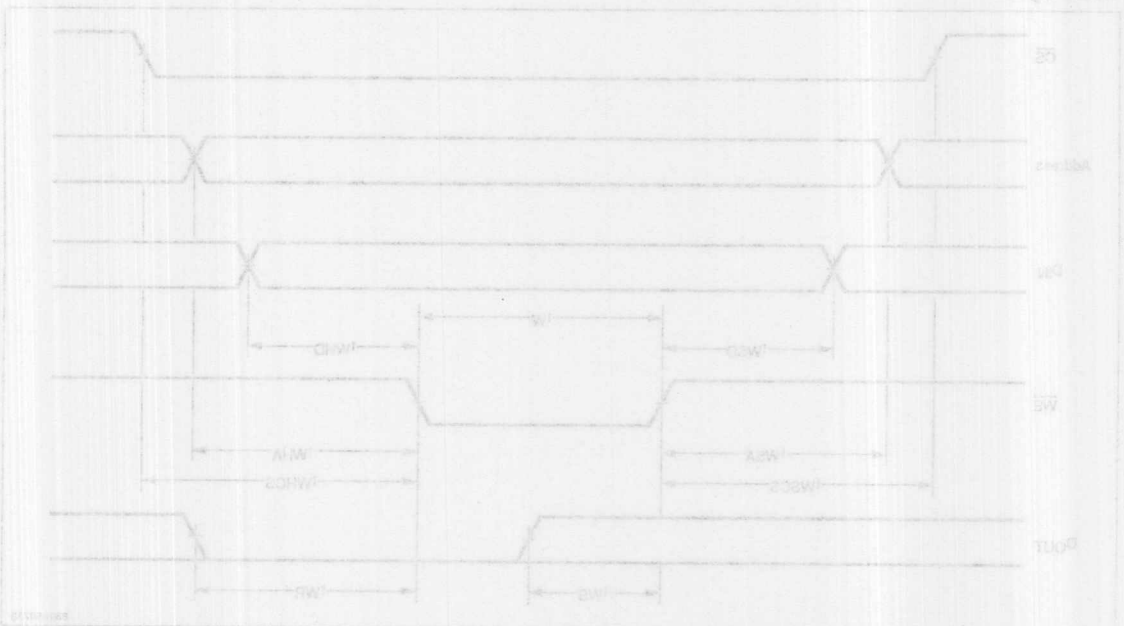
Write Cycle



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NEC Electronics Inc.

μPD100504
65,536 x 4-Bit
100K BiCMOS ECL RAM

PRELIMINARY INFORMATION

Description

The μPD100504 is a very high-speed BiCMOS RAM with full voltage and temperature compensation for a 100K ECL interface. Its unique design uses blended CMOS and bipolar peripheral circuits and N-channel MOS memory cells. The device is organized as 65,536 words by 4 bits and designed with an open-emitter output (noninverted) for low power consumption. A fast access time of 15 ns maximum is available in hermetic, 400-mil, 32-pin cerdip packaging.

Features

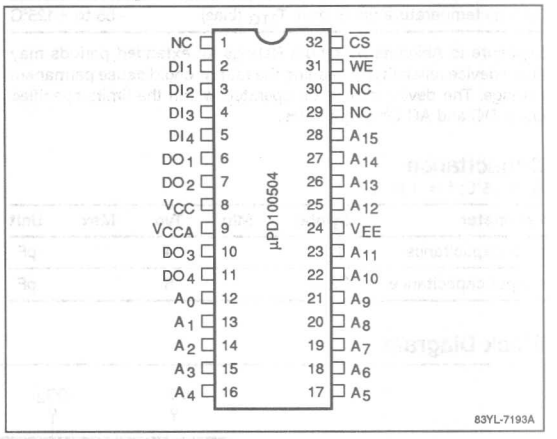
- BiCMOS technology
- 65,536-word x 4-bit organization
- 100K interface ECL with full voltage and temperature compensation
- Noninverted, open-emitter output
- Fast access time of 15 ns maximum
- Low power consumption
- 400-mil, 32-pin cerdip packaging

Ordering Information

Part Number	Access Time (max)	Power Consumption (max)	Package
μPD100504D-15	15 ns	810 mW	32-pin cerdip

Pin Configuration

32-Pin Cerdip



Pin Identification

Symbol	Function
A_0 - A_{15}	Address inputs
DI_1 - DI_4	Data inputs
D_{01} - D_{04}	Data outputs
$\overline{CS}$	Chip select
$\overline{WE}$	Write enable
V_{CC}, V_{CCA}	Ground
V_{EE}	−4.5-volt power supply
NC	No connection

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Absolute Maximum Ratings

Supply voltage, V_{EE}	−7.0 to +0.5 V
Input voltage, V_{IN}	V_{EE} to +0.5 V
Output current, I_{OUT}	−30 to +0.1 mA
Storage temperature, T_{STG}	−65 to +150°C
Storage temperature under bias, T_{STG} (bias)	−55 to +125°C

Exposure to Absolute Maximum Ratings for extended periods may affect device reliability; exceeding the ratings could cause permanent damage. The device should be operated within the limits specified under DC and AC Characteristics.

Capacitance

T_A = 25°C; f = 1 MHz

Parameter	Symbol	Min	Typ	Max	Unit
Input capacitance	C_{IN}		4		pF
Output capacitance	C_{OUT}		6		pF

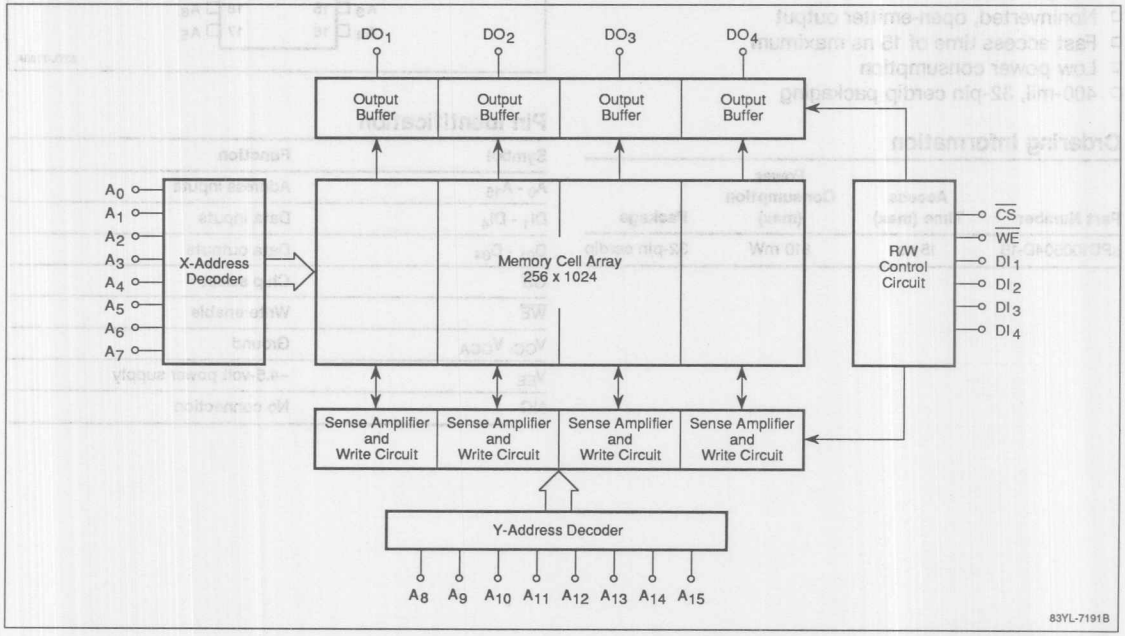
Truth Table

$\overline{CS}$	$\overline{WE}$	DI	Output	Mode
H	X	X	L	Not selected
L	L	L	L	Write 0
L	L	H	L	Write 1
L	H	X	D_{OUT}	Read

Notes:

(1) X = don't care.

Block Diagram



DC Characteristics

T_A = 0 to +85°C; V_{EE} = −4.5 V ±5%; output load = 50 Ω to −2.0 V; V_{CC} = 0 V

Parameter	Symbol	Min	Max	Unit	Test Conditions
Output voltage, high	V_{OH}	−1025	−880	mV	V_{IN} = V_{IH} max or V_{IL} min
Output voltage, low	V_{OL}	−1810	−1620	mV	V_{IN} = V_{IH} max or V_{IL} min
Output threshold voltage, high	V_{OHC}	−1035		mV	V_{IN} = V_{IH} min or V_{IL} max
Output threshold voltage, low	V_{OLC}		−1610	mV	V_{IN} = V_{IH} min or V_{IL} max
Input voltage, high	V_{IH}	−1165	−880	mV	Guaranteed input voltage high for all inputs
Input voltage, low	V_{IL}	−1810	−1475	mV	Guaranteed input voltage low for all inputs
Input current, high	I_{IH}		220	μA	V_{IN} = V_{IH} max
Input current, low	I_{IL}	0.5	170	μA	For $\overline{CS}$: V_{IN} = V_{IL} min
		−50		μA	For all others: V_{IN} = V_{IL} min
Supply current	I_{EE}	−180		mA	All inputs and outputs open

Notes:

(1) The device under test is mounted in a test socket and is measured at a thermal equilibrium established with a transverse air flow maintained at greater than 2.0 m/s.

AC Characteristics

T_A = 0 to +85°C; V_{EE} = −4.5 V ± 5%; V_{CC} = 0 V

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions
Read Operation						
Address access time	t_{AA}			15	ns	
Chip select access time	t_{ACS}			10	ns	
Chip select recovery time	t_{RCS}			10	ns	
Write Operation						
Write pulse width	t_W	10			ns	
Data setup time	t_{WSD}	2			ns	
Data hold time	t_{WHD}	3			ns	
Address setup time	t_{WSA}	2			ns	
Address hold time	t_{WHA}	3			ns	
Chip select setup time	t_{WSCS}	2			ns	
Chip select hold time	t_{WHCS}	3			ns	
Write disable time	t_{WS}			10	ns	
Write recovery time	t_{WR}			18	ns	
Output Rise and Fall Times						
Rise time	t_R		2		ns	
Fall time	t_F		2		ns	

Notes:

(1) The device under test is mounted in a test socket and is measured at a thermal equilibrium established with a transverse air flow maintained at greater than 2.0 m/s.

(2) Input pulse levels = −1.7 to −0.9 V; input rise and fall times (measured between 20% and 80% or 80% and 20%) = 2.0 ns; input and output timing reference levels = 50%.

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Figure 1. Loading Conditions Test Circuit

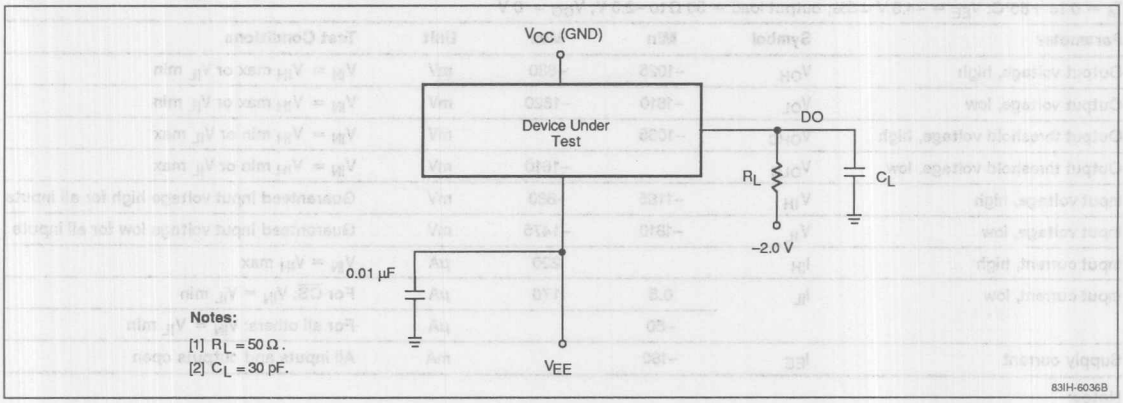
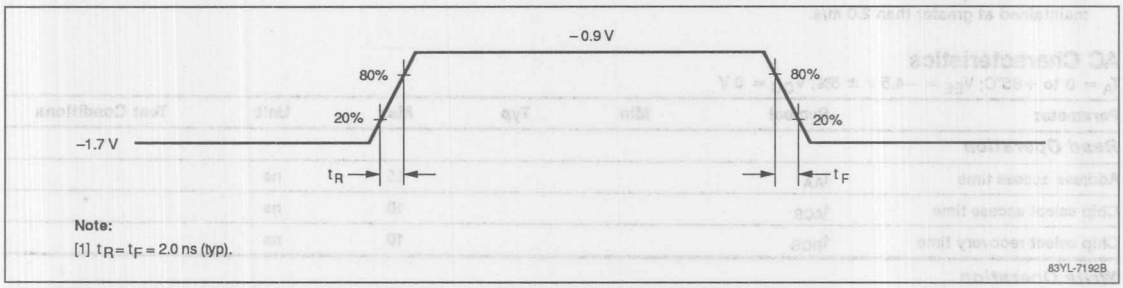
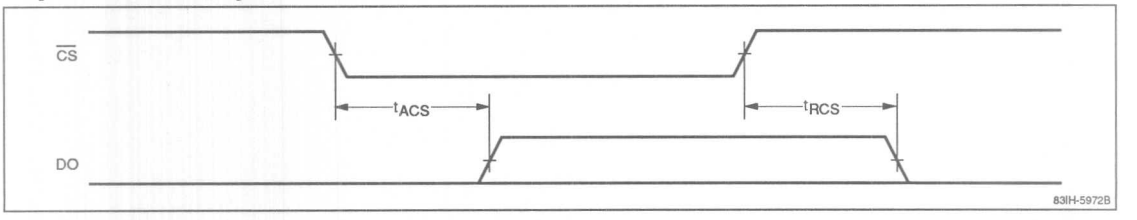


Figure 2. Input Pulse

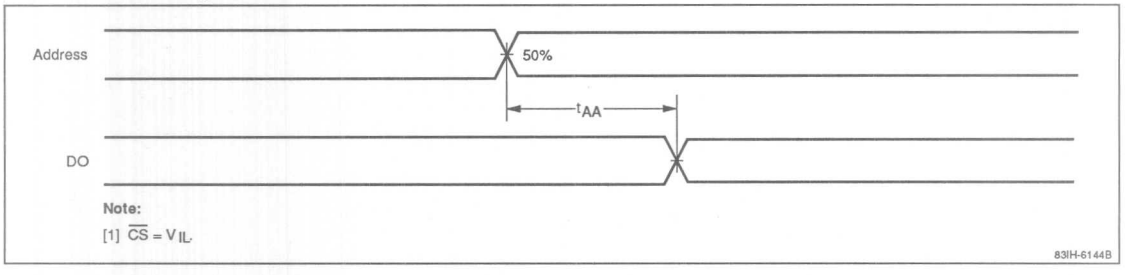


Timing Waveforms

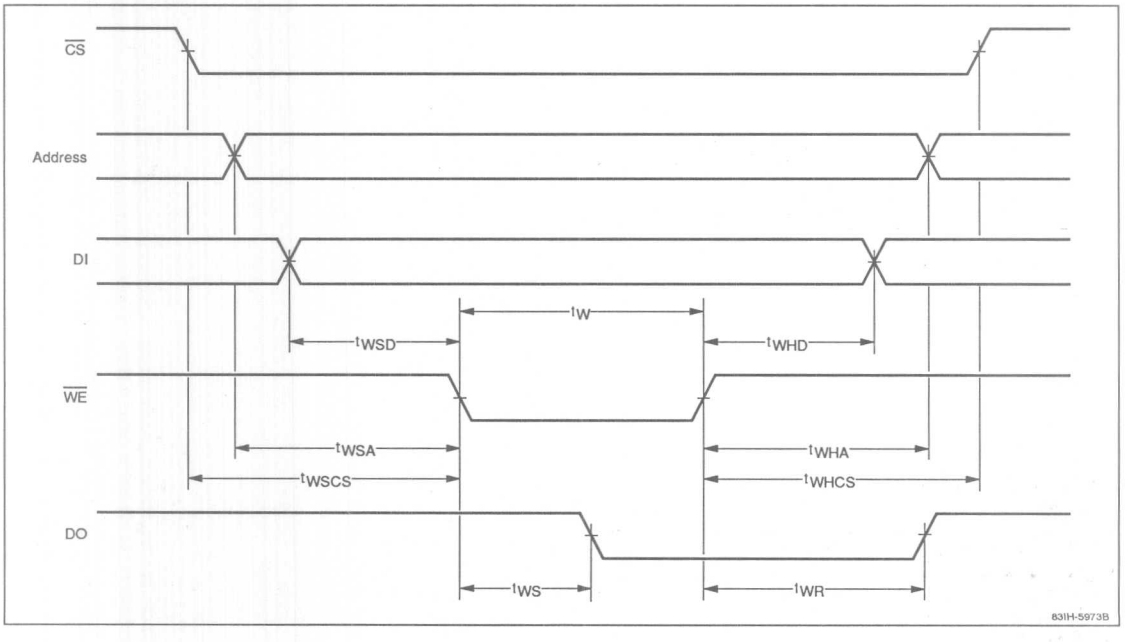
Chip Select Access Cycle



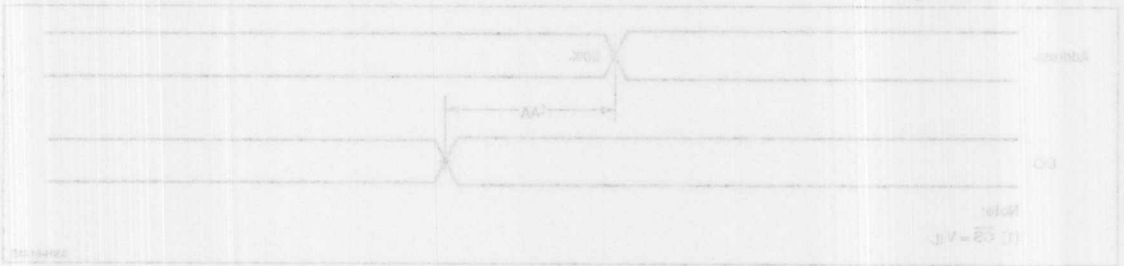
Address Access Cycle

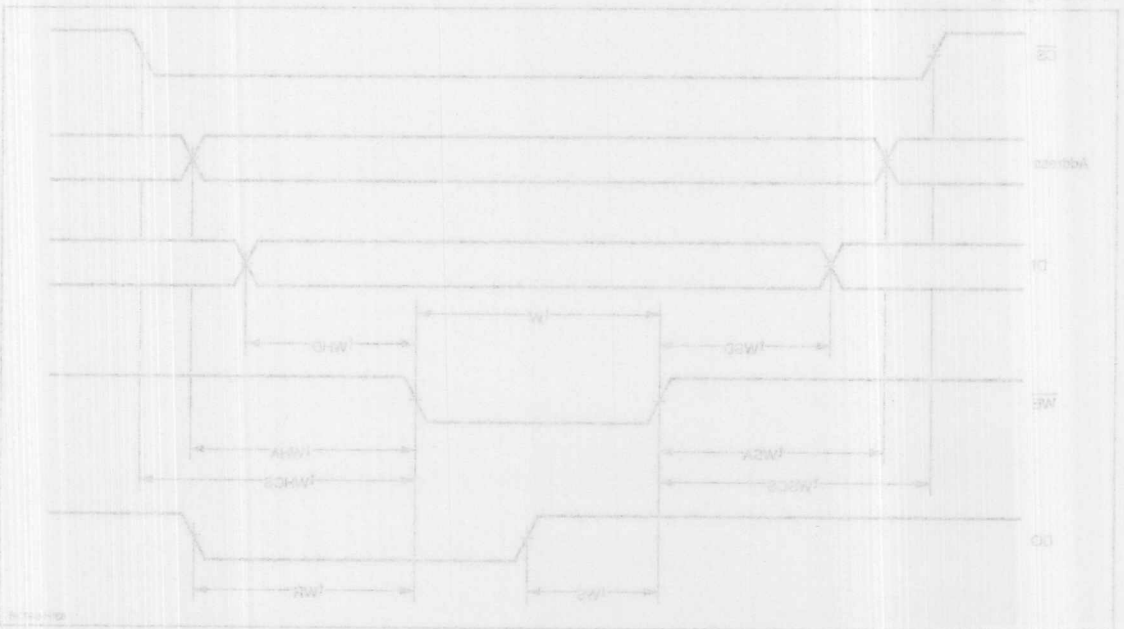


Write Cycle



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Section 9
EPROMs

μPD27HC65 8,192 x 8-Bit CMOS UV EPROM	**9-1**
μPD27C1000A 131,072 x 8-Bit CMOS UV EPROM	**9-13**
μPD27C10001A 131,072 x 8-Bit CMOS UV EPROM	**9-25**
μPD27C1024A 65,536 x 16-Bit CMOS UV EPROM	**9-37**
μPD27C2001 262,144 x 8-Bit CMOS UV EPROM	**9-49**
μPD27C4001 524,288 x 8-Bit CMOS UV EPROM	**9-61**

Additional New Product Information

Device Number	Description	Comments
EPROMs		
μPD27C1000A	128K x 8 bits, ROM-compatible, WSOP packaging	New package (B suffix)
μPD27C1001A	128K x 8 bits, JEDEC-compatible, WSOP packaging	New package (B suffix)
μPD27C2001	256K x 8 bits, WSOP packaging	New speed of 120 ns and new package (B suffix)
μPD27C4000	256K x 16 bits or 512K x 8 bits	New device, with speeds to 150 ns
μPD27C4096	256K x 16 bits	New device, with speeds to 120 ns

NEC Electronics Inc.

μPD27HC65
8,192 x 8-Bit
CMOS UV EPROM

Description

The μPD27HC65 is an ultraviolet erasable and electricaly programmable read-only memory fabricated with double-polysilicon CMOS technology for high speed and low operating and standby power. The μPD27HC65 is organized as 8,192 words by 8 bits and has three-state outputs, fully TTL-compatible inputs and outputs, and a program voltage (V_{PP}) of 12.5 volts. The device is packaged in a 24-pin cerdip with quartz window.

Features

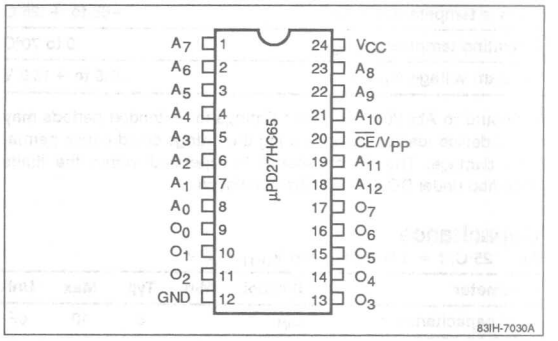
- 8,192-word x 8-bit organization
- Ultraviolet erasable and electrically programmable
- Ultra-high-speed access time
- Low power dissipation
  - 100 mA maximum (active)
  - 25 mA maximum (standby)
- TTL-compatible I/O for reading and programming
- Single +5-volt power supply
- Double polysilicon CMOS technology
- 24-pin cerdip packaging

Ordering Information

Part Number	Access Time (max)	Package
μPD27HC65DX-25	25 ns	24-pin cerdip with quartz window
DX-35	35 ns	
DX-45	45 ns	

Pin Configuration

24-Pin Cerdip



Pin Identification

Symbol	Function
A_0 - A_{12}	Address inputs
O_0 - O_7	Data outputs
$\overline{CE}/V_{PP}$	Chip enable/program voltage
GND	Ground
V_{CC}	+5-volt power supply

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Absolute Maximum Ratings

Power supply voltage, V_{CC}	−0.6 to +7.0 V
Input voltage, V_{IN}	−0.6 to +7.0 V
Input voltage, A_9 and A_{10}	−0.6 to +13.5 V
Output voltage, V_{OUT}	−0.6 to +7.0 V
Storage temperature, T_{STG}	−65 to +125°C
Operating temperature, T_{OPR}	0 to 70°C
Program voltage, V_{PP}	−0.6 to +13.5 V

Exposure to Absolute Maximum Ratings for extended periods may affect device realiability; exceeding the ratings could cause permanent damage. The device should be operated within the limits specified under DC and AC Characteristics.

Capacitance

T_A = 25°C; f = 1 MHz; V_{IN} and V_{OUT} = 0 V

Parameter	Symbol	Min	Typ	Max	Unit
Input capacitance	C_{IN}		5	10	pF
Output capacitance	C_{OUT}		10	15	pF
$\overline{CE}/V_{PP}$ input capacitance	C_P		10	20	pF

Truth Table

Cycle	$\overline{CE}/V_{PP}$	A_9	A_{10}	V_{CC}	Output
Read	V_{IL}	X	X	+5.0 V	D_{OUT}
Standby	V_{IH}	X	X	+5.0 V	High-Z
Byte program	+12.5 V	X	X	+6.0 V	D_{IN}
Program verify	V_{IL}	X	X	+6.0 V	D_{OUT}
Blank page set	V_{IH}	XX	V_{IHH}	+5.0 V	High-Z
Blank read (type 1)	V_{IL}	X	V_{IHH}	+5.0 V	D_{OUT}
Blank read (type 2)	V_{IL}	V_{IHH}	V_{IHH}	+5.0 V	D_{OUT}

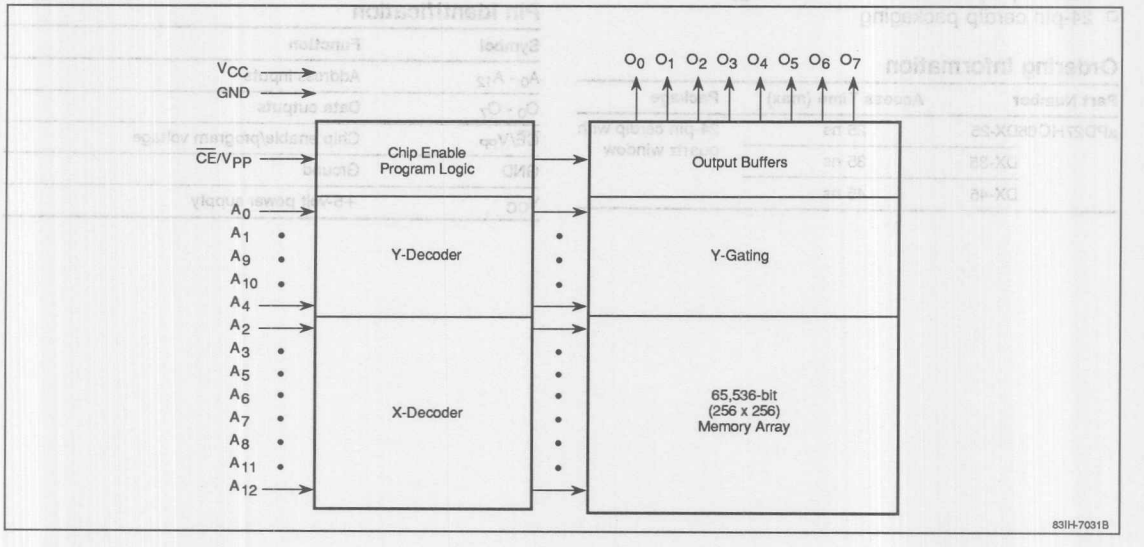
Notes:

(1) V_{IHH} = +12 V ±0.5.

(2) X can be either V_{IL} or V_{IH}.

(3) XX can be either V_{IL}, V_{IH}, or V_{IHH}.

Block Diagram



Recommended Operating Conditions

Parameter	Symbol	Min	Typ	Max	Unit
Read Operation or Standby					
Supply voltage	V_{CC}	4.75	5.0	5.25	V
Input voltage, high	V_{IH}	2.2		V_{CC} + 0.3	V
Input voltage, low (Note 1)	V_{IL}	−0.3		0.8	V
Operating temperature	T_A	0		70	°C
Programming Operation					
Supply voltage	V_{CC}	6.25	6.5	6.75	V
	$\overline{CE}/V_{PP}$	12.2	12.5	12.8	V
Input voltage, high	V_{IH}	2.4		V_{CC} + 0.3	V
Input voltage, low	V_{IL}	−0.3		0.8	V
Operating temperature	T_A	20	25	30	V

Notes:

(1) V_{IL} = −1.5 V minimum for 10 ns maximum pulse width.

DC Characteristics

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions
Read Operation or Standby T_A = 0 to +70°C; V_{CC} = +5.0 V ±5%						
Output voltage, high	V_{OH}	2.4			V	I_{OH} = −4 mA
Output voltage, low	V_{OL}			0.45	V	I_{OL} = 6 mA
Output leakage current	I_{LO}	−10		10	μA	V_{OUT} = 0 V to V_{CC}; $\overline{CE}/V_{PP}$ = V_{IH}
Input leakage current	I_{LI}	−10		10	μA	V_{IN} = 0 V to V_{CC}
V_{CC} current (active)	I_{CCA}			100	mA	$\overline{CE}/V_{PP}$ = V_{IL}; I_{OUT} = 0 mA (minimum cycle time)
V_{CC} current (standby)	I_{CCS1}			50	mA	$\overline{CE}/V_{PP}$ = V_{IH} (min); V_{IN} = V_{IH} or V_{IL}
	I_{CCS2}			25	mA	$\overline{CE}/V_{PP}$ ≥ V_{CC} − 0.2 V; V_{IN} ≥ V_{CC} − 0.2 V ≤ 0.2 V
Programming Operation T_A = 25 ±5°C; V_{CC} = +6.5 V ±0.25; $\overline{CE}/V_{PP}$ = +12.5 V ±0.3						
Output voltage, high	V_{OH}	2.4			V	I_{OH} = −4 mA
Output voltage, low	V_{OL}			0.45	V	I_{OL} = 6 mA
Input leakage current	I_{LI}	−10		10	μA	V_{IN} = 0 V to V_{CC}
V_{PP} current	I_{PP}			50	mA	
V_{CC} current	I_{CC}			100	mA	
Blank Read Operation T_A = 25 ±5°C; V_{CC} = +5.0 ±0.5 V						
Input voltage, high	V_{IH}	2.2		V_{CC} + 0.3	V	
	V_{IHH}	11.5	12	12.5	V	
Input voltage, low	V_{IL}	−0.3		0.8	V	
Output voltage, high	V_{OH}	2.4			V	I_{OH} = −4 mA
Output voltage, low	V_{OL}			0.45	V	I_{OL} = 6 mA
Input leakage current	I_{LI}	−10		10	μA	V_{IN} = 0 V to V_{CC}
V_{CC} current	I_{CC}			100	mA	

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AC Characteristics

T_A = 0 to +70°C; V_{CC} = +5.0 V ±5%

Parameter	Symbol	μPD27HC65-25 Min	μPD27HC65-25 Max	μPD27HC65-35 Min	μPD27HC65-35 Max	μPD27HC65-45 Min	μPD27HC65-45 Max	Unit	Test Conditions
Read Operation									
Address to output delay	t_{ACC}		25		35		45	ns	$\overline{CE}/V_{PP}$ = V_{IL}
$\overline{CE}$ to output delay	t_{CE}		20		30		30	ns	
$\overline{OE}$ or $\overline{CE}$ high to output float	t_{DF}		20		30		30	ns	
Address to output hold	t_{OH}	0		0		0		ns	$\overline{CE}/V_{PP}$ = V_{IL}

AC Characteristics (cont)

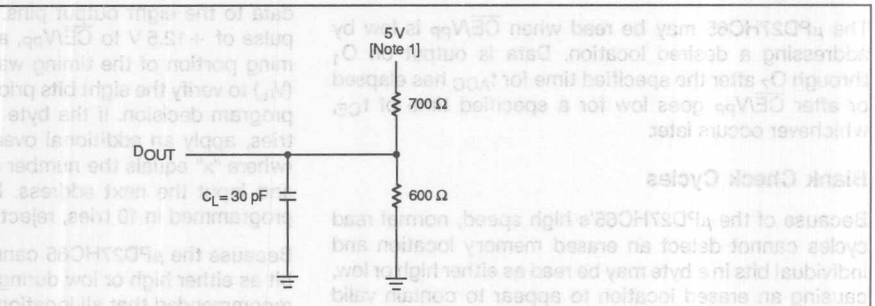
T_A = 25 ±5°C; V_{CC} = +6.0 V ±0.25; $\overline{CE}/V_{PP}$ = +12.5 V ±0.3

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions
Programming Operation						
Address setup time	t_{AS}	2			μs	
Address hold time	t_{AH}	2			μs	
Data setup time	t_{DS}	2			μs	
Data hold time	t_{DH}	2			μs	
V_{CC} setup time	t_{VCS}	2			μs	
V_{PP} rise time	t_R	1			μs	10% to 90%
V_{PP} fall time	t_F	1			μs	90% to 10%
$\overline{CE}/V_{PP}$ setup time	t_{CES}	2			μs	
$\overline{CE}/V_{PP}$ to data delay	t_{CEP}			500	ns	
$\overline{CE}/V_{PP}$ to output float	t_{DFP}			500	ns	
Verify pulse width	t_{VP}	1			μs	
Program pulse width	t_{PW}	0.095	0.1	0.105	ms	
Overprogram pulse width	t_{OPW}	0.095		1.05	ms	
Blank Read Operation						
Page address setup time	t_{PAS}	0			μs	
Blank read setup time	t_{BRS}	1			μs	
Page programming pulse width	t_{PPW}	1			μs	
Page address hold time	t_{PAH}	1			μs	
Address setup time	t_{ASB}	0			μs	
Address to output delay	t_{ACCB}			500	ns	
Address hold time	t_{AHB}	1			μs	

Notes:

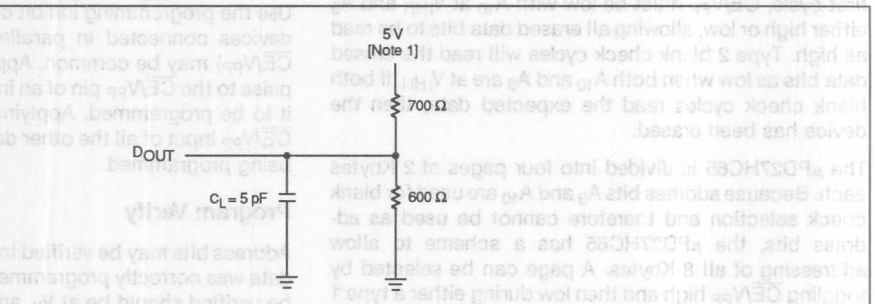
(1) Input pulse levels = 0 to 3 V; input and output timing reference levels = 1.5 V; input rise and fall times ≤ 5 ns. See figures 1 and 2 for output load.

Figure 1. Output Load



Note:
[1] Voltage is + 6.0 V for t_{AS}, t_{AW}, t_{CEP}, t_{CES}, t_{DH}, t_{DS}, t_F, t_{OPW}, t_{PW}, t_R, t_{VCS}, t_{VP}.

Figure 2. Output Load for t_{DF} and t_{DFP}



Note:
[1] Voltage is + 6.0 V for t_{DFP}.

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Read Operation

The μPD27HC65 may be read when $\overline{CE}/V_{PP}$ is low by addressing a desired location. Data is output on O_1 through O_7 after the specified time for t_{ACC} has elapsed or after $\overline{CE}/V_{PP}$ goes low for a specified time of t_{CE}, whichever occurs later.

Blank Check Cycles

Because of the μPD27HC65's high speed, normal read cycles cannot detect an erased memory location and individual bits in a byte may be read as either high or low, causing an erased location to appear to contain valid data. The only certain method of reading an erased location is by means of blank check cycles.

Two types of cycles must be executed to assure that addresses have been completely erased. To initiate the first cycle, $\overline{CE}/V_{PP}$ must be low with A_{10} at V_{IHH} and A_9 either high or low, allowing all erased data bits to be read as high. Type 2 blank check cycles will read the erased data bits as low when both A_{10} and A_9 are at V_{IHH}. If both blank check cycles read the expected data, then the device has been erased.

The μPD27HC65 is divided into four pages of 2 Kbytes each. Because address bits A_9 and A_{10} are used for blank check selection and therefore cannot be used as address bits, the μPD27HC65 has a scheme to allow addressing of all 8 Kbytes. A page can be selected by toggling $\overline{CE}/V_{PP}$ high and then low during either a type 1 or type 2 blank check cycle to read the page address on A_0 and A_1. Subsequently, all addresses in the selected page are read from A_0 through A_8, A_{11} and A_{12} to determine whether or not they have been erased. Once a page is verified, $\overline{CE}/V_{PP}$ may again be toggled high and then low to read the next addressed page on A_0 and A_1 and then the addresses in the selected page. This process continues until all four pages have been checked.

To determine whether the μPD27HC65 has been successfully erased, both types of blank check cycles must be executed. If both pass, then the device has been erased.

PROGRAMMING

Begin programming by erasing all data; this sets all data bits to an indeterminate level, the condition in which the μPD27HC65 is originally shipped. To enter data, raise V_{CC} to +6.0 V, address the first byte, and apply valid data to the eight output pins. Apply a 0.1-ms program pulse of +12.5 V to $\overline{CE}/V_{PP}$, as shown in the programming portion of the timing waveforms. Set $\overline{CE}/V_{PP}$ low (V_{IL}) to verify the eight bits prior to making a program/no program decision. If the byte is programmed within 10 tries, apply an additional overprogram pulse of "x" ms (where "x" equals the number of tries multiplied by 0.1) and input the next address. If the μPD27HC65 is not programmed in 10 tries, reject it as a program failure.

Because the μPD27HC65 cannot distinguish an erased bit as either high or low during a normal read cycle, it is recommended that all locations be programmed to prevent reading of incorrect data by EPROM programmers or the system CPU.

Program Inhibit

Use the programming inhibit option to program multiple devices connected in parallel. All like inputs (except $\overline{CE}/V_{PP}$) may be common. Applying a +12.5 V program pulse to the $\overline{CE}/V_{PP}$ pin of an individual device will cause it to be programmed. Applying a high level (V_{IH}) to the $\overline{CE}/V_{PP}$ input of all the other devices prevents them from being programmed.

Program Verify

Address bits may be verified to determine whether or not data was correctly programmed. $\overline{CE}/V_{PP}$ of the device to be verified should be at V_{IL} and V_{CC} at +6.0 V.

Program Erasure

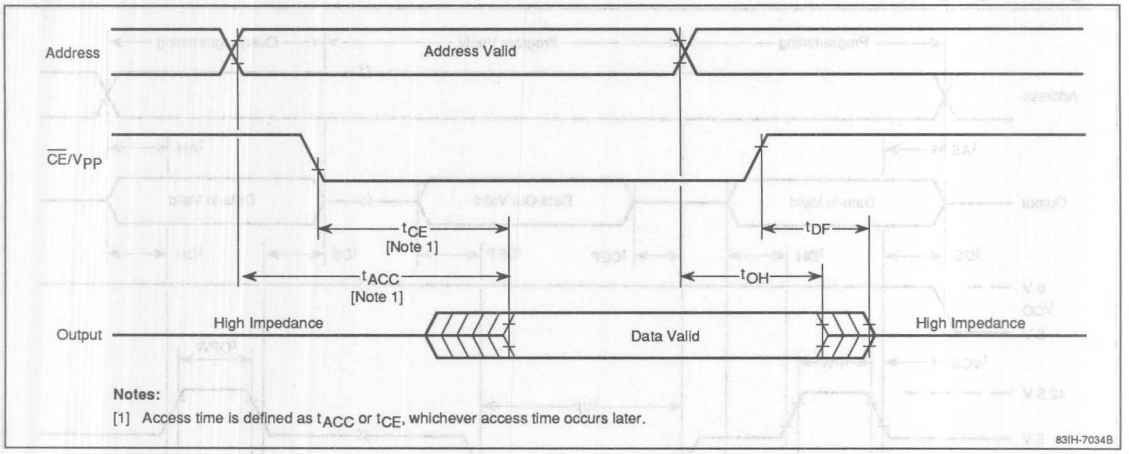
Erase data on the μPD27HC65 by exposing it to light with a wavelength shorter than 400 nm. Because exposure to direct sunlight or room-level fluorescent light could also erase the data, mask the window to prevent unintentional erasure by ultraviolet rays. Opaque labels are supplied with every device.

Data is typically erased by ultraviolet rays with a wavelength of 254 nm. A minimum integrated dose of 15 W-sec/cm^2 (ultraviolet lighting intensity multiplied by exposure time) is required to completely erase written data.

An ultraviolet lamp rated at 12,000 μW/cm^2 will complete erasure in approximately 20 minutes. Place the μPD27HC65 within 2.5 cm of the lamp tubes and remove any filter on the lamp.

Timing Waveforms

Read Cycle



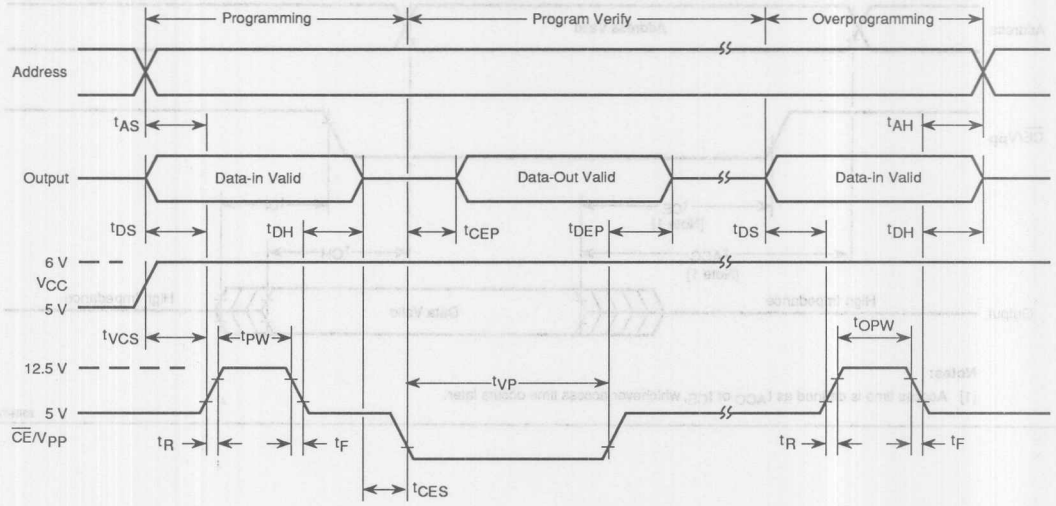
Notes:

[1] Access time is defined as t_{ACC} or t_{CE}, whichever access time occurs later.

9

Timing Waveforms (cont)

Programming Cycle



Notes:

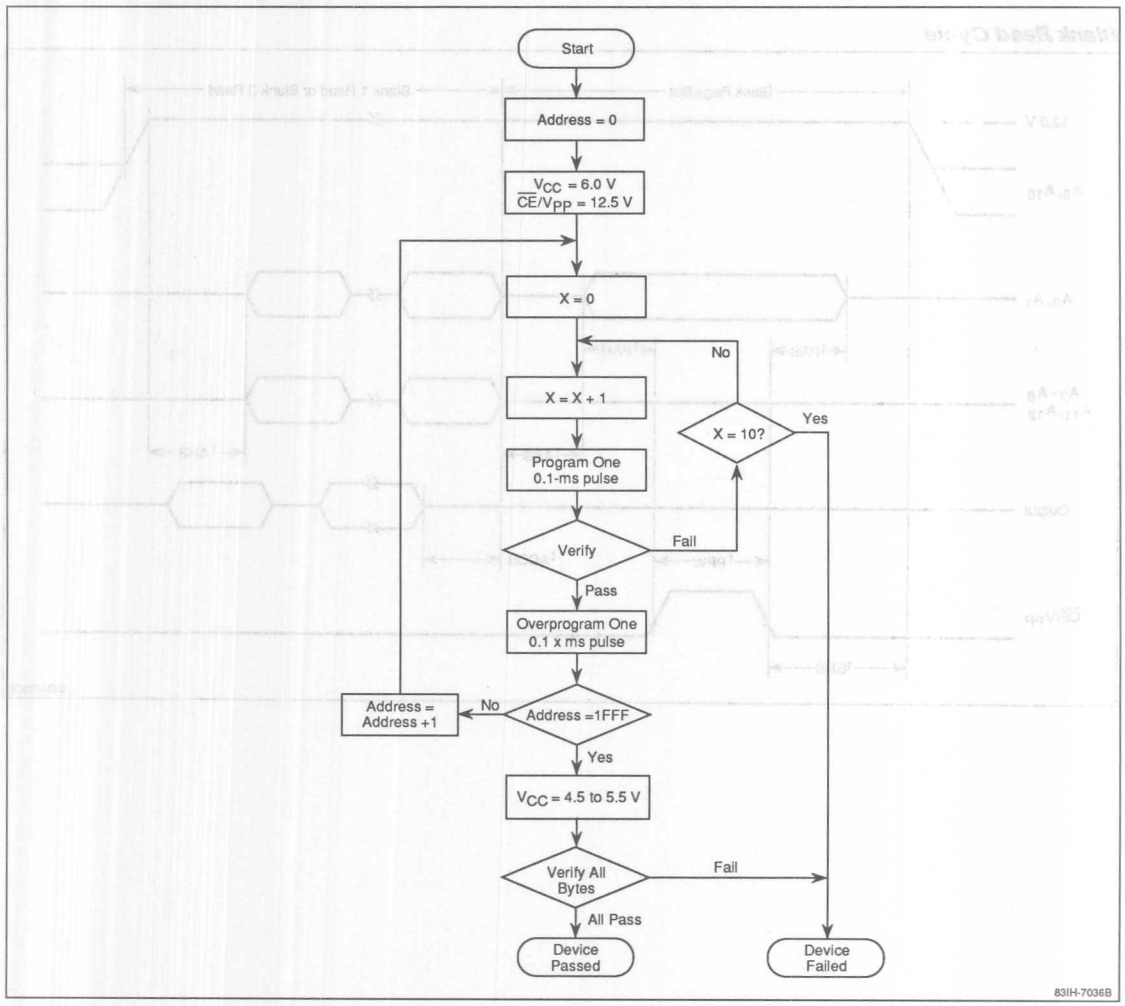
[1] V_{PP} must not be greater than + 13.5 V, including overshoot.

[2] Removing and reinserting the device while a voltage of 12.5 V is applied to V_{PP} may affect device reliability.

[3] The output lines are also used for data input when programming the device.

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Figure 3. Programming Flowchart



Timing Waveforms (cont)

Blank Read Cycle

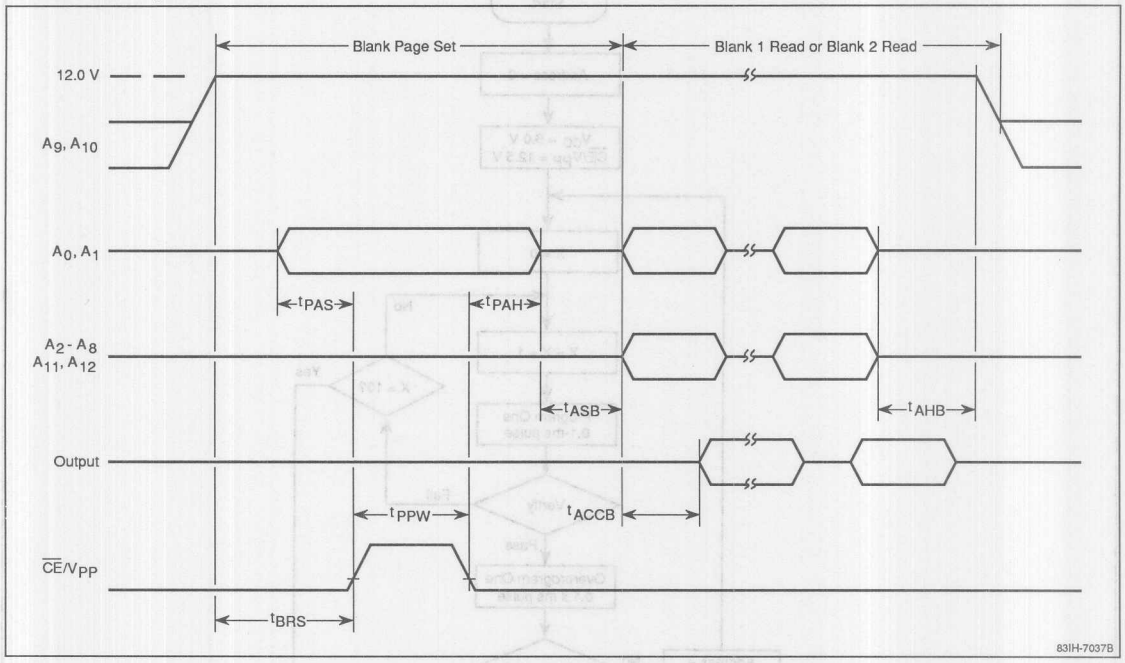
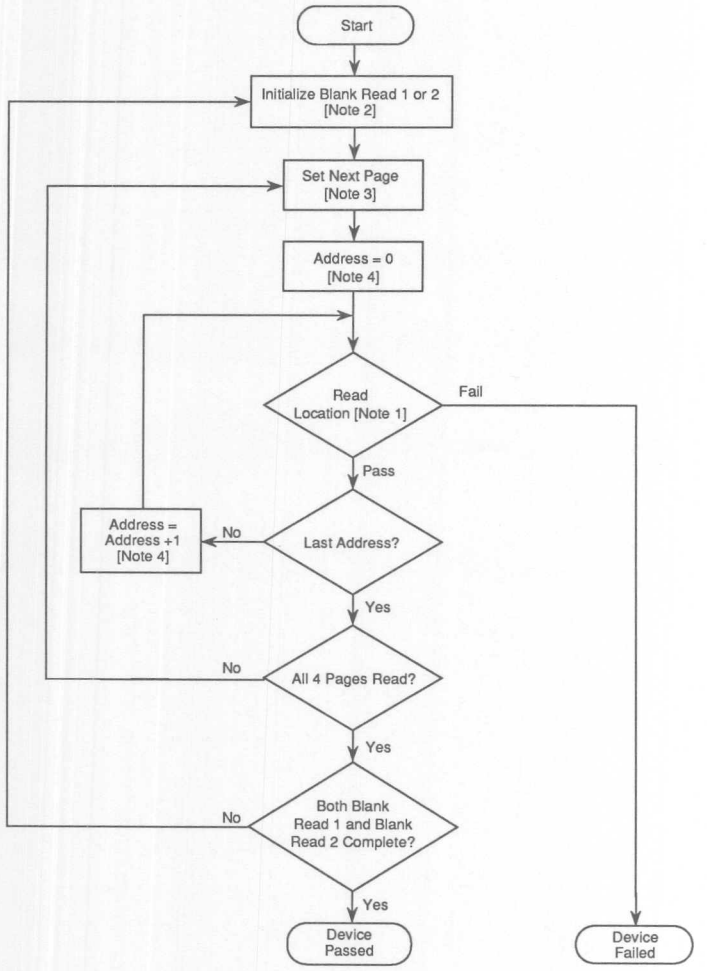


Figure 4. Blank Read Flowchart



Notes:

[1] Data must equal FF Hex for type 1 blank read cycles and 00 Hex for type 2 blank read cycles.

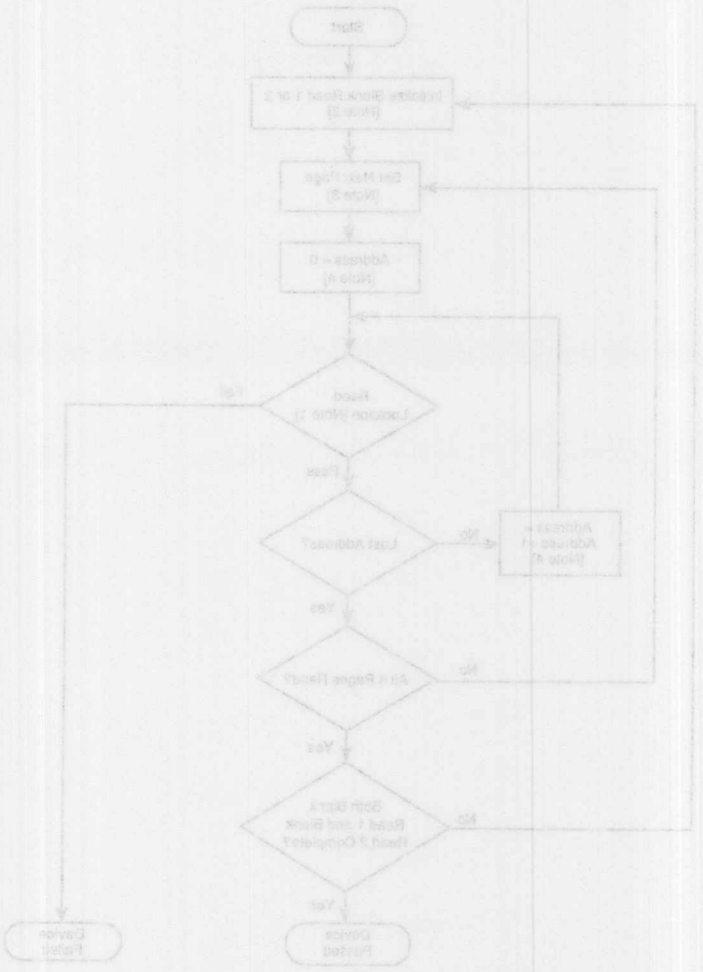
[2] For type 1 blank read cycles, $\overline{CE}/V_{PP} = V_{IL}$; $A_9 = V_{IL}$ or V_{IH}; $A_{10} = V_{IHH}$.
For type 2 blank read cycles, $\overline{CE}/V_{PP} = V_{IL}$; $A_9 = A_{10} = V_{IHH}$.

[3] Use A_0 and A_1 for setting the page address when toggling $\overline{CE}/V_{PP}$.

[4] Use only addresses A_0 through A_8 and A_{11} and A_{12}.

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9



NEC Electronics Inc.

μPD27C1000A
131,072 x 8-Bit
CMOS UV EPROM

Description

The μPD27C1000A is a 1,048,576-bit ultraviolet erasable and electrically programmable read-only memory fabricated with double-polysilicon CMOS technology for a substantial savings in both operating and standby power. The device is organized as 131,072 words by 8 bits and operates from a single +5-volt power supply.

The μPD27C1000A has both page and single-location programming features, three-state outputs, and fully TTL-compatible inputs and outputs. It also has a program voltage (V_{PP}) of 12.5 volts and is available in a 32-pin cerdip with quartz window.

Features

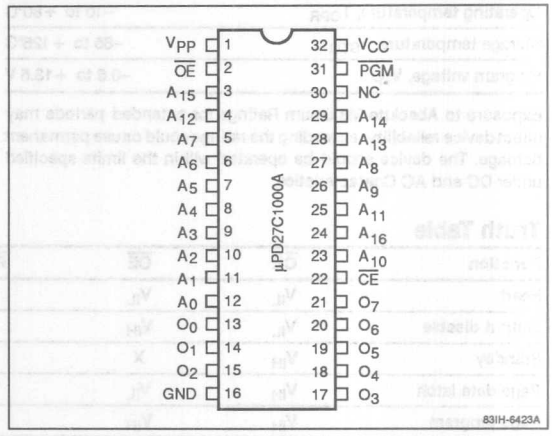
- 131,072-word x 8-bit organization
- Ultraviolet erasable and electrically programmable
- High-speed programming capability
  - Page programming
  - Byte programming
- Low power dissipation
  - 40 mA maximum (active)
  - 100 μA maximum (standby)
- TTL-compatible I/O for reading and programming
- Single +5-volt power supply
- Double-polysilicon CMOS technology
- 32-pin cerdip packaging
- Pinout compatibility with 28-pin mask-programmable μPD23C1000s

Ordering Information

Part Number	Access Time (max)	Package
μPD27C1000AD-12	120 ns	32-pin cerdip with a quartz window
D-15	150 ns	
D-20	200 ns	

Pin Configuration

32-Pin Cerdip



Pin Identification

Symbol	Function
A_0 - A_{16}	Address inputs
O_0 - O_7	Data outputs
$\overline{CE}$	Chip enable
$\overline{OE}$	Output enable
$\overline{PGM}$	Program
GND	Ground
V_{CC}	+5-volt power supply
V_{PP}	Program voltage
NC	No connection

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New WSOP package will be available in 1991.

Absolute Maximum Ratings

Power supply voltage, V_{CC}	−0.6 to +7.0 V
Input voltage, V_{IN}	−0.6 to +7.0 V
Input voltage, A_9	−0.6 to +13.5 V
Output voltage, V_{OUT}	−0.6 to +7.0 V
Operating temperature, T_{OPR}	−10 to +80°C
Storage temperature, T_{STG}	−65 to +125°C
Program voltage, V_{PP}	−0.6 to +13.5 V

Exposure to Absolute Maximum Ratings for extended periods may affect device reliability; exceeding the ratings could cause permanent damage. The device should be operated within the limits specified under DC and AC Characteristics.

Capacitance

T_A = 25°C; f = 1 MHz; V_{IN} and V_{OUT} = 0 V

Parameter	Symbol	Min	Typ	Max	Unit
Input capacitance	C_{IN}			14	pF
Output capacitance	C_{OUT}			16	pF

Truth Table

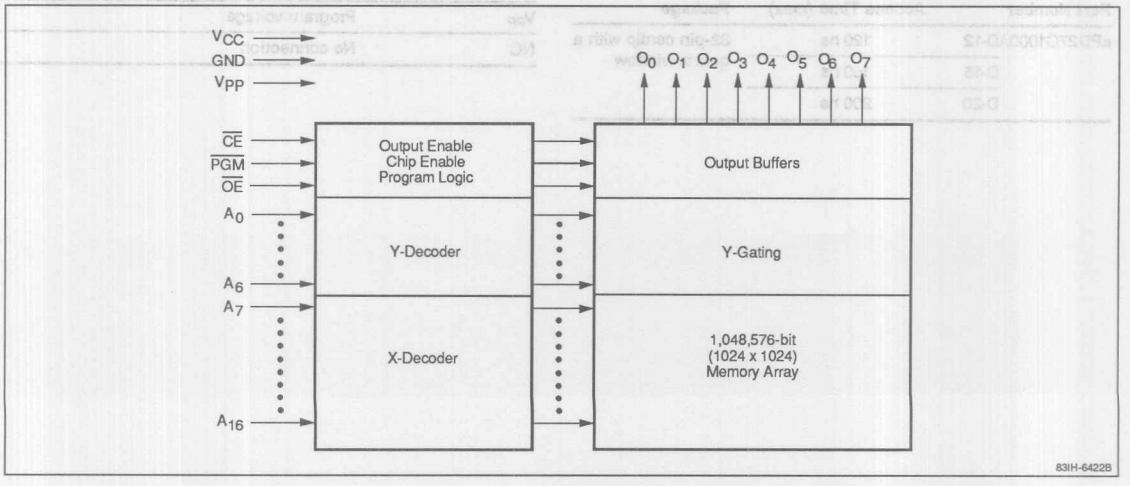
Function	$\overline{CE}$	$\overline{OE}$	$\overline{PGM}$	V_{PP}	V_{CC}	Output
Read	V_{IL}	V_{IL}	V_{IH}	+5.0 V	+5.0 V	D_{OUT}
Output disable	V_{IL}	V_{IH}	X	+5.0 V	+5.0 V	High-Z
Standby	V_{IH}	X	X	+5.0 V	+5.0 V	High-Z
Page data latch	V_{IH}	V_{IL}	V_{IH}	+12.5 V	+6.5 V	D_{IN}
Page program	V_{IH}	V_{IH}	V_{IL}	+12.5 V	+6.5 V	High-Z
Byte program	V_{IL}	V_{IH}	V_{IL}	+12.5 V	+6.5 V	D_{IN}
Program verify	V_{IL}	V_{IL}	V_{IH}	+12.5 V	+6.5 V	D_{OUT}
Program inhibit	X	V_{IL}	V_{IL}	+12.5 V	+6.5 V	High-Z
	X	V_{IH}	V_{IH}			

Notes:

(1) X can be either V_{IL} or V_{IH}.

(2) In read operation, $\overline{PGM}$ must be set to V_{IH} at all times, or switched from V_{IL} to V_{IH} at least 2 μs before $\overline{OE}$ or $\overline{CE}$ goes to V_{IH}.

Block Diagram



Recommended Operating Conditions

Parameter	Symbol	Min	Typ	Max	Unit
Read Operation or Standby					
Supply voltage	V_{CC}	4.5	5.0	5.5	V
	V_{PP}	V_{CC} – 0.6	V_{CC}	V_{CC} + 0.6	V
Input voltage, high	V_{IH}	2.0		V_{CC} + 0.3	V
Input voltage, low	V_{IL}	–0.3		0.8	V
Operating temperature	T_A	0		70	°C
Programming Operation					
Supply voltage	V_{CC}	6.25	6.5	6.75	V
	V_{PP}	12.2	12.5	12.8	V
Input voltage, high	V_{IH}	2.4		V_{CC} + 0.3	V
Input voltage, low	V_{IL}	–0.3		0.8	V
Operating temperature	T_A	20	25	30	°C

DC Characteristics

T_A = 0 to +70°C; V_{CC} = +5.0 V ±10%; V_{PP} = V_{CC} ±0.6

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions
Read Operation or Standby						
Output voltage, high	V_{OH1}	2.4			V	I_{OH} = –400 μA
	V_{OH2}	V_{CC} – 0.7			V	I_{OH} = –100 μA
Output voltage, low	V_{OL}			0.45	V	I_{OL} = 2.1 mA
Output leakage current	I_{LO}	–10		10	μA	V_{OUT} = 0 V to V_{CC}; $\overline{OE}$ = V_{IH}
Input leakage current	I_{LI}	–10		10	μA	V_{IN} = 0 V to V_{CC}
V_{PP} current	I_{PP}		1	100	μA	V_{PP} = V_{CC}
V_{CC} current (active)	I_{CCA1}			15	mA	$\overline{CE}$ = V_{IL}; V_{IN} = V_{IH}
	I_{CCA2}			40	mA	f = 8.4 MHz; I_{OUT} = 0 mA; t_{ACC} = 120 ns
				30	mA	f = 6.7 MHz; I_{OUT} = 0 mA; t_{ACC} = 150 ns
				25	mA	f = 5 MHz; I_{OUT} = 0 mA; t_{ACC} = 200 ns
V_{CC} current (standby)	I_{CCS1}			1	mA	$\overline{CE}$ = V_{IH}
	I_{CCS2}		1	100	μA	$\overline{CE}$ = V_{CC}; V_{IN} = 0 V to V_{CC}

DC Characteristics (cont)

T_A = 25 ±5°C; V_{CC} = +6.5 V ±0.25; V_{PP} = +12.5 V ± 0.3

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions
Programming Operation						
Output voltage, high	V_{OH}	2.4			V	I_{OH} = –400 μA
Output voltage, low	V_{OL}			0.45	V	I_{OL} = 2.1 mA
Input leakage current	I_{LI}	–10		10	μA	V_{IN} = V_{IL} or V_{IH}
V_{PP} current	I_{PP}			50	mA	$\overline{CE}$ = $\overline{PGM}$ = V_{IL}
V_{CC} current	I_{CC}			30	mA	

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AC Characteristics

T_A = 0 to +70°C; V_{CC} = +5.0 V ± 10%; V_{PP} = V_{CC} ± 0.6 V

		μPD27C1000A-12		μPD27C1000A-15		μPD27C1000A-20			
Parameter	**Symbol**	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**	**Unit**	**Test Conditions**
Read Operation or Standby									
Address to output delay	t_{ACC}		120		150		200	ns	$\overline{CE}$ = $\overline{OE}$ = V_{IL}
$\overline{CE}$ to output delay	t_{CE}		120		150		200	ns	$\overline{OE}$ = V_{IL}
$\overline{OE}$ to output delay	t_{OE}		70		70		75	ns	$\overline{CE}$ = V_{IL}
$\overline{OE}$ or $\overline{CE}$ high to output float	t_{DF}	0	50	0	50	0	60	ns	$\overline{CE}$ = V_{IL} or $\overline{OE}$ = V_{IL}
Address to output hold	t_{OH}	0		0		0		ns	$\overline{CE}$ = $\overline{OE}$ = V_{IL}

AC Characteristics (cont)

T_A = +25 ± 5°C; V_{CC} = +6.5 ± 0.25 V; V_{PP} = +12.5 ± 0.3 V

Parameter	**Symbol**	**Min**	**Typ**	**Max**	**Unit**	**Test Conditions**
Page Programming Operation						
Address setup time	t_{AS}	2			μs	
$\overline{CE}$ setup time	t_{CES}	2			μs	
Data setup time	t_{DS}	2			μs	
Address hold time	t_{AH}	2			μs	
	t_{AHL}	2			μs	
	t_{AHV}	0			μs	
Data hold time	t_{DH}	2			μs	
$\overline{OE}$ to output float time	t_{DF}	0		130	ns	
V_{PP} setup time	t_{VPS}	2			μs	
V_{CC} setup time	t_{VCS}	2			μs	
Program pulse width	t_{PW}	0.095	0.1	0.105	ms	
$\overline{OE}$ setup time	t_{OES}	2			μs	
$\overline{OE}$ to output delay	t_{OE}			150	ns	
$\overline{OE}$ pulse width during data latch	t_{LW}	1			μs	
$\overline{PGM}$ setup time	t_{PGMS}	2			μs	
$\overline{CE}$ hold time	t_{CEH}	2			μs	
OE hold time	t_{OEH}	2			μs	

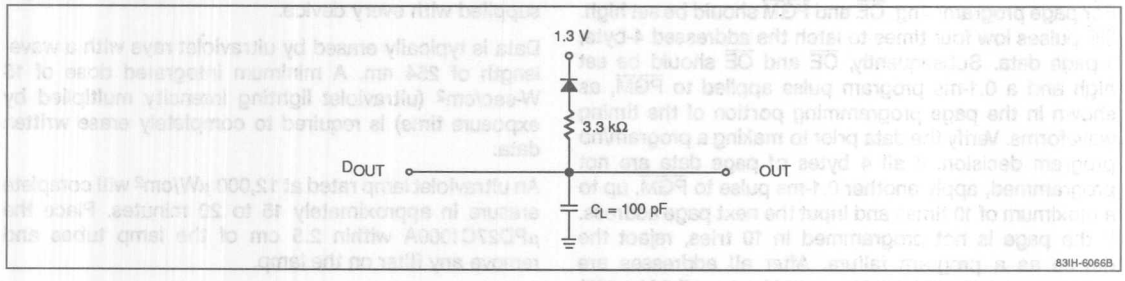
AC Characteristics (cont)

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions
Byte Programming Operation						
Address setup time	t_{AS}	2			μs	
$\overline{OE}$ setup time	t_{OES}	2			μs	
Data setup time	t_{DS}	2			μs	
Address hold time	t_{AH}	2			μs	
Data hold time	t_{DH}	2			μs	
$\overline{OE}$ to output float time	t_{DF}	0		130	ns	
V_{PP} setup time	t_{VPS}	2			μs	
V_{CC} setup time	t_{VCS}	2			μs	
Program pulse width	t_{PW}	0.095	0.1	0.105	ms	
$\overline{CE}$ setup time	t_{CES}	2			μs	
$\overline{OE}$ to output delay	t_{OE}			150	ns	

Notes:

(1) Input pulse levels = 0.45 to 2.4 V; input and output timing reference levels = 0.8 and 2.0 V; input rise and fall times ≤ 20 ns. See figure 1 for output load.

Figure 1. Output Load



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Programming Operation

Begin programming by erasing all data; this sets all data bits high. The μPD27C1000A is originally shipped in this condition. To enter data, program a low-level TTL signal into the chosen location. Address the first byte or page location and apply valid data at the eight output pins. Raise V_{CC} to +6.5 V ± 0.25 and V_{PP} to +12.5 V ± 0.3.

Byte Programming

For byte programming, $\overline{CE}$ should be set low and $\overline{OE}$ high to start programming at the initial address. Apply a 0.1-ms program pulse to $\overline{PGM}$, as shown in the byte programming portion of the timing waveforms. Set $\overline{OE}$ low to verify the eight bits prior to making a program/no program decision. If the byte is not programmed, apply another 0.1-ms pulse to $\overline{PGM}$, up to a maximum of 10 times, and input the next address. If the bits are not programmed in 10 tries, reject the device as a program failure. After all addresses are programmed, lower both V_{CC} and V_{PP} to +5.0 V ± 10% and verify all data again.

Page Programming

For page programming, $\overline{CE}$ and $\overline{PGM}$ should be set high. $\overline{OE}$ pulses low four times to latch the addressed 4-byte, 1-page data. Subsequently, $\overline{CE}$ and $\overline{OE}$ should be set high and a 0.1-ms program pulse applied to $\overline{PGM}$, as shown in the page programming portion of the timing waveforms. Verify the data prior to making a program/no program decision. If all 4 bytes of page data are not programmed, apply another 0.1-ms pulse to $\overline{PGM}$, up to a maximum of 10 times and input the next page address. If the page is not programmed in 10 tries, reject the device as a program failure. After all addresses are programmed, lower both V_{CC} and V_{PP} to +5.0 V ±10% and verify all data again.

Program Inhibit

Use the programming inhibit option to program multiple μPD27C1000As connected in parallel. All like inputs except $\overline{PGM}$ and $\overline{OE}$ may be common. Program individual devices by applying a low-level TTL pulse to the $\overline{PGM}$ pin of the devices to be programmed. Apply a high-level signal to the $\overline{PGM}$ pins of the other devices to prevent them from being programmed.

Program Verification

To verify that the device is correctly programmed, normal read cycles can be executed with a high logic level applied to the $\overline{PGM}$ pin and low logic levels applied to the $\overline{CE}$ and $\overline{OE}$ pins of the device to be verified. The $\overline{CE}$ or $\overline{OE}$ pins of all other devices should be set high.

Program Erasure

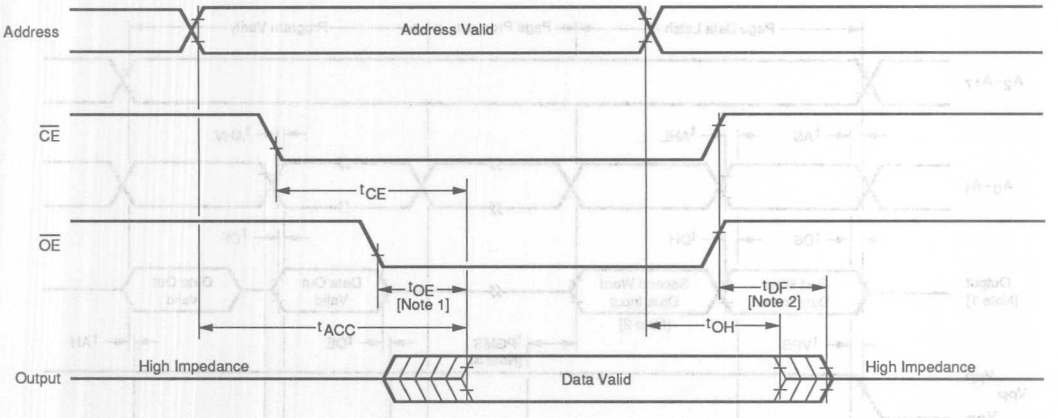
Erase data on the μPD27C1000A by exposing it to light with a wavelength shorter than 400 nm. Since exposure to direct sunlight or room-level fluorescent light could also erase the data, mask the window to prevent unintentional erasure by ultraviolet rays. Opaque labels are supplied with every device.

Data is typically erased by ultraviolet rays with a wavelength of 254 nm. A minimum integrated dose of 15 W-sec/cm^2 (ultraviolet lighting intensity multiplied by exposure time) is required to completely erase written data.

An ultraviolet lamp rated at 12,000 μW/cm^2 will complete erasure in approximately 15 to 20 minutes. Place the μPD27C1000A within 2.5 cm of the lamp tubes and remove any filter on the lamp.

Timing Waveforms

Read Cycle



Notes:

[1] $\overline{OE}$ may be delayed for read operation up to $t_{ACC} - t_{OE}$, after the falling edge of $\overline{CE}$, without impact on t_{ACC}.

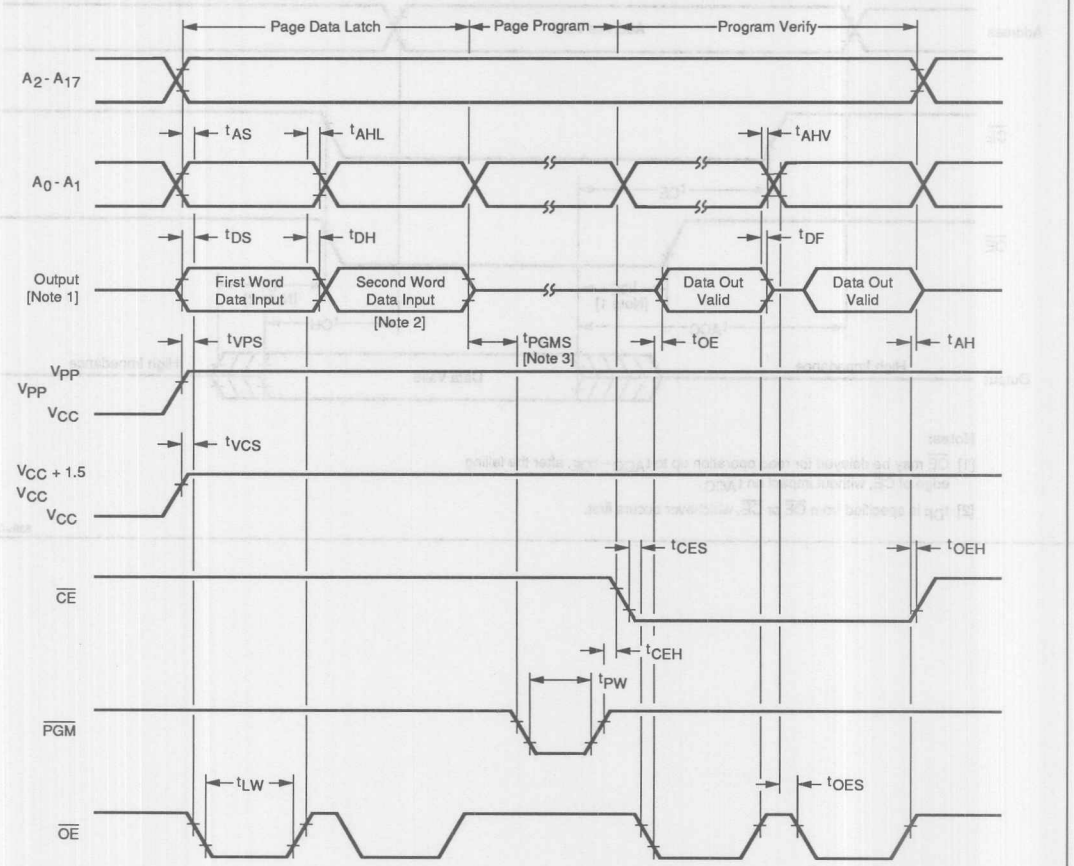
[2] t_{DF} is specified from $\overline{OE}$ or $\overline{CE}$, whichever occurs first.

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Timing Waveforms (cont)

Page Programming Cycle



Notes:

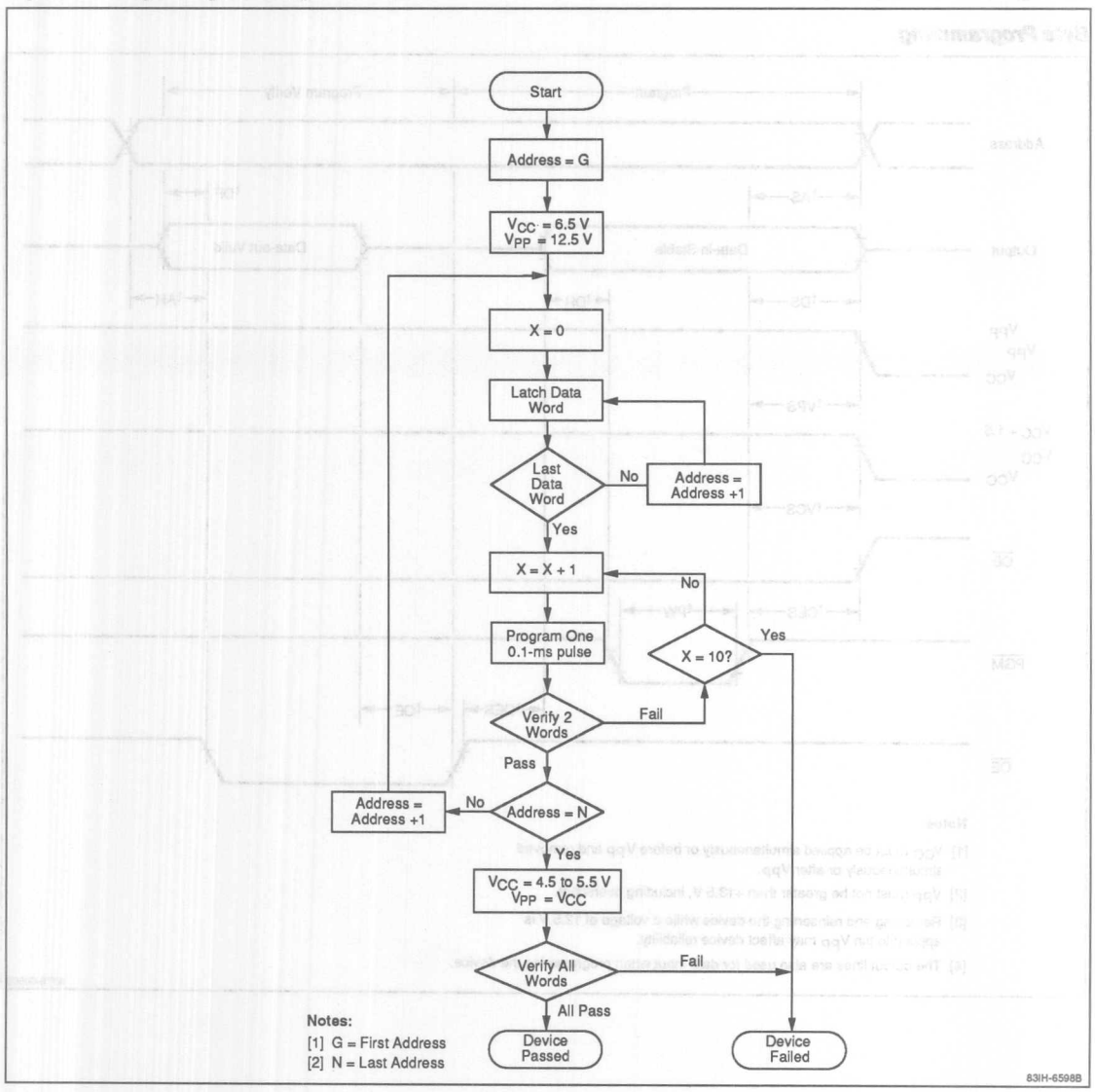
[1] The output lines are also used for data input when programming the device.

[2] Up to 32 words may be written during each page programming cycle.

[3] t_{PGMS} timing begins after the last data word has been input.

83TB-6057B

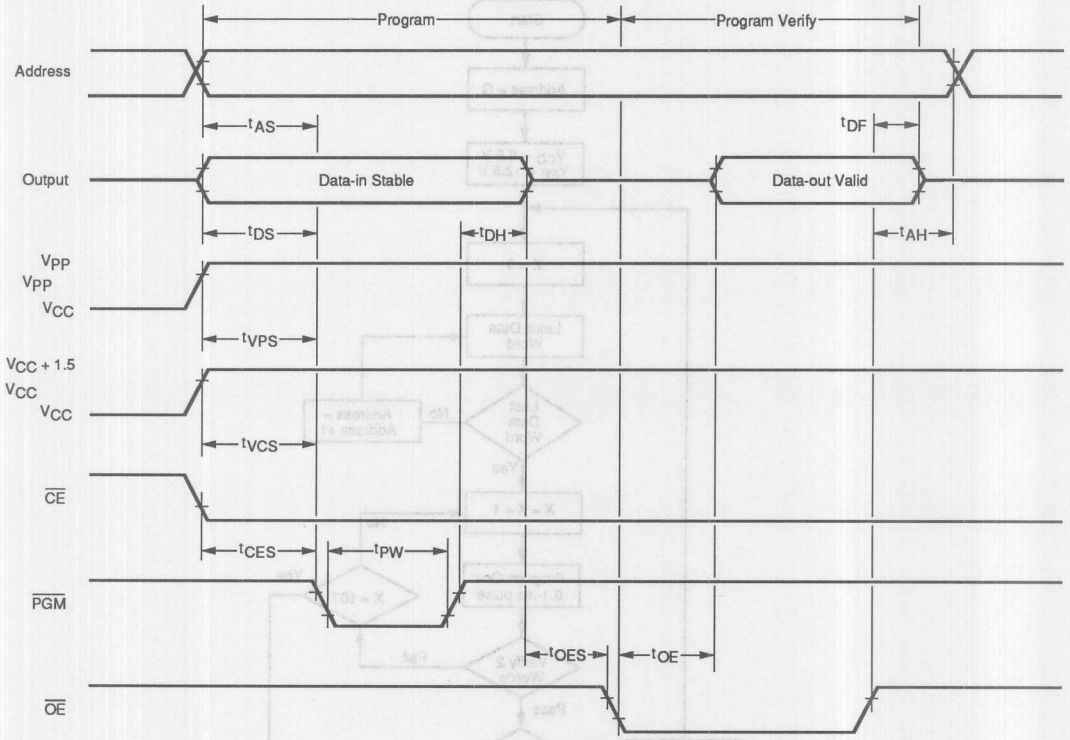
Figure 2. Page Programming Flowchart



9

Timing Waveforms (cont)

Byte Programming



Notes:

[1] V_{CC} must be applied simultaneously or before V_{PP} and removed simultaneously or after V_{PP}.

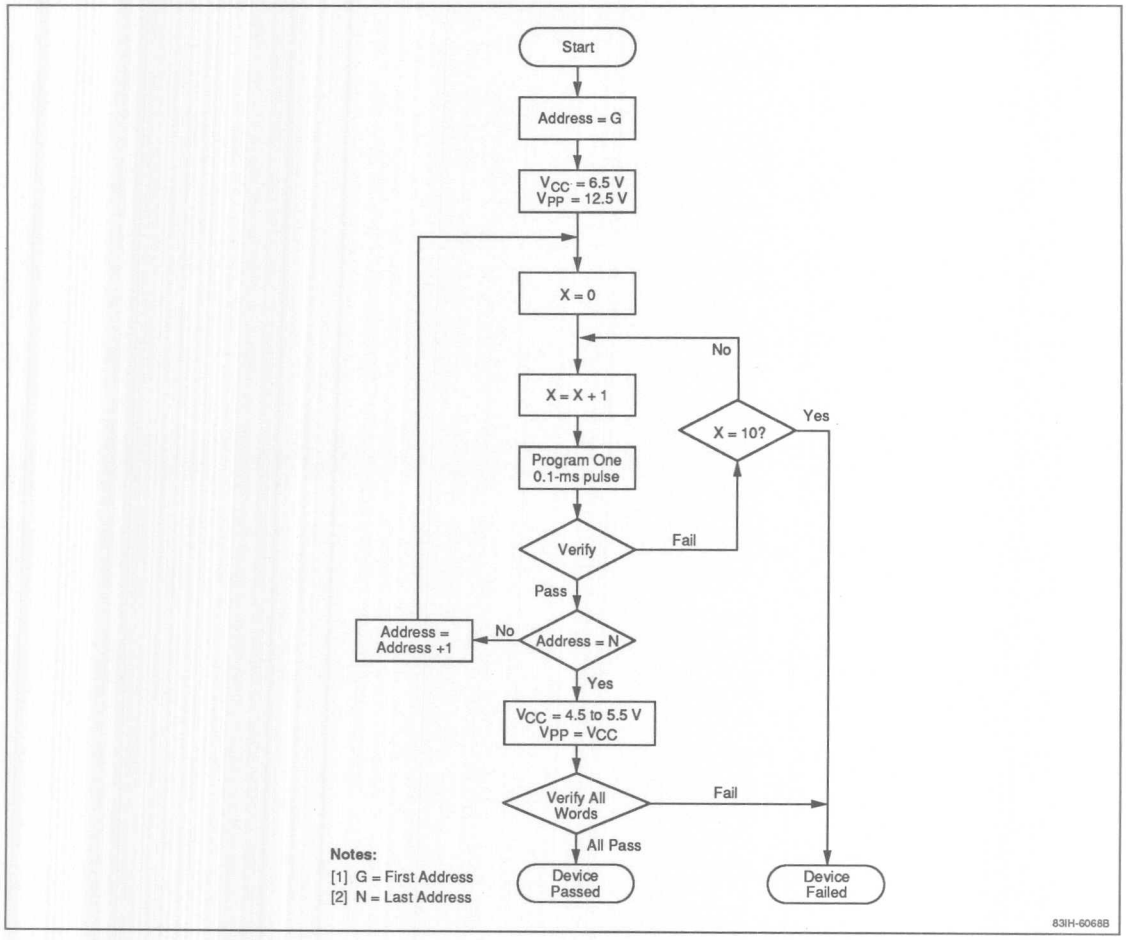
[2] V_{PP} must not be greater than +13.5 V, including overshoot.

[3] Removing and reinserting the device while a voltage of 12.5 V is applied to pin V_{PP} may affect device reliability.

[4] The output lines are also used for data input when programming the device.

83TB-6058B

Figure 3. Byte Programming Flowchart



NEC Electronics Inc.

μPD27C1001A
131,072 x 8-Bit
CMOS UV EPROM

Description

The μPD27C1001A is a 1,048,576-bit ultraviolet erasable and electrically programmable read-only memory (EPROM) fabricated with double-polysilicon CMOS technology for a substantial savings in both operating and standby power. The device is organized as 131,072 words by 8 bits and operates from a single +5-volt power supply.

The μPD27C1001A has both page and single-location programming features, three-state outputs, fully TTL-compatible inputs and outputs, and a program voltage (V_{PP}) of 12.5 volts.

The μPD27C1001A is available in a 32-cerdip with a quartz window.

Features

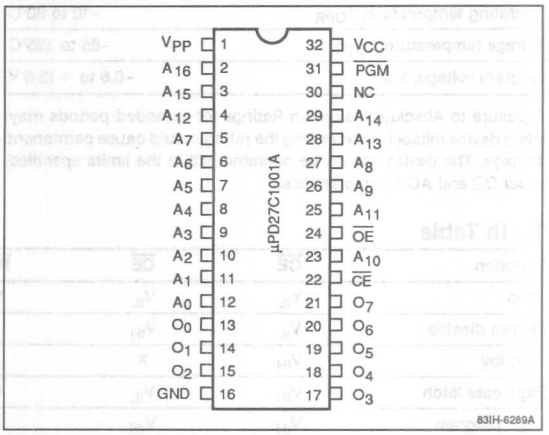
- 131,072-word x 8-bit organization
- Ultraviolet erasable and electrically programmable
- High-speed byte or page programming
- Low power dissipation
  - 40 mA active (max)
  - 100 μA standby (max)
- TTL-compatible I/O for reading and programming
- Single +5-volt power supply
- Double-polysilicon CMOS technology
- 32-pin cerdip packaging
- JEDEC-compatible pinout

Ordering Information

Part Number	Access Time (max)	Package
μPD27C1001AD-12	120 ns	32-pin cerdip with a quartz window
D-15	150 ns	
D-20	200 ns	

Pin Configuration

32-Pin Cerdip



Pin Identification

Symbol	Function
A_0 - A_{16}	Address inputs
O_0 - O_7	Data outputs
$\overline{CE}$	Chip enable
$\overline{OE}$	Output enable
$\overline{PGM}$	Program
GND	Ground
V_{CC}	+5-volt power supply
V_{PP}	Program voltage
NC	No connection

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New WSOP package will be available in 1991.

Absolute Maximum Ratings

Power supply voltage, V_{CC}	−0.6 to +7.0 V
Input voltage, V_{IN}	−0.6 to +7.0 V
Input voltage, A_9	−0.6 to +13.5 V
Output voltage, V_{OUT}	−0.6 to +7.0 V
Operating temperature, T_{OPR}	−10 to 80°C
Storage temperature, T_{STG}	−65 to 125°C
Program voltage, V_{PP}	−0.6 to +13.5 V

Exposure to Absolute Maximum Ratings for extended periods may affect device reliability; exceeding the ratings could cause permanent damage. The device should be operated within the limits specified under DC and AC Characteristics.

Capacitance

T_A = 25°C; f = 1 MHz; V_{IN} and V_{OUT} = 0 V

Parameter	Symbol	Min	Typ	Max	Unit
Input capacitance	C_I			14	pF
Output capacitance	C_O			16	pF

Truth Table

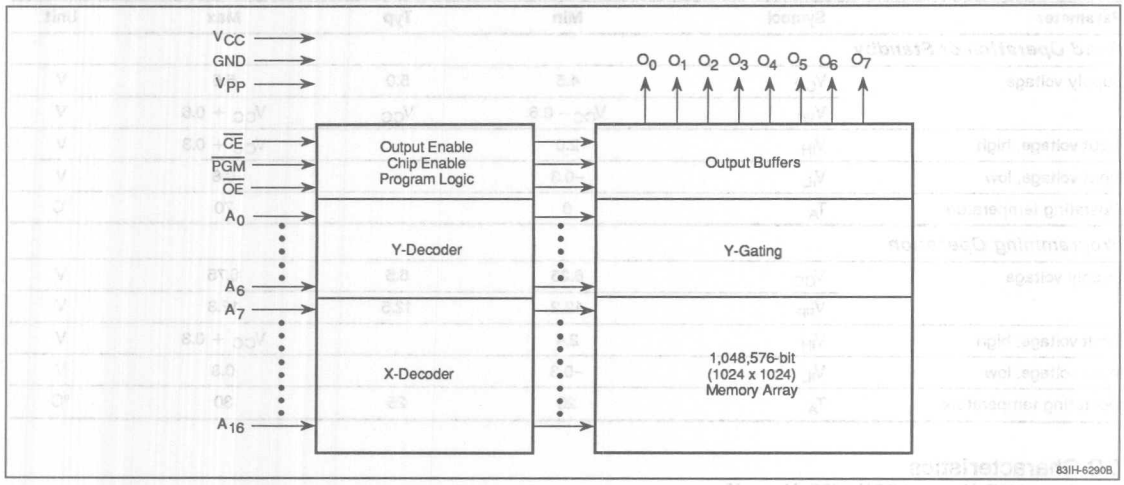
Function	$\overline{CE}$	$\overline{OE}$	$\overline{PGM}$	V_{PP}	V_{CC}	Output
Read	V_{IL}	V_{IL}	V_{IH}	+5.0 V	+5.0 V	D_{OUT}
Output disable	V_{IL}	V_{IH}	X	+5.0 V	+5.0 V	High-Z
Standby	V_{IH}	X	X	+5.0 V	+5.0 V	High-Z
Page data latch	V_{IH}	V_{IL}	V_{IH}	+12.5 V	+6.5 V	D_{IN}
Page program	V_{IH}	V_{IH}	V_{IL}	+12.5 V	+6.5 V	High-Z
Byte program	V_{IL}	V_{IH}	V_{IL}	+12.5 V	+6.5 V	D_{IN}
Program verify	V_{IL}	V_{IL}	V_{IH}	+12.5 V	+6.5 V	D_{OUT}
Program inhibit	X	V_{IL}	V_{IL}	+12.5 V	+6.5 V	High-Z
	X	V_{IH}	V_{IH}			

Notes:

(1) X can be either V_{IL} or V_{IH}.

(2) In read operation, $\overline{PGM}$ must be sent to V_{IH} at all times, or switched from V_{IL} to V_{IH} at least 2 μs before $\overline{OE}$ or $\overline{CE}$ goes to V_{IH}.

Block Diagram



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Recommended Operating Conditions

Parameter	Symbol	Min	Typ	Max	Unit
Read Operation or Standby					
Supply voltage	V_{CC}	4.5	5.0	5.5	V
	V_{PP}	V_{CC} – 0.6	V_{CC}	V_{CC} + 0.6	V
Input voltage, high	V_{IH}	2.0		V_{CC} + 0.3	V
Input voltage, low	V_{IL}	–0.3		0.8	V
Operating temperature	T_A	0		70	°C
Programming Operation					
Supply voltage	V_{CC}	6.25	6.5	6.75	V
	V_{PP}	12.2	12.5	12.8	V
Input voltage, high	V_{IH}	2.4		V_{CC} + 0.3	V
Input voltage, low	V_{IL}	–0.3		0.8	V
Operating temperature	T_A	20	25	30	°C

DC Characteristics

T_A = 0 to +70°C; V_{CC} = +5.0 V ±10%; V_{PP} = V_{CC}

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions
Read Operation or Standby						
Output voltage, high	V_{OH1}	2.4			V	I_{OH} = –400 μA
	V_{OH2}	V_{CC} – 0.7			V	I_{OH} = –100 μA
Output voltage, low	V_{OL}			0.45	V	I_{OL} = 2.1 mA
Output leakage current	I_{LO}	–10		10	μA	V_{OUT} = 0 V to V_{CC}; $\overline{OE}$ = V_{IH}
Input leakage current	I_{LI}	–10		10	μA	V_{IN} = 0 V to V_{CC}
V_{PP} current	I_{PP}		1	100	μA	V_{PP} = V_{CC}
V_{CC} current (active)	I_{CCA1}			15	mA	$\overline{CE}$ = V_{IL}; V_{IN} = V_{IH}
	I_{CCA2}			40	mA	f = 8.4 MHz; I_{OUT} = 0 mA; t_{ACC} = 120 ns
				30	mA	f = 6.7 MHz; I_{OUT} = 0 mA; t_{ACC} = 150 ns
				25	mA	f = 5 MHz; I_{OUT} = 0 mA; t_{ACC} = 200 ns
V_{CC} current (standby)	I_{CCS1}			1	mA	$\overline{CE}$ = V_{IH} min
	I_{CCS2}		1	100	μA	$\overline{CE}$ = V_{CC}; V_{IN} = 0 V to V_{CC}

DC Characteristics (cont)

T_A = 25 ±5°C; V_{CC} = +6.5 V ±0.25; V_{PP} = +12.5 V ± 0.3

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions
Programming Operation						
Output voltage, high	V_{OH}	2.4			V	I_{OH} = –400 μA
Output voltage, low	V_{OL}			0.45	V	I_{OL} = 2.1 mA
Input leakage current	I_{LI}	–10		10	μA	V_{IN} = 0 V to V_{CC}
V_{PP} current	I_{PP}			50	mA	$\overline{CE}$ = $\overline{PGM}$ = V_{IL}
V_{CC} current	I_{CC}			30	mA	

AC Characteristics

T_A = 0 to +70°C; V_{CC} = +5.0 V ± 10%; V_{PP} = V_{CC} ± 0.6 V

		μPD27C1001A-12		μPD27C1001A-15		μPD27C1001A-20			
Parameter	**Symbol**	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**	**Unit**	**Test Conditions**
Read Operation or Standby									
Address to output delay	t_{ACC}		120		150		200	ns	$\overline{CE}$ = $\overline{OE}$ = V_{IL}
$\overline{CE}$ to output delay	t_{CE}		120		150		200	ns	$\overline{OE}$ = V_{IL}
$\overline{OE}$ to output delay	t_{OE}		70		70		75	ns	$\overline{CE}$ = V_{IL}
$\overline{OE}$ high to output float	t_{DF}	0	50	0	50	0	60	ns	$\overline{CE}$ = V_{IL} or $\overline{OE}$ = V_{IL}
Address to output hold	t_{OH}	0		0		0		ns	$\overline{CE}$ = $\overline{OE}$ = V_{IL}

AC Characteristics (cont)

T_A = 25 ± 5°C; V_{CC} = +6.5 ± 0.25 V; V_{PP} = +12.5 ± 0.3 V

Parameter	**Symbol**	**Min**	**Typ**	**Max**	**Unit**	**Test Conditions**
Page Programming Operation						
Address setup time	t_{AS}	2			μs	
$\overline{CE}$ setup time	t_{CES}	2			μs	
Data setup time	t_{DS}	2			μs	
Address hold time	t_{AH}	2			μs	
	t_{AHL}	2			μs	
	t_{AHV}	0			μs	
Data hold time	t_{DH}	2			μs	
$\overline{OE}$ to output float time	t_{DF}	0		130	ns	
V_{PP} setup time	t_{VPS}	2			μs	
V_{CC} setup time	t_{VCS}	2			μs	
Program pulse width	t_{PW}	0.095	0.1	0.105	ms	
$\overline{OE}$ setup time	t_{OES}	2			μs	
$\overline{OE}$ to output delay	t_{OE}			150	ns	
$\overline{OE}$ pulse width during data latch	t_{LW}	1			μs	
$\overline{PGM}$ setup time	t_{PGMS}	2			μs	
$\overline{CE}$ hold time	t_{CEH}	2			μs	
OE hold time	t_{OEH}	2			μs	

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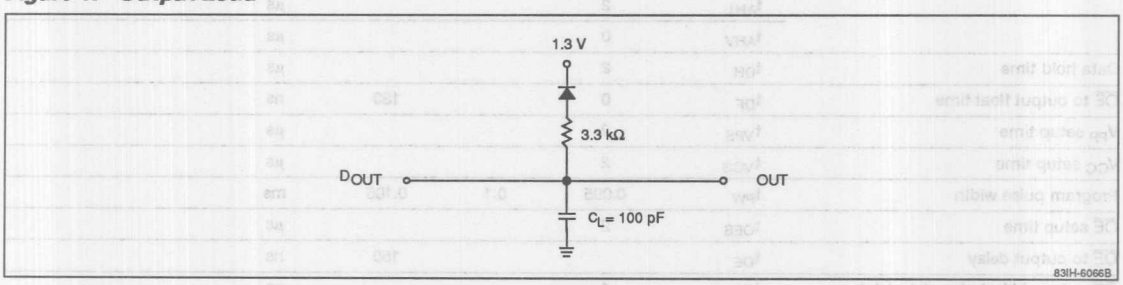
AC Characteristics (cont)

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions
Byte Programming Operation						
Address setup time	t_{AS}	2			μs	
$\overline{OE}$ setup time	t_{OES}	2			μs	
Data setup time	t_{DS}	2			μs	
Address hold time	t_{AH}	2			μs	
Data hold time	t_{DH}	2			μs	
$\overline{OE}$ to output float time	t_{DF}	0		130	ns	
V_{PP} setup time	t_{VPS}	2			μs	
V_{CC} setup time	t_{VCS}	2			μs	
Program pulse width	t_{PW}	0.095	0.1	0.105	ms	
$\overline{CE}$ setup time	t_{CES}	2			μs	
$\overline{OE}$ to output delay	t_{OE}			150	ns	

Notes:

(1) Input pulse levels = 0.45 to 2.4 V; input and output timing reference levels = 0.8 and 2.0 V; input rise and fall times ≤ 20 ns. See figure 1 for output load.

Figure 1. Output Load



Programming Operation

Begin programming by erasing all data; this sets all bits high. The μPD27C1001A is originally shipped in this condition. Address the first byte or page location and apply valid data at the eight output pins. Raise V_{CC} to +6.5 ±0.25 V; then raise V_{PP} to +12.5 ±0.3 V.

Byte Programming

$\overline{CE}$ should be set low and $\overline{OE}$ high to start programming at the initial byte address. Apply a 0.1 ms program pulse to $\overline{PGM}$ as shown in the byte programming portion of the timing waveforms. Set $\overline{OE}$ low to verify the eight bits prior to making a program/no program decision. If the byte is not programmed, apply another 0.1-ms pulse to $\overline{PGM}$, up to a maximum of 10 times, and input the next address. If the bits are not programmed in 10 tries, reject the device as a program failure. After all addresses are programmed, lower both V_{CC} and V_{PP} to +5.0 V ±10% and verify all data again.

Page Programming

For page programming, $\overline{CE}$ and $\overline{PGM}$ should be set high. $\overline{OE}$ pulses low four times to latch each of the 4 data bytes onto the page. Subsequently, $\overline{CE}$ and $\overline{OE}$ should be set high and a 0.1-ms program pulse applied to $\overline{PGM}$ as shown in the page programming portion of the timing waveforms. Verify the data prior to making a program/no program decision. If all four bytes of page data are not programmed, apply another 0.1-ms pulse to $\overline{PGM}$, up to a maximum of 10 times, and input the next page address. If the page is not programmed in 10 tries, reject the device as a program failure. After all addresses are programmed, lower both V_{CC} and V_{PP} to +5.0 V ±10% and verify all data again.

Program Inhibit

Use the program inhibit option to program multiple μPD27C1001As connected in parallel. All like inputs (except $\overline{CE}$, but including $\overline{OE}$) may be common. Program individual devices by applying a low-level TTL pulse to the $\overline{CE}$ input of the device to be programmed. Applying a high level to the $\overline{CE}$ input of the other devices prevents them from being programmed.

Program Verification

To verify that the device is correctly programmed, normal read cycles can be executed with a high logic level applied to the $\overline{PGM}$ pin and a low logic level applied to the $\overline{CE}$ and $\overline{OE}$ pins of the device to be verified. The $\overline{CE}$ and $\overline{OE}$ pins of all other devices should be set high.

Program Erasure

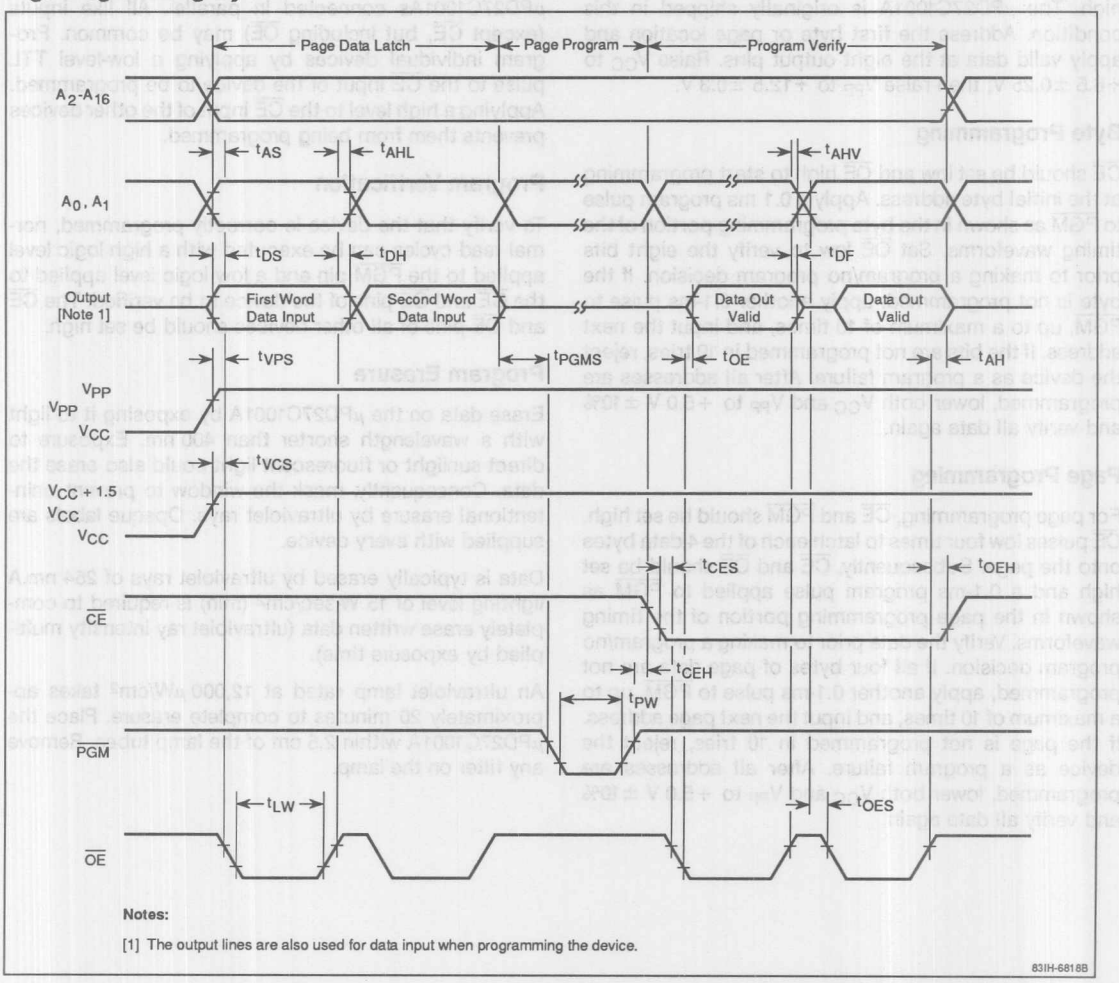
Erase data on the μPD27C1001A by exposing it to light with a wavelength shorter than 400 nm. Exposure to direct sunlight or fluorescent light could also erase the data. Consequently, mask the window to prevent unintentional erasure by ultraviolet rays. Opaque labels are supplied with every device.

Data is typically erased by ultraviolet rays of 254 nm.A lighting level of 15 W-sec/cm^2 (min) is required to completely erase written data (ultraviolet ray intensity multiplied by exposure time).

An ultraviolet lamp rated at 12,000 μW/cm^2 takes approximately 20 minutes to complete erasure. Place the μPD27C1001A within 2.5 cm of the lamp tubes. Remove any filter on the lamp.

Timing Waveforms

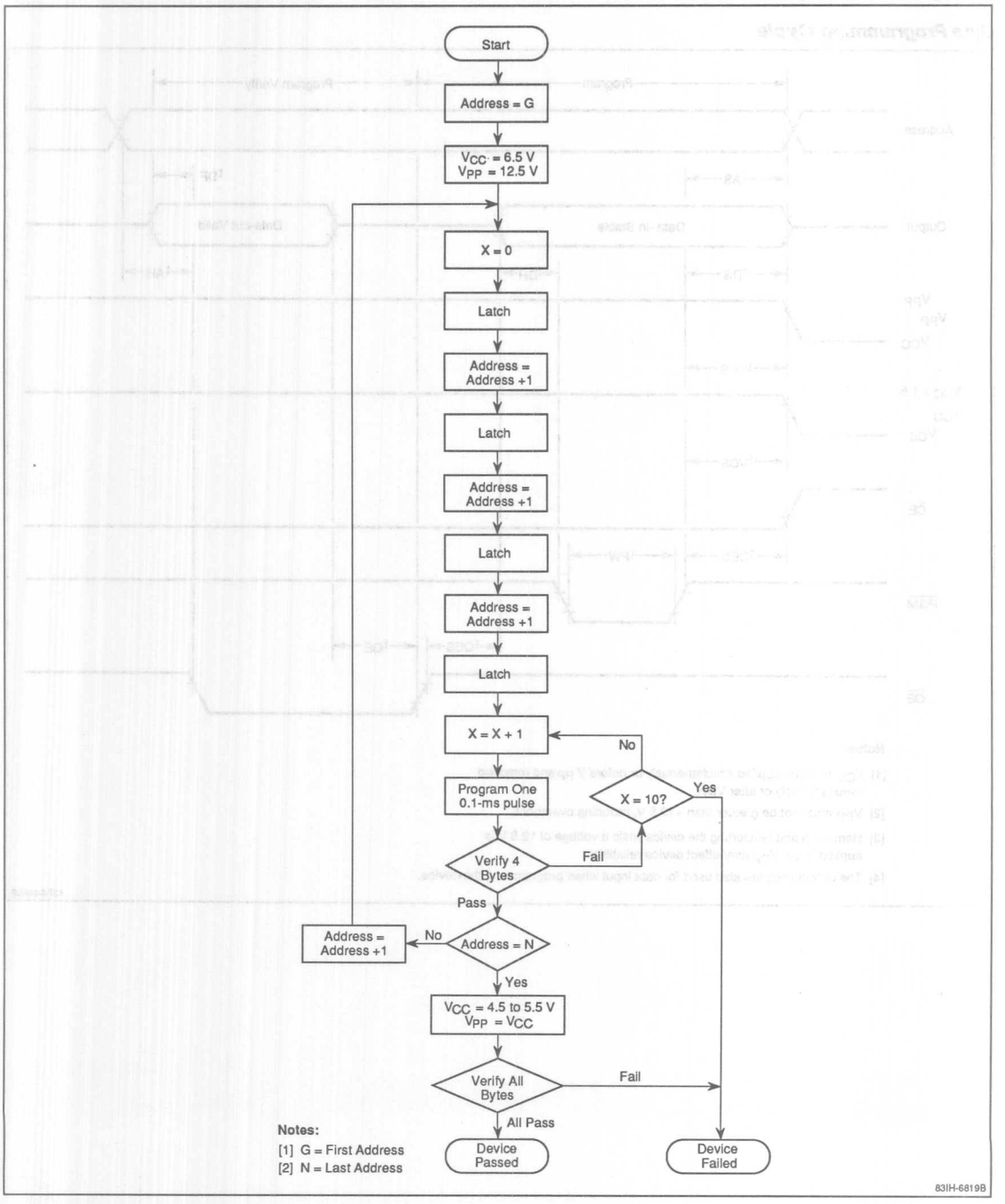
Page Programming Cycle



Notes:

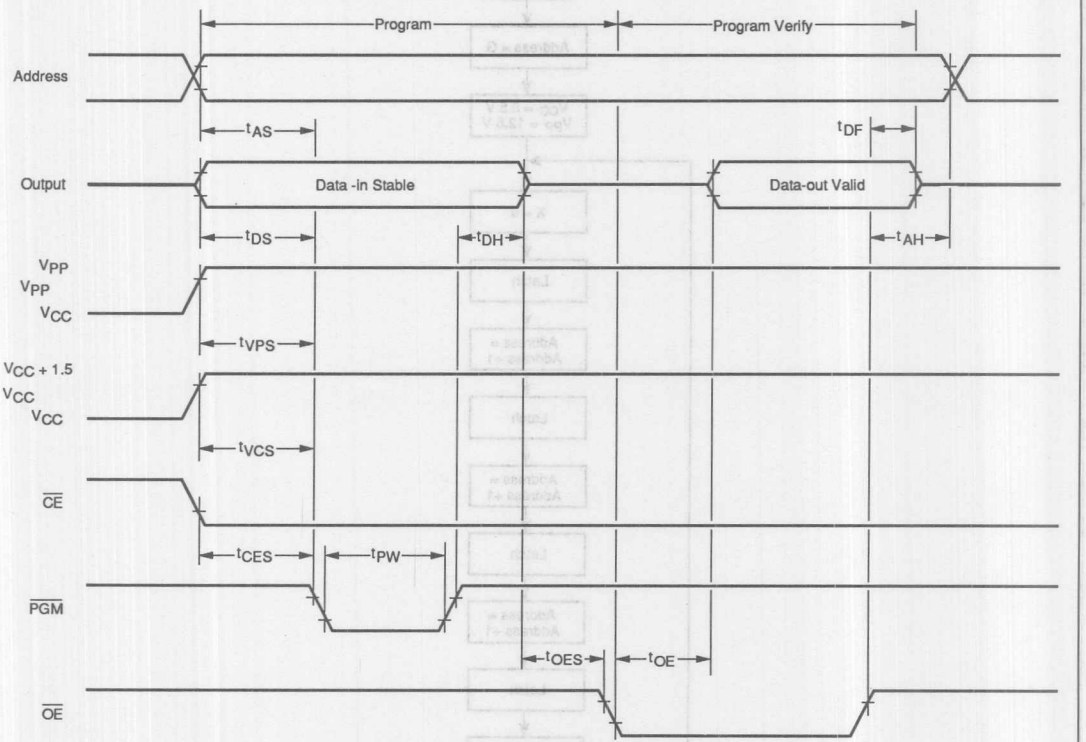
[1] The output lines are also used for data input when programming the device.

Figure 2. Page Programming Flowchart



Timing Waveforms (cont)

Byte Programming Cycle



Notes:

[1] V_{CC} must be applied simultaneously or before V_{PP} and removed simultaneously or after V_{PP}.

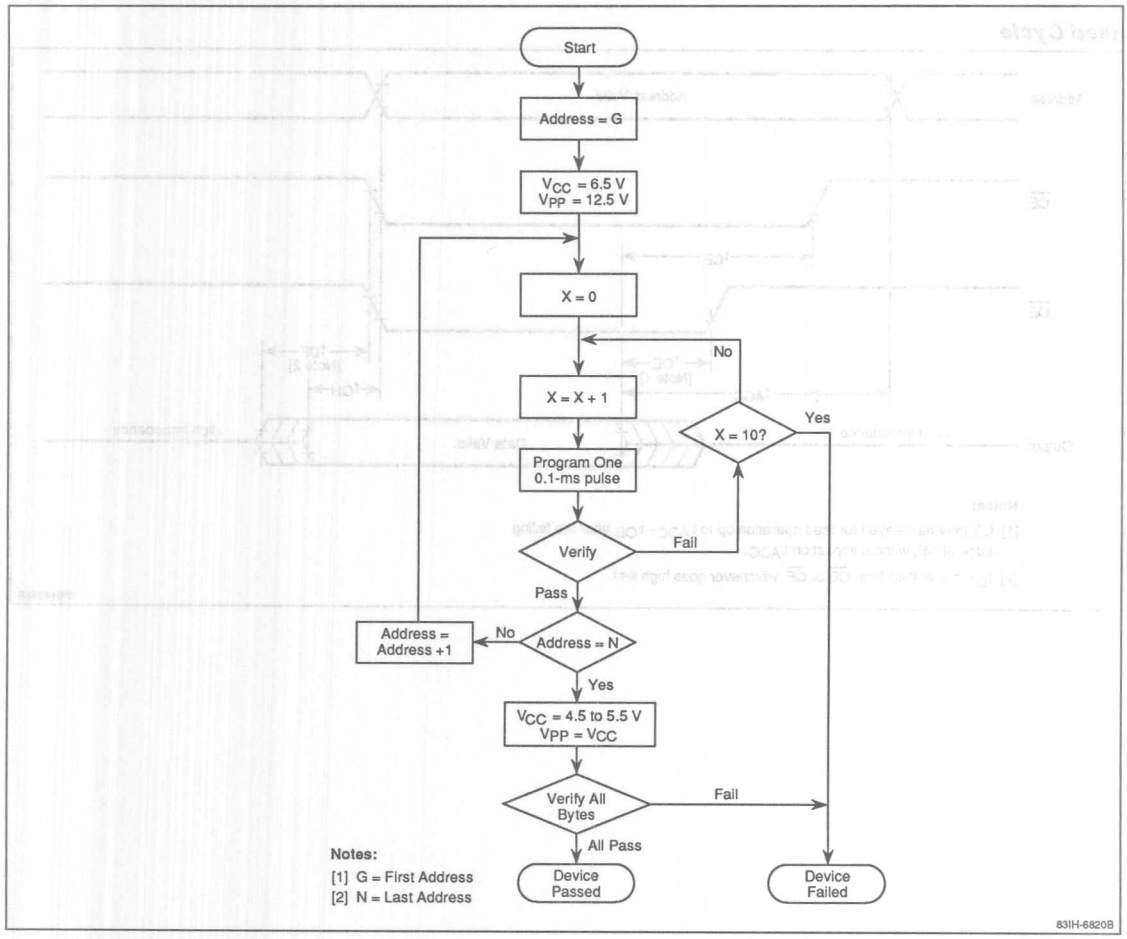
[2] V_{PP} must not be greater than +13.5 V, including overshoot.

[3] Removing and reinserting the device while a voltage of 12.5 V is applied to pin V_{PP} may affect device reliability.

[4] The output lines are also used for data input when programming the device.

83TB-6058B

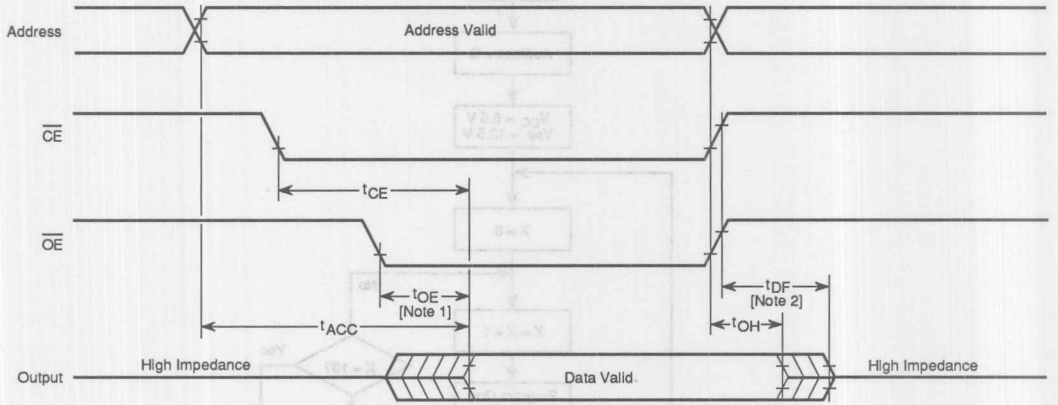
Figure 3. Byte Programming Flowchart



9

Timing Waveforms

Read Cycle



Notes:

[1] $\overline{OE}$ may be delayed for read operation up to $t_{ACC} - t_{OE}$ after the falling edge of $\overline{CE}$, without impact on t_{ACC}.

[2] t_{DF} is specified from $\overline{OE}$ or $\overline{CE}$, whichever goes high first.

83IH-6286B

NEC Electronics Inc.

μPD27C1024A
65,536 x 16-Bit
CMOS UV EPROM

Description

The μPD27C1024A is a 1,048,576-bit ultraviolet erasable and electrically programmable ROM fabricated with an advanced CMOS process for substantial power savings. The device is organized as 65,536 words by 16 bits and operates from a single + 5-volt power supply. All inputs and outputs are TTL-compatible.

The μPD27C1024A is available in a 40-pin ceramic DIP with quartz window.

Features

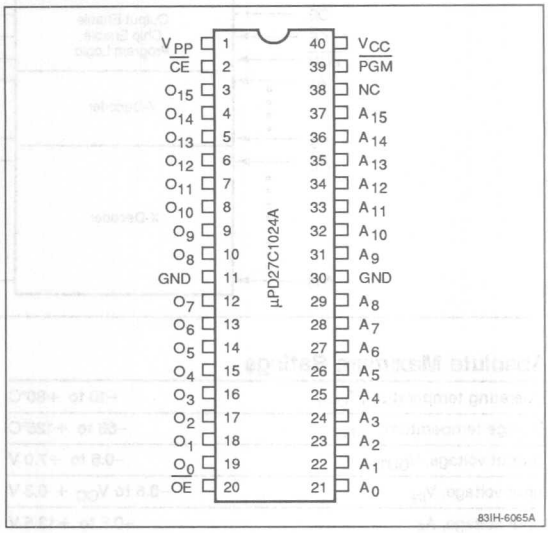
- 65,536 x 16-bit organization
- Ultraviolet erasable and electrically programmable
- High-speed word and page programming
- Low power dissipation
  - 50 mA max (active)
  - 100 μA max (standby)
- TTL-compatible inputs and outputs
- Three-state outputs
- Single + 5-volt power supply
- Advanced CMOS technology
- 40-pin cerdip packaging with quartz window

Ordering Information

Part Number		Access Time (max)	Package
μPD27C1024AD-12		120 ns	40-pin cerdip with quartz window
	D-15	150 ns	
	D-20	200 ns	

Pin Configuration

40-Pin Cerdip

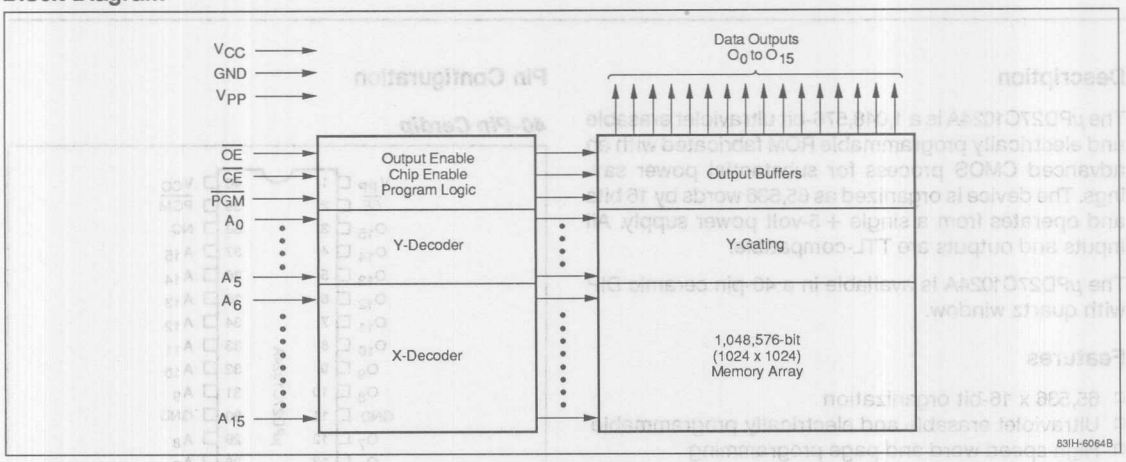


Pin Identification

Symbol	Function
A_0 - A_{15}	Address inputs
O_0 - O_{15}	Data outputs
$\overline{CE}$	Chip enable
$\overline{OE}$	Output enable
$\overline{PGM}$	Program
GND	Ground
V_{CC}	+5-volt power supply
V_{PP}	Program voltage
NC	No connection

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Block Diagram



Absolute Maximum Ratings

Operating temperature, T_{OPR}	−10 to +80°C
Storage temperature, T_{STG}	−65 to +125°C
Output voltage, V_{OUT}	−0.6 to +7.0 V
Input voltage, V_{IN}	−0.6 to V_{CC} + 0.3 V
Input voltage, A_9	−0.6 to +13.5 V
Supply voltage, V_{CC}	−0.6 to +7.0 V
Supply voltage, V_{PP}	−0.6 to +13.5 V

Exposure to Absolute Maximum Ratings for extended periods may affect device reliability; exceeding the ratings could cause permanent damage. The device should be operated within the limits specified under DC and AC Characteristics.

Capacitance

T_A = 25°C; f = 1 MHz; V_{IN} and V_{OUT} = 0 V

Parameter	Symbol	Min	Typ	Max	Unit
Input capacitance	C_{IN}			14	pF
Output capacitance	C_{OUT}			16	pF

Truth Table

Function	$\overline{CE}$	$\overline{OE}$	$\overline{PGM}$	V_{PP}	V_{CC}	Outputs
Read	V_{IL}	V_{IL}	V_{IH}	5.0 V	5.0 V	D_{OUT}
Output disable	V_{IL}	V_{IH}	X	5.0 V	5.0 V	High-Z
Standby	V_{IH}	X	X	5.0 V	5.0 V	High-Z
Page data latch	V_{IH}	V_{IL}	V_{IH}	12.5 V	6.5 V	D_{IN}
Page program	V_{IH}	V_{IH}	V_{IL}	12.5 V	6.5 V	High-Z
Word program	V_{IL}	V_{IH}	V_{IL}	12.5 V	6.5 V	D_{IN}
Program verify	V_{IL}	V_{IL}	V_{IH}	12.5 V	6.5 V	D_{OUT}
Program inhibit	X	V_{IL}	V_{IL}	12.5 V	6.5 V	High-Z
	X	V_{IH}	V_{IH}			

Notes:

(1) X = V_{IL} or V_{IH}.

(2) In read operation, $\overline{PGM}$ must be set to V_{IH} at all times, or for at least 2 μs before $\overline{OE}$ or $\overline{CE}$ returns to V_{IH}.

Recommended Operating Conditions

Parameter	Symbol	Min	Typ	Max	Unit
Read Operation or Standby					
Supply voltage	V_{CC}	4.5	5.0	5.5	V
	V_{PP}	V_{CC} – 0.6	V_{CC}	V_{CC} + 0.6	V
Input voltage, high	V_{IH}	2.0		V_{CC} + 0.3	V
Input voltage, low	V_{IL}	–0.3		0.8	V
Operating temperature	T_A	0		70	°C
Programming Operation					
Supply voltage	V_{CC}	6.25	6.5	6.75	V
	V_{PP}	12.2	12.5	12.8	V
Input voltage, high	V_{IH}	2.0		V_{CC} + 0.3	V
Input voltage, low	V_{IL}	–0.3		0.8	V
Operating temperature	T_A	20	25	30	°C

DC Characteristics

T_A = 0 to +70°C; V_{CC} = +5.0 V ± 10%; V_{PP} = V_{CC} ± 0.6 V

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions
Read Operation						
Output voltage, high	V_{OH1}	2.4			V	I_{OH} = –400 μA
	V_{OH2}	V_{CC} – 0.7			V	I_{OH} = –100 μA
Output voltage, low	V_{OL}			0.45	V	I_{OL} = 2.1 mA
Output leakage current	I_{LO}	–10		10	μA	V_{OUT} = 0 to V_{CC}; $\overline{OE}$ = V_{IH}
Input leakage current	I_{LI}	–10		10	μA	V_{IN} = 0 to V_{CC}
V_{PP} current	I_{PP}		1	100	μA	V_{PP} = V_{CC}
V_{CC} current (active)	I_{CCA1}			15	mA	$\overline{CE}$ = V_{IL}; V_{IN} = V_{IH}
	I_{CCA2}			50	mA	f = 8.4 MHz; I_{OUT} = 0 mA
V_{CC} current (standby)	I_{CCS1}			1	mA	$\overline{CE}$ = V_{IH} min
	I_{CCS2}		1	100	μA	$\overline{CE}$ ≥ V_{CC} – 0.2 V; V_{IN} = 0 to V_{CC}

DC Characteristics (cont)

T_A = 25 ± 5°C; V_{CC} = +6.5 V ± 0.25; V_{PP} = +12.5 V ± 0.3

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions
Programming Operation						
Output voltage, high	V_{OH}	2.4			V	I_{OH} = –400 μA
Output voltage, low	V_{OL}			0.45	V	I_{OL} = 2.1 mA
Input leakage current	I_{LI}	–10		10	μA	V_{IN} = 0 to V_{CC}
V_{PP} current	I_{PP}			50	mA	$\overline{CE}$ = $\overline{PGM}$ = V_{IL}
V_{CC} current	I_{CC}			30	mA	

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AC Characteristics

T_A = 0 to +70°C; V_{CC} = +5.0 V ± 10%; V_{PP} = V_{CC} ± 0.6 V

		μPD27C1024A-12		μPD27C1024A-15		μPD27C1024A-20			
Parameter	**Symbol**	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**	**Unit**	**Test Conditions**
Read Operation									
Address to output delay	t_{ACC}		120		150		200	ns	$\overline{CE}$ = $\overline{OE}$ = V_{IL}
$\overline{CE}$ to output delay	t_{CE}		120		150		200	ns	$\overline{OE}$ = V_{IL}
$\overline{OE}$ to output delay	t_{OE}		60		70		70	ns	$\overline{CE}$ = V_{IL}
$\overline{OE}$ high to output float	t_{DF}	0	50	0	55	0	55	ns	$\overline{CE}$ = V_{IL}
Address to output hold	t_{OH}	0		0		0		ns	$\overline{CE}$ = $\overline{OE}$ = V_{IL}

AC Characteristics (cont)

T_A = 25 ± 5°C; V_{CC} = +6.5 V ± 0.25; V_{PP} = +12.5 V ± 0.3

Parameter	**Symbol**	**Min**	**Typ**	**Max**	**Unit**	**Test Conditions**
Page Programming Operation						
Address setup time	t_{AS}	2			μs	
$\overline{CE}$ setup time	t_{CES}	2			μs	
Data setup time	t_{DS}	2			μs	
Address hold time	t_{AH}	2			μs	
	t_{AHL}	2			μs	
	t_{AHV}	0			μs	
Data hold time	t_{DH}	2			μs	
$\overline{OE}$ to output float time	t_{DF}	0		130	ns	
V_{PP} setup time	t_{VPS}	2			μs	
V_{CC} setup time	t_{VCS}	2			μs	
Program pulse width	t_{PW}	0.095	0.1	0.105	ms	
$\overline{OE}$ setup time	t_{OES}	2			μs	
$\overline{OE}$ to output delay	t_{OE}			150	ns	
$\overline{OE}$ pulse width during data latch	t_{LW}	1			μs	
$\overline{PGM}$ setup time	t_{PGMS}	2			μs	
$\overline{CE}$ hold time	t_{CEH}	2			μs	
OE hold time	t_{OEH}	2			μs	

AC Characteristics (cont)

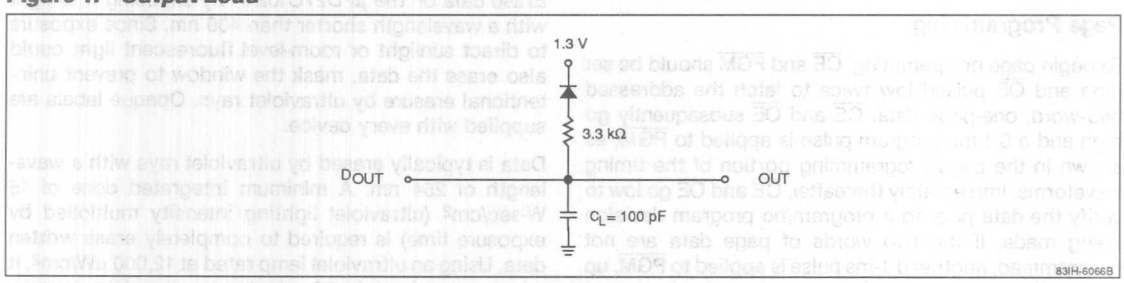
T_A = 25 ± 5°C; V_{CC} = +6.5 V ± 0.25; V_{PP} = +12.5 V ± 0.3

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions
Word Programming Operation						
Address setup time	t_{AS}	2			μs	
$\overline{OE}$ setup time	t_{OES}	2			μs	
Data setup time	t_{DS}	2			μs	
Address hold time	t_{AH}	2			μs	
Data hold time	t_{DH}	2			μs	
$\overline{OE}$ to output float time	t_{DF}	0		130	ns	
V_{PP} setup time	t_{VPS}	2			μs	
V_{CC} setup time	t_{VCS}	2			μs	
Program pulse width	t_{PW}	0.095	0.1	0.105	ms	
$\overline{CE}$ setup time	t_{CES}	2			μs	
$\overline{OE}$ to output delay	t_{OE}			150	ns	

Notes:

(1) Input pulse levels = 0.45 to 2.4 V; input and output timing reference levels = 0.8 and 2.0 V; input rise and fall times ≤ 20 ns. See figure 1 for output load.

Figure 1. Output Load



9

PROGRAMMING

Before programming the μPD27C1024A, erase all data; this sets all data bits high. The μPD27C1024A is originally shipped in this condition. To begin programming, first raise V_{CC} to +6.5 V ± 0.25, and then raise V_{PP} to 12.5 V ± 0.3. At this point, data to be programmed can be directly input in 16-bit format through the data bus. Programming causes relevant bits to go low.

Word Programming

For word programming, $\overline{CE}$ should be set low and $\overline{OE}$ high to start programming at the initial address. A 0.1-ms pulse is applied to $\overline{PGM}$, as shown in the word programming portion of the timing waveforms, and $\overline{OE}$ goes low to verify the 16 bits prior to making a program/no program decision. If the word is not programmed, another 0.1-ms pulse is applied to $\overline{PGM}$, up to a maximum of 10 times, before the next address is input. If the bits are not programmed in 10 tries, reject the device as a program failure.

After all addresses are programmed, lower both V_{CC} and V_{PP} to +5.0 V ± 10% and verify all data again.

Page Programming

To begin page programming, $\overline{CE}$ and $\overline{PGM}$ should be set high and $\overline{OE}$ pulsed low twice to latch the addressed two-word, one-page data. $\overline{CE}$ and $\overline{OE}$ subsequently go high and a 0.1-ms program pulse is applied to $\overline{PGM}$, as shown in the page programming portion of the timing waveforms. Immediately thereafter, $\overline{CE}$ and $\overline{OE}$ go low to verify the data prior to a program/no program decision being made. If the two words of page data are not programmed, another 0.1-ms pulse is applied to $\overline{PGM}$, up to a maximum of 10 times. If the page is not programmed in 10 tries, reject the device as a program failure.

Program Inhibit

The program inhibit option can be used in either word or page operation to program one of multiple μPD27C1024A devices whose $\overline{CE}$ pins are independent and $\overline{OE}$, V_{PP}, and O_0 through O_{15} pins are connected in parallel. For word programming, $\overline{OE}$ must be high and $\overline{CE}$ of the device to be programmed low. For page programming, both $\overline{OE}$ and $\overline{CE}$ must be high. Applying a low-level TTL pulse to $\overline{PGM}$ of the device to be programmed and a high-level TTL pulse to the $\overline{PGM}$ pins of the other devices enables the one device to be programmed while the others are inhibited.

Program Verification

To verify that the device is correctly programmed, execute a normal read cycle with a high logic level applied to the $\overline{PGM}$ pin and a low logic level applied to the $\overline{CE}$ and $\overline{OE}$ pins of the device to be verified. A high should be applied to the $\overline{CE}$ or $\overline{OE}$ pin of all other devices.

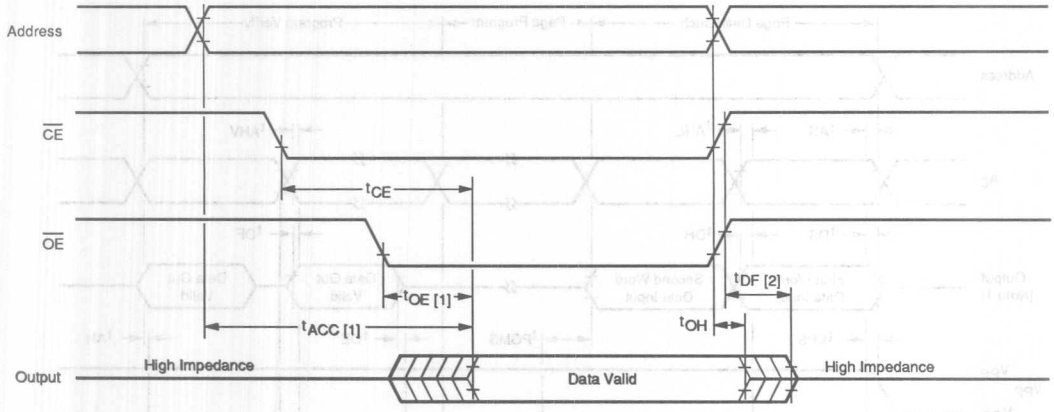
Erasure

Erase data on the μPD27C1024A by exposing it to light with a wavelength shorter than 400 nm. Since exposure to direct sunlight or room-level fluorescent light could also erase the data, mask the window to prevent unintentional erasure by ultraviolet rays. Opaque labels are supplied with every device.

Data is typically erased by ultraviolet rays with a wavelength of 254 nm. A minimum integrated dose of 15 W-sec/cm^2 (ultraviolet lighting intensity multiplied by exposure time) is required to completely erase written data. Using an ultraviolet lamp rated at 12,000 μW/cm^2, it takes approximately 20 minutes to complete erasure. Place the μPD27C1024A within 2.5 cm of the lamp tubes and remove any filter on the lamp.

Timing Waveforms

Read Cycle



Notes:

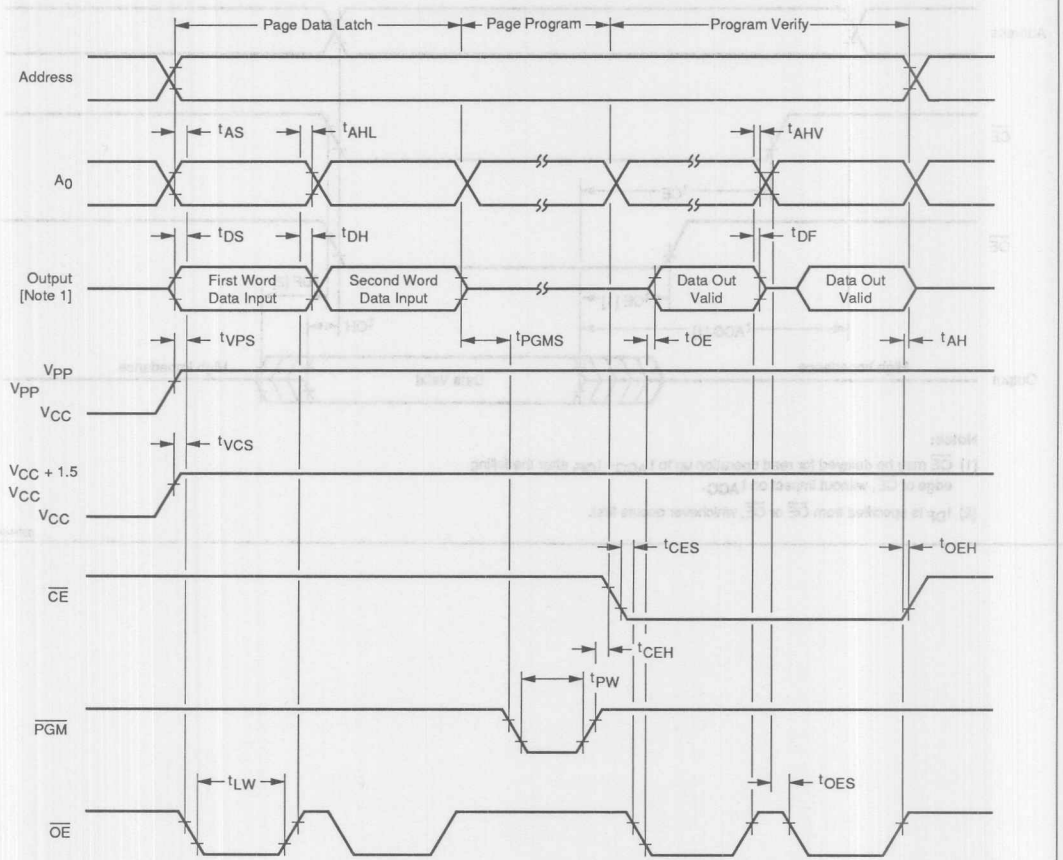
[1] $\overline{OE}$ may be delayed for read operation up to $t_{ACC} - t_{OE}$, after the falling edge of $\overline{CE}$, without impact on t_{ACC}.

[2] t_{DF} is specified from $\overline{OE}$ or $\overline{CE}$, whichever occurs first.

9

Timing Waveforms (cont)

Page Programming Cycle

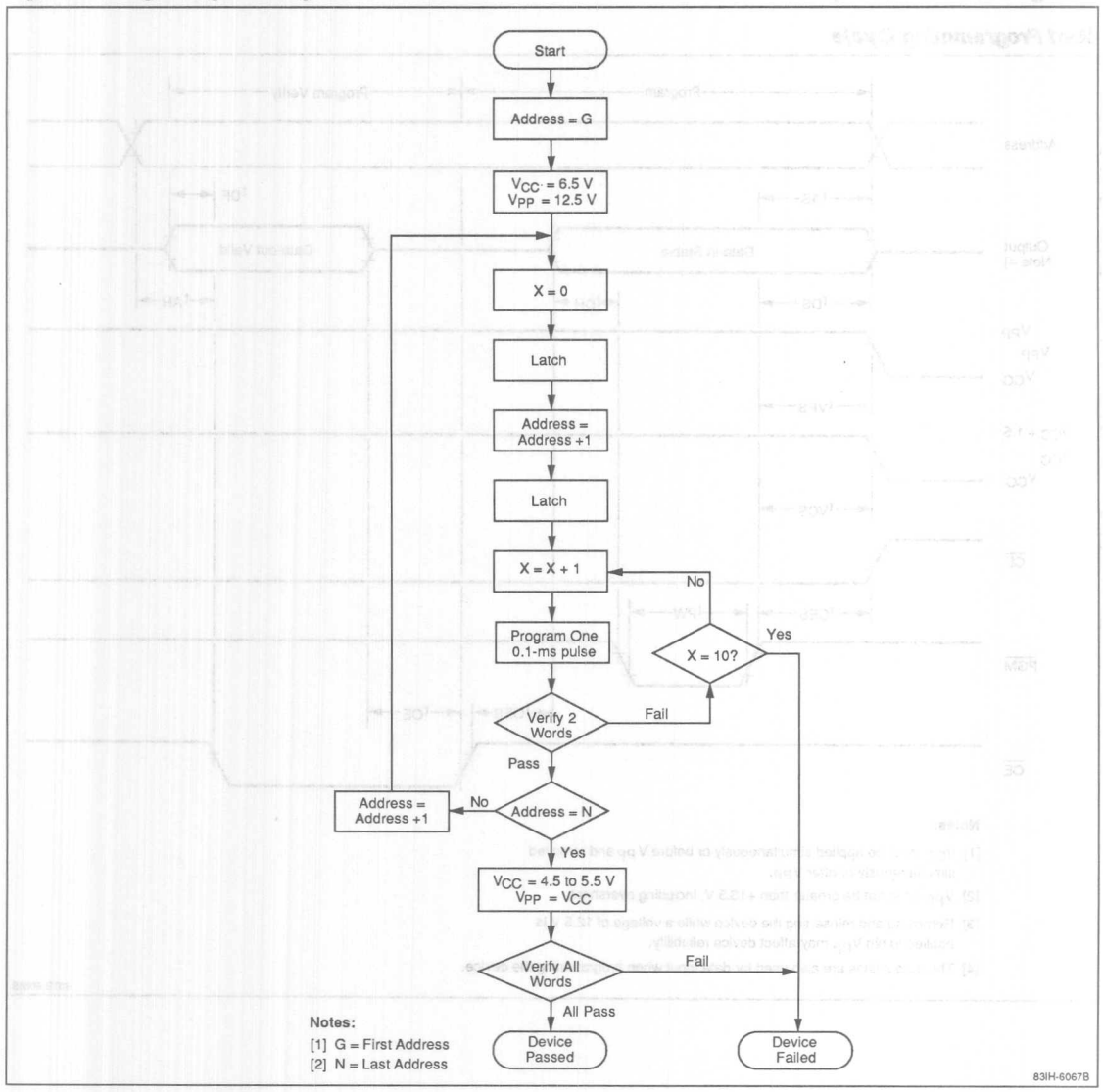


Notes:

[1] The output lines are also used for data input when programming the device.

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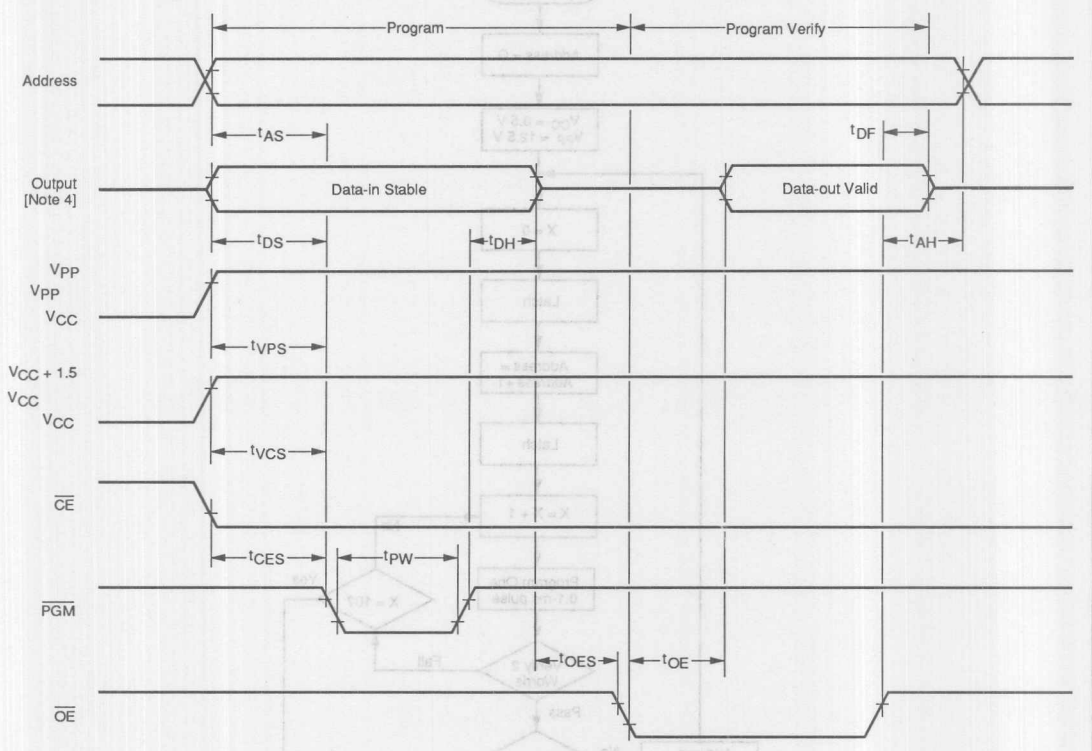
Figure 2. Page Programming Flowchart



9

Timing Waveforms (cont)

Word Programming Cycle



Notes:

[1] V_{CC} must be applied simultaneously or before V_{PP} and removed simultaneously or after V_{PP}.

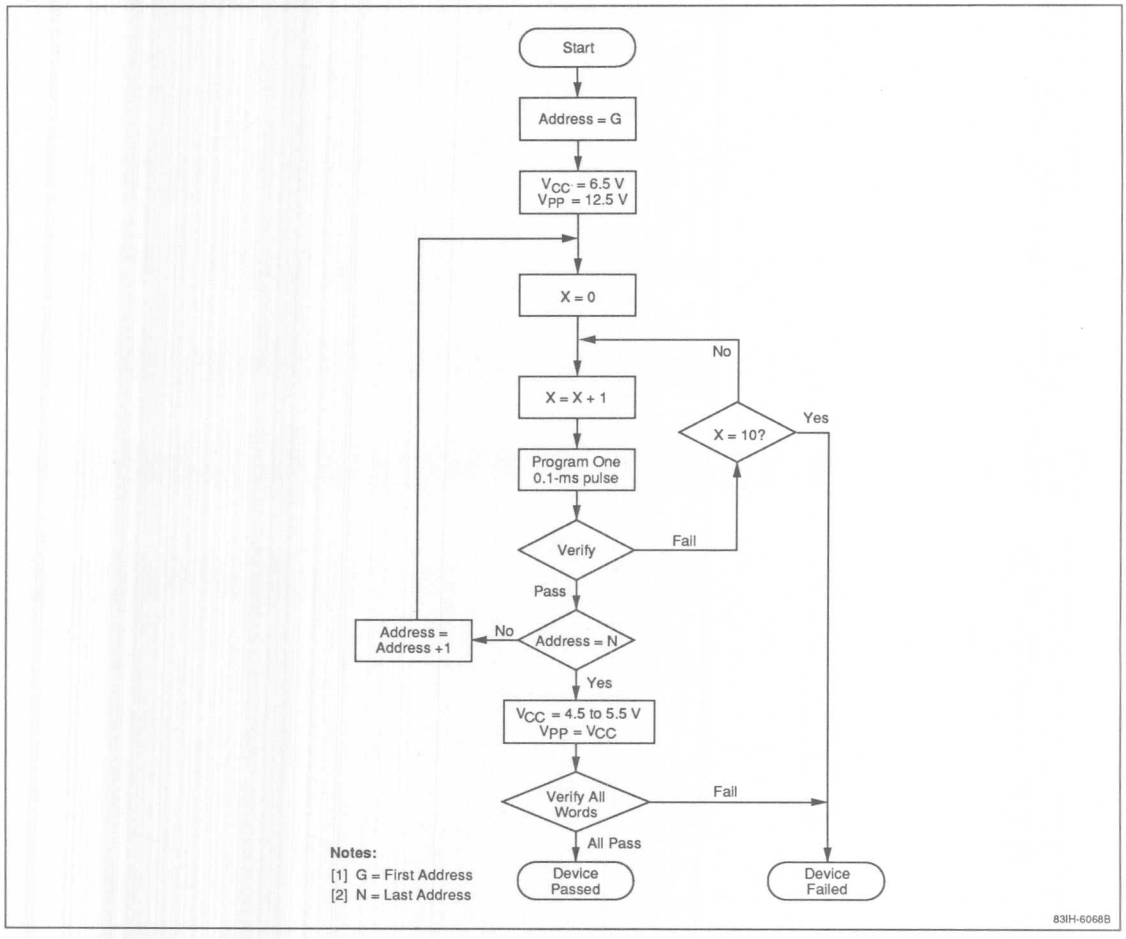
[2] V_{PP} must not be greater than +13.5 V, including overshoot.

[3] Removing and reinserting the device while a voltage of 12.5 V is applied to pin V_{PP} may affect device reliability.

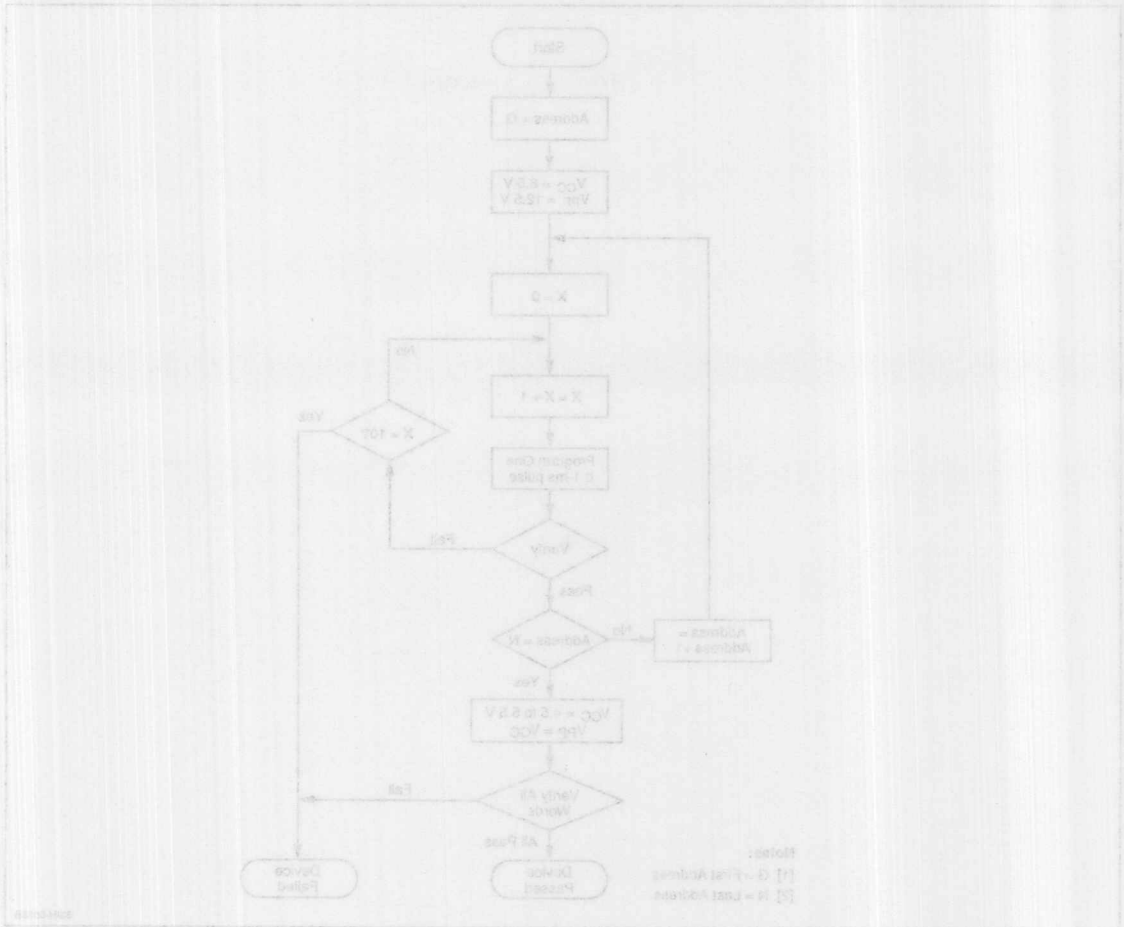
[4] The output lines are also used for data input when programming the device.

83TB-6058B

Figure 3 Word Programming Flowchart



9



NEC Electronics Inc.

μPD27C2001
262,144 x 8-Bit
CMOS UV EPROM

Description

The μPD27C2001 is a 2,097,152-bit ultraviolet erasable EPROM fabricated with double-polysilicon CMOS technology for a substantial savings in both operating and standby power. The device is organized as 262,144 words by 8 bits and operates from a single +5-volt power supply.

The μPD27C2001 has a single-location programming feature, three-state ouputs, and fully TTL-compatible inputs and outpus. It also has a program voltage (V_{PP}) of 12.5 volts and is available in a 32-pin cerdip with quartz window.

Features

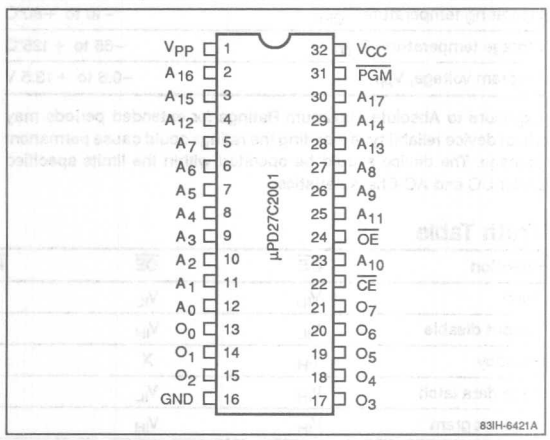
- 262,144 x 8-bit organization
- Ultraviolet erasable and electrically programmable
- High-speed page or byte programming
- Low power dissipation
  - 30 mA max (active)
  - 100 μA max (standby)
- TTL-compatible I/O for reading and programming
- Single +5-volt power supply
- Double-polysilicon CMOS technology
- 32-pin cerdip packaging with quartz window
- JEDEC-compatible pinout

Ordering Information

Part Number	Access Time (max)	Package
μPD27C2001D-15	150 ns	32-pin cerdip with quartz window
D-17	170 ns	
D-20	200 ns	

Pin Configuration

32-Pin Cerdip



Pin Identification

Symbol	Function
A_0 - A_{17}	Address inputs
O_0 - O_7	Data outputs
$\overline{CE}$	Chip enable
$\overline{OE}$	Output enable
$\overline{PGM}$	Program
GND	Ground
V_{CC}	+5-volt power supply
V_{PP}	Program voltage

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New 120 ns speed and WSOP package will be available in 1991.

Absolute Maximum Ratings

Power supply voltage, V_{CC}	−0.6 to +7.0 V
Input voltage, V_{IN}	−0.6 to + 7.0 V
Input voltage, A_9	−0.6 to +13.5 V
Output voltage, V_{OUT}	−0.6 to +7.0 V
Operating temperature, T_{OPR}	−10 to +80°C
Storage temperature, T_{STG}	−65 to +125°C
Program voltage, V_{PP}	−0.6 to +13.5 V

Exposure to Absolute Maximum Ratings for extended periods may affect device reliability; exceeding the ratings could cause permanent damage. The device should be operated within the limits specified under DC and AC Characteristics.

Capacitance

T_A = 25°C; f = 1 MHz; V_{IN} and V_{OUT} = 0 V

Parameter	Symbol	Min	Typ	Max	Unit
Input capacitance	C_{IN}			14	pF
Output capacitance	C_{OUT}			16	pF

Truth Table

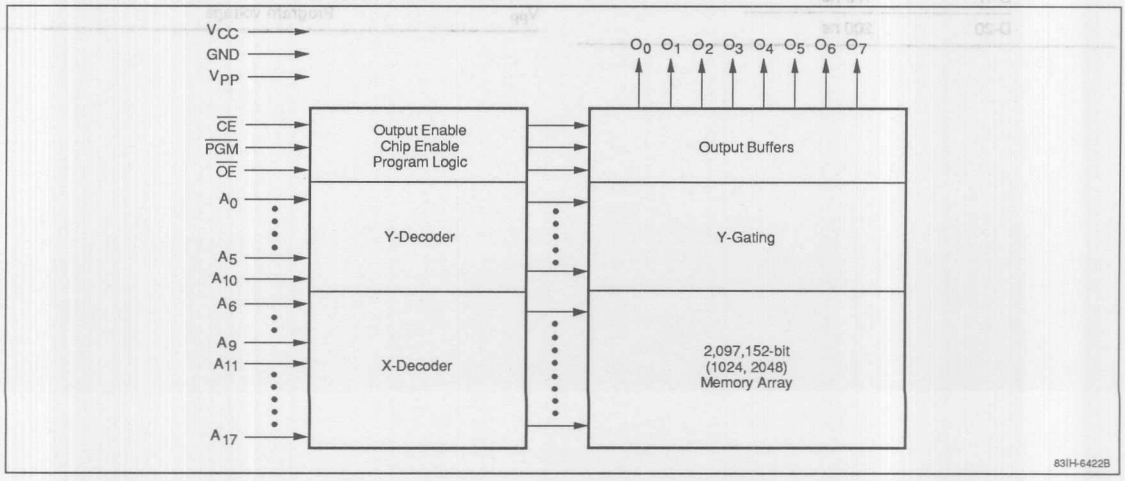
Function	$\overline{CE}$	$\overline{OE}$	$\overline{PGM}$	V_{PP}	V_{CC}	Outputs
Read	V_{IL}	V_{IL}	V_{IH}	5.0 V	5.0 V	D_{OUT}
Output disable	V_{IL}	V_{IH}	X	5.0 V	5.0 V	High-Z
Standby	V_{IH}	X	X	5.0 V	5.0 V	High-Z
Page data latch	V_{IH}	V_{IL}	V_{IH}	12.5 V	6.5 V	D_{IN}
Page program	V_{IH}	V_{IH}	V_{IL}	12.5 V	6.5 V	High-Z
Byte program	V_{IL}	V_{IH}	V_{IL}	12.5 V	6.5 V	D_{IN}
Program verify	V_{IL}	V_{IL}	V_{IH}	12.5 V	6.5 V	D_{OUT}
Program inhibit	X	V_{IL}	V_{IL}	12.5 V	6.5 V	High-Z
	X	V_{IH}	V_{IH}			

Notes:

(1) X = V_{IL} or V_{IH}.

(2) In read operation, $\overline{PGM}$ must be set to V_{IH} at all times, or for at least 2 μs before $\overline{OE}$ or $\overline{CE}$ returns to V_{IH}.

Block Diagram



Recommended Operating Conditions

Parameter	Symbol	Min	Typ	Max	Unit
Read Operation or Standby					
Supply voltage	V_{CC}	4.5	5.0	5.5	V
	V_{PP}	V_{CC} – 0.6	V_{CC}	V_{CC} + 0.6	V
Input voltage, high	V_{IH}	2.0		V_{CC} + 0.3	V
Input voltage, low	V_{IL}	–0.3		0.8	V
Operating temperature	T_A	0		70	°C
Programming Operation					
Supply voltage	V_{CC}	6.25	6.5	6.75	V
	V_{PP}	12.2	12.5	12.8	V
Input voltage, high	V_{IH}	2.4		V_{CC} + 0.3	V
Input voltage, low	V_{IL}	–0.3		0.8	V
Operating temperature	T_A	20	25	30	°C

DC Characteristics

T_A = 0 to +70°C; V_{CC} = +5.0 V ± 10%; V_{PP} = V_{CC} ± 0.6 V

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions
Read Operation						
Output voltage, high	V_{OH1}	2.4			V	I_{OH} = –400 μA
	V_{OH2}	V_{CC} – 0.7			V	I_{OH} = –100 μA
Output voltage, low	V_{OL}			0.45	V	I_{OL} = 2.1 mA
Output leakage current	I_{LO}			10	μA	V_{OUT} = 0 V to V_{CC}; $\overline{OE}$ = V_{IH}
Input leakage current	I_{LI}			10	μA	V_{IN} = 0 V to V_{CC}
V_{PP} current	I_{PP}		1	100	μA	V_{PP} = V_{CC}
V_{CC} current (active)	I_{CCA1}			30	mA	$\overline{CE}$ = V_{IL}; V_{IN} = V_{IH}
	I_{CCA2}			30	mA	f = 6.7 MHz; I_{OUT} = 0 mA
V_{CC} current (standby)	I_{CCS1}			1	mA	$\overline{CE}$ = V_{IH} min
	I_{CCS2}		1	100	μA	$\overline{CE}$ = V_{CC}; V_{IN} = 0 V to V_{CC}

DC Characteristics (cont)

T_A = 25 ± 5°C; V_{CC} = +6.5 V ± 0.25; V_{PP} = +12.5 V ± 0.3

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions
Programming Operation						
Output voltage, high	V_{OH}	2.4			V	I_{OH} = –400 μA
Output voltage, low	V_{OL}			0.45	V	I_{OL} = 2.1 mA
Input leakage current	I_{LI}			10	μA	V_{IN} = V_{IL} or V_{IH}
V_{PP} current	I_{PP}			50	mA	$\overline{CE}$ = $\overline{PGM}$ = V_{IL}
V_{CC} current	I_{CC}			30	mA	

9

AC Characteristics

T_A = 0 to +70°C; V_{CC} = +5.0 V ± 10%; V_{PP} = V_{CC} ± 0.6 V

		μPD27C2001-15		μPD27C2001-17		μPD27C2001-20			
Parameter	**Symbol**	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**	**Unit**	**Test Conditions**
Read Operation									
Address to output delay	t_{ACC}		150		170		200	ns	$\overline{CE}$ = $\overline{OE}$ = V_{IL}
$\overline{CE}$ to output delay	t_{CE}		150		170		200	ns	$\overline{OE}$ = V_{IL}
$\overline{OE}$ to output delay	t_{OE}		70		70		75	ns	$\overline{CE}$ = V_{IL}
$\overline{OE}$ high to output float	t_{DF}	0	55	0	55	0	60	ns	$\overline{CE}$ = V_{IL} or $\overline{OE}$ = V_{IL}
Address to output hold	t_{OH}	0		0		0		ns	$\overline{CE}$ = $\overline{OE}$ = V_{IL}

AC Characteristics (cont)

T_A = 25 ± 5°C; V_{CC} = +6.5 V ± 0.25; V_{PP} = +12.5 V ± 0.3

Parameter	**Symbol**	**Min**	**Typ**	**Max**	**Unit**	**Test Conditions**
Page Programming Operation						
Address setup time	t_{AS}	2			μs	
$\overline{CE}$ setup time	t_{CES}	2			μs	
Data setup time	t_{DS}	2			μs	
Address hold time	t_{AH}	2			μs	
	t_{AHL}	2			μs	
	t_{AHV}	0			μs	
Data hold time	t_{DH}	2			μs	
$\overline{OE}$ to output float time	t_{DF}	0		130	ns	
V_{PP} setup time	t_{VPS}	2			μs	
V_{CC} setup time	t_{VCS}	2			μs	
Program pulse width	t_{PW}	0.095	0.1	0.105	ms	
$\overline{OE}$ setup time	t_{OES}	2			μs	
$\overline{OE}$ to output delay	t_{OE}			150	ns	
$\overline{OE}$ pulse width during data latch	t_{LW}	1			μs	
$\overline{PGM}$ setup time	t_{PGMS}	2			μs	
$\overline{CE}$ hold time	t_{CEH}	2			μs	
OE hold time	t_{OEH}	2			μs	

AC Characteristics (cont)

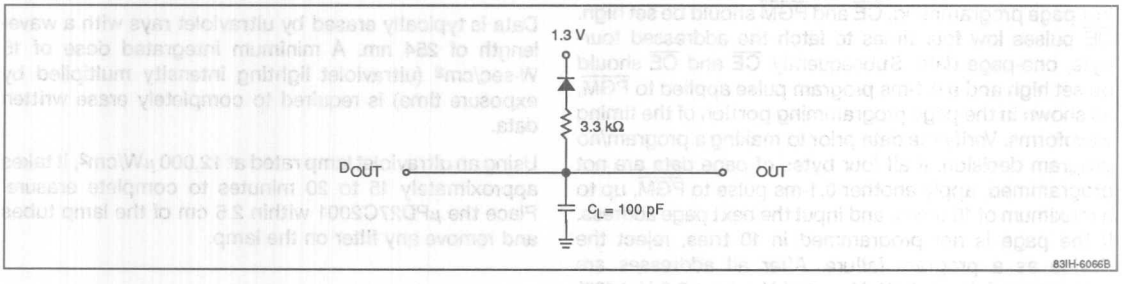
T_A = 25 ± 5°C; V_{CC} = +6.5 V ± 0.25; V_{PP} = +12.5 V ± 0.3

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions
Byte Programming Operation						
Address setup time	t_{AS}	2			μs	
$\overline{OE}$ setup time	t_{OES}	2			μs	
Data setup time	t_{DS}	2			μs	
Address hold time	t_{AH}	2			μs	
Data hold time	t_{DH}	2			μs	
$\overline{OE}$ to output float time	t_{DF}	0		130	ns	
V_{PP} setup time	t_{VPS}	2			μs	
V_{CC} setup time	t_{VCS}	2			μs	
Program pulse width	t_{PW}	0.095	0.1	0.105	ms	
$\overline{CE}$ setup time	t_{CES}	2			μs	
$\overline{OE}$ to output delay	t_{OE}			150	ns	

Notes:

(1) Input pulse levels = 0.45 to 2.4 V; input and output timing reference levels = 0.8 and 2.0 V; input rise and fall times ≤ 20 ns. See figure 1 for output load.

Figure 1. Output Load



9

PROGRAMMING

Begin programming by erasing all data; this sets all bits high. The μPD27C2001 is originally shipped in this condition. To enter data, program a low-level TTL signal into the chosen location. Address the first byte or page location and apply valid data at the eight ouput pins. Raise V_{CC} to +6.5 V ±0.25 and then V_{PP} to +12.5 V ±0.3.

Byte Programming

$\overline{CE}$ should be set low and $\overline{OE}$ high to start programming at the initial byte address. Apply a 0.1-ms program pulse to $\overline{PGM}$, as shown in the byte programming portion of the timing waveforms. Set $\overline{OE}$ low to verify the eight bits prior to making a program/no program decision. If the byte is not programmed, apply another 0.1-ms pulse to $\overline{PGM}$, up to a maximum of 10 times, and input the next address. If the bits are not programmed in 10 tries, reject the device as a program failure. After all addresses are programmed, lower both V_{CC} and V_{PP} to +5.0 V ±10% and verify all data again.

Page Programming

For page programming, $\overline{CE}$ and $\overline{PGM}$ should be set high. $\overline{OE}$ pulses low four times to latch the addressed four-byte, one-page data. Subsequently, $\overline{CE}$ and $\overline{OE}$ should be set high and a 0.1-ms program pulse applied to $\overline{PGM}$, as shown in the page programming portion of the timing waveforms. Verify the data prior to making a program/no program decision. If all four bytes of page data are not programmed, apply another 0.1-ms pulse to $\overline{PGM}$, up to a maximum of 10 times, and input the next page address. If the page is not programmed in 10 tries, reject the device as a program failure. After all addresses are programmed, lower both V_{CC} and V_{PP} to +5.0 V ±10% and verify all data again.

Program Inhibit

Use the programming inhibit option to program multiple μPD27C2001s connected in parallel. All like inputs except $\overline{PGM}$ and $\overline{OE}$ may be common. Program individual devices by applying a low-level TTL pulse to the $\overline{PGM}$ pin of the device to be programmed. Apply a high-level signal to the $\overline{PGM}$ pins of the other devices to prevent them from being programmed.

Program Verification

To verify that the device is correctly programmed, normal read cycles can be executed with a high logic level applied to the $\overline{PGM}$ pin and a low logic level applied to $\overline{CE}$ and $\overline{OE}$ of the device to be verified. The $\overline{CE}$ or $\overline{OE}$ pins of all other devices should be set high.

Program Erasure

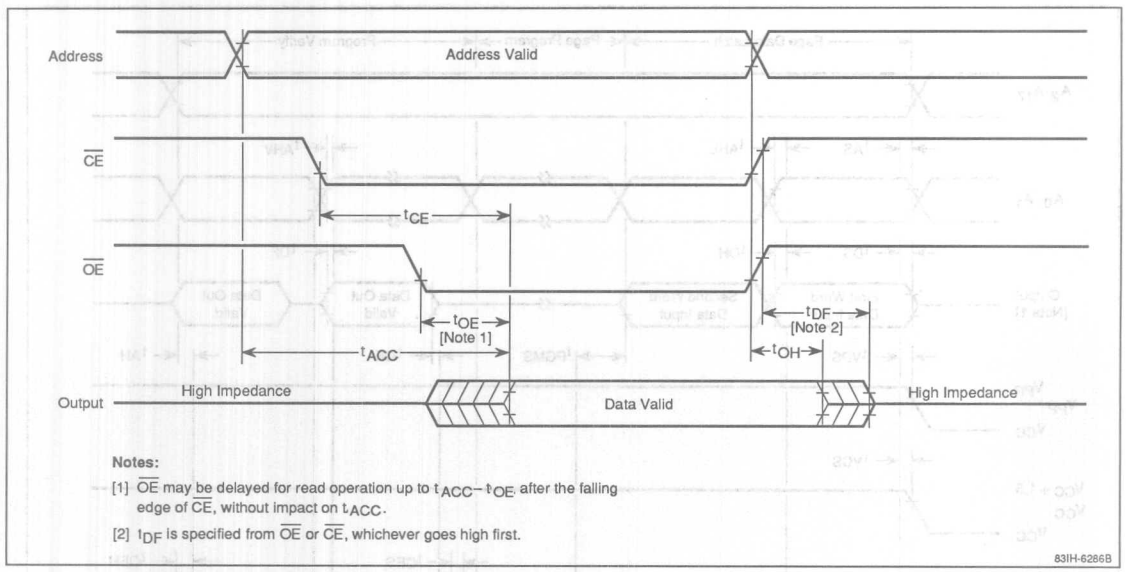
Erase data on the μPD27C2001 by exposing it to light with a wavelength shorter than 400 nm. Since exposure to direct sunlight or room-level fluorescent light could also erase the data, mask the window to prevent unintentional erasure by ultraviolet rays. Opaque labels are supplied with every device.

Data is typically erased by ultraviolet rays with a wavelength of 254 nm. A minimum integrated dose of 15 W-sec/cm^2 (ultraviolet lighting intensity multiplied by exposure time) is required to completely erase written data.

Using an ultraviolet lamp rated at 12,000 μW/cm^2, it takes approximately 15 to 20 minutes to complete erasure. Place the μPD27C2001 within 2.5 cm of the lamp tubes and remove any filter on the lamp.

Timing Waveforms

Read Cycle



Notes:

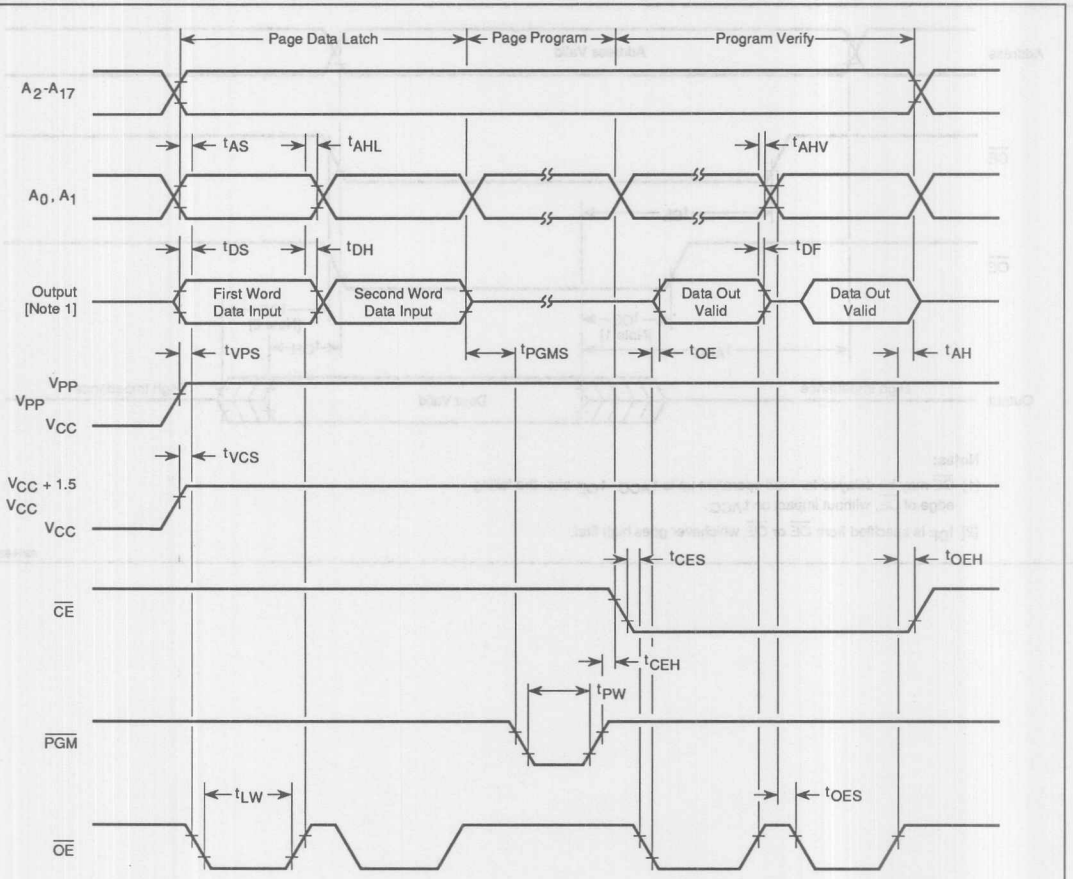
[1] $\overline{OE}$ may be delayed for read operation up to $t_{ACC} - t_{OE}$ after the falling edge of $\overline{CE}$, without impact on t_{ACC}.

[2] t_{DF} is specified from $\overline{OE}$ or $\overline{CE}$, whichever goes high first.

9

Timing Waveforms (cont)

Page Programming

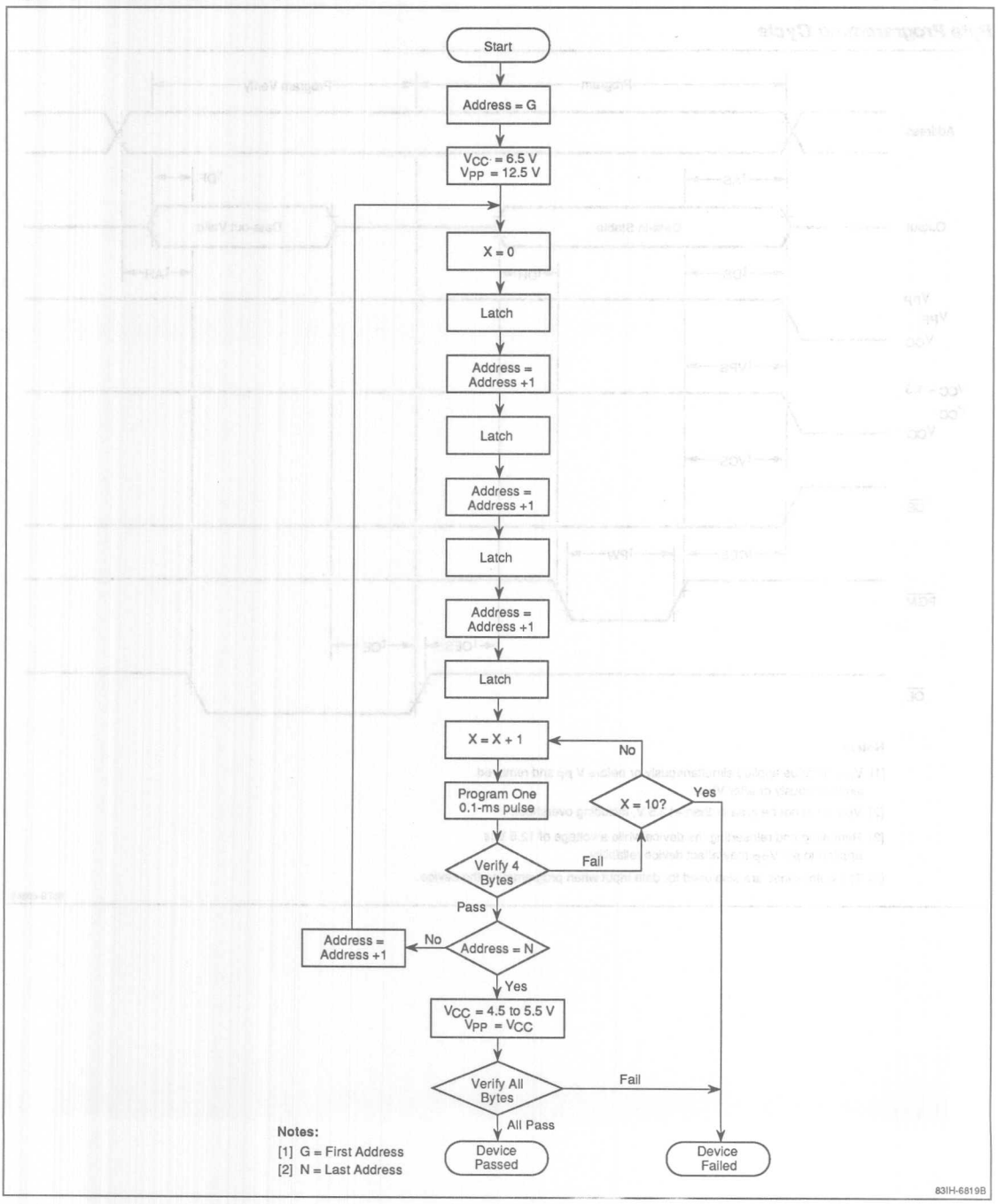


Notes:

[1] The output lines are also used for data input when programming the device.

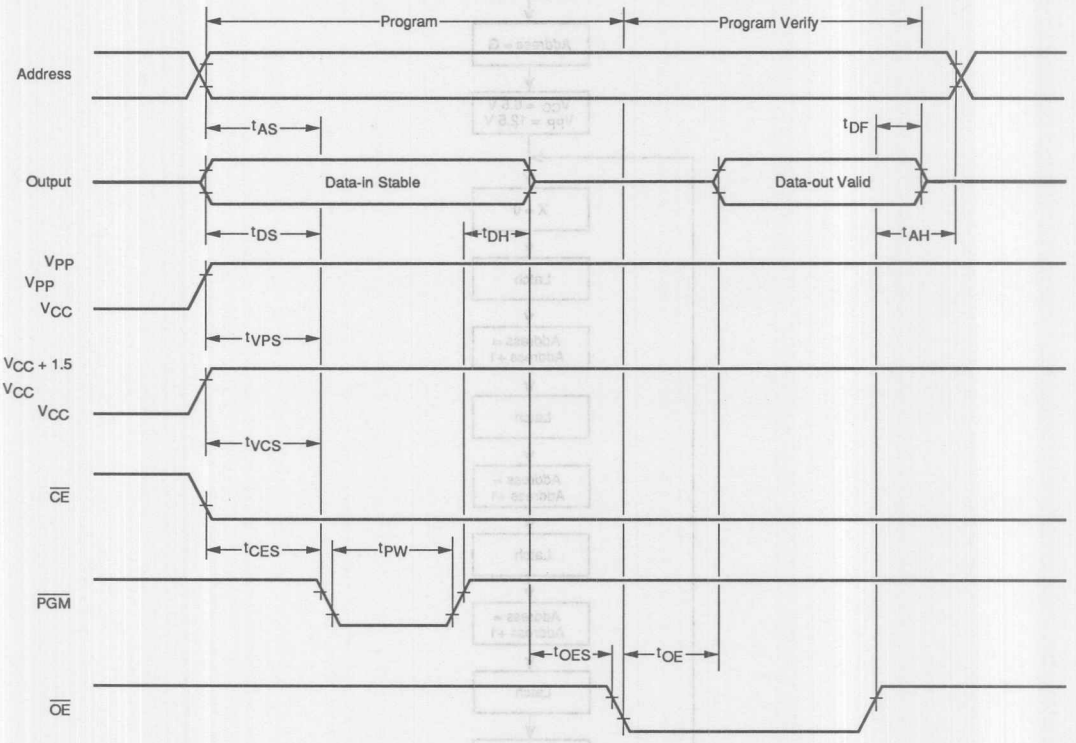
83IH-6999B

Figure 2. Page Programming Flowchart



Timing Waveforms (cont)

Byte Programming Cycle



Notes:

[1] V_{CC} must be applied simultaneously or before V_{PP} and removed simultaneously or after V_{PP}.

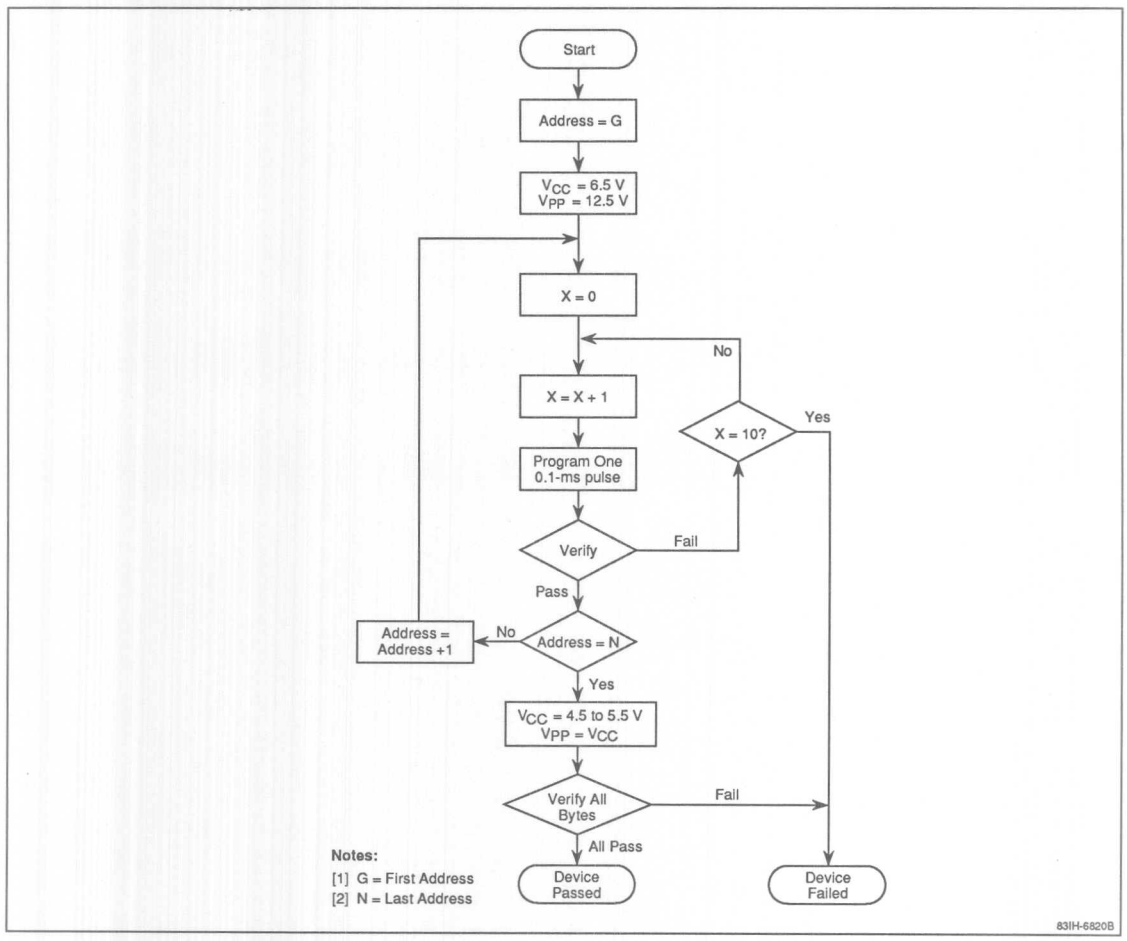
[2] V_{PP} must not be greater than +13.5 V, including overshoot.

[3] Removing and reinserting the device while a voltage of 12.5 V is applied to pin V_{PP} may affect device reliability.

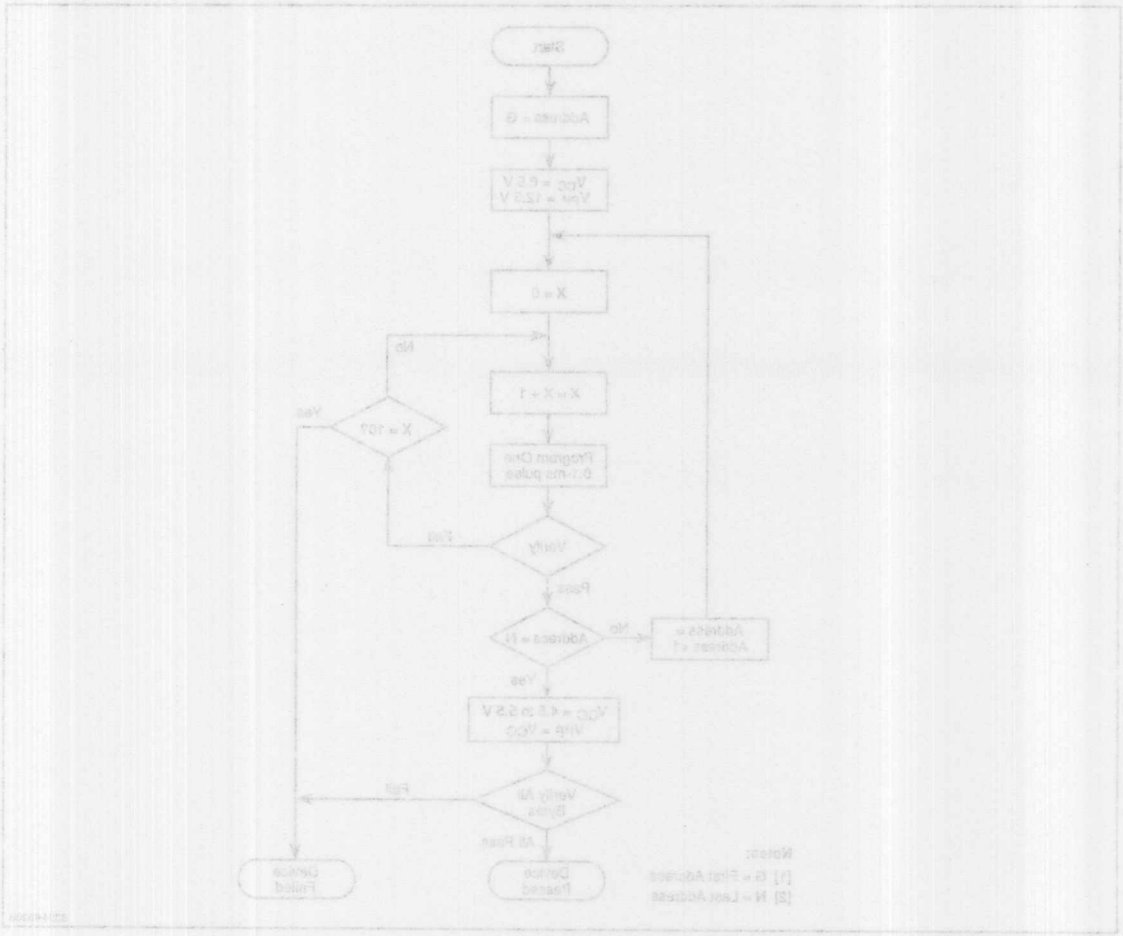
[4] The output lines are also used for data input when programming the device.

83TB-6058B

Figure 3. Byte Programming Flowchart



9



NEC Electronics Inc.

μPD27C4001
524,288 x 8-Bit
CMOS UV EPROM

Description

The μPD27C4001 is a 4,194,304-bit ultraviolet erasable EPROM fabricated with double-polysilicon CMOS technology for a substantial savings in both operating and standby power. The device is organized as 524,288 words by 8 bits and operates from a single +5-volt power supply.

The μPD27C4001 has a single-location programming feature, three-state outputs, and fully TTL-compatible inputs and outputs. It also has a program voltage (V_{PP}) of 12.5 volts and is available in a 32-pin cerdip with quartz window.

Features

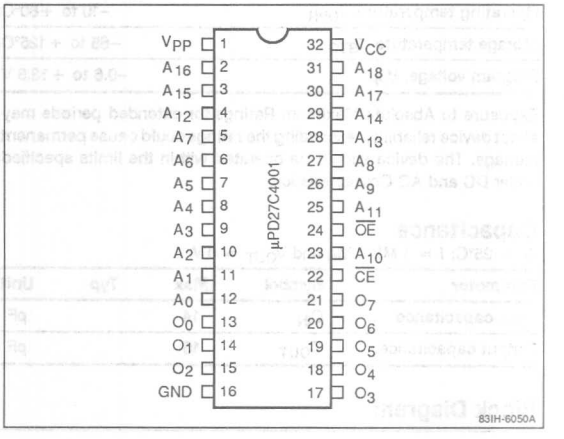
- 524,288-word by 8-bit organization
- Ultraviolet erasable and electrically programmable
- High-speed programming
- Low power dissipation
  - — 30 mA (active)
  - — 100 μA (standby)
- TTL-compatible I/O for reading and programming
- Single +5-volt power supply
- Double-polysilicon CMOS technology
- 32-pin cerdip packaging with a quartz window
- JEDEC-compatible pinout

Ordering Information

Part Number		Access Time (max)	Package
μPD27C4001	DZ-15	150 ns	32-pin cerdip with quartz window
	DZ-17	170 ns	
	DZ-20	200 ns	

Pin Configuration

32-Pin Cerdip



Pin Identification

Symbol	Function
A_0 - A_{18}	Address inputs
O_0 - O_7	Data outputs
$\overline{CE}$	Chip enable
$\overline{OE}$	Output enable
GND	Ground
V_{CC}	+5-volt power supply
V_{PP}	Program voltage

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Absolute Maximum Ratings

Power supply voltage, V_{CC}	−0.6 to +7.0 V
Input voltage, V_{IN}	−0.6 to V_{CC} + 0.3 V
Input voltage, A_9	−0.6 to +13.5 V
Output voltage, V_{OUT}	−0.6 to +7.0 V
Operating temperature, T_{OPR}	−10 to +80°C
Storage temperature, T_{STG}	−65 to +125°C
Program voltage, V_{PP}	−0.6 to +13.5 V

Exposure to Absolute Maximum Ratings for extended periods may affect device reliability; exceeding the ratings could cause permanent damage. The device should be operated within the limits specified under DC and AC Characteristics.

Capacitance

T_A = 25°C; f = 1 MHz; V_{IN} and V_{OUT} = 0 V

Parameter	Symbol	Max	Typ	Unit
Input capacitance	C_{IN}	14		pF
Output capacitance	C_{OUT}	16		pF

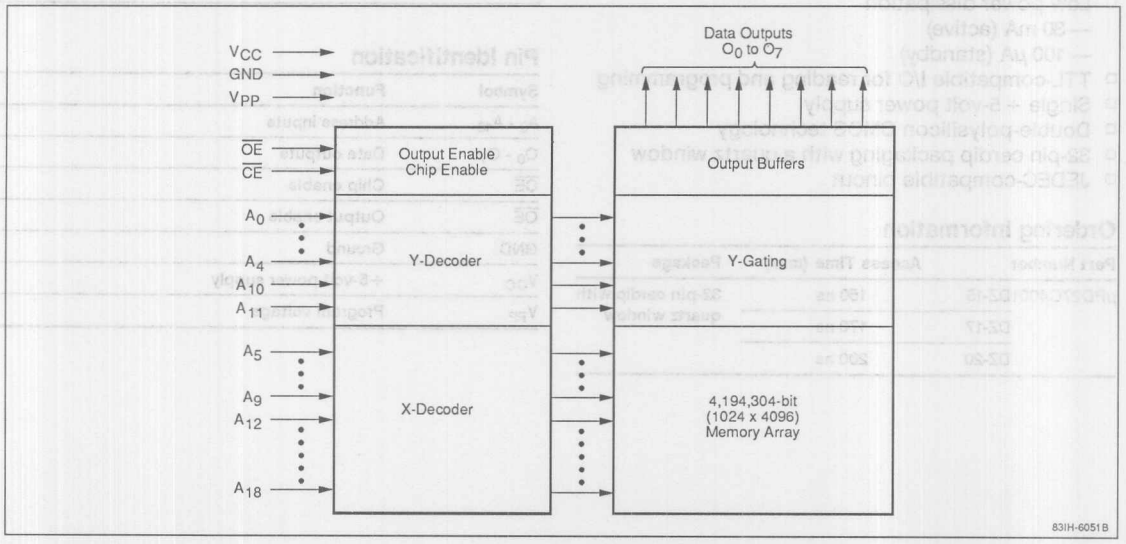
Truth Table

Function	$\overline{CE}$	$\overline{OE}$	V_{PP}	V_{CC}	Outputs
Read	V_{IL}	V_{IL}	+5.0 V	+5.0 V	D_{OUT}
Output disable	V_{IL}	V_{IH}	+5.0 V	+5.0 V	High-Z
Standby	V_{IH}	X	+5.0 V	+5.0 V	High-Z
Program verify	X	V_{IL}	+12.5 V	+6.5 V	D_{OUT}
Program	V_{IL}	V_{IH}	+12.5 V	+6.5 V	D_{IN}
Program inhibit	V_{IH}	V_{IH}	+12.5 V	+6.5 V	High-Z

Notes:

(1) "X" can be either V_{IL} or V_{IH}.

Block Diagram



Recommended Operating Conditions

Parameter	Symbol	Min	Typ	Max	Unit
Read Operation or Standby					
Supply voltage	V_{CC}	4.5	5.0	5.5	V
	V_{PP}	V_{CC} – 0.6	V_{CC}	V_{CC} + 0.6	V
Input voltage, high	V_{IH}	2.0		V_{CC} + 0.3	V
Input voltage, low	V_{IL}	–0.3		0.8	V
Operating temperature	T_A	0		70	°C
Programming Operation					
Supply voltage	V_{CC}	6.25	6.5	6.75	V
	V_{PP}	12.2	12.5	12.8	V
Input voltage, high	V_{IH}	2.4		V_{CC} + 0.3	V
Input voltage, low	V_{IL}	–0.3		0.8	V
Operating temperature	T_A	20	25	30	°C

DC Characteristics

T_A = 0 to +70°C; V_{CC} = +5.0 V ±10%; V_{PP} = V_{CC} ± 0.6 V

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions
Read Operation, Output Disabled, and Standby						
Output voltage, high	V_{OH1}	2.4			V	I_{OH} = –400 μA
	V_{OH2}	V_{CC} – 0.7			V	I_{OH} = –100 μA
Output voltage, low	V_{OL}			0.45	V	I_{OL} = 2.1 mA
Output leakage current	I_{LO}	–10		10	μA	$\overline{OE}$ = V_{IH}; V_{OUT} = 0 V to V_{CC}
Input leakage current	I_{LI}	–10		10	μA	V_{IN} = 0 V to V_{CC}
Operating supply current	I_{CCA1}			30	mA	$\overline{CE}$ = V_{IL}; V_{IN} = V_{IH}
	I_{CCA2}			30	mA	f = 6.7 MHz; I_{OUT} = 0 mA
Standby supply current	I_{CCS1}			1	mA	$\overline{CE}$ = V_{IH} min
	I_{CCS2}		1	100	μA	$\overline{CE}$ ≥ V_{CC} –0.2 V; V_{IN} = 0 V to V_{CC}
Program voltage current	I_{PP}		1	100	μA	V_{PP} = V_{CC}

DC Characteristics (cont)

T_A = +25 ± 5°C; V_{CC} = +6.5 V ± 0.25; V_{PP} = +12.5 V ± 0.3

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions
Programming Operation						
Output voltage, high	V_{OH}	2.4			V	I_{OH} = –400 μA
Output voltage, low	V_{OL}			0.45	V	I_{OL} = 2.1 mA
Input leakage current	I_{LI}	–10		10	μA	V_{IN} = 0 to V_{CC}
Operating supply current	I_{CC}			30	mA	
Program voltage current	I_{PP}			30	mA	$\overline{CE}$ = V_{IL}; $\overline{OE}$ = V_{IH}

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AC Characteristics

T_A = 0 to +70°C; V_{CC} = +5.0 V ± 10%; V_{PP} = V_{CC}

		μPD27C4001-15		μPD27C4001-17		μPD27C4001-20			
Parameter	**Symbol**	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**	**Unit**	**Test Conditions** (Note 1)
Read Operation and Standby									
Address to output delay	t_{ACC}		150		170		200	ns	$\overline{CE}$ = $\overline{OE}$ = V_{IL}
$\overline{CE}$ to output delay	t_{CE}		150		170		200	ns	$\overline{OE}$ = V_{IL}
$\overline{OE}$ to output delay	t_{OE}		70		70		75	ns	$\overline{CE}$ = V_{IL}
$\overline{OE}$ or $\overline{CE}$ to data output float delay	t_{DF}	0	55	0	55	0	60	ns	$\overline{CE}$ = V_{IL} or $\overline{OE}$ = V_{IL}
Address to output hold time	t_{OH}	0		0		0		ns	$\overline{CE}$ = $\overline{OE}$ = V_{IL}

AC Characteristics (cont)

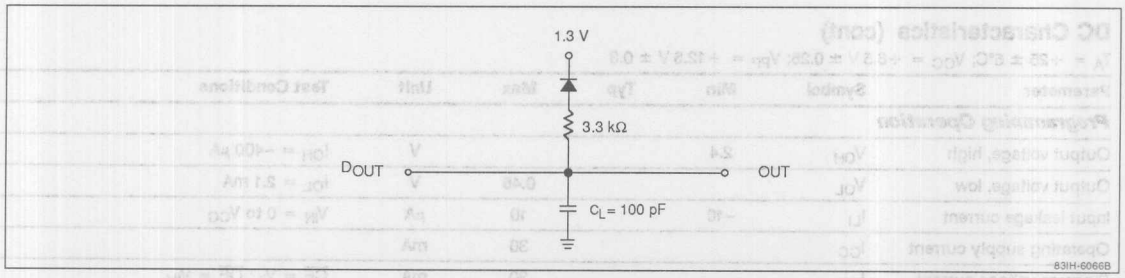
T_A = +25 ± 5°C; V_{CC} = +6.5 V ± 0.25; V_{PP} = +12.5 V ± 0.3

Parameter	**Symbol**	**Min**	**Typ**	**Max**	**Unit**	**Test Conditions** (Note 1)
Programming Operation						
Address setup time	t_{AS}	2			μs	
$\overline{OE}$ setup time	t_{OES}	2			μs	
Data setup time	t_{DS}	2			μs	
Address hold time	t_{AH}	2			μs	
Data hold time	t_{DH}	2			μs	
Output enable to output float delay	t_{DF}	0		130	ns	
V_{PP} setup time	t_{VPS}	2			μs	
Program pulse width	t_{PW}	0.095	0.1	0.105	ms	
V_{CC} setup time	t_{VCS}	2			μs	
Data valid from $\overline{OE}$	t_{OE}			150	ns	

Notes:

(1) Inputs levels = 0.45 to 2.4 V; input and output timing reference levels = 0.8 V and 2.0 V; input rise and fall times ≤ 20 ns. See figure 1 for output load.

Figure 1. Output Load



PROGRAMMING OPERATION

Begin programming by erasing all data; this sets all bits at a high logic level. The μPD27C4001 is originally shipped in this condition. To enter data, apply valid data at the eight output pins of the chosen address. Raise V_{CC} to +6.5 V ±0.25; then raise V_{PP} to +12.5 V ±0.3.

$\overline{OE}$ should be set high to to start programming the initial address. Apply a 0.1-ms program pulse to $\overline{CE}$ as shown in the programming portion of the timing waveforms. Set $\overline{OE}$ low to verify the eight bits prior to making a program/no program decision. If the address is not programmed, apply another 0.1-ms pulse to $\overline{CE}$, up to a maximum of 10 times, and input the next address. If the bits are not programmed in 10 tries, reject the device as a program failure. After all addresses are programmed, lower V_{PP} and then V_{CC} to +5.0 V ±10% and verify all data again.

Program Inhibit

This option is used to program multiple μPD27C4001s connected in parallel. All like inputs except $\overline{CE}$ and $\overline{OE}$ may be common. Program individual devices by applying a high level to all $\overline{OE}$ pins and a low-level TTL pulse to the $\overline{CE}$ pin of the device to be programmed. Applying a high-level signal to the $\overline{CE}$ pins of the other devices prevents them from being programmed.

Program Verification

To verify that the device is correctly programmed, normal read cycles can be executed with a high logic level applied to all $\overline{CE}$ pins and a low logic level applied to the $\overline{OE}$ pin of the device to be verified. A high logic level should be applied to the $\overline{OE}$ pins of all other devices.

Program Erasure

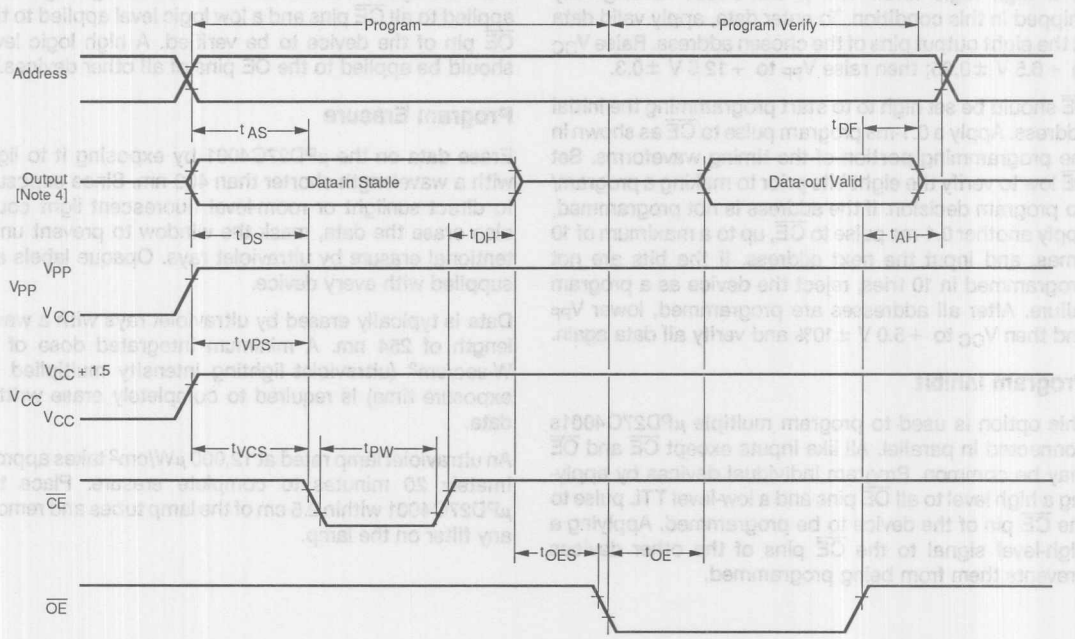
Erase data on the μPD27C4001 by exposing it to light with a wavelength shorter than 400 nm. Since exposure to direct sunlight or room-level fluorescent light could also erase the data, mask the window to prevent unintentional erasure by ultraviolet rays. Opaque labels are supplied with every device.

Data is typically erased by ultraviolet rays with a wavelength of 254 nm. A minimum integrated dose of 15 W-sec/cm^2 (ultraviolet lighting intensity multiplied by exposure time) is required to completely erase written data.

An ultraviolet lamp rated at 12,000 μW/cm^2 takes approximately 20 minutes to complete erasure. Place the μPD27C4001 within 2.5 cm of the lamp tubes and remove any filter on the lamp.

Timing Waveforms

Programming Cycle



Notes:

[1] V_{CC} must be applied simultaneously or before V_{PP} and removed simultaneously or after V_{PP}.

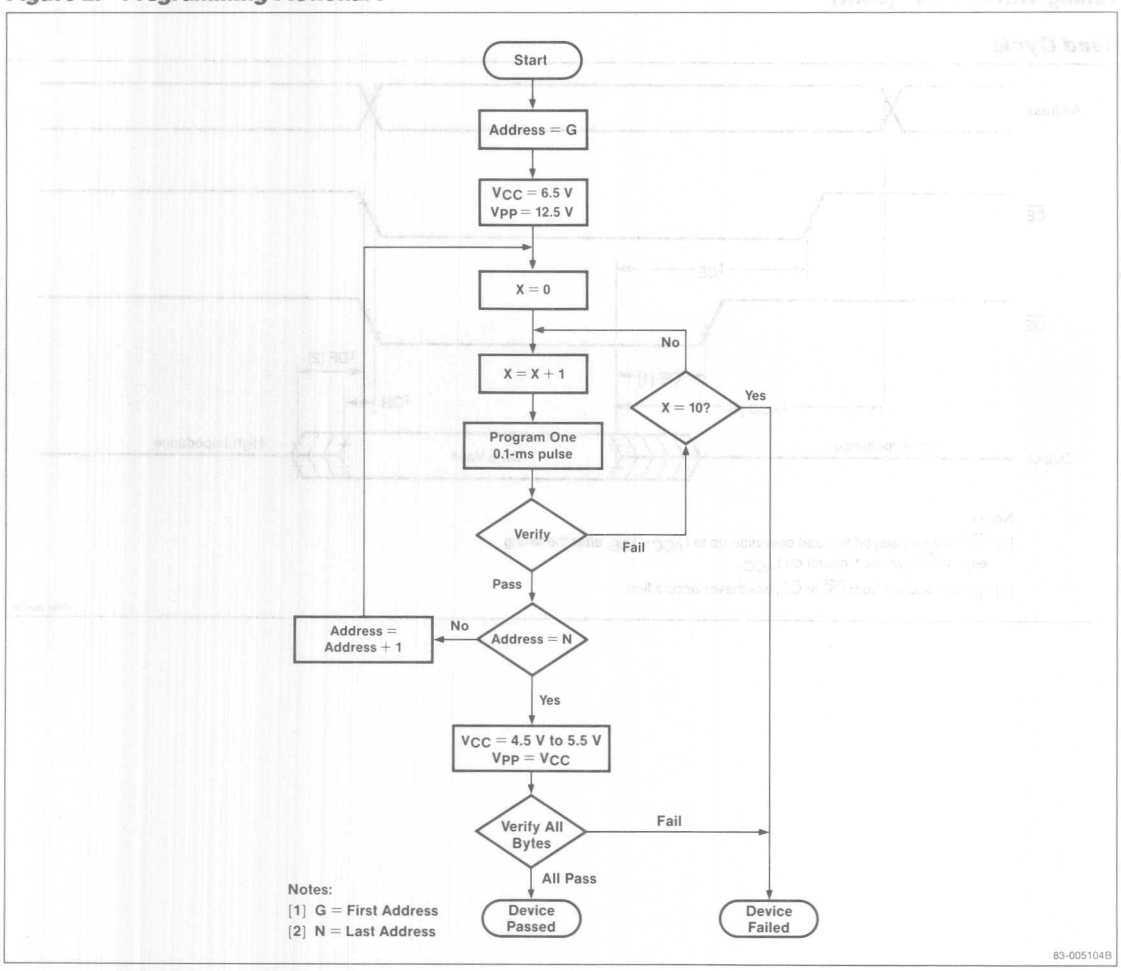
[2] V_{PP} must not be greater than +13.5 V, including overshoot.

[3] Removing and reinserting the device while a voltage of 12.5 V is applied to pin V_{PP} may affect device reliability.

[4] The output lines are used for data input when programming the device.

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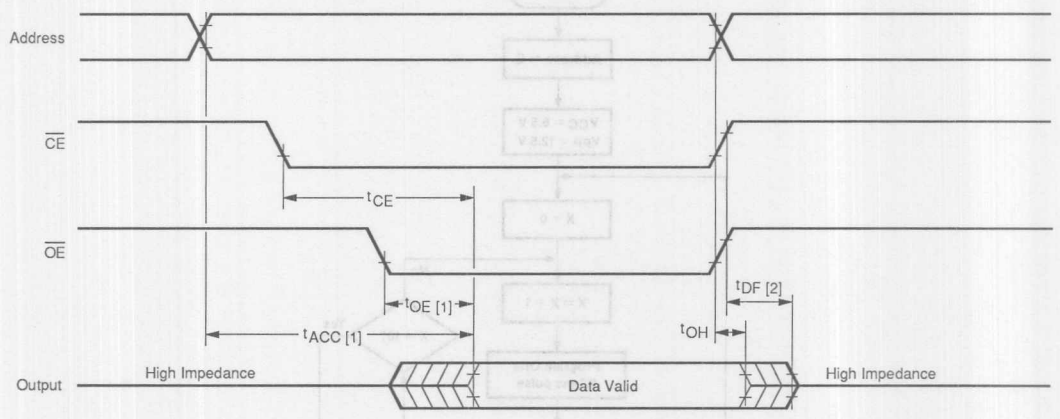
Figure 2. Programming Flowchart



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Timing Waveforms (cont)

Read Cycle



Notes:

[1] $\overline{OE}$ may be delayed for read operation up to $t_{ACC} - t_{OE}$, after the falling edge of $\overline{CE}$, without impact on t_{ACC}.

[2] t_{DF} is specified from $\overline{OE}$ or $\overline{CE}$, whichever occurs first.

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NEC

EEPROMs 10

Section 10
EEPROMs

μPD28C04 512 x 8-Bit CMOS EEPROM	**10-1**
μPD28C05 512 x 8-Bit CMOS EEPROM	**10-11**
μPD28C64 8,192 x 8-Bit CMOS EEPROM	**10-21**
μPD28C256 32,768 x 8-Bit CMOS EEPROM	**10-31**

Additional New Product Information

Device Number	Description	Comments
EEPROMs		
μPD28C64	8K x 8 bits, TSOP packaging	New package (GX suffix)

NEC Electronics Inc.

μPD28C04
512 x 8-Bit
CMOS EEPROM

Description

The μPD28C04 is a 4,096-bit electrically erasable and programmable read-only memory (EEPROM) organized as 512 x 8 bits and fabricated with an advanced CMOS process for high performance and low power consumption.

The device operates from a single +5-volt power supply and provides a $\overline{\text{DATA}}$ polling function to indicate the precise end of write cycles. Additional features include chip erase, auto erase and programming cycles. The μPD28C04 is available in standard 24-pin plastic DIP or miniflat packaging.

Features

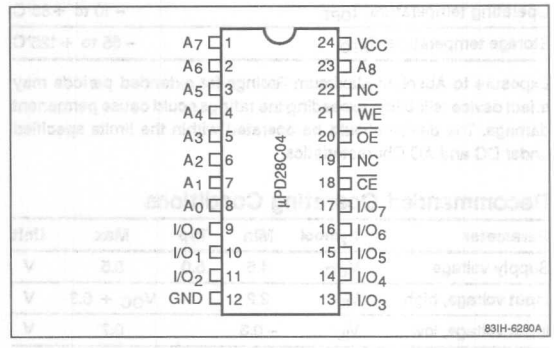
- Fast access times of 200 and 250 ns maximum
- Single +5-volt power supply
- Chip erase feature
- Auto erase and programming at 10 ms maximum
- $\overline{\text{DATA}}$ polling verification
- Low power dissipation
  - 17 mA max (active)
  - 100 μA max (standby)
- Endurance: 100,000 erase/write cycles per byte
- TTL-compatible inputs and outputs
- Three-state outputs
- Advanced CMOS technology
- 24-pin plastic DIP or miniflat packaging

Ordering Information

Part Number	Access Time (max)	Package
μPD28C04C-20	200 ns	24-pin plastic DIP
C-25	250 ns	
μPD28C04G-20	200 ns	24-pin plastic miniflat
G-25	250 ns	

Pin Configuration

24-Pin Plastic DIP or Miniflat



Pin Identification

Symbol	Function
A_0 - A_8	Address inputs
I/O_0 - I/O_7	Data inputs/outputs
$\overline{\text{CE}}$	Chip enable
$\overline{\text{OE}}$	Output enable
$\overline{\text{WE}}$	Write enable
GND	Ground
V_{CC}	+5-volt power supply
NC	No connection

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Absolute Maximum Ratings

Supply voltage, V_{CC}	−0.6 to +7.0 V
Input voltage, V_{I1}	−0.6 to +7.0 V
Input voltage, V_{I3} ($\overline{OE}$)	−0.6 to +16.5 V
Output voltage, V_O	−0.6 to +7.0 V
Operating temperature, T_{OPT}	−10 to +85°C
Storage temperature, T_{STG}	−65 to +125°C

Exposure to Absolute Maximum Ratings for extended periods may affect device reliability; exceeding the ratings could cause permanent damage. The device should be operated within the limits specified under DC and AC Characteristics.

Recommended Operating Conditions

Parameter	Symbol	Min	Typ	Max	Unit
Supply voltage	V_{CC}	4.5	5.0	5.5	V
Input voltage, high	V_{IH}	2.2		V_{CC} + 0.3	V
Input voltage, low	V_{IL}	−0.3		0.7	V
Ambient temperature	T_A	0		70	°C

Capacitance

T_A = 25°C; f = 1 MHz; V_{IN} and V_{OUT} = 0 V

Parameter	Symbol	Min	Typ	Max	Unit
Input capacitance	C_I		7	12	pF
Output capacitance	C_O			10	pF

Truth Table

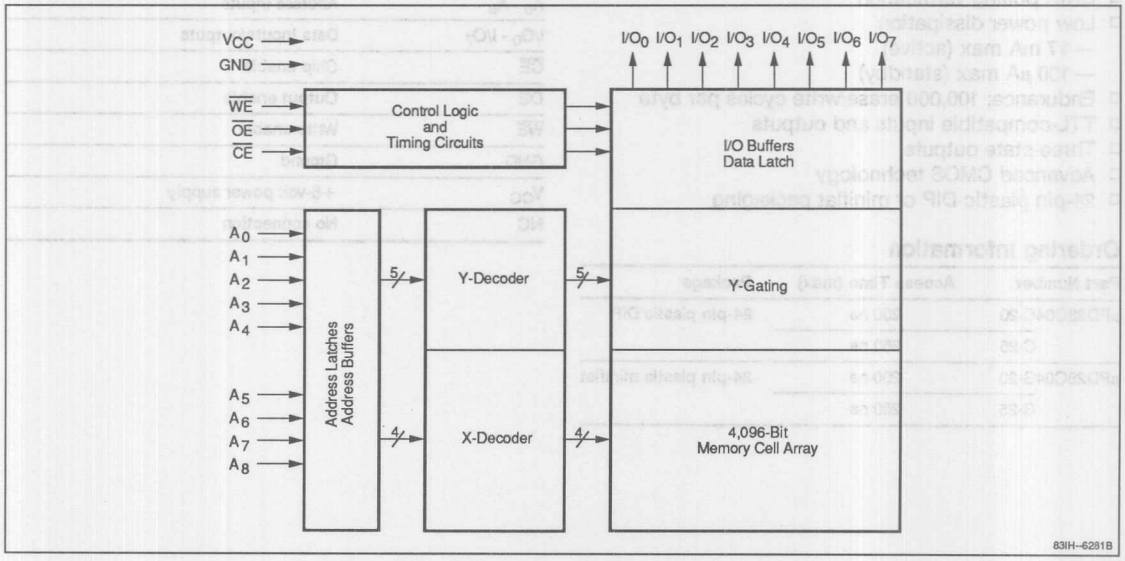
Function	$\overline{CE}$	$\overline{OE}$	$\overline{WE}$	I/O	I_{CC}
Read	V_{IL}	V_{IL}	V_{IH}	D_{OUT}	Active
Standby and write inhibit	V_{IH}	X	X	High-Z	Standby
Write	V_{IL}	V_{IH}	V_{IL}	D_{IN}	Active
Chip erase	V_{IL}	V_{IHH}	V_{IL}	$D_{IN} = V_{IH}$	Active
Write inhibit	X	V_{IL}	X	—	—
	X	X	V_{IH}		

Notes:

(1) X can be either V_{IL} or V_{IH}.

(2) V_{IHH} = +15 ± 0.5 V.

Block Diagram



DC Characteristics

T_A = 0 to +70°C; V_{CC} = +5.0 V ± 10%

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions
Output voltage, high	V_{OH1}	2.4			V	I_{OH} = −400 μA
	V_{OH2}	V_{CC} − 0.7			V	I_{OH} = −100 μA
Output voltage, low	V_{OL}			0.45	V	I_{OL} = 2.1 mA
Output leakage current	I_{LO}			10	μA	V_{OUT} = 0 to V_{CC}
Input leakage current	I_{LI}			10	μA	V_{IN} = 0 to V_{CC}
V_{CC} current (active)	I_{CCA1}			20	mA	$\overline{CE}$ = V_{IL}; V_{IN} = V_{IH}
	I_{CCA2}			50	mA	f = 5 MHz; I_{OUT} = 0 mA
V_{CC} current (standby)	I_{CCS1}			1	mA	$\overline{CE}$ = V_{IH}
	I_{CCS2}			100	μA	$\overline{CE}$ = V_{CC}; V_{IN} = 0 V to V_{CC}

AC Characteristics

T_A = 0 to +70°C; V_{CC} = +5.0 V ± 10%

		μPD28C04-20		μPD28C04-25			
Parameter	Symbol	Min	Max	Min	Max	Unit	Test Conditions
Read Operation							
Address to output delay	t_{ACC}		200		250	ns	$\overline{CE}$ = $\overline{OE}$ = V_{IL}; $\overline{WE}$ = V_{IH}
$\overline{CE}$ to output delay	t_{CE}		200		250	ns	$\overline{OE}$ = V_{IL}; $\overline{WE}$ = V_{IH}
$\overline{OE}$ to output delay	t_{OE}	10	75	10	100	ns	$\overline{CE}$ = V_{IL}; $\overline{WE}$ = V_{IH}
$\overline{CE}$ high to output float	t_{DFC}	0	60	0	80	ns	$\overline{OE}$ = V_{IL}; $\overline{WE}$ = V_{IH}
$\overline{OE}$ high to output float	t_{DFO}	0	60	0	80	ns	$\overline{CE}$ = V_{IL}; $\overline{WE}$ = V_{IH}
Output hold time from address change	t_{OHA}	0		0		ns	$\overline{CE}$ = $\overline{OE}$ = V_{IL}; $\overline{WE}$ = V_{IH} (Note 2)
Output hold time from rising edge of $\overline{CE}$	t_{OHC}	0		0		ns	$\overline{OE}$ = V_{IL}; $\overline{WE}$ = V_{IH} (Note 2)
Output hold time from rising edge of $\overline{OE}$	t_{OHO}	0		0		ns	$\overline{CE}$ = V_{IL}; $\overline{WE}$ = V_{IH}
$\overline{WE}$ setup time to $\overline{CE}$	t_{WSC}	10		10		ns	$\overline{CE}$ = V_{IH}
$\overline{WE}$ setup time to $\overline{OE}$	t_{WSO}	10		10		ns	$\overline{OE}$ = V_{IH}
$\overline{WE}$ hold time from rising edge of $\overline{OE}$	t_{WHO}	10		10		ns	$\overline{OE}$ = V_{IH}
Write Operation							
Write cycle time	t_{WC}	10		10		ms	
Address setup time	t_{AS}	10		10		ns	
Address hold time	t_{AH}	200		200		ns	
Write setup time	t_{CS}	0		0		ns	
Write hold time	t_{CH}	0		0		ns	

10

AC Characteristics (cont)

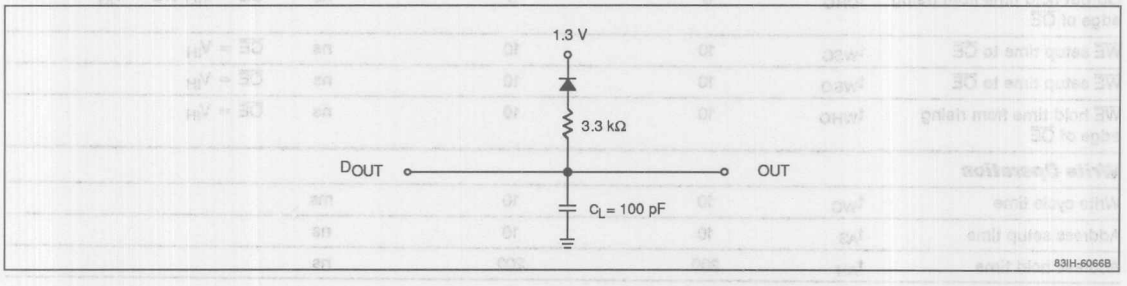
Parameter	Symbol	μPD28C04-20 Min	μPD28C04-20 Max	μPD28C04-25 Min	μPD28C04-25 Max	Unit	Test Conditions
Write Operation (cont)							
$\overline{CE}$ pulse width	t_{CW}	150		150		ns	
$\overline{OE}$ high setup time	t_{OES}	10		10		ns	
$\overline{OE}$ high hold time	t_{OEH}	10		10		ns	
$\overline{WE}$ pulse width	t_{WP}	150		150		ns	
Data setup time	t_{DS}	100		100		ns	
Data hold time	t_{DH}	20		20		ns	
$\overline{WE}$ high after $\overline{WE}$-controlled write cycle	t_{WEH}	9.9		9.9		ms	
$\overline{CE}$ high after $\overline{CE}$-controlled write cycle	t_{CEH}	9.9		9.9		ms	
Chip Erase Operation							
$\overline{CE}$ setup time	t_{ECS}	500		500		ns	
$\overline{OE}$ setup time	t_{EOES}	500		500		ns	
Data setup time	t_{EDS}	500		500		ns	
Data hold time	t_{EDH}	100		100		ns	
$\overline{WE}$ pulse width	t_{EWP}	10		10		ms	
$\overline{CE}$ hold time	t_{ECH}	5		5		μs	
$\overline{OE}$ hold time	t_{EOEH}	t_{ECH} + 3		t_{ECH} + 3		μs	

Notes:

(1) See figure 1 for the output load. Input rise and fall time ≤ 20 ns; input pulse levels = 0.45 and 2.4 V; timing measurement reference levels = 0.8 and 2.0 V for both inputs and outputs.

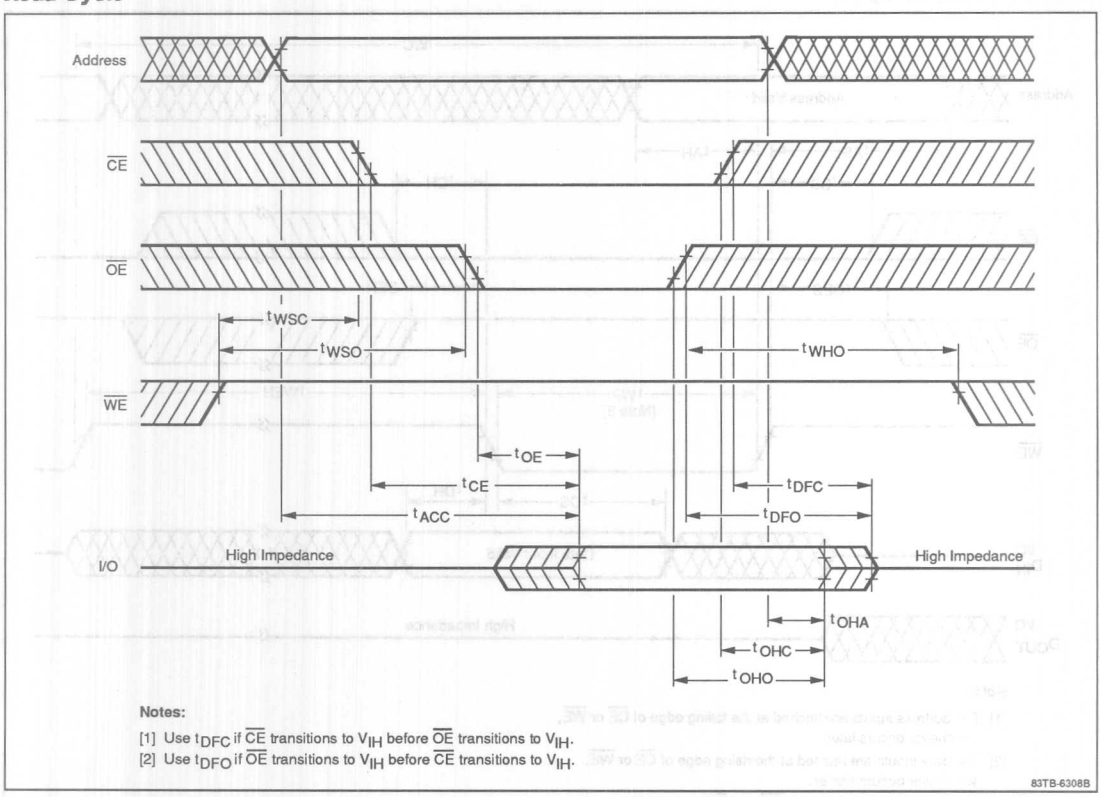
(2) Output hold time is specified from address, $\overline{OE}$ or $\overline{CE}$, whichever goes invalid first.

Figure 1. Output Load



Timing Waveforms

Read Cycle



Notes:

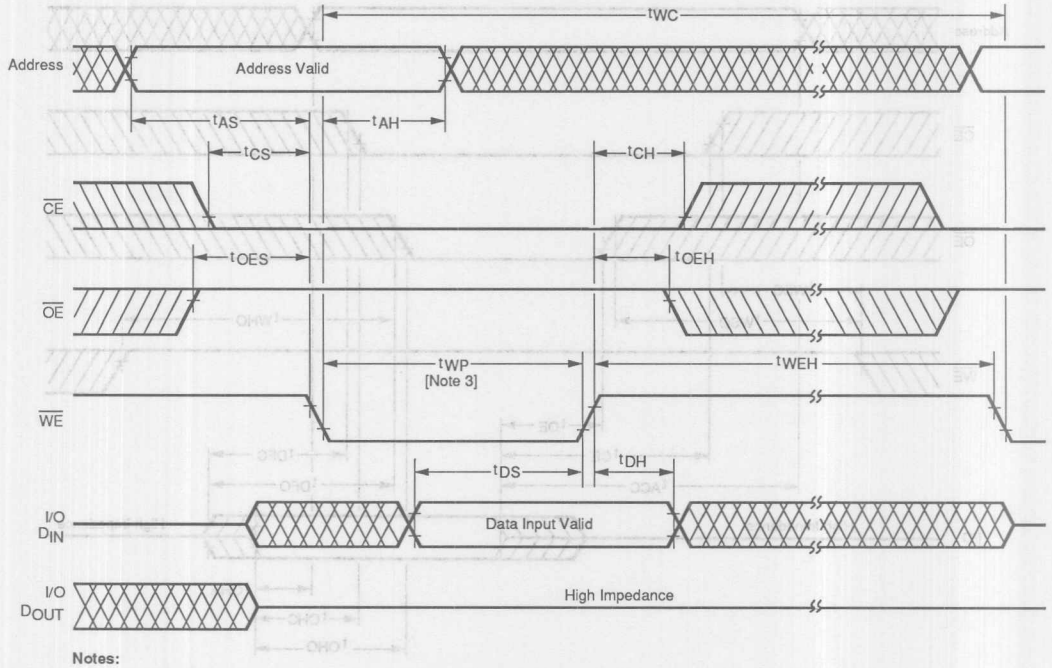
[1] Use t_{DFC} if $\overline{CE}$ transitions to V_{IH} before $\overline{OE}$ transitions to V_{IH}.

[2] Use t_{DFO} if $\overline{OE}$ transitions to V_{IH} before $\overline{CE}$ transitions to V_{IH}.

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Timing Waveforms (cont)

$\overline{WE}$-Controlled Write Cycle



Notes:

[1] The address inputs are latched at the falling edge of $\overline{CE}$ or $\overline{WE}$, whichever occurs later.

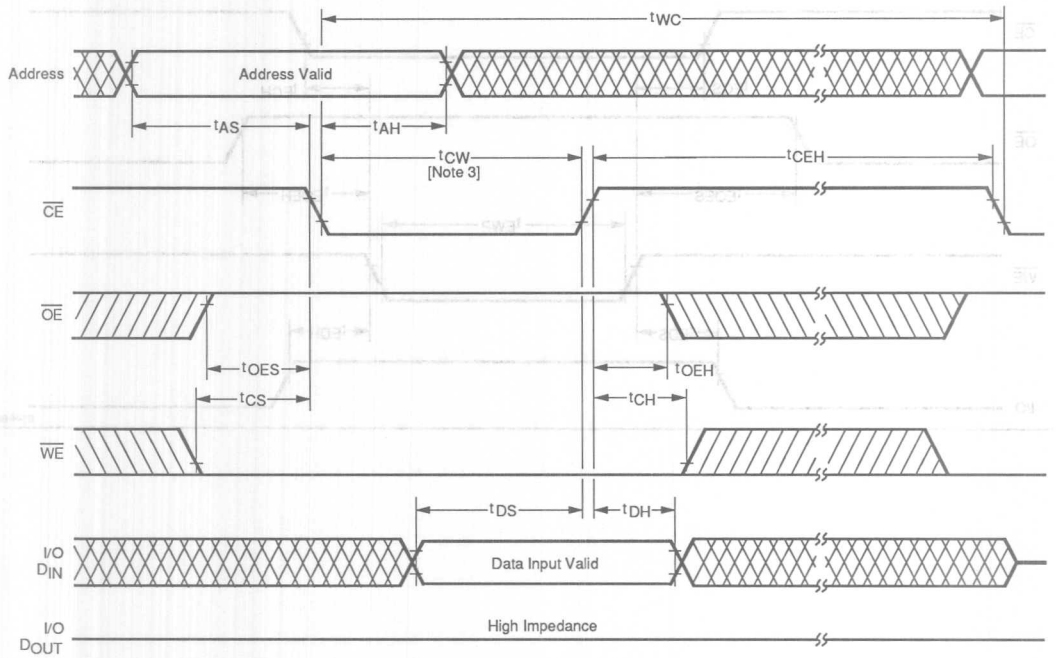
[2] The data inputs are latched at the rising edge of $\overline{CE}$ or $\overline{WE}$, whichever occurs earlier.

[3] Write operation requires both $\overline{CE}$ and $\overline{WE}$ to be at V_{IL}. Parameter t_{WP} is defined only for the period when both $\overline{CE}$ and $\overline{WE}$ are at V_{IL}.

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Timing Waveforms (cont)

$\overline{CE}$-Controlled Write Cycle



Notes:

[1] The address inputs are latched at the falling edge of $\overline{CE}$ or $\overline{WE}$, whichever occurs later.

[2] The data inputs are latched at the rising edge of $\overline{CE}$ or $\overline{WE}$, whichever occurs earlier.

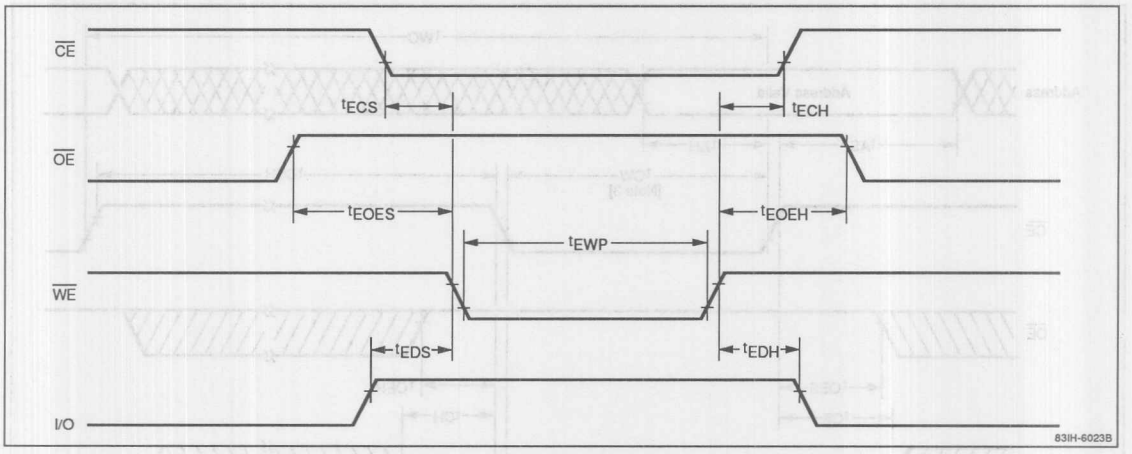
[3] Write operation requires both $\overline{CE}$ and $\overline{WE}$ to be at V_{IL}. Parameter t_{CW} is defined only for the period when both $\overline{CE}$ and $\overline{WE}$ are at V_{IL}.

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Timing Waveforms (cont)

Chip Erase Cycle



Read Cycle

Both $\overline{CE}$ and $\overline{OE}$ must be at V_{IL} in order to read stored data. While the device is executing read cycles, bringing either of these inputs to V_{IH} will place the outputs in a state of high impedance. This two-line output control allows bus contention to be eliminated in the system application.

Byte Write Cycle

Low levels on $\overline{CE}$ and $\overline{WE}$ and a high level on $\overline{OE}$ place the μPD28C04 in write operation. The write address inputs are latched by the falling edge of either $\overline{CE}$ or $\overline{WE}$, whichever occurs later. The data inputs are latched by the rising edge of either $\overline{CE}$ or $\overline{WE}$, whichever occurs earlier. Once byte write cycles begin executing, internal circuits assume all timing control and the byte being addressed is automatically erased and then programmed. The operation is completed within a write cycle time (t_{WC}) of 10 ms.

Chip Erase Cycle

All bytes of the μPD28C04 can be erased simultaneously by making $\overline{CE}$ and $\overline{WE}$ fall to V_{IL} after $\overline{OE}$ has been increased to V_{IHH} (15±0.5 V). The address inputs are "don't care," but the data inputs must all be driven to V_{IH} before the chip erase cycle begins.

$\overline{DATA}$ Polling Feature

This feature supports system software by indicating the precise end of byte write cycles. $\overline{DATA}$ polling can be used to reduce the total programming time of the μPD28C04 to a minimum value, which varies with the system environment.

While internal automatic write cycles are in progress, any attempt to read data at the last externally supplied address location will result in inverted data on pin I/O_7 (for example, if write data = 1xxx xxxx, then read data = 0xxx xxxx). Once the write cycle is complete, a read cycle will result in true data being output on I/O_7.

Write Protection Features

The μPD28C04 provides three features to prevent invalid write cycles:

- Noise immunity, where write operation is inhibited when the $\overline{WE}$ pulse width is 20 ns or less.
- Supply voltage-level detection, where write operation is inhibited when V_{CC} is 2.5 volts or less.
- Write protection logic, where write operation is inhibited if $\overline{OE}$ is held low or $\overline{CE}$ or $\overline{WE}$ is held high during power-on or -off of the V_{CC} supply voltage.

Description

The μPD28C05 is an electrically erasable and programmable read-only memory (EEPROM) organized as 512 words by 8 bits. The device operates from a +5-volt power supply and is fabricated with an advanced CMOS process for high performance and low power consumption.

The device offers an $\overline{ALE}$ pin to control the latching of addresses and a $\overline{DATA}$ polling function to indicate the precise end of write cycles. Additional features include chip erase, auto erase and programming. The μPD28C05 is available in standard 24-pin plastic DIP or miniflat packaging.

Features

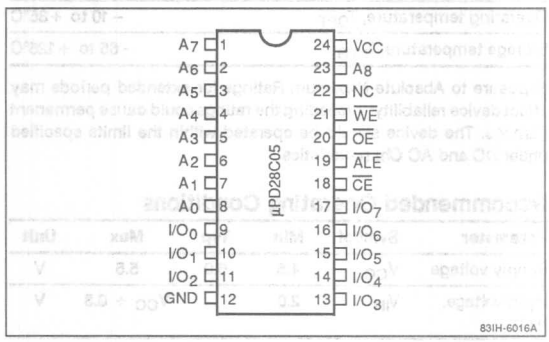
- 512-word by 8-bit organization
- Single +5-volt power supply
- Fast access times of 200 and 250 ns maximum
- Chip erase feature
- Auto erase and programming: 10 ms maximum
- $\overline{DATA}$ polling feature
- Address latching by means of $\overline{ALE}$ pin
- Low power dissipation
  - — 50 mA max
  - — 100 μA max
- Endurance: 100,000 erase/write cycles per byte
- TTL-compatible inputs and outputs
- Three-state outputs
- Advanced CMOS technology
- 24-pin plastic DIP or miniflat packaging

Ordering Information

Part Number	Access Time (max)	Package
μPD28C05C-20	200 ns	24-pin plastic DIP
C-25	250 ns	
μPD28C05G-20	200 ns	24-pin plastic miniflat
G-25	250 ns	

Pin Configuration

24-Pin Plastic DIP or Miniflat



Pin Identification

Symbol	Function
A_0 - A_8	Address inputs
I/O_0 - I/O_7	Data inputs and outputs
$\overline{CE}$	Chip enable
$\overline{OE}$	Output enable
$\overline{WE}$	Write enable
$\overline{ALE}$	Address latch enable
GND	Ground
V_{CC}	+5-volt power supply
NC	No connection

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Absolute Maximum Ratings

Supply voltage, V_{CC}	−0.6 to +7.0 V
Input voltage, V_{I1}	−0.6 to +7.0 V
Input voltage, V_{I2} ($\overline{OE}$)	−0.6 to +16.5 V
Output voltage, V_{OUT}	−0.6 to +7.0 V
Operating temperature, T_{OPT}	−10 to +85°C
Storage temperature, T_{STG}	−65 to +125°C

Exposure to Absolute Maximum Ratings for extended periods may affect device reliability; exceeding the ratings could cause permanent damage. The device should be operated within the limits specified under DC and AC Characteristics.

Recommended Operating Conditions

Parameter	Symbol	Min	Typ	Max	Unit
Supply voltage	V_{CC}	4.5	5.0	5.5	V
Input voltage, high	V_{IH}	2.0		V_{CC} + 0.3	V
Input voltage, low	V_{IL}	−0.3		0.8	V
Operating temperature	T_A	0		70	°C

Capacitance

T_A = 25°C; f = 1 MHz

Parameter	Symbol	Min	Max	Unit
Input capacitance	C_I		12	pF
Output capacitance	C_O		10	pF

Truth Table

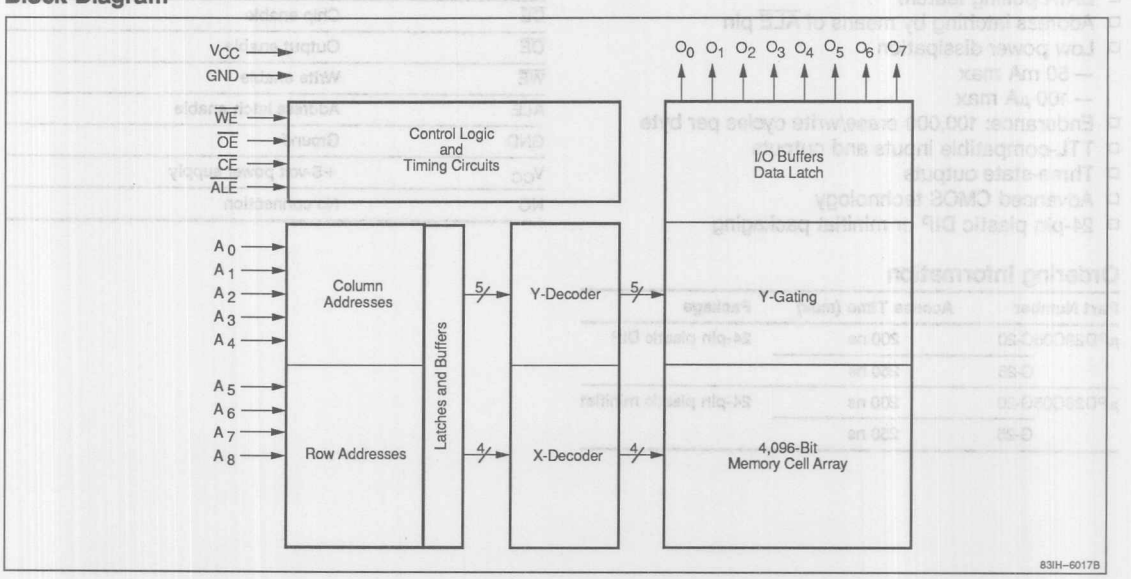
Function	$\overline{CE}$	$\overline{OE}$	$\overline{WE}$	$\overline{ALE}$	I/O	I_{CC}
Read	V_{IL}	V_{IL}	V_{IH}	X	D_{OUT}	Active
Standby and write inhibit	V_{IH}	X	X	X	High-Z	Standby
Write	V_{IL}	V_{IH}	V_{IL}	V_{IH}	D_{IN}	Active
Chip erase	V_{IL}	V_{IHH}	V_{IL}	V_{IH}	$D_{IN} = V_{IH}$	Active
Write inhibit	X	V_{IL}	X	X	—	—
	X	X	V_{IH}	X	—	—

Notes:

(1) X can be either V_{IL} or V_{IH}.

(2) V_{IHH} = +15 ±0.5 V.

Block Diagram



DC Characteristics

T_A = 0 to +70°C; V_{CC} = +5.0 V ± 10%

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions
Output voltage, high	V_{OH1}	2.4			V	I_{OH} = −400 μA
	V_{OH2}	V_{CC} − 0.7			V	I_{OH} = −100 μA
Output voltage, low	V_{OL}			0.45	V	I_{OL} = 2.1 mA
Output leakage current	I_{LO}			10	μA	V_{OUT} = 0 to V_{CC} (max)
Input leakage current	I_{LI}			10	μA	V_{IN} = 0 to V_{CC} (max)
V_{CC} current (active)	I_{CCA1}			20	mA	$\overline{CE}$ = V_{IL}; V_{IN} = V_{IH}
	I_{CCA2}			50	mA	f = 5 MHz; I_{OUT} = 0 mA
V_{CC} current (standby)	I_{CCS1}			1	mA	$\overline{CE}$ = V_{IH}
	I_{CCS2}			100	μA	$\overline{CE}$ = V_{CC}; V_{IN} = 0 to V_{CC}

AC Characteristics

T_A = 0 to +70°C; V_{CC} = +5.0 V ± 10%

		μPD28C05-20		μPD28C05-25			
Parameter	Symbol	Min	Max	Min	Max	Unit	Test Conditions
Read Cycle							
Address to output delay	t_{ACC}		200		250	ns	$\overline{CE}$ = $\overline{OE}$ = V_{IL}; $\overline{ALE}$ = $\overline{WE}$ = V_{IH}
$\overline{ALE}$ to output delay	t_{ALE}		200		250	ns	$\overline{CE}$ = $\overline{OE}$ = V_{IL}; $\overline{WE}$ = V_{IH}
$\overline{CE}$ to output delay	t_{CE}		200		250	ns	$\overline{OE}$ = V_{IL}; $\overline{WE}$ = V_{IH}
$\overline{OE}$ to output delay	t_{OE}	10	75	10	100	ns	$\overline{CE}$ = V_{IL}; $\overline{WE}$ = V_{IH}
$\overline{CE}$ high to output float	t_{DFC}	0	60	0	80	ns	$\overline{OE}$ = V_{IL}; $\overline{WE}$ = V_{IH}
$\overline{OE}$ high to output float	t_{DFO}	0	60	0	80	ns	$\overline{CE}$ = V_{IL}; $\overline{WE}$ = V_{IH}
Output hold time from address change	t_{OHA}	0		0		ns	$\overline{CE}$ = $\overline{OE}$ = V_{IL}; $\overline{ALE}$ = $\overline{WE}$ = V_{IH} (Note 2)
Output hold time from rising edge of $\overline{ALE}$	t_{OHL}	0		0		ns	$\overline{CE}$ = $\overline{OE}$ = V_{IL}; $\overline{WE}$ = V_{IH} (Note 2)
Output hold time from rising edge of $\overline{CE}$	t_{OHC}	0		0		ns	$\overline{OE}$ = V_{IL}; $\overline{WE}$ = V_{IH} (Note 2)
Output hold time from rising edge of $\overline{OE}$	t_{OHO}	0		0		ns	$\overline{CE}$ = V_{IL}; $\overline{WE}$ = V_{IH}
$\overline{ALE}$ high-level pulse width	t_{LL}	40		40		ns	$\overline{WE}$ = V_{IH}
Address setup time to $\overline{ALE}$	t_{ASL}	15		20		ns	$\overline{WE}$ = V_{IH}
Address hold time from $\overline{ALE}$	t_{AHL}	20		30		ns	$\overline{WE}$ = V_{IH}
$\overline{CE}$ setup time to $\overline{ALE}$	t_{CSL}	20		20		ns	$\overline{WE}$ = V_{IH}
$\overline{WE}$ setup time to $\overline{CE}$	t_{WSC}	10		10		ns	$\overline{CE}$ = V_{IH}
$\overline{WE}$ setup time to $\overline{OE}$	t_{WSO}	10		10		ns	$\overline{OE}$ = V_{IH}
$\overline{WE}$ hold time from rising edge of $\overline{OE}$	t_{WHO}	10		10		ns	$\overline{OE}$ = V_{IH}

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AC Characteristics (cont)

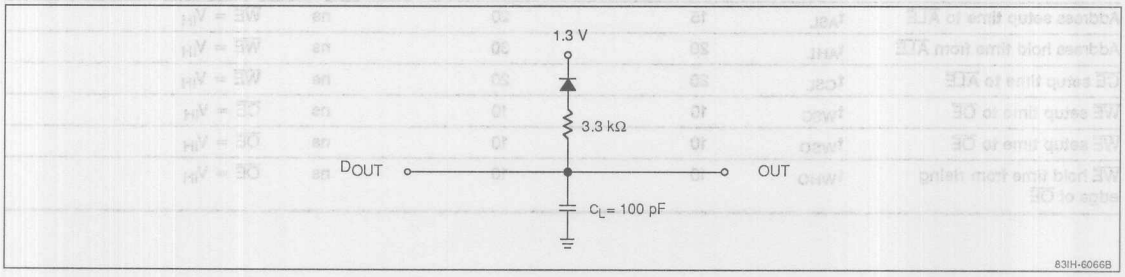
Parameter	Symbol	μPD28C05-20 Min	μPD28C05-20 Max	μPD28C05-25 Min	μPD28C05-25 Max	Unit	Test Conditions
Write Cycle							
Write cycle time	t_{WC}	10		10		ms	
Address setup time to $\overline{WE}$	t_{AS}	10		10		ns	
Address hold time from $\overline{WE}$	t_{AH}	200		200		ns	
$\overline{CE}$ setup time to $\overline{WE}$	t_{CS}	0		0		ns	
$\overline{CE}$ hold time from $\overline{WE}$ high	t_{CH}	0		0		ns	
$\overline{CE}$ pulse width	t_{CW}	150		150		ns	
$\overline{OE}$ high setup time	t_{OES}	10		10		ns	
$\overline{OE}$ high hold time	t_{OEH}	10		10		ns	
$\overline{WE}$ pulse width	t_{WP}	150		150		ns	
Data setup time	t_{DS}	100		100		ns	
Data hold time	t_{DH}	20		20		ns	
$\overline{CE}$ high after $\overline{CE}$-controlled write cycle	t_{CEH}	9.9		9.9		ms	
$\overline{WE}$ high after $\overline{WE}$-controlled write cycle	t_{WEH}	9.9		9.9		ms	
Chip Erase Cycle							
$\overline{CE}$ setup time	t_{ECS}	500		500		ns	
$\overline{OE}$ setup time	t_{EOES}	500		500		ns	
Data setup time	t_{EDS}	500		500		ns	
Data hold time	t_{EDH}	100		100		ns	
$\overline{WE}$ pulse width	t_{EWP}	10		10		ms	
$\overline{CE}$ hold time	t_{ECH}	5		5		μs	
$\overline{OE}$ hold time	t_{EOEH}	t_{ECH} + 3		t_{ECH} + 3		μs	

Notes:

(1) Input rise and fall time ≤ 20 ns; input pulse levels = 0.45 and 2.4 V; timing measurement reference levels = 0.8 and 2.0 V for both inputs and outputs. See figure 1 for output load.

(2) Output hold time is specified either from the address, or from the $\overline{ALE}$, $\overline{OE}$ or $\overline{CE}$ pins, whichever goes invalid first.

Figure 1. Output Load



Read Cycles

$\overline{CE}$ and $\overline{OE}$ must both be at V_{IL} for read cycles to be executed. If either of these inputs rise to V_{IH} while the device is reading stored data, the outputs will be placed in a state of high impedance. This two-line output control eliminates bus contention in the system application.

Byte Write Cycles

Low logic levels on $\overline{CE}$ and $\overline{WE}$ and high logic levels on $\overline{OE}$ and $\overline{ALE}$ place the μPD28C05 in write operation. The write address inputs are latched by the falling edge of either $\overline{CE}$ or $\overline{WE}$, whichever occurs later. The data inputs are latched by the rising edge of either $\overline{CE}$ or $\overline{WE}$, whichever occurs earlier. Once byte write operation has begun, the internal circuitry assumes all timing control and the byte being addressed in automatically erased and then programmed. The operation completes within the write cycle time (t_{WC}) of 10 ms.

Chip Erase Cycles

All bytes of the μPD28C05 can be erased simultaneously by making $\overline{CE}$ and $\overline{WE}$ fall to V_{IL} and $\overline{ALE}$ rise to V_{IH} after $\overline{OE}$ has been increased to V_{IHH} (+15 ± 0.5 V). The address inputs are "don't care," but the data inputs must all be driven to V_{IH} before the chip erase cycle begins.

$\overline{DATA}$ Polling Feature

This feature supports system software by indicating the precise end of byte write cycles and can be used to reduce the total programming time of the μPD28C05 to a minimum value, which varies with the system environment.

While internal automatic write cycles are being executed, any attempt to read data at the last externally supplied address location will result in inverted data on pin I/O_7. For example, if write data = 1xxx xxxx, then read data = 0xxx xxxx. Once write cycles have finished executing, the execution of a subsequent read cycle will result in true data being output on I/O_7.

Write Protection Features

Three features protect against invalid write cycles:

- Noise immunity, where write operation is inhibited when the $\overline{WE}$ pulse width is 20 ns or less;
- Supply voltage-level detection, where write operation is inhibited when V_{CC} is 2.5 volts or less; and
- Write protection logic, where write operation is inhibited if $\overline{OE}$ is held low or $\overline{CE}$ or $\overline{WE}$ is held high during power-on or off of the V_{CC} supply voltage.

Truth Table

Function	$\overline{CE}$	$\overline{OE}$	$\overline{WE}$	$\overline{ALE}$	I/O_0 - I/O_7	I_{CC}
Read	V_{IL}	V_{IL}	V_{IH}	X	D_{OUT}	Active
Standby and write inhibit	V_{IH}	X	X	X	High-Z	Standby
Write	V_{IL}	V_{IH}	V_{IL}	V_{IH}	D_{IN}	Active
Chip erase	V_{IL}	V_{IHH}	V_{IL}	V_{IH}	$D_{IN} = V_{IH}$	Active
Write inhibit	X	V_{IL}	X	X	—	—
	X	X	V_{IH}	X		

Notes:

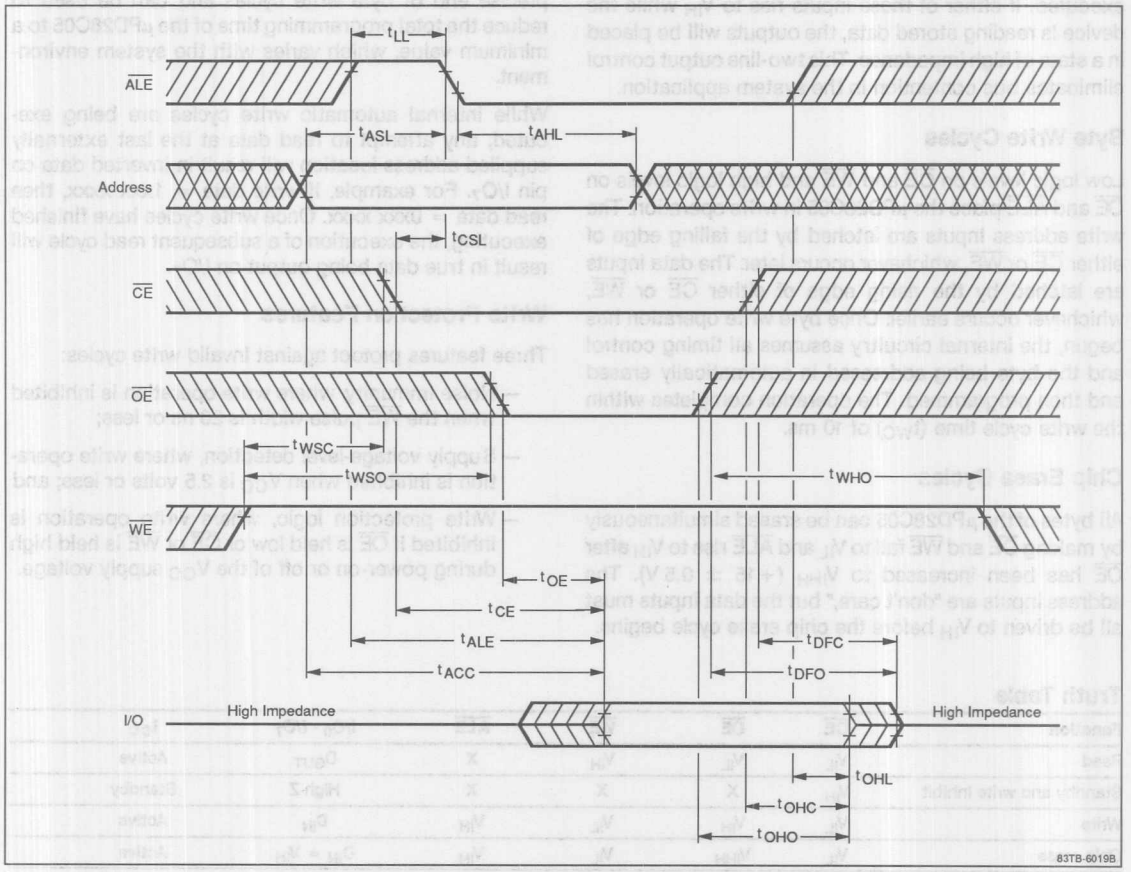
(1) X can be either V_{IL} or V_{IH}.

(2) V_{IHH} = +15 ± 0.5 V.

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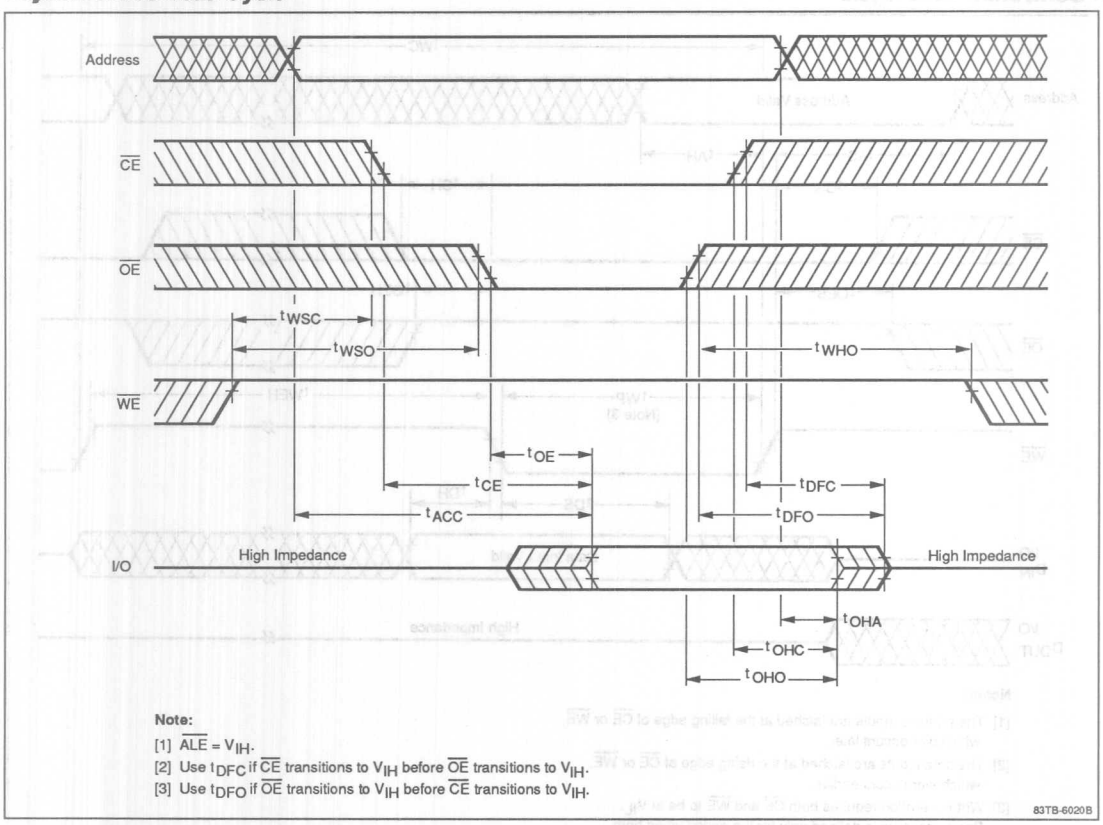
Timing Waveforms

Synchronous Read Cycle ($\overline{ALE}$-Controlled)



Timing Waveforms (cont)

Asynchronous Read Cycle



Note:

[1] $\overline{ALE} = V_{IH}$.

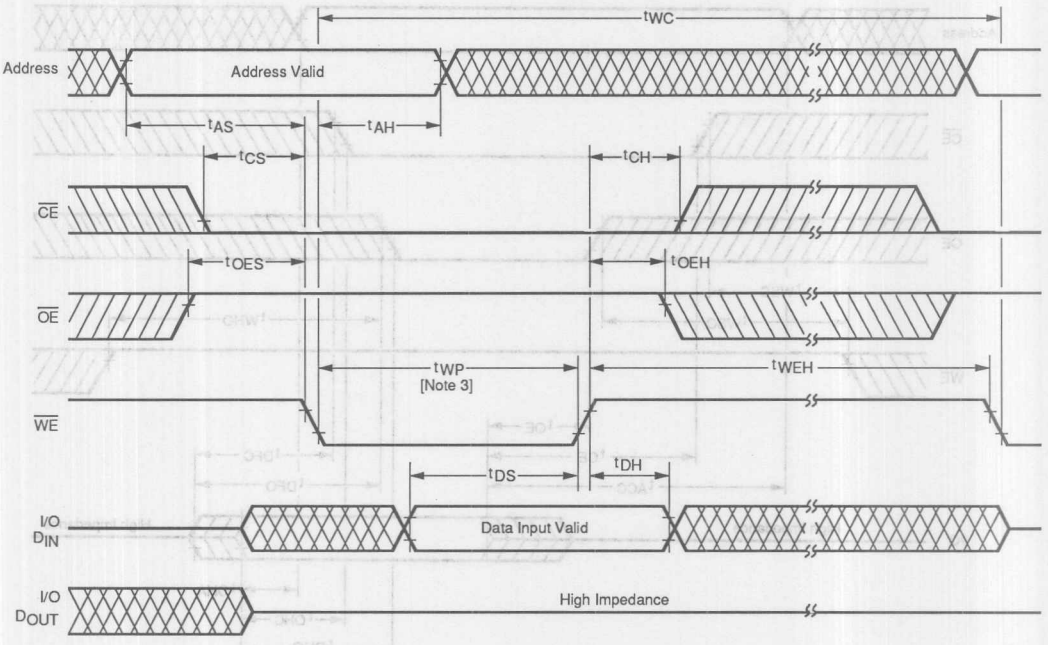
[2] Use t_{DFC} if $\overline{CE}$ transitions to V_{IH} before $\overline{OE}$ transitions to V_{IH}.

[3] Use t_{DFO} if $\overline{OE}$ transitions to V_{IH} before $\overline{CE}$ transitions to V_{IH}.

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Timing Waveforms (cont)

$\overline{WE}$-Controlled Write Cycle



Notes:

[1] The address inputs are latched at the falling edge of $\overline{CE}$ or $\overline{WE}$, whichever occurs later.

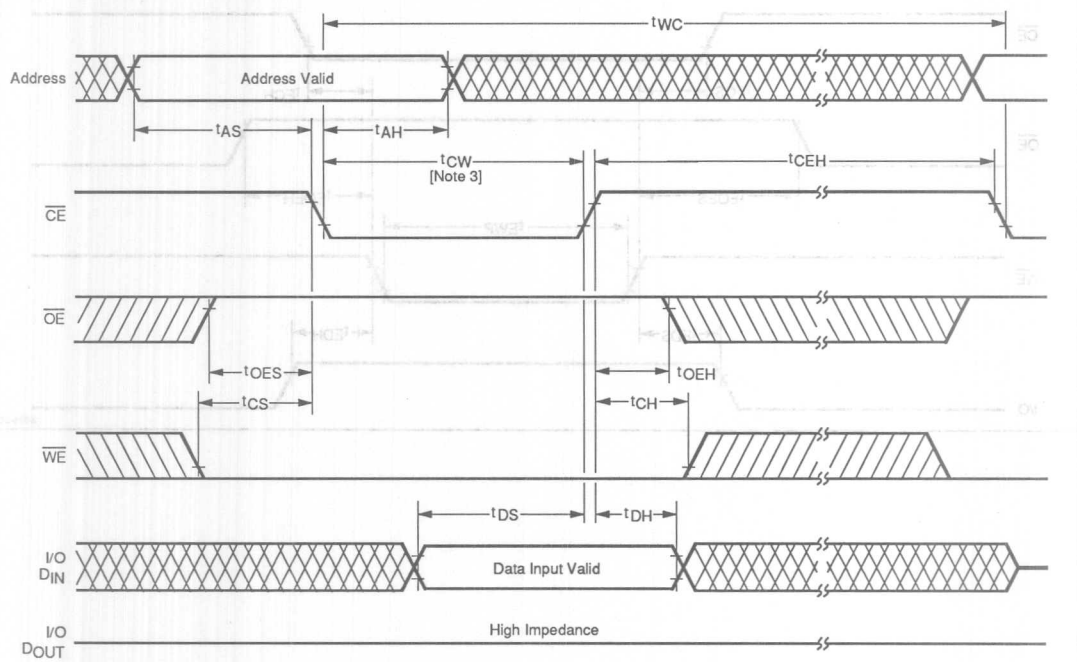
[2] The data inputs are latched at the rising edge of $\overline{CE}$ or $\overline{WE}$, whichever occurs earlier.

[3] Write operation requires both $\overline{CE}$ and $\overline{WE}$ to be at V_{IL}. Parameter t_{WP} is defined only for the period when both $\overline{CE}$ and $\overline{WE}$ are at V_{IL}.

83IH-6223B

Timing Waveforms (cont)

$\overline{CE}$-Controlled Write Cycle



Notes:

[1] The address inputs are latched at the falling edge of $\overline{CE}$ or $\overline{WE}$, whichever occurs later.

[2] The data inputs are latched at the rising edge of $\overline{CE}$ or $\overline{WE}$, whichever occurs earlier.

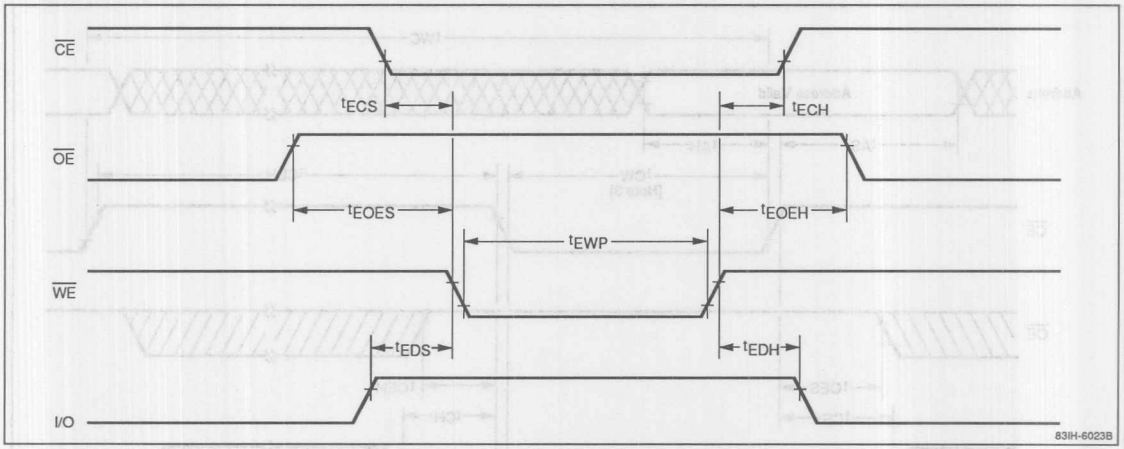
[3] Write operation requires both $\overline{CE}$ and $\overline{WE}$ to be at V_{IL}. Parameter t_{CW} is defined only for the period when both $\overline{CE}$ and $\overline{WE}$ are at V_{IL}.

83IH-6224B

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Timing Waveforms (cont)

Chip Erase Cycle



μPD28C64
8192 x 8-Bit
CMOS EEPROM

Description

The μPD28C64 is a 65,536-bit electrically erasable and programmable read-only memory (EEPROM) organized as 8,192 x 8 bits and fabricated with an advanced CMOS process for high performance and low power consumption.

Operating from a single +5-volt power supply, the μPD28C64 provides $\overline{\text{DATA}}$ polling function to indicate the precise end of write cycles. Additional features include chip erase, auto erase and programming, and 32-byte page write cycles.

The μPD28C64 is available in standard 28-pin plastic DIP.

Features

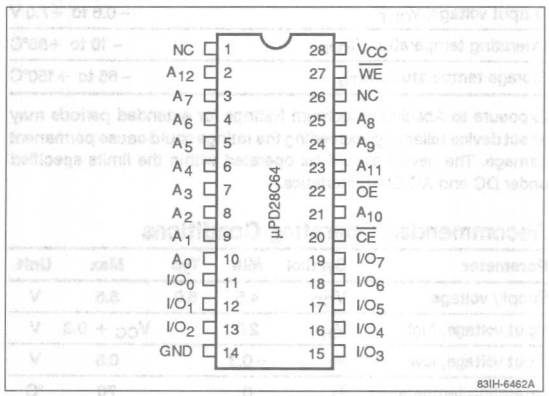
- Single +5-volt power supply
- Chip erase cycles
- Auto erase and programming at 10 ms max
- 32-byte page programming cycles
- $\overline{\text{DATA}}$ polling verification
- Low power dissipation
  - 50 mA max (active)
  - 100 μA max (standby)
- Endurance: 100,000 erase/write cycles per byte
- Silicon signature
- TTL-compatible inputs and outputs
- Three-state outputs
- Advanced CMOS technology
- 28-pin plastic DIP packaging

Ordering Information

Part Number	Access Time (max)	Package
μPD28C64C-20	200 ns	28-pin plastic DIP
C-25	250 ns	

Pin Configuration

28-Pin Plastic DIP



Pin Identification

Symbol	Function
A_0 - A_{12}	Address inputs
I/O_0 - I/O_7	Data inputs and outputs
$\overline{CE}$	Chip enable
$\overline{OE}$	Output enable
$\overline{WE}$	Write enable
GND	Ground
V_{CC}	+5-volt power supply
NC	No connection

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TSOP package will be available in 1991.

Absolute Maximum Ratings

Supply voltage, V_{CC}	−0.6 to +7.0 V
Input voltage, V_{IN}	−0.6 to +7.0 V
Input voltage, (A_9)	−0.6 to +13.5 V
Input voltage, ($\overline{OE}$)	−0.6 to +16.5 V
Output voltage, V_{OUT}	−0.6 to +7.0 V
Operating temperature, T_{OPR}	−10 to +85°C
Storage temperature, T_{STG}	−65 to +150°C

Exposure to Absolute Maximum Ratings for extended periods may affect device reliability; exceeding the ratings could cause permanent damage. The device should be operated within the limits specified under DC and AC Characteristics.

Recommended Operating Conditions

Parameter	Symbol	Min	Typ	Max	Unit
Supply voltage	V_{CC}	4.5	5.0	5.5	V
Input voltage, high	V_{IH}	2.0		V_{CC} + 0.3	V
Input voltage, low	V_{IL}	−0.3		0.8	V
Operating temperature	T_A	0		70	°C

Capacitance

T_A = 25°C; f = 1 MHz; V_{IN} and V_{OUT} = 0 V

Parameter	Symbol	Min	Typ	Max	Unit
Input capacitance	C_I		7	12	pF
Output capacitance	C_O			10	pF

Truth Table

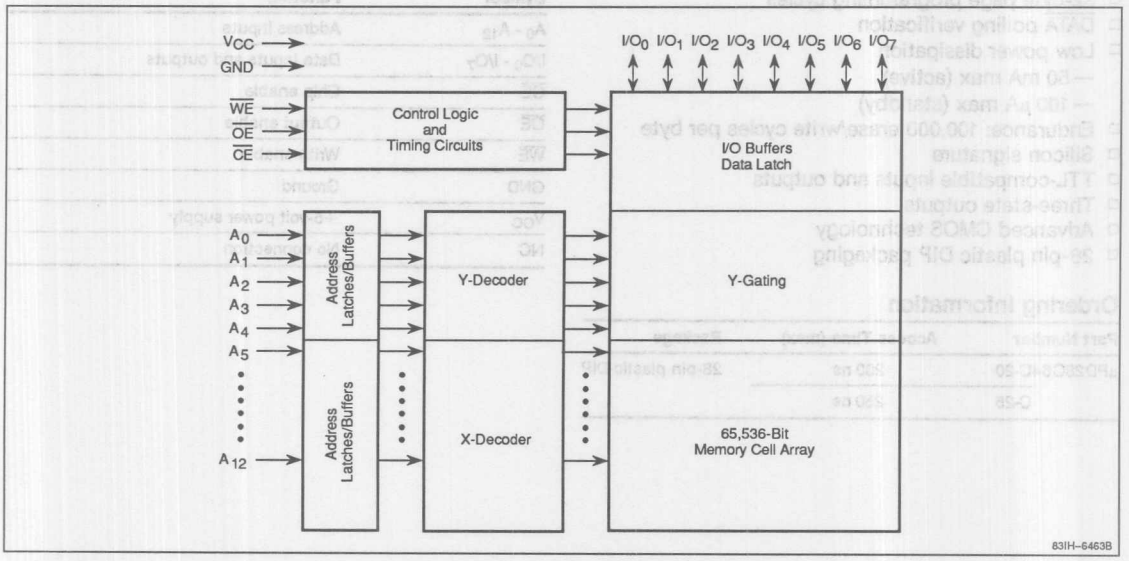
Function	$\overline{CE}$	$\overline{OE}$	$\overline{WE}$	Input/Output	I_{CC}
Read	V_{IL}	V_{IL}	V_{IH}	D_{OUT}	Active
Standby and write inhibit	V_{IH}	X	X	High-Z	Standby
Write	V_{IL}	V_{IH}	V_{IL}	D_{IN}	Active
Chip erase	V_{IL}	V_{IHH}	V_{IL}	D_{IN} = V_{IH}	Active
Write inhibit	X	V_{IL}	X	—	—
	X	X	V_{IH}		

Notes:

(1) X can be either V_{IL} or V_{IH}.

(2) V_{IHH} = +15 V ± 0.5.

Block Diagram



DC Characteristics

T_A = 0 to +70°C; V_{CC} = +5.0 V ± 10%

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions
Output voltage, high	V_{OH1}	2.4			V	I_{OH} = −400 μA
	V_{OH2}	V_{CC} − 0.7			V	I_{OH} = −100 μA
Output voltage, low	V_{OL}			0.45	V	I_{OL} = 2.1 mA
Output leakage current	I_{LO}			10	μA	V_{OUT} = 0 V to V_{CC}; $\overline{CE}$ or $\overline{OE}$ = V_{IH}
Input leakage current	I_{LI}			10	μA	V_{IN} = 0 V to V_{CC}
V_{CC} current (active)	I_{CCA1}			20	mA	$\overline{CE}$ = V_{IL}; $\overline{OE}$ = V_{IH}
	I_{CCA2}			50	mA	f = 5 MHz; I_{OUT} = 0 mA
V_{CC} current (standby)	I_{CCS1}			1	mA	$\overline{CE}$ = V_{IH}
	I_{CCS2}			100	μA	$\overline{CE}$ = V_{CC}; V_{IN} = 0 V to V_{CC}

AC Characteristics

T_A = 0 to +70°C; V_{CC} = +5.0 V ± 10%

		μPD28C64-20		μPD28C64-25			
Parameter	Symbol	Min	Max	Min	Max	Unit	Test Conditions
Read Operation							
Address to output delay	t_{ACC}		200		250	ns	$\overline{CE}$ = $\overline{OE}$ = V_{IL}
$\overline{CE}$ to output delay	t_{CE}		200		250	ns	$\overline{OE}$ = V_{IL}
$\overline{OE}$ to output delay	t_{OE}	10	75	10	100	ns	$\overline{CE}$ = V_{IL}
$\overline{OE}$ or $\overline{CE}$ high to output float	t_{DF}	0	60	0	80	ns	$\overline{CE}$ = V_{IL} or $\overline{OE}$ = V_{IL}
Output hold from address, $\overline{OE}$ or $\overline{CE}$, whichever transition occurs first	t_{OH}	0		0		ns	$\overline{CE}$ = $\overline{OE}$ = V_{IL}

AC Characteristics (cont)

T_A = 0 to +70°C; V_{CC} = +5.0 V ± 10%

Parameter	Symbol	Min	Max	Unit	Test Conditions
Write Operation					
Write cycle time	t_{WC}	10		ms	
Address setup time	t_{AS}	10		ns	
Address hold time	t_{AH}	200		ns	
Write setup time	t_{CS}	0		ns	
Write hold time	t_{CH}	0		ns	
$\overline{CE}$ pulse width	t_{CW}	150		ns	
$\overline{OE}$ high setup time	t_{OES}	10		ns	
$\overline{OE}$ high hold time	t_{OEH}	10		ns	
$\overline{WE}$ pulse width	t_{WP}	150		ns	
$\overline{WE}$ high hold time	t_{WPH}	50		ns	

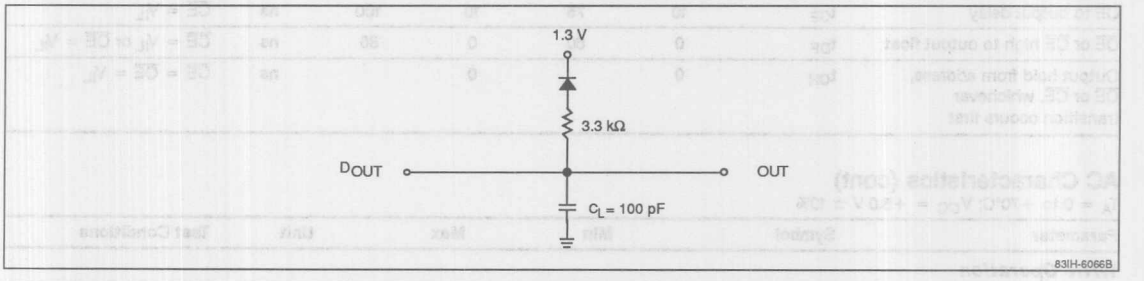
AC Characteristics (cont)

Parameter	Symbol	Min	Max	Unit	Test Conditions
Write Operation					
Data valid time	t_{DV}		300	ns	
Data setup time	t_{DS}	100		ns	
Data hold time	t_{DH}	20		ns	
Byte load cycle time	t_{BLC}	3	100	μs	
Chip Erase Operation					
$\overline{CE}$ setup time	t_{CS}	500		ns	
$\overline{OE}$ setup time	t_{OES}	500		ns	
Data setup time	t_{DS}	500		ns	
Data hold time	t_{DH}	100		ns	
$\overline{WE}$ pulse width	t_{WP}	10		ms	
$\overline{CE}$ hold time	t_{CH}	5		μs	
$\overline{OE}$ hold time	t_{CEH}	t_{CH} + 3		μs	

Notes:

(1) See figure 1 for the output load. Input rise and fall times ≤ 20 ns; input pulse levels = 0.45 and 2.4 V; timing measurement reference levels = 0.8 and 2.0 V for both inputs and outputs.

Figure 1. Output Load



Read Cycles

Both $\overline{CE}$ and $\overline{OE}$ must both be at V_{IL} in order to read stored data. While the device is executing read cycles, bringing either of these inputs to V_{IH} will place the outputs in a state of high impedance. This two-line output control allows bus contention to be eliminated in the system application.

Byte Write Cycles

Low levels on $\overline{CE}$ and $\overline{WE}$ and a high level on $\overline{OE}$ place the μPD28C64 in write operation. Write address inputs are latched by the falling edge of either $\overline{CE}$ or $\overline{WE}$, whichever occurs later. The data inputs are latched by the rising edge of either $\overline{CE}$ or $\overline{WE}$, whichever occurs earlier. Once byte write operation has begun, the internal circuits assume all timing control. The byte being addressed is automatically erased and then programmed. The operation completes within the write cycle time (t_{WC}) of 10 ms.

Page Write Cycle

This option allows the μPD28C64 to be completely programmed in a much shorter time than is required using byte write cycles. The loading of up to 32 bytes of data before internal write cycles program all of these bytes simultaneously allows the μPD28C64 to be completely written in a maximum of 2.6 seconds. The page address is specified by the inputs A_5 through A_{12}; once set, this address cannot be changed during a page write cycle. Within the page, address inputs A_0 through A_4 can be used sequentially or in random order to specify individual bytes.

The beginning of a page write cycle is the same as a $\overline{WE}$-controlled byte write cycle. If the next falling edge of $\overline{WE}$ occurs within a byte load cycle time of 100 μs, the internal byte load register will be loaded with another byte of input data. This cycle can be repeated to load a maximum of 32 bytes of data. At any point in the sequence, if $\overline{WE}$ does not have a new falling edge within the byte load cycle time of 100 μs, byte load operation will terminate and automatic erasing and programming operations will begin.

Chip Erase Cycles

All bytes of the μPD28C64 can be erased simultaneously by making $\overline{CE}$ and $\overline{WE}$ fall to V_{IL} after $\overline{OE}$ has been increased to V_{IHH} (15 V ±0.5). The address inputs are "don't care," but the data inputs must all be driven to V_{IH} before the chip erase cycle begins.

$\overline{DATA}$ Polling Feature

This feature supports system software by indicating the precise end of byte write and page write cycles. $\overline{DATA}$ polling can be used to reduce total programming time of the μPD28C64 to a minimum value, which varies with the system environment.

While internal automatic write operation is in progress, any attempt to read data at the last externally supplied address location will result in inverted data on pin I/O_7 (for example, if write data = 1xxx xxxx, then read data = 0xxx xxxx). Once the write cycle is complete, a read cycle will result in true data being output on I/O_7.

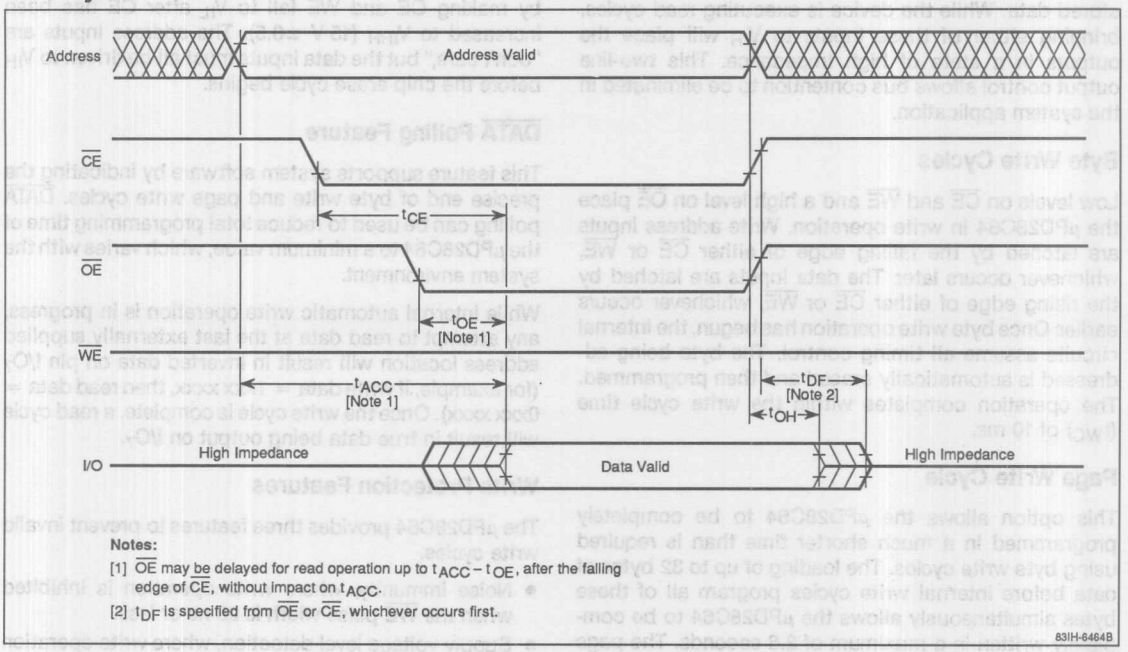
Write Protection Features

The μPD28C64 provides three features to prevent invalid write cycles.

- Noise immunity, where write operation is inhibited when the $\overline{WE}$ pulse width is 20 ns or less.
- Supply voltage level detection, where write operation is inhibited when V_{CC} is 2.5 V or less.
- Write protection logic, where write operation is inhibited if $\overline{OE}$ is held low or $\overline{CE}$ or $\overline{WE}$ is held high during power on or off of the V_{CC} supply voltage.

Timing Waveforms

Read Cycle



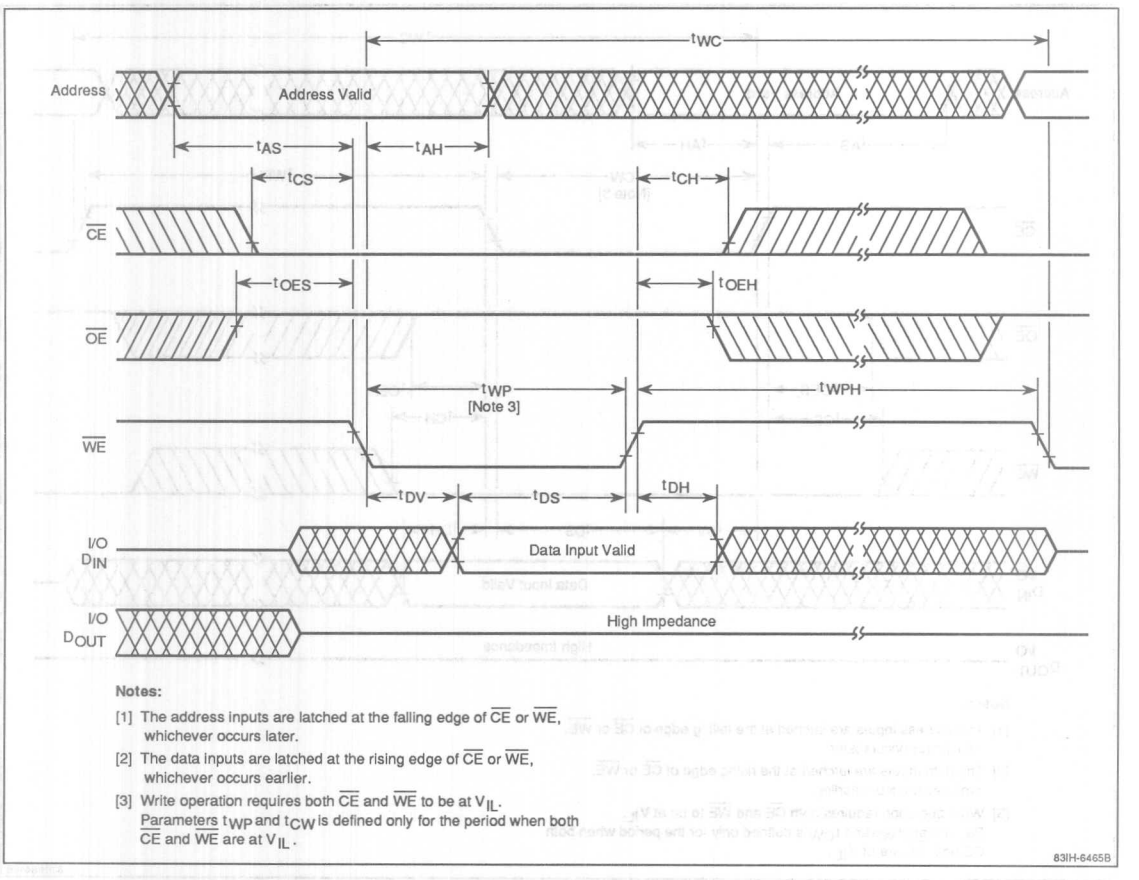
Notes:

[1] $\overline{OE}$ may be delayed for read operation up to $t_{ACC} - t_{OE}$, after the falling edge of $\overline{CE}$, without impact on t_{ACC}.

[2] t_{DF} is specified from $\overline{OE}$ or $\overline{CE}$, whichever occurs first.

Timing Waveforms (cont)

$\overline{WE}$-Controlled Write Cycle



Notes:

[1] The address inputs are latched at the falling edge of $\overline{CE}$ or $\overline{WE}$, whichever occurs later.

[2] The data inputs are latched at the rising edge of $\overline{CE}$ or $\overline{WE}$, whichever occurs earlier.

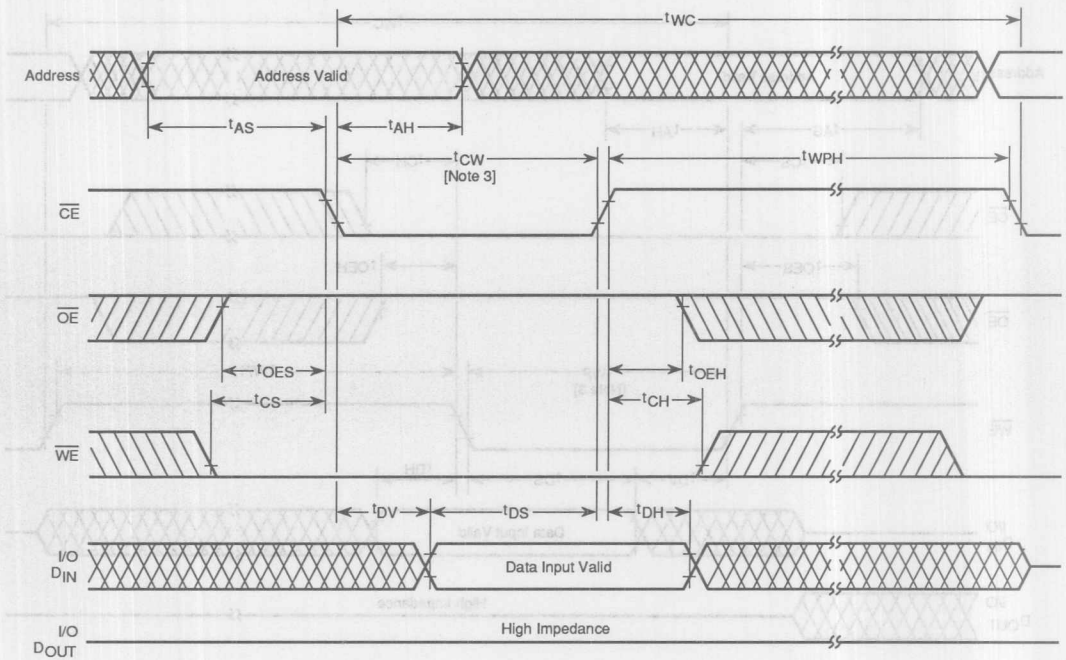
[3] Write operation requires both $\overline{CE}$ and $\overline{WE}$ to be at V_{IL}. Parameters t_{WP} and t_{CW} is defined only for the period when both $\overline{CE}$ and $\overline{WE}$ are at V_{IL}.

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Timing Waveforms (cont)

$\overline{CE}$-Controlled Write Cycle



Notes:

[1] The address inputs are latched at the falling edge of $\overline{CE}$ or $\overline{WE}$, whichever occurs later.

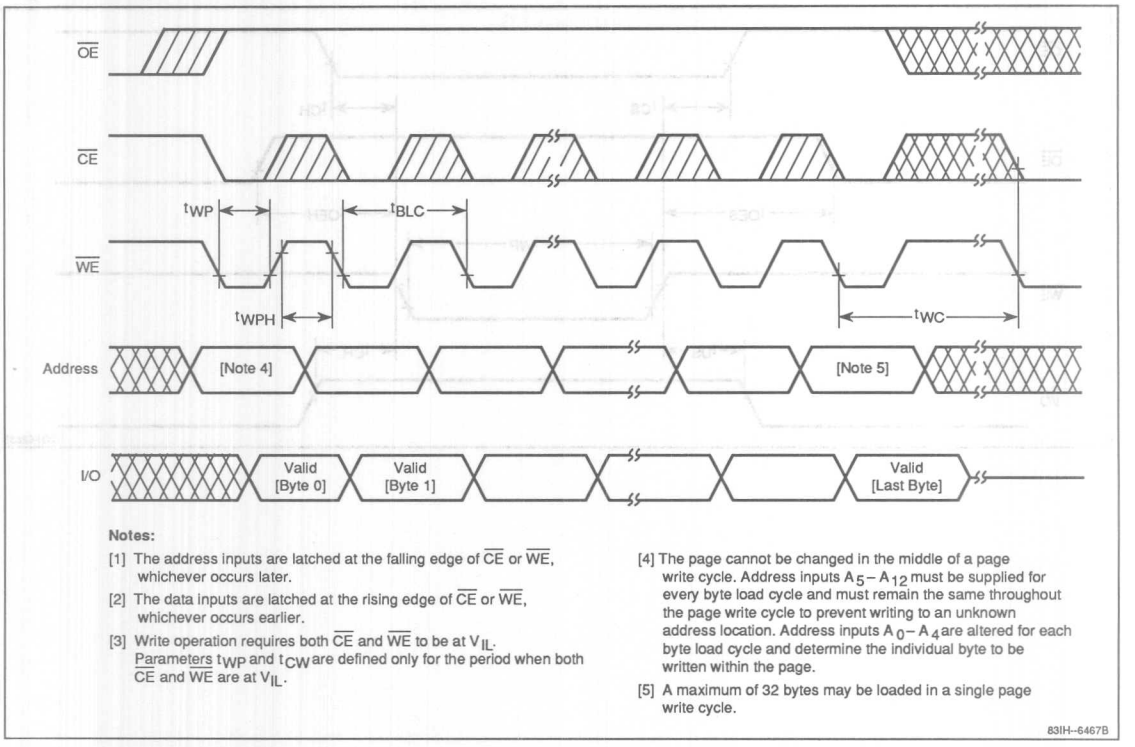
[2] The data inputs are latched at the rising edge of $\overline{CE}$ or $\overline{WE}$, whichever occurs earlier.

[3] Write operation requires both $\overline{CE}$ and $\overline{WE}$ to be at V_{IL}. Parameters t_{WP} and t_{CW} is defined only for the period when both $\overline{CE}$ and $\overline{WE}$ are at V_{IL}.

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Timing Waveforms (cont)

Page Write Cycle



Notes:

[1] The address inputs are latched at the falling edge of $\overline{CE}$ or $\overline{WE}$, whichever occurs later.

[2] The data inputs are latched at the rising edge of $\overline{CE}$ or $\overline{WE}$, whichever occurs earlier.

[3] Write operation requires both $\overline{CE}$ and $\overline{WE}$ to be at V_{IL}. Parameters t_{WP} and t_{CW} are defined only for the period when both $\overline{CE}$ and $\overline{WE}$ are at V_{IL}.

[4] The page cannot be changed in the middle of a page write cycle. Address inputs $A_5 - A_{12}$ must be supplied for every byte load cycle and must remain the same throughout the page write cycle to prevent writing to an unknown address location. Address inputs $A_0 - A_4$ are altered for each byte load cycle and determine the individual byte to be written within the page.

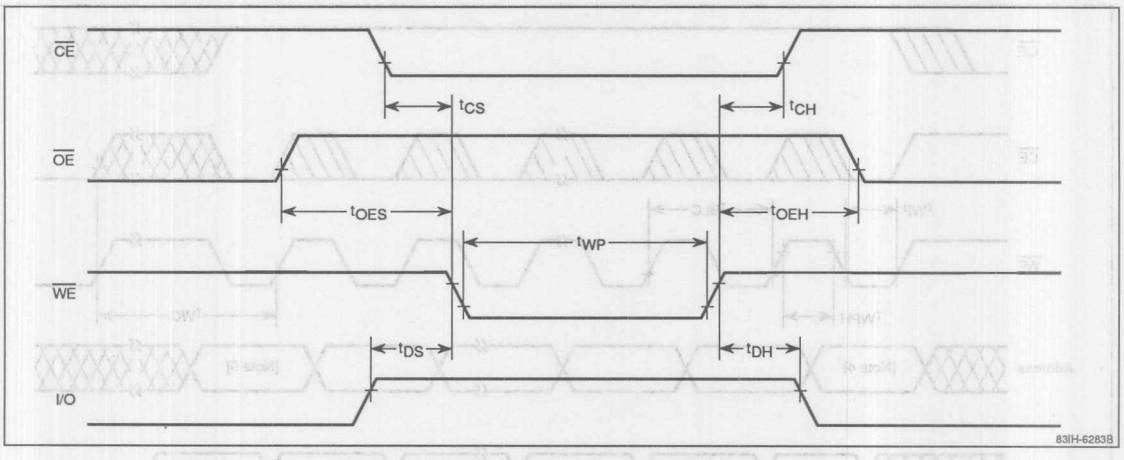
[5] A maximum of 32 bytes may be loaded in a single page write cycle.

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Timing Waveforms (cont)

Chip Erase Cycle



NEC Electronics Inc.

μPD28C256
32,768 x 8-Bit
CMOS EEPROM

PRELIMINARY INFORMATION

Description

The μPD28C256 is a 262,144-bit electrically erasable and programmable read-only memory (EEPROM) organized as 32,768 x 8 bits and fabricated with an advanced CMOS process for high performance and low power consumption.

Operating from a single +5-volt power supply, the μPD28C256 provides $\overline{\text{DATA}}$ polling and toggle bit functions to indicate the precise end of write cycles. Additional features include software data protection, software chip erase, auto erase and programming, and 64-byte page write operation using automatic write timing and internal address and data latches.

The μPD28C256 is available in standard 28-pin plastic DIP packaging.

Features

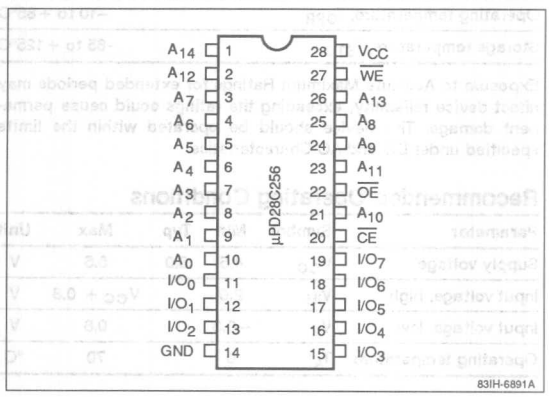
- Single +5-volt power supply
- Fast access time of 200 ns (max)
- Software chip erase cycles
- Auto erase and programming at 10 ms (max)
- 64-byte page programming cycles
- End of write detection
  - — $\overline{\text{DATA}}$ polling
  - — Toggle bit
- Software data protection
- Low power dissipation
  - — 50 mA max (active)
  - — 100 μA max (standby)
- 10,000 erase/write cycles per byte
- Silicon signature included
- Advanced CMOS technology
- 28-pin plastic DIP packaging

Ordering Information

Part Number	Access Time (max)	Package
μPD28C256CZ-20	200 ns	28-pin plastic DIP
CZ-25	250 ns	

Pin Configuration

28-Pin Plastic DIP



Pin Identification

Symbol	Function
A_0 - A_{14}	Address inputs
I/O_0 - I/O_7	Data inputs and outputs
$\overline{CE}$	Chip enable
$\overline{OE}$	Output enable
$\overline{WE}$	Write enable
GND	Ground
V_{CC}	+5-volt power supply

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Absolute Maximum Ratings

Supply voltage, V_{CC}	−0.6 to +7.0 V
Input voltage, V_{IN}	−0.6 to V_{CC} + 0.3 V
Input voltage (A_9)	−0.6 to +13.5 V
Output voltage, V_{OUT}	−0.6 to +7.0 V
Operating temperature, T_{OPR}	−10 to +85°C
Storage temperature, T_{STG}	−65 to +125°C

Exposure to Absolute Maximum Ratings for extended periods may affect device reliability; exceeding the ratings could cause permanent damage. The device should be operated within the limits specified under DC and AC Characteristics.

Recommended Operating Conditions

Parameter	Symbol	Min	Typ	Max	Unit
Supply voltage	V_{CC}	4.5	5.0	5.5	V
Input voltage, high	V_{IH}	2.0		V_{CC} + 0.3	V
Input voltage, low	V_{IL}	−0.3		0.8	V
Operating temperature	T_A	0		70	°C

Capacitance

T_A = 25°C; f = 1 MHz; V_{IN} and V_{OUT} = 0 V

Parameter	Symbol	Min	Typ	Max	Unit
Input capacitance	C_I			12	pF
Output capacitance	C_O			10	pF

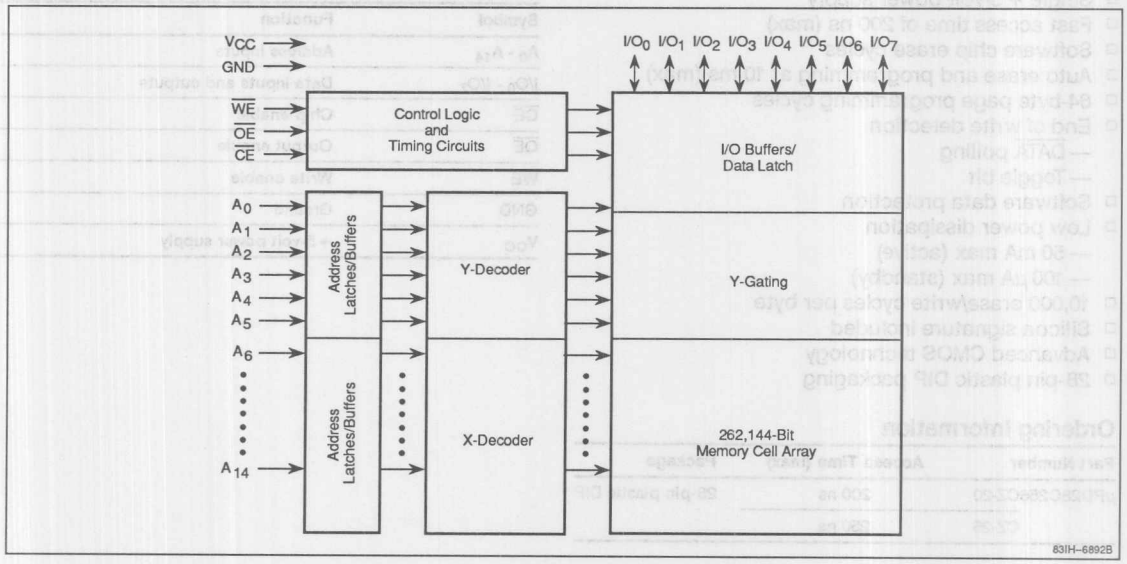
Truth Table

Function	$\overline{CE}$	$\overline{OE}$	$\overline{WE}$	Input/Output	I_{CC}
Read	V_{IL}	V_{IL}	V_{IH}	D_{OUT}	Active
Standby and write inhibit	V_{IH}	X	X	High-Z	Standby
Write	V_{IL}	V_{IH}	V_{IL}	D_{IN}	Active
Write Inhibit	X	V_{IL}	X	—	—
	X	X	V_{IH}		

Notes:

(1) X can be either V_{IL} or V_{IH}.

Block Diagram



DC Characteristics

T_A = 0 to +70°C; V_{CC} = +5.0 V ± 10%

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions
Output voltage, high	V_{OH1}	2.4			V	I_{OH} = −400 μA
	V_{OH2}	V_{CC} − 0.7			V	I_{OH} = −100 μA
Output voltage, low	V_{OL}			0.45	V	I_{OL} = 2.1 mA
Output leakage current	I_{LO}	−10		10	μA	V_{OUT} = 0 V to V_{CC}; $\overline{CE}$ or $\overline{OE}$ = V_{IH}
Input leakage current	I_{LI}	−10		10	μA	V_{IN} = 0 V to V_{CC}
V_{CC} current (active)	I_{CCA1}			20	mA	$\overline{CE}$ = V_{IL}; V_{IN} = V_{IH}
	I_{CCA2}			50	mA	f = 5 MHz; I_{OUT} = 0 mA
V_{CC} current (standby)	I_{CCS1}			1	mA	$\overline{CE}$ = V_{IH}
	I_{CCS2}			100	μA	$\overline{CE}$ = V_{CC}; V_{IN} = 0 V to V_{CC}

AC Characteristics

T_A = 0 to +70°C; V_{CC} = +5.0 V ± 10%

		μPD28C256-20		μPD28C256-25			
Parameter	Symbol	Min	Max	Min	Max	Unit	Test Conditions
Read Operation							
Address to output delay	t_{ACC}		200		250	ns	$\overline{CE}$ = $\overline{OE}$ = V_{IL}
$\overline{CE}$ to output delay	t_{CE}		200		250	ns	$\overline{OE}$ = V_{IL}
$\overline{OE}$ to output delay	t_{OE}	10	75	10	100	ns	$\overline{CE}$ = V_{IL}
$\overline{OE}$ or $\overline{CE}$ high to output float	t_{DF}	0	60	0	80	ns	$\overline{CE}$ = V_{IL} or $\overline{OE}$ = V_{IL}
Output hold from address, $\overline{OE}$ or $\overline{CE}$, whichever transition occurs first	t_{OH}	0		0		ns	$\overline{CE}$ = $\overline{OE}$ = V_{IL}
Write Operation							
Write cycle time	t_{WC}	10		10		ms	
Address setup time	t_{AS}	10		10		ns	
Address hold time	t_{AH}	200		200		ns	
Write setup time	t_{CS}	0		0		ns	
Write hold time	t_{CH}	0		0		ns	
$\overline{CE}$ pulse width	t_{CW}	150		150		ns	
$\overline{OE}$ high setup time	t_{OES}	10		10		ns	
$\overline{OE}$ high hold time	t_{OEH}	50		50		ns	
$\overline{WE}$ pulse width	t_{WP}	150		150		ns	
$\overline{WE}$ high pulse width	t_{WPH}	2		2		μs	
$\overline{WE}$ high hold time	t_{WEH}	9.9		9.9		ms	
$\overline{CE}$ high hold time	t_{CEH}	9.9		9.9		ms	
Data setup time	t_{DS}	100		100		ns	
Data hold time	t_{DH}	50		50		ns	
Byte load cycle time	t_{BLC}	3	100	3	100	μs	

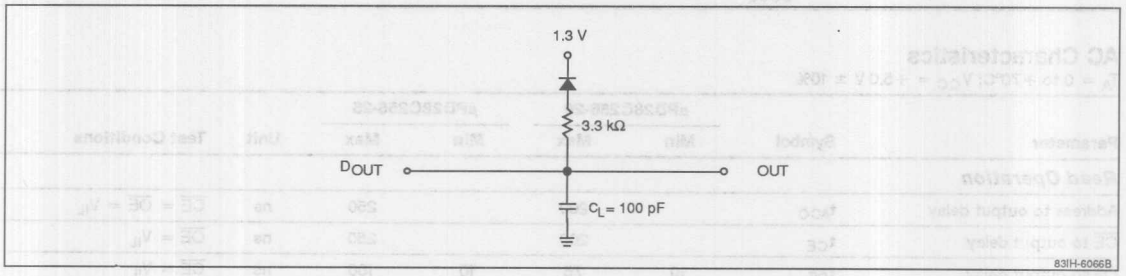
AC Characteristics (cont)

Parameter	Symbol	μPD28C256-20 Min	μPD28C256-20 Max	μPD28C256-25 Min	μPD28C256-25 Max	Unit	Test Conditions
Software Chip Erase Operation							
$\overline{CE}$ setup time	t_{ECS}	500		500		ns	
$\overline{WE}$ pulse width	t_{EWP}	10		10		ms	
$\overline{CE}$ hold time	t_{ECH}	20		20		μs	

Notes:

(1) See figure 1 for the output load. Input rise and fall times ≤ 20 ns; input pulse levels = 0.45 and 2.4 V; timing measurement reference levels = 0.8 and 2.0 V for both inputs and outputs.

Figure 1. Output Load



Read Cycles

Both $\overline{CE}$ and $\overline{OE}$ must be at V_{IL} to enable stored data to be read. While the device is executing read cycles, bringing either of these inputs to V_{IH} will place the outputs in high impedance. This two-line output control allows bus contention to be eliminated in the system application.

Byte Write Cycles

Low levels on $\overline{CE}$ and $\overline{WE}$ and a high level on $\overline{OE}$ place the μPD28C256 in write operation. Write address inputs are latched by the falling edge of either $\overline{CE}$ or $\overline{WE}$, whichever occurs later. Data inputs are latched by the rising edge of either $\overline{CE}$ or $\overline{WE}$, whichever occurs earlier. Once byte write operation has begun, the internal circuits assume all timing control and the byte being addressed is automatically erased and then programmed within the write cycle time (t_{WC}) of 10 ms.

Page Write Cycles

This option allows the μPD28C256 to be completely programmed in a much shorter time than is required by byte write cycles. Page write cycles can program up to 64 bytes simultaneously, enabling the μPD28C256 to be completely written within a maximum of 5.2 seconds. The page address is specified by the inputs A_6 through A_{14}; once set, this address cannot be changed. Within the page, address inputs A_0 through A_5 can be used sequentially or in random order to specify individual bytes.

The beginning of a page write cycle is the same as a $\overline{WE}$-controlled byte write cycle. If the next falling edge of $\overline{WE}$ occurs within a byte load cycle time of 100 μs, the internal byte register will be loaded with another byte of input data. This cycle can be repeated to load a maximum of 64 bytes of data. At any point in the sequence, if $\overline{WE}$ does not have a new falling edge within the cycle time of 100 μs, byte loading will terminate and automatic erasing and programming operations will begin.

$\overline{DATA}$ Polling Feature

This feature supports system software by indicating the precise end of byte write and page write cycles. $\overline{DATA}$ polling can be used to reduce total programming time of the μPD28C256 to a minimum value, which varies with the system environment.

While internal automatic write operation is in progress, any attempt to read data at the last externally supplied address location will result in inverted data on pin I/O_7 (for example, if write data = 1xxx xxxx, then read data = 0xxx xxxx). Once the write cycle is complete, a read cycle will result in true data being output on I/O_7.

Toggle Bit Feature

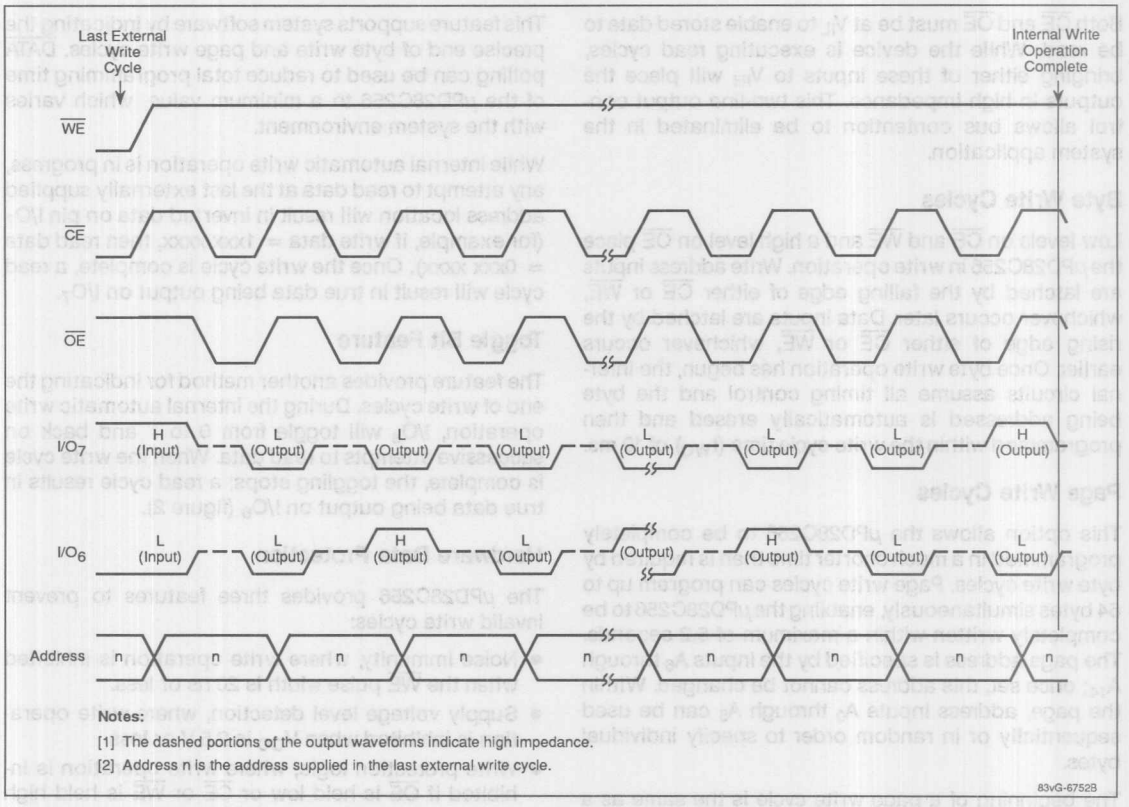
The feature provides another method for indicating the end of write cycles. During the internal automatic write operation, I/O_6 will toggle from 0 to 1 and back on successive attempts to read data. When the write cycle is complete, the toggling stops; a read cycle results in true data being output on I/O_6 (figure 2).

Hardware Data Protection

The μPD28C256 provides three features to prevent invalid write cycles:

- Noise immunity, where write operation is inhibited when the $\overline{WE}$ pulse width is 20 ns or less.
- Supply voltage level detection, where write operation is inhibited when V_{CC} is 2.5 V or less.
- Write protection logic, where write operation is inhibited if $\overline{OE}$ is held low or $\overline{CE}$ or $\overline{WE}$ is held high during power on or off of the V_{CC} supply voltage.

Figure 2. Data Polling and Toggle Bit Operation



Notes:

[1] The dashed portions of the output waveforms indicate high impedance.

[2] Address n is the address supplied in the last external write cycle.

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Software Data Protection

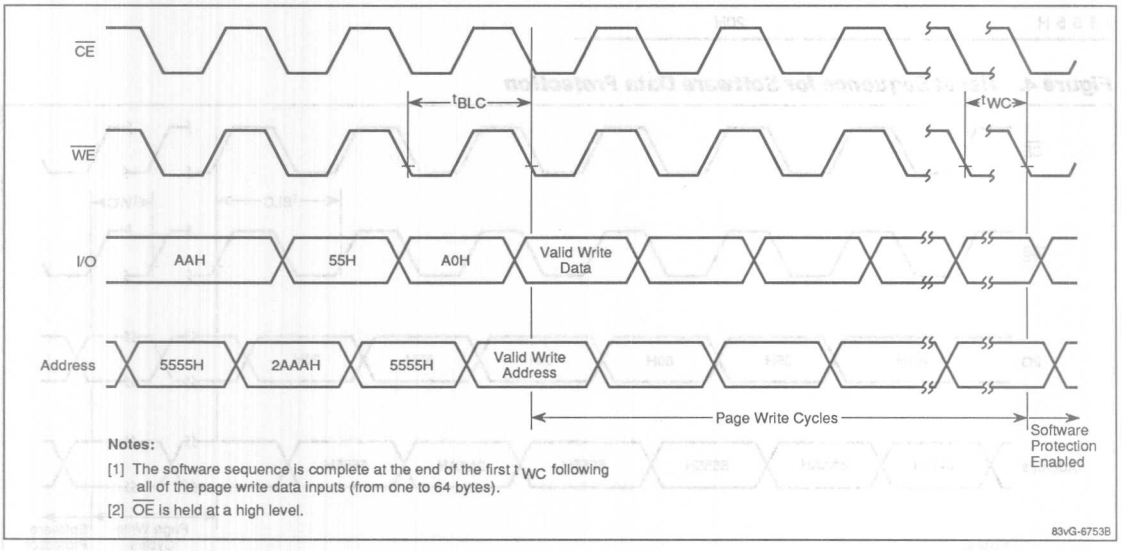
Additional protection of data is available using software control. Standard, unprotected write cycles are illustrated in the timing waveforms. Additional software-controlled protection is enabled or reset with two special sequences of write cycles. To enable software data protection, or to execute additional write cycles after the μPD28C256 is in a protected state, use the address and data sequence shown in table 1. All three byte write cycles must be issued in sequence and must meet the timing illustrated in figure 3.

Table 1. Sequence to Enable Software Data Protection

Address Input (Hex)	Write Data (Hex)
5555H	AAH
2AAAH	55H
5555H	A0H

Under software protection, no write cycles will be executed unless preceded by the above sequence. The protection circuit is nonvolatile and continues to protect the data during power-down and power-up.

Figure 3. Sequence to Initiate or Continue Software Data Protection



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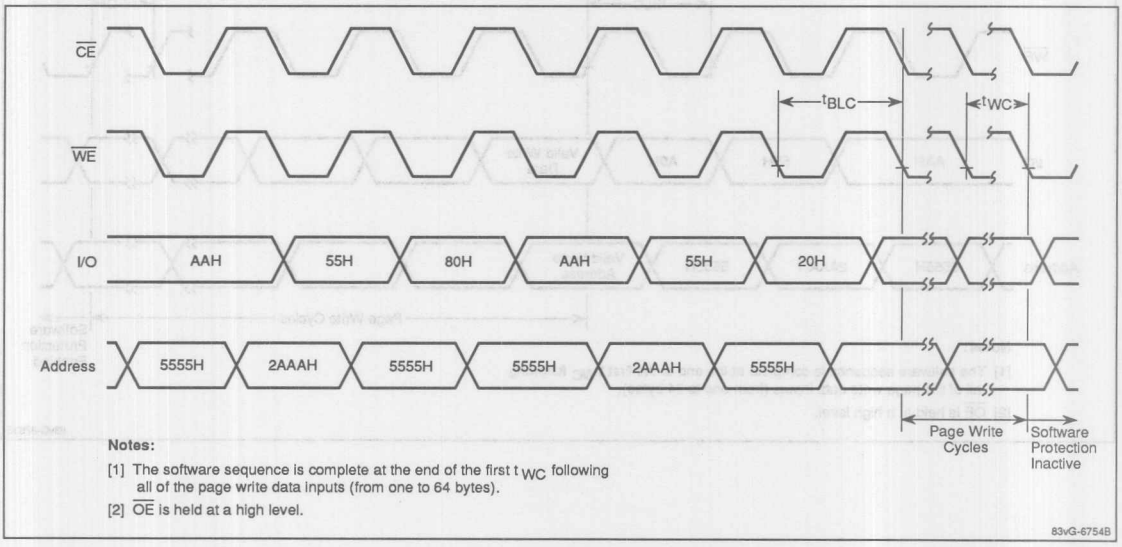
To disable software protection for ease in testing or reprogramming of the μPD28C256, the byte reset sequence shown in table 2 must be issued. The timing is illustrated in figure 4.

Table 2. Sequence to Disable Software Data Protection

Address Input (Hex)	Write Data (Hex)
5 5 5 5 H	AAH
2 A A A H	55H
5 5 5 5 H	80H
5 5 5 5 H	AAH
2 A A A H	55H
5 5 5 5 H	20H

At the end of this sequence, and after a minimum delay of t_{WC} to reset the nonvolatile protection circuit, the μPD28C256 is in an unprotected state. Any standard write cycle can be executed as desired. In this state, the hardware features provide all data protection.

Figure 4. Reset Sequence for Software Data Protection



Notes:

[1] The software sequence is complete at the end of the first t_{WC} following all of the page write data inputs (from one to 64 bytes).

[2] $\overline{OE}$ is held at a high level.

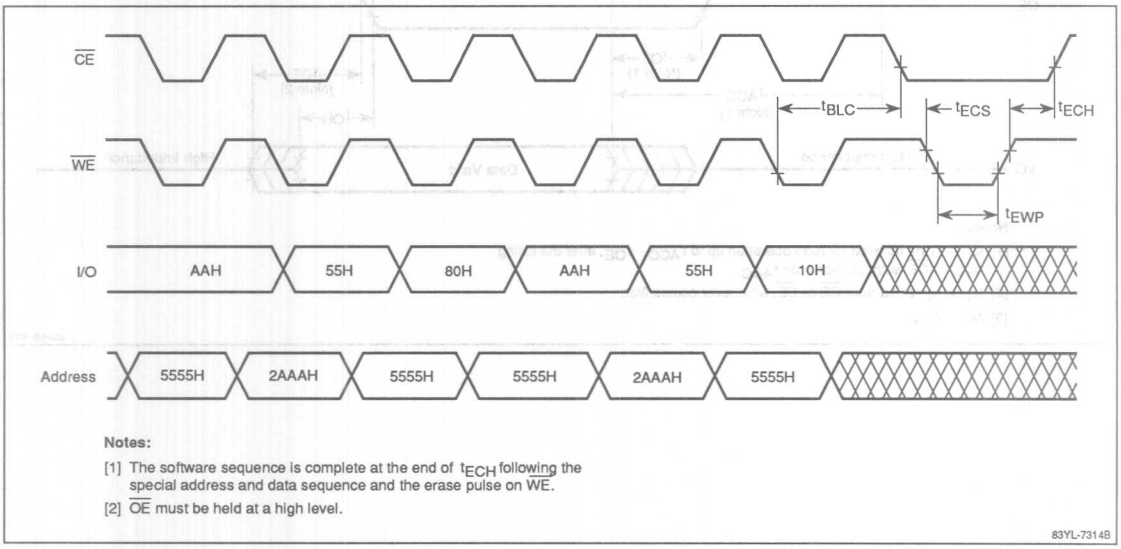
Software Chip Erase Feature

All bytes of the μPD28C256 can be erased simultaneously by making $\overline{CE}$ and then $\overline{WE}$ fall to V_{IL} using the address and data sequence shown in table 3. The required timing is illustrated in figure 5.

Table 3. Sequence to Set Up Software Chip Erase

Address Input (Hex)	Write Data (Hex)
5 5 5 5 H	AAH
2 A A A H	55H
5 5 5 5 H	80H
5 5 5 5 H	AAH
2 A A A H	55H
5 5 5 5 H	10H

Figure 5. Sequence for Software Chip Erase



Notes:

[1] The software sequence is complete at the end of t_{ECH} following the special address and data sequence and the erase pulse on $\overline{WE}$.

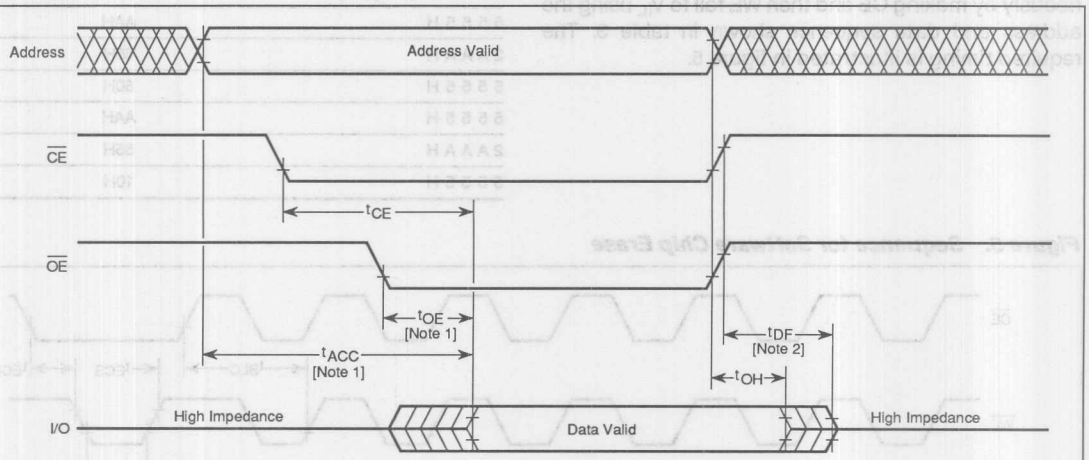
[2] $\overline{OE}$ must be held at a high level.

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Timing Waveforms

Read Cycle



Notes:

[1] $\overline{OE}$ may be delayed for read operation up to $t_{ACC} - t_{OE}$, after the falling edge of $\overline{CE}$, without impact on t_{ACC}.

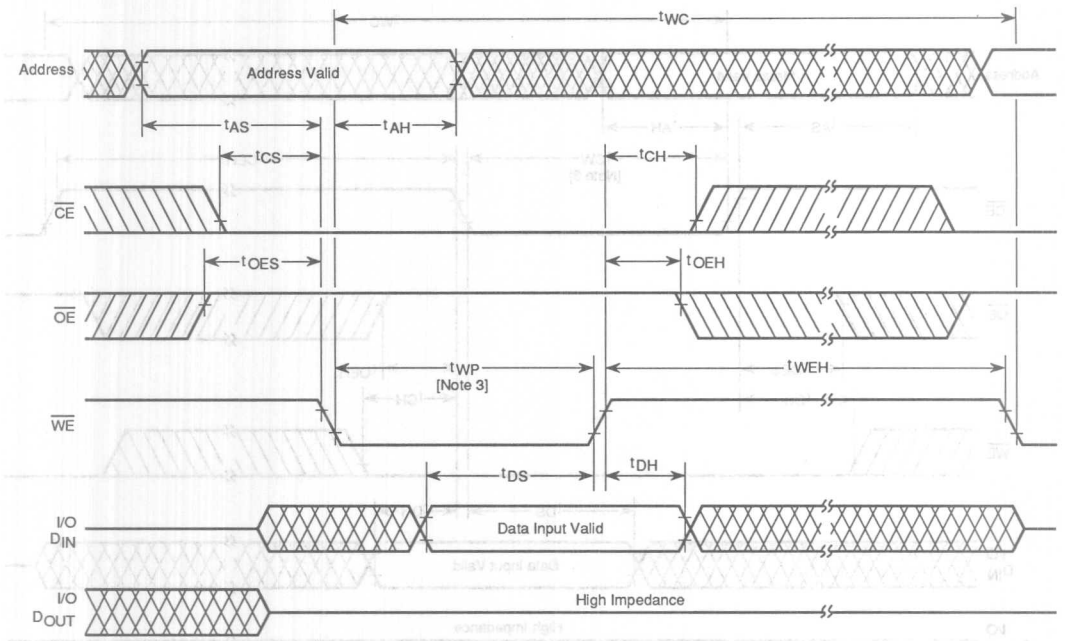
[2] t_{DF} is specified from $\overline{OE}$ or $\overline{CE}$, whichever occurs first.

[3] $\overline{WE} = V_{IH}$.

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Timing Waveforms (cont)

$\overline{WE}$-Controlled Write Cycle



Notes:

[1] The address inputs are latched at the falling edge of $\overline{CE}$ or $\overline{WE}$, whichever occurs later.

[2] The data inputs are latched at the rising edge of $\overline{CE}$ or $\overline{WE}$, whichever occurs earlier.

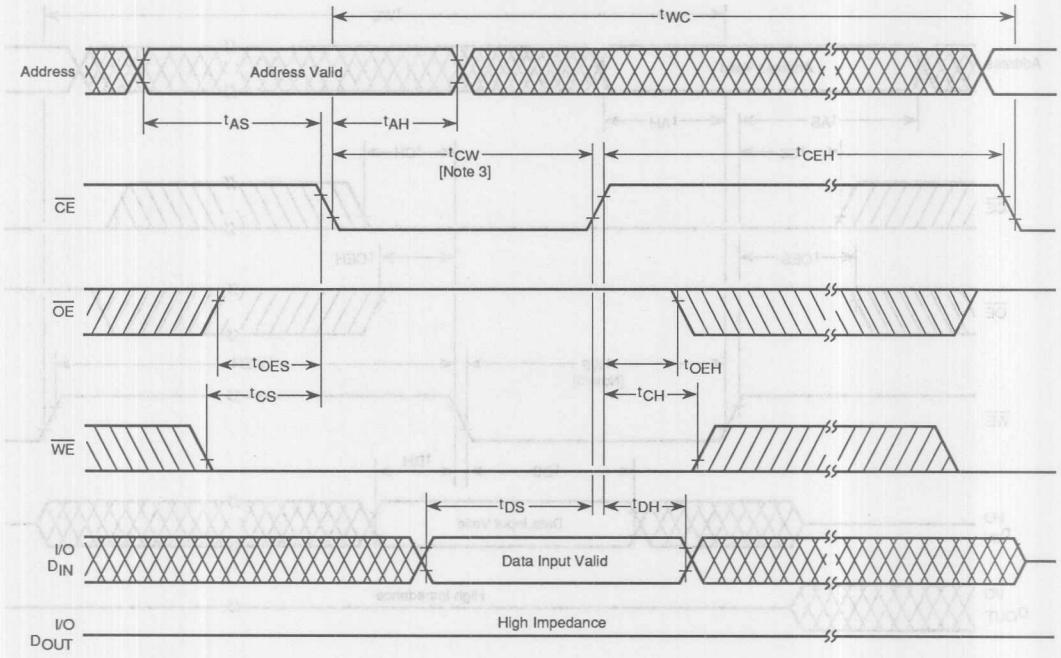
[3] Write operation requires both $\overline{CE}$ and $\overline{WE}$ to be at V_{IL}. Parameters t_{WP} and t_{CW} are defined only for the period when both $\overline{CE}$ and $\overline{WE}$ are at V_{IL}.

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Timing Waveforms (cont)

$\overline{CE}$-Controlled Write Cycle



Notes:

[1] The address inputs are latched at the falling edge of $\overline{CE}$ or $\overline{WE}$, whichever occurs later.

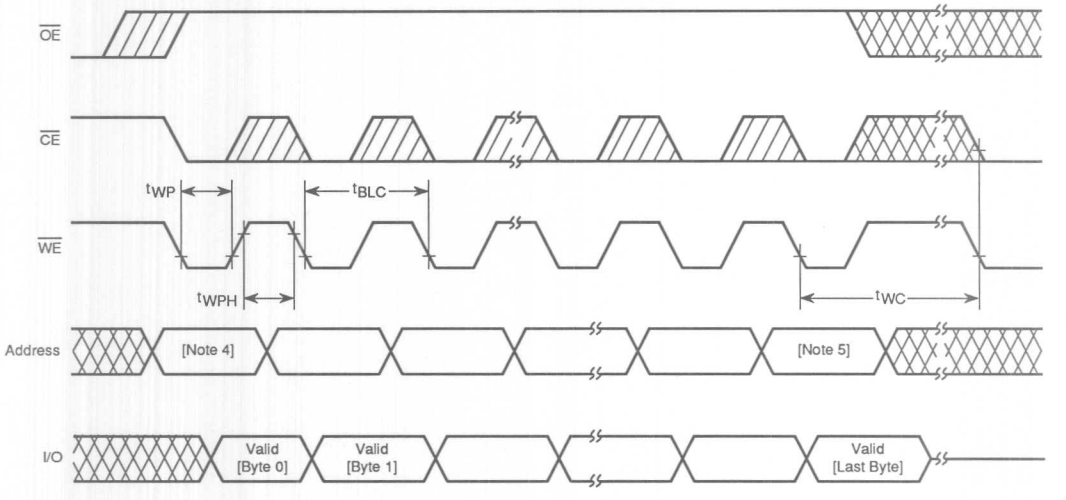
[2] The data inputs are latched at the rising edge of $\overline{CE}$ or $\overline{WE}$, whichever occurs earlier.

[3] Write operation requires both $\overline{CE}$ and $\overline{WE}$ to be at V_{IL}. Parameters t_{WP} and t_{CW} are defined only for the period when both $\overline{CE}$ and $\overline{WE}$ are at V_{IL}.

83IH-6894B

Timing Waveforms (cont)

Page Write Cycle



Notes:

[1] The address inputs are latched at the falling edge of $\overline{CE}$ or $\overline{WE}$, whichever occurs later.

[2] The data inputs are latched at the rising edge of $\overline{CE}$ or $\overline{WE}$, whichever occurs earlier.

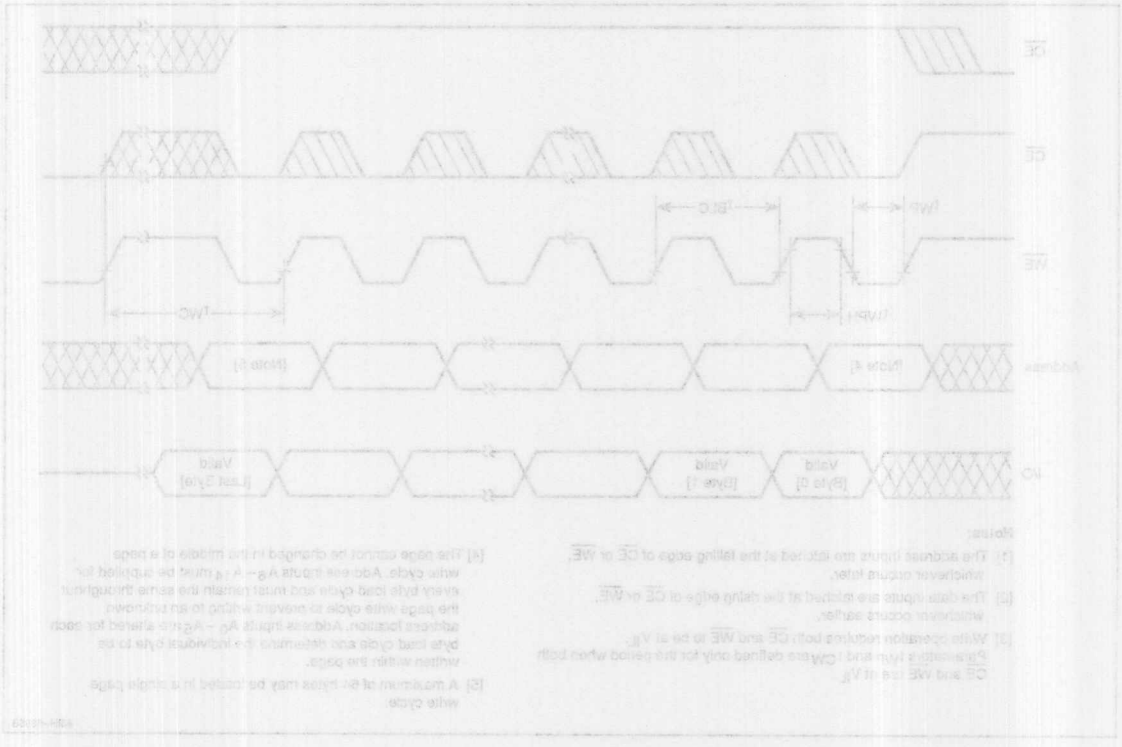
[3] Write operation requires both $\overline{CE}$ and $\overline{WE}$ to be at V_{IL}. Parameters t_{WP} and t_{CW} are defined only for the period when both $\overline{CE}$ and $\overline{WE}$ are at V_{IL}.

[4] The page cannot be changed in the middle of a page write cycle. Address inputs $A_6 - A_{14}$ must be supplied for every byte load cycle and must remain the same throughout the page write cycle to prevent writing to an unknown address location. Address inputs $A_0 - A_5$ are altered for each byte load cycle and determine the individual byte to be written within the page.

[5] A maximum of 64 bytes may be loaded in a single page write cycle.

83IH-6895B

10



Section 11
Mask-Programmable ROMs

μPD23C1000A 11-1
131,072 x 8-Bit
Mask-Programmable CMOS ROM

μPD23C1000EA 11-5
131,072 x 8-Bit
Mask-Programmable CMOS ROM

μPD23C1001E 11-9
131,072 x 8-Bit
Mask-Programmable CMOS ROM

μPD23C1010A 11-13
131,072 x 8-Bit
Mask-Programmable CMOS ROM

μPD23C1024E 11-17
65,536 x 16-Bit
Mask-Programmable CMOS ROM

μPD23C2000 11-21
2,097,152-Bit Mask-Programmable CMOS ROM

μPD23C2000A 11-25
2,097,152-Bit
Mask-Programmable CMOS ROM

μPD23C2001 11-29
262,144 x 8-Bit
Mask-Programmable CMOS ROM

μPD23C4000 11-33
4,194,304-Bit
Mask-Programmable CMOS ROM

μPD23C4000A 11-37
4,194,304-Bit
Mask-Programmable CMOS ROM

μPD23C4001E 11-41
524,288 x 8-Bit
Mask-Programmable CMOS ROM

μPD23C8000 11-45
8,388,608-Bit
Mask-Programmable CMOS ROM

μPD23C8001E 11-49
1,048,576 x 8-Bit
Mask-Programmable CMOS ROM

μPD23C16000 11-53
16,777,216-Bit
Mask-Programmable CMOS ROM

Application Note 90-05 11-57
ROM Code Submission Guide

Additional New Product Information

Device Number	Description	Comments
Mask-Programmable ROMs		
μPD23C2001E	256K x 8 bits	New device, with speed of 200 ns
μPD23C4001EA	512K x 8 bits	New speed of 200 ns
μPD23HC4001E	512K x 8 bits	New device, with speed of 100 ns

NEC Electronics Inc.

μPD23C1000A
131,072 x 8-Bit
Mask-Programmable CMOS ROM

Description

The μPD23C1000A is a 131,072-word by 8-bit static ROM fabricated with CMOS silicon-gate technology and designed to operate from a single +5-volt power supply. The device has three-state outputs and fully TTL-compatible inputs and outputs, and is available in 28-pin plastic DIP or miniflat packaging.

Features

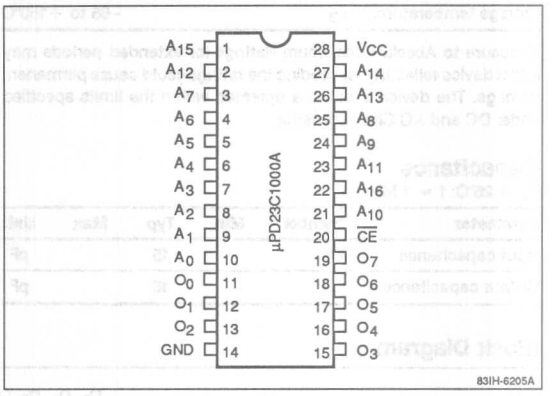
- 131,072-word by 8-bit organization
- TTL-compatible inputs and outputs
- Three-state outputs
- Single +5-volt power supply
- CMOS process technology
- Fully static operation
- Low power dissipation
  - 220 mW (active)
  - 550 μW (standby)

Ordering Information

Part Number	Access Time (max)	Package
μPD23C1000AC	200 ns	28-pin plastic DIP
μPD23C1000AG	200 ns	28-pin plastic miniflat

Pin Configuration

28-Pin Plastic DIP or Miniflat



Pin Identification

Symbol	Function
A_0 - A_{16}	Address inputs
O_0 - O_7	Data outputs
$\overline{CE}$	Chip enable
GND	Ground
V_{CC}	+5-volt power supply

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Absolute Maximum Ratings

Supply voltage, V_{CC}	−0.3 to +7.0 V
Input voltage, V_I	−0.3 V to V_{CC} + 0.3 V
Output voltage, V_O	−0.3 V to V_{CC} + 0.3 V
Operating temperature, T_{OPR}	−10 to +70°C
Storage temperature, T_{STG}	−65 to +150°C

Exposure to Absolute Maximum Ratings for extended periods may affect device reliability; exceeding the ratings could cause permanent damage. The device should be operated within the limits specified under DC and AC Characteristics.

Capacitance

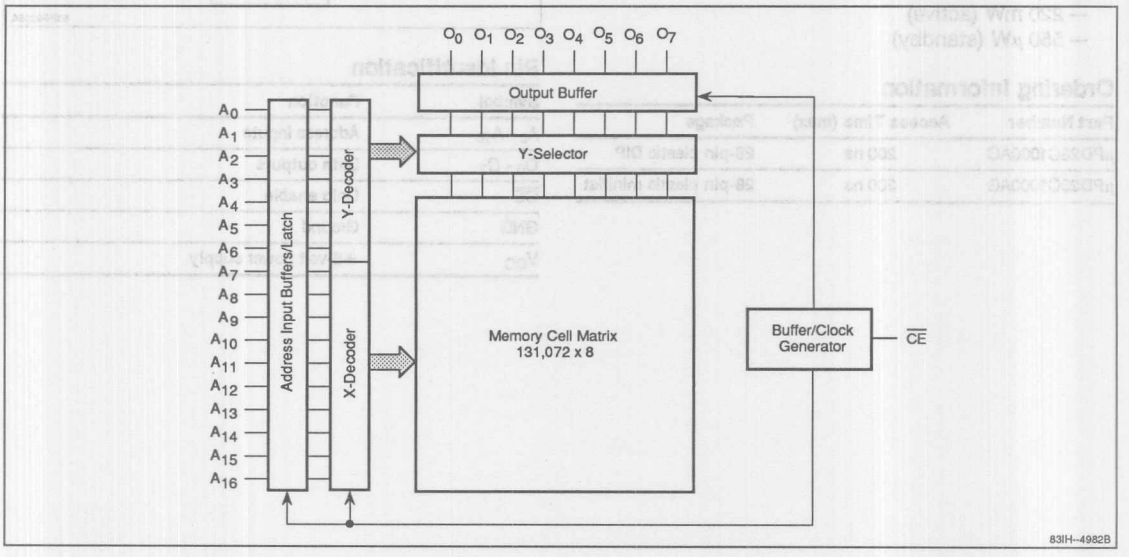
T_A = 25°C; f = 1 MHz

Parameter	Symbol	Min	Typ	Max	Unit
Input capacitance	C_I		15		pF
Output capacitance	C_O		15		pF

Recommended Operating Conditions

Parameter	Symbol	Min	Typ	Max	Unit
Input voltage, high	V_{IH}	2.2		V_{CC} + 0.3	V
Input voltage, low	V_{IL}	−0.3		0.8	V
Supply voltage	V_{CC}	4.5	5.0	5.5	V
Ambient temperature	T_A	−10		70	°C

Block Diagram



DC Characteristics

T_A = −10 to +70°C; V_{CC} = +5.0 V ±10%

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions
Output voltage, high	V_{OH}	2.4			V	I_{OH} = −400 μA
Output voltage, low	V_{OL}			0.4	V	I_{OL} = +2.5 mA
Input leakage current	I_{LI}	−10		10	μA	V_I = 0 V to V_{CC}
Output leakage current	I_{LO}	−10		10	μA	V_O = 0 V to V_{CC}; chip deselected
Power supply current	I_{CC1}			40	mA	$\overline{CE}$ = V_{IL}
	I_{CC2}			1.5	mA	$\overline{CE}$ = V_{IH} (standby)
	I_{CC3}			100	μA	$\overline{CE}$ ≥ V_{CC} − 0.2 (standby)

AC Characteristics

T_A = −10 to +70°C; V_{CC} = +5.0 V ±10% (Note 1)

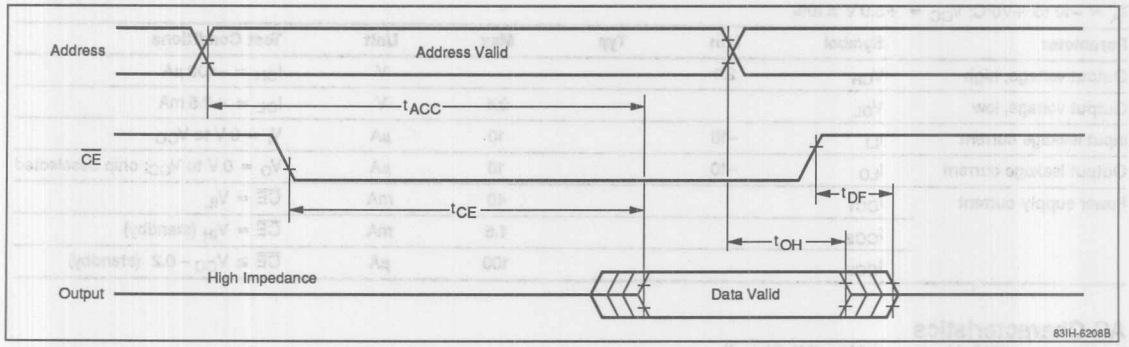
Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions
Address access time	t_{ACC}			200	ns	
Chip enable access time	t_{CE}			200	ns	
Output hold time	t_{OH}	0			ns	
Output disable time	t_{DF}	0		60	ns	

Notes:

(1) Input voltage rise and fall times = 20 ns; input and output timing reference levels = 0.8 and 2.0 V; output load = 1 TTL + 100 pF.

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Timing Waveform



μPD23C1000EA
131,072 x 8-Bit
Mask-Programmable CMOS ROM

Description

The μPD23C1000EA is a 131,072-word by 8-bit static ROM fabricated with CMOS silicon-gate technology. Designed to operate from a single +5-volt power supply, the device has three-state outputs and fully TTL-compatible inputs and outputs, and is packaged in a 600-mil, 32-pin plastic DIP.

Features

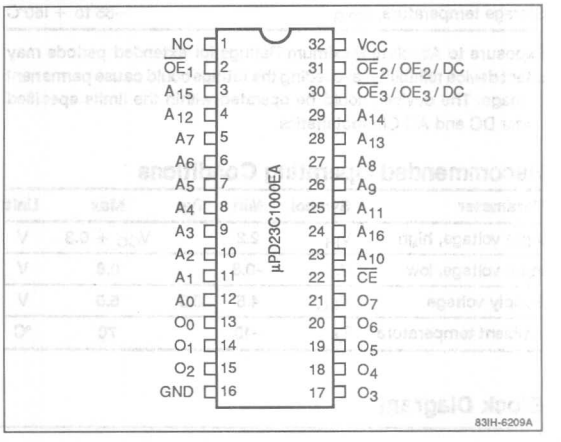
- 131,072-word by 8-bit organization
- Fast access time of 200 ns maximum
- TTL-compatible inputs and outputs
- Three-state outputs
- Single +5-volt power supply
- CMOS process technology
- Fully static operation
- Low power dissipation
  - 220 mW (active)
  - 550 μW (standby)

Ordering Information

Part Number	Access Time (max)	Package
μPD23C1000EAC	200 ns	32-pin plastic DIP

Pin Configuration

32-Pin Plastic DIP



Pin Identification

Symbol	Function
A_0 - A_{16}	Address inputs
O_0 - O_7	Data outputs
$\overline{CE}$	Chip enable
$\overline{OE}_1$	Output enable 1
$\overline{OE}_2$/OE_2/DC	Output enable 2 (Note 1)
$\overline{OE}_3$/OE_3/DC	Output enable 3 (Note 1)
GND	Ground
V_{CC}	+5-volt power supply
NC	No connection

Notes:

(1) This pin is user-definable as active low, active high, or "don't care" (in the cases of $\overline{OE}_2$/OE_2/DC and $\overline{OE}_3$/OE_3/DC).

11

Absolute Maximum Ratings

Supply voltage, V_{CC}	−0.3 to +7.0 V
Input voltage, V_I	−0.3 V to V_{CC} + 0.3 V
Output voltage, V_O	−0.3 V to V_{CC} + 0.3 V
Operating temperature, T_{OPR}	−10 to +70°C
Storage temperature, T_{STG}	−65 to +150°C

Exposure to Absolute Maximum Ratings for extended periods may affect device reliability; exceeding the ratings could cause permanent damage. The device should be operated within the limits specified under DC and AC Characteristics.

Recommended Operating Conditions

Parameter	Symbol	Min	Typ	Max	Unit
Input voltage, high	V_{IH}	2.2		V_{CC} + 0.3	V
Input voltage, low	V_{IL}	−0.3		0.8	V
Supply voltage	V_{CC}	4.5	5.0	5.5	V
Ambient temperature	T_A	−10		70	°C

Capacitance

T_A = 25°C; f = 1 MHz

Parameter	Symbol	Min	Typ	Max	Unit
Input capacitance	C_I		15		pF
Output capacitance	C_O		15		pF

Truth Table

$\overline{CE}$	$\overline{OE_1}$	$\overline{OE_2}$/OE_2/DC	$\overline{OE_3}$/OE_3/DC	Outputs	Function
V_{IH}	X	X	X	High-Z	Standby
V_{IL}	V_{IH}	X	X	High-Z	Active
V_{IL}	X	I	X	High-Z	Active
V_{IL}	X	X	I	High-Z	Active
V_{IL}	V_{IL}	A	A	D_{OUT}	Read

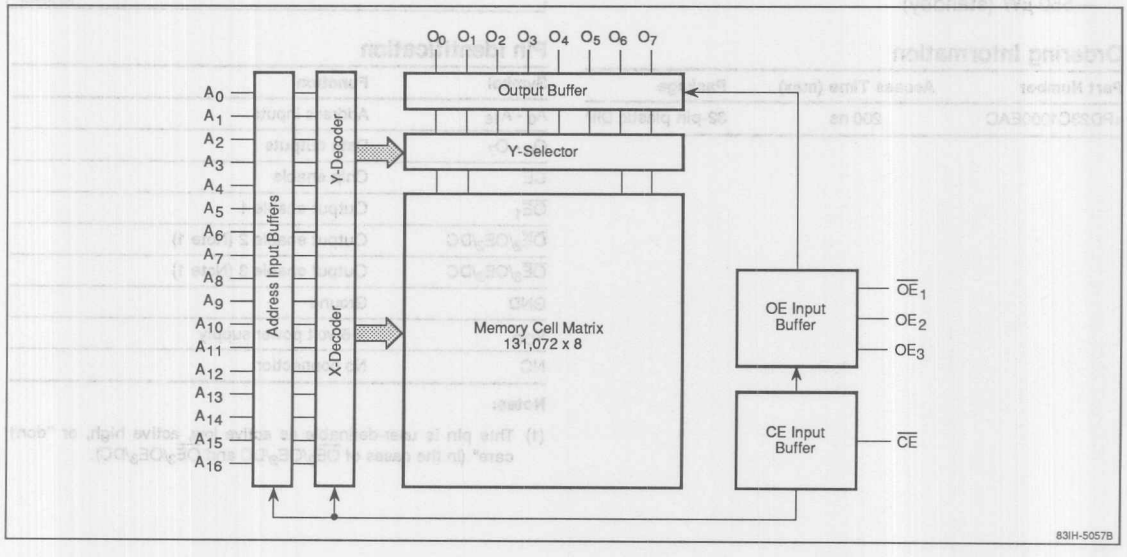
Notes:

(1) I = Inactive

(2) A = Active

(3) X = "don't care"

Block Diagram



DC Characteristics

T_A = −10 to +70°C; V_{CC} = +5.0 V ±10%

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions
Output voltage, high	V_{OH}	2.4			V	I_{OH} = −400 μA
Output voltage, low	V_{OL}			0.4	V	I_{OL} = +2.5 mA
Input leakage current	I_{LI}	−10		10	μA	V_I = 0 V to V_{CC}
Output leakage current	I_{LO}	−10		10	μA	V_O = 0 V to V_{CC}; outputs disabled
Power supply current	I_{CC1}			40	mA	$\overline{CE}$ = V_{IL} (active)
	I_{CC2}			1.5	mA	$\overline{CE}$ = V_{IH} (standby)
	I_{CC3}			100	μA	$\overline{CE}$ ≥ V_{CC} − 0.2 V (standby)

AC Characteristics

T_A = −10 to +70°C; V_{CC} = +5.0 V ±10% (Note 1)

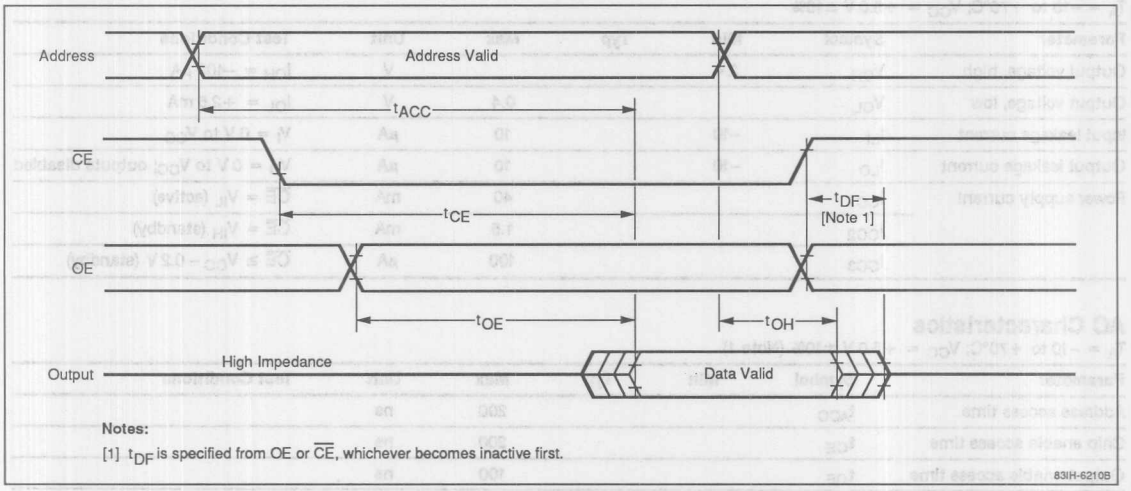
Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions
Address access time	t_{ACC}			200	ns	
Chip enable access time	t_{CE}			200	ns	
Output enable access time	t_{OE}			100	ns	
Output hold time	t_{OH}	0			ns	
Output disable time	t_{DF}	0		60	ns	

Notes:

(1) Input voltage rise and fall times = 20 ns; input and output timing reference levels = 0.8 and 2.0 V; output load = 1 TTL + 100 pF.

11

Timing Waveform



Notes:

[1] t_{DF} is specified from OE or $\overline{CE}$, whichever becomes inactive first.

NEC Electronics Inc.

μPD23C1001E
131,072 x 8-Bit
Mask-Programmable CMOS ROM

Description

The μPD23C1001E is a 131,072-word by 8-bit static ROM fabricated with CMOS silicon-gate technology and designed to operate from a single +5-volt power supply. The device has three-state outputs and fully TTL-compatible inputs and outputs, and is packaged in a 600-mil, 32-pin plastic DIP.

Features

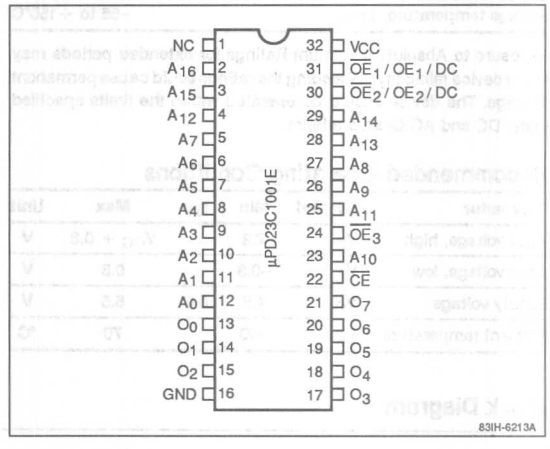
- 131,072-word by 8-bit organization
- Fast access time of 200 ns maximum
- TTL-compatible inputs and outputs
- Three-state outputs
- Single +5-volt power supply
- CMOS process technology
- Fully static operation
- Low power dissipation
  - 220 mW (active)
  - 550 μW (standby)

Ordering Information

Part Number	Access Time (max)	Package
μPD23C1001EC	200 ns	32-pin plastic DIP

Pin Configuration

32-Pin Plastic DIP



Pin Identification

Symbol	Function
A_0 - A_{16}	Address inputs
O_0 - O_7	Data outputs
$\overline{CE}$	Chip enable
$\overline{OE}_1/OE_1/DC$	Output enable 1 (Note 1)
$\overline{OE}_2/OE_2/DC$	Output enable 2 (Note 1)
$\overline{OE}_3$	Output enable 3
GND	Ground
V_{CC}	+5-volt power supply
NC	No connection

Notes:

(1) This pin is user-definable as active low, active high, or "don't care" (in the cases of $\overline{OE}_1/OE_1/DC$ and $\overline{OE}_2/OE_2/DC$).

11

Absolute Maximum Ratings

Supply voltage, V_{CC}	−0.3 to +7.0 V
Input voltage, V_I	−0.3 V to V_{CC} + 0.3 V
Output voltage, V_O	−0.3 V to V_{CC} + 0.3 V
Operating temperature, T_{OPR}	−10 to +70°C
Storage temperature, T_{STG}	−65 to +150°C

Exposure to Absolute Maximum Ratings for extended periods may affect device reliability; exceeding the ratings could cause permanent damage. The device should be operated within the limits specified under DC and AC Characteristics.

Recommended Operating Conditions

Parameter	Symbol	Min	Typ	Max	Unit
Input voltage, high	V_{IH}	2.2		V_{CC} + 0.3	V
Input voltage, low	V_{IL}	−0.3		0.8	V
Supply voltage	V_{CC}	4.5	5.0	5.5	V
Ambient temperature	T_A	−10		70	°C

Capacitance

T_A = 25°C; f = 1 MHz

Parameter	Symbol	Min	Typ	Max	Unit
Input capacitance	C_I		15		pF
Output capacitance	C_O		15		pF

Truth Table

$\overline{CE}$	$\overline{OE_1}/OE_1/DC$	$\overline{OE_2}/OE_2/DC$	$\overline{OE_3}$	Outputs	Function
V_{IH}	X	X	X	High-Z	Standby
V_{IL}	I	X	X	High-Z	Active
V_{IL}	X	I	X	High-Z	Active
V_{IL}	X	X	V_{IH}	High-Z	Active
V_{IL}	A	A	V_{IL}	D_{OUT}	Read

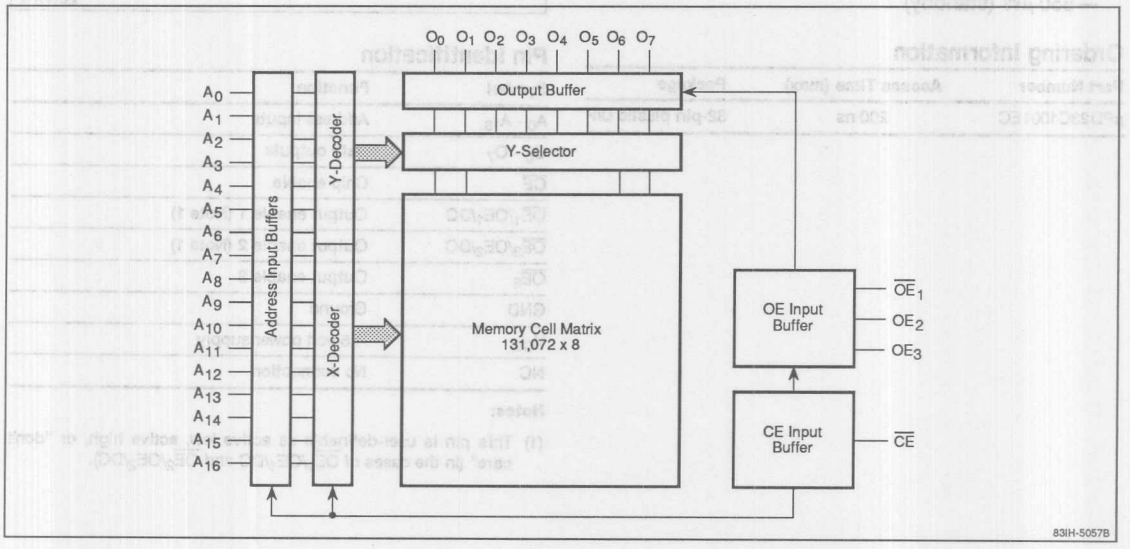
Notes:

(1) I = Inactive

(2) A = Active

(3) X = "don't care"

Block Diagram



DC Characteristics

T_A = −10 to +70°C; V_{CC} = +5.0 V ±10%

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions
Output voltage, high	V_{OH}	2.4			V	I_{OH} = −400 μA
Output voltage, low	V_{OL}			0.4	V	I_{OL} = +2.5 mA
Input leakage current	I_{LI}	−10		10	μA	V_I = 0 V to V_{CC}
Output leakage current	I_{LO}	−10		10	μA	V_O = 0 V to V_{CC}; outputs disabled
Power supply current	I_{CC1}			40	mA	$\overline{CE}$ = V_{IL} (active)
	I_{CC2}			1.5	mA	$\overline{CE}$ = V_{IH} (standby)
	I_{CC3}			100	μA	$\overline{CE}$ ≥ V_{CC} − 0.2 V (standby)

AC Characteristics

T_A = −10 to +70°C; V_{CC} = +5.0 V ±10% (Note 1)

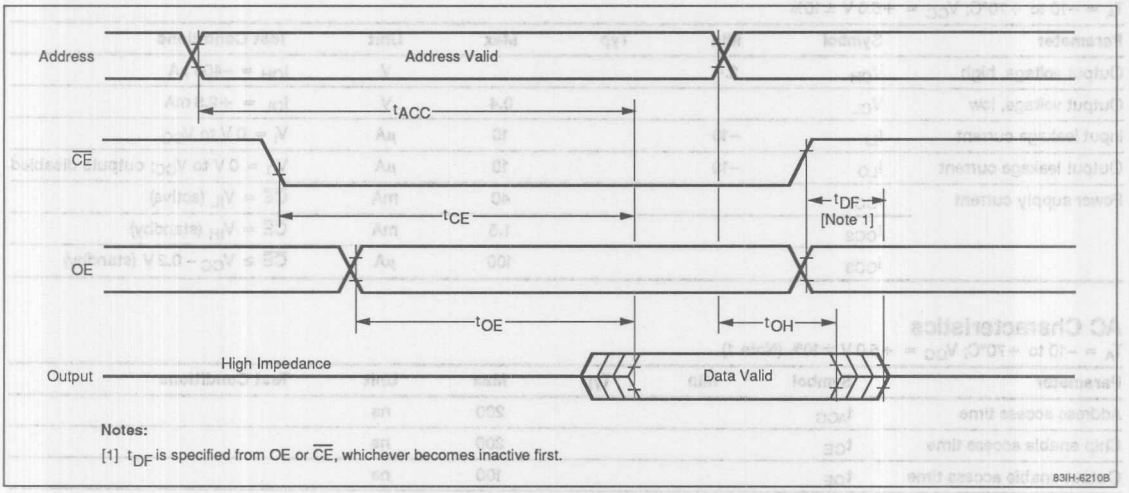
Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions
Address access time	t_{ACC}			200	ns	
Chip enable access time	t_{CE}			200	ns	
Output enable access time	t_{OE}			100	ns	
Output hold time	t_{OH}	0			ns	
Output disable time	t_{DF}	0		60	ns	

Notes:

(1) Input voltage rise and fall times = 20 ns; input and output timing reference levels = 0.8 and 2.0 V; output load = 1 TTL + 100 pF.

11

Timing Waveform



Notes:

[1] t_{DF} is specified from OE or $\overline{CE}$, whichever becomes inactive first.

μPD23C1010A
131,072 x 8-Bit
Mask-Programmable CMOS ROM

Description

The μPD23C1010A is a 1,048,576-bit ROM fabricated with CMOS silicon-gate technology. The device is static in operation and organized as 131,072 words by 8 bits. It has three-state outputs, fully TTL-compatible inputs and outputs, and is available in a 28-pin plastic DIP .

Features

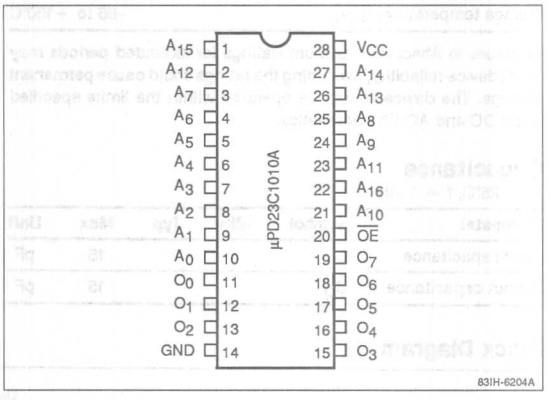
- 131,072 words by 8-bit organization
- Fast access time
- TTL-compatible inputs and outputs
- Three-state outputs
- Single +5-volt power supply
- CMOS technology
- Fully static operation
- Low power dissipation of 220 mW

Ordering Information

Part Number	Address Access Time (max)	Output Enable Access Time (max)	Package
μPD23C1010AC	200 ns	100 ns	28-pin plastic DIP

Pin Configuration

28-Pin Plastic DIP



Pin Identification

Symbol	Function
A_0 - A_{16}	Address inputs
O_0 - O_7	Data outputs
$\overline{OE}$	Output enable
GND	Ground
V_{CC}	+5-volt power supply

11

Absolute Maximum Ratings

Supply voltage, V_{CC}	−0.3 to +7.0 V
Input voltage, V_I	−0.3 V to V_{CC} + 0.3 V
Output voltage, V_O	−0.3 V to V_{CC} + 0.3 V
Operating temperature, T_{OPR}	−10 to +70°C
Storage temperature, T_{STG}	−65 to +150°C

Exposure to Absolute Maximum Ratings for extended periods may affect device reliability; exceeding the ratings could cause permanent damage. The device should be operated within the limits specified under DC and AC Characteristics.

Capacitance

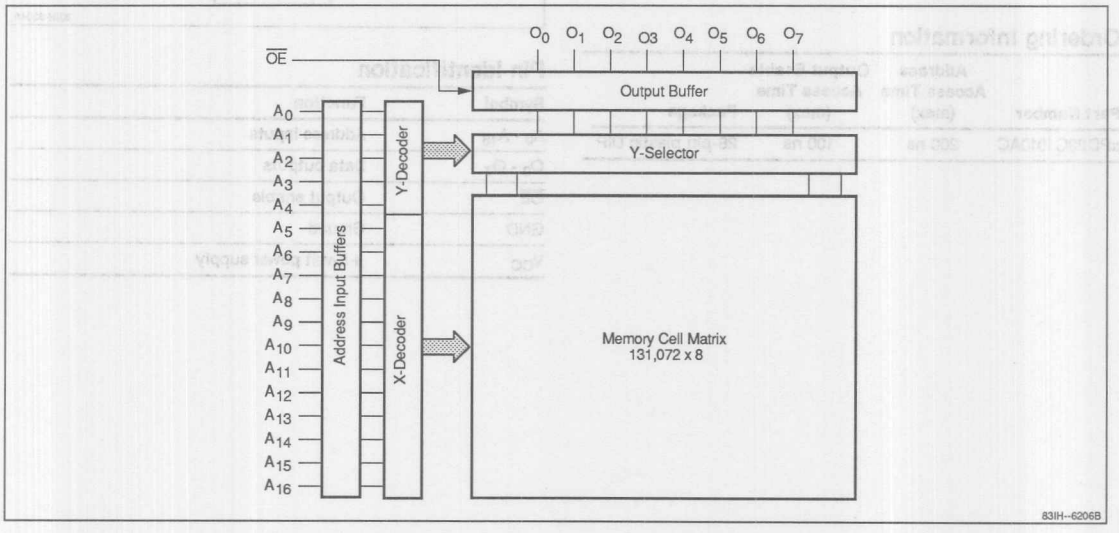
T_A = 25°C; f = 1 MHz

Parameter	Symbol	Min	Typ	Max	Unit
Input capacitance	C_I			15	pF
Output capacitance	C_O			15	pF

Recommended Operating Conditions

Parameter	Symbol	Min	Typ	Max	Unit
Input voltage, high	V_{IH}	2.2		V_{CC} + 0.3	V
Input voltage, low	V_{IL}	−0.3		0.8	V
Supply voltage	V_{CC}	4.5	5.0	5.5	V
Ambient temperature	T_A	−10		70	°C

Block Diagram



DC Characteristics

T_A = −10 to +70°C; V_{CC} = +5.0 V ±10%

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions
Output voltage, high	V_{OH}	2.4			V	I_{OH} = −400 μA
Output voltage, low	V_{OL}			0.4	V	I_{OL} = +2.5 mA
Input leakage current, high	I_{LIH}			10	μA	$V_I = V_{CC}$
Input leakage current, low	I_{LIL}			−10	μA	V_I = 0 V
Output leakage current, high	I_{LOH}			10	μA	$V_O = V_{CC}$; output disabled
Output leakage current, low	I_{LOL}			−10	μA	V_O = 0 V; output disabled
Power supply current	I_{CC1}			40	mA	

AC Characteristics

T_A = −10 to +70°C; V_{CC} = +5.0 V ±10%

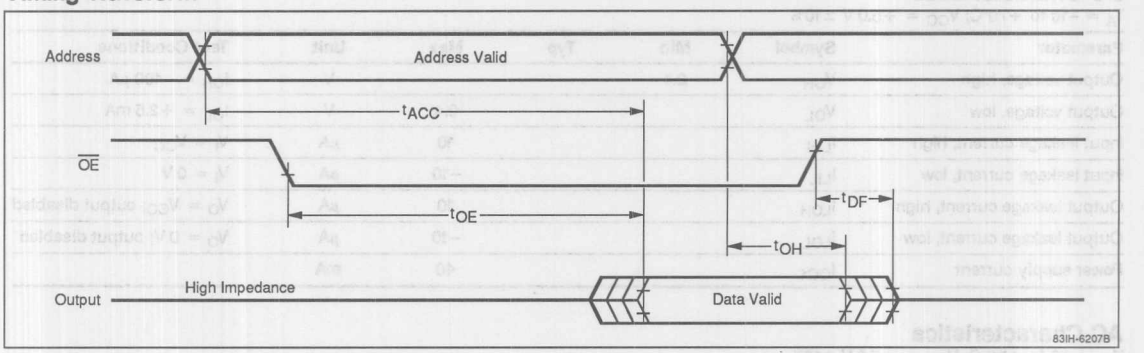
Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions
Address access time	t_{ACC}			200	ns	
Output enable access time	t_{OE}			100	ns	
Output hold time	t_{OH}	0			ns	
Output disable time	t_{DF}	0		60	ns	

Notes:

(1) Input voltage rise and fall times = 20 ns; input and output timing reference levels = 0.8 and 2.0 V; output load = 1 TTL + 100 pF.

11

Timing Waveform



μPD23C1024E
65,536 x 16-Bit
Mask-Programmable CMOS ROM

Description

The μPD23C1024E is a 65,536-word by 16-bit mask-programmable ROM fabricated with CMOS silicon-gate technology and designed to operate from a single +5-volt power supply. The device has three-state outputs and fully TTL-compatible inputs and outputs, and is packaged in a 600-mil, 40-pin plastic DIP.

Features

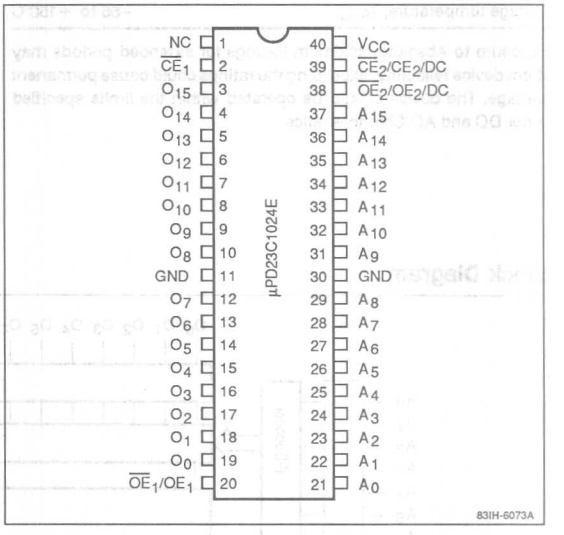
- 65,536-word by 16-bit organization
- Fast access time: 200 ns maximum
- TTL-compatible inputs and outputs
- Three-state outputs
- Single +5-volt power supply
- CMOS process technology
- Fully static operation
- Low power dissipation

Ordering Information

Part Number	Access Time (max)	Package
μPD23C1024EC	200 ns	40-pin plastic DIP

Pin Configuration

40-Pin Plastic DIP



Pin Identification

Symbol	Function
A_0 - A_{15}	Address inputs
O_0 - O_{15}	Data outputs
$\overline{CE}_1$	Chip enable 1
$\overline{CE}_2/CE_2/DC$	Chip enable 2 (Note 1)
$\overline{OE}_1/OE_1$	Output enable 1
$\overline{OE}_2/OE_2/DC$	Output enable 2 (Note 1)
GND	Ground
V_{CC}	+5-volt power supply
NC	No connection

Notes:

(1) This pin is user-definable as active low, active high, or "don't care."

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Absolute Maximum Ratings

Supply voltage, V_{CC}	−0.3 to +7.0 V
Input voltage, V_I	−0.3 V to V_{CC} +0.3 V
Output voltage, V_O	−0.3 V to V_{CC} +0.3 V
Operating temperature, T_{OPR}	−10 to +70°C
Storage temperature, T_{STG}	−65 to +150°C

Exposure to Absolute Maximum Ratings for extended periods may affect device reliability; exceeding the ratings could cause permanent damage. The device should be operated within the limits specified under DC and AC Characteristics.

Capacitance

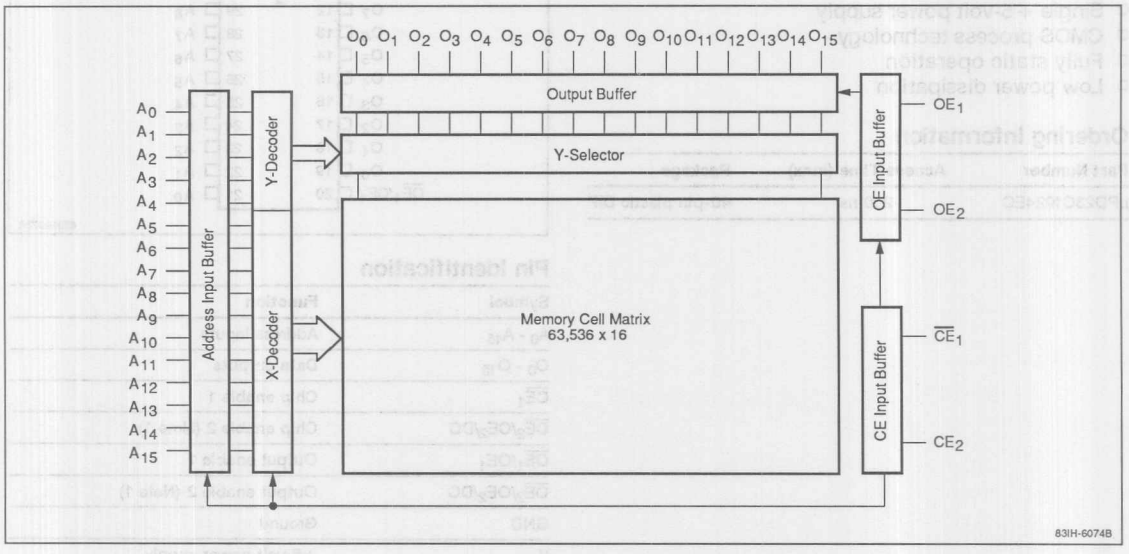
T_A = 25°C; f = 1 MHz

Parameter	Symbol	Min	Typ	Max	Unit
Input capacitance	C_I			15	pF
Output capacitance	C_O			15	pF

Recommended Operating Conditions

Parameter	Symbol	Min	Typ	Max	Unit
Input voltage, high	V_{IH}	2.2		V_{CC} + 0.3	V
Input voltage, low	V_{IL}	−0.3		0.8	V
Supply voltage	V_{CC}	4.5	5.0	5.5	V
Ambient temperature	T_A	−10		70	°C

Block Diagram



Truth Table

$\overline{CE}_1$	CE_2	OE_1	OE_2	Function	Outputs	I_{CC}
V_{IH}	X	X	X	Not Selected	High-Z	Standby
X	Inactive	X	X	Not Selected	High-Z	Standby
V_{IL}	Active	Inactive	X	Selected	High-Z	Active
V_{IL}	Active	X	Inactive	Selected	High-Z	Active
V_{IL}	Active	Active	Active	Read	Data Output	Active

Notes:

(1) X = don't care.

DC Characteristics

$T_A = -10$ to $+70°C$; $V_{CC} = +5.0\ V \pm 10\%$

Parameter	Symbol	Min	Max	Unit	Test Conditions
Output voltage, high	V_{OH}	2.4		V	$I_{OH} = -400\ \mu A$
Output voltage, low	V_{OL}		0.4	V	$I_{OL} = +2.5\ mA$
Input leakage current	I_{LI}	−10	10	μA	$V_I = 0\ V$ to V_{CC}
Output leakage current	I_{LO}	−10	10	μA	$V_O = 0\ V$ to V_{CC} (chip deselected)
Power supply current	I_{CC1}		40	mA	$\overline{CE}_1 = V_{IL}$; CE_2 = active (chip selected)
	I_{CC2}		1.5	mA	$\overline{CE}_1 = V_{IH}$ or CE_2 = inactive (chip deselected)
	I_{CC3}		100	μA	$\overline{CE}_1 \geq V_{CC} - 0.2\ V$; $CE_2 \leq 0.2\ V$ (if CE_2 is programmed active high) or $CE_2 \geq V_{CC} - 0.2\ V$ (if CE_2 is programmed active low)

AC Characteristics

$T_A = -10$ to $+70°C$; $V_{CC} = +5.0\ V \pm 10\%$

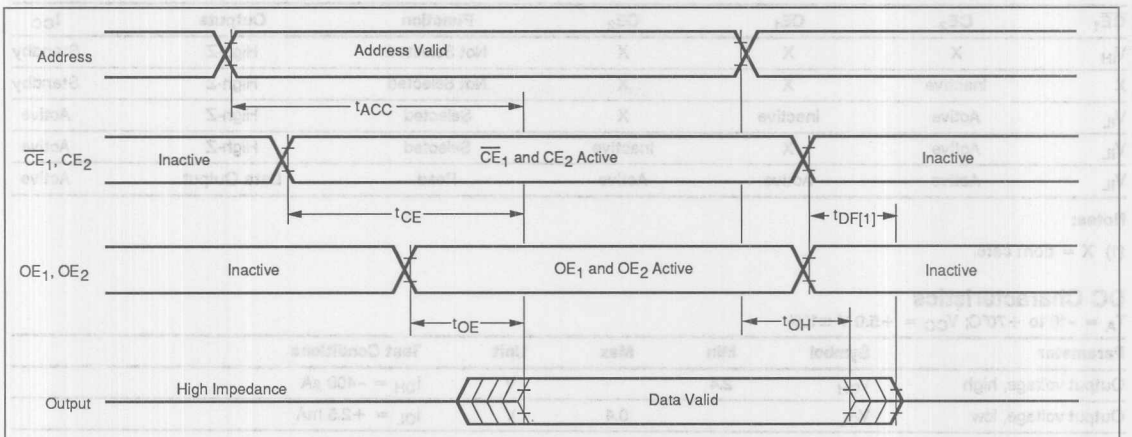
Parameter	Symbol	Min	Max	Unit	Test Conditions
Address access time	t_{ACC}		200	ns	
Chip enable access time	t_{CE}		200	ns	
Output enable access time	t_{OE}		100	ns	
Output hold time	t_{OH}	0		ns	
Output disable time	t_{DF}	0	70	ns	

Notes:

(1) Input voltage rise and fall times = 20 ns; input and output timing reference levels = 0.8 V and 2.0 V; output load = 1 TTL + 100 pF.

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Timing Waveform



Notes:

[1] t_{DF} is specified from $\overline{CE}_1$, CE_2, OE_1, OE_2, whichever goes inactive first.

[2] t_{CE} is specified from $\overline{CE}_1$ or CE_2, whichever goes active last.

[3] t_{OE} is specified from OE_1 or OE_2, whichever goes active last.

83IH-6075B

μPD23C2000
2,097,152-Bit
Mask-Programmable CMOS ROM

Description

The μPD23C2000 is a 2,097,152-bit ROM fabricated with CMOS silicon-gate technology. The device is static in operation and can be organized as 131,072 words by 16 bits (word configuration) or as 262,144 words by 8 bits (byte configuration). In word configuration, pins $O_0 - O_{15}$ are active. In byte configuration, pin O_{15}/A_{-1} becomes the additional bit required to address 256K bytes.

The μPD23C2000 has three-state outputs, fully TTL-compatible inputs and outputs, and an output enable pin which is mask-programmable and can be specified as active low, active high, or don't care. The choice between word or byte configuration must also be specified for mask programming.

The μPD23C2000 is available in 40-pin plastic DIP or 52-pin plastic quad flatpack packaging.

Features

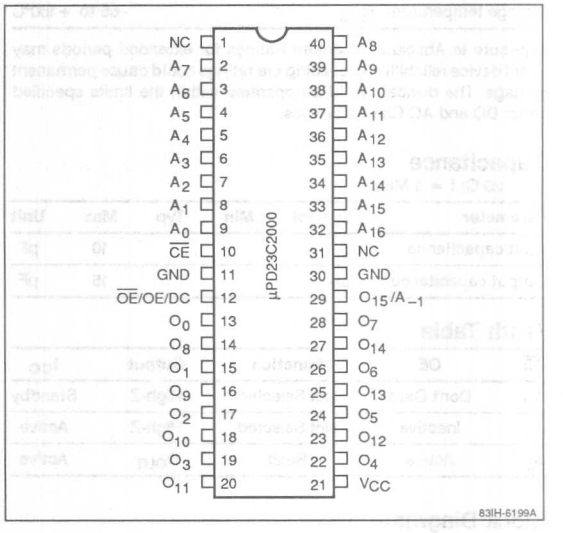
- Programmable organization
  - 131,072 words by 16 bits (word)
  - 262,144 words by 8 bits (byte)
- Fast access time of 250 ns maximum
- TTL-compatible inputs and outputs
- Three-state outputs
- Single +5-volt power supply
- CMOS technology
- Fully static operation
- Low power dissipation
  - 220 mW (active)
  - 550 μW (standby)
- 40-pin plastic DIP or 52-pin plastic QFP packaging

Ordering Information

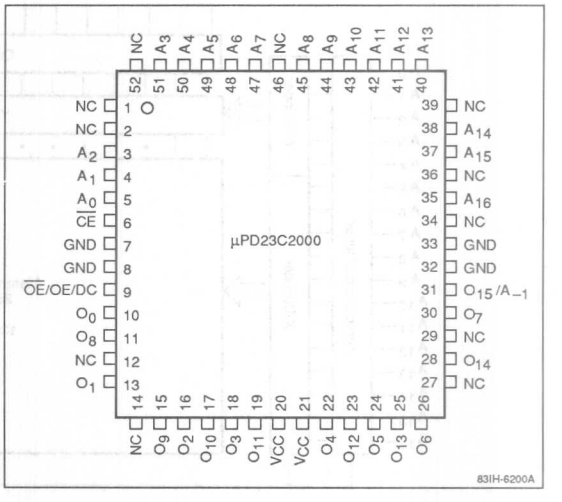
Part Number	Access Time (max)	Power Consumption (max) Active	Standby	Package
μPD23C2000C	250 ns	40 mA	100 μA	40-pin plastic DIP
μPD23C2000GC	250 ns	40 mA	100 μA	52-pin plastic QFP

Pin Configurations

40-Pin Plastic DIP



52-Pin Plastic Quad Flatpack



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Absolute Maximum Ratings

Supply voltage, V_{CC}	−0.3 to +7.0 V
Input voltage, V_I	−0.3 V to V_{CC} + 0.3 V
Output voltage, V_O	−0.3 V to V_{CC} + 0.3 V
Operating temperature, T_{OPR}	−10 to +70°C
Storage temperature, T_{STG}	−65 to +150°C

Exposure to Absolute Maximum Ratings for extended periods may affect device reliability; exceeding the ratings could cause permanent damage. The device should be operated within the limits specified under DC and AC Characteristics.

Capacitance

T_A = 25°C; f = 1 MHz

Parameter	Symbol	Min	Typ	Max	Unit
Input capacitance	C_I			10	pF
Output capacitance	C_O			15	pF

Truth Table

$\overline{CE}$	OE	Function	Output	I_{CC}
V_{IH}	Don't Care	Not Selected	High-Z	Standby
V_{IL}	Inactive	Not Selected	High-Z	Active
V_{IL}	Active	Read	D_{OUT}	Active

Pin Identification

Symbol	Function
A_0 - A_{16}	Address inputs
O_0 - O_{14}	Data outputs
O_{15}/A_{-1}	Output 15 (word)/LSB address (byte)
$\overline{CE}$	Chip enable
$\overline{OE}$/OE/DC	Output enable (Note 1)
GND	Ground
V_{CC}	+5-volt power supply
NC	No connection

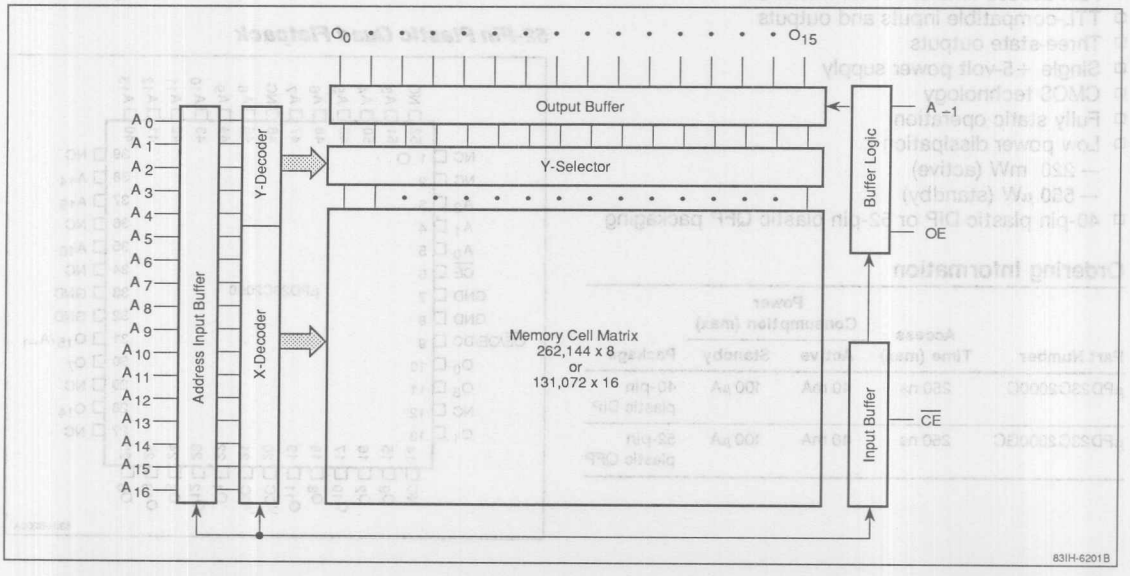
Notes:

(1) This pin is user-definable as active low, active high, or don't care.

Recommended Operating Conditions

Parameter	Symbol	Min	Typ	Max	Unit
Input voltage, high	V_{IH}	2.2		V_{CC} + 0.3	V
Input voltage, low	V_{IL}	−0.3		0.8	V
Supply voltage	V_{CC}	4.5	5.0	5.5	V
Ambient temperature	T_A	−10		70	°C

Block Diagram



DC Characteristics

T_A = −10 to +70°C; V_{CC} = +5.0 V ±10%

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions
Output voltage, high	V_{OH}	2.4			V	I_{OH} = −400 μA
Output voltage, low	V_{OL}			0.4	V	I_{OL} = 2.5 mA
Input leakage current	I_{LI}	−10		10	μA	V_I = 0 V to V_{CC}
Output leakage current	I_{LO}	−10		10	μA	V_O = 0 V to V_{CC}; chip deselected
Power supply current	I_{CC1}			40	mA	$\overline{CE}$ = V_{IL}
	I_{CC2}			1.5	mA	$\overline{CE}$ = V_{IH} (standby)
	I_{CC3}			100	μA	$\overline{CE}$ ≥ V_{CC} − 0.2 V (standby)

AC Characteristics

T_A = −10 to +70°C; V_{CC} = +5.0 V ±10%

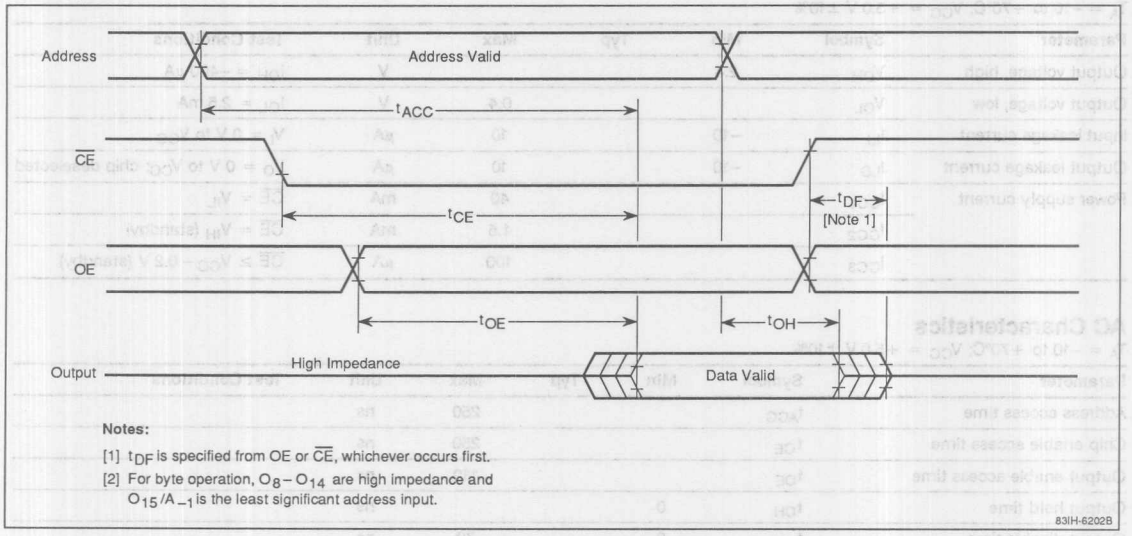
Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions
Address access time	t_{ACC}			250	ns	
Chip enable access time	t_{CE}			250	ns	
Output enable access time	t_{OE}			110	ns	
Output hold time	t_{OH}	0			ns	
Output disable time	t_{DF}	0		70	ns	

Notes:

(1) Input voltage rise and fall times = 20 ns; input and output timing reference levels = 0.8 and 2.0 V; output load = 1 TTL +100 pF.

11

Timing Waveform



Notes:

[1] t_{DF} is specified from OE or $\overline{CE}$, whichever occurs first.

[2] For byte operation, $O_8 - O_{14}$ are high impedance and O_{15}/A_{-1} is the least significant address input.

NEC Electronics Inc.

μPD23C2000A
2,097,152-Bit
Mask-Programmable CMOS ROM

Description

The μPD23C2000A is a 2,097,152-bit ROM fabricated with CMOS silicon-gate technology. This device is static in operation and can be organized as 131,072 words by 16 bits (word configuration) or as 262,144 words by 8 bits (byte configuration). In word configuration, pins O_0 - O_{15} are active. In byte configuration, pin O_{15}/A_{-1} becomes the additional bit required to address 256K bytes.

The μPD23C2000A has three-state outputs, fully TTL-compatible inputs and outputs, and an output enable pin which is mask-programmable and can be specified as active high, active low, or don't care. The choice between word or byte configuration must also be specified for mask programming.

The μPD23C2000A is available in a 40-pin plastic DIP.

Features

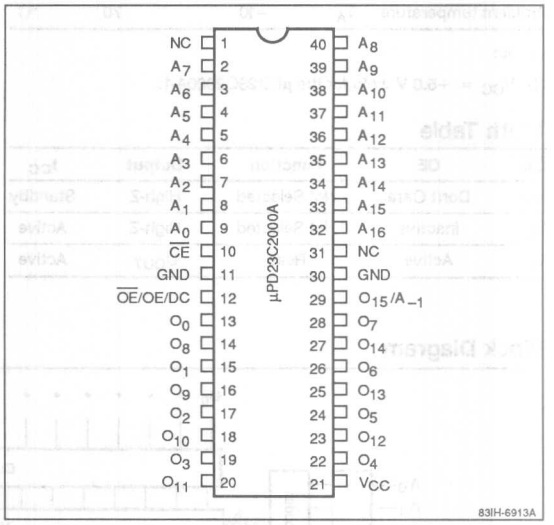
- Programmable organization
  - 131,072 words by 16 bits (word)
  - 262,144 words by 8 bits (byte)
- Fast access time of 175 ns maximum
- TTL-compatible inputs and outputs
- Three-state outputs
- Single +5-volt power supply
- CMOS technology
- Fully static operation
- Low power dissipation
  - 357.5 mW (active)
  - 550 μW (standby)

Ordering Information

Part Number	Access Time (max)	Power Consumption (max) Active	Standby	Package
μPD23C2000AC-1	175 ns	65 mA	100 μA	40-pin plastic DIP
μPD23C2000AC	200 ns			

Pin Configuration

40-Pin Plastic DIP



Pin Identification

Symbol	Function
A_0 - A_{16}	Address inputs
O_0 - O_{14}	Data outputs
O_{15}/A_{-1}	Output 15 (word)/LSB address (byte)
$\overline{CE}$	Chip enable
$\overline{OE}$/OE/DC	Output enable/don't care
GND	Ground
V_{CC}	+5-volt power supply
NC	No connection

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Recommended Operating Conditions

Parameter	Symbol	Min	Typ	Max	Unit
Input voltage, high	V_{IH}	2.2		V_{CC} + 0.3	V
Input voltage, low	V_{IL}	−0.3		0.8	V
Supply voltage	V_{CC}	4.5	5.0	5.5	V
Ambient temperature	T_A	−10		70	°C

Notes:

(1) V_{CC} = +5.0 V ±5% for the μPD23C2000A-1.

Truth Table

$\overline{CE}$	OE	Function	Output	I_{CC}
V_{IH}	Don't Care	Not Selected	High-Z	Standby
V_{IL}	Inactive	Not Selected	High-Z	Active
V_{IL}	Active	Read	D_{OUT}	Active

Absolute Maximum Ratings

Supply voltage, V_{CC}	−0.3 to +7.0 V
Input voltage, V_I	−0.3 V to V_{CC} + 0.3 V
Output voltage, V_O	−0.3 V to V_{CC} + 0.3 V
Operating temperature, T_{OPR}	−10 to +70°C
Storage temperature, T_{STG}	−65 to +150°C

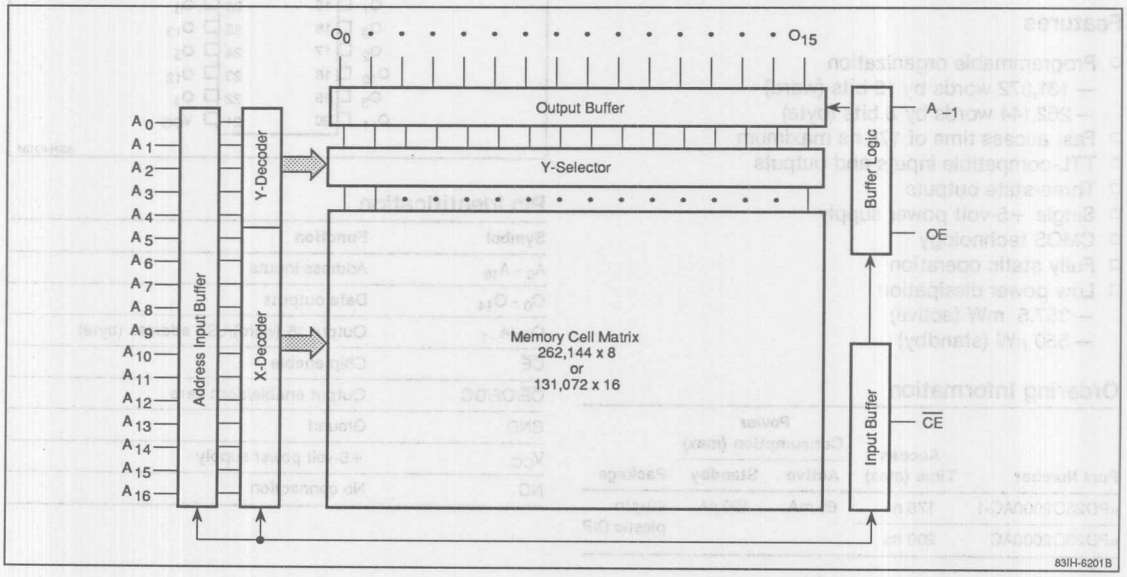
Exposure to Absolute Maximum Ratings for extended periods may affect device reliability; exceeding the ratings could cause permanent damage. The device should be operated within the limits specified under DC and AC Characteristics.

Capacitance

T_A = 25°C; f = 1 MHz

Parameter	Symbol	Min	Typ	Max	Unit
Input capacitance	C_I			15	pF
Output capacitance	C_O			15	pF

Block Diagram



DC Characteristics

T_A = −10 to +70°C; V_{CC} = +5.0 V ±5% for μPD23C2000A-1 and +5.0 V ±10% for μPD23C2000A

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions
Output voltage, high	V_{OH}	2.4			V	I_{OH} = −400 μA
Output voltage, low	V_{OL}			0.4	V	I_{OL} = 2.5 mA
Input leakage current	I_{LI}	−10		10	μA	V_I = 0 V to V_{CC}
Output leakage current	I_{LO}	−10		10	μA	V_O = 0 V to V_{CC}; chip deselected
Power supply current	I_{CC1}			65	mA	$\overline{CE}$ = V_{IL}
	I_{CC2}			1.5	mA	$\overline{CE}$ = V_{IH} (standby)
	I_{CC3}			100	μA	$\overline{CE}$ ≥ V_{CC} − 0.2 V (standby)

AC Characteristics

T_A = −10 to +70°C; V_{CC} = +5.0 V ±5% for μPD23C2000A-1 and +5.0 V ±10% for μPD23C2000A

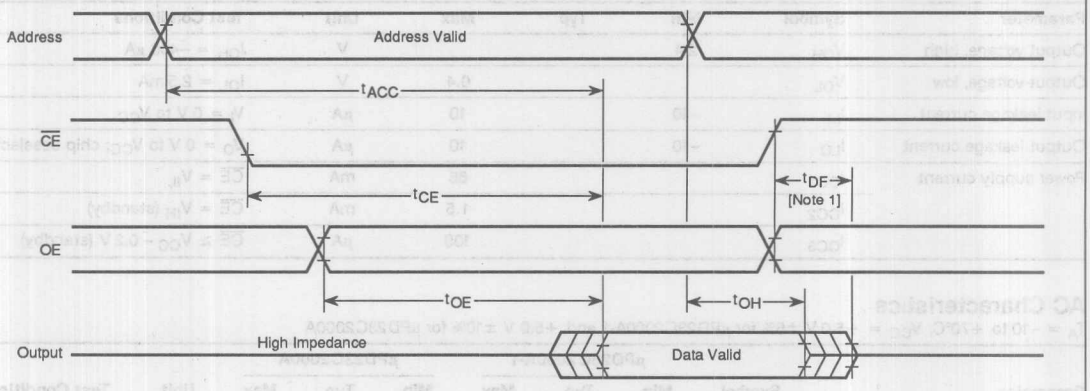
		μPD23C2000A-1			μPD23C2000A				
Parameter	Symbol	Min	Typ	Max	Min	Typ	Max	Unit	Test Conditions
Address access time	t_{ACC}			175			200	ns	
Chip enable access time	t_{CE}			175			200	ns	
Output enable access time	t_{OE}			100			100	ns	
Output hold time	t_{OH}	0			0			ns	
Output disable time	t_{DF}	0		60	0		60	ns	

Notes:

(1) Input voltage rise and fall times = 20 ns; input and output timing reference levels = 0.8 and 2.0 V; output load = 1 TTL +100 pF.

11

Timing Waveform



Notes:

[1] t_{DF} is specified from OE or $\overline{CE}$, whichever occurs first.

[2] For byte operation, $O_8 - O_{14}$ are high impedance and O_{15}/A_{-1} is the least significant address input.

NEC Electronics Inc.

μPD23C2001
262,144 x 8-Bit
Mask-Programmable CMOS ROM

Description

The μPD23C2001 is a 262,144-word by 8-bit static ROM fabricated with CMOS silicon-gate technology and designed to operate from a single +5-volt power supply. The device has three-state outputs and fully TTL-compatible inputs and outputs and is packaged in a 32-pin plastic DIP.

Features

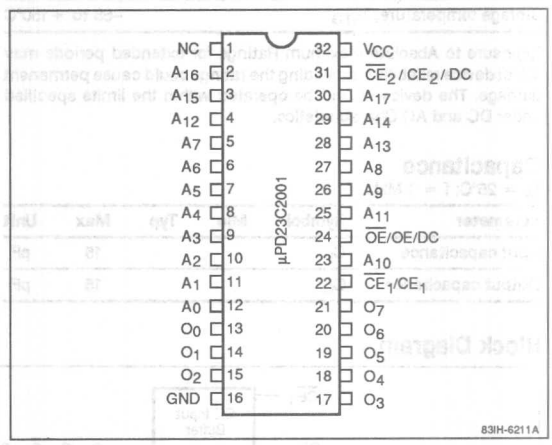
- 262,144-word by 8 bit organization
- Fast access time of 250 ns maximum
- TTL-compatible inputs and outputs
- Three-state outputs
- Single +5-volt power supply
- CMOS technology
- Fully static operation
- Low power dissipation
  - 220 mW (active)
  - 550 μW (standby)

Ordering Information

Part Number	Access Time (max)	Package
μPD23C2001C	250 ns	32-pin plastic DIP

Pin Configuration

32-Pin Plastic DIP



Pin Identification

Symbol	Function
A_0 - A_{17}	Address inputs
O_0 - O_7	Data outputs
$\overline{CE_1}/CE_1$	Chip enable 1 (Note 1)
$\overline{CE_2}/CE_2/DC$	Chip enable 2 (Note 1)
$\overline{OE}/OE/DC$	Output enable (Note 1)
GND	Ground
V_{CC}	+5-volt power supply
NC	No connection

Notes:

(1) This pin is user-definable as active low, active high, or "don't care" (in the cases of $\overline{CE_2}/CE_2/DC$ and $\overline{OE}/OE/DC$).

11

Absolute Maximum Ratings

Supply voltage, V_{CC}	−0.3 to +7.0 V
Input voltage, V_I	−0.3 V to V_{CC} + 0.3 V
Output voltage, V_O	−0.3 V to V_{CC} + 0.3 V
Operating temperature, T_{OPR}	−10 to +70°C
Storage temperature, T_{STG}	−65 to +150°C

Exposure to Absolute Maximum Ratings for extended periods may affect device reliability; exceeding the ratings could cause permanent damage. The device should be operated within the limits specified under DC and AC Characteristics.

Recommended Operating Conditions

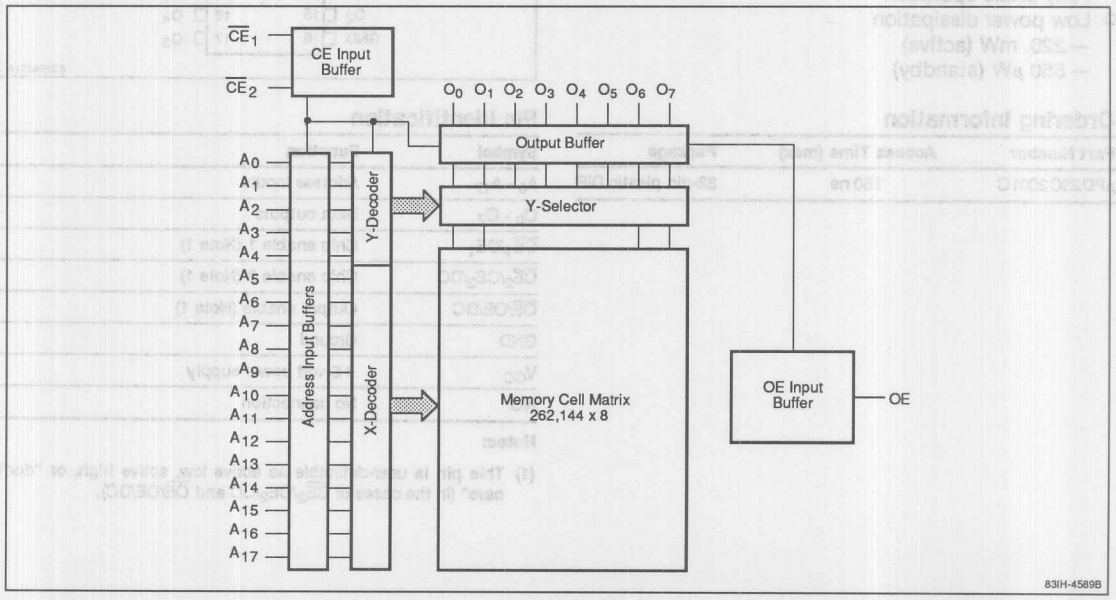
Parameter	Symbol	Min	Typ	Max	Unit
Input voltage, high	V_{IH}	2.2		V_{CC} + 0.3	V
Input voltage, low	V_{IL}	−0.3		0.8	V
Supply voltage	V_{CC}	4.5	5.0	5.5	V
Ambient temperature	T_A	−10		70	°C

Capacitance

T_A = 25°C; f = 1 MHz

Parameter	Symbol	Min	Typ	Max	Unit
Input capacitance	C_I			15	pF
Output capacitance	C_O			15	pF

Block Diagram



DC Characteristics

T_A = −10 to +70°C; V_{CC} = +5.0 V ±10%

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions
Output voltage, high	V_{OH}	2.4			V	I_{OH} = −400 μA
Output voltage, low	V_{OL}			0.4	V	I_{OL} = +2.1 mA
Input leakage current, high	I_{LIH}			10	μA	$V_I = V_{CC}$
Input leakage current, low	I_{LIL}			−10	μA	V_I = 0 V
Output leakage current, high	I_{LOH}			10	μA	$V_O = V_{CC}$ (outputs disabled)
Output leakage current, low	I_{LOL}			−10	μA	V_O = 0 V (outputs disabled)
Power supply current	I_{CC1}			40	mA	Both $\overline{CE}_1$ and $\overline{CE}_2$ inactive
	I_{CC2}			1.5	mA	Either $\overline{CE}_1$ or $\overline{CE}_2$ inactive (V_{IL}, V_{IH})
	I_{CC3}			100	μA	Either $\overline{CE}_1$ or $\overline{CE}_2$ inactive (both ≤ 0.2 V or ≥ V_{CC} − 0.2 V)

AC Characteristics

T_A = −10 to +70°C; V_{CC} = +5.0 V ±10% (Note 1)

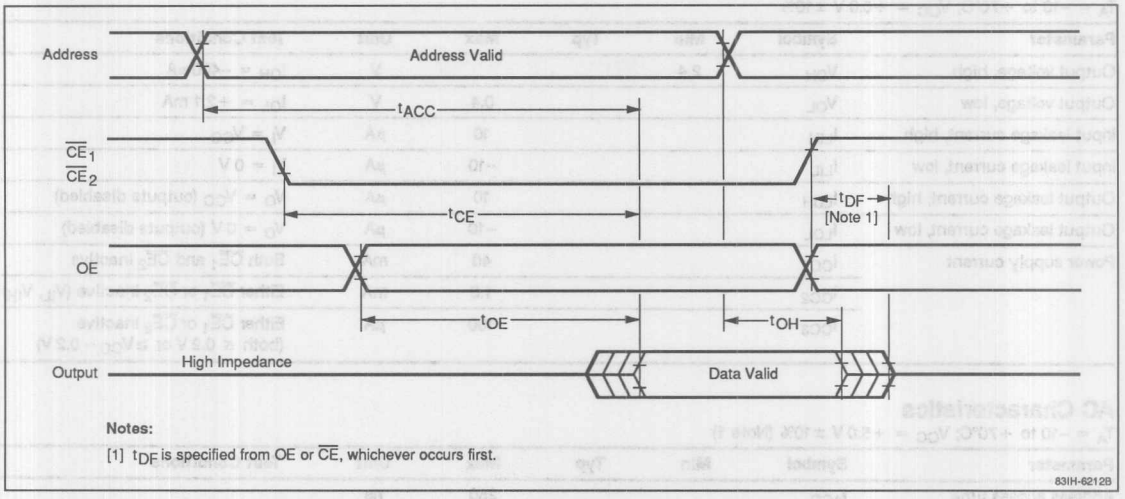
Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions
Address access time	t_{ACC}			250	ns	
Chip enable access time	t_{CE}			250	ns	
Output enable access time	t_{OE}			110	ns	
Output hold time	t_{OH}	0			ns	
Output disable time	t_{DF}	0		60	ns	

Notes:

(1) Input voltage rise and fall times = 20 ns; input and output timing reference levels = 0.8 and 2.0 V; output load = 1 TTL + 100 pF.

11

Timing Waveform



Notes:

[1] t_{DF} is specified from OE or $\overline{CE}$, whichever occurs first.

NEC Electronics Inc.

μPD23C4000
4,194,304-Bit
Mask-Programmable CMOS ROM

Description

The μPD23C4000 is a 4,194,304-bit ROM fabricated with CMOS silicon-gate technology. The device is static in operation and has three-state outputs, fully TTL-compatible inputs and outputs, and an output enable pin which is mask-programmable and can be specified as active low, active high, or don't care.

The μPD23C4000 can be hardware-configured as either 256K x 16 bits or as 512K x 8 bits by tying the WORD/$\overline{\text{BYTE}}$ pin high or low, respectively. In the word configuration, pins O_0-O_{15} are active. In the byte configuration, pin O_{15}/A_{-1} becomes the additional bit required to address 512K bytes.

The μPD23C4000 is available in a 40-pin plastic DIP and a 64-pin plastic QFP.

Features

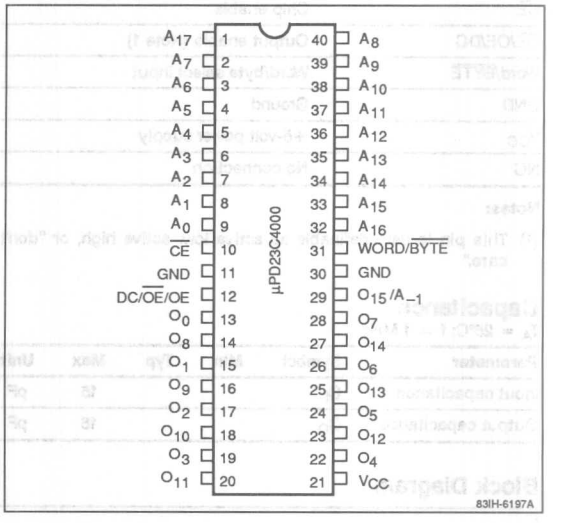
- Programmable organization
  - 262,144 words by 16 bits (word)
  - 524,288 words by 8 bits (byte)
- Fast access time of 250 ns maximum
- TTL-compatible inputs and outputs
- Three-state outputs
- Single +5-volt power supply
- CMOS technology
- Fully static operation
- Low power dissipation
- 40-pin plastic DIP or 64-pin plastic QFP packaging

Ordering Information

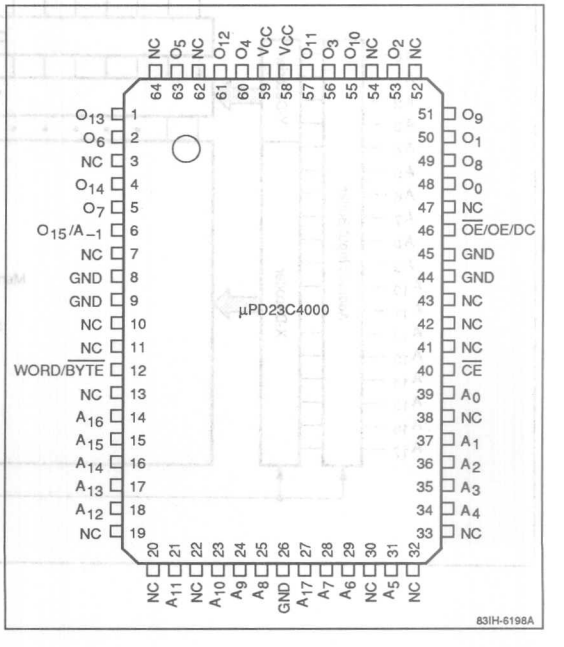
Part Number	Access Time (max)	Package
μPD23C4000C	250 ns	40-pin plastic DIP
μPD23C4000GF	250 ns	64-pin plastic QFP

Pin Configurations

40-Pin Plastic DIP



64-Pin Plastic QFP



11

Pin Identification

Symbol	Function
A_0 - A_{17}	Address inputs
O_0 - O_{14}	Outputs
O_{15}/A_{-1}	Output 15 (word)/LSB address (byte)
$\overline{CE}$	Chip enable
$\overline{OE}$/OE/DC	Output enable (Note 1)
Word/$\overline{BYTE}$	Word/byte select input
GND	Ground
V_{CC}	+5-volt power supply
NC	No connection

Notes:

(1) This pin is user definable as active low, active high, or "don't care."

Capacitance

T_A = 25°C; f = 1 MHz

Parameter	Symbol	Min	Typ	Max	Unit
Input capacitance	C_I			15	pF
Output capacitance	C_O			15	pF

Absolute Maximum Ratings

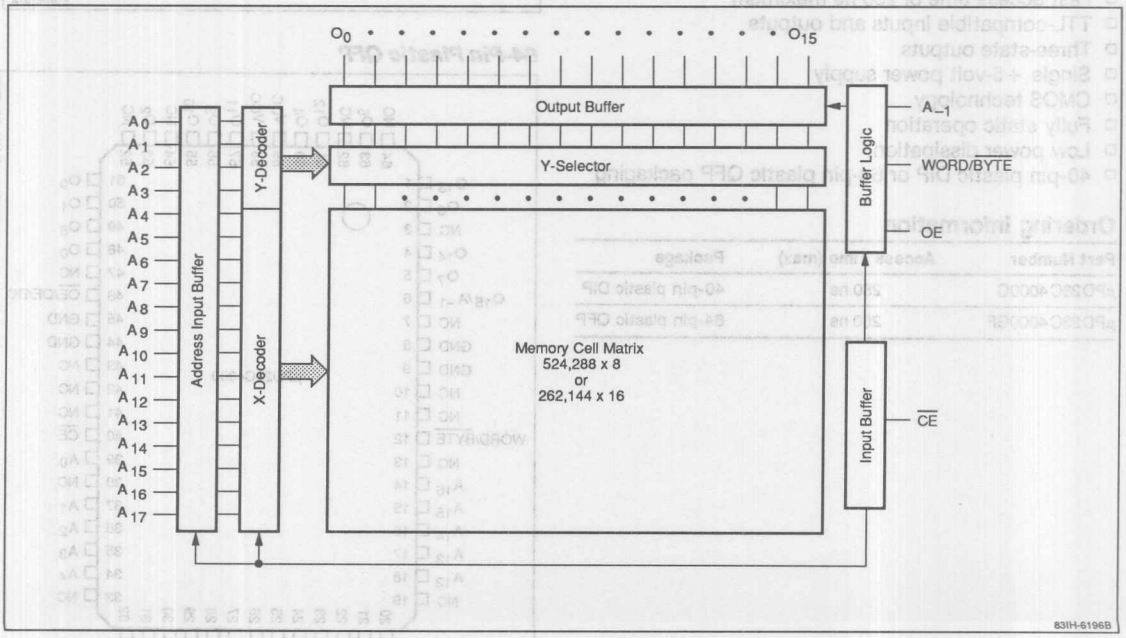
Supply voltage, V_{CC}	−0.3 to +7.0 V
Input voltage, V_I	−0.3 V to V_{CC} + 0.3 V
Output voltage, V_O	−0.3 V to V_{CC} + 0.3 V
Operating temperature, T_{OPR}	−10 to +70°C
Storage temperature, T_{STG}	−65 to +150°C

Exposure to Absolute Maximum Ratings for extended periods may affect device reliability; exceeding the ratings could cause permanent damage. The device should be operated within the limits specified under DC and AC Characteristics.

Recommended Operating Conditions

Parameter	Symbol	Min	Typ	Max	Unit
Input voltage, high	V_{IH}	2.2		V_{CC} + 0.3	V
Input voltage, low	V_{IL}	−0.3		0.8	V
Supply voltage	V_{CC}	4.5	5.0	5.5	V
Ambient temperature	T_A	−10		70	°C

Block Diagram



DC Characteristics

T_A = −10 to +70°C; V_{CC} = +5.0 V ±10%

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions
Output voltage, high	V_{OH}	2.4			V	I_{OH} = −400 μA
Output voltage, low	V_{OL}			0.4	V	I_{OL} = +2.5 mA
Input leakage current	I_{LI}	−10		10	μA	V_I = 0 V to V_{CC}
Output leakage current	I_{LOH}	−10		10	μA	V_O = 0 V to V_{CC}; chip deselected
Power supply current	I_{CC1}			50	mA	$\overline{CE}$ = V_{IL}
	I_{CC2}			1.5	mA	$\overline{CE}$ = V_{IH}; chip deselected
	I_{CC3}			100	μA	$\overline{CE}$ ≥ V_{CC} − 0.2 V; chip deselected

AC Characteristics

T_A = −10 to +70°C; V_{CC} = +5.0 V ±10%

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions
Address access time	t_{ACC}			250	ns	
Chip enable access time	t_{CE}			250	ns	
Output enable access time	t_{OE}			110	ns	
Output hold time	t_{OH}	0			ns	
Output disable time	t_{DF}	0		70	ns	
Output disable time for O_8-O_{15} referenced to WORD/$\overline{BYTE}$	t_{HDF}			100	ns	
Output enable access time referenced to WORD/$\overline{BYTE}$	t_{WB}			250	ns	

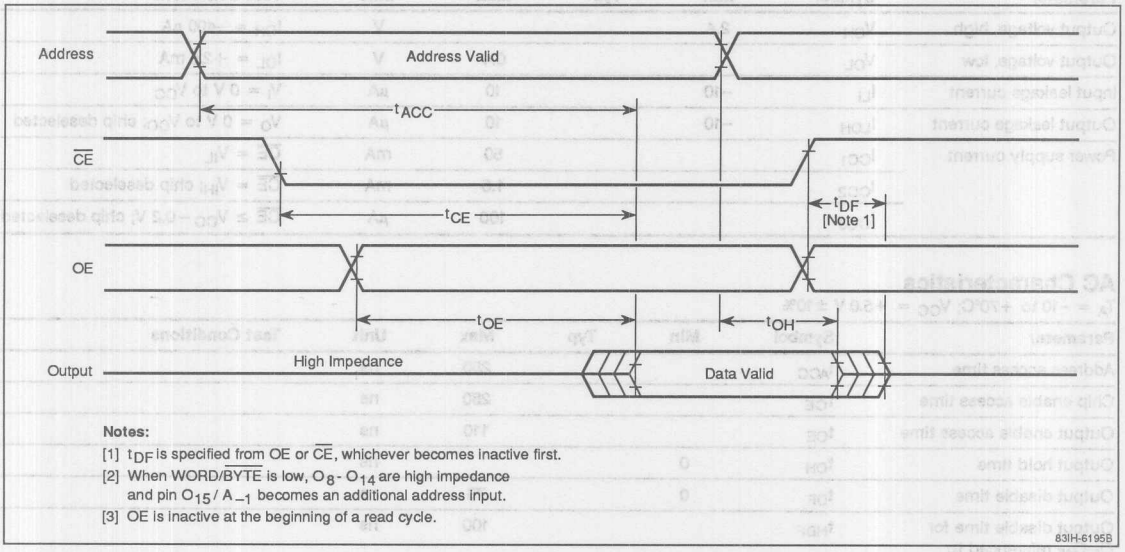
Notes:

(1) Input voltage rise and fall times = 20 ns; input and output timing reference levels = 0.8 and 2.0 V; output load = 1 TTL +100 pF.

11

Timing Waveform

Read Cycle



Notes:

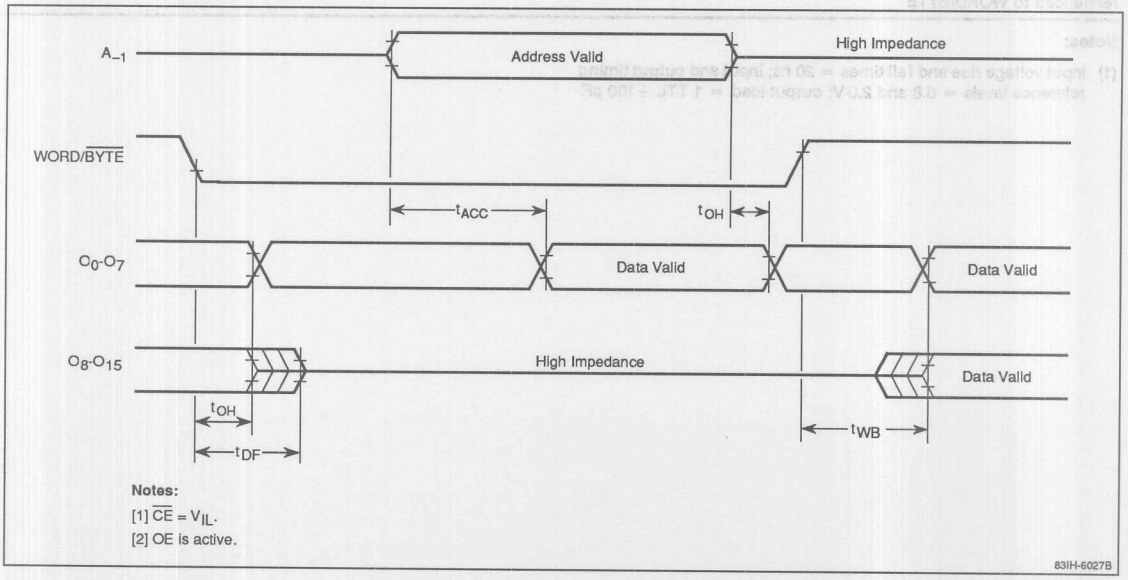
[1] t_{DF} is specified from OE or $\overline{CE}$, whichever becomes inactive first.

[2] When WORD/$\overline{BYTE}$ is low, O_8 - O_{14} are high impedance and pin O_{15} / A_{-1} becomes an additional address input.

[3] OE is inactive at the beginning of a read cycle.

83IH-6195B

WORD/$\overline{BYTE}$ Selection Timing



Notes:

[1] $\overline{CE}$ = V_{IL}.

[2] OE is active.

83IH-6027B

μPD23C4000A
4,194,304-Bit
Mask-Programmable CMOS ROM

Description

The μPD23C4000A is a 4,194,304-bit ROM fabricated with CMOS silicon-gate technology. The device is static in operation and has three-state outputs, fully TTL-compatible inputs and outputs, and an output enable pin which is mask-programmable and can be specified as active low, active high, or don't care.

The μPD23C4000A can be hardware-configured as either 256K x 16 bits or as 512K x 8 bits by tying the WORD/$\overline{\text{BYTE}}$ pin high or low, respectively. In the word configuration, pins O_0-O_{15} are active. In the byte configuration, pin O_{15}/A_{-1} becomes the additional bit required to address 512K bytes.

The μPD23C4000A is available in a 40-pin plastic DIP.

Features

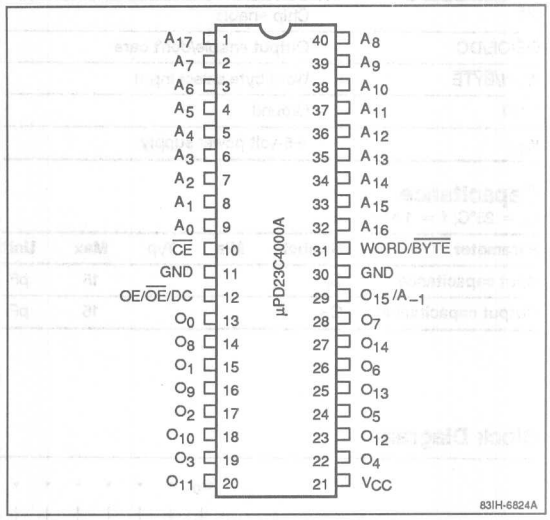
- Programmable organization
  - — 262,144 words by 16 bits (word)
  - — 524,288 words by 8 bits (byte)
- Fast access time of 200 ns maximum
- TTL-compatible inputs and outputs
- Three-state outputs
- Single + 5-volt power supply
- CMOS technology
- Fully static operation
- Low power dissipation
- 40-pin plastic DIP packaging

Ordering Information

Part Number	Access Time (max)	Package
μPD23C4000AC	200 ns	40-pin plastic DIP

Pin Configuration

40-Pin Plastic DIP



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Pin Identification

Symbol	Function
A_0 - A_{17}	Address inputs
O_0 - O_{14}	Outputs
O_{15}/A_{-1}	Output 15 (word)/LSB address (byte)
$\overline{CE}$	Chip enable
$\overline{OE}$/OE/DC	Output enable/don't care
Word/$\overline{BYTE}$	Word/byte select input
GND	Ground
V_{CC}	+5-volt power supply

Capacitance

T_A = 25°C; f = 1 MHz

Parameter	Symbol	Min	Typ	Max	Unit
Input capacitance	C_I			15	pF
Output capacitance	C_O			15	pF

Absolute Maximum Ratings

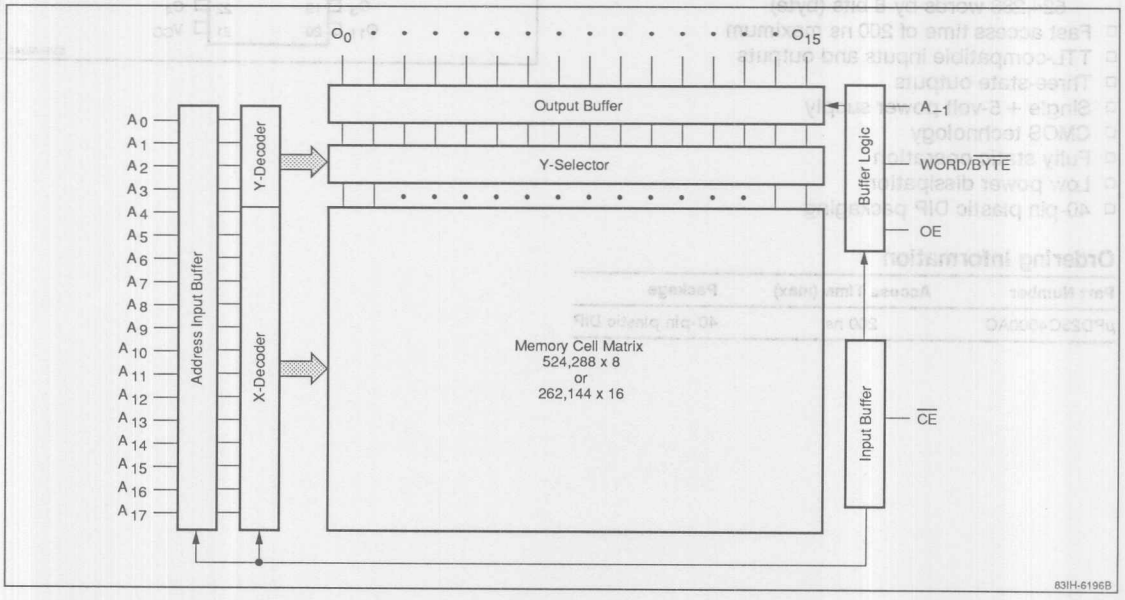
Supply voltage, V_{CC}	−0.3 to +7.0 V
Input voltage, V_I	−0.3 V to V_{CC} + 0.3 V
Output voltage, V_O	−0.3 V to V_{CC} + 0.3 V
Operating temperature, T_{OPR}	−10 to +70°C
Storage temperature, T_{STG}	−65 to +150°C

Exposure to Absolute Maximum Ratings for extended periods may affect device reliability; exceeding the ratings could cause permanent damage. The device should be operated within the limits specified under DC and AC Characteristics.

Recommended Operating Conditions

Parameter	Symbol	Min	Typ	Max	Unit
Input voltage, high	V_{IH}	2.2		V_{CC} + 0.3	V
Input voltage, low	V_{IL}	−0.3		0.8	V
Supply voltage	V_{CC}	4.75	5.0	5.25	V
Ambient temperature	T_A	−10		70	°C

Block Diagram



DC Characteristics

T_A = −10 to +70°C; V_{CC} = +5.0 V ±5%

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions
Output voltage, high	V_{OH}	2.4			V	I_{OH} = −400 μA
Output voltage, low	V_{OL}			0.4	V	I_{OL} = 2.5 mA
Input leakage current, high	I_{IH}	−10		10	μA	V_I = 0 V to V_{CC}
Output leakage current, high	I_{OH}	−10		10	μA	V_O = 0 V to V_{CC}; chip deselected
Power supply current	I_{CC1}			60	mA	$\overline{CE}$ = V_{IL}
	I_{CC2}			1.5	mA	$\overline{CE}$ = V_{IH}; chip deselected
	I_{CC3}			100	μA	$\overline{CE}$ ≥ V_{CC} − 0.2 V; chip deselected

AC Characteristics

T_A = −10 to +70°C; V_{CC} = +5.0 V ±5%

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions
Address access time	t_{ACC}			200	ns	
Chip enable access time	t_{CE}			200	ns	
Output enable access time	t_{OE}			100	ns	
Output hold time	t_{OH}	0			ns	
Output disable time	t_{DF}	0		70	ns	
WORD/$\overline{BYTE}$ output disable time	t_{HDF}			100	ns	
WORD/$\overline{BYTE}$ access time	t_{WB}			200	ns	

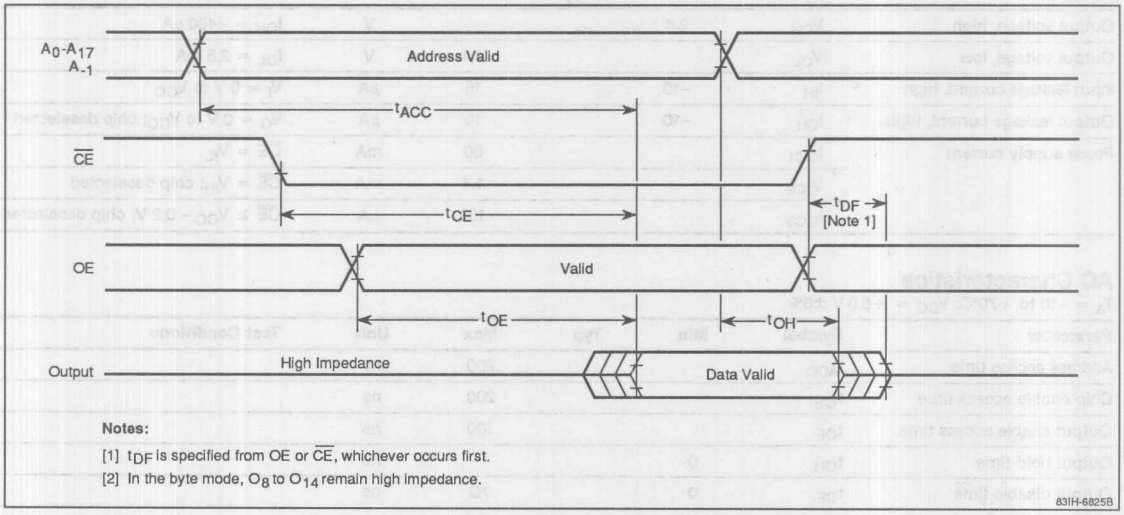
Notes:

(1) Input voltage rise and fall times = 20 ns; input and output timing reference levels = 0.8 and 2.0 V; output load = 1 TTL +100 pF.

11

Timing Waveform

Read Cycle

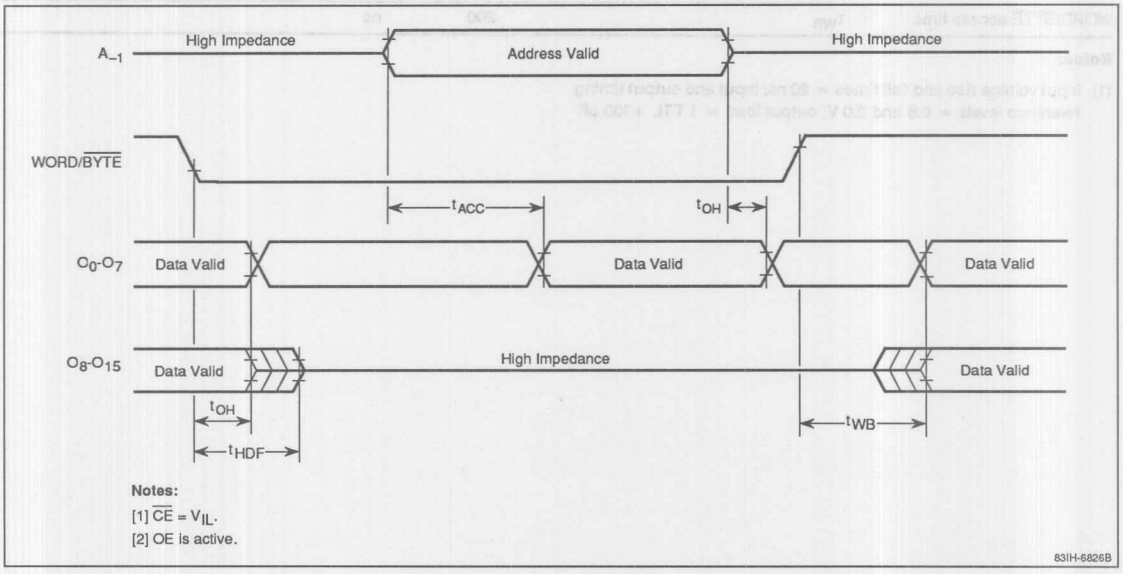


Notes:

[1] t_{DF} is specified from OE or $\overline{CE}$, whichever occurs first.

[2] In the byte mode, O_8 to O_{14} remain high impedance.

Word/Byte Switching



Notes:

[1] $\overline{CE} = V_{IL}$.

[2] OE is active.

NEC Electronics Inc.

μPD23C4001E
524,288 x 8-Bit
Mask-Programmable CMOS ROM

Description

The μPD23C4001E is a 524,288-word by 8-bit static ROM fabricated with CMOS silicon-gate technology and designed to operate from a single +5-volt power supply. It has three-state outputs and fully TTL-compatible inputs and outputs, and is packaged in a 600-mil, 32-pin plastic DIP.

The chip enable and output enable pins are mask-programmable as active low, active high or "don't care."

Features

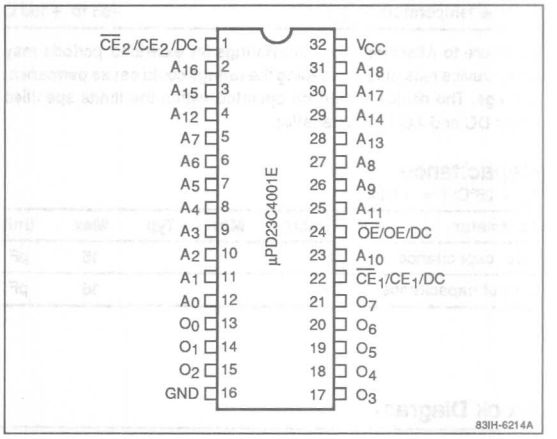
- 524,288-word by 8-bit organization
- Fast access time of 250 ns maximum
- TTL-compatible inputs and outputs
- Three-state outputs
- Single +5-volt power supply
- CMOS process technology
- Fully static operation
- Low power dissipation
  - 220 mW (active)
  - 550 μW (standby)

Ordering Information

Part Number	Access Time (max)	Package
μPD23C4001EC	250 ns	32-pin plastic DIP
μPD23C4001EGW	250 ns	32-pin miniflat

Pin Configuration

32-Pin Plastic DIP and Miniflat



Pin Identification

Symbol	Function
A_0 - A_{18}	Address inputs
O_0 - O_7	Data outputs
$\overline{CE}_1/CE_1/DC$	Chip enable 1/don't care (Note 1)
$\overline{CE}_2/CE_2/DC$	Chip enable 2/don't care (Note 1)
$\overline{OE}/OE/DC$	Output enable (Note 1)
GND	Ground
V_{CC}	+5-volt power supply

Notes:

(1) This pin is user-definable as active low, active high, or "don't care."

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Absolute Maximum Ratings

Supply voltage, V_{CC}	−0.3 to +7.0 V
Input voltage, V_I	−0.3 V to V_{CC} + 0.3 V
Output voltage, V_O	−0.3 V to V_{CC} + 0.3 V
Operating temperature, T_{OPR}	−10 to +70°C
Storage temperature, T_{STG}	−65 to +150°C

Exposure to Absolute Maximum Ratings for extended periods may affect device reliability; exceeding the ratings could cause permanent damage. The device should be operated within the limits specified under DC and AC Characteristics.

Capacitance

T_A = 25°C; f = 1 MHz

Parameter	Symbol	Min	Typ	Max	Unit
Input capacitance	C_I			15	pF
Output capacitance	C_O			15	pF

Truth Table

Function	CE_1	CE_2	OE	Outputs
Standby	I	X	X	High-Z
Standby	X	I	X	High-Z
Active	A	A	I	High-Z
Read	A	A	A	Data out

Notes:

(1) I = inactive.

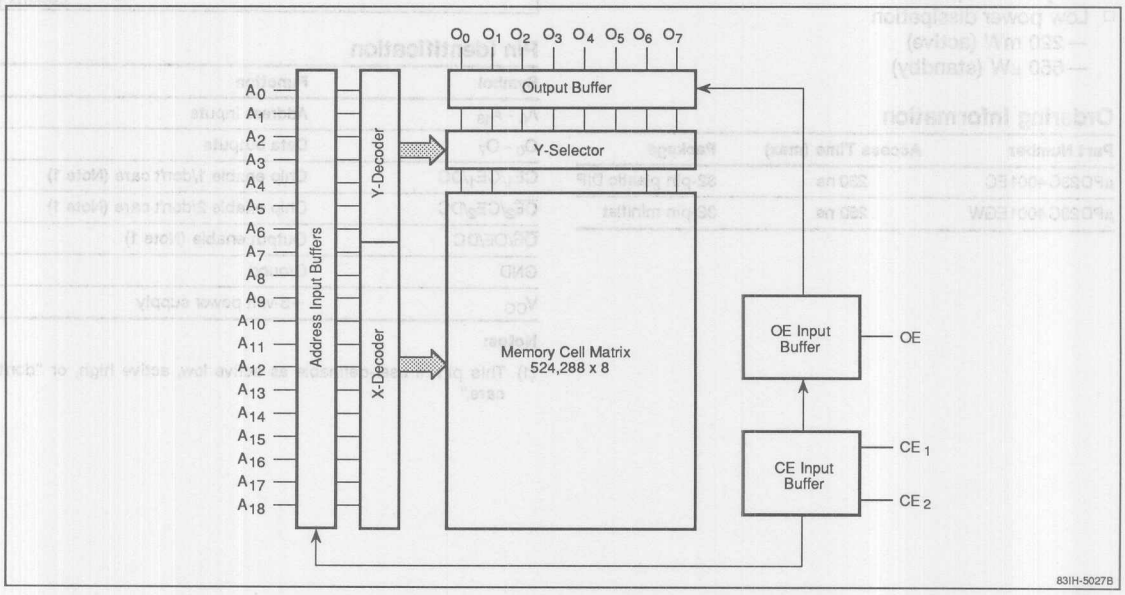
(2) A = active.

(3) X = don't care.

Recommended Operating Conditions

Parameter	Symbol	Min	Typ	Max	Unit
Input voltage, high	V_{IH}	2.2		V_{CC} + 0.3	V
Input voltage, low	V_{IL}	−0.3		0.8	V
Supply voltage	V_{CC}	4.5	5.0	5.5	V
Ambient temperature	T_A	−10		70	°C

Block Diagram



DC Characteristics

T_A = −10 to +70°C; V_{CC} = +5.0 V ±10%

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions
Output voltage, high	V_{OH}	2.4			V	I_{OH} = −400 μA
Output voltage, low	V_{OL}			0.4	V	I_{OL} = +2.1 mA
Input leakage current	I_{LI}	−10		10	μA	V_I = 0 V to V_{CC}
Output leakage current	I_{LO}	−10		10	μA	V_O = 0 V to V_{CC} (outputs disabled)
Power supply current	I_{CC1}			40	mA	Both CE_1 and CE_2 active
	I_{CC2}			1.5	mA	Either CE_1 or CE_2 inactive; CE = V_{IH}
	I_{CC3}			100	μA	Either CE_1 or CE_2 inactive (both ≤ 0.2 V or ≥ V_{CC} − 0.2 V)

AC Characteristics

T_A = −10 to +70°C; V_{CC} = +5.0 V ±10% (Note 1)

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions
Address access time	t_{ACC}			250	ns	
Chip enable access time	t_{CE}			250	ns	
Output enable access time	t_{OE}			110	ns	
Output hold time	t_{OH}	0			ns	
Output disable time	t_{DF}	0		70	ns	(Note 2)

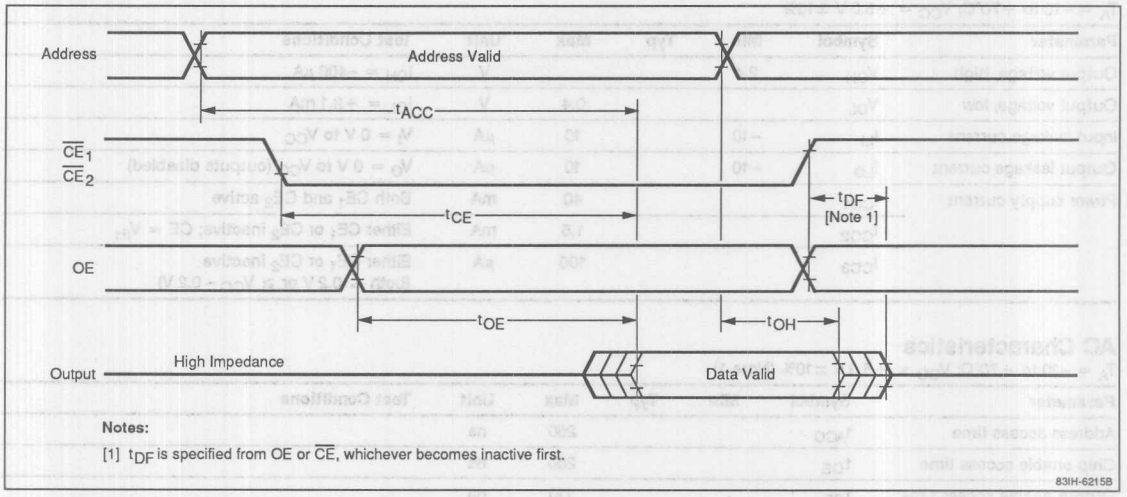
Notes:

(1) Input voltage rise and fall times = 20 ns; input and output timing reference levels = 0.8 and 2.0 V; output load = 1 TTL + 100 pF.

(2) t_{DF} is specified from OE or CE, whichever becomes inactive first.

11

Timing Waveform



Notes:

[1] t_{DF} is specified from OE or $\overline{CE}$, whichever becomes inactive first.

NEC Electronics Inc.

μPD23C8000
8,388,608-Bit
Mask-Programmable CMOS ROM

Description

The μPD23C8000 is a 8,388,608-bit ROM fabricated with CMOS silicon-gate technology. It is static in operation and has three-state outputs, fully TTL-compatible inputs and outputs, and an output enable pin which is mask-programmable and can be specified as active high, active low, or don't care.

The μPD23C8000 can be hardware-configured as either 512K x 16 bits or as 1M x 8 bits by tying the WORD/$\overline{\text{BYTE}}$ pin high or low, respectively. In the word configuration, pins O_0-O_{15} are active. In the byte configuration, pins O_0-O_7 are active, pins O_8-O_{14} are high impedance, and pin O_{15}/A_{-1} becomes the additional bit required to address 1M bytes.

The μPD23C8000 is available in a 42-pin plastic DIP.

Features

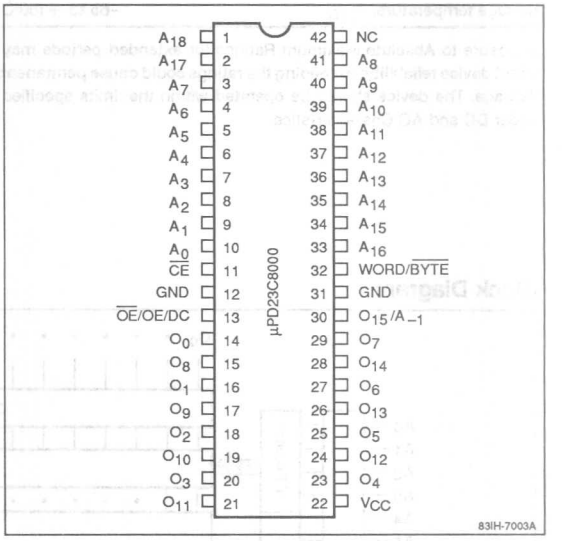
- Programmable organization
  - — 524,288 words by 16 bits (word)
  - — 1,048,576 words by 8 bits (byte)
- Fast access time of 250 ns maximum
- TTL-compatible inputs and outputs
- Three-state outputs
- Single + 5-volt power supply
- CMOS technology
- Fully static operation
- Low power dissipation
- 42-pin plastic DIP packaging

Ordering Information

Part Number	Access Time (max)	Package
μPD23C8000CZ	250 ns	42-pin plastic DIP

Pin Configuration

42-Pin Plastic DIP



Pin Identification

Symbol	Function
A_0 - A_{18}	Address inputs
O_0 - O_{14}	Outputs
O_{15}/A_{-1}	Output 15 (word)/LSB address (byte)
$\overline{CE}$	Chip enable
$\overline{OE}$/OE/DC	Output enable/don't care (Note 1)
WORD/$\overline{BYTE}$	Word/byte select
GND	Ground
V_{CC}	+5-volt power supply
NC	No connection

Notes:

(1) This pin is user-definable as active low, active high, or "don't care."

11

Absolute Maximum Ratings

Supply voltage, V_{CC}	−0.3 to +7.0 V
Input voltage, V_I	−0.3 V to V_{CC} + 0.3 V
Output voltage, V_O	−0.3 V to V_{CC} + 0.3 V
Operating temperature, T_{OPR}	−10 to +70°C
Storage temperature, T_{STG}	−65 to +150°C

Exposure to Absolute Maximum Ratings for extended periods may affect device reliability; exceeding the ratings could cause permanent damage. The device should be operated within the limits specified under DC and AC Characteristics.

Capacitance

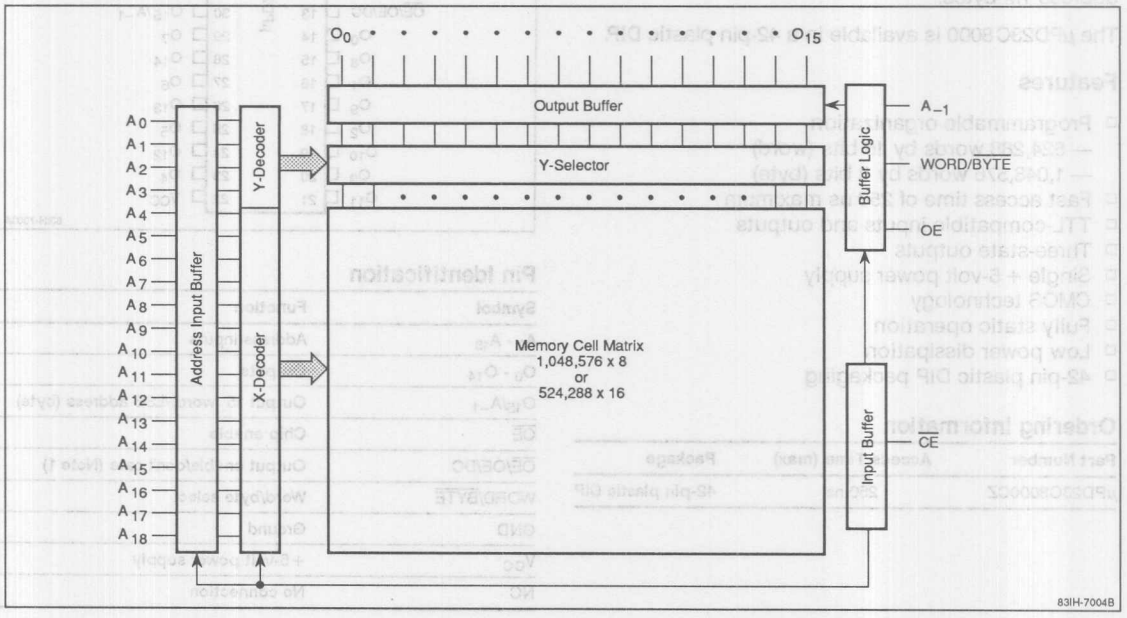
T_A = 25°C; f = 1 MHz

Parameter	Symbol	Min	Typ	Max	Unit
Input capacitance	C_I			15	pF
Output capacitance	C_O			15	pF

Recommended Operating Conditions

Parameter	Symbol	Min	Typ	Max	Unit
Input voltage, high	V_{IH}	2.2		V_{CC} + 0.3	V
Input voltage, low	V_{IL}	−0.3		0.8	V
Supply voltage	V_{CC}	4.5	5.0	5.5	V
Ambient temperature	T_A	−10		70	°C

Block Diagram



DC Characteristics

T_A = −10 to +70°C; V_{CC} = +5.0 V ±10%

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions
Output voltage, high	V_{OH}	2.4			V	I_{OH} = −400 μA
	V_{OH2}	V_{CC} − 0.5			V	I_{OH} = −100 μA
Output voltage, low	V_{OL}			0.4	V	I_{OL} = +2.1 mA
Input leakage current	I_{LI}	−10		10	μA	V_I = 0 V to V_{CC}
Output leakage current	I_{LO}	−10		10	μA	V_O = 0 V to V_{CC}; chip deselected
Power supply current	I_{CC1}			50	mA	$\overline{CE}$ = V_{IL}
	I_{CC2}			1.5	mA	$\overline{CE}$ = V_{IH}; chip deselected
	I_{CC3}			100	μA	$\overline{CE}$ ≥ V_{CC} − 0.2 V; chip deselected

AC Characteristics

T_A = −10 to +70°C; V_{CC} = +5.0 V ±10%

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions
Address access time	t_{ACC}			250	ns	
Chip enable access time	t_{CE}			250	ns	
Output enable access time	t_{OE}			100	ns	
Output hold time	t_{OH}	0			ns	
Output disable time	t_{DF}	0		70	ns	
Output enable access time referenced to WORD/$\overline{BYTE}$	t_{WB}			250	ns	

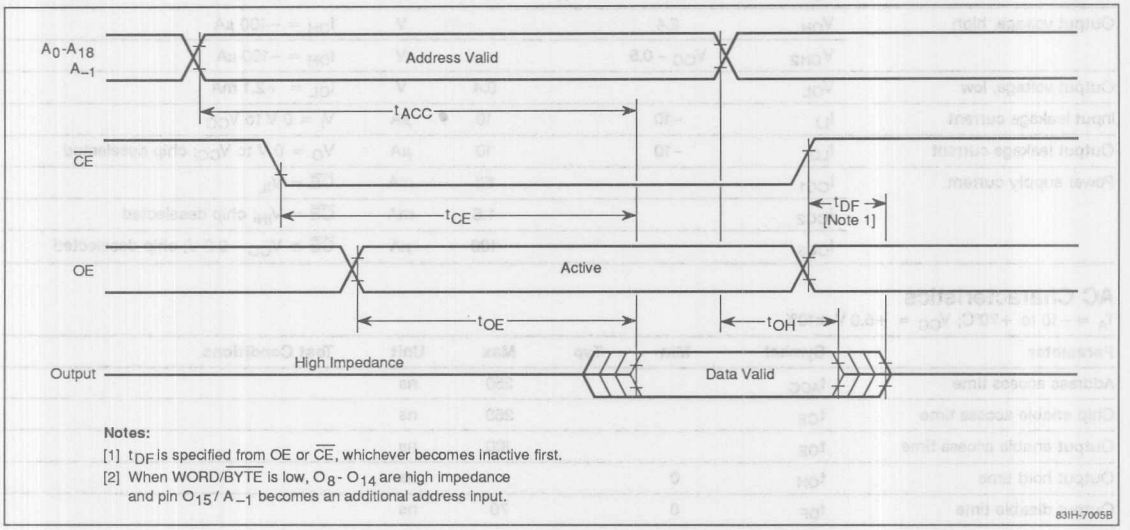
Notes:

(1) Input voltage rise and fall times = 20 ns; input and output timing reference levels = 0.8 and 2.0 V; output load = 1 TTL +100 pF.

11

Timing Waveforms

Read Cycle

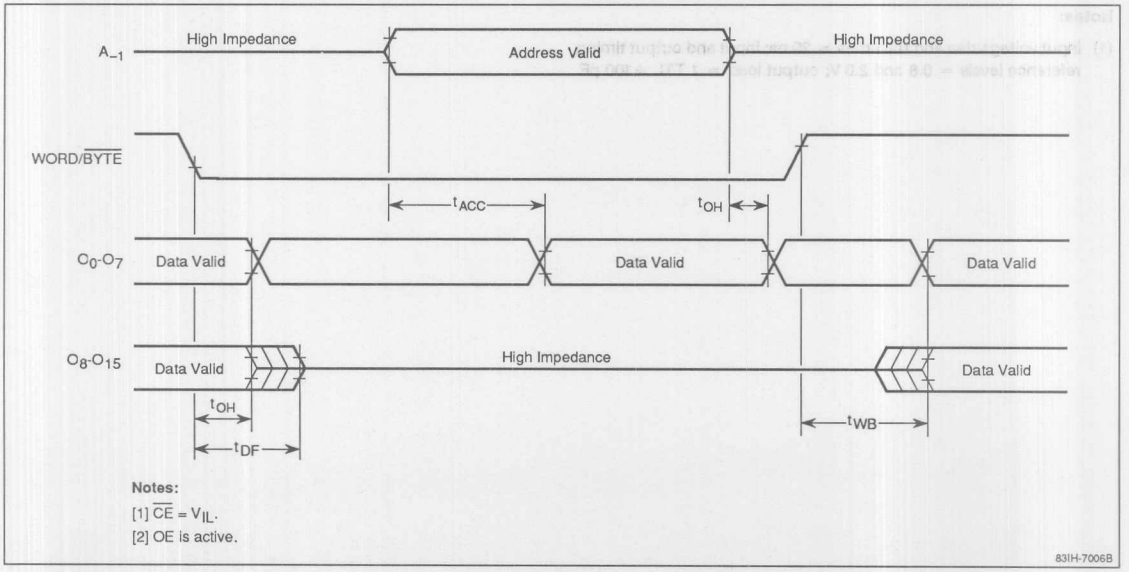


Notes:

[1] t_{DF} is specified from OE or $\overline{CE}$, whichever becomes inactive first.

[2] When WORD/$\overline{BYTE}$ is low, O_8- O_{14} are high impedance and pin O_{15}/ A_{-1} becomes an additional address input.

Word/Byte Selection Timing



Notes:

[1] $\overline{CE}$ = V_{IL}.

[2] OE is active.

NEC Electronics Inc.

μPD23C8001E
1,048,576 x 8-Bit
Mask-Programmable CMOS ROM

Description

The μPD23C8001E is a 1,084,576-word by 8-bit ROM fabricated with CMOS silicon-gate technology and designed to operate from a single +5-volt power supply. The device has three-state outputs, fully TTL-compatible inputs and outputs, and is available in 32-pin plastic DIP and miniflat packaging.

Features

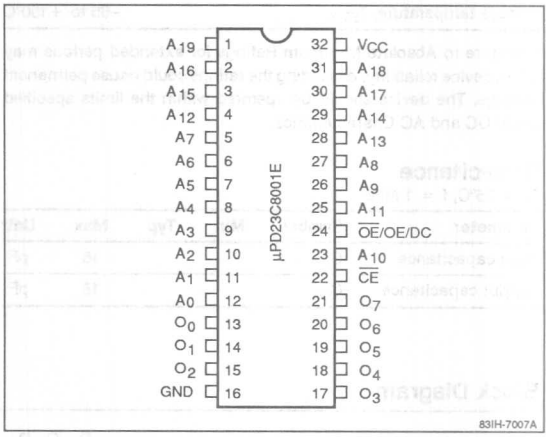
- 1,084,576-word by 8-bit organization
- Fast access time of 250 ns maximum
- TTL-compatible inputs and outputs
- Three-state outputs
- Single +5-volt power supply
- CMOS process technology
- Fully static operation
- Low power dissipation
  - 220 mW (active)
  - 550 μW (standby)

Ordering Information

Part Number	Access Time (max)	Package
μPD23C8001ECZ	250 ns	32-pin plastic DIP
μPD23C8001EGW	250 ns	32-pin plastic miniflat

Pin Configuration

32-Pin Plastic DIP and Miniflat



Pin Identification

Symbol	Function
A_0 - A_{19}	Address inputs
O_0 - O_7	Data outputs
$\overline{CE}$	Chip enable
$\overline{OE}$/OE/DC	Output enable/don't care (Note 1)
GND	Ground
V_{CC}	+5-volt power supply

Notes:

(1) This pin is user-definable as active low, active high, or "don't care."

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Absolute Maximum Ratings

Supply voltage, V_{CC}	−0.3 to +7.0 V
Input voltage, V_I	−0.3 V to V_{CC} + 0.3 V
Output voltage, V_O	−0.3 V to V_{CC} + 0.3 V
Operating temperature, T_{OPR}	−10 to +70°C
Storage temperature, T_{STG}	−65 to +150°C

Exposure to Absolute Maximum Ratings for extended periods may affect device reliability; exceeding the ratings could cause permanent damage. The device should be operated within the limits specified under DC and AC Characteristics.

Capacitance

T_A = 25°C, f = 1 MHz

Parameter	Symbol	Min	Typ	Max	Unit
Input capacitance	C_I			15	pF
Output capacitance	C_O			15	pF

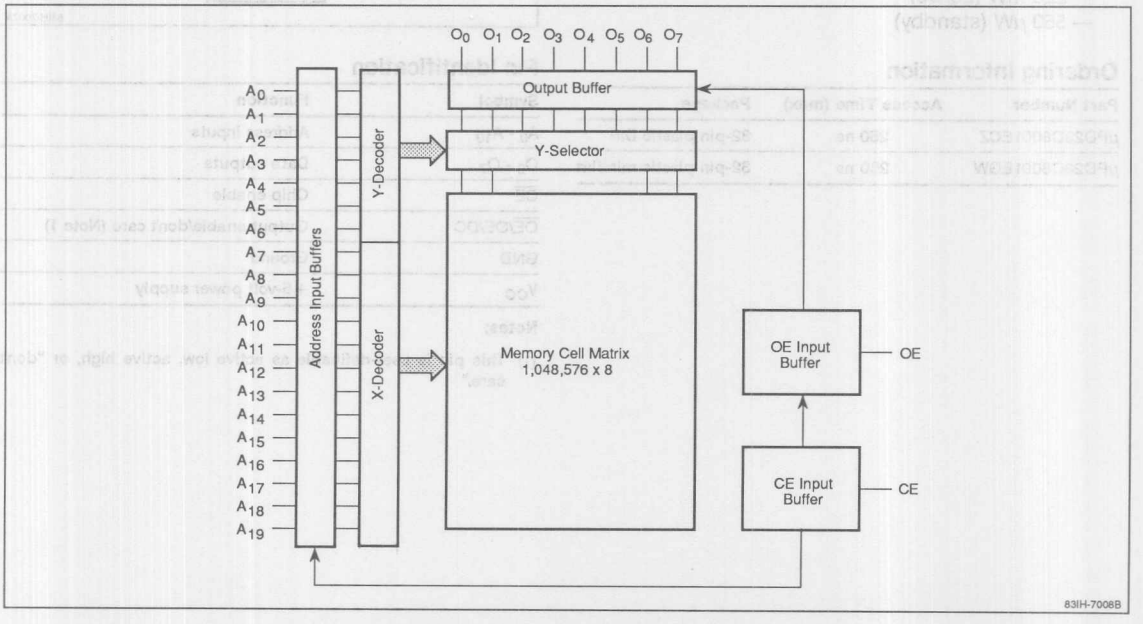
Truth Table

$\overline{CE}$	$\overline{OE}$/OE/DC	Function	Outputs
V_{IH}	Don't care	Standby	High-Z
V_{IL}	Inactive	Active	High-Z
V_{IL}	Active	Read	D_{OUT}

Recommended Operating Conditions

Parameter	Symbol	Min	Typ	Max	Unit
Input voltage, high	V_{IH}	2.2		V_{CC} + 0.3	V
Input voltage, low	V_{IL}	−0.3		0.8	V
Supply voltage	V_{CC}	4.5	5.0	5.5	V
Ambient temperature	T_A	−10		70	°C

Block Diagram



DC Characteristics

T_A = −10 to +70°C; V_{CC} = +5.0 V ±10%

Parameter	Symbol	Min	Max	Unit	Test Conditions
Output voltage, high	V_{OH1}	2.4		V	I_{OH} = −400 μA
	V_{OH2}	V_{CC} −0.5		V	I_{OH} = −100 μA
Output voltage, low	V_{OL}		0.4	V	I_{OL} = 2.1 mA
Input leakage current	I_{LI}	−10	10	μA	V_I = 0 V to V_{CC}
Output leakage current	I_{LO}	−10	10	μA	V_O = 0 V to V_{CC} (chip deselected)
Power supply current	I_{CC1}		40	mA	$\overline{CE}$ = V_{IL}
	I_{CC2}		1.5	mA	$\overline{CE}$ = V_{IH}
	I_{CC3}		100	μA	$\overline{CE}$ ≥ V_{CC} − 0.2 (standby)

AC Characteristics

T_A = −10 to +70°C; V_{CC} = +5.0 V ±10%

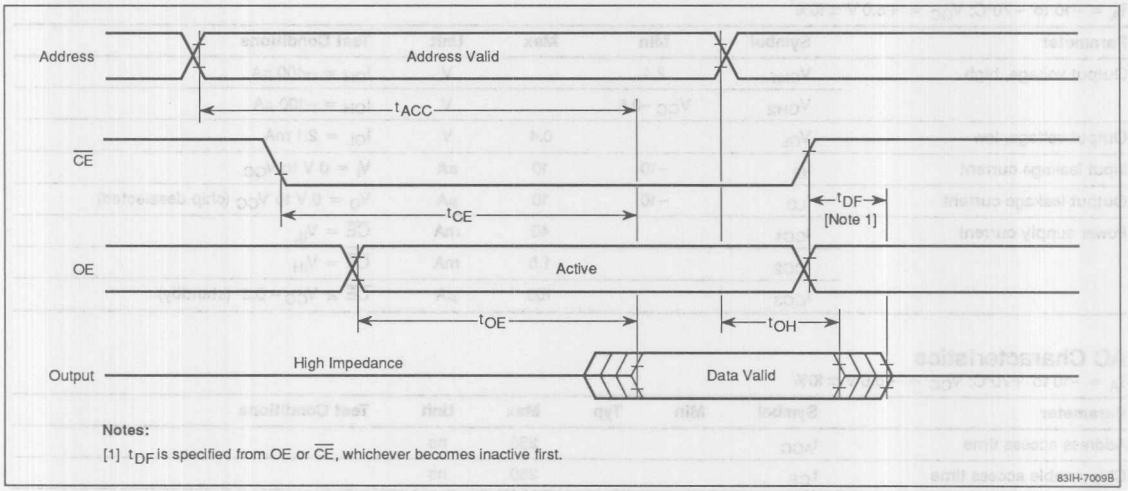
Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions
Address access time	t_{ACC}			250	ns	
Chip enable access time	t_{CE}			250	ns	
Output enable access time	t_{OE}			100	ns	
Output hold time	t_{OH}	0			ns	
Output disable time	t_{DF}	0		70	ns	

Notes:

(1) Input voltage rise and fall times = 20 ns; input and output timing reference levels = 0.8 and 2.0 V; output load = 1 TTL +100 pF.

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Timing Waveform



Notes:

[1] t_{DF} is specified from OE or $\overline{CE}$, whichever becomes inactive first.

μPD23C16000
16,777,216-Bit
Mask-Programmable CMOS ROM

Description

The μPD23C16000 is a 16,777,216-bit ROM fabricated with CMOS silicon-gate technology. The device is static in operation and has three-state outputs and fully TTL-compatible inputs and outputs.

The μPD23C16000 can be configured as either 1M x 16 bits or as 2M x 8 bits by tying the WORD/$\overline{\text{BYTE}}$ pin high or low, respectively. In the word configuration, pins O_0 - O_{15} are active. In the byte configuration, pins O_0 - O_7 are active, pins O_8 - O_{14} are high impedance, and pin O_{15}/A_{-1} becomes the additional bit required to address 2 Mbytes.

The μPD23C16000 is available in a 42-pin plastic DIP.

Features

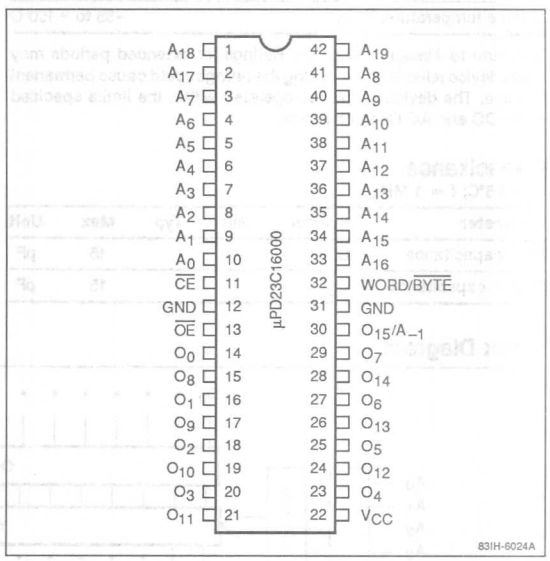
- User-selectable organization
  - 1,048,576 words by 16 bits (word)
  - 2,097,152 words by 8 bits (byte)
- Fast access time: 250 ns maximum
- TTL-compatible inputs and outputs
- Three-state outputs
- Single +5-volt power supply
- CMOS technology
- Fully static operation
- Low power dissipation
- 42-pin plastic DIP packaging

Ordering Information

Part Number	Access Time (max)	Package
μPD23C16000CZ	250 ns	42-pin plastic DIP

Pin Configuration

42-Pin Plastic DIP



Pin Identification

Symbol	Function
A_0 - A_{19}	Address inputs
O_0 - O_{14}	Outputs
O_{15}/A_{-1}	Output 15 (word)/LSB address (byte)
WORD/$\overline{\text{BYTE}}$	Word/byte selection
$\overline{\text{CE}}$	Chip enable
$\overline{\text{OE}}$	Output enable
GND	Ground
V_{CC}	+5-volt power supply

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Absolute Maximum Ratings

Supply voltage, V_{CC}	−0.3 to +7.0 V
Input voltage, V_I	−0.3 V to V_{CC} +0.3 V
Output voltage, V_O	−0.3 V to V_{CC} +0.3 V
Operating temperature, T_{OPR}	−10 to +70°C
Storage temperature, T_{STG}	−65 to +150°C

Exposure to Absolute Maximum Ratings for extended periods may affect device reliability; exceeding the ratings could cause permanent damage. The device should be operated within the limits specified under DC and AC Characteristics.

Recommended Operating Conditions

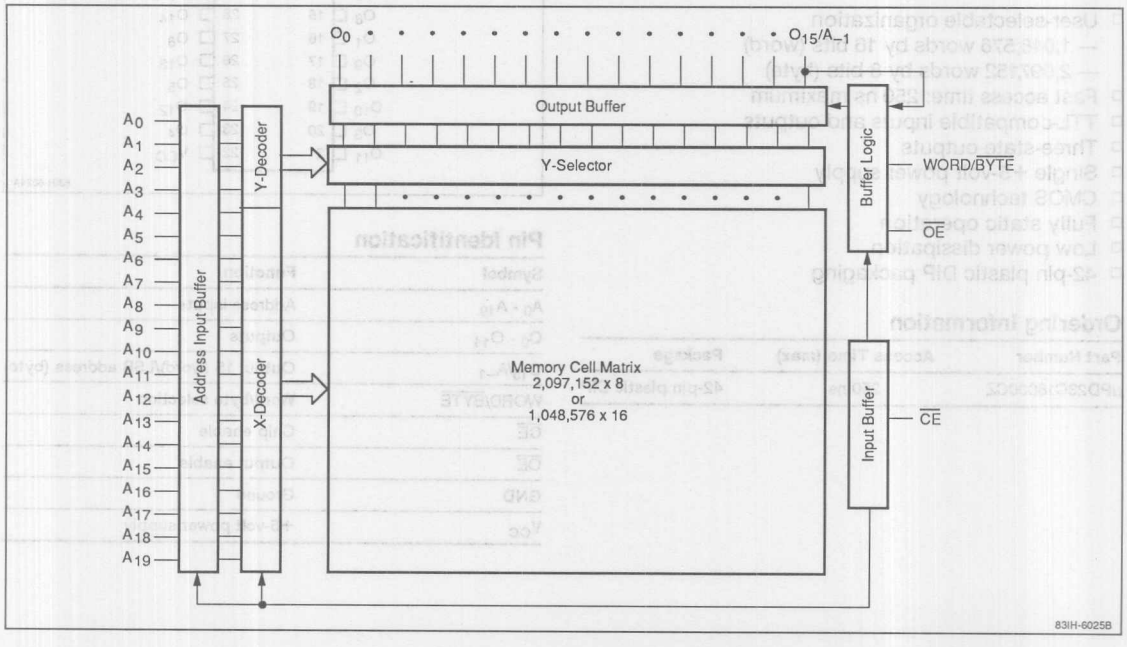
Parameter	Symbol	Min	Typ	Max	Unit
Input voltage, high	V_{IH}	2.2		V_{CC} + 0.3	V
Input voltage, low	V_{IL}	−0.3		0.8	V
Supply voltage	V_{CC}	4.5	5.0	5.5	V
Ambient temperature	T_A	−10		70	°C

Capacitance

T_A = 25°C; f = 1 MHz

Parameter	Symbol	Min	Typ	Max	Unit
Input capacitance	C_I			15	pF
Output capacitance	C_O			15	pF

Block Diagram



DC Characteristics

T_A = −10 to +70 °C; V_{CC} = +5.0 V ± 10%

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions
Output voltage, high	V_{OH}	2.4			V	I_{OH} = −400 μA
Output voltage, low	V_{OL}			0.4	V	I_{OL} = +3.2 mA
Input leakage current	I_{LI}	−10		10	μA	V_I = 0 V to V_{CC}
Output leakage current	I_{LO}	−10		10	μA	V_O = 0 V to V_{CC}; chip deselected
Power supply current	I_{CC1}			50	mA	$\overline{CE}$ = V_{IL}
	I_{CC2}			1.5	mA	$\overline{CE}$ = V_{IH}; chip deselected
	I_{CC3}			100	μA	$\overline{CE}$ = V_{CC} − 0.2 V; chip deselected

AC Characteristics

T_A = −10 to +70 °C; V_{CC} = +5.0 V ± 10%

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions
Address access time	t_{ACC}			250	ns	
Chip enable access time	t_{CE}			250	ns	
Output enable access time	t_{OE}			100	ns	
Output hold time	t_{OH}	0			ns	
Output disable time	t_{DF}	0		70	ns	
Output enable access time referenced to WORD/$\overline{BYTE}$	t_{WB}			250	ns	

Notes:

(1) Input voltage rise and fall times = 20 ns; input and output timing reference levels = 0.8 V and 2.0 V; output load = 1 TTL + 100 pF.

Truth Table

$\overline{CE}$	$\overline{OE}$	WORD/$\overline{BYTE}$	Mode	O_0 - O_7	O_8 - O_{14}	O_{15}/A_{-1}	I_{CC}
V_{IH}	X	X	Not selected	High-Z	High-Z	High-Z	Standby
V_{IL}	V_{IH}	X	Output disable	High-Z	High-Z	High-Z	Active
V_{IL}	V_{IL}	V_{IL}	Selected	Data output	High-Z	LSB	Active
V_{IL}	V_{IL}	V_{IH}	Selected	Data output	Data output	Data output	Active

Notes:

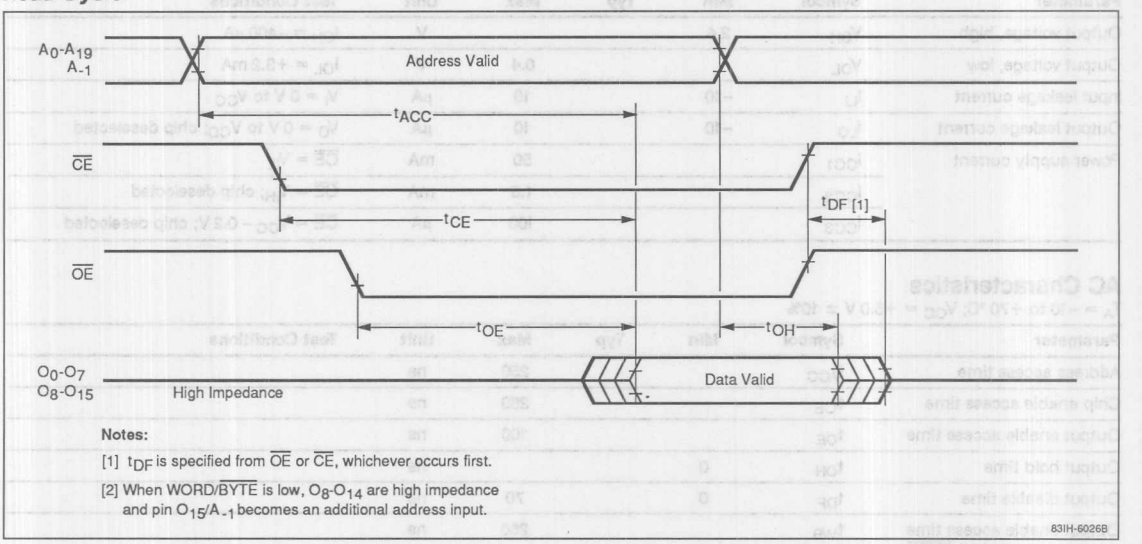
(1) X = don't care.

(2) LSB = least significant bit of the address input.

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Timing Waveforms

Read Cycle

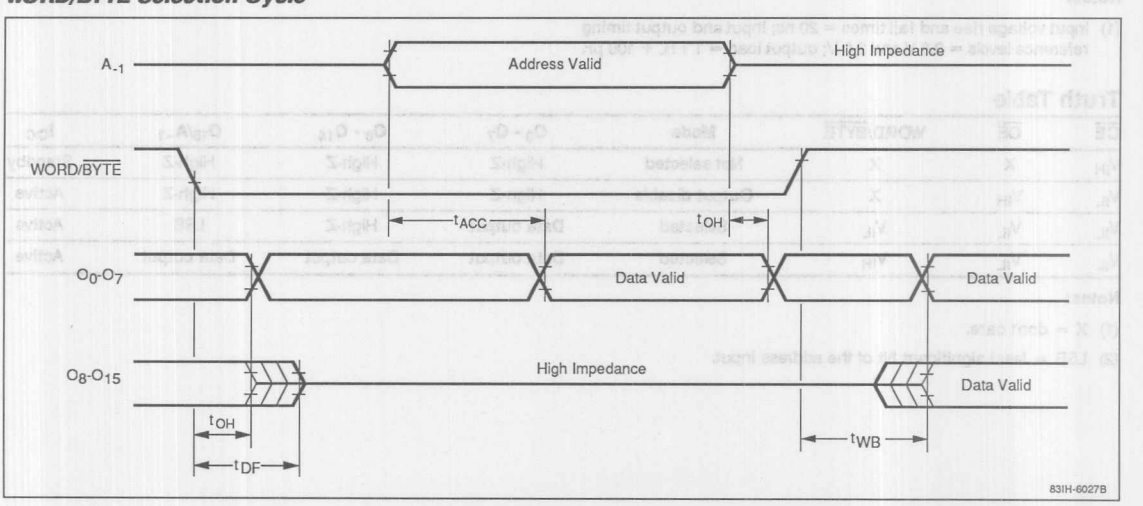


Notes:

[1] t_{DF} is specified from $\overline{OE}$ or $\overline{CE}$, whichever occurs first.

[2] When WORD/$\overline{BYTE}$ is low, O_8-O_{14} are high impedance and pin O_{15}/A_{-1} becomes an additional address input.

WORD/$\overline{BYTE}$ Selection Cycle



Introduction

This application note provides guidelines for submitting the data files used by NEC to program semicustomized integrated circuits (a complete list of which appears in table 4).

Where to Send Files

Data files should be sent directly to Customer Marketing, NEC Electronics, Mountain View, California.

Acceptable Media

NEC accepts data from the following:

- In programmable ICs such as NEC's μPD27C2000 UV EPROM or μPD75P308 programmable 4-bit microprocessor
- On floppy diskette in MS-DOS® or PC-DOS® formats

— 5-1/4 inch disk (either 360K or 1.2 Mbyte)
— 3-1/2 inch disk (either 360K, 720K or 1.44 Mbyte)

- Via modem over the telephone lines

— At 300 to 9600 bps
— With 8 data bits, no parity, 1 stop bit
— Using XMODEM, YMODEM or KERMIT protocol

When opting for modem transmittal, call Customer Marketing for the appropriate engineering contact, dial-up number, and hours of availability.

MS-DOS and PC-DOS are registered trademarks of Microsoft.
Intel is a trademark of Intel.

Minimum Requirements

Any one of the means described above may be selected, but NEC requires multiple copies of every file, as well as device-specific information such as chip type, package type and package lead type.

- A minimum of two copies of the chosen media must be submitted. Three copies are preferred, as this lessens the problems caused when one copy is flawed. Please note that for modem transfers, the file must be transmitted twice to NEC and retransmitted twice from NEC back to you.
- Unless submitted by means of programmable ICs, data files must be in Intel™ hexadecimal or extended hexadecimal format.
- Source code or the executable binary of a data file may be submitted but is not required.
- Files taken from or read from previously built ICs, even those produced for you by NEC, will not be accepted.

Taking Precautions

NEC assumes no responsibility for data bits within a target device's programmable area, and it is therefore imperative that you define all bits within the possible range of addresses. For example, if programmable area is 128K x 8 bits, and your data file defines only the first 64K x 8 bits, there is no way for NEC to know how to program the remaining 64K.

Furthermore, if your programming equipment was left with random data in its memory from a previous operation, valid data would be built into the first half of the programmable area and garbage data into the second half—causing unforeseen and possibly very expensive problems in the final design. Blank space must be defined as either all 0s or all 1s, or as binary NOP, in which case the binary code for an NOP instruction needs to be specified.

What You Can Expect from NEC

After the media or devices have been received by NEC, the copies will be compared to ensure they match (customers whose files don't match will be contacted by Customer Marketing). NEC will then duplicate the media and return the following for verification:

- One copy of the original media
- One copy of NEC's duplicate media
- A hard copy listing of the data files (for target devices with less than 512K, i.e., 64K x 8, of ROM)
- Two floppy diskettes containing those data files transmitted via modem
- A ROM Code Verification Form, which must be signed and returned before any devices can be built

Upon receipt of the signed verification form, NEC will produce ten engineering samples for testing and approval prior to building and shipping the entire order. Data files are kept in archival storage for two years (more than two years is not guaranteed) in one or more of the following formats:

- In one original IC and one NEC duplicate IC, if programmable ICs were initially submitted
- In a hard-copy listing of the hexadecimal file
- In electronic storage using either magnetic or optical media (Write Once Read Many, i.e., WORM, disk)

Please note that IC masks will be stored at NEC's manufacturing facility for only one year after the last order is received.

Peculiar Addressing

Although addresses are usually contiguous, e.g., from 0000_{16} to a maximum, these devices require special consideration.

μPD77P20, μPD7720, μPD77C20. The first two locations of data ROM cannot be used in these devices. In the μPD77P20, addresses 0_{16} and 1_{16} must be left blank. (In UV EPROMs, addresses 800_{16} and 805_{16} must be left blank.)

μPD70322/332 (V25™ and V35™). Addresses $FF00_{16}$ through $FFEF_{16}$ and $FFF8_{16}$ through $FFFF_{16}$ are reserved for IC testing purposes by the factory and may not be used.

μPD75104 - μPD75516 (μPD75xxx-Series). Special requirements for these devices are shown below.

Table 1. Valid Addresses for μPD75xxx-Series

Device	Initial Address	Last Address
μPD75106	0000_{16}	$177F_{16}$
μPD75108	0000_{16}	$1F7F_{16}$
μPD75208	0000_{16}	$1F7F_{16}$
μPD75216	0000_{16}	$3F7F_{16}$
μPD75308	0000_{16}	$1F7F_{16}$
μPD75316	0000_{16}	$3F7F_{16}$

ROMs with 16-Bit Data Buses. Data submitted for these ROMs in devices with 8-bit data buses should be organized this way.

Table 2. Sequence for 8-Bit Data Bus Devices

Sequence	Addresses	Outputs
Device #1	00000 - 0FFFF	O_0 - O_7
Device #2	10000 - 1FFFF	O_0 - O_7
Device #3	00000 - 0FFFF	O_8 - O_{15}
Device #4	10000 - 1FFFF	O_8 - O_{15}

Data submitted from a 16-bit data bus device would be handled similarly.

Table 3. Sequence for 16-Bit Data Bus Devices

Sequence	Addresses	Outputs
Device #1	00000 - 0FFFF	O_0 - O_7
	10000 - 1FFFF	O_8 - O_{15}

In both cases, segments corresponding to the lower data outputs are submitted first, a pattern that should be followed for larger devices as well. Please be aware that NEC has no way of identifying the sequential order of individual segments if they're submitted in incorrect order.

Refer to the section entitled ORGANIZING 16-BIT DEVICE DATA INTO HEX FORMAT for more detailed information about these requirements.

V25 and V35 are trademarks of NEC Corporation.

Table 4. Applicable Device Types

Part Number(s)	Description	Organization	Last Address
ROMs	CMOS ROM		
μPD23C1000A		131,072 x 8 bits	
μPD23C1000EA		131,072 x 8 bits	
μPD23C1001E		131,072 x 8 bits	
μPD23C1010A		131,072 x 8 bits	
μPD23C1024E		65,536 x 16 bits	
μPD23C2000		262,144 x 8 bits or 131,072 x 16 bits	
UPD23C2000A		262,144 x 8 bits or 131,072 x 16 bits	
μPD23C2001		262,144 x 8 bits	
μPD23C4000		524,288 x 8 bits or 262,144 x 16 bits	
μPD23C4000A		524,288 x 8 bits or 262,144 x 16 bits	
μPD23C4001E		524,288 x 8 bits	
μPD23C8000		1,048,576 x 8 bits or 524,288 x 16 bits	
μPD23C8001E		1,048,576 x 8 bits	
μPD23C16000		2,097,152 x 8 bits or 1,048,576 x 16 bits	
4-Bit Microcomputers	μC with ROM memory		
μPD7502		2,048 x 8 bits	
μPD7503		4,096 x 8 bits	
μPD7507H		2,048 x 8 bits	
μPD7508H		4,096 x 8 bits	
μPD7514		4,096 x 8 bits	
μPD7527A		2,048 x 8 bits	
μPD7528A/CG28E		4,096 x 8 bits	
μPD7533/CG33E		4,096 x 8 bits	
μPD7537A		2,048 x 8 bits	
μPD7538A/CG38E		4,096 x 8 bits	
μPD7554/64		1,024 x 8 bits	
μPD7556/66		1,024 x 8 bits	
μPD75004/104/304		4,096 bits	
μPD75006/106/206/306		6,144 bits	$177F_{16}$
μPD75008/108/208/308		8,192 bits	$1F7F_{16}$
μPD75112/212A/312		12,288 bits	$2F7F_{16}$
μPD75116/216A/316		16,384 bits	$3F7FF_{16}$
μPD75328		8,192 bits	$1F7F_{16}$
μPD75402		2,048 bits	$F7F_{16}$
μPD75516		16,384 bits	$3F7F_{16}$

Table 4. Applicable Device Types (cont)

Part Number(s)	Description	Organization	Last Address
8-Bit Microcomputers	μC with ROM memory		
μPD7810/11		4,096 x 8 bits	
μPD78C11A		4,096 x 8 bits	
μPD78C12A		8,192 x 8 bits	
μPD78C14		16,384 x 8 bits	
μPD7821x-Series		16,384 x 8 bits	
μPD7822x-Series		16,384 x 8 bits	
μPD7823x-Series		16,384 x 8 bits	
μPD78312A		8,192 x 8 bits	
μPD78322		16,384 x 8 bits	
Digital Signal Processors			
μPD7720A/C20A	Instruction ROM	512 x 23 bits	
	Data ROM	510 x 13 bits	
μPD77C25	Instruction ROM	2,048 x 24 bits	
	Data ROM	1,024 x 16 bits	
μPD77220/230	Instruction ROM	2,048 x 24 bits	
	Data ROM	1,024 x 24 bits	
μPD77810	Instruction ROM	2,048 x 24 bits	
	Data ROM	1,024 x 16 bits	
μPD7755	ROM memory	98,304 bits	
μPD7756	ROM memory	262,144 bits	
μPD7757	ROM memory	524,288 bits	

USING THE INTEL HEXADECIMAL FORMAT

Intel's hexadecimal format allows addressing of up to 512 kbits of data, or 64K x 8 bits (0000_{16} through $FFFF_{16}$). Data records larger than 64K x 8 must be expressed in multiple segments, with each individually addressed segment equal to or smaller than 64K x 8.

Each byte of data must be expressed as a printable ASCII character, and each line must contain these elements:

- A colon to begin each line
- A two-character data word count for the line
- A four-character address of the first word of data
- A two-character record type identifier, e.g., 00, 01, 02 for data, end of file, segment address
- The data words
- A two-character line checksum at the end of each line

For example, a line showing the "End of File" record would be formatted as :00000001FF, while a typical data line would be constructed this way:

:WWAAAATTDDDDDDDDDDDDDDDDDDDDDDDDDDDDDDDDCC

Table 5. Description of Elements

Code	Description
:	Beginning of line
WW	Data word count
AAAA	Address of the first data word
TT	Record type
D...D	Data words
CC	Checksum

Table 6. Description of Record Type

TT	Description
00	Data follows
01	End of file
02	Begin new 64K x 8 data segment

Table 7 shows an address shift from one 32K x 8 segment to the next segment in hexadecimal format.

Table 7. Sample Hexadecimal Addressing

Coded Segment	Instruction
:100000007F7F7F7F7F7E7D7B797878787A7D2C	Begin first segment
:10FFF000FFFFFFFFFFFFFFFFFFFFFFFFFFFF11	End first segment
:020000021000EC	Second segment record
:100000007F7F7F7F7E7E7D7B7A797877797B7F2C	Begin second segment
:10FFF000FFFFFFFFFFFFFFFFFFFFFFFFFFFF11	End second segment
:00000001FF	End of file record

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ORGANIZING 16-BIT DEVICE DATA INTO HEX

The following examples illustrate how 16-bit devices may be organized into 8-bit hexadecimal format.

When ordering the 64K x 16-Bit μPD23C1024, it is recommended that data files be submitted in devices such as the 64K x 16-Bit μPD27C1024 because there's a one-to-one match of addresses, device outputs, and data word length. Data files submitted in two μPD27C512 64K x 8 EPROMs, for example, would have to be organized in this sequence.

Table 8. Sequence of Two 64K x 16-Bit Devices

μPD27C512	Addresses	Data Outputs
Device #1	0000_{16} - $FFFF_{16}$	O_0 - O_7
Device #2	0000_{16} - $FFFF_{16}$	O_8 - O_{15}

If data is submitted in four 32K x 8-bit devices such as the μPD27C256, then the following would apply.

Table 9. Sequence of Four 32K x 8-Bit Devices

μPD27C256	Addresses	Data Outputs
Device #1	0000_{16} - $7FFF_{16}$	O_0 - O_7
Device #2	8000_{16} - $FFFF_{16}$	O_0 - O_7
Device #3	0000_{16} - $7FFF_{16}$	O_8 - O_{15}
Device #4	8000_{16} - $FFFF_{16}$	O_8 - O_{15}

When ordering the 128K x 16 μPD23C2000, data files submitted in two 128K x 8-bit EPROMs such as the μPD27C1001 should be organized as shown in table 10.

Table 10. Sequence of Two 128K x 8-Bit Devices

μPD27C1001	Addresses	Data Outputs
Device #1	0000_{16} - $1FFFF_{16}$	O_0 - O_7
Device #2	0000_{16} - $1FFFF_{16}$	O_8 - O_{15}

Data files submitted in four 64K x 8-bit μPD27C512 devices would require this sequence.

Table 11. Sequence of Four 64K x 8-Bit Devices

μPD27C512	Addresses	Data Outputs
Device #1	00000_{16} - $0FFFF_{16}$	O_0 - O_7
Device #2	10000_{16} - $1FFFF_{16}$	O_0 - O_7
Device #3	00000_{16} - $0FFFF_{16}$	O_8 - O_{15}
Device #4	10000_{16} - $1FFFF_{16}$	O_8 - O_{15}

When ordering the 256K x 16-bit μPD23C4000, data submitted in four 64K x 16-bit devices such as the μPD27C1024 EPROM should be organized as shown in table 12.

Table 12. Sequence of Four 64K x 16-Bit Devices

μPD27C1024	Addresses	Data Outputs
Device #1	00000_{16} - $0FFFF_{16}$	O_0 - O_{15}
Device #2	10000_{16} - $1FFFF_{16}$	O_0 - O_{15}
Device #3	20000_{16} - $2FFFF_{16}$	O_0 - O_{15}
Device #4	30000_{16} - $3FFFF_{16}$	O_0 - O_{15}

If eight 64K x 8-bit devices such as the μPD27C512 are being used, the following applies.

Table 13. Sequence of Eight 64K x 8-Bit Devices

μPD27C512	Addresses	Data Outputs
Device #1	00000_{16} - $0FFFF_{16}$	O_0 - O_7
Device #2	00000_{16} - $0FFFF_{16}$	O_8 - O_{15}
Device #3	10000_{16} - $1FFFF_{16}$	O_0 - O_7
Device #4	10000_{16} - $1FFFF_{16}$	O_8 - O_{15}
Device #5	20000_{16} - $2FFFF_{16}$	O_0 - O_7
Device #6	20000_{16} - $2FFFF_{16}$	O_8 - O_{15}
Device #7	30000_{16} - $3FFFF_{16}$	O_0 - O_7
Device #8	30000_{16} - $3FFFF_{16}$	O_8 - O_{15}

NEC

Packaging Information 12

Section 12
Packaging Information

Device/Package Cross Reference	12-1
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18-Pin Packages	12-6
20-Pin Packages	12-8
22-Pin Packages	12-10
24-Pin Packages	12-12
26/20-Pin Packages	12-19
28-Pin Packages	12-20
30-Pin Packages	12-24
32-Pin Packages	12-29
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42-Pin Packages	12-36
52-Pin Package	12-37
60-Pin Package	12-38
64-Pin Package	12-39
72-Pin Packages	12-40

Device/Package Cross Reference

Part Number	Package	Ordering Designation	Page
MC-157	30-Pin SIMM (Socket-Mountable) #7	B	12-29
MC-174/176	60-Pin IC Card	N/A	12-38
MC-41256A8	30-Pin SIMM (Socket-Mountable) #3	B	12-27
MC-41256A9	30-Pin SIMM (Socket-Mountable) #6	B	12-28
MC-421000A36	72-Pin SIMM (Socket-Mountable) #3	B	12-42
MC-421000A8	30-Pin SIMM (Leaded) #1	A	12-24
	30-Pin SIMM (Socket-Mountable) #1	B	12-26
MC-421000A9	30-Pin SIMM (Leaded) #3	A	12-25
	30-Pin SIMM (Socket-Mountable) #2	B	12-27
MC-422000A36	72-Pin SIMM (Socket-Mountable) #2	BH/FH	12-41
MC-424100A8	30-Pin SIMM (Leaded) #4	A	12-26
	30-Pin SIMM (Socket-Mountable) #5	B	12-28
MC-424100A9	30-Pin SIMM (Leaded) #2	A	12-25
	30-Pin SIMM (Socket-Mountable) #4	B	12-28
MC-424256A36	72-Pin SIMM (Socket-Mountable) #4	B/F	12-43
MC-424256A36BH/FH	72-Pin SIMM (Socket-Mountable) #5	BH/FH	12-44
MC-424512A36	72-Pin SIMM (Socket-Mountable) #6	B/F	12-45
MC-424512A36BH/FH	72-Pin SIMM (Socket-Mountable) #1	BH/FH	12-40
μPB100422	24-Pin Ceramic Flatpack	B	12-12
	24-Pin Ceramic DIP	D	12-15
μPB100470	18-Pin Cerdip	D	12-7
μPB100474	24-Pin Ceramic Flatpack	B	12-12
	24-Pin Ceramic DIP	D	12-15
	24-Pin Ceramic LCC	K	12-17
μPB100474A	24-Pin Ceramic Flatpack	BH	12-12
	24-Pin Cerdip #2	D	12-16
μPB100474E	24-Pin Ceramic Flatpack	BH	12-12
	24-Pin Cerdip #2	D	12-16
μPB100480	20-Pin Ceramic Flatpack	B	12-8
	20-Pin Cerdip	D	12-9
μPB100484	28-Pin Ceramic Flatpack	B	12-20
	28-Pin Cerdip	D	12-22
μPB100484A	28-Pin Ceramic Flatpack	B	12-20
	28-Pin Cerdip	D	12-22
μPB100A484	28-Pin Ceramic Flatpack	B	12-20
	28-Pin Cerdip	D	12-22
μPB10422	24-Pin Ceramic DIP	D	12-15
μPB10470	18-Pin Cerdip	D	12-7
μPB10474	24-Pin Cerdip #2	D	12-16
μPB10474A	24-Pin Cerdip #2	D	12-16

Device/Package Cross Reference (cont)

Part Number	Package	Ordering Designation	Page
μPB10474E	24-Pin Cerdip #2	D	12-16
μPB10480	20-Pin Ceramic Flatpack	B	12-8
	20-Pin Cerdip	D	12-9
μPB10484	28-Pin Ceramic Flatpack	B	12-20
	28-Pin Cerdip	D	12-22
μPB10484A	28-Pin Ceramic Flatpack	B	12-20
	28-Pin Cerdip	D	12-22
μPB10A484	28-Pin Ceramic Flatpack	BH	12-20
	28-Pin Cerdip	D	12-22
μPD100500	24-Pin Cerdip #1	D	12-15
μPD100504	32-Pin Ceramic Flatpack	B	Not available at time of print
	32-Pin Cerdip	D	Not available at time of print
μPD10500	24-Pin Cerdip #1	D	12-15
μPD10504	32-Pin Ceramic Flatpack	B	Not available at time of print
	32-Pin Cerdip	D	Not available at time of print
μPD23C1000A	28-Pin Plastic DIP #2	C	12-21
	28-Pin Plastic Miniflat #1	G	12-22
μPD23C1000EA	32-Pin Plastic DIP	C	12-29
μPD23C1001E	32-Pin Plastic DIP	C	12-29
μPD23C1010A	28-Pin Plastic DIP #2	C	12-21
μPD23C1024E	40-Pin Plastic DIP	C	12-35
μPD23C16000	42-Pin Plastic DIP	CZ	12-36
μPD23C2000	40-Pin Plastic DIP	C	12-35
	52-Pin Plastic Miniflat	G	12-37
μPD23C2000A	40-Pin Plastic DIP	C	12-35
μPD23C2001	32-Pin Plastic DIP	C	12-29
μPD23C4000	40-Pin Plastic DIP	C	12-35
	64-Pin Plastic QFP	GF	12-39
μPD23C4000A	40-Pin Plastic DIP	C	12-35
μPD23C4001E	32-Pin Plastic DIP	C	12-29
	32-Pin Plastic Miniflat	GW	12-31
μPD23C8000	42-Pin Plastic DIP	CZ	12-36
μPD23C8001E	32-Pin Plastic DIP	CZ	12-29
	32-Pin Plastic Miniflat	GW	12-31
μPD27C1000A	32-Pin Cerdip #1	D	12-30
μPD27C1001A	32-Pin Cerdip #1	D	12-30
μPD27C1024A	40-Pin Cerdip	D	12-35
μPD27C2001	32-Pin Cerdip #2	D	12-30
μPD27C4001	32-Pin Cerdip #3	DZ	12-31
μPD27HC65	24-Pin Cerdip #3	DX	12-16

Device/Package Cross Reference (cont)

Part Number	Package	Ordering Designation	Page
μPD28C04	24-Pin Plastic DIP #3	C	12-14
	24-Pin Plastic Miniflat	G	12-17
μPD28C05	24-Pin Plastic DIP #3	C	12-14
	24-Pin Plastic Miniflat	G	12-17
μPD28C256	28-Pin Plastic DIP #2	CZ	12-21
μPD28C64	28-Pin Plastic DIP #2	C	12-21
μPD41256	16-Pin Plastic DIP	C	12-6
	18-Pin Plastic Leaded Chip Carrier	L	12-8
μPD41264	24-Pin Plastic DIP #2	C	12-13
	24-Pin Plastic ZIP	V	12-18
μPD41464	18-Pin Plastic DIP #1	C	12-6
	18-Pin Plastic Leaded Chip Carrier	L	12-8
μPD421000	18-Pin Plastic DIP #2	C	12-7
	26/20-Pin Plastic SOJ #1	LA	12-19
	20-Pin Plastic ZIP	V	12-10
μPD421001	18-Pin Plastic DIP #2	C	12-7
	26/20-Pin Plastic SOJ #1	LA	12-19
	20-Pin Plastic ZIP	V	12-10
μPD421002	18-Pin Plastic DIP #2	C	12-7
	26/20-Pin Plastic SOJ #1	LA	12-19
	20-Pin Plastic ZIP	V	12-10
μPD42101	24-Pin Plastic DIP #1	C	12-13
	24-Pin Plastic Miniflat	G	12-17
μPD42102	24-Pin Plastic DIP #1	C	12-13
	24-Pin Plastic Miniflat	G	12-17
μPD42264	24-Pin Plastic DIP #2	C	12-13
	24-pin Plastic SOJ	LA	12-18
	24-Pin Plastic ZIP	V	12-18
μPD42270	28-Pin Plastic DIP #1	C	12-20
μPD42273	28-Pin Plastic SOJ	LE	12-23
	28-Pin Plastic ZIP	V	12-24
μPD42274	28-Pin Plastic SOJ	LE	12-23
	28-Pin Plastic ZIP	V	12-24
μPD42275	40-Pin Plastic SOJ	LE	12-36
μPD424100	26/20-Pin Plastic SOJ #2	LB	12-19
	20-Pin Plastic ZIP	V	12-10
μPD424101	26/20-Pin Plastic SOJ #2	L	12-19
	20-Pin Plastic ZIP	V	12-10
μPD424102	26/20-Pin Plastic SOJ #2	LB	12-19
	20-Pin Plastic ZIP	V	12-10

Device/Package Cross Reference (cont)

Part Number	Package	Ordering Designation	Page
μPD424256	20-Pin Plastic DIP	C	12-9
	26/20-Pin Plastic SOJ #1	LA	12-19
	20-Pin Plastic ZIP	V	12-10
μPD424258	20-Pin Plastic DIP	C	12-9
	26/20-Pin Plastic SOJ #1	LA	12-19
	20-Pin Plastic ZIP	V	12-10
μPD424266	20-Pin Plastic DIP	C	12-9
	26/20-Pin Plastic SOJ #1	LA	12-19
	20-Pin Plastic ZIP	V	12-10
μPD424268	20-Pin Plastic DIP	C	12-9
	26/20-Pin Plastic SOJ #1	LA	12-19
	20-Pin Plastic ZIP	V	12-10
μPD424400	26/20-Pin Plastic SOJ #2	LB	12-19
	20-Pin Plastic ZIP	V	12-10
μPD424402	26/20-Pin Plastic SOJ #2	LB	12-19
	20-Pin Plastic ZIP	V	12-10
μPD424410	26/20-Pin Plastic SOJ #2	LB	12-19
	20-Pin Plastic ZIP	V	12-10
μPD424412	26/20-Pin Plastic SOJ #2	LB	12-19
	20-Pin Plastic ZIP	V	12-10
μPD424800	28-Pin Plastic SOJ	LE	12-23
	28-Pin Plastic ZIP	V	12-24
μPD42505	24-Pin Plastic DIP #1	C	12-13
	28-Pin Plastic ZIP	V	12-24
μPD42532	40-Pin Plastic DIP	C	12-35
μPD42601	26/20-Pin Plastic SOJ #1	LA	12-19
	20-Pin Plastic ZIP	V	12-10
μPD431000	32-Pin Plastic DIP	C	12-29
	32-Pin Plastic Miniflat	GW	12-31
μPD431000A	32-Pin Plastic DIP	CZ	12-29
	32-Pin Plastic Miniflat	GW	12-31
	32-Pin Plastic TSOP (Normal Leads) #2	GZ-KJH	12-32
	32-Pin Plastic TSOP (Reverse Leads) #2	GZ-KKH	12-34
μPD431001	28-Pin Plastic SOJ	LE	12-23
μPD431004	28-Pin Plastic SOJ	LE	12-23
μPD43251	24-Pin Plastic DIP #4	C	12-14
	24-Pin Plastic SOJ	LA	12-18
μPD43254	24-Pin Plastic DIP #4	C	12-14
	24-Pin Plastic SOJ	LA	12-18

Device/Package Cross Reference (cont)

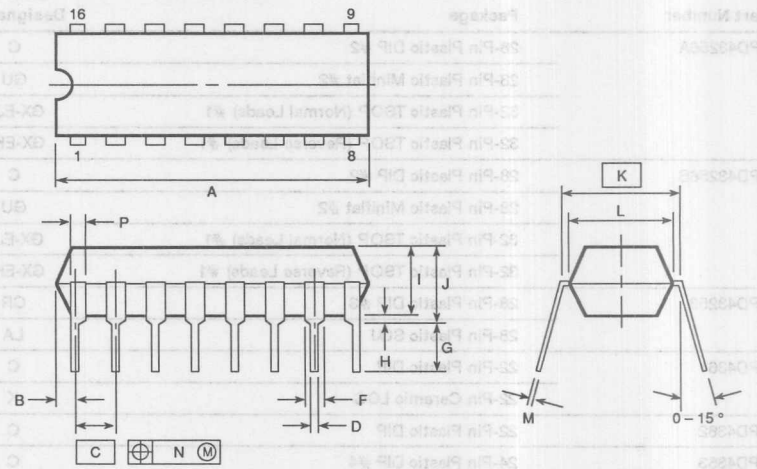
Part Number	Package	Ordering Designation	Page
μPD43256A	28-Pin Plastic DIP #2	C	12-21
	28-Pin Plastic Miniflat #2	GU	12-23
	32-Pin Plastic TSOP (Normal Leads) #1	GX-EJA	12-32
	32-Pin Plastic TSOP (Reverse Leads) #1	GX-EKA	12-33
μPD43256B	28-Pin Plastic DIP #2	C	12-21
	28-Pin Plastic Miniflat #2	GU	12-23
	32-Pin Plastic TSOP (Normal Leads) #1	GX-EJA	12-32
	32-Pin Plastic TSOP (Reverse Leads) #1	GX-EKA	12-33
μPD43258	28-Pin Plastic DIP #3	CR	12-21
	28-Pin Plastic SOJ	LA	Not available at time of print
μPD4361	22-Pin Plastic DIP	C	12-10
	22-Pin Ceramic LCC	K	12-11
μPD4362	22-Pin Plastic DIP	C	12-10
μPD4363	24-Pin Plastic DIP #4	C	12-14
μPD46251	24-Pin Plastic SOJ	LA	12-18

NEC

16-Pin Plastic DIP

Item	Millimeters	Inches
A	20.32 max	.800 max
B	1.27 max	.050 max
C	2.54 (TP)	.100 (TP)
D	0.50 ±0.10	.020 $^{+.004}_{-.005}$
F	1.2 min	.047 min
G	3.2 ±0.3	.126 ±.012
H	0.51 min	.020 min
I	4.31 max	.170 max
J	5.08 max	.200 max
K*	7.62 (TP)	.300 (TP)
L	6.7	.264
M	0.25 $^{+0.10}_{-0.05}$	.010 $^{+.004}_{-.003}$
N	0.25	.010
P	1.0 min	.039 min

* Item K to center of leads when formed parallel.



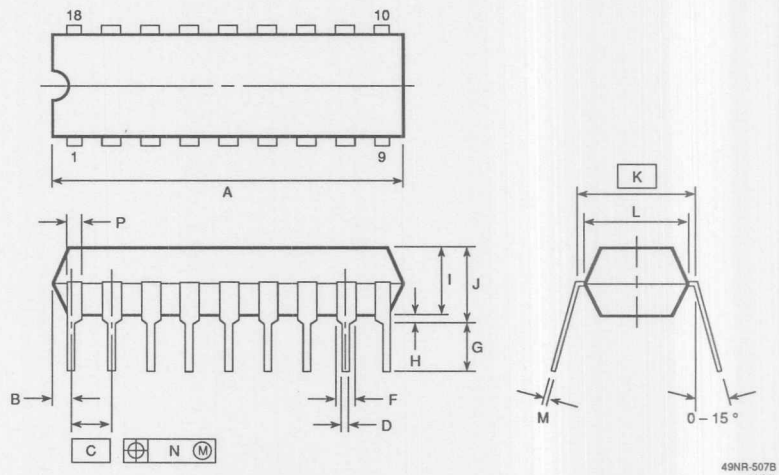
P16C-100-300SA

49NR-674B (2/90)

18-Pin Plastic DIP #1

Item	Millimeters	Inches
A	22.86 max	.900 max
B	1.27 max	.050 max
C	2.54 (TP)	.100 (TP)
D	0.50 ±0.10	.020 $^{+.004}_{-.005}$
F	1.2 min	.047 min
G	3.2 ±0.3	.126 ±.012
H	0.51 min	.020 min
I	4.31 max	.170 max
J	5.08 max	.200 max
K*	7.62 (TP)	.300 (TP)
L	6.7	.264
M	0.25 $^{+0.10}_{-0.05}$	.010 $^{+.004}_{-.003}$
N	0.25	.010
P	1.0 min	.039 min

* Item K to center of leads when formed parallel.



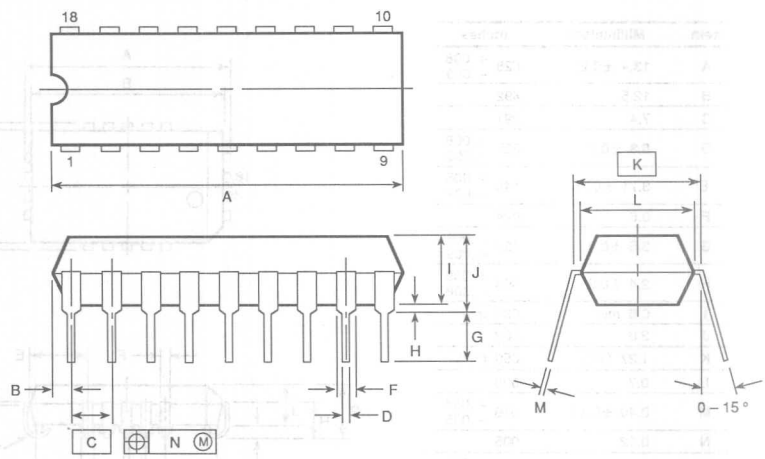
P18C-100-300SA

49NR-507B (4/89)

18-Pin Plastic DIP #2

Item	Millimeters	Inches
A	22.86 max	.900 max
B	1.27 max	.050 max
C	2.54 (TP)	.100 (TP)
D	0.50 ±0.10	.020 $^{+.004}_{-.005}$
F	1.2 min	.047 min
G	3.2 ±0.3	.126 ±.012
H	0.51 min	.020 min
I	4.31 max	.170 max
J	5.08 max	.200 max
K*	7.62 (TP)	.300 (TP)
L	7.35	.289
M	0.25 $^{+0.10}_{-0.05}$	.010 $^{+.004}_{-.003}$
N	0.25	.010

* Item K to center of leads when formed parallel.

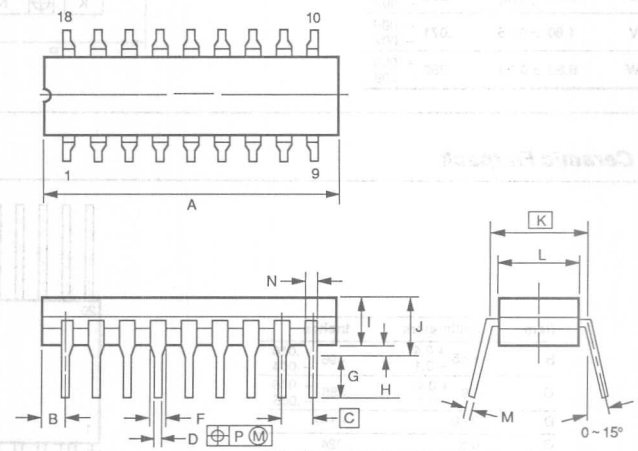


P18C-100-300WA

49NR-657B (1/90)

18-Pin Cerdip

Item	Millimeters	Inches
A	22.86 max	.900 max
B	1.27 max	.050 max
C	2.54 [TP]	.100[TP]
D	0.46 ± .05	.018 $^{+.003}_{-.002}$
F	1.42 min	.055 min
G	3.50 ±.30	.138 ±.012
H	0.51 min	.020 min
I	3.95	.156
J	5.08 max	.200 max
K	7.62 [TP]	.300 [TP]
L	6.60	.260
M	0.25 ±.05	.010 $^{+.002}_{-.003}$
N	0.89 min	.035 min
P	0.25	.010



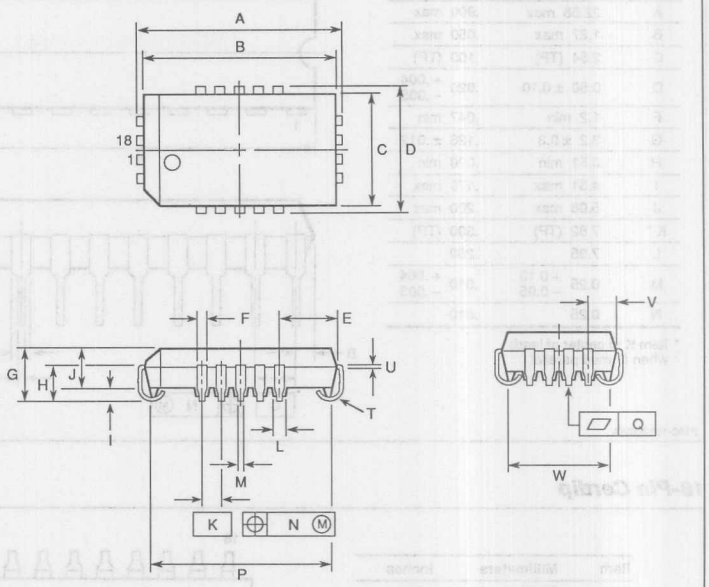
P18DH-100-300A

83H-6063B (6/89)

12

18-Pin Plastic Leaded Chip Carrier

Item	Millimeters	Inches
A	13.4 ±0.2	.528 $^{+.008}_{-.009}$
B	12.5	.492
C	7.4	.291
D	8.3 ±0.2	.327 $^{+.008}_{-.009}$
E	3.71 ±0.15	.146 $^{+.006}_{-.007}$
F	0.6	.024
G	3.5 ±0.2	.138 $^{+.008}_{-.009}$
H	2.4 ±0.2	.094 $^{+.009}_{-.008}$
I	0.8 min	.031 min
J	2.6	.102
K	1.27 (TP)	.050 (TP)
L	0.7	.028
M	0.40 ±0.10	.016 $^{+.004}_{-.005}$
N	0.12	.005
P	11.68 ±0.20	.460 $^{+.008}_{-.009}$
Q	0.15	.006
T	0.8 rad	.031 rad
U	0.20 $^{+0.10}_{-0.05}$	.008 $^{+.004}_{-.002}$
V	1.80 ±0.15	.071 $^{+.006}_{-.007}$
W	6.60 ±0.20	.260 $^{+.008}_{-.009}$

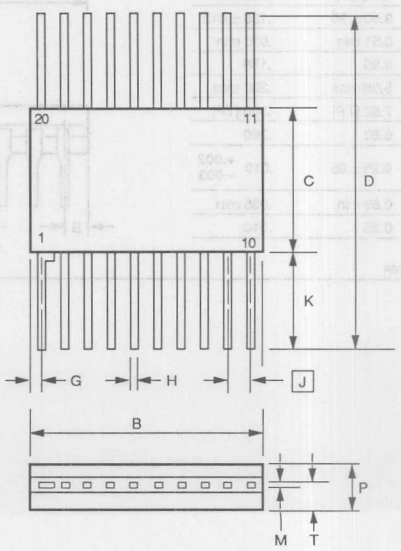


P18L-50A

49NR-675B (2/90)

20-Pin Ceramic Flatpack

Item	Millimeters	Inches
B	12.6 $^{+0.4}_{-0.1}$	.496 $^{+.016}_{-.004}$
C	9.8 $^{+0.4}_{-0.1}$	.388 $^{+.016}_{-.005}$
D	29.0	1.142
G	0.6	.024
H	0.43	.169
J	1.27	.050
K	9.6	.378
M	0.13	.005
P	2.18 max	.086 max
T	1.14 max	.045 max



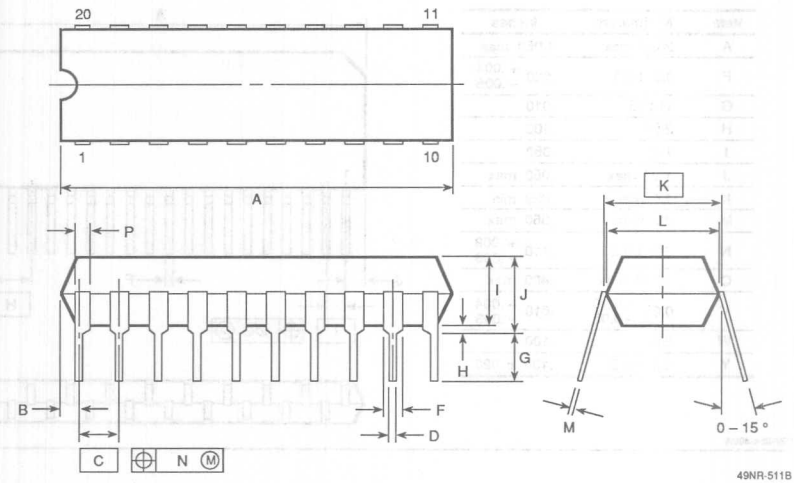
X20B-100A

83IH-5014B (7/89)

20-Pin Plastic DIP

Item	Millimeters	Inches
A	25.4 max	1.000 max
B	1.27 max	.050 max
C	2.54 (TP)	.100 (TP)
D	0.50 ± 0.10	.020 $^{+.004}_{-.005}$
F	1.2 min	.047 min
G	3.2 ± 0.3	.126 ± .012
H	0.51 min	.020 min
I	4.31 max	.170 max
J	5.08 max	.200 max
K *	7.62 (TP)	.300 (TP)
L	7.35	.289
M	0.25 $^{+0.10}_{-0.05}$	.010 $^{+.004}_{-.003}$
N	0.25	.010
P	1.0 min	.039 min

* Item K to center of leads when formed parallel.

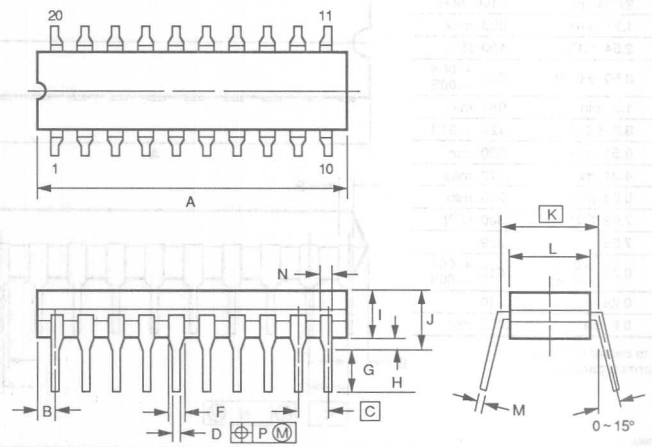


P20C-100-300WA

49NR-511B (5/89)

20-Pin Cerdip

Item	Millimeters	Inches
A	25.4 max	1.00 max
B	1.27 max	.050 max
C	2.54 [TP]	.100 [TP]
D	0.46 ± 0.05	.018 ± .002
F	1.42 min	.055 min
G	3.50 ± 0.30	.138 ± .012
H	0.51 min	.020 min
I	3.95	.156
J	5.08 max	.200 max
K	7.62 [TP]	.300 [TP]
L	7.32	.288
M	0.25 ± 0.05	.010 $^{+.002}_{-.003}$
N	0.89 min	.035 min
P	0.25	.010



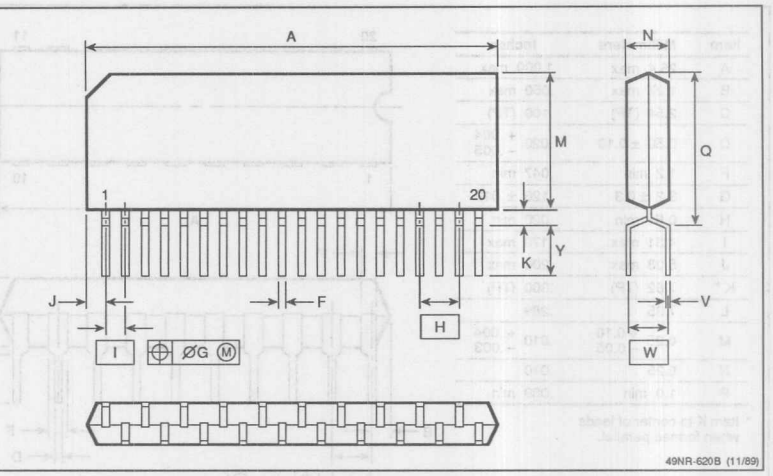
P20DH-100-300A

83H-6194B

12

20-Pin Plastic ZIP

Item	Millimeters	Inches
A	26.67 max	1.050 max
F	0.5 ±0.1	.020 $^{+.004}_{-.005}$
G	Ø0.25	.010
H	2.54	.100
I	1.27	.050
J	1.27 max	.050 max
K	1.0 min	.039 min
M	8.9 max	.350 max
N	2.8 ±0.2	.110 $^{+.009}_{-.008}$
Q	10.16 max	.400 max
V	0.25 $^{+0.10}_{-0.05}$	.010 $^{+.004}_{-.003}$
W	2.54	.100
Y	3.3 ±0.5	.130 ±.020



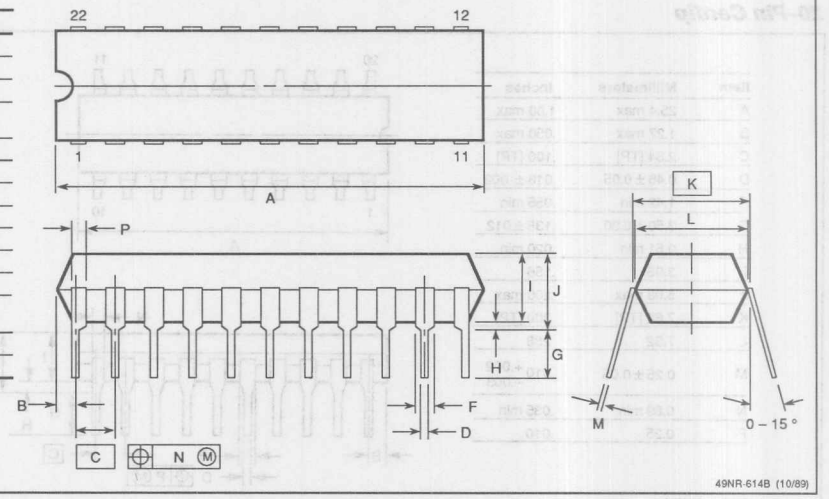
P20V-254-400A

49NR-620B (11/89)

22-Pin Plastic DIP

Item	Millimeters	Inches
A	27.94 max	1.100 max
B	1.27 max	.050 max
C	2.54 (TP)	.100 (TP)
D	0.50 ±0.10	.020 $^{+.004}_{-.005}$
F	1.2 min	.047 min
G	3.2 ±0.3	.126 ±.012
H	0.51 min	.020 min
I	4.31 max	.170 max
J	5.08 max	.200 max
K *	7.62 (TP)	.300 (TP)
L	7.35	.289
M	0.25 $^{+0.10}_{-0.05}$	.010 $^{+.004}_{-.003}$
N	0.25	.010
P	0.9 min	.035 min

* Item K to center of leads when formed parallel.

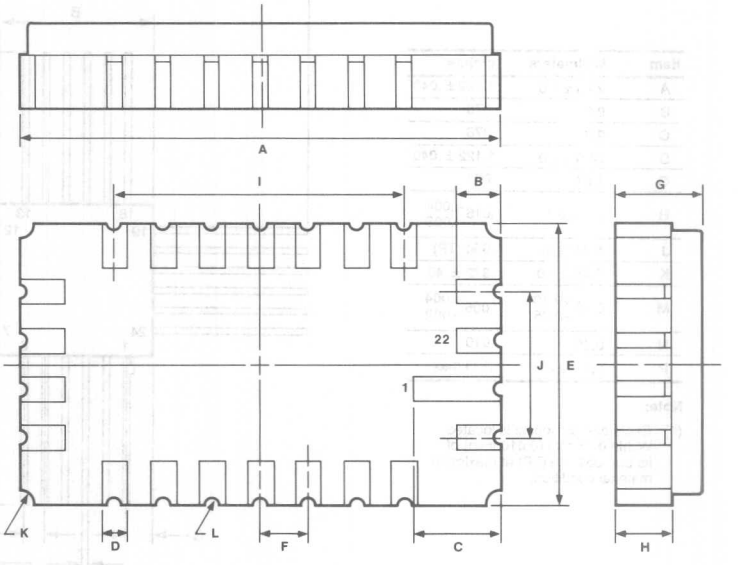


P22C-100-300WA

49NR-614B (10/89)

22-Pin Ceramic LCC

Item	Millimeters	Inches
A	12.45 ± .35	.490 ± .014
B	1.14	.045
C	2.29	.090
D	.64	.025
E	7.37 ± .35	.290 ± .014
F	1.27	.050
G	2.26 max	.089 max
H	1.40	.055
I	7.62	.300
J	3.81	.150
K	.3 rad	.012 rad
L	.2 rad	.008 rad



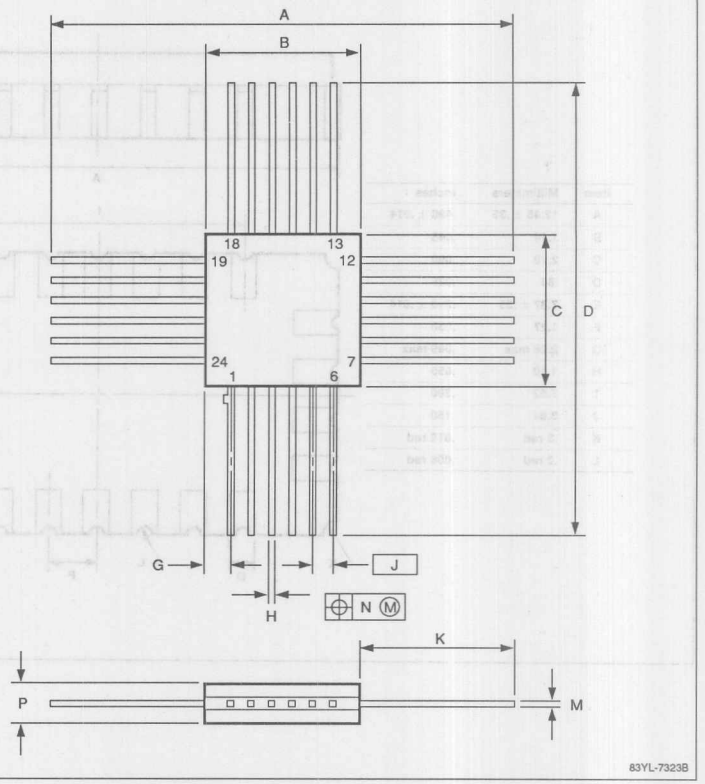
83-003578B

24-Pin Ceramic Flatpack

Item	Millimeters	Inches
A	28.5 ± 1.0	1.122 ± .040
B	9.6	.378
C	9.6	.378
D	28.5 ± 1.0	1.122 ± .040
G	1.62	.064
H	0.4 ± 0.1	$.016^{+.004}_{-.005}$
J	1.27 (TP)	.050 (TP)
K	9.45 ± 1.0	.372 ± .40
M	$0.15^{+0.10}_{-0.05}$	$.006^{+.004}_{-.002}$
N	0.25	.010
P	2.6 max	.103 max

Note:

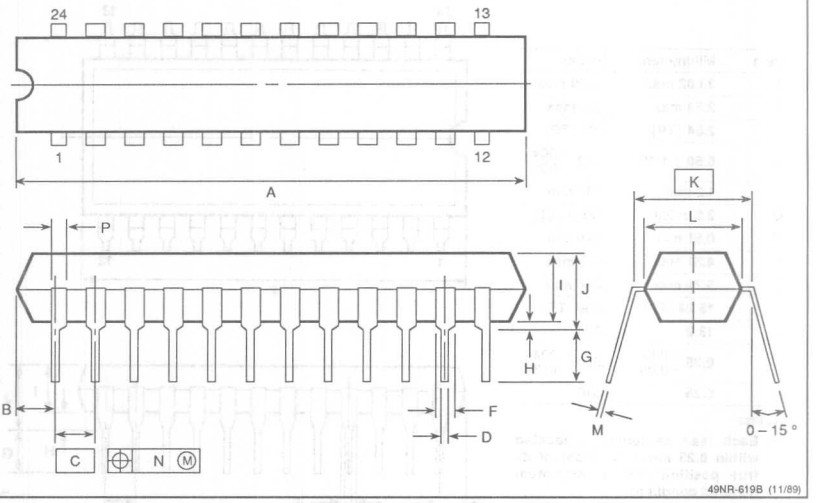
(1) Each lead centerline is located Within 0.25 mm (0.010 Inch) of its true position (TP) at maximum material condition.



24-Pin Plastic DIP #1

Item	Millimeters	Inches
A	33.02 max	1.300 max
B	2.54 max	.100 max
C	2.54 (TP)	.100 (TP)
D	0.50 ±0.10	.020 $^{+.004}_{-.005}$
F	1.2 min	.047 min
G	3.5 ±0.3	.138 ±.012
H	0.51 min	.020 min
I	4.31 max	.170 max
J	5.08 max	.200 max
K*	7.62 (TP)	.300 (TP)
L	6.4	.252
M	0.25 $^{+0.10}_{-0.05}$	.010 $^{+.004}_{-.003}$
N	0.25	.010
P	1.0 min	.039 min

* Item K to center of leads when formed parallel.



P24C-100-300A

49NR-619B (11/89)

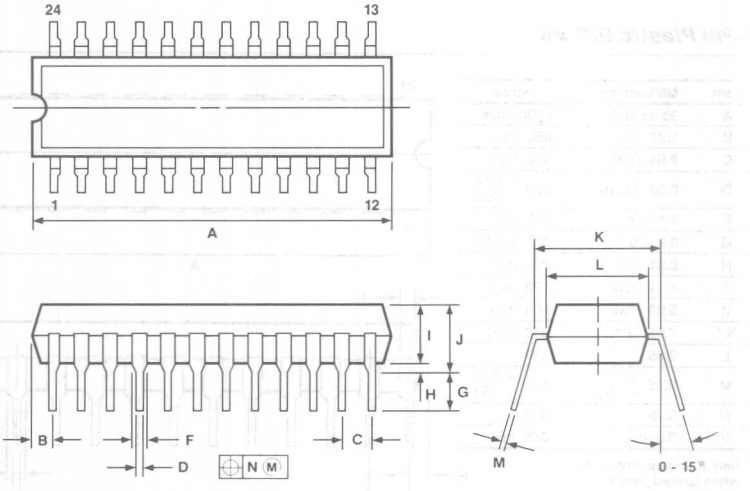
24-Pin Plastic DIP #2

Item	Millimeters	Inches
A	30.48 max	1.200 max
B	1.27 max	.050 max
C	2.54 [TP]	.100 [TP]
D	0.50 ± 0.10	.020 $^{+.004}_{-.005}$
F	1.2 min	.047 min
G	3.2 ± 0.3	.126 ± .012
H	0.51 min	.020 min
I	4.31 max	.170 max
J	5.08 max	.200 max
K	10.16 [TP]	.400 [TP]
L	8.6	.339
M	.25 $^{+0.10}_{-0.05}$	.010 $^{+.004}_{-.003}$
N	0.25	.010

Notes:

[1] Each lead centerline is located within 0.25 mm [.010 inch] of its true position [TP] at maximum material condition.

[2] Item "K" to center of leads when formed parallel.



P24C-100-400A1

83-003627B

12

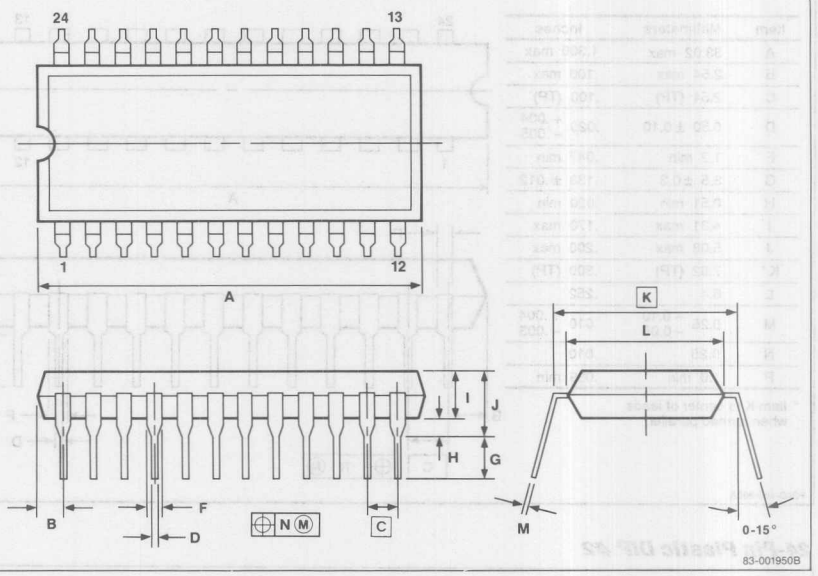
24-Pin Plastic DIP #3

Item	Millimeters	Inches
A	33.02 max	1.300 max
B	2.54 max	.100 max
C	2.54 [TP]	.100 [TP]
D	0.50 ± 0.10	.020 $^{+.004}_{-.005}$
F	1.2 min	.047 min
G	3.5 ± 0.3	.138 ± .012
H	0.51 min	.020 min
I	4.31 max	.170 max
J	5.72 max	.226 max
K	15.24 [TP]	.600 [TP]
L	13.2	.520
M	0.25 $^{+0.10}_{-0.05}$	.010 $^{+.004}_{-.003}$
N	0.25	.010

Notes:

[1] Each lead centerline is located within 0.25 mm [.010 inch] of its true position [TP] at maximum material condition.

[2] Item "K" to center of leads when formed parallel.



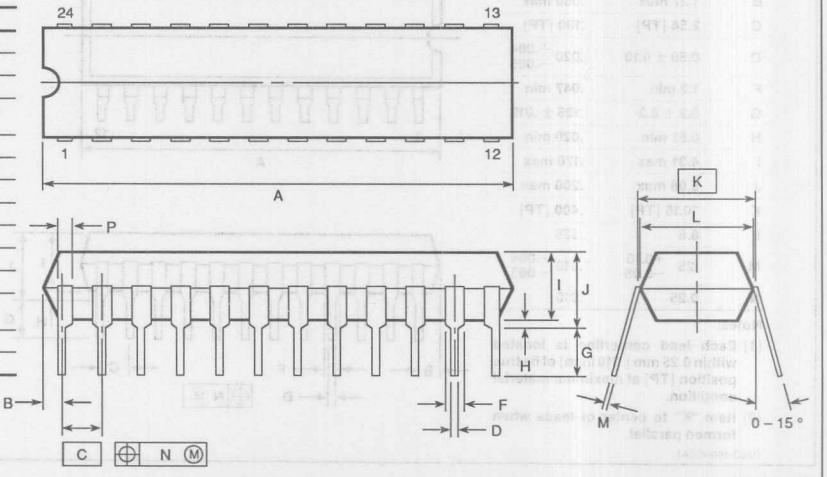
P24C-100-600

83-001950B

24-Pin Plastic DIP #4

Item	Millimeters	Inches
A	30.48 max	1.200 max
B	1.27 max	.050 max
C	2.54 (TP)	.100 (TP)
D	0.50 ±0.10	.020 $^{+.004}_{-.005}$
F	1.1 min	.043 min
G	3.2 ±0.3	.126 ±.012
H	0.51 min	.020 min
I	4.31 max	.170 max
J	5.08 max	.200 max
K *	7.62 (TP)	.300 (TP)
L	7.35	.289
M	0.25 $^{+0.10}_{-0.05}$	.010 $^{+.004}_{-.003}$
N	0.25	.010
P	0.9 min	.035 min

* Item K to center of leads when formed parallel.



P24C-100-300WA

49NR-590B (9/89)

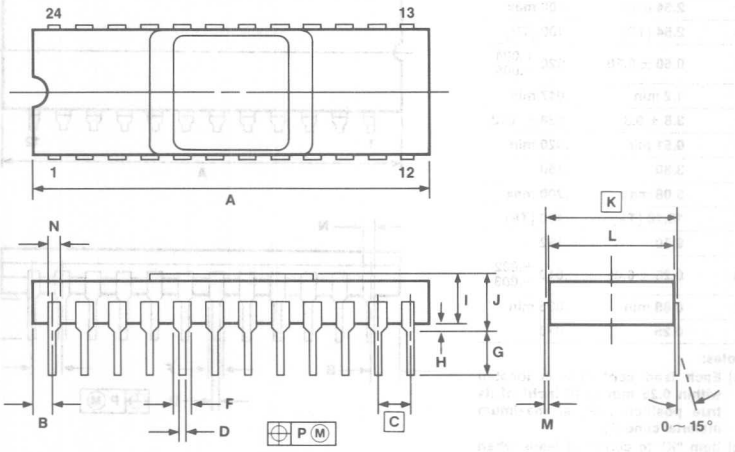
24-Pin Ceramic DIP

Item	Millimeters	Inches
A	33.02 max	1.30 max
B	2.54 max	.100 max
C	2.54 [TP]	.100 [TP]
D	0.46 ± 0.05	.018 ± .002
F	1.25 min	.049 min
G	3.50 ± 0.30	.138 ± .012
H	0.51 min	.020 min
I	2.74	.108
J	4.57 max	.180 max
K	10.16 [TP]	.400 [TP]
L	10.0	.394
M	0.25 ± 0.05	.010 $^{+.002}_{-.003}$
N	1.00 min	.039 min
P	0.25	.010

Notes:

[1] Each lead centerline is located within 0.25 mm [.010 inch] of its true position [TP] at maximum material condition.

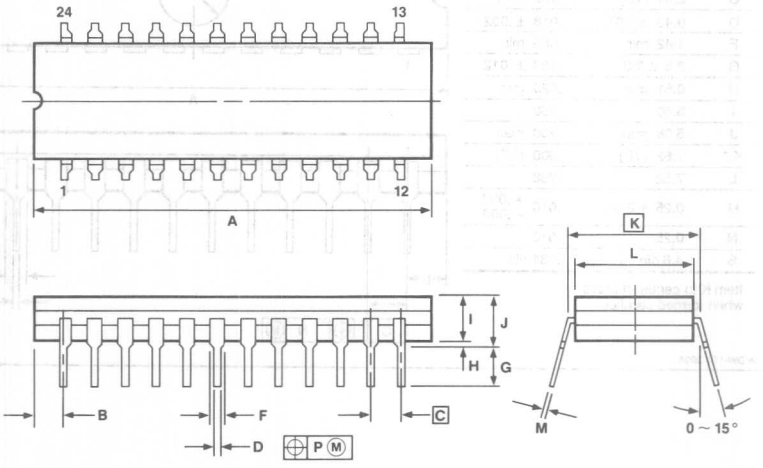
[2] Item "K" to center of leads when formed parallel.



83-003579B

24-Pin Cerdip #1

Item	Millimeters	Inches
A	33.02 max	1.300 max
B	2.54 max	.100 max
C	2.54 [TP]	.100 [TP]
D	0.46 ± 0.05	.018 ±.002
F	1.42 min	.055 min
G	3.5 ± 0.3	.138 ± .012
H	0.51 min	.020 min
I	3.80	.150
J	5.08 max	.200 max
K	7.62 [TP]	.300 [TP]
L	7.32	.288
M	0.25 ± 0.05	.010 $^{+.002}_{-.003}$
P	0.25	.010



P24DH-100-300A

83-006012B

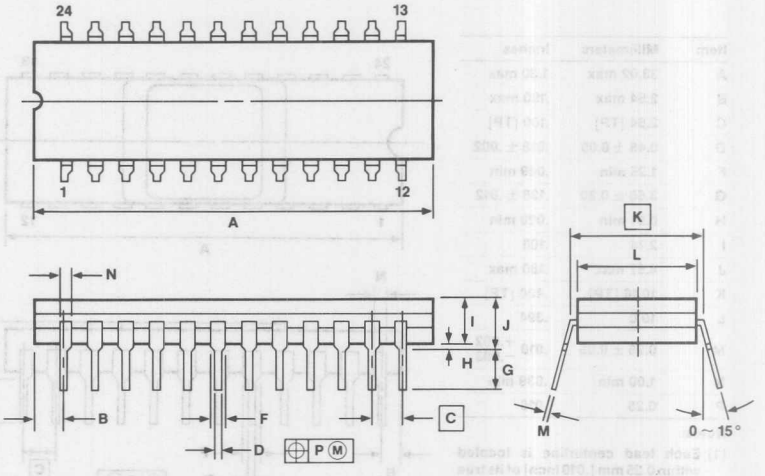
12

NEC

24-Pin Cerdip #2

Item	Millimeters	Inches
A	33.02 max	1.300 max
B	2.54 max	.100 max
C	2.54 [TP]	.100 [TP]
D	0.50 ± 0.10	.020 $^{+.004}_{-.005}$
F	1.2 min	.047 min
G	3.5 ± 0.3	.138 ± .012
H	0.51 min	.020 min
I	3.80	.150
J	5.08 max	.200 max
K	10.16 [TP]	.400 [TP]
L	9.70	.382
M	0.25 ± 0.05	.010 $^{+.002}_{-.003}$
N	0.89 min	.035 min
P	0.25	.010

Notes:
[1] Each lead centerline is located within 0.25 mm [.010 inch] of its true position [TP] at maximum material condition.
[2] Item "K" to center of leads when formed parallel.



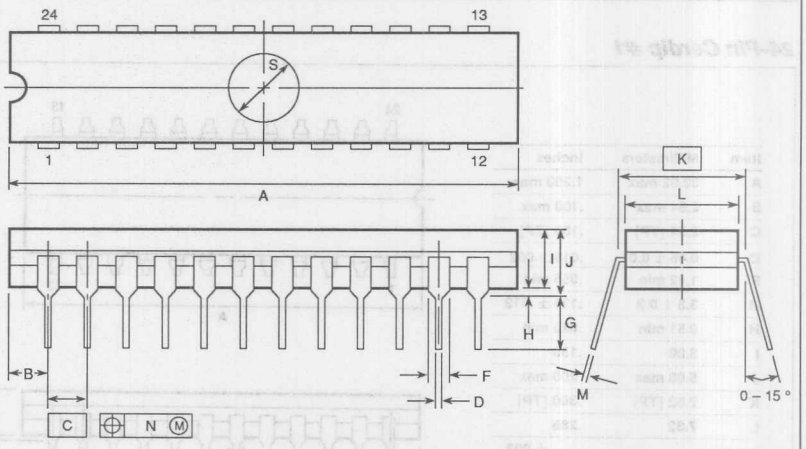
P24DH-100-400A

83-005012B

24-Pin Cerdip #3

Item	Millimeters	Inches
A	33.02 max	1.300 max
B	2.54 max	.100 max
C	2.54 (TP)	.100 (TP)
D	0.46 ±0.05	.018 ±.002
F	1.42 min	.055 min
G	3.5 ±0.3	.138 ±.012
H	0.51 min	.020 min
I	3.80	.150
J	5.08 max	.200 max
K *	7.62 (TP)	.300 (TP)
L	7.32	.288
M	0.25 ±0.05	.010 $^{+.002}_{-.003}$
N	0.25	.010
S	4.6 dia	.181 dia

* Item K to center of leads when formed parallel.

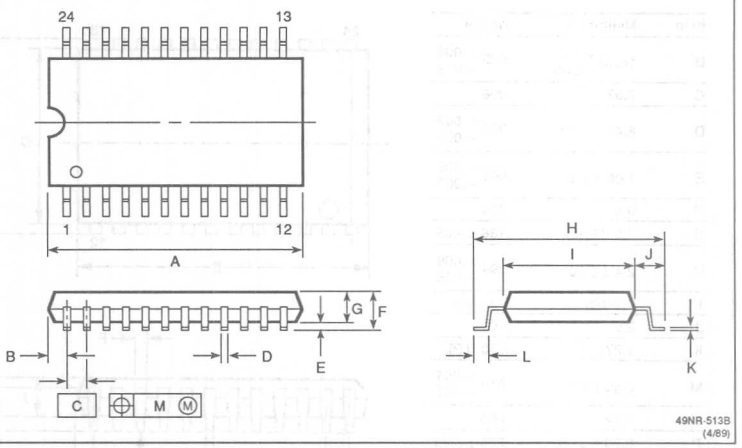


P24DW-100-300A

49NR-709B (3/90)

24-Pin Plastic Miniflat

Item	Millimeters	Inches
A	16.51 max	.650 max
B	1.27 max	.050 max
C	1.27 (TP)	.050 (TP)
D	0.40 ±0.10	.016 $^{+.004}_{-.005}$
E	0.1 $^{+0.2}_{-0.1}$	.004 $^{+.008}_{-.004}$
F	2.5 max	.099 max
G	2.00	.079
H	12.2 ±0.3	.480 $^{+.013}_{-.012}$
I	8.4	.331
J	1.9	.075
K	0.15 $^{+0.10}_{-0.05}$	.006 $^{+.004}_{-.002}$
L	0.9 ±0.2	.035 $^{+.009}_{-.008}$
M	0.12	.005

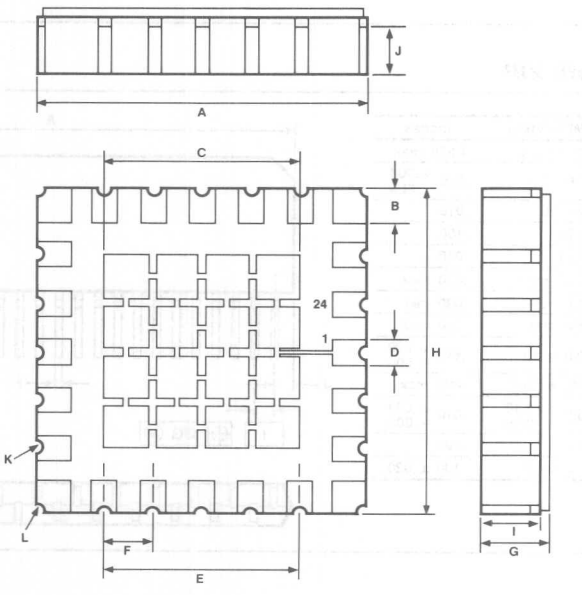


P24GM-50-450A

49NR-513B
(4/89)

24-Pin Ceramic LCC

Item	Millimeters	Inches
A	8.51 ±0.4	.335 ±.016
B	.89 ±0.2	.035 ±.008
C	5.14	.202
D	.64 ±0.1	.025 $^{+.005}_{-.004}$
E	5.08	.200
F	1.27	.050
G	2.0 max	.079 max
H	8.51 ±0.4	.335 ±.016
I	1.4	.055
J	1.02	.040
K	0.2R	.008R
L	0.3R	.012R

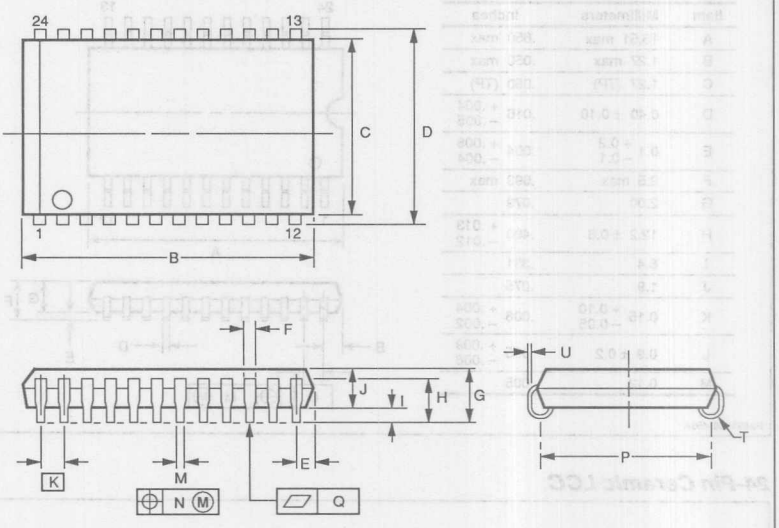


83-003582B

12

24-Pin Plastic SOJ

Item	Millimeters	Inches
B	$16.13^{+0.20}_{-0.35}$	$.635^{+.008}_{-.013}$
C	7.57	.298
D	8.47 ± 0.20	$.333^{+.009}_{-.008}$
E	1.08 ± 0.15	$.043^{+.006}_{-.007}$
F	0.6	.024
G	3.5 ± 0.20	.138 ± .008
H	2.4 ± 0.20	$.094^{+.009}_{-.008}$
I	0.8 min	.031 min
J	2.6	.102
K	1.27 [TP]	.050 [TP]
M	0.40 ± 0.10	$.016^{+.004}_{-.005}$
N	0.12	.005
P	6.73 ± 0.20	.265 ± .008
Q	0.15	.006
T	R 0.85	R .033
U	$0.20^{+0.10}_{-0.05}$	$.008^{+.004}_{-.002}$

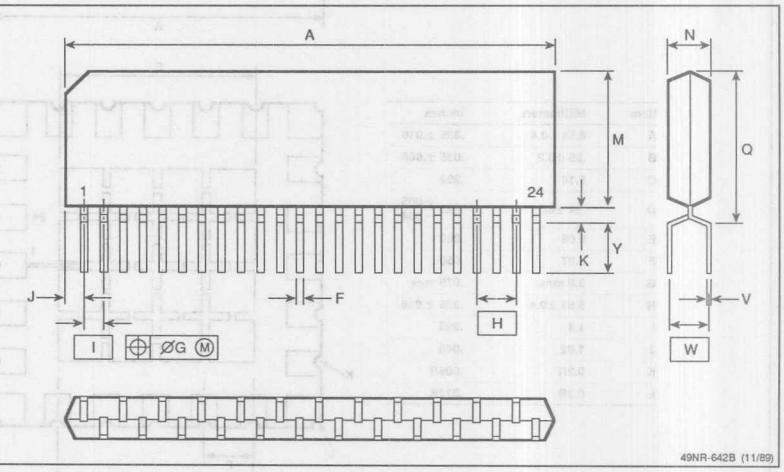


P24LA-50A

83IH-5851B

24-Pin Plastic ZIP

Item	Millimeters	Inches
A	31.75 max	1.250 max
F	0.5 ± 0.1	$.020^{+.004}_{-.005}$
G	Ø0.25	.010
H	2.54	.100
I	1.27	.050
J	1.27 max	.050 max
K	1.0 min	.039 min
M	8.9 max	.350 max
N	2.8 ± 0.2	$.110^{+.009}_{-.008}$
Q	10.16 max	.400 max
V	$0.25^{+0.10}_{-0.05}$	$.010^{+.004}_{-.003}$
W	2.54	.100
Y	3.3 ± 0.5	.130 ± .020



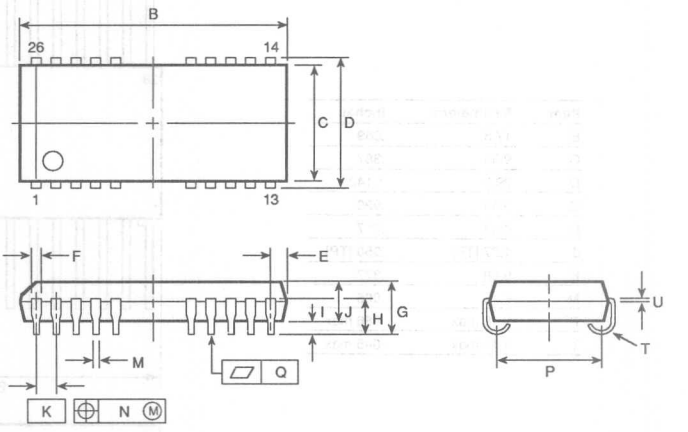
P24V-254-400A

49NR-642B (11/89)

26/20-Pin Plastic SOJ #1

Item	Millimeters	Inches
B	17.4 $^{+0.2}_{-0.35}$	.685 $^{+.008}_{-.013}$
C	7.57	.298
D	8.47 ±0.2	.333 $^{+.009}_{-.008}$
E	1.08 ±0.15	.043 $^{+.006}_{-.007}$
F	0.6	.024
G	3.5 ±0.2	.138 ±.008
H	2.4 ±0.2	.094 $^{+.009}_{-.008}$
I	0.8 min	.031 min
J	2.6	.102
K	1.27 (TP)	.050 (TP)
M	0.40 ±0.10	.016 $^{+.004}_{-.005}$
N	0.12	.005
P *	6.73 ±0.20	.265 ±.008
Q	0.15	.006
T	0.85 rad	.033 rad
U	0.20 $^{+0.10}_{-0.05}$	.008 $^{+.004}_{-.002}$

* Item P to center of leads.



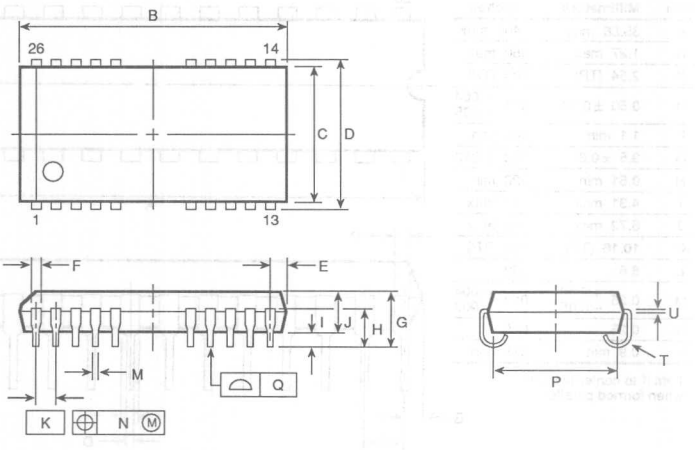
P26LA-50A

49NR-651B (12/89)

26/20-Pin Plastic SOJ #2

Item	Millimeters	Inches
B	17.4 $^{+0.2}_{-0.35}$	.685 $^{+.008}_{-.013}$
C	8.89	.350
D	9.78 ±0.2	.385 ±.008
E	1.08 ±0.15	.043 $^{+.006}_{-.007}$
F	0.6	.024
G	3.6 ±0.2	.142 $^{+.008}_{-.007}$
H	2.45 ±0.2	.096 $^{+.009}_{-.008}$
I	0.8 min	.031 min
J	2.7	.106
K	1.27 (TP)	.050 (TP)
M	0.40 ±0.10	.016 $^{+.004}_{-.005}$
N	0.12	.005
P *	8.06 ±0.20	.317 $^{+.008}_{-.007}$
Q	0.15	.006
T	0.85 rad	.033 rad
U	0.20 $^{+0.10}_{-0.05}$	.008 $^{+.004}_{-.002}$

* Item P to center of leads.

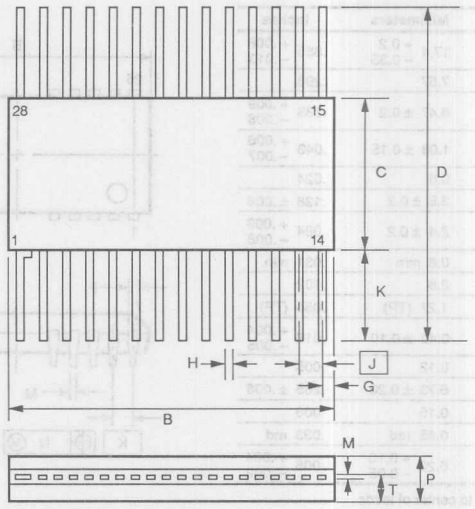


P26LB-350A

49NR-673B (2/90)

28-Pin Ceramic Flatpack

Item	Millimeters	Inches
B	17.5	.689
C	9.84	.387
D	29.0	1.142
G	0.50	.020
H	0.43	.017
J	1.27 [TP]	.050 [TP]
K	9.58	.377
M	0.15	.006
P	2.18 max	.086 max
T	1.14 max	.045 max



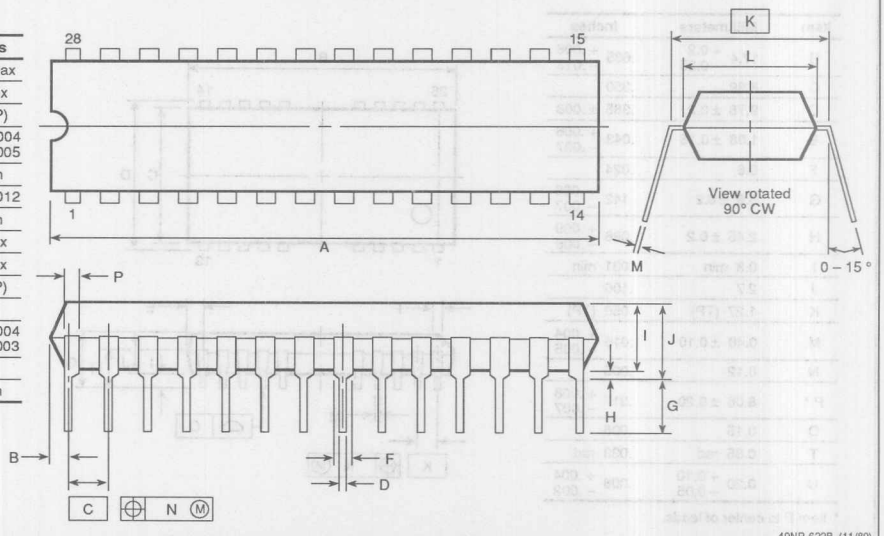
X28B-100A

83IH-4510B (5/89)

28-Pin Plastic DIP #1

Item	Millimeters	Inches
A	35.56 max	1.400 max
B	1.27 max	.050 max
C	2.54 (TP)	.100 (TP)
D	0.50 ±0.10	.020 $^{+.004}_{-.005}$
F	1.1 min	.043 min
G	3.5 ±0.3	.138 ±.012
H	0.51 min	.020 min
I	4.31 max	.170 max
J	5.72 max	.226 max
K *	10.16 (TP)	.400 (TP)
L	8.6	.339
M	0.25 $^{+0.10}_{-0.05}$	.010 $^{+.004}_{-.003}$
N	0.25	.010
P	0.9 min	.035 min

* Item K to center of leads when formed parallel.



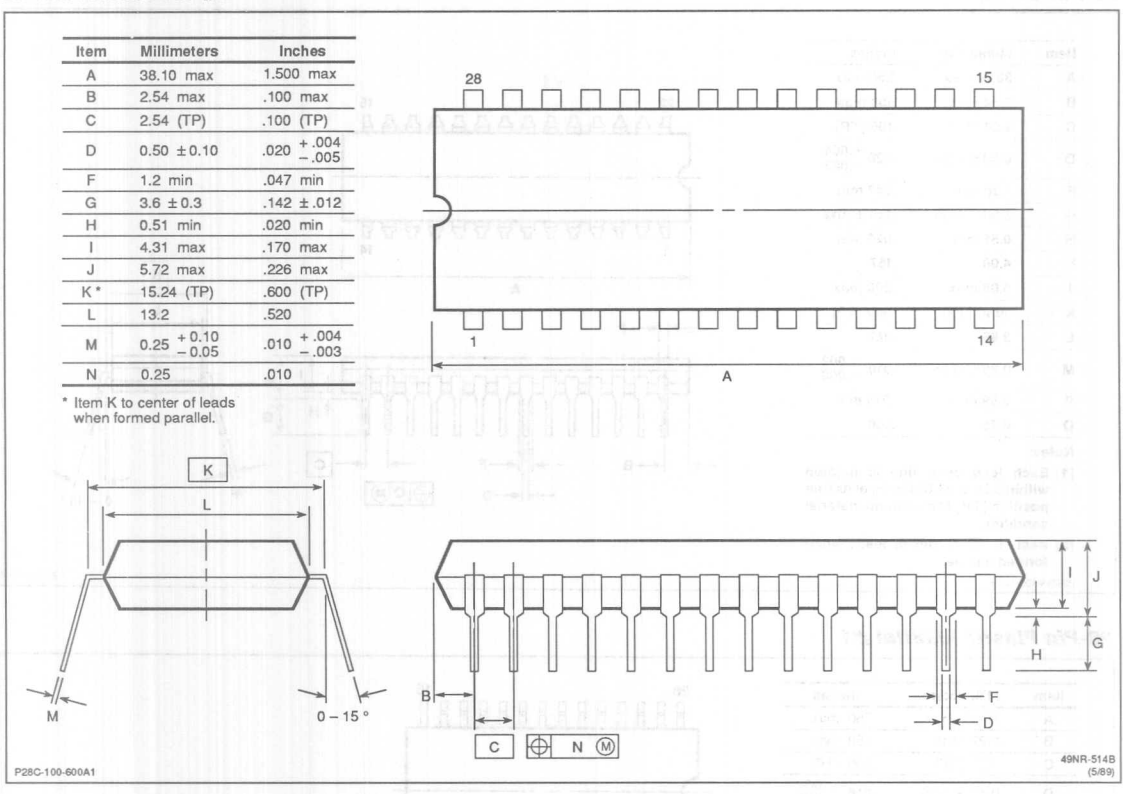
P28C-100-400

49NR-622B (11/89)

28-Pin Plastic DIP #2

Item	Millimeters	Inches
A	38.10 max	1.500 max
B	2.54 max	.100 max
C	2.54 (TP)	.100 (TP)
D	0.50 ±0.10	.020 $^{+.004}_{-.005}$
F	1.2 min	.047 min
G	3.6 ±0.3	.142 ±.012
H	0.51 min	.020 min
I	4.31 max	.170 max
J	5.72 max	.226 max
K *	15.24 (TP)	.600 (TP)
L	13.2	.520
M	0.25 $^{+0.10}_{-0.05}$	.010 $^{+.004}_{-.003}$
N	0.25	.010

* Item K to center of leads when formed parallel.



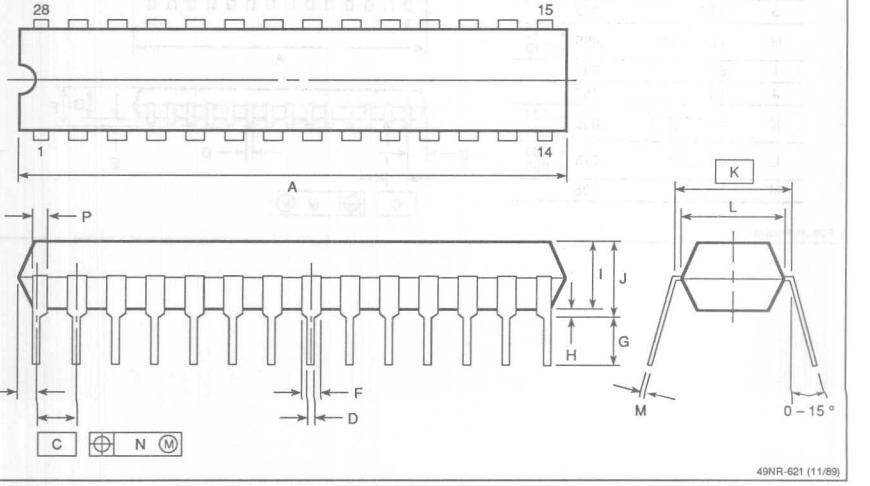
P28C-100-600A1

49NR-514B (5/89)

28-Pin Plastic DIP #3

Item	Millimeters	Inches
A	35.56 max	1.400 max
B	1.27 max	.050 max
C	2.54 (TP)	.100 (TP)
D	0.50 ±0.10	.020 $^{+.004}_{-.005}$
F	1.2 min	.047 min
G	3.2 ±0.3	.126 ±.012
H	0.51 min	.020 min
I	4.31 max	.170 max
J	5.08 max	.200 max
K *	7.62 (TP)	.300 (TP)
L	6.7	.264
M	0.25 $^{+0.10}_{-0.05}$	.010 $^{+.004}_{-.003}$
N	0.25	.010
P	1.0 min	.039 min

* Item K to center of leads when formed parallel.



P28C-100-300SA

49NR-621 (11/89)

12

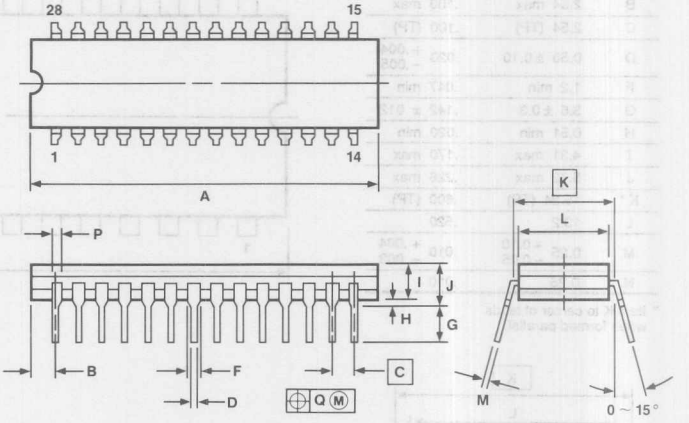
28-Pin Cerdip

Item	Millimeters	Inches
A	38.10 max	1.50 max
B	2.54 max	.100 max
C	2.54 [TP]	.100 [TP]
D	0.50 ± 0.10	.020 $^{+.004}_{-.005}$
F	1.20 min	.047 min
G	3.50 ± 0.30	.138 ± .012
H	0.51 min	.020 min
I	4.00	.157
J	5.08 max	.200 max
K	10.16 [TP]	.400 [TP]
L	9.65	.380
M	0.25 ± 0.05	.010 $^{+.002}_{-.003}$
P	0.89 min	.035 min
Q	0.25	.010

Notes:

[1] Each lead centerline is located within 0.25 mm [.010 inch] of its true position [TP] at maximum material condition.

[2] Item "K" to center of leads when formed parallel.

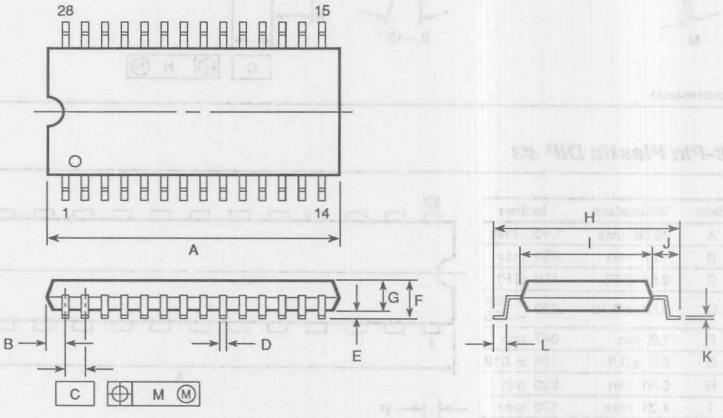


P28DH-100-400A

83-005015B

28-Pin Plastic Miniflat #1

Item	Millimeters	Inches
A	19.05 max	.750 max
B	1.27 max	.050 max
C	1.27 (TP)	.050 (TP)
D	0.40 ± 0.10	.016 $^{+.004}_{-.005}$
E	0.1 $^{+0.2}_{-0.1}$	.004 $^{+.008}_{-.004}$
F	2.5 max	.099 max
G	2.00	.079
H	11.8 ± 0.3	.465 $^{+.012}_{-.013}$
I	8.4	.331
J	1.7	.067
K	0.15 $^{+0.10}_{-0.05}$	.006 $^{+.004}_{-.002}$
L	0.7 ± 0.2	.028 $^{+.008}_{-.009}$
M	0.12	.005

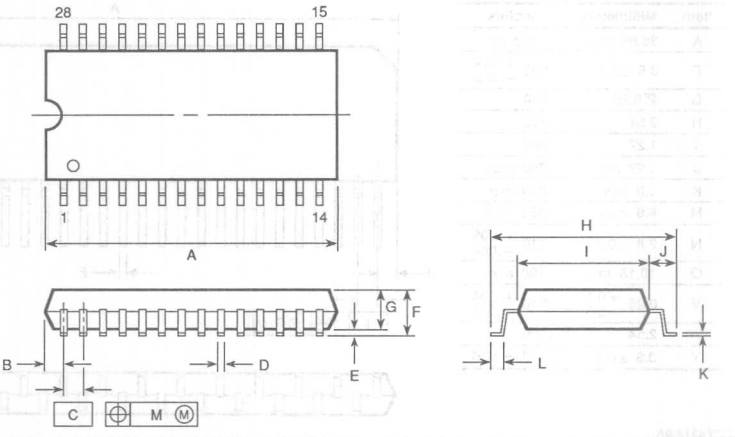


P28GM-50-450A1

49NR-623B (11/89)

28-Pin Plastic Miniflat #2

Item	Millimeters	Inches
A	19.05 max	.750 max
B	1.27 max	.050 max
C	1.27 (TP)	.050 (TP)
D	0.40 ±0.10	.016 $^{+.004}_{-.005}$
E	0.1 ±0.1	.004 $^{+.005}_{-.004}$
F	3.0 max	.119 max
G	2.55	.100
H	11.8 ±0.3	.465 $^{+.012}_{-.013}$
I	8.4	.331
J	1.7	.067
K	0.15 $^{+0.10}_{-0.05}$	.006 $^{+.004}_{-.002}$
L	0.7 ±0.2	.028 $^{+.008}_{-.009}$
M	0.12	.005



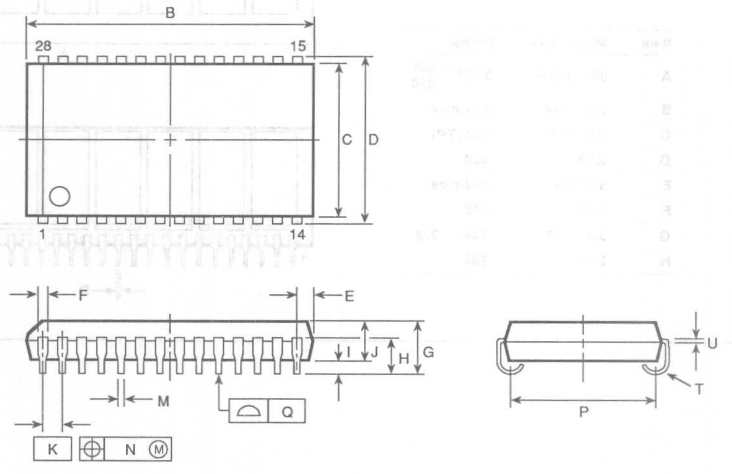
P28GM-50-450A2

49NR-635B (11/89)

28-Pin Plastic SOJ

Item	Millimeters	Inches
B	18.67 $^{+0.20}_{-0.35}$	.735 $^{+.008}_{-.013}$
C	10.16	.400
D	11.18 ±0.20	.440 $^{+.006}_{-.007}$
E	1.08 ±0.15	.043 $^{+.006}_{-.007}$
F	0.6	.024
G	3.5 ±0.2	.138 $^{+.006}_{-.007}$
H	2.4 ±0.2	.094 $^{+.006}_{-.007}$
I	0.8 min	.031 min
J	2.6	.102
K	1.27 (TP)	.050 (TP)
M	0.40 ±0.10	.016 $^{+.004}_{-.005}$
N	0.12	.005
P *	9.40 ±0.20	.370 $^{+.006}_{-.007}$
Q	0.15	.006
T	0.85 rad	.033 rad
U	0.20 $^{+0.10}_{-0.05}$	.008 $^{+.004}_{-.002}$

* Item P to center of leads.



P28LA-400A-1

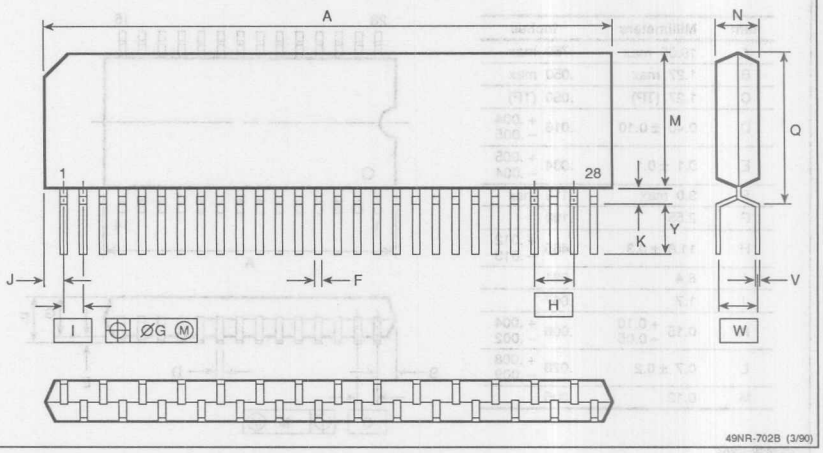
49NR-690B (2/90)

12

NEC

28-Pin Plastic ZIP

Item	Millimeters	Inches
A	36.83 max	1.450 max
F	0.5 ±0.1	.020 $^{+.004}_{-.005}$
G	Ø0.25	.010
H	2.54	.100
I	1.27	.050
J	1.27 max	.050 max
K	1.0 min	.039 min
M	8.9 max	.350 max
N	2.8 ±0.2	.110 $^{+.009}_{-.008}$
Q	10.16 max	.400 max
V	0.25 $^{+0.10}_{-0.05}$	.010 $^{+.004}_{-.003}$
W	2.54	.100
Y	3.3 ±0.5	.130 ±.020

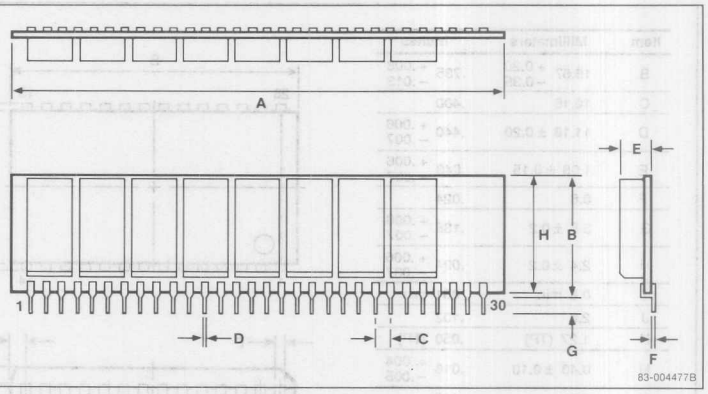


P28V-254-400A

49NR-702B (3/90)

30-Pin SIMM (Leaded) #1

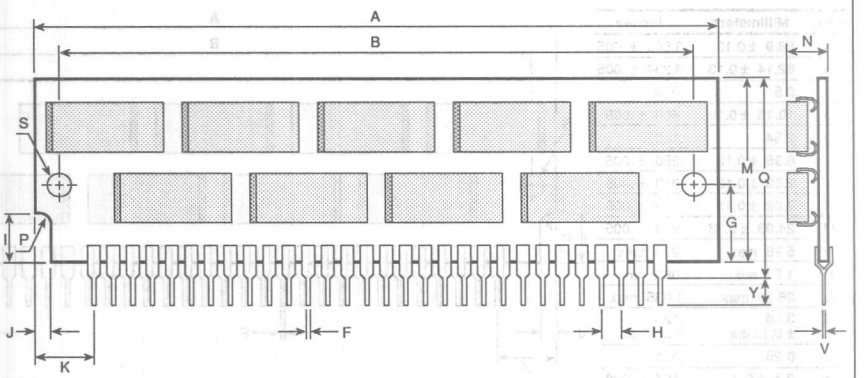
Item	Millimeters	Inches
A	80.3 ± 0.5	3.161 $^{+.021}_{-.020}$
B	21.6 max	.851 max
C	2.54 [TP]	.100 [TP]
D	0.50	.020
E	5.5 max	.217 max
F	0.25	.010
G	3.4 ± 0.7	.134 ± .028
H	20.0	.787



83-004477B

30-Pin SIMM (Leaded) #2

Item	Millimeters	Inches
A	88.9 ±0.13	3.500 ±.005
B	82.14 ±0.13	3.234 ±.005
F	0.5	.020
G	10.16 ±0.13	.400 ±.005
H	2.54	.100
I	6.35 ±0.13	.250 ±.005
J	2.03 ±0.13	.080 ±.005
K	7.62 ±0.13	.300 ±.005
M	24.03 ±0.13	.946 ±.005
N	5.28 max	.208 max
P	1.57 rad	.062 rad
Q	26.28 max	1.035 max
S	3.18 ±0.13 dia	.125 ±.005 dia
V	0.25	.010
Y	3.4 ±0.7	.134 ±.028

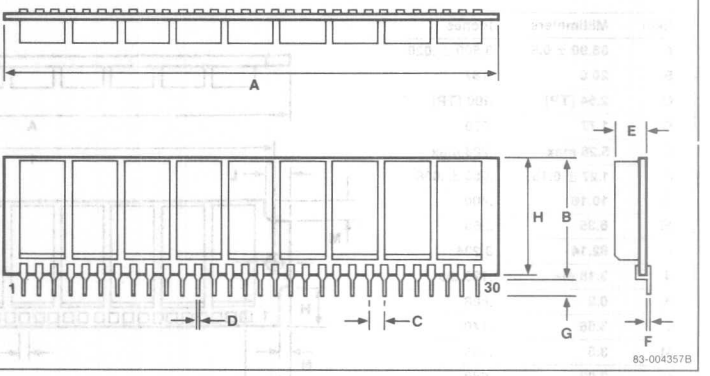


MC-424100A9A

49NR-707B (3/90)

30-Pin SIMM (Leaded) #3

Item	Millimeters	Inches
A	80.3 ± 0.5	3.161 $^{+.021}_{-.020}$
B	21.6 max	.851 max
C	2.54 [TP]	.100 [TP]
D	0.50	.020
E	5.5 max	.217 max
F	0.25	.010
G	3.4 ± 0.7	.134 ± .028
H	20.0	.787

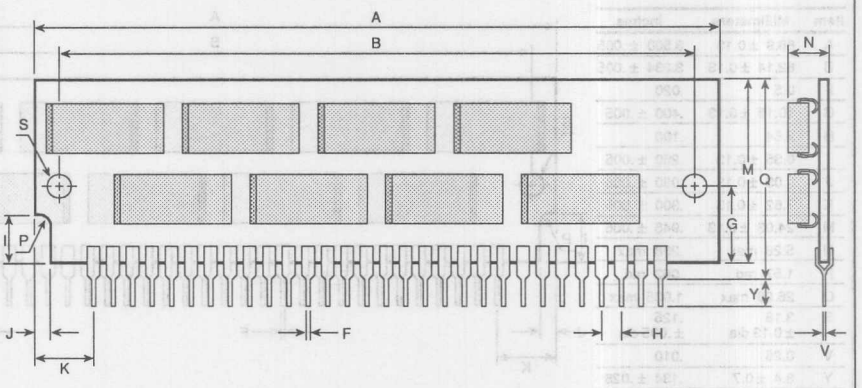


83-004357B

12

30-Pin SIMM (Leaded) #4

Item	Millimeters	Inches
A	88.9 ±0.13	3.500 ±.005
B	82.14 ±0.13	3.234 ±.005
F	0.5	.020
G	10.16 ±0.13	.400 ±.005
H	2.54	.100
I	6.35 ±0.13	.250 ±.005
J	2.03 ±0.13	.080 ±.005
K	7.62 ±0.13	.300 ±.005
M	24.03 ±0.13	.946 ±.005
N	5.28 max	.208 max
P	1.57 rad	.062 rad
Q	26.28 max	1.035 max
S	3.18 ±0.13 dia	.125 ±.005 dia
V	0.25	.001
Y	3.4 ±0.7	.134 ±.028

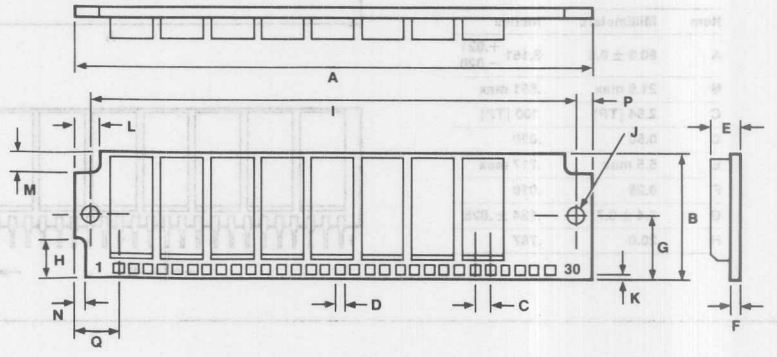


MC-424100A8A

49NR-703B (3/90)

30-Pin SIMM (Socket Mountable) #1

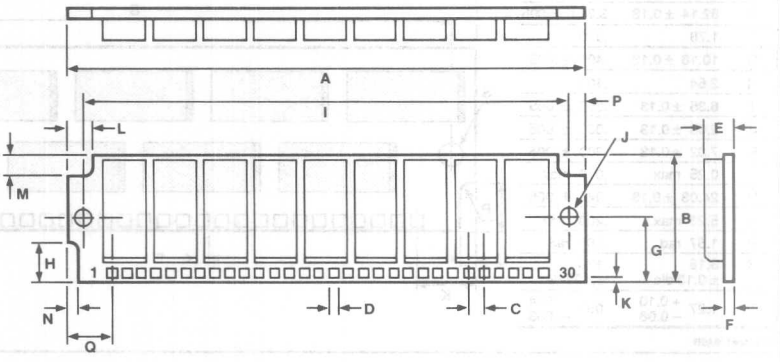
Item	Millimeters	Inches
A	88.90 ± 0.5	3.500 ± .020
B	20.0	.787
C	2.54 [TP]	.100 [TP]
D	1.77	.070
E	5.28 max	.208 max
F	1.27 ± 0.15	.050 ± .006
G	10.16	.400
H	6.35	.250
I	82.14	3.234
J	3.18 dia	.125 dia
K	0.2	.008
L	3.56	.140
M	3.5	.138
N	2.03	.080
P	3.38	.133
Q	7.62	.300



83-004478B

30-Pin SIMM (Socket Mountable) #2

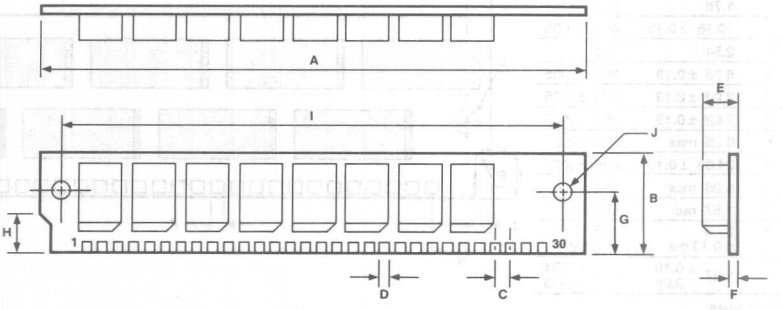
Item	Millimeters	Inches
A	88.90 ± 0.5	3.500 ± .020
B	20.0	.787
C	2.54 [TP]	.100 [TP]
D	1.77	.070
E	5.28 max	.208 max
F	1.27 ± 0.15	.050 ± .006
G	10.16	.400
H	6.35	.250
I	82.14	3.234
J	3.18 dia	.125 dia
K	0.2	.008
L	3.56	.140
M	3.5	.138
N	2.03	.080
P	3.38	.133
Q	7.62	.300



83-004358B

30-Pin SIMM (Socket Mountable) #3

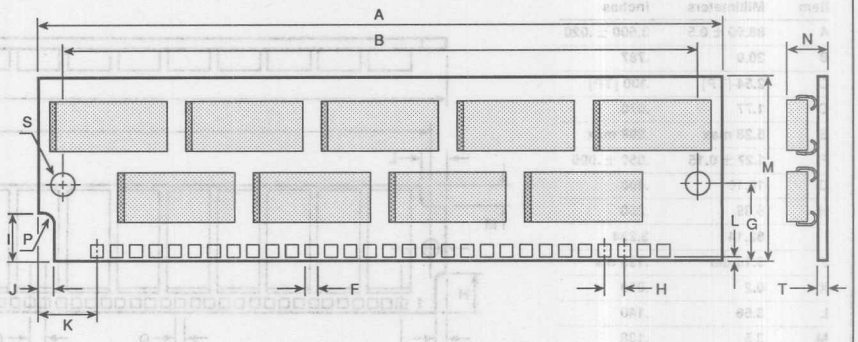
Item	Millimeters	Inches
A	88.90	3.500
B	16.80 max	.661 max
C	2.54	.100
D	1.78	.070
E	5.08 max	.200 max
F	1.27 ± .08	.050 ± .0032
G	10.16	.400
H	6.35	.250
I	82.10	3.232
J	3.175 dia	.125 dia



83-003210B

30-Pin SIMM (Socket Mountable) #4

Item	Millimeters	Inches
A	88.9 ±0.13	3.500 ±.005
B	82.14 ±0.13	3.234 ±.005
F	1.78	.070
G	10.16 ±0.13	.400 ±.005
H	2.54	.100
I	6.35 ±0.13	.250 ±.005
J	2.03 ±0.13	.080 ±.005
K	7.62 ±0.13	.300 ±.005
L	0.25 max	.010 max
M	24.03 ±0.13	.946 ±.005
N	5.28 max	.208 max
P	1.57 rad	.062 rad
S	3.18 ±0.13 dia	.125 ±.005 dia
T	1.27 $^{+0.10}_{-0.08}$	.050 $^{+.004}_{-.003}$

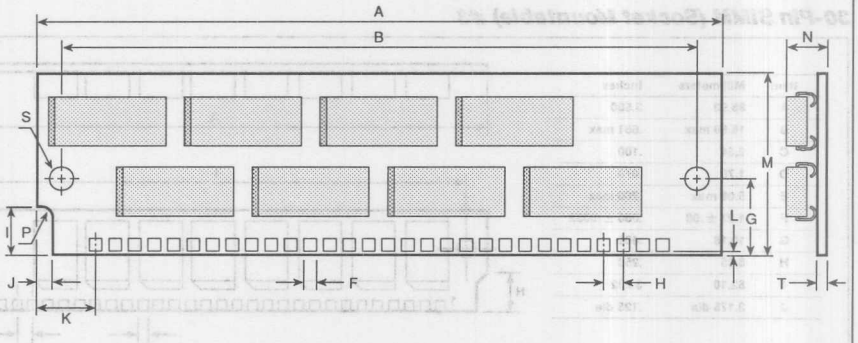


MC-424100A9B

49NR-708B (3/90)

30-Pin SIMM (Socket Mountable) #5

Item	Millimeters	Inches
A	88.9 ±0.13	3.500 ±.005
B	82.14 ±0.13	3.234 ±.005
F	1.78	.070
G	10.16 ±0.13	.400 ±.005
H	2.54	.100
I	6.35 ±0.13	.250 ±.005
J	2.03 ±0.13	.080 ±.005
K	7.62 ±0.13	.300 ±.005
L	0.25 max	.001 max
M	24.03 ±0.13	.946 ±.005
N	5.28 max	.208 max
P	1.57 rad	.062 rad
S	3.18 ±0.13 dia	.125 ±.005 dia
T	1.27 $^{+0.10}_{-0.08}$	.050 $^{+.004}_{-.003}$

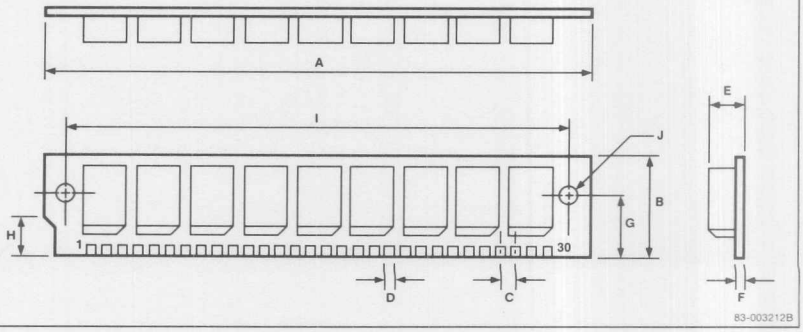


MC-424100A8B

49NR-705B (3/90)

30-Pin SIMM (Socket Mountable) #6

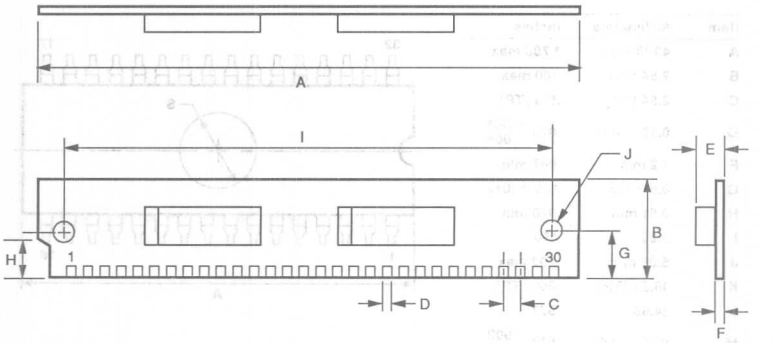
Item	Millimeters	Inches
A	88.90	3.500
B	16.80 max	.661 max
C	2.54	.100
D	1.78	.070
E	5.08 max	.200 max
F	1.27 ± .08	.050 ± .0032
G	10.16	.400
H	6.35	.250
I	82.10	3.232
J	3.175 dia	.125 dia



83-003212B

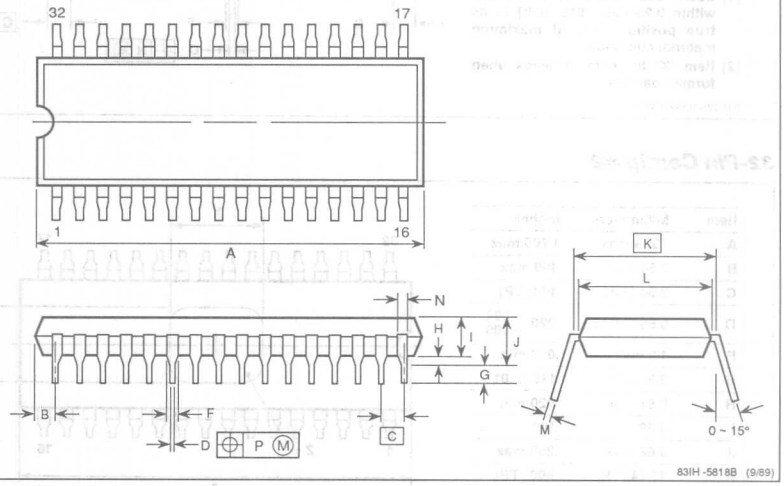
30-Pin SIMM (Socket Mountable) #7

Item	Millimeters	Inches
A	88.90	3.500
B	16.80 max	.661 max
C	2.54	.100
D	1.78	.070
E	5.08 max	.200 max
F	1.27 ±.08	.050 ±.0032
G	10.16	.400
H	6.35	.250
I	82.10	3.232
J	3.175 dia	.125 dia



32-Pin Plastic DIP

Item	Millimeters	Inches
A	40.64 max	1.60 max
B	1.27 max	.050 max
C	2.54 [TP]	.100 [TP]
D	0.50 ± 0.10	$.020^{+.004}_{-.005}$
F	1.1 min	.043 min
G	3.2 ± 0.30	.126 ± .012
H	0.51 min	.020 min
I	4.31 max	.170 max
J	5.08 max	.200 max
K	15.24 [TP]	.600 [TP]
L	13.2	.520
M	$0.25^{+0.10}_{-0.05}$	$.010^{+.004}_{-.003}$
N	0.9 min	.035 min
P	0.25	.010



12

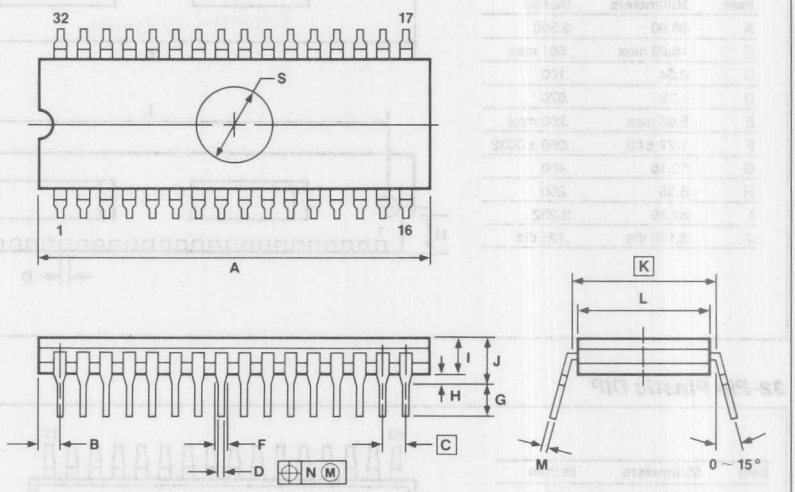
32-Pin Cerdip #1

Item	Millimeters	Inches
A	43.18 max	1.700 max
B	2.54 max	.100 max
C	2.54 [TP]	.100 [TP]
D	0.50 ± 0.10	.020 $^{+.004}_{-.005}$
F	1.2 min	.047 min
G	3.5 ± 0.3	.138 ± .012
H	0.51 min	.020 min
I	3.80	.150
J	5.08 max	.200 max
K	15.24 [TP]	.600 [TP]
L	14.66	.577
M	0.25 ± 0.05	.010 $^{+.002}_{-.003}$
N	0.25	.010
S	ϕ 9.66	ϕ .380

Notes:

[1] Each lead centerline is located within 0.25 mm [.010 inch] of its true position [TP] at maximum material condition.

[2] Item "K" to center of leads when formed parallel.



P32DW-100-600WA1

83-005013B

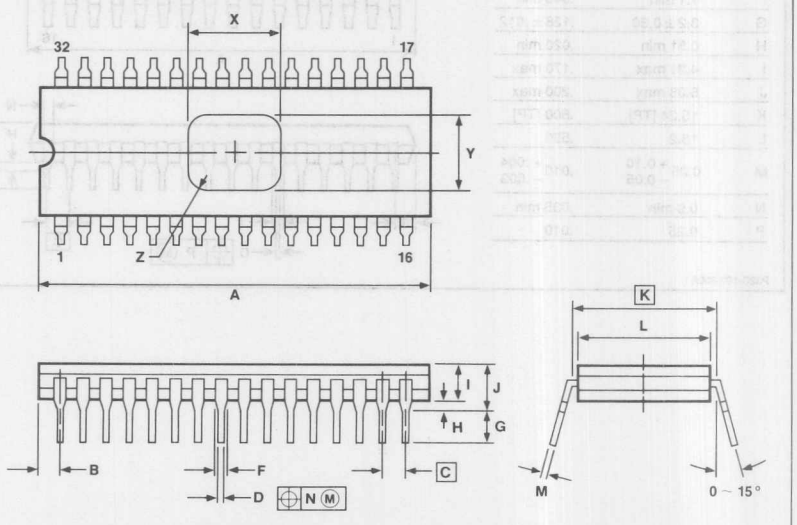
32-Pin Cerdip #2

Item	Millimeters	Inches
A	43.18 max	1.700 max
B	2.54 max	.100 max
C	2.54 [TP]	.100 [TP]
D	0.50 ± 0.10	.020 $^{+.004}_{-.005}$
F	1.2 min	.047 min
G	3.5 ± 0.3	.138 ± .012
H	0.51 min	.020 min
I	3.80	.150
J	5.08 max	.200 max
K	15.24 [TP]	.600 [TP]
L	14.66	.577
M	0.25 ± 0.05	.010 $^{+.002}_{-.003}$
N	0.25	.010
X	12.50	.492
Y	8.50	.335
Z	4-R2.0	4-R0.079

Notes:

[1] Each lead centerline is located within 0.25 mm [.01 inch] of its true position [TP] at maximum material condition.

[2] Item "K" to center of leads when formed parallel.



P32DW-100-600WA2-1

83-005105B

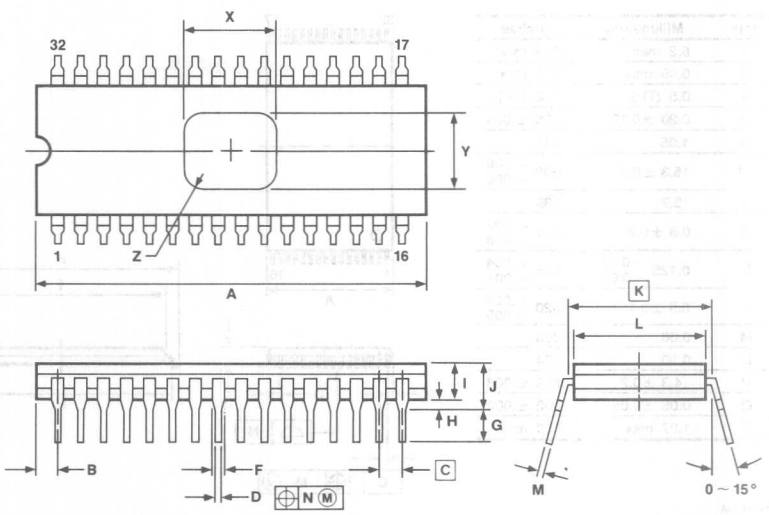
32-Pin Cerdip #3

Item	Millimeters	Inches
A	43.18 max	1.700 max
B	2.54 max	.100 max
C	2.54 [TP]	.100 [TP]
D	0.50 ± 0.10	.020 $^{+.004}_{-.005}$
F	1.2 min	.047 min
G	3.5 ± 0.3	.138 ± .012
H	0.51 min	.020 min
I	3.80	.150
J	5.08 max	.200 max
K	15.24 [TP]	.600 [TP]
L	14.66	.577
M	0.25 ± 0.05	.010 $^{+.002}_{-.003}$
N	0.25	.010
X	16.50	.650
Y	7.50	.295
Z	4-R2.0	4-R0.079

Notes:

[1] Each lead centerline is located within 0.25 mm [.01 inch] of its true position [TP] at maximum material condition.

[2] Item "K" to center of leads when formed parallel.

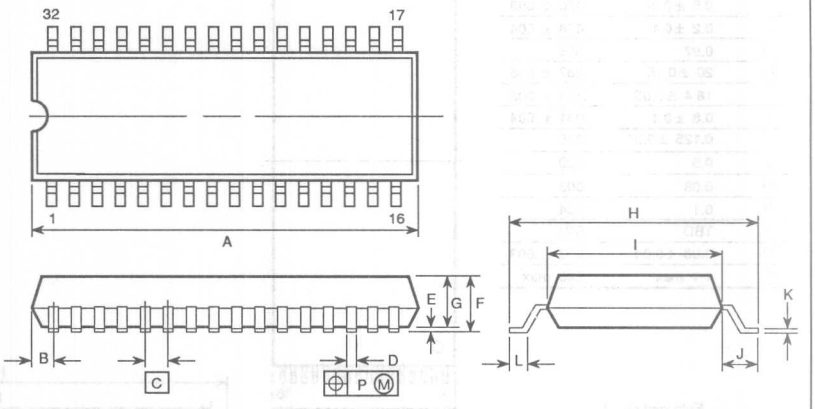


P32DW-100-600WA3-1

83-006189B

32-Pin Plastic Miniflat

Item	Millimeters	Inches
A	20.61 max	.812
B	0.78 max	.031 max
C	1.27 [TP]	.050 [TP]
D	0.40 $^{+0.10}_{-0.05}$	.016 $^{+.004}_{-.003}$
E	0.05 ±0.05	.002 ±.002
F	2.85 max	.113 max
G	2.70	.106
H	14.10 ±0.3	.555 ±.012
I	11.30	.445
J	1.40	.055
K	0.20 $^{+0.10}_{-0.05}$	.008 $^{+.004}_{-.002}$
L	0.80 ±0.20	.031 $^{+.009}_{-.008}$
P	0.12	.005



S32GM-50-525A-1

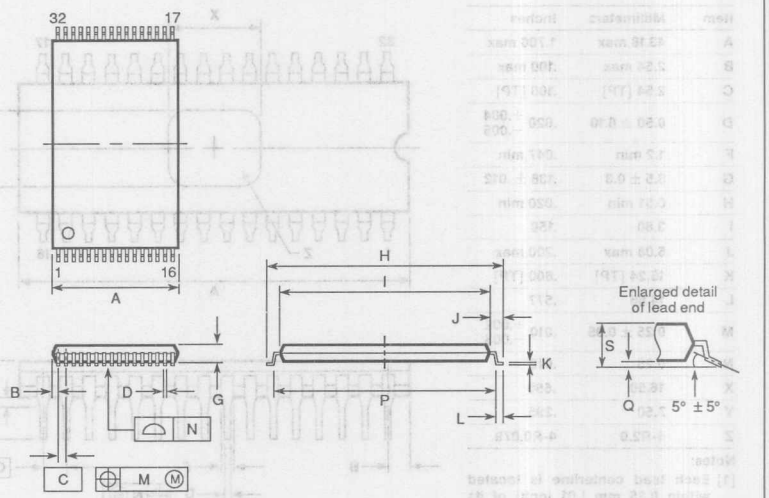
83IH-6227B (7/89)

12

NEC

32-Pin Plastic TSOP (Normal Leads) #1

Item	Millimeters	Inches
A	8.2 max	.323 max
B	0.45 max	.018 max
C	0.5 (TP)	.020 (TP)
D	0.20 ±0.10	.008 ±.004
G	1.05	.041
H	15.3 ±0.2	.602 $^{+.009}_{-.008}$
I	13.7	.539
J	0.8 ±0.2	.031 $^{+.009}_{-.008}$
K	0.125 $^{+0.10}_{-0.05}$	.005 $^{+.004}_{-.001}$
L	0.5 ±0.1	.020 $^{+.004}_{-.005}$
M	0.08	.003
N	0.10	.004
P	14.3 ±0.2	.563 ±.008
Q	0.05 ±0.05	.002 ±.002
S	1.27 max	.050 max

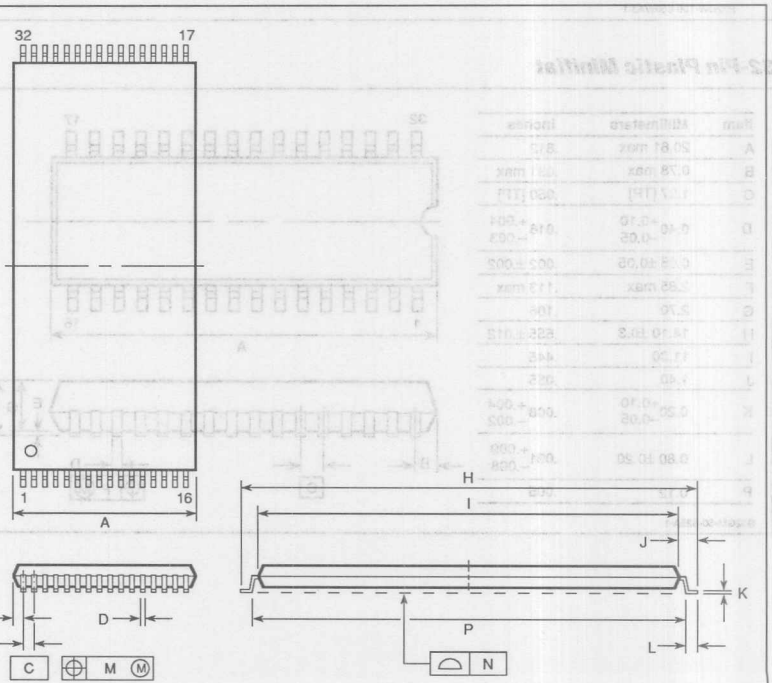


S32GX-50-EJA

49NR-601B (10/89)

32-Pin Plastic TSOP (Normal Leads) #2

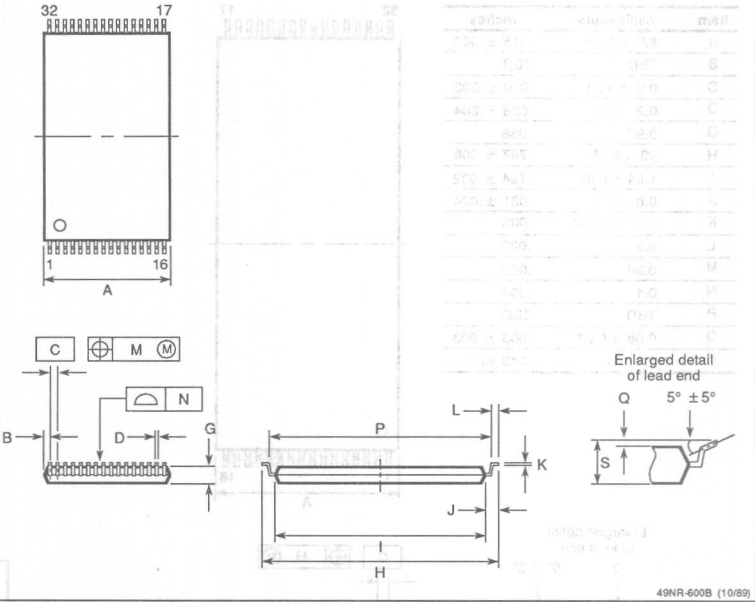
Item	Millimeters	Inches
A	8.0 ±0.05	.315 ±.002
B	TBD	TBD
C	0.5 ±0.08	.020 ±.003
D	0.2 ±0.1	.008 ±.004
G	0.97	.038
H	20 ±0.15	.787 ±.006
I	18.4 ±0.05	.724 ±.002
J	0.8 ±0.1	.031 ±.004
K	0.125 ±0.01	.005
L	0.5	.020
M	0.08	.003
N	0.1	.004
P	TBD	TBD
Q	0.08 ±0.08	.003 ±.003
S	1.1 max	.043 max



49NR-737B (5/90)

32-Pin Plastic TSOP (Reverse Bent Leads) #1

Item	Millimeters	Inches
A	8.2 max	.323 max
B	0.45 max	.018 max
C	0.5 (TP)	.020 (TP)
D	0.20 ±0.10	.008 ±.004
G	1.05	.041
H	15.3 ±0.2	.602 $^{+.009}_{-.008}$
I	13.7	.539
J	0.8 ±0.2	.031 $^{+.009}_{-.008}$
K	0.125 $^{+0.10}_{-0.05}$	.005 $^{+.004}_{-.001}$
L	0.5 ±0.1	.020 $^{+.004}_{-.005}$
M	0.08	.003
N	0.10	.004
P	14.3 ±0.2	.563 ±.008
Q	0.05 ±0.05	.002 ±.002
S	1.27 max	.050 max



S32GX-50-EKA

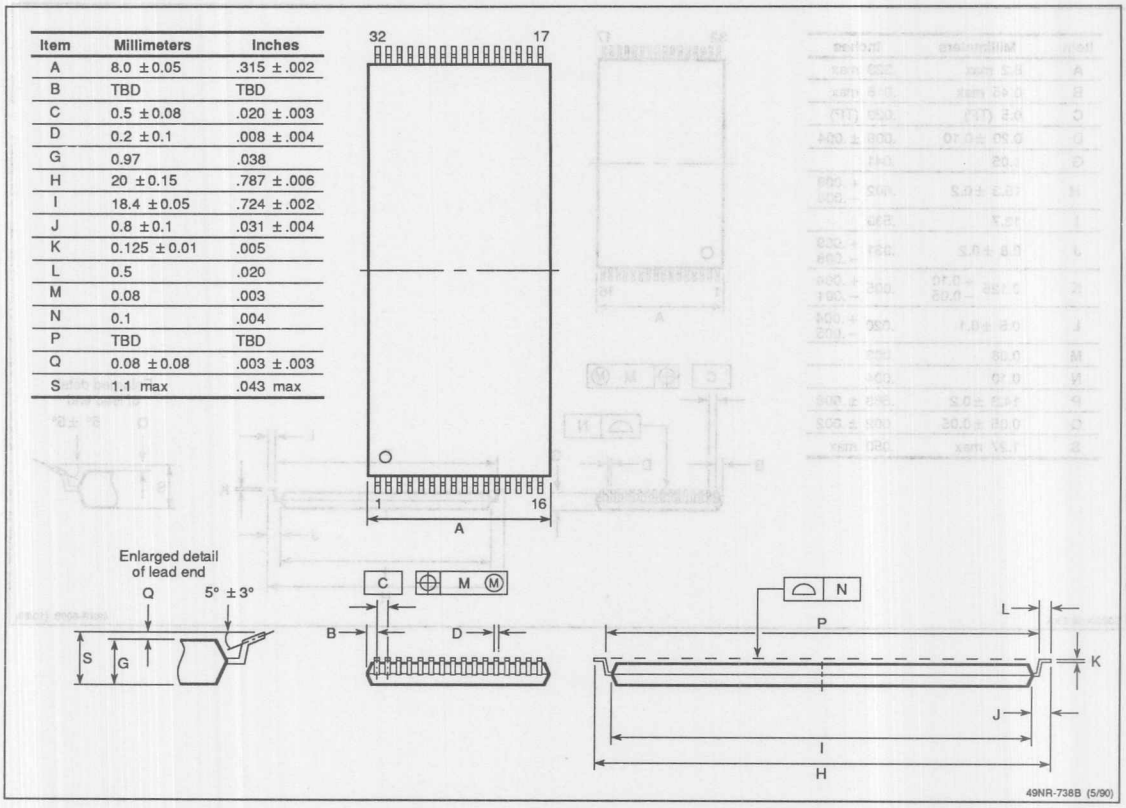
49NR-600B (10/89)

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NEC

32-Pin Plastic TSOP (Reverse Bent Leads) #2

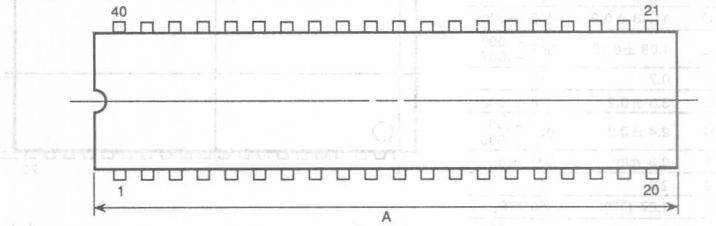
Item	Millimeters	Inches
A	8.0 ±0.05	.315 ±.002
B	TBD	TBD
C	0.5 ±0.08	.020 ±.003
D	0.2 ±0.1	.008 ±.004
G	0.97	.038
H	20 ±0.15	.787 ±.006
I	18.4 ±0.05	.724 ±.002
J	0.8 ±0.1	.031 ±.004
K	0.125 ±0.01	.005
L	0.5	.020
M	0.08	.003
N	0.1	.004
P	TBD	TBD
Q	0.08 ±0.08	.003 ±.003
S	1.1 max	.043 max

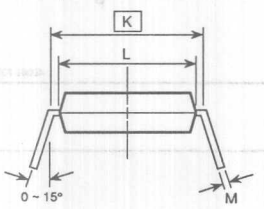


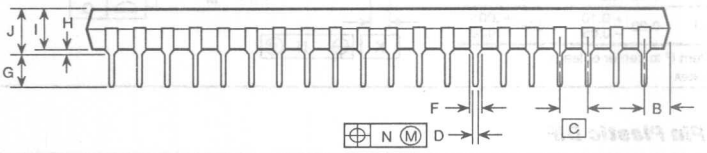
40-Pin Plastic DIP

Item	Millimeters	Inches
A	53.34 max	2.100 max
B	2.54 max	.100 max
C	2.54 (TP)	.100 (TP)
D	0.50 ±0.10	.020 $^{+.004}_{-.005}$
F	1.2 min	.047 min
G	3.6 ±0.3	.142 ±.012
H	0.51 min	.020 min
I	4.31 max	.170 max
J	5.72 max	.226 max
K*	15.24 (TP)	.600 (TP)
L	13.2	.520
M	0.25 $^{+0.10}_{-0.05}$	.010 $^{+.004}_{-.003}$
N	0.25	.010

* Item K to center of leads when formed parallel







P40C-100-600A

83vO-6140B (1/90)

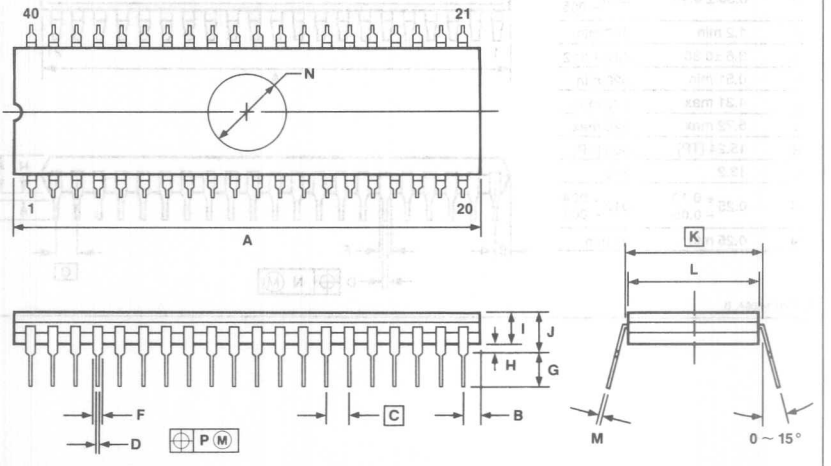
40-Pin Cerdip

Item	Millimeters	Inches
A	53.34 max	2.100 max
B	2.54 max	.100 max
C	2.54 [TP]	.100 [TP]
D	0.50 ± 0.10	.020 $^{+.004}_{-.005}$
F	1.2 min	.047 min
G	3.5 ± 0.3	.138 ± .012
H	0.51 min	.020 min
I	3.80	.150
J	5.08 max	.200 max
K	15.24 [TP]	.600 [TP]
L	14.66	.577
M	0.25 ± 0.05	.010 $^{+.002}_{-.003}$
N	8.89 dia	.350 dia
P	0.25	.010

Notes:

[1] Each lead centerline is located within 0.25 mm [.010 inch] of its true position [TP] at maximum material condition.

[2] Item "K" to center of leads when formed parallel.



P40DW-100-600WA

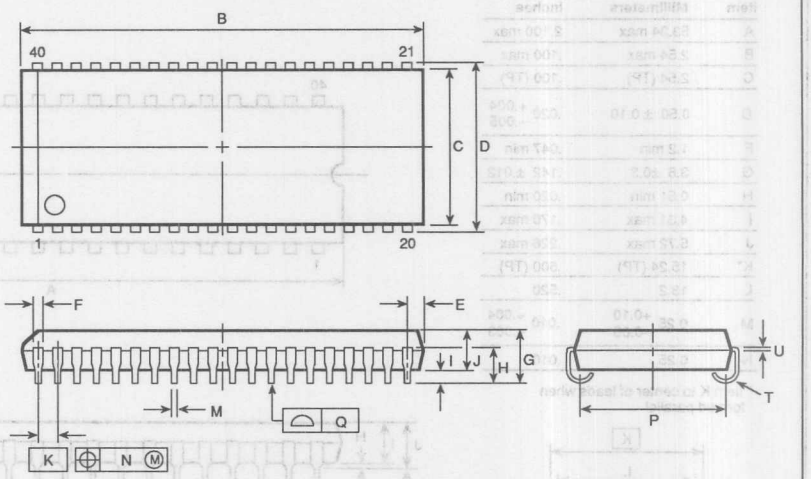
83-003631B

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40-Pin Plastic SOJ

Item	Millimeters	Inches
B	26.29 $^{+.02}_{-.035}$	1.035 $^{+.008}_{-.014}$
C	10.16	.400
D	11.18 ± 0.2	.440 ± .008
E	1.08 ± 0.15	.043 $^{+.006}_{-.007}$
F	0.7	.028
G	3.5 ± 0.2	.138 ± .008
H	2.4 ± 0.2	.094 $^{+.007}_{-.008}$
I	0.8 min	.031 min
J	2.6	.102
K	1.27 (TP)	.050 (TP)
M	0.40 ± 0.10	.016 $^{+.004}_{-.005}$
N	0.12	.005
P *	9.40 ± 0.20	.370 ± .008
Q	0.15	.006
T	0.85 rad	.033 rad
U	0.20 $^{+0.10}_{-0.05}$	.008 $^{+.004}_{-.002}$

* Item P to center of leads.

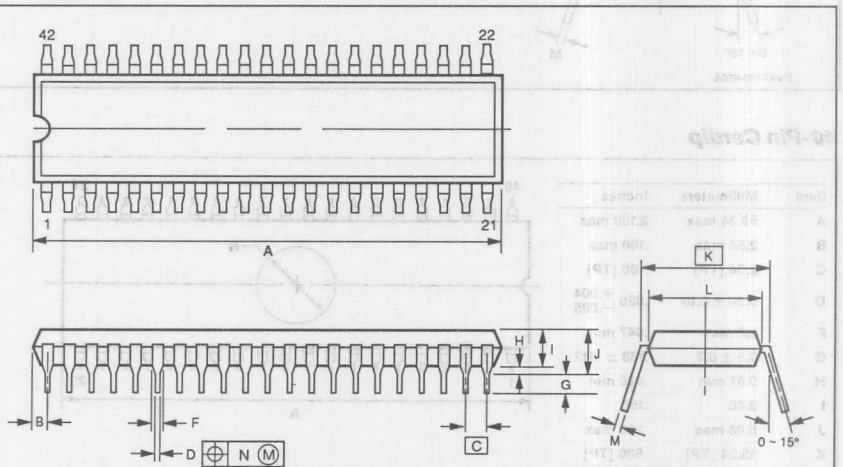


P40LE-400A

49NR-700B (5/90)

42-Pin Plastic DIP

Item	Millimeters	Inches
A	55.88 max	2.2 max
B	2.54 max	.100 max
C	2.54 [TP]	.100 [TP]
D	0.50 ± 0.10	.020 $^{+.004}_{-.005}$
F	1.2 min	.047 min
G	3.6 ±0.30	.142 ± .012
H	0.51 min	.020 min
I	4.31 max	.170 max
J	5.72 max	.226 max
K	15.24 [TP]	.600 [TP]
L	13.2	.520
M	0.25 $^{+0.10}_{-0.05}$	.010 $^{+.004}_{-.003}$
N	0.25 min	.01 min



P42C-100-600A, B

83IH-6028B (3/90)

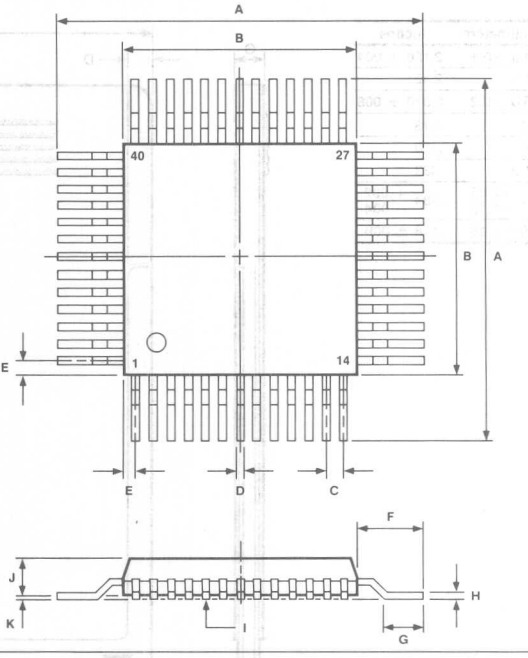
52-Pin Plastic Miniflat

Item	Millimeters	Inches
A	21.04 ± 0.4	.827 ± .016
B	14 ± 0.2	.551 $^{+.009}_{-.008}$
C	1.0 [TP]	.039 [TP]
D	0.40 ± 0.10	.016 $^{+.004}_{-.005}$
E	1.0	.039
F	3.5 ± 0.2	.138 $^{+.008}_{-.009}$
G	2.2 ± 0.2	.087 $^{+.008}_{-.009}$
H	0.15 $^{+0.10}_{-0.05}$	.006 $^{+.004}_{-.003}$
I	0.15	.006
J	2.6 $^{+0.2}_{-0.1}$	.102 $^{+.009}_{-.004}$
K	0.1 ± 0.1	.004 ± .004

Notes:

[1] Each lead centerline is located within 0.20 mm [.008 inch] of its true position [TP] at maximum material condition.

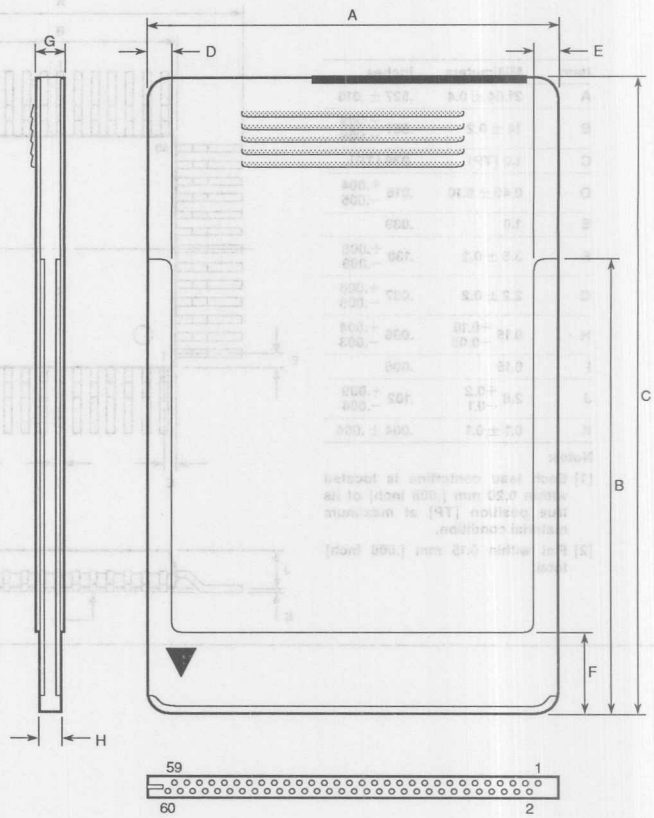
[2] Flat within 0.15 mm [.006 inch] total.



NEC

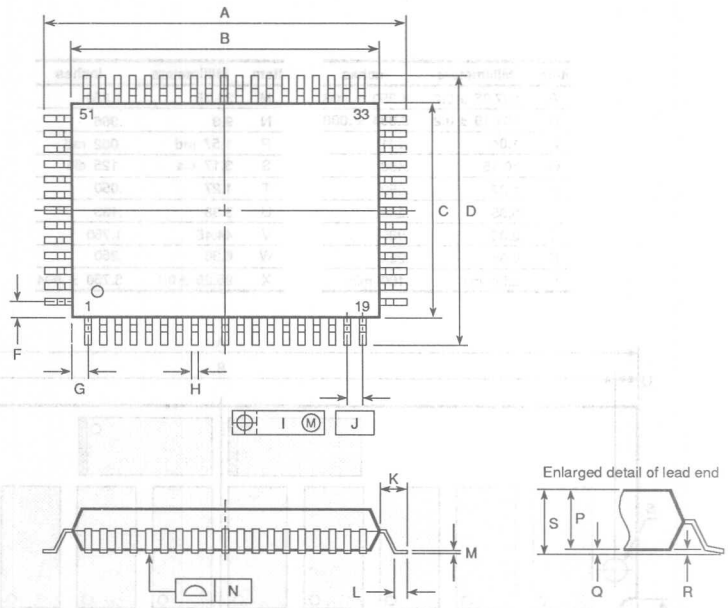
60-Pin IC Card

Item	Millimeters	Inches
A	54.0 ±0.1	2.126 ±.004
B	61.5	2.421
C	85.6 ±0.2	3.370 ±.008
D	3.0	.118
E	3.0	.118
F	11.0	.433
G	$3.4^{+0.05}_{-0.10}$	$.134^{+.002}_{-.004}$
H	3.0 ±0.15	.118 ±.006



64-Pin Plastic QFP

Item	Millimeters	Inches
A	23.6 ±0.4	.929 ±.016
B	20.0 ±0.2	.795 $^{+.009}_{-.008}$
C	14.0 ±0.2	.551 $^{+.009}_{-.008}$
D	17.6 ±0.4	.693 ±.016
F	1.0	.039
G	1.0	.039
H	0.40 ±0.10	.016 $^{+.004}_{-.005}$
I	0.20	.008
J	1.0 (TP)	.039 (TP)
K	1.8 ±0.2	.071 $^{+.008}_{-.009}$
L	0.8 ±0.2	.031 $^{+.009}_{-.008}$
M	0.15 $^{+0.10}_{-0.05}$	.006 $^{+.004}_{-.003}$
N	0.15	.006
P	2.7	.106
Q	0.1 ±0.1	.004 ±.004
R	0.1 ±0.1	.004 ±.004
S	3.0 max	.119 max



P64GF-100-3B8, 3BE

49NR-599B (9/89)

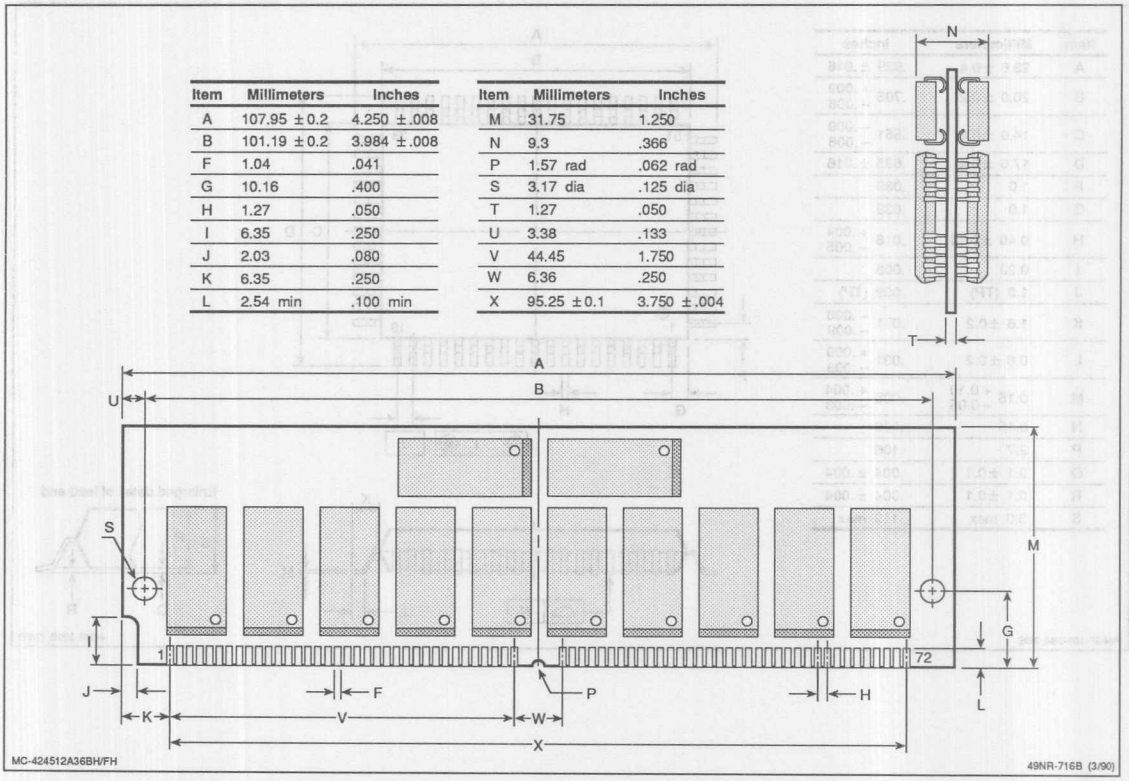
12

NEC

72-Pin SIMM (Socket Mountable) #1

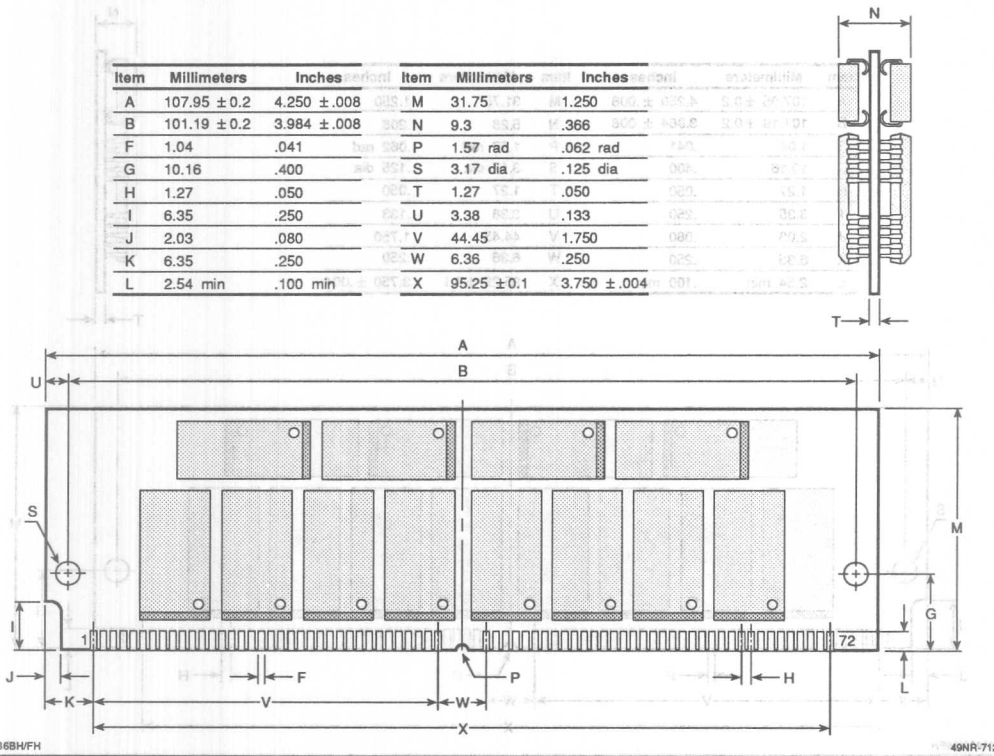
Item	Millimeters	Inches
A	107.95 ±0.2	4.250 ±.008
B	101.19 ±0.2	3.984 ±.008
F	1.04	.041
G	10.16	.400
H	1.27	.050
I	6.35	.250
J	2.03	.080
K	6.35	.250
L	2.54 min	.100 min

Item	Millimeters	Inches
M	31.75	1.250
N	9.3	.366
P	1.57 rad	.062 rad
S	3.17 dia	.125 dia
T	1.27	.050
U	3.38	.133
V	44.45	1.750
W	6.36	.250
X	95.25 ±0.1	3.750 ±.004



72-Pin SIMM (Socket Mountable) #2

Item	Millimeters	Inches	Item	Millimeters	Inches
A	107.95 ±0.2	4.250 ±.008	M	31.75	1.250
B	101.19 ±0.2	3.984 ±.008	N	9.3	.366
F	1.04	.041	P	1.57 rad	.062 rad
G	10.16	.400	S	3.17 dia	.125 dia
H	1.27	.050	T	1.27	.050
I	6.35	.250	U	3.38	.133
J	2.03	.080	V	44.45	1.750
K	6.35	.250	W	6.36	.250
L	2.54 min	.100 min	X	95.25 ±0.1	3.750 ±.004



MC-422000A36BH/FH

49NR-712B (3/90)

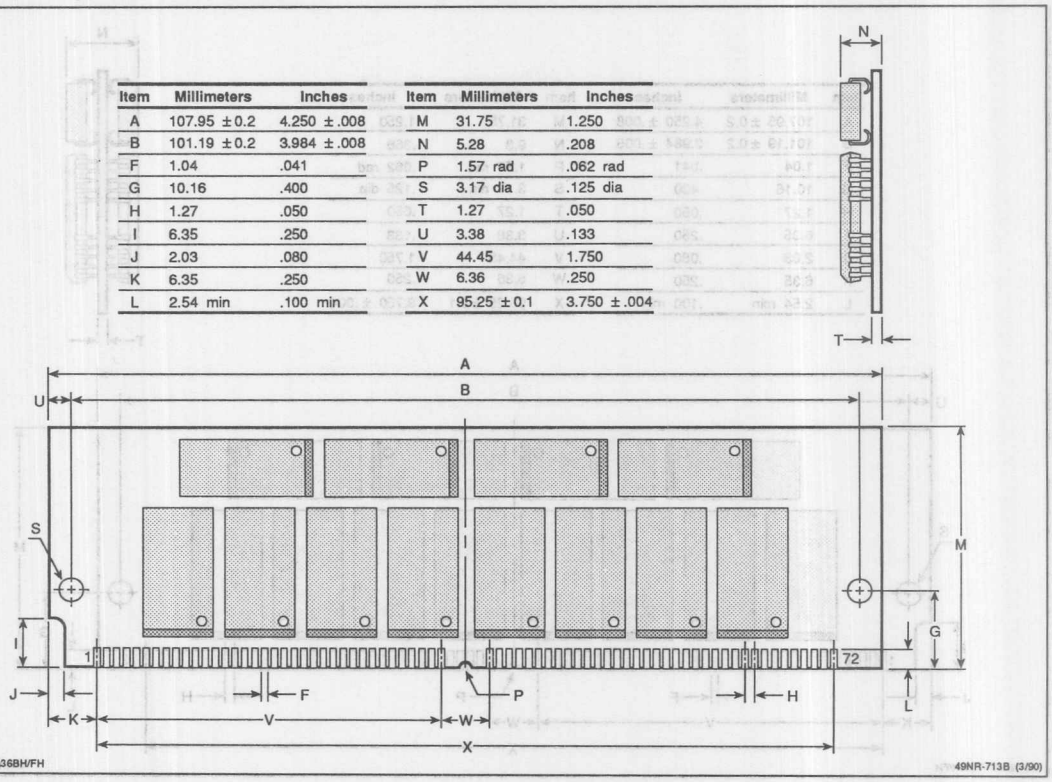
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72-Pin SIMM (Socket Mountable) #3

Item	Millimeters	Inches
A	107.95 ±0.2	4.250 ±.008
B	101.19 ±0.2	3.984 ±.008
F	1.04	.041
G	10.16	.400
H	1.27	.050
I	6.35	.250
J	2.03	.080
K	6.35	.250
L	2.54 min	.100 min

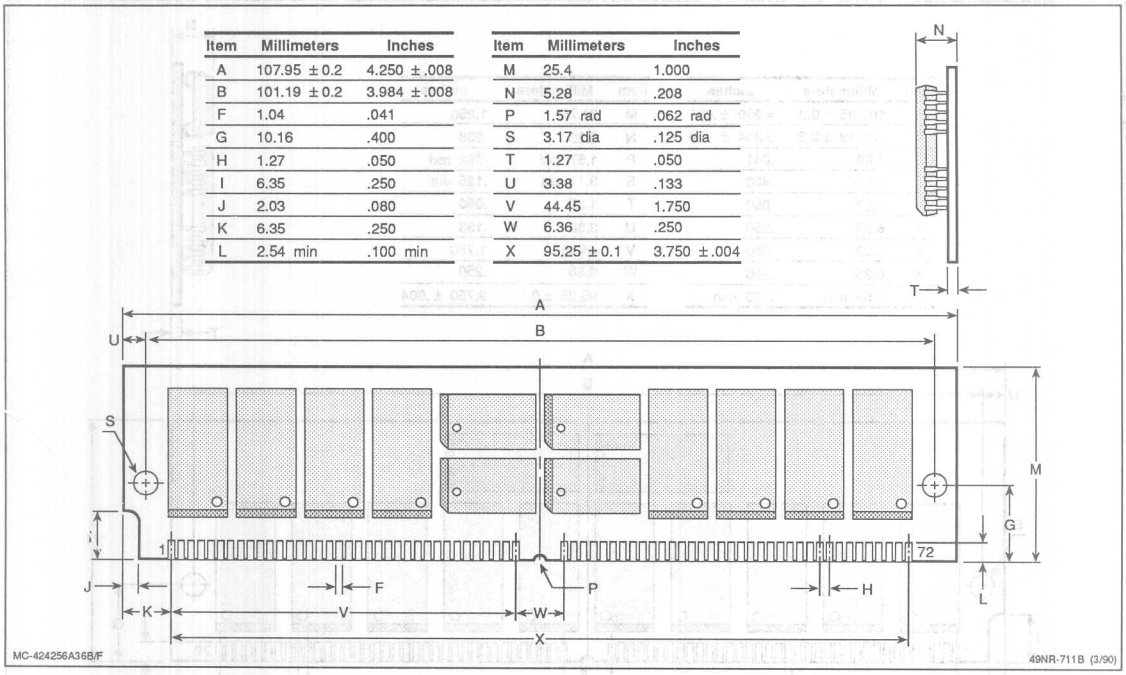
Item	Millimeters	Inches
M	31.75	1.250
N	5.28	.208
P	1.57 rad	.062 rad
S	3.17 dia	.125 dia
T	1.27	.050
U	3.38	.133
V	44.45	1.750
W	6.36	.250
X	95.25 ±0.1	3.750 ±.004



72-Pin SIMM (Socket Mountable) #4

Item	Millimeters	Inches
A	107.95 ±0.2	4.250 ±.008
B	101.19 ±0.2	3.984 ±.008
F	1.04	.041
G	10.16	.400
H	1.27	.050
I	6.35	.250
J	2.03	.080
K	6.35	.250
L	2.54 min	.100 min

Item	Millimeters	Inches
M	25.4	1.000
N	5.28	.208
P	1.57 rad	.062 rad
S	3.17 dia	.125 dia
T	1.27	.050
U	3.38	.133
V	44.45	1.750
W	6.36	.250
X	95.25 ±0.1	3.750 ±.004



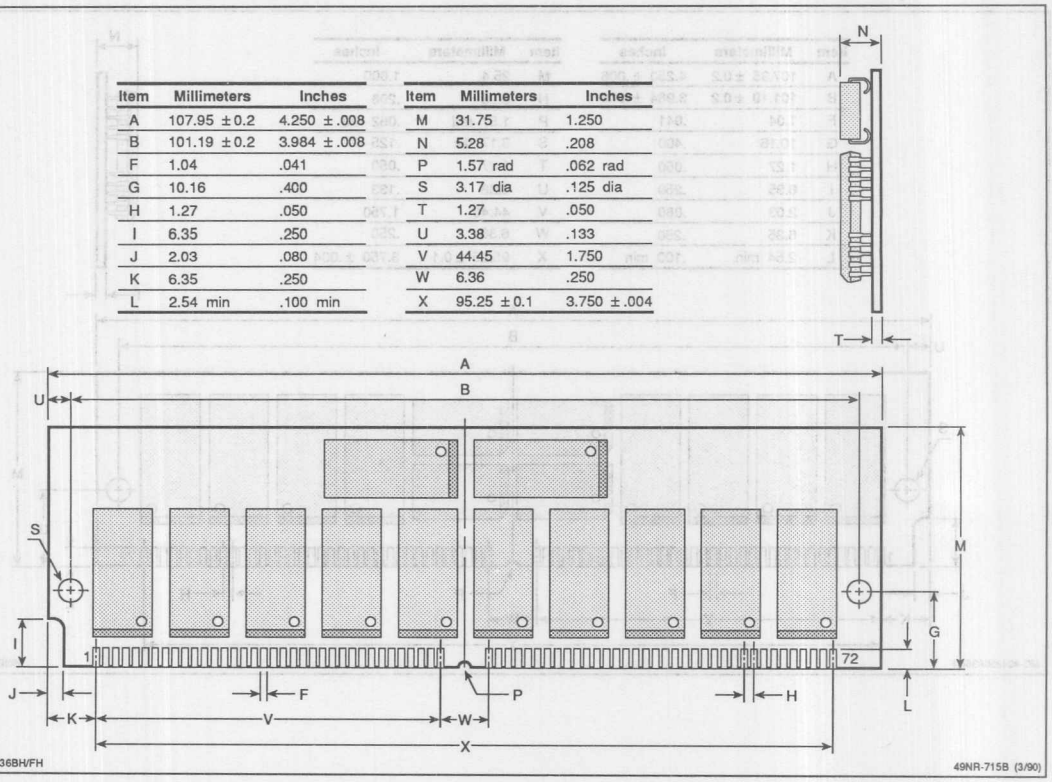
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72-Pin SIMM (Socket Mountable) #5

Item	Millimeters	Inches
A	107.95 ±0.2	4.250 ±.008
B	101.19 ±0.2	3.984 ±.008
F	1.04	.041
G	10.16	.400
H	1.27	.050
I	6.35	.250
J	2.03	.080
K	6.35	.250
L	2.54 min	.100 min

Item	Millimeters	Inches
M	31.75	1.250
N	5.28	.208
P	1.57 rad	.062 rad
S	3.17 dia	.125 dia
T	1.27	.050
U	3.38	.133
V	44.45	1.750
W	6.36	.250
X	95.25 ±0.1	3.750 ±.004



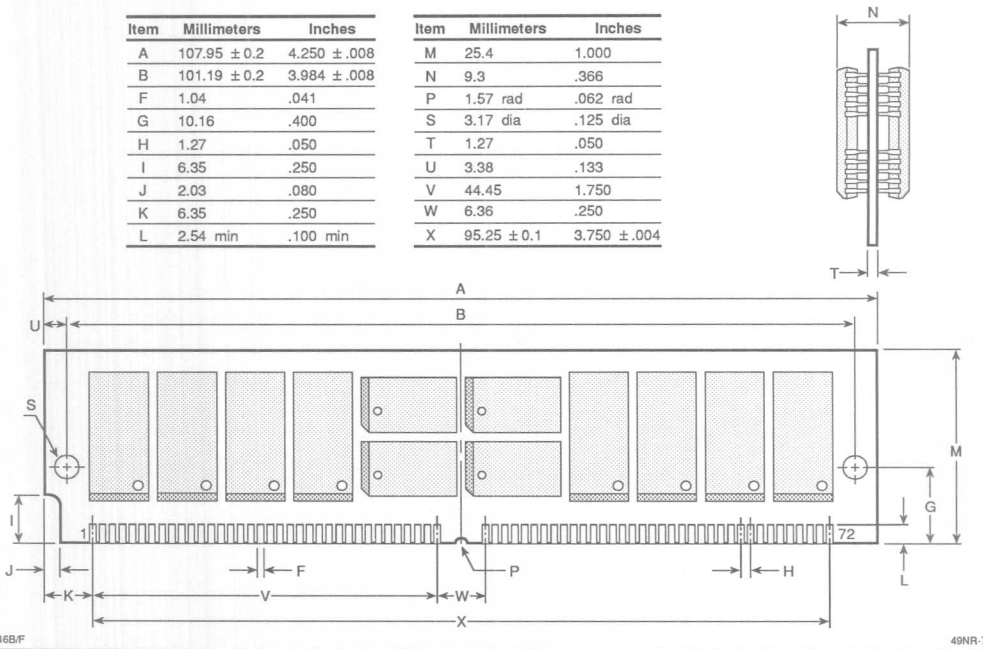
MC-424256A36BH/FH

49NR-715B (3/90)

72-Pin SIMM (Socket Mountable) #6

Item	Millimeters	Inches
A	107.95 ±0.2	4.250 ±.008
B	101.19 ±0.2	3.984 ±.008
F	1.04	.041
G	10.16	.400
H	1.27	.050
I	6.35	.250
J	2.03	.080
K	6.35	.250
L	2.54 min	.100 min

Item	Millimeters	Inches
M	25.4	1.000
N	9.3	.366
P	1.57 rad	.062 rad
S	3.17 dia	.125 dia
T	1.27	.050
U	3.38	.133
V	44.45	1.750
W	6.36	.250
X	95.25 ±0.1	3.750 ±.004



MC-424512A36B/F

49NR-710B (3/90)

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